國 立 交 通 大 學

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應用於超寬頻脈衝通訊系統之接收機前端電路設計與實現

A Front-End Receiver Design and Implementation for Impulse Radio Ultra-Wideband Communication Systems

研 究 生：謝明憲 **(Ming-Hsien Hsieh)**

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中 華 民 國 九 十 六 年 九 月

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摘 要

在本論文研究中，將針對脈衝超寬頻的低功率、低複雜度架構之特性，設計出適用於脈衝超寬頻通訊系統之接收機前端電路。首先各別設計低雜訊放大器及相關器。低雜訊放大器方面採用變壓器作輸入匹配，由於反向變壓器之電感隨著頻率增加而變小，經小訊號模型推導後發現可將此特性應用在寬頻匹配上。另外在增益級部分運用電流再利用技巧達到低功耗、高增益之特性。經量測後得到在 3.1~10.6GHz 輸入反射損耗 S11<-9.8dB，平均順向增益 S21=11.2dB，且頻帶內變異為 1.2dB。最低雜訊表現為 3.2dB。另外相關器是作為訊號偵測及解調之用，此次以吉伯特架構作時域訊號相乘，並以電感產生零點作頻寬的延伸，再加上可調增益之機制。實際量測得到輸出振幅為 36-89mV，與模擬之可調範圍有些許差距。最後我們整合前端電路在單一晶片上，其子電路包含低雜訊放大器、脈波產生器以及類比相關器三個子電路。首先雙極性之開關式二階微分高斯脈波產生器，經模擬後得到脈波寬度約為 260ps。而相關器有別於之前設計，此次乘法器是以四相位架構實現，目的是將接收後經放大的訊號與脈波產生器產生當作本地訊號作相乘，並經過在差動輸出端加上的跨接電容以完成積分，另外再串一級運算放大器，加上主極點消除技術以延

伸頻寬，由於此技術所用之電容橫跨在運算放大器的輸入輸出級上，同樣亦具有積分效果。整個接收電路經量測後適用在 110Mbps 或更高之傳輸速率上，上升時間約為 1.8ns，持續時間為 2.2ns。此高傳輸以及低功耗等特性證明可應用在超寬頻脈衝通訊系統上。

A Front-End Receiver Design and Implementation for Impulse Radio Ultra-Wideband Communication Systems

Student: Ming-Hsien Hsieh Advisor: Dr. Fu-Chiarng Chen

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ABSTRACT

In this thesis we focus on the characteristics of low power, low complex architecture and design of a front-end receiver used in IR-UWB communication systems. First of all, the LNA and correlator are designed separately. The wideband input matching of LNA is realized by the transformer feedback topology instead of multi-stage filters. Since the inductance of the inverting transformer degrades as frequency increases, this characteristic can be applied in wideband matching by means of small-signal model. As to gain stage, the current-reuse technique reduces power dissipation and obtains adequate gain simultaneously. The measured results in 3.1 to 10.6 GHz show that S11 is less than -9.8 dB, S21 is equal to 11.2 dB with 1.2 dB variation, the minimum NF is 3.2 dB. Further, the correlator used for detecting signal is realized by the Gilbert multiplier. Some mechanisms are developed for bandwidth extension and dynamic gain control. The practical measurement shows that the output amplitude is 36-89mV. The adjustable range is slightly different from that in simulation. Finally, the integrated front-end receiver is proposed. The single chip comprises three sub-blocks including a wideband LNA, a pulse

generator, and an analog correlator. The bi-phase, switched, 2nd derivative pulse generator can generate the pulse width of 260ps. The analog correlator is modified and different from the previous design. It utilizes a four-quadrant multiplier and integral capacitors to implement the design. Besides, we exploit zero-pole cancelling topology to reach bandwidth enhancement and doubly integration simultaneously. The whole front-end receiver can work functionally in 110Mb/s, and the rise time and hold time of the demodulated signal are about 1.8ns and 2.2ns, respectively. The features prove that it is suitable in IR-UWB communication systems.

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FIGURE CAPTIONS

TABLE CAPTIONS

Chapter 1

Introduction

1.1 Motivation

Ultra-wideband (UWB) technology has been proposed since the 1980s [1][2], but mainly used for radar-based applications due to recent developments in high speed switching technology, UWB is becoming more attractive for low cost consumer communications applications. UWB systems allow to overlay existing narrowband systems, and result in a much more efficient use of the available spectrum. Therefore, the Federal Communications Commission (FCC) has allocated 7500MHz of spectrum for unlicensed use of ultra-wideband devices in the 3.1 to 10.6GHz frequency band. UWB is emerging as a solution for the IEEE 802.15.3a (TG3a) standard [2]. This standard is provided as a specification for a low complexity, low cost, low power consumption, and high data rate wireless connectivity among devices around the personal operating space. The data rate must be high enough (greater than 110Mb/s) to satisfy a set of consumer multimedia industry needs for wireless personal area networks (WPAN) communications, and the standard also addresses the quality of service (QoS) capabilities required to support multimedia data streams.

In this thesis, we put emphasis on the front-end receiver design of impulse-radio UWB communication system, which is implemented and fabricated by the standard TSMC 0.18μm CMOS process. First, we design a wideband low-noise amplifier. Then a correlator used for demodulating the received signal is implemented for applying in UWB receiver. Finally we will integrate the overall blocks of front end in a chip. Design methodologies, simulation and measurement results would present in this thesis in detail.

1.2 Thesis Organization

The organization of this thesis is overviewed as follows:

In Chapter 2, we will introduce the overview of ultra-wideband system. Two possible approaches are introduced in brief at the section, and we pay attention to impulse-radio UWB system. Some relations about definition, features, pulse shaping, modulation, and several receiver architectures will be presented in the chapter.

In Chapter 3, we start to design circuits used in UWB systems, concluding a low-power LNA with the transformer-feedback matching network and an analog correlator with variable gain control. Individual design concepts, simulation and measured results would be presented in detail. Eventually we also make short discussion and conclusion in each circuit.

In Chapter 4, based on the previous circuits, we propose a novel front-end receiver circuit design of impulse-radio UWB system. In this chapter, the architecture of the proposed receiver and principles of circuit design and even layout consideration will be presented. Furthermore, the integrated circuit has been fabricated and the measured results are exhibited in the chapter.

In Chapter 5, conclusions and future work are presented.

Chapter 2

Ultra-Wideband Communication System

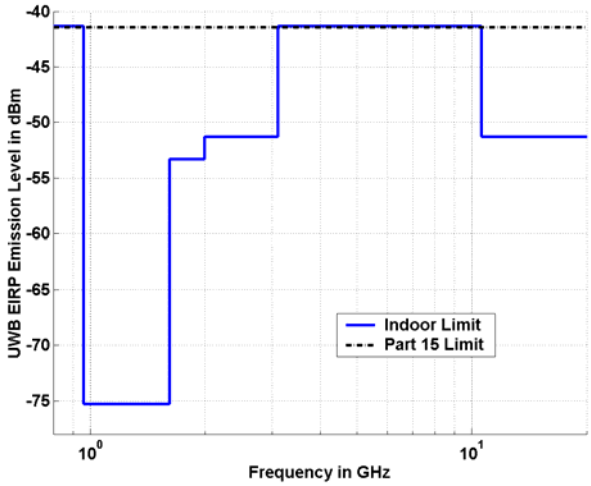
2.1 Introduction

The FCC issued in February 2002, allocated 7500MHz of spectrum for unlicensed use of UWB devices in the 3.1 to 10.6 GHz frequency band. The FCC defines UWB as any signal that occupies more than 500MHz bandwidth in the 3.1 to 10.6 GHz band and that meets the spectrum mask shown in Fig.2-1. This is by far the largest spectrum allocation for unlicensed use the FCC has ever granted. It is even more relevant that the radiation power is relatively low. A comparison with the other unlicensed bands currently available and used in United States is shown in Table 2-1. This allocation opens up new possibilities to develop UWB technologies different from older approaches based on impulse radios. This novel wireless short range communicative specification is deserved to expect.

Two proposals detailing the operation of UWB devices are being considered. One is multi-band orthogonal frequency division multiplexing (MB-OFDM) [3] and the other is direct sequence spread spectrum (DSSS) [4]. We will make a brief introduction in each approach as following.

MB-OFDM UWB

The Multiband OFDM Alliance (MBOA) standard for UWB communications draws heavily upon prior research in wireless local area network (WLAN) systems. In a manner similar to IEEE 802.11a/g, MBOA partitions the spectrum from 3 to 10 GHz into several 528-MHz bands and employs OFDM in each band to transmit data rates as high as 480Mb/s. A significant departure from the original principle of “carrier-free”



Radiation limits	
Frequency range(MHz)	EIRP (dBm/MHz)
960-1610	-75.3
1610-1900	-53.3
1900-3100	-51.3
3100-10600	**-41.3**
10600 up	-51.3

Figure 2-1 UWB spectrum mask for indoor communication systems

Table 2-1 U.S. spectrum allocation for unlicensed use

Unlicensed bands	Frequency of operation	Bandwidth
ISM at 2.4 GHz	2.4000-2.4835 GHz	83.5 MHz
U-NII at 5 GHz	5.15-5.35 GHz 5.75-5.85 GHz	300 MHz
UWB	3.1-10.6 GHz	7500 MHz

signaling, the multiband operation is chosen to both simplify the generation and detection of signals and achieve well-established OFDM solutions from WLAN systems. To ensure negligible interference with other existing standards, the FCC has limited the output power level of UWB transmitters to 41.3 dBm/MHz.

Fig.2-2 shows the plan of the MB-OFDM bands and the channelization within each band. The 14 bands span the range of 3168 MHz to 10560 MHz. In contrast to IEEE 802.11a/g, MB-OFDM employs only QPSK modulation in each sub channel to allow low resolution in the baseband analog-to-digital (A/D) and digital-to-analog (D/A) converters. Usually, bands 1-3 constitute “Mode 1” and are mandatory for operation

whereas the remaining bands are envisioned for high-end products [5].

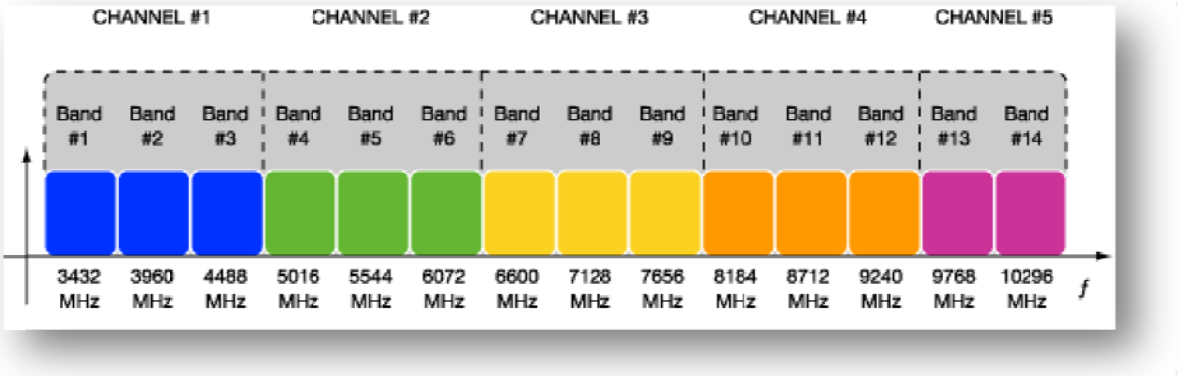


Figure 2-2 Multi-band OFDM frequency band plan

DS-UWB (DSSS)

DS-UWB uses a combination of a single-carrier spread-spectrum design and wide coherent bandwidth. The UWB Forum, an industry organization focusing on DS-UWB design and application, says it provides low-fading, optimal interference characteristics, inherent frequency diversity and precision ranging capabilities. Recently, dual-band of DS-UWB systems is suggested to avoid the interference with narrow band systems between 5.15GHz and 5.825GHz. The DS-UWB system utilizes the dual band, one is the low band (LB) from 3.1GHz to 5.15GHz and the other is the high band (HB) from 5.825GHz to 10.6GHz. The illustration is shown in Fig.2-3.

Unlike conventional wireless systems which use narrowband modulated carrier waves to transmit information, DS-UWB transmits data with pulses at very high rates. A fixed UWB chip rate in conjunction with variable-length spreading code words enables this scalable support. By using the widest possible bandwidth to produce the shortest possible pulses, DS-UWB supports robust, high-data-rate links in a high multipath environment and offers precise spatial resolution for location detection of UWB devices.

Furthermore, DS-UWB provides four key advantages over other wireless technologies: quality of service; high data rates that scale to 1 Gbit/sec or more; lower cost; and longer battery life. That the technology reduces implementation complexity while allows increased scalability, makes it ideal for applications such as high-rate data transmission and power-constrained handheld devices. These attributes mean DS-UWB is well suited to be the physical layer for PANs.

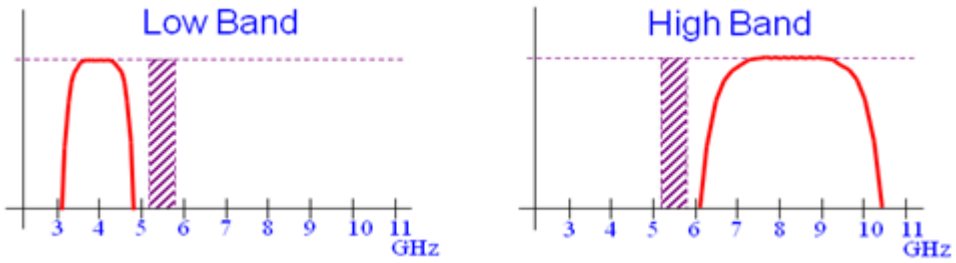


Figure 2-3 DS-UWB operating band (a) low band (b) high band

2.2 Impulse-Radio UWB Communication System

2.2.1 Definition

FCC provides the following definitions for UWB operation [6], and the illustration is shown in Fig.2-4.

(a) *UWB bandwidth*

The UWB bandwidth is the frequency band bounded by the points that are 10 dB below the highest radiated emission, as based on the complete transmission system including the antenna. The upper boundary is designated f_H and the lower boundary is designated f_L.

(b) *Center frequency*

The center frequency, f_c, equals $(f_H + f_L)/2$.

(c) *Fractional bandwidth*

The fractional bandwidth equals $2(f_H - f_L)/(f_H + f_L)$.

(d) *Ultra-wideband (UWB) transmitter*

An intentional radiator that, at any point in time, has a fractional bandwidth equal to or greater than 20% or has a UWB bandwidth equal to or greater than 500 MHz, regardless of the fractional bandwidth.

(e) Equivalent isotropically radiated power (EIRP)

The product of the power supplied to the antenna and the antenna gain in a given direction relative to an isotropic antenna. At UWB specification, the signal of 3.1 to 10.6 GHz frequency allocation cannot exceed -41.3dBm/MHz of power spectral density (PSD).

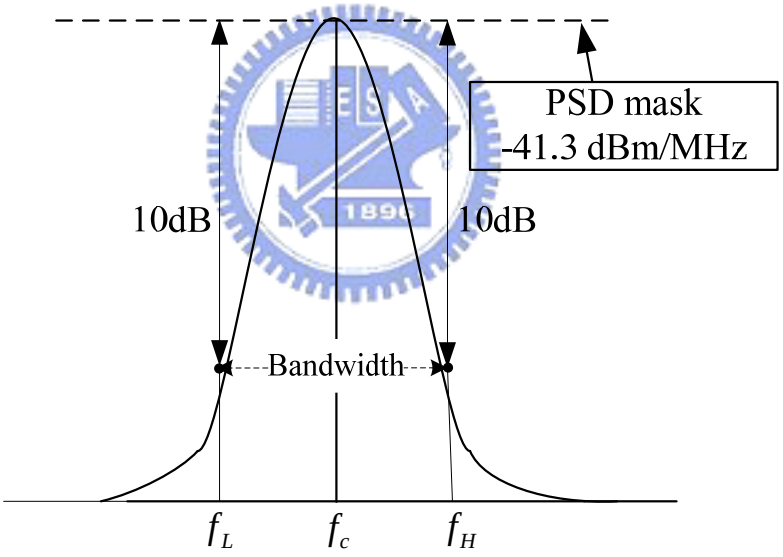


Figure 2-4 Illustration of UWB

Generally speaking, IR-UWB specification is similar to DS-UWB. The reason is that they both transmit data by pulses. However they still have slight difference in sub-channel allocation. DS-UWB system is divided into high band and low band for avoiding the interference with narrow band communication systems. Therefore, IR-UWB use very short pulses which occupy the almost entire band (3~10 GHz) for

high data rate and average power degradation. In this thesis we focus on IR-UWB and design receiver block circuits suited in IR-UWB system.

2.2.2 Features and Advantages

UWB has a lot of advantages that make it attractive for consumer communications applications [7,8]. In particular, IR-UWB systems owns the advantages of

(1) High-data transmission rate

According to channel capacity formula, (i.e. $C = B \times \log_2(1 + \frac{S}{N})$), the data capacity (C) is proportional to channel bandwidth (B). In terms of 7.5 GHz of UWB bandwidth, the transmission rate can reach in 110Mbit/s if the range is less than 10m and up to 480Mbit/s if less than 2m. It is an ideal technology for realizing wireless personal area network (WPAN) systems. In addition, UWB systems coexist with other communication systems band instead of occupying crowded and expansive frequency bands arbitrarily.

(2) Low power consumption

UWB system delivers data by discrete-impulse instead of continuous sinewave, and the hold time of impulse is very short. Compare with continuous-signal of conventional communication system, impulse radio system can achieve ultra low power consumption. The consumption of UWB is only 1/100 of traditional mobile phone, and 1/20 of Bluetooth equipments. Therefore, impulse radio UWB system is superior to typical wireless system concerning battery life and electromagnetic radiation.

(3) Low cost and low complex architecture

Unlike conventional radio system, the UWB transmitter produces a very short time domain pulse, which is able to propagate without the need for an additional RF mixing stage. The signal will propagate well without any additional up-conversion. The reverse

process of down-conversion is also not required in the UWB receiver. In other words, one of the greatest benefits of UWB architecture compared to continuous-wave one is that there is no need for complex circuits such as the power amplifier and frequency synthesizer, and these are the most complex components of conventional architecture. In addition, UWB will have potential of low cost if circuits are integrated in single chip by CMOS process.

(4) High security

Due to the low energy density and the pseudo-random (PR) characteristics of the transmitted signal, the UWB signal is noiselike, which makes unintended detection quite difficult. If the transmitted signal collocates with pseudo-random noise sequence for coding, the receiver must have the accurate transmitter's pulse sequence. As a result, it can get the right signal from the transmitter, and the impulse radio therefore has high security in data transmission.

(5) High positioning resolution

Due to the characteristic of very narrow impulse, IR-UWB is easy to combine with positioning system and communication system. Moreover, the narrow-impulse has robust penetration, which can apply in precision position in door or below ground. Compared to general global position system (GPS) mechanism which only works in visible range of the positioning satellite, impulse radio can achieve an accurate scale of centimeter.

(6) Multi-path capacity

The radio signal of the conventional wireless communication mostly adopts continuous-wave, and the sustained time is far longer than multi-path propagation time. So multipath effect limits the quality of service and data rate and causes channel distortion. Besides, traditional receivers deal with multi-path signal by rake receivers. When multipath effect becomes more serious, the circuits' complexity, power, and

storage requirements are potentially higher. However, the emission of impulse-radio UWB is narrow impulse, which can directly be decomposed in multipath without interference. It is suitable in multi-path signal processing.

2.3 Pulse Shaping

In impulse-radio UWB, it delivers data by very short pulses. Different kinds of pulse would affect the spectrum distribution [9]. In this section we will introduce some pulses and each spectrum used in UWB system.

(1) Gaussian pulse

As shown in Fig.2-5, Gaussian pulse is the common waveform in impulse communication. The mathematic equation is

$$w(t) = Ae^{-[(t-Tc)/Tau]^2} \tag{2-1}$$

where A is amplitude, T_c is the pulse width, and T_{au} is the parameter about pulse forming, or called pulse shape parameter, which is mainly in the adjustment of central frequency and bandwidth of signal. This spectrum allocation has large DC component and the central frequency is close to low band.

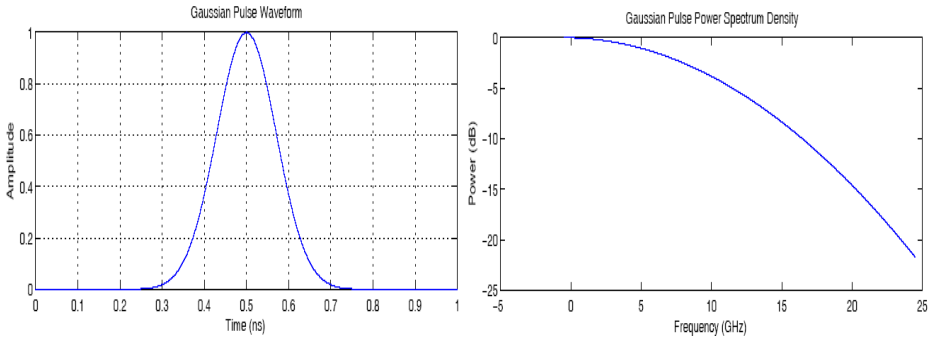


Figure 2-5 Gaussian pulse and spectrum allocation

(2) Gaussian monocycle

As shown in Fig.2-6, Gaussian monocycle is the 1st derivative form of Gaussian

pulse. It can be observed that the central frequency moves toward higher band. However, it still cannot satisfy the spectrum mask of UWB. The mathematic equation is

$$w(t)=2\times\frac{A}{Tau}\times\sqrt{e}\times(t-Tc)\times e^{-2\times[(t-Tc)/Tau]^2} \tag{2-2}$$

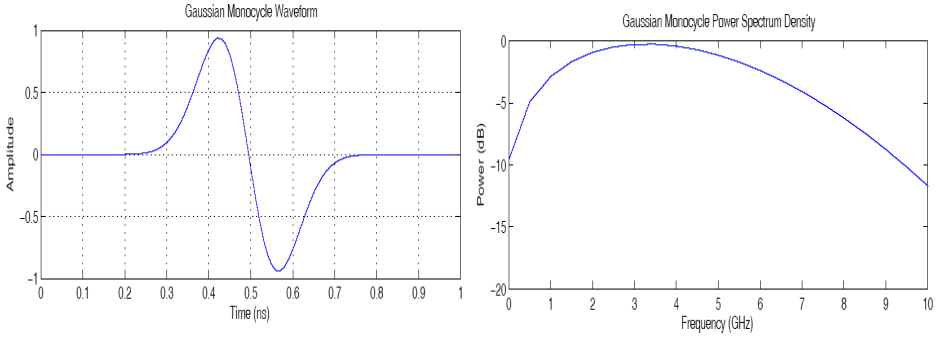


Figure 2-6 Gaussian monocycle and spectrum allocation

(3) Scholtz's monocycle

As shown in Fig.2-7, the waveform was presented initially in [10] by Dr. Scholtz. This pulse approximates the 2nd derivative form of Gaussian pulse, and the mathematic equation is

$$w(t)=A[1-4\pi(\frac{t-Tc}{T_{au}})^2]e^{-2\pi(\frac{t-Tc}{T_{au}})^2} \tag{2-3}$$

We can observe the spectrums of these three kinds of pulse above. Gaussian pulse has more DC components, which would degrade the efficiency of antenna radiation. The 2nd derivative of Gaussian pulse (or Scholtz's monocycle) has wider 3dB bandwidth and fewer components in low band. This pulse occupies much bandwidth under UWB specific mask and be appropriate in the waveform of impulse radio UWB.

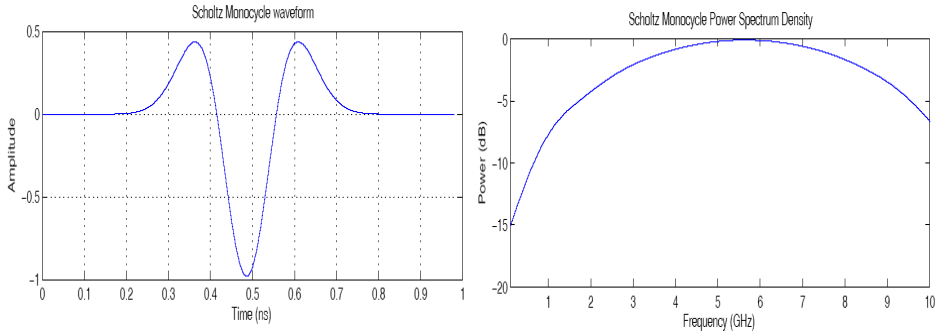


Figure 2-7 Scholtz's monocycle and spectrum allocation

(4) Higher-order derivatives of Gaussian pulse

Higher-order derivatives of Gaussian pulse indicate that the derivative order is higher than three. Although more derivative orders cause the central frequency toward high frequency [11], as shown in Fig.2-8, but the circuit architecture becomes more complex to realize the high-order pulse. Furthermore, signal processing in receiver is very difficult. In practical, we select 2nd-order derivative Gaussian pulse as the signal of the receiver design in the thesis.

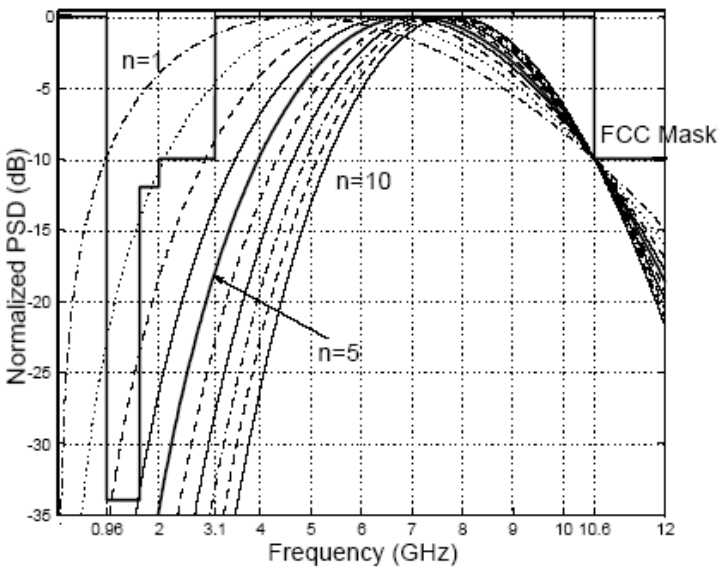


Figure 2-8 Spectrum allocations of higher-order derivatives of Gaussian pulse

2.4 Pulse Modulation

Information can be encoded in a UWB signal in a variety of methods. The most popular modulation schemes developed to date for UWB are pulse-position modulation (PPM), on-off keying (OOK), pulse-amplitude modulation (PAM) and binary phase-shift keying (BPSK), which also is called biphase. Other schemes have been selected by various groups to meet the different design parameters for different applications. We will make a brief explanation in each modulation method as follows.

PAM (or OOK)

PAM is based on the principle of encoding information with the amplitude of the impulses, as shown in Fig.2-9. The picture shows a two-level modulation, respectively. The difference is that bit 0 is presented by zero and lower amplitude, where one bit is encoded in one impulse. As with pulse position, more amplitude levels can be used to encode more than one bit per symbol.

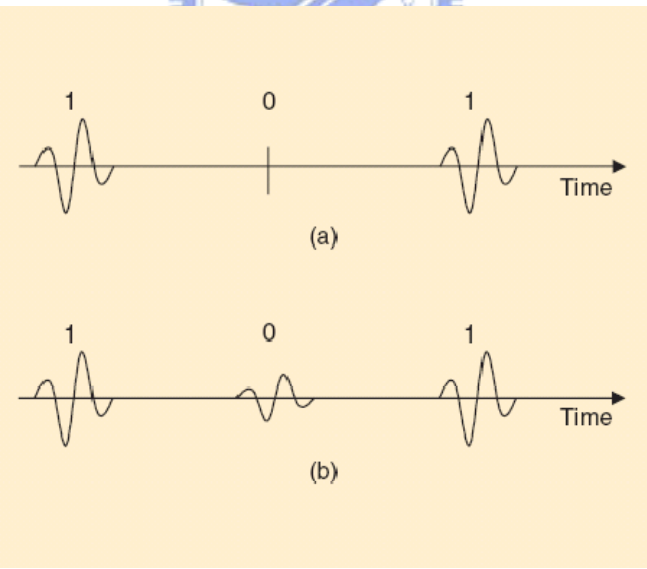


Figure 2-9 (a) OOK (b) PAM

BPSK (Biphase)

In biphase modulation, information is encoded with the polarity of the impulses, as shown in Fig.2-10. The polarity of the impulses is switched to encode a 0 or a 1. In this

case, only one bit per impulse can be encoded because there are only two polarities available to choose from.

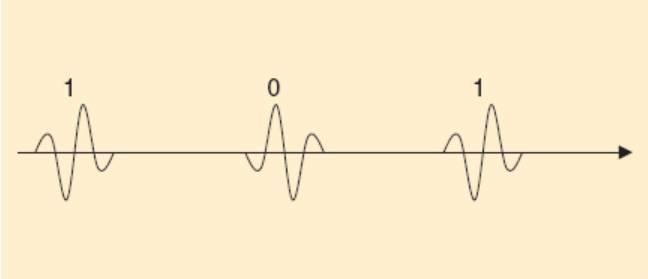


Figure 2-10 BPSK

PPM

PPM is based on the principle of encoding information with two or more positions in time, referred to the nominal pulse position, as shown in Fig.2-11. A pulse transmitted at the nominal position represents a 0, and a pulse transmitted after the nominal position represents a 1. The picture shows a two-position modulation, where one bit is encoded in one impulse. Additional positions can be used to provide more bits per symbol. The time delay between positions is typically a fraction of a nanosecond, while the time between nominal positions is typically much longer to avoid interference between impulses.

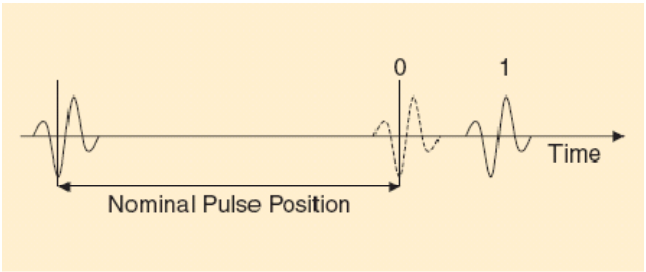


Figure 2-11 PPM

Additionally, combining with PPM and random-time hopping code can flat the spectrum of signals. It also mitigates multi-path effect and interference between clients. As a result, it accomplishes UWB time-hopping system for multiple-user case. The

transmitted signal for single user is coding by pseudo random code (PR code) to control the pulse position in each frame. The equation of time-hopping PPM can be presented as [7]

$$S_{tr}^{(k)}(t^{(k)}) = \sum_{j=-\infty}^{\infty} w_{tr}\left(t^{(k)} - jT_f - c_j^{(k)}T_c - \delta d_{(j/N_s)}^{(k)}\right) \qquad (2\text{-}1)$$

where $S_{tr}^{(k)}(t^{(k)})$ is the transmitted signal of k-th user, w_{tr} is the transmitted pulse, T_f is pulse repetition time, which also be called time frame width. For fixed T_f, symbol rate (R_s) can be represented as $R_s = 1/N_s T_f$. It can be observed that if time frame width keeps fixed, the transmission rate would decrease. $c_j^{(k)}$ represents the time-hopping sequence of k-th user's own, which is decided by PR code. T_c is the chip rate. δ is the parameter of pulse position modulation, which can be changed for optimal modulated efficiency. $d^{(k)}$ indicates the binary data.

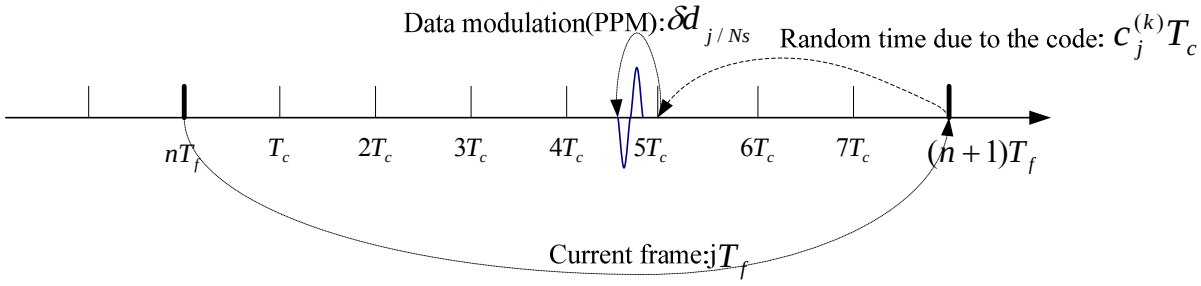


Figure 2-12 Graphic form of time-hopping pulse position modulation

2.5 IR-UWB Receiver

The main characteristic of UWB impulse radios is that very low emission power density can be achieved by spreading the energy of short-time pulses in wideband. These radios present the advantage of not requiring up/down conversion of frequency,

which results in reduced complexity and low cost of manufacturing. According to the demodulated method, IR-UWB receivers can be divided into two architectures: coherent receiver and non-coherent receiver. Coherent receivers, as shown in Fig.2-13, rely on the correlation of the received pulses and a local template demand complex implementations [12,13]. Because of short pulse adoption and known position, it has some advantages of high data rate and high SNR. Unfortunately, it needs precision timing synchronization between transmitter and receiver ends. Generally the requirement is realized by delay lock loop (DLL) circuits to achieve synchronization. On the other hand, the non-coherent receiver shown as Fig.2-14 requires neither pulse synchronization nor estimation of the shape of the incoming pulses. Instead, it recovers the energy of the pulses during a symbol time and compares it to the noise level in order to determine the presence or absence of a symbol [14]. The main drawback of using this kind of detector is that the UWB pulses cannot be detected when the signal-to noise ratio (SNR) is very low, and hence, it cannot make use of the processing gain that spread spectrum systems have. Accordingly, the non-coherent impulse receiver will only work properly when the SNR is above a threshold which is close to the noise level. Due to the very limited power that is allowed in the UWB transmitter, this only occurs at very short distances.

As to sensitivity, the BER vs. SNR curves of a non-coherent receiver is simulated and compared to that of a coherent receiver using BPSK modulation [14]. The simulation results are presented in Fig.2-15. Both simulations are executed for 10, 25, 50, and 100 Mbps using a pulse rate of 100MHz. The monocycles pulses are shaped to use the low part of the UWB spectrum 3.1GHz-5GHz. As expected, the coherent receiver presents processing gain and hence requires less SNR than the non-coherent receiver for a fixed BER. In addition, the simulation shows that the non-coherent receiver can still detect the UWB pulses for SNR close 0 dB.

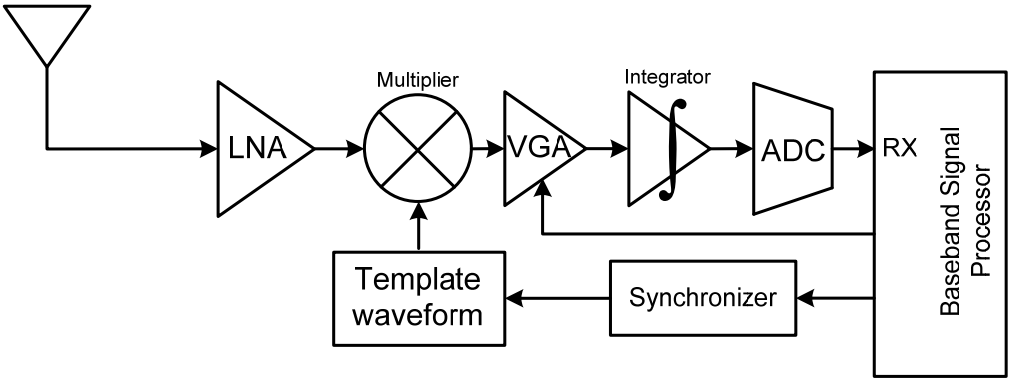


Figure 2-13 Architecture of the coherent receiver

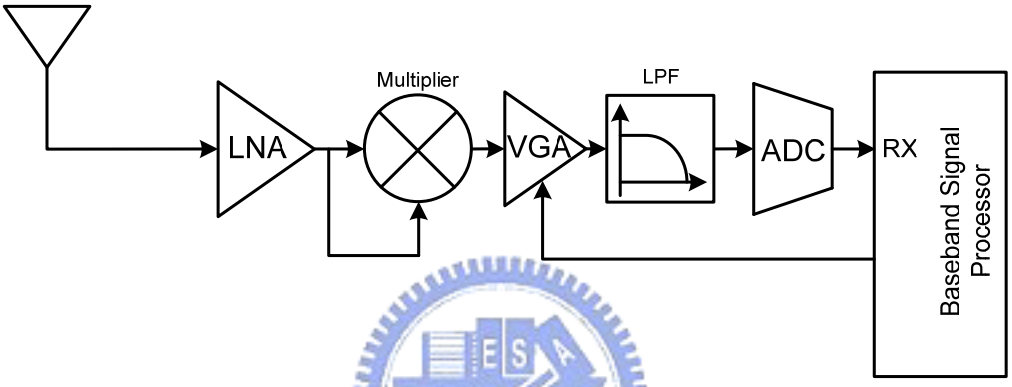


Figure 2-14 Architecture of the non-coherent receiver

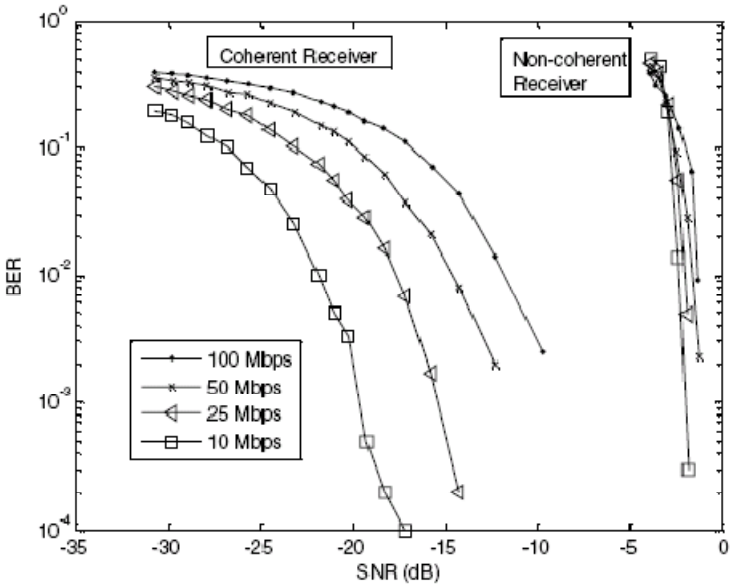


Figure 2-15 Performance curves of a non-coherent receiver and a coherent receiver using BPSK modulation

Chapter 3

Design of the Ultra-wideband LNA and Correlator

3.1 Overview

In this chapter we propose two circuits, which can apply in the front-end receiver of impulse-radio UWB system. The first one is a UWB LNA with transformer-feedback matching network. It employs the characteristic of the transformer to achieve good input matching and noise performance. Subsequently, the correlator with dynamic gain control has presented. In addition, the wide bandwidth is achieved by canceling the dominant pole at the internal node with the zero introduced by the shunt inductor at the loading stage. These circuits have been fabricated by TSMC 0.18μm 1P6M CMOS technology. We also exhibit the simulation and measurement results of each circuit.

3.2 A UWB LNA with Transformer Feedback Matching Network

In this section we propose another UWB LNA design method. It utilizes transformer feedback for wideband matching and noise degradation. First, the general monolithic transformer prototype is introduced. Then we analysis different kinds of transformer and list each advantages and disadvantages. Then we demonstrate that the design concepts in the proposed UWB LNA in detail. Subsequently, we show the simulation and measured results. Finally, the differences between the simulation and measured results are discussed.

3.2.1 Introduction of Monolithic Transformers

Transformers have been used in radio frequency (RF) circuits since the early days of telegraphy. Recent works have shown that it is possible to integrate passive

transformers in silicon IC technologies because of useful performance characteristics [15,16,17]. In general, the operation of a passive transformer is based upon the mutual inductance between two conductors. Basically, the transformers are used for the following three different functions.

1. *Impedance matching*: depending on the number of windings, the transformer has the property to change the impedance of the primary or secondary when measuring from the opposite port.
2. *Balun*: balanced to unbalanced conversion and vice versa
3. *DC isolation*: obtained with the magnetic (nonelectric) connection between the primary and secondary

Fig.3-1(a) summarizes the basis of an ideal transformer where the primary self-inductance L_1 and the secondary self-inductance L_2 are characterized with ideal inductors. The mutual inductance is represented by M, the primary and secondary currents and voltages are i_1, i_2, v_1, and v_2, and the primary and secondary winding numbers are N_1 and N_2, respectively. The coupling factor k is defined by M, L_1, and L_2 and represents the energy transmitted from the primary port to the secondary port [18,19].

The behavior of the ideal transformer in Fig.3-1(a) is ruled by its characteristic equations

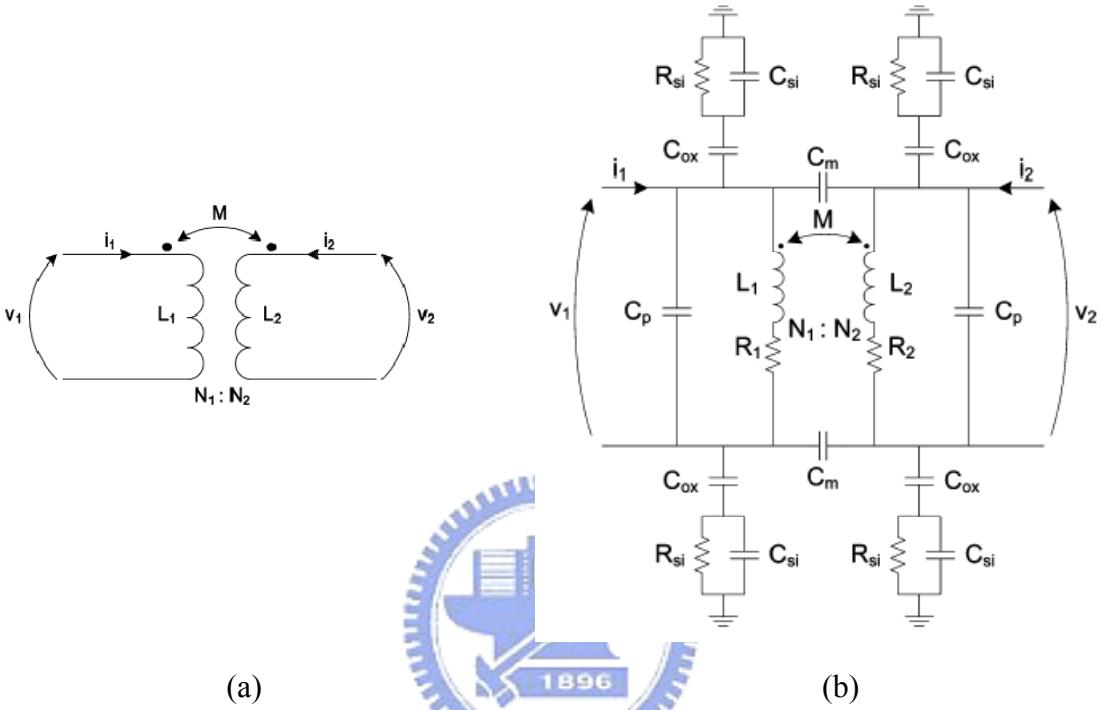
$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} j\omega L_1 & M \\ M & j\omega L_2 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \tag{3-1}$$

$$\frac{v_1}{v_2} = \frac{i_2}{i_1} = \frac{N_1}{N_2} = n \tag{3-2}$$

$$k = \frac{M}{\sqrt{L_1 L_2}} \leq 1 \tag{3-3}$$

When transformers are applied in silicon ICs, the ideal model cannot be easily establish

because of substrate loss and parasitic effects. Thus, the electrical model of an integrated transformer must be redefined, and the equivalent model of an integrated transformer is shown in Fig.3-1(b).



(a) (b)

Figure 3-1 (a) Electrical model for an ideal transformer (b) Equivalent circuit of an integrated transformer

where R_1 and R_2 represent the ohmic losses due to the resistivity of the inductor metal tracks; C_p is the capacitive coupling caused by the voltage difference between the turns in the same metal, which form a spiral; C_m represents the capacitive coupling caused by the voltage difference between the turns of the primary and secondary spirals; C_{ox} is the capacitive coupling between the metal used for each inductor and ground; C_{si} and R_{si} represent the coupling and ohmic losses due to the conductive substrate.

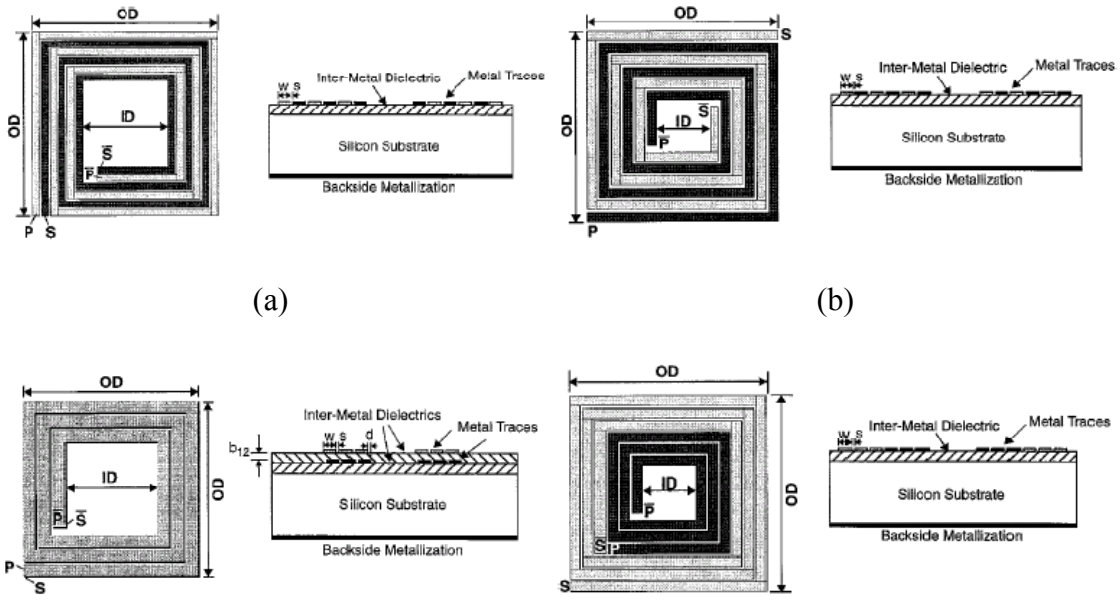


Figure 3-2 Monolithic transformer winding configurations (a) Parallel conductor winding (b) Interwound winding (c) Overlay winding (d) Concentric spiral winding

A monolithic transformer is constructed using conductors interwound in the same plane or overlaid as stacked metal layers, as shown in Fig.3-2(a). The type of parallel conductor winding is interwound to promote edge coupling of the magnetic field between windings. The primary and secondary windings lie in the same plane, as illustrated in the cross-section at the right of Fig.3-2(a). Because of the asymmetric characteristic, the ratio of transformer turns is not unity.

As shown in Fig.3-2(b), the type of interwound winding has feature of symmetry. It ensures that electrical characteristics of primary and secondary are identical when they have the same number of turns. Another advantage of this design is that the transformer terminals are on the opposite sides of the physical layout, which facilitates connections to other circuits.

Integrated transformers with multiple conductor layers are illustrated in Fig.3-2(c). The overlay winding utilizes both edge and broadside magnetic coupling to reduce the

overall area required in the physical layout. Flux linkages between the conductor layers can be improved as the intermetal dielectric is thinned. In addition, there is a large parallel-plate component to the capacitance between windings due to the overlapping of metal layers, which limits the frequency response.

Transformers can also be implemented using concentrically wound planer spirals as shown in Fig.3-2(d). The periphery between the two windings is limited to just a single turn. Therefore, mutual coupling between adjacent conductors contributes mainly to the self-inductance of each winding and not to mutual inductance between the windings. As a result, the concentric spiral transformer has less mutual inductance and more self-inductance than other types. This kind of low ratio of mutual inductance to self-inductance is useful in applications such as high-performance broadband amplifiers.

The four kinds of monolithic transformers above are summarized in Table 3-1. We can select an appropriate type for an specific design. For instance, when designing an amplifier for UWB, we can use the type of concentric spiral winding for achieving wideband response.

Table 3-1 Comparison of differential transformers

Transformer type	Coupling coefficient	L_{Self}	f_{SR}
Parallel conductor winding	Middle	Low	High
Interwound winding	Middle	Low	High
Overlay winding	High	High	Low
Concentric spiral winding	Low	Middle	High

3.2.2 Design Concepts

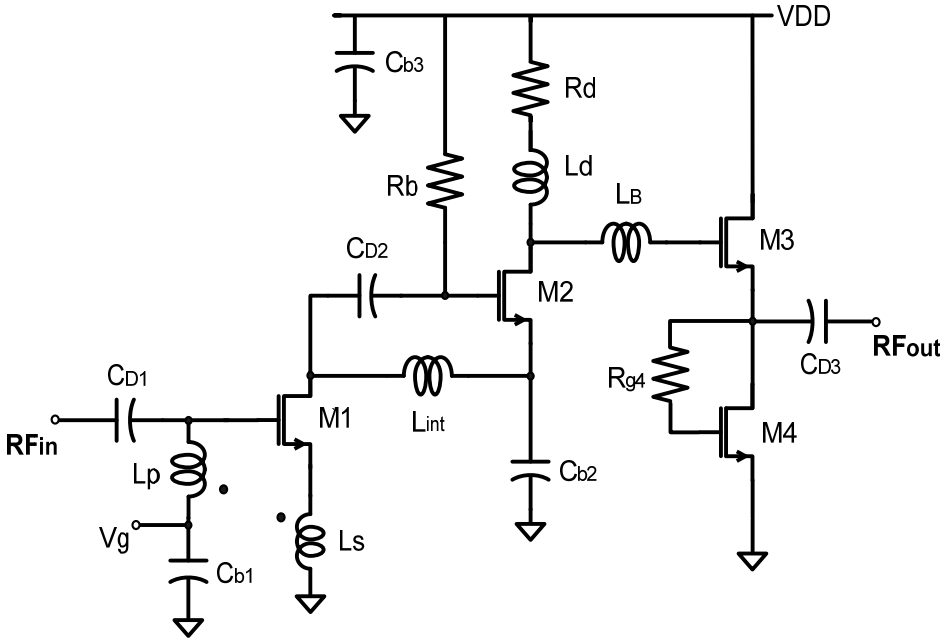


Figure 3-3 Schematic of the proposed UWB LNA.

Transformer-feedback matching network

The proposed LNA is shown in Fig.3-3. The transformer consists of two inductors. The primary winding is shunt with the gate end of M1; the secondary winding is series to the source end of M1. There are no extra lumped elements placing at the input port excluding ac-coupling capacitance C_{D1} and bypass capacitance C_{b1}. In general, the common-source amplifier with the inductive degeneration has been popularly used because it can generate real impedance to match source resistance. The imaginary part can be cancelled by the reactive elements located at the gate of M1. But the method only suits in narrow band amplifier design because it satisfies above only at a specific frequency. Therefore, we modify the conventional matching skills for broadband matching purpose as explained in the following. The simplified input impedance diagram is shown in Fig.3-4.

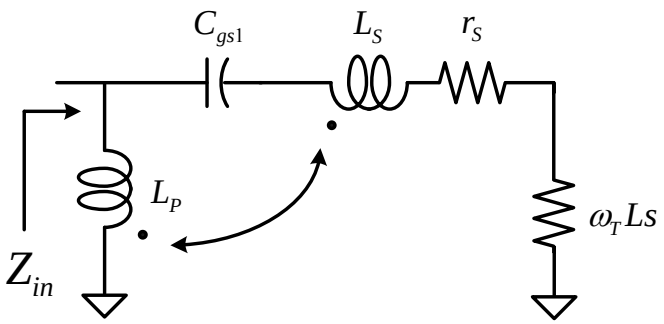


Figure 3-4 The simplified input impedance network

r_s is the parasitic resistance of L_s and the parasitic resistance of L_p is neglected for simplifying the analysis. C_{gs1} is the gate-source capacitance of M1. The input impedance can be represented in s-domain as

$$Z_{in}(s) = (r_s + \frac{gm_1}{C_{gs1}} L_S) + \left[(sL_S + 1/sC_{gs1}) // sL_P \right]$$

$$= (r_s + \omega_T L_S) + \frac{sL_P(1 + s^2 L_S C_{gs1})}{1 + s^2 C_{gs1}(L_S + L_P)} \qquad (3\text{-}4)$$

The imaginary part forms a equation comprising three zero-point frequencies, one resonant frequency is zero, the others are both $1/\sqrt{L_S C_{gs1}}$. It means that if the operating frequency is equivalent to $1/\sqrt{L_S C_{gs1}}$, the impedance matching can accomplish due to the cancellation of the imaginary part. Generally C_{gs1} is a fixed value as long as the biasing is determined. Then, L_s would need to be decreased as the operating frequency rises in order to meet the matching condition. This is the reason that we use transformer in the matching network. The self-inductance and mutual inductance of the transformer are appropriately selected and the practical inductance looked into the source of M1 decreases apparently. The broadband matching can be realized by the phenomenon of the transformer feedback.

Noise Analysis and Current-reuse Technique

The noise performance of the proposed topology is determined by two main contributors: the losses of the input network and the noise of the first amplifying device (M1). The general expression for noise figure as given by a classical noise theory [20]:

$$F = F_{\min} + \frac{R_n}{G_s}\left|Y_s - Y_{s,opt}\right|^2 \tag{3-5}$$

where $F_{\min}$ is the minimum noise factor, R_n is the noise resistance, Y_s is the source admittance ($Y_s = 1/Z_s$), $Y_{s,opt}$ is the optimum source admittance ($Y_{s,opt} = 1/Z_{s,opt}$), and G_s is the real part of the source admittance. We can derive the optimal noise figure if the condition of $Z_s \approx Z_{opt}$ is sustained.

In order to have adequate power gain at the condition of the limited power consumption, we adopt the current-reuse technique at gain stages. The second stage (M_2) is stacked on the top of the first stage (M_1). A coupling capacitor (C_{D2}) and a bypass capacitor (C_{b2}) are required for this topology. Both C_{D2} and C_{b2} are metal-insulator-metal (MIM) capacitors. The choice of large capacitance of C_{D2} is preferred to perform better signal coupling. However, too large MIM capacitors may suffer from parasitic capacitance between the bottom plate of the capacitor and ground, which would degrade the circuit gain. The value of C_{b2} is chosen to be as large as possible to provide ideal ac ground. In addition, R_L and L_L are designed to have a peaking characteristic to compensate the low frequency roll-off of the device.

L_B connects between the main stage and buffer in order to enhance wideband characteristic. The further bandwidth extension is achieved due to a series LC resonance with the gate capacitance of M_4. Various values of L_B can cause different performances of bandwidth enhancement. Fig.3-5 exhibits the gain performance with different value of L_B. We select L_B=2.75 nH for the trade-off between bandwidth and

gain flatness for our design purpose.

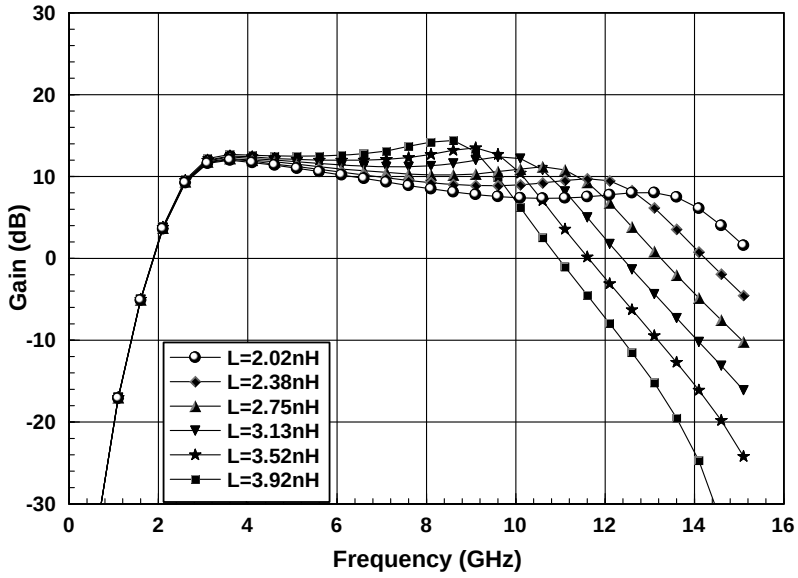


Figure 3-5 Gain performance with L_B variation

A source follower is adopted as the output buffer for a wideband output matching purpose. The current source is different from the conventional one because it is driven by itself without extra bias voltage. The buffer is not needed if the LNA integrates directionally to mixer or other circuit block.

Layout consideration

The geometric layout of the transformer [19] will impact the input return loss, noise figure, and stability, etc. Rectangular-type and concentric spiral windings are adopted to reduce the Q factor for wideband applications. Turn numbers of separate inductor and the spacing between the two inductors inside the transformer are appropriately chosen to achieve feasible self-inductance and mutual inductance, respectively. The transformer of this proposed LNA is simulated by ADS Momentum and the geometric photo is shown in Fig.3-6. Metal 6 is used to layout the transformer because that thicker metal reduces the ohmic losses in the primary and secondary windings of a planar transformer. The size of M1 is 150×0.18 μm^2 for noise optimum

source impedance. The 130×0.18 μm^2 of M_2 size is selected as the trade-off between gain and nonlinearity. The value of L_{int} is 4.8nH to make sure in inter-stage stability.

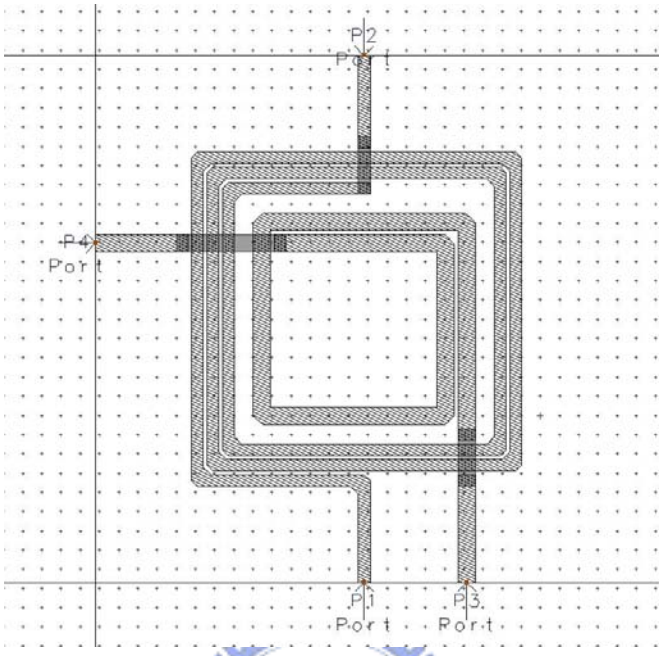


Figure 3-6 Diagram of the proposed transformer applied in this design

3.2.3 Simulation and Measurement Results

The Ultra-wideband LNA with the transformer feedback matching network is fabricated using TSMC 0.18μm RF CMOS process. Fig.3-7 shows the microphotograph and the total area is about 0.6 mm^2. The whole measurement is on-wafer test on the RF probestation. Two three-pin GSG RF probes are used for transmission of input and output signal, and one three-pin PGP DC probe provides the biasing and supply voltage. The scattering parameters are measured by HP 8510C. Fig.3-8~3-11 illustrate the measured results of individual s-parameters. The simulation results are also put together to compare the difference. In Fig.3-8 the measured input return loss (S11) is better than -9.8 dB over the entire UWB band with two dips at 3.7GHz and 6.2GHz. The performance proves that transformer feedback is feasible in wideband matching. The output return loss (S22) is -10.4 dB below from Fig.3-11. Fig.3-10 shows that the

measured isolation form output to input is under -28 dB. Fig. 3-9 is the simulated and measured results of the power gain. The measured power gain has a peak value in 12.4dB and the average value is 11.2dB with 1.2dB ripple from 3.1GHz to 10.6GHz. The result presents a good feature of flatness. For the noise figure measurement, we exploit noise figure analyzer (Agilent N8975A) and noise source (Agilent 346C). The results of simulated and measured noise figure are shown in Fig.3-12. It is obvious that the curves of NF_{sim} and $NF_{\min}$ are mostly overlap in the UWB band. It indicates that transformer feedback has an optimal noise figure performance as well. The measured results of NF have the minimum value 3.2dB at 5GHz and the average is 4dB.

As to in-band linearity, the 1-dB compression input point (P_{1dB}) with 5GHz is -14dBm as shown in Fig.3-13. Two-tone signals of 5GHz and 5.01GHz are applied to the LNA to observe the input referred third-order intercept point (IIP3), and the spectral diagram has shown in Fig. 3-14. The measured value is in the range of -5 to -10dBm over 3 to 10-GHz system while P_{1dB} is about -22dBm to -14dBm. From Fig.3-15 it can observed that IIP3 is around 10 dB less than P_{1dB} over the entire band.

Table 3-2 makes a comparison between simulation and measurement results. It demonstrates that they are only slightly different. Table 3-3 lists some previously-proposed references. Each input matching method and characteristic of LNA is summarized to make comparison. It can be observed that our UWB LNA with transformer feedback has competitive performances at I/O return loss, power gain, power consumption, and even chip size.

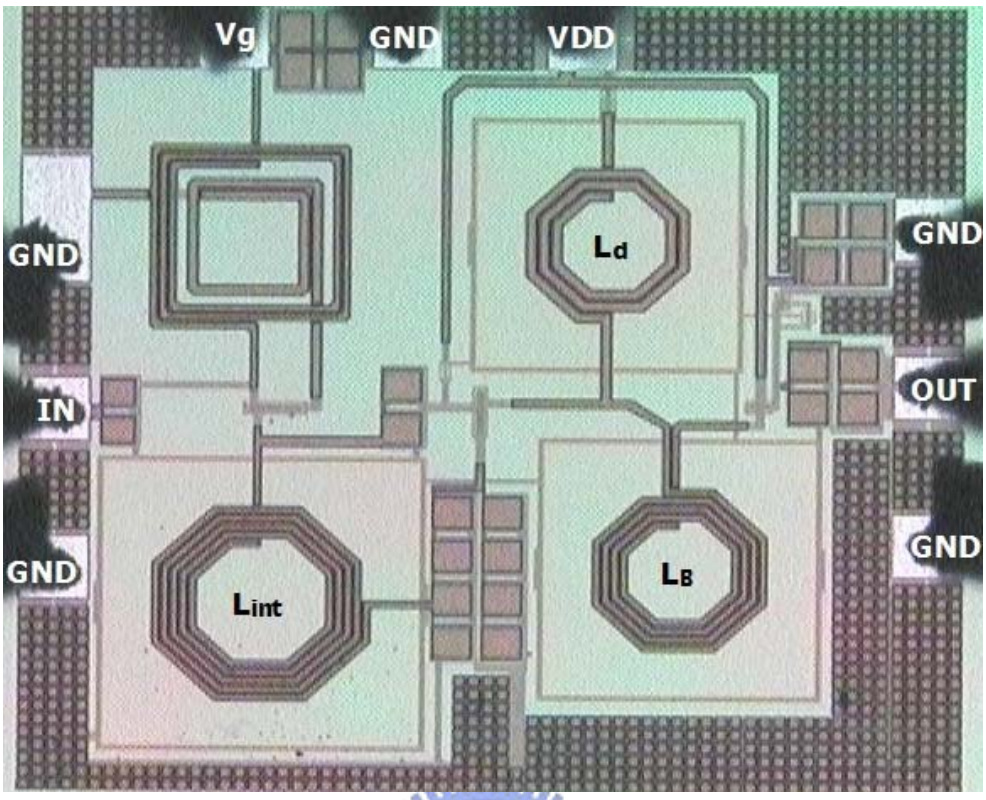


Figure 3-7 Microphotograph of the proposed LNA

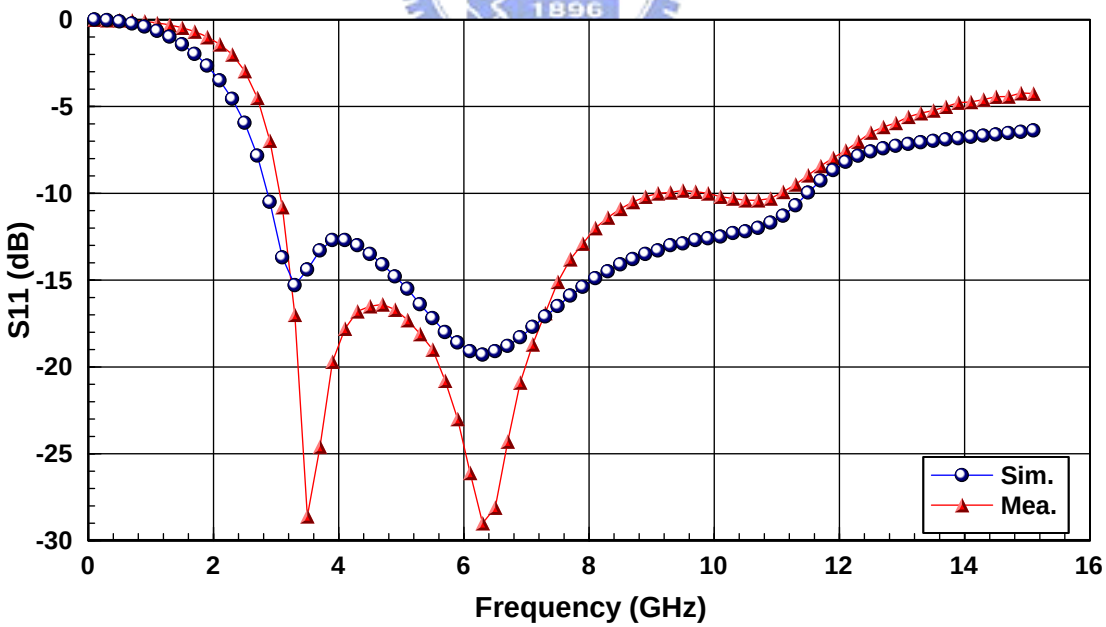


Figure 3-8 S11 simulation and measured results of UWB LNA

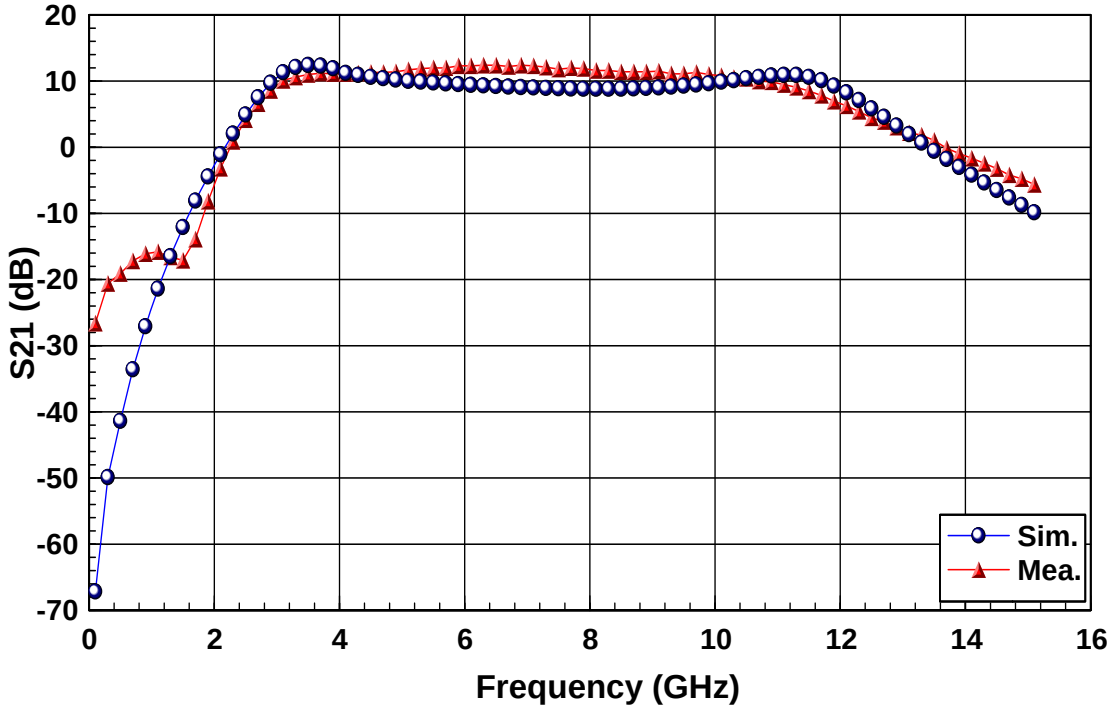


Figure 3-9 S21 simulation and measured results of UWB LNA

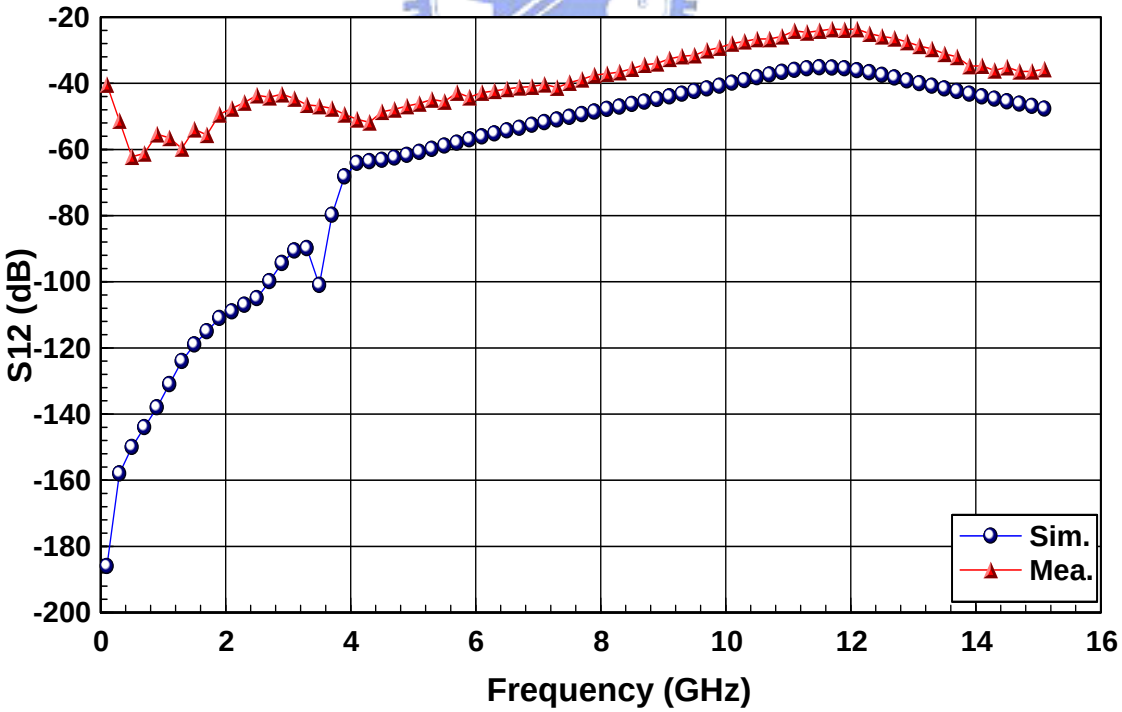


Figure 3-10 S12 simulation and measured results of UWB LNA

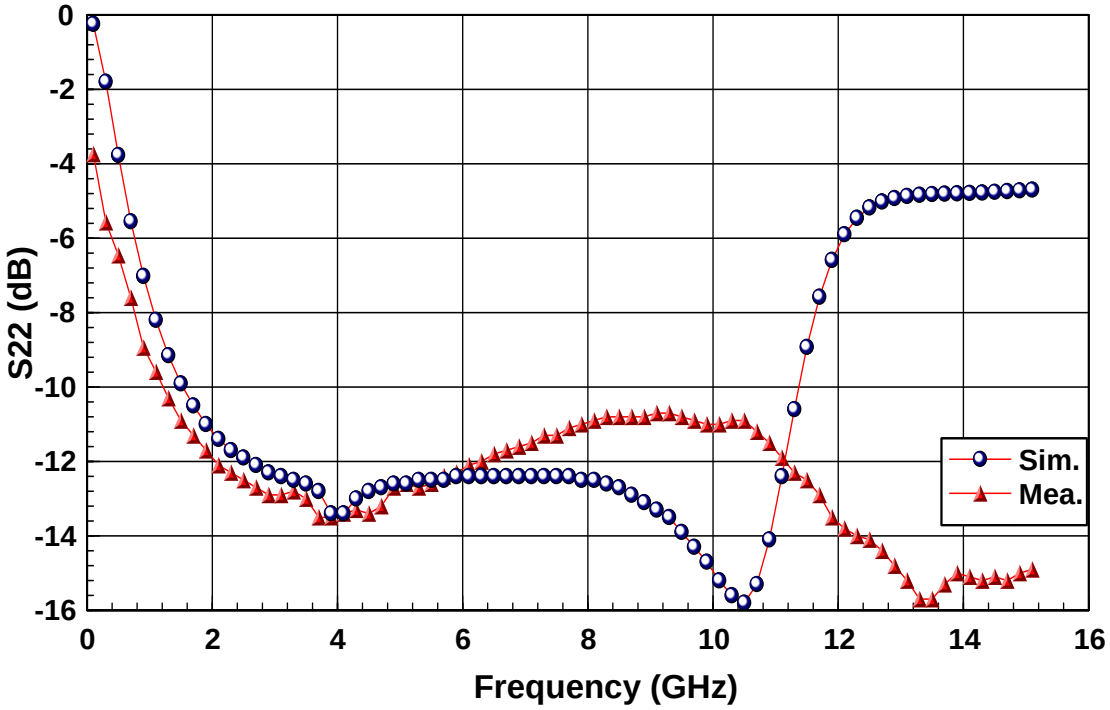


Figure 3-11 S22 simulation and measured results of UWB LNA

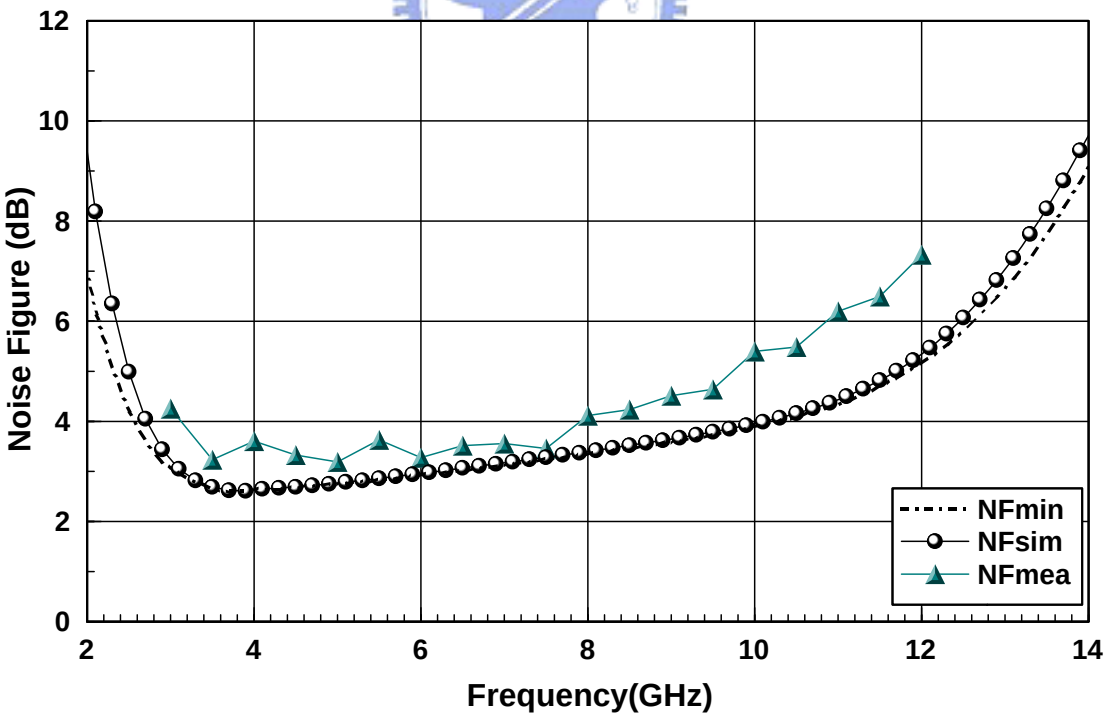


Figure 3-12 NF simulation and measured results of UWB LNA

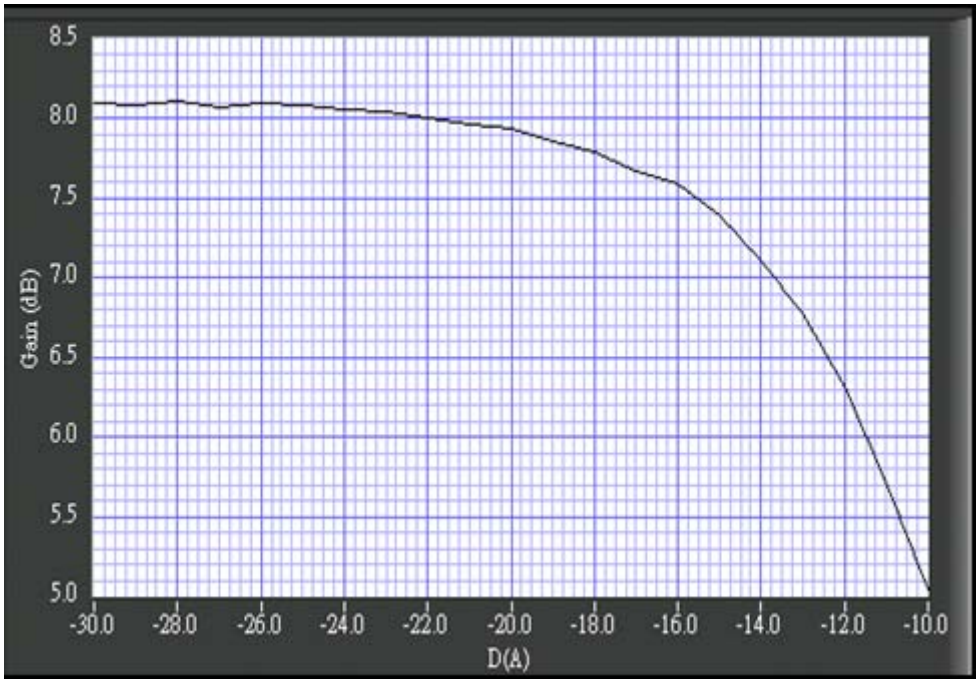


Figure 3-13 Measured input 1dB compression point at 5GHz

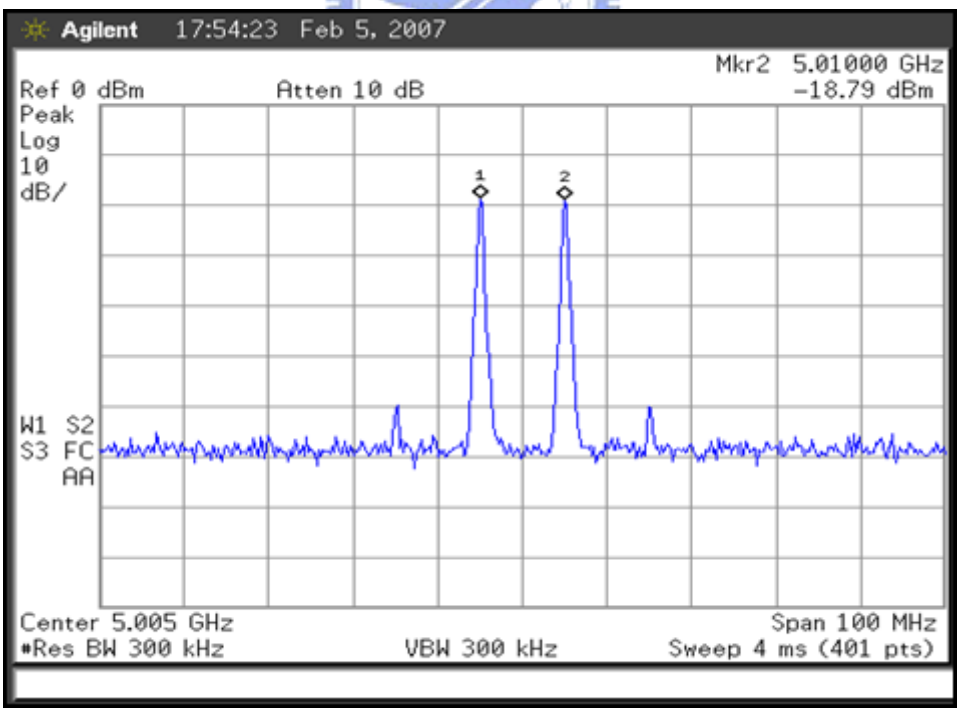


Figure 3-14 Spectral diagram of the IIP3 measurement (one tone is 5GHz, and the other tone is 5.01GHz)

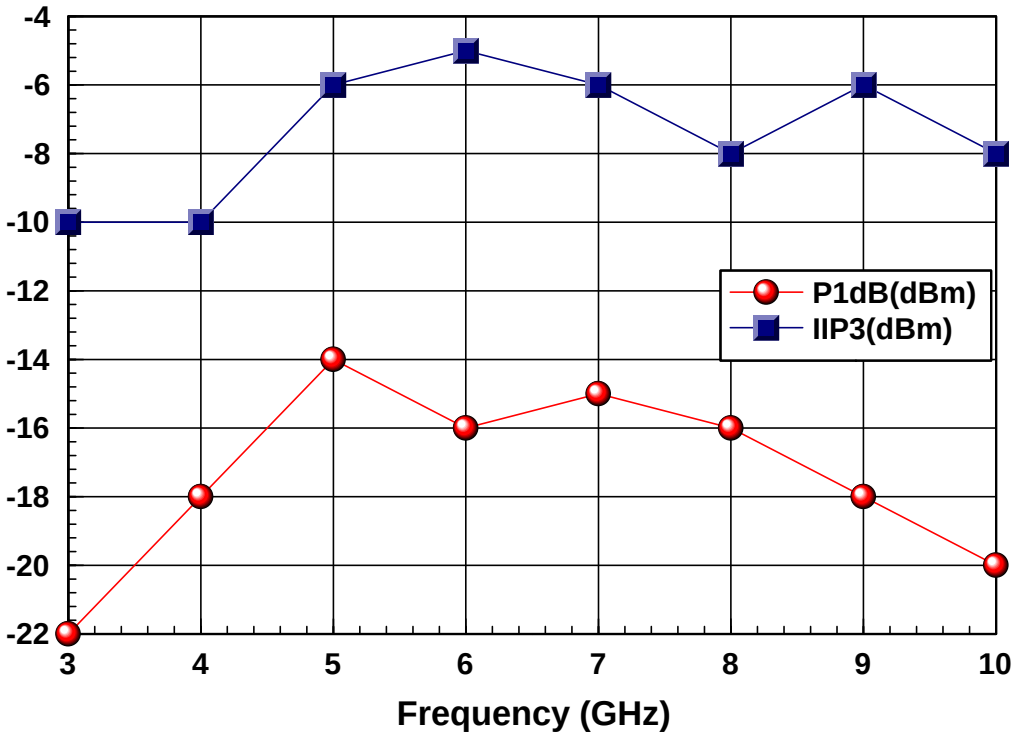


Figure 3-15 Measured P_{1dB} and IIP3 curves over the UWB band

Table 3-2 Comparison of simulation and measurement results of UWB LNA

	Simulation results	Measurement results
S11 (dB)	<-10.7	<-9.8
S21 (dB)	12	11.2±1.2
S12 (dB)	<-36	<-24
S22 (dB)	<-11.6	<-10.4
NF (dB)	<4.6	3.2~5.5
P1dB (dBm)	-14 ~ -23	-14 ~ -22
IIP3 (dBm)	-3 ~ -13	-5 ~ -10
Power dissipation (mW)	11.4	11.1

Table 3-3 Performance of summary and comparison to other wideband LNAs

Ref.	BW (GHz)	Input matching method	S11 (dB)	S21 (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	Technology	Area (mm^2)
[21]	2.3~9.2	3rd-order Chebyshev filter	<-9.9	9.3	4~9.2	-8.2~-5.6	9* @1.8V	0.18um CMOS	1.1
[22]	3.1~10.6	Distributed amplifier	<-10	16.8~19.2	5~7	N/A	54 @1.8V	0.18um CMOS	2.2
[23]	3~5	Resistive-shunt feedback	<-9	9.8	2.3~5.2	-7	12.6 @ 1.8V	0.18um CMOS	0.9
[16]	3.1~10.6	Dual feedback	<-11.2	10.8~12	4.7~5.6	-12 ~-10.6	10.57* @1.5V	0.18um CMOS	0.665
This work	**3.1~10.6**	**Transformer feedback**	**<-9.8**	**11.2±1.2**	**3.2~5.5**	**-10 ~ -5**	**11.1 @1.5V**	**0.18um CMOS**	**0.6**

* without adding consumption of buffer stage

3.2.4 Discussion

In section 3.2, we propose a novel UWB LNA and implement successfully by TSMC 0.18μm CMOS process. This circuit uses the transformer feedback topology to realize broadband matching and noise optimization. At the gain stage, it adopts current-reuse technique to have adequate gain performance under power consumption limits. A source follower with self-biasing can reduce extra bias voltage and achieve output matching. The measured results of S11, S21, and S22 are similar to the simulation results. The measured NF is close to simulation result at the low band and only higher than simulation result about 1dB at the high band. The reason may be that parasitic resistance affects apparently at the higher frequency band. As to linearity, the maximum IIP3 is -5dBm at 6GHz while P_{1dB} is -14dBm. It can be observed that our UWB LNA with transformer feedback has competitive performances at I/O return loss, power gain, power consumption, and even chip area.

3.3 Analog Correlator with Dynamic Gain Control

This section describes the circuit design principle of a correlator suitable for UWB systems. The technique of dynamic gain control is inserted for a VGA-like architecture in this correlator. The simulation and measurement results are exhibited and discussed in the final of this section.

3.3.1 Design Concepts

The function of correlator is detecting and demodulating the received signal for the following A/D converter or comparator. Normally a correlator incorporates a separate multiplier and a separate integrator. There are some main problems in designing the correlator of pulse-based UWB receiver [24]. For instance, the multiplier should have very wide-band input frequency response, even the lower band UWB pulse is very large depending on data and applications. Therefore, though the DC offset current or 1/f noise current must be much smaller than the signal current, it can integrate on the integral capacitor for a much longer time the multiplied signal. Another problem is that after the pulse correlation, the output voltage should maintain for a long time for the ADC to sample, but the output impedance of the integrator normally is not large enough, and results in large leakage from the integrator. These ultra-wideband characteristics of the input pulses make the digital domain correlation not suitable in this application. According to above discussions, we adopt the analog correlator in UWB system receiver.

Generally multipliers are much more difficult to design than mixers. For mixers, the gain doesn't need to vary linearly with the LO signal, and only the first harmonics of the LO is needed to multiply with the input signal. Working in linear region makes the multiplier very difficult to bias. In this design of multiplier we apply a Gilbert-cell with bandwidth extension and linear adjustment for UWB systems.

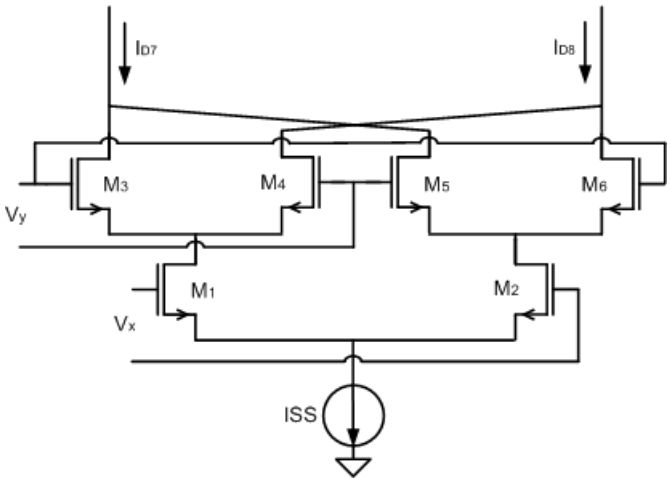


Figure 3-16 A Gilbert multiplier

Gilbert-cell multiplier is the common architecture used in communication circuit [7]. Besides circuit simplicity and high isolation, double-balanced type also has some advantages about eliminating even-mode harmonic and common-mode noise. For example in Fig.3-16, the output differential current can be expressed as follow

$$\begin{aligned} I_{out} &= I_{D7} - I_{D8} = (I_{D3} + I_{D5}) - (I_{D4} + I_{D6}) \\ &= (I_{D3} - I_{D4}) + (I_{D6} - I_{D5}) \end{aligned} \tag{3-6}$$

$$\begin{aligned} &= kV_X[\sqrt{(\sqrt{\frac{ISS}{k} - \frac{V_Y^2}{2}} + \frac{V_Y}{\sqrt{2}})^2} - \sqrt{(\sqrt{\frac{ISS}{k} - \frac{V_Y^2}{2}} - \frac{V_Y}{\sqrt{2}})^2}] \\ &= \sqrt{2}kV_XV_Y \end{aligned} \tag{3-7}$$

Based on the Gilbert-cell, we design a novel correlator with dynamic gain control, whose overall schematic of circuit is shown in Fig.3-17. The additional transistors (M_{C1}, M_{C2}) are added at the source of the transconductance stage. The additional transistors operating in triode region are used as resistors and each resistance value is $r_{ds} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})}$. The resistance looking in current source is r_o. From Fig.4-18 we can know that the overall resistance looking in the source of M_1 is

$R_s = r_o // r_{ds} \approx r_{ds}$, and the overall transconductance is $Gm = gm/1 + gmR_s$, where gm is the intrinsic transconductance of M_1. It means that Gm is dominantly controlled by r_{ds}. Moreover, the value of r_{ds} can be changed by V_{ctrl}. Thereby a tunability is achieved by changing the value of the control voltage at the gate of transistor M_c. By adjusting the magnitude of transconductance, the amplitude of output waveforms can be controlled.

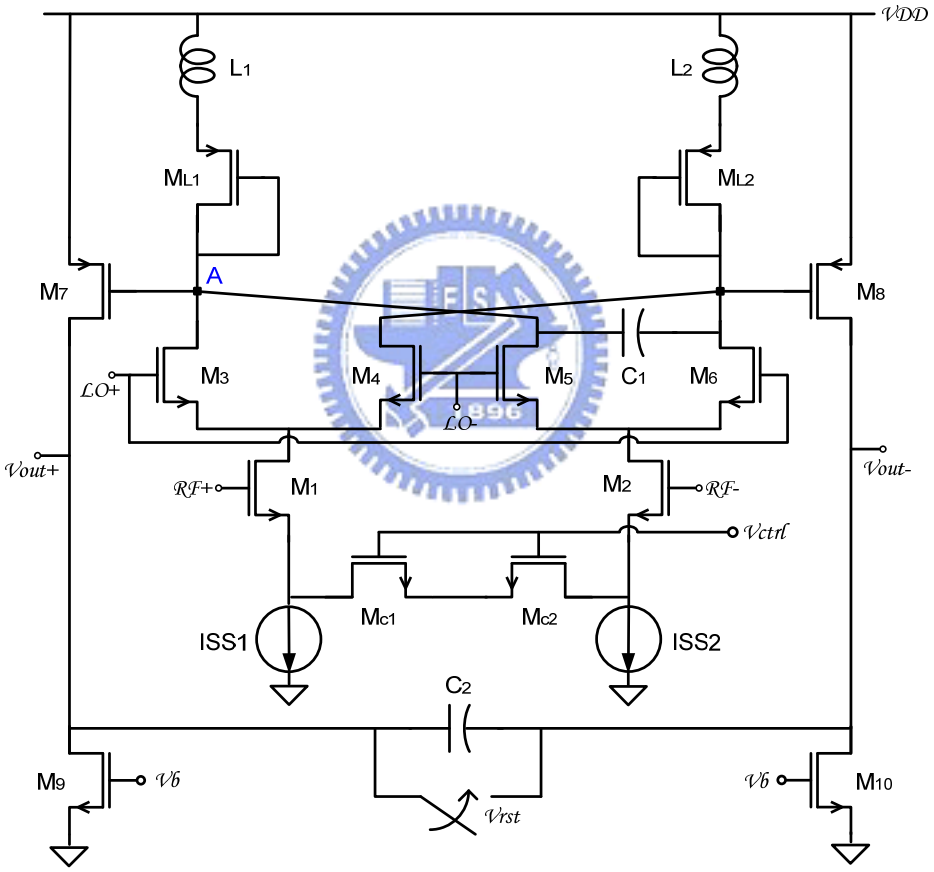


Figure 3-17 Schematic of the proposed correlator circuit

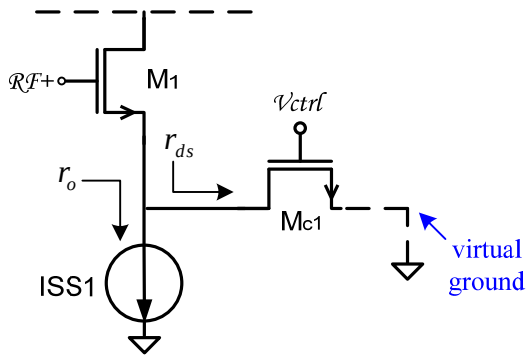


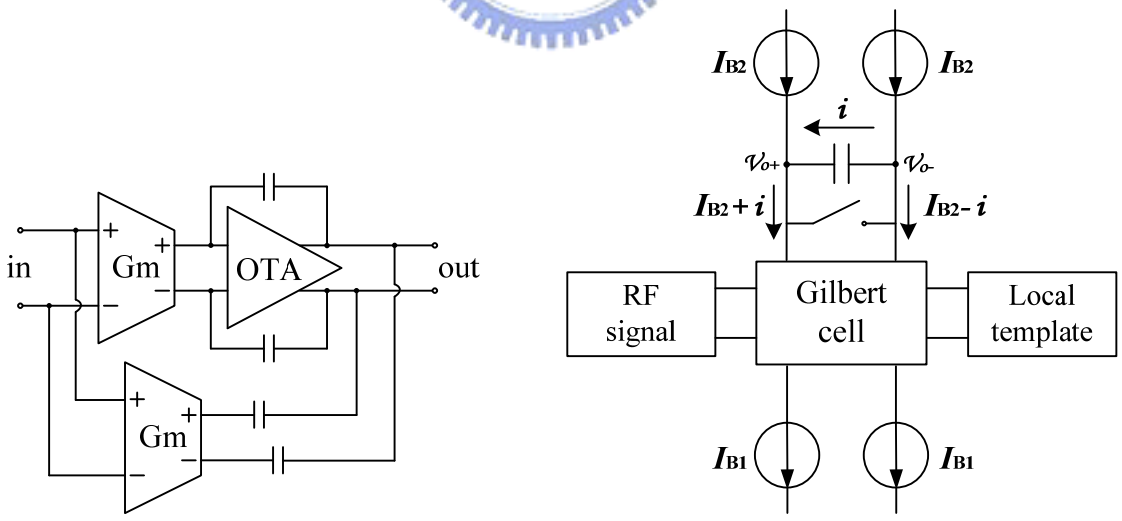
Figure 3-18 The transconductance stage with source degeneration

As for loading end, the correlator needs wider frequency response for UWB systems. The zero-point frequency is generated purposely to cancel the dominant pole frequency for achieving wideband characteristic. There are four transistors connecting at the load-end of the first stage, so the parasitic capacitance is large enough to form the dominant pole. The PMOS (M_{L1}, M_{L2}) with diode connecting plays the role of the load resistors whose value are $R = \frac{1}{gm} // r_o$. There are two extra advantages about diode-connected PMOS as load. First, the cross voltage is $V_{ov} + V_{th}$, which can make sure the next stage at the on state. Second, the correlator can be viewed as a direct conversion architecture. The interference of the flicker noise of NMOS affects the received signal deeply. For the reason, PMOS is used at the loading stage due to the lower flicker noise than NMOS.

The function of integration is to spread the multiplied signal and hold for a long time for the next stage. Generally some references apply Gm-C-OTA integrator in UWB systems [12,13]. The benefits are low voltage variation and unapparent parasitic capacitance effect, which can stabilize the integration. In order to have faster integration and shorter rise time, this architecture must need large current to drive. Besides, another parallel transconductance is used to create a feed-forward path for compensating the high-frequency response and building the rapidly rising edge of the output signal. This

architecture is good but it cost large power because of multi-stage circuits. In this design we directly add a capacitor (C_1) at the differential output of the multiplier. Because of $I_{out} = C\frac{dV_{out}}{dt}$ and $V_{out} = \frac{1}{C}\int I_{out}dt$, the integration results can be achieved at the differential output of the multiplier. The method not only reduces complexity of the circuit design but also avoids extra power dissipation of separate integrators.

It can be observed that the signal after integrating operation still has apparent drop and don't hold for a long time. Two-stage architecture is proposed in this correlator because that the second stage can amplify and integrate signal again. The mechanism is also presented in Fig.3-17. C_2 is the second integrating capacitor and locates between the differential output of the second stage. Moreover, there is a switch parallel to C_2. The purpose of the switch is resetting the output data by controlling voltage V_{rst}. When the switch turns off, the circuit works normally; when the switch turns on, the differential output is short. Voltage V_{rst} is a square pulse train with 1.8V amplitude. The period of V_{rst} is similar to input data and the duty cycle is 50%.



(a) (b)

Figure 3-19 (a) Gm-C-OTA integrators (b) The correlator with direct integration

Finally, in order to measure the output waveform, source followers are added at the final stage for 50Ω matching (not illustrate in Fig.3-17). Unfortunately, it may generate unnecessary parasitic capacitance and degrade performance. The buffer is not needed if the correlator integrates directly to other circuits.

3.3.2 Simulation and Measurement Results

Fig.3-20 illustrates that the input signal is an ideal Gaussian monocycle, which amplitude is ±0.4V. In simulation verification the pulse repetition rate is 100MHz. The reason is for the sake of verifying the feasibility of the correlator in high data rate. The simulation output waveform is shown in Fig.3-21. In the thesis we list the definitions about rise time, fall time, and hold time. The time required for a signal to change from a specified low value to a specified high value is rise time. Typically, these values are 10% and 90% of the peak value. Corresponsively, fall time is the value of 90% and 10% of the height. Hold time is the duration when the amplitude of signal is over 90% of the peak value. It can be observed that the rise time, fall time, and hold time are 1.3ns, 3.0ns, and 1.1ns, respectively in Fig.3-21. Different output waveforms with V_{ctrl} variation are shown in Fig.3-22. The range of output amplitude is 0.08V to 0.131V while V_{ctrl} is 0.7V to 1.8V. The output amplitude is not proportional to V_{ctrl} because of nonlinear characteristics of transistor. As to linearity, the linear input range is from -0.17V to +0.17V and has been shown in Fig.3-23. A good linearity is obtained as well.

The practical input signal is a Gaussian monocycle generator implemented by schottky diodes and lumped elements on the PCB. The generator is for the purpose to converts square waves to Gaussian monocycles. The photo and waveform is shown in Fig.3-24. As for the measurement setup, the chip on the PCB by wire bonding is adopted because of limits of probes. The measured results of singly-ended output waveforms are shown in Fig.3-26, 3-27. In Fig.3-26, the peak value is 44.5mV and rise

time is close to 1.8ns while repetition data rate and V_{ctrl} are 100MHz and 1.8V, respectively. Fig.3-27 shows that the peak value is 18.1mV while V_{ctrl} is 0.7V. Fig.3-28 records the different differential output amplitude versus the control voltage ranging from 0.7V to 1.8V. It can be observed that the trend is similar to simulation. Fig.3-29 shows the chip microphotograph of correlator.

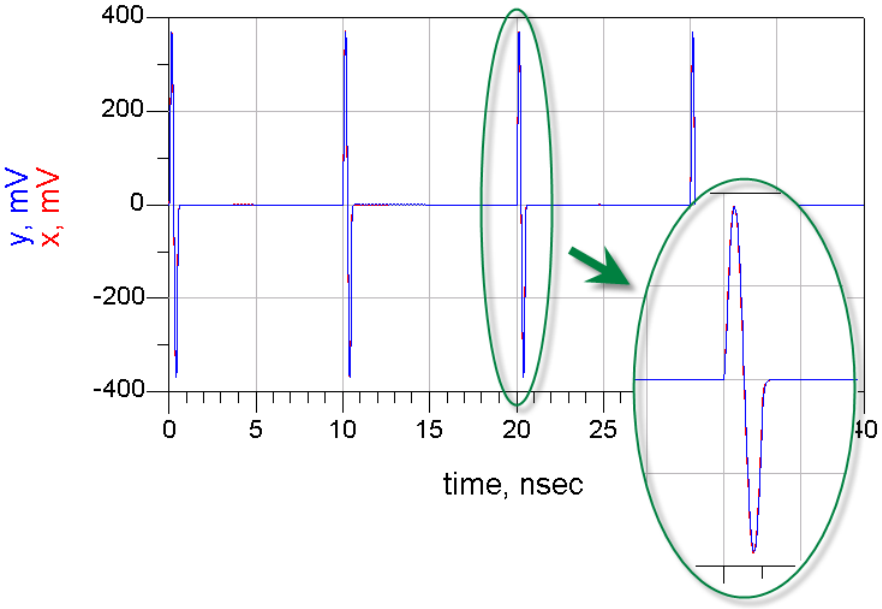


Figure 3-20 Input waveforms

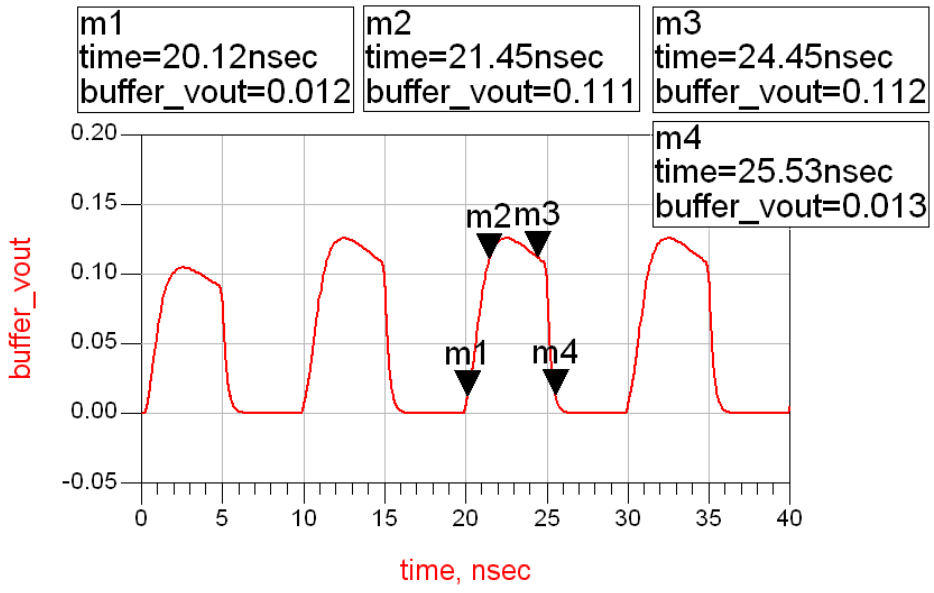
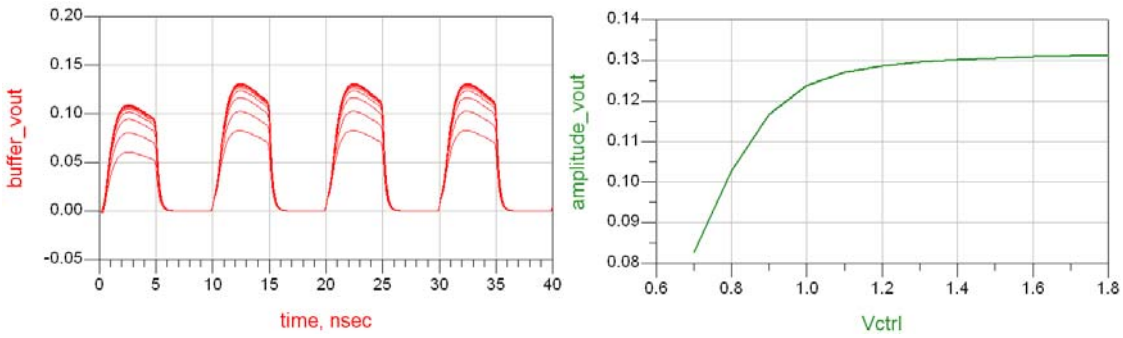


Figure 3-21 Simulation output waveforms



(a) (b)

Figure 3-22 Simulation (a) different output waveforms with V_{ctrl} variation (V_{ctrl} =0.7V~1.8V) (b) output amplitude versus V_{ctrl}

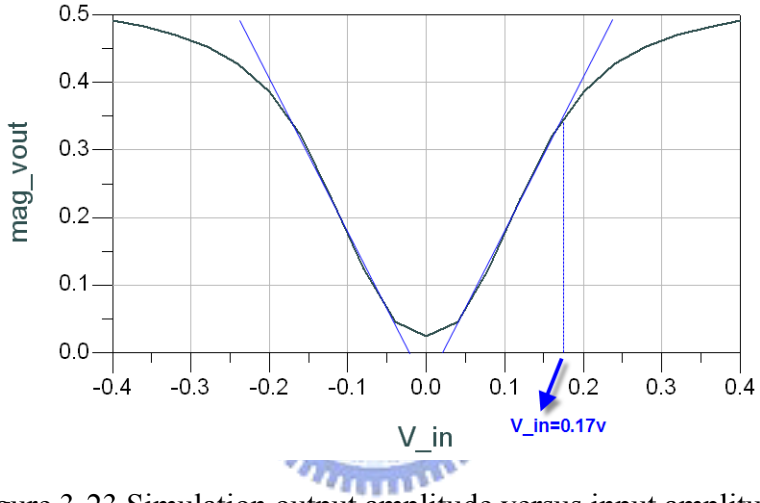
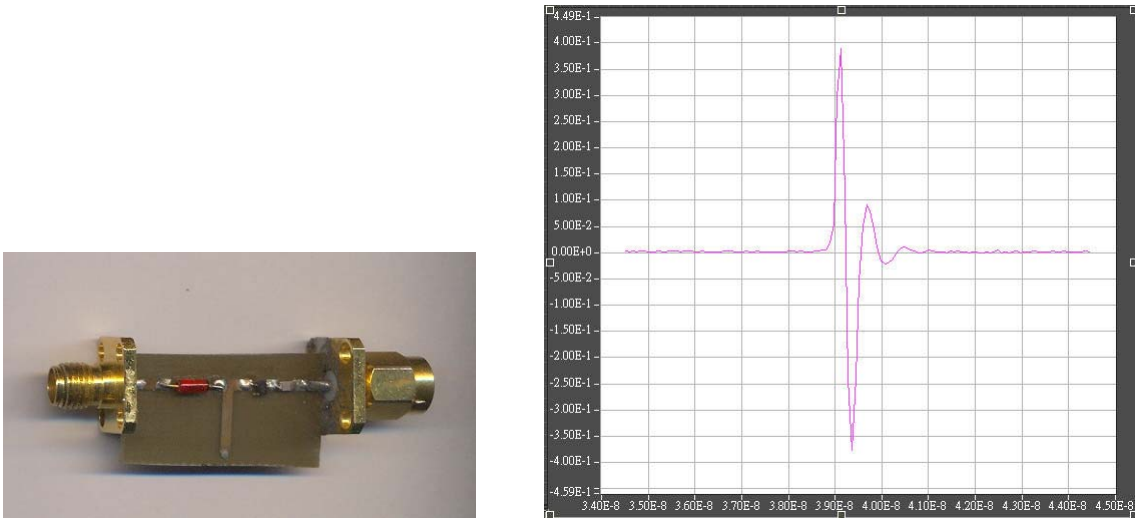


Figure 3-23 Simulation output amplitude versus input amplitude



(a) (b)

Figure 3-24 (a) Practical monocycle pulse generator (b) Measured waveform

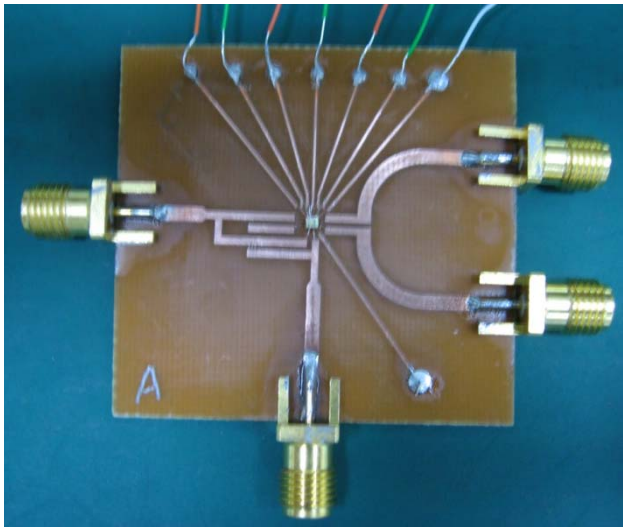


Figure 3-25 Photo of chip on board with bonding wire

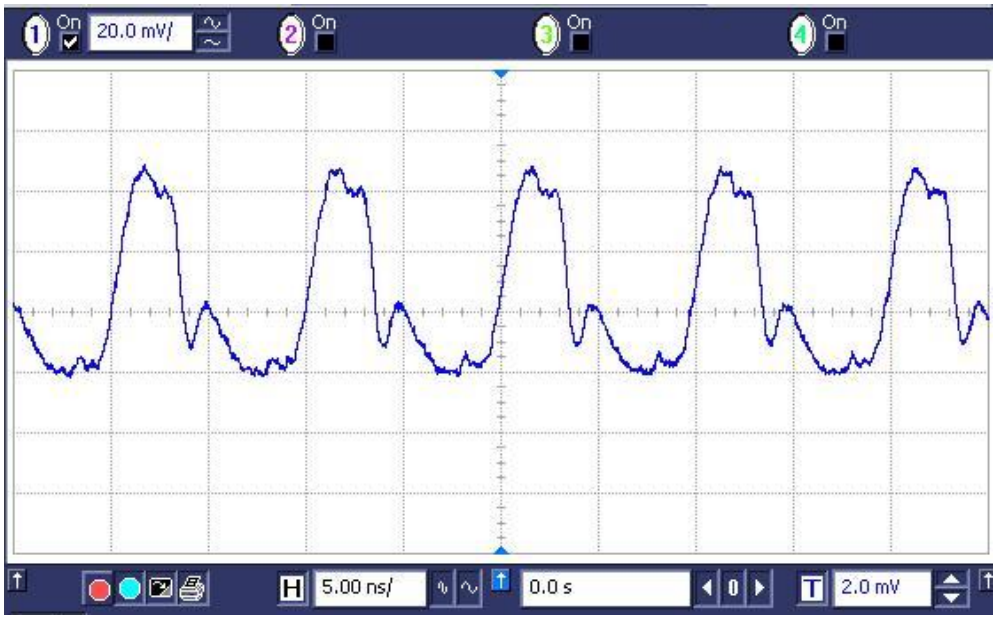


Figure 3-26 Measured single-end output waveforms (V_{ctrl} = 1.8V)

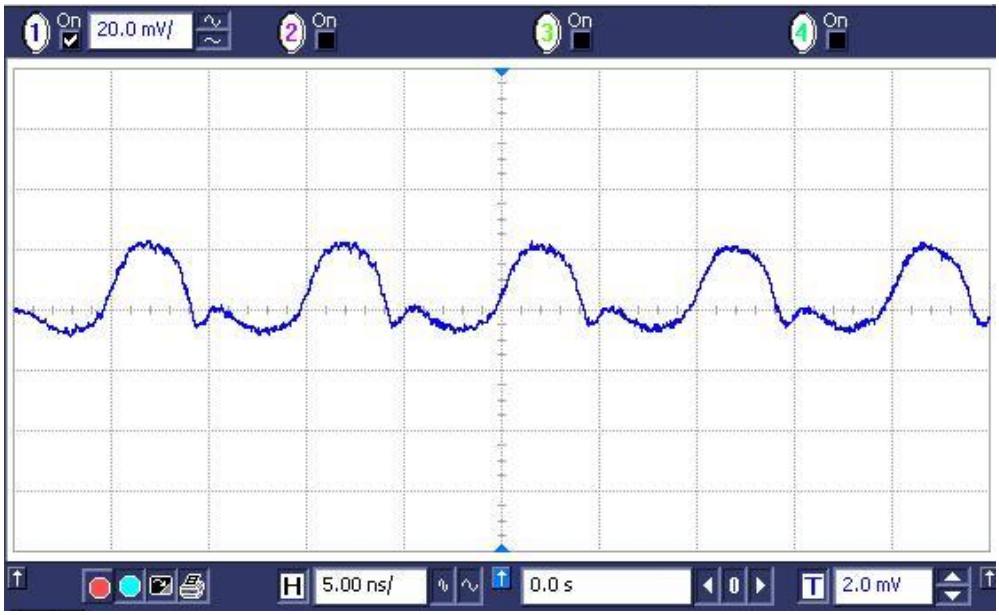


Figure 3-27 Measured single-end output waveforms (V_{ctrl} = 0.7V)

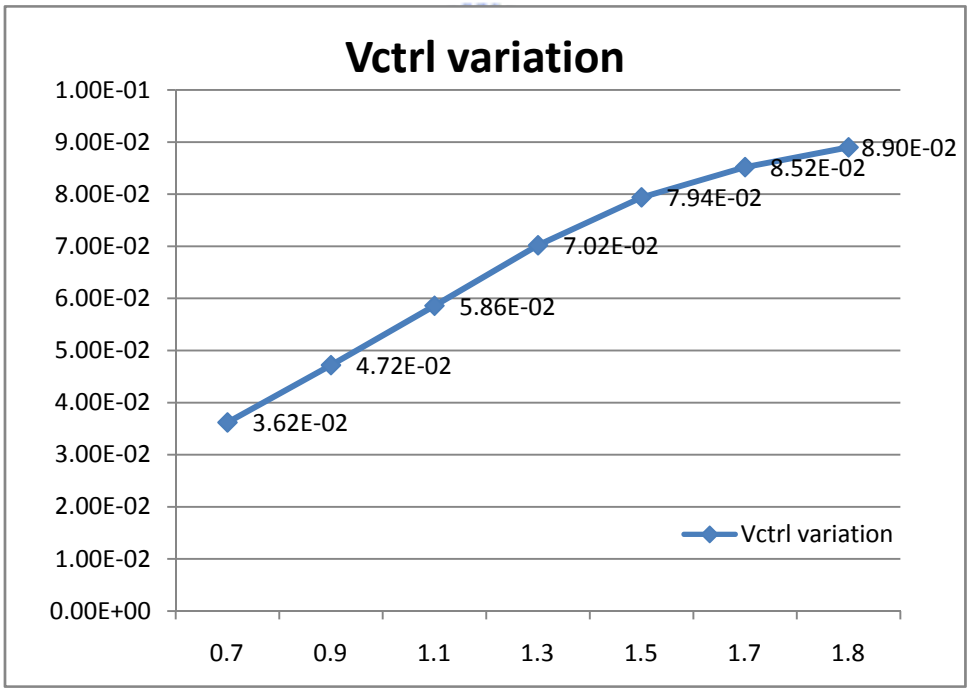


Figure 3-28 Measured output amplitude versus V_{ctrl} (V_{ctrl} = 0.7~1.8V)

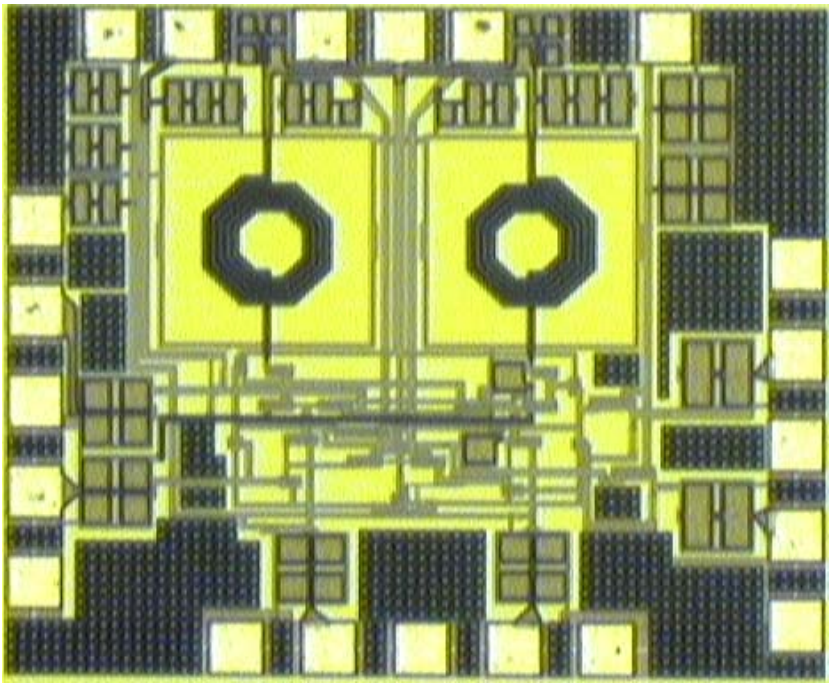


Figure 3-29 Microphotograph of the proposed correlator

Table 3-4 Comparison of simulation and measurement results of the correlator

	Simulation results	Measured results
Technology	TSMC 1P6M 0.18μm	
Supply voltage(VDD)	1.8 V	
Chip area	0.74mm×0.88mm	
Repetition data rate	100MHz	
Max. V_{out} amplitude	133 mV	89mV
V_{ctrl} control range	0.7V~1.8V	
Tuning range of output amplitude	82~133mV	36~89mV
Rise time	0.82ns	1.8ns
Hold time	3.0ns	2.9ns
Linear input range	±0.17 V	
Power consumption (exclude buffer)	10.26mW	8.78mW

3.3.3 Discussion

It can be observed that the measured results do not achieve expectation. We consider that the imperfect pulse generator (PG) is the dominant problem. The practical PG does not generate complete symmetrical Gaussian monocycle with slight ringings. In addition, the pulse generator connects a single-to-differential balun to generate the differential pulses in order to make synchronization between the dual input ports. However, the balun only has an operating bandwidth from 2 to 4 GHz. The output pulses of balun have more distortion than the primary ones. The distortion may result in measurement discrepancy. Moreover, the chip with wire bonding may be another potential problem. Although the measured results don't accomplish primary result in the simulation, but the correlator still functionally work. We will consider carefully for later integration.

Due to the similar waveforms of dual inputs, the correlator can be regarded as a direct-conversion (zero-IF) architecture. According to the measured results, it can be observed that DC offset occurs. The generation of DC offset usually has several reasons, which like self-mixing, even-mode nonlinear distortion, and imbalance turn-on time between the positive end and the negative end. These reasons above may cause the output waveforms do not have good performance. Some resolutions can decrease the happen of DC offset. First, it can add extra a low pass filter to isolate high-frequency harmonic elements and make sure the low-frequency elements exist. Second, the mechanism of common-mode feedback (CMFB) can add at the differential output to degrade the imbalance of the differential pair.

3.4 Conclusion

In this chapter we have designed and implemented a UWB LNA and a correlator individually. The LNA uses transformer feedback matching and current reuse technique

to achieve good input matching, noise figure, and gain performance. Because of complete layout consideration and post simulation, the measurement results of LNA show that they are similar to simulation results. It indicates that the transformer feedback topology is feasible for broadband matching. With respect to the correlator, bandwidth extension and dynamic gain control techniques are used in this design. Due to imperfect measurement consideration and signal source, the measured results are more different than simulations. However, it is convinced that these design concepts are suitable in the coherent receiver of IR-UWB systems.

Chapter 4

An Integrated Front-end Receiver for IR-UWB Wireless Communication Systems

4.1 Overview

In this chapter we present a fully integrated front-end receiver of System-On-Chip (SOC) implementation for impulse-radio UWB communication systems. The block diagram is shown in Fig.4-1. It comprises a wideband LNA, a pulse generator, and a correlator. The LNA with transformer feedback and current-reuse topology can accomplish good input matching, low noise figure, and low power consumption. The 2^{nd} –order derivative Gaussian pulse generator used for generating template waveforms applied to correlate the received signal. The correlator works as multiplication and doubly integration to demodulate the received signals. The overall integrated circuit is fabricated by TSMC 0.18-μm 1P6M CMOS technology and has 19.96-mW total power consumption with 1.48 mm^2 chip area. In this chapter, we only introduce the design concepts of pulse generator and correlator (for LNA has been demonstrated in Chapter 3). The clock timing of the coherent receiver must to be discussed because of synchronization. Finally, we also introduce the measurement environment and exhibit the simulation and measured results.

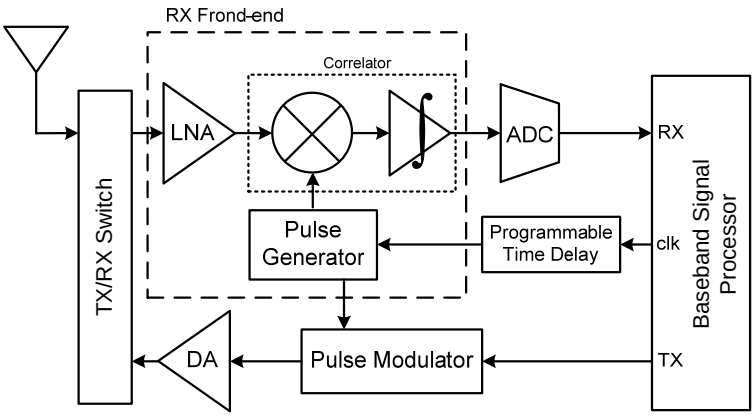


Figure 4-1 System architecture of IR-UWB transceiver (dash line indicates RX front end)

4.2 Switched 2nd-order derivative Gaussian Pulse Generator

In order to generate a local 2nd-order Gaussian pulse, the pulse generator (PG) comprises three cascade stages to realize the square, exponential, and second-order derivative functions, respectively [25]. The illustration is shown in Fig.4-2. Based on Fig.4-2, we propose that switched pulse generator (WSG) applied in this receiver. WSG has low-power property because there is nearly no static power consumption. The circuit is shown in Fig.4-3, including a clock shaping, a transient circuit, and a 2nd-order derivative circuit. First, in order to achieve a more ideal clock signal for next stage, the clock shaping network consists of four-cascaded inverters which can improve the rise/fall time of the clock signal in the sub-nanosecond range. The simulation waveforms are shown in Fig.4-4. The black line indicates non-ideal clock waveform, whose rise and fall time are both 1.5ns and period is 10ns. The modified clock by shaping circuit is presented in gray line and the rise time is less than 100ps. Although the amplitude of modified clock degrades slightly compared to the original clock signal, but it is enough to drive accurately for circuits of next stage. The simulation results shows the practical clock becomes more ideal clock by a shaping circuit made of four-cascaded inverters.

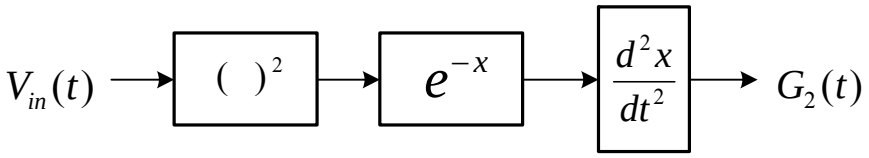


Figure 4-2 Block diagram of the generation of the 2nd-order derivative Gaussian pulse

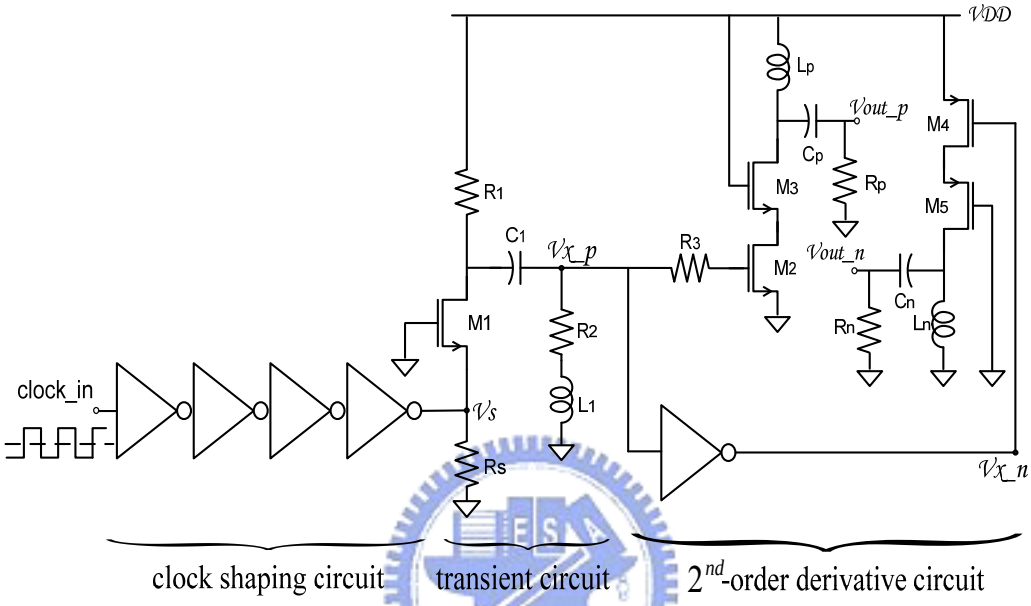


Figure 4-3 Schematic of 2nd-order derivative Gaussian pulse generator

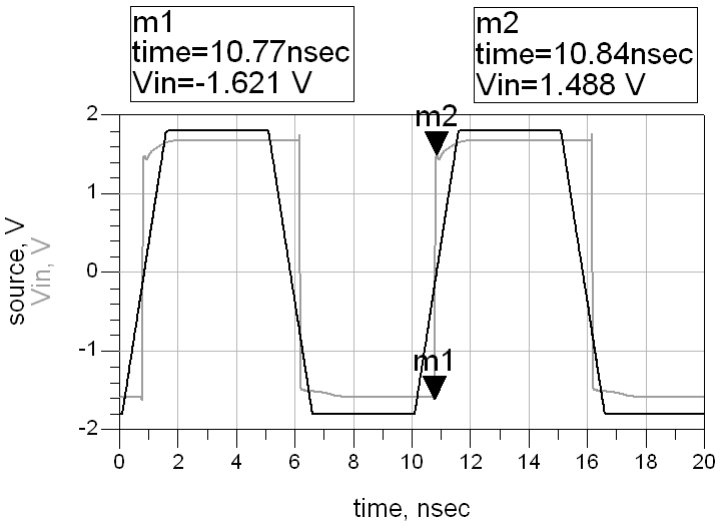


Figure 4-4 Non-ideal clock and clock after shaping

As for the transient circuit, the common-gate stage (M_1) works as a switch. When

clock V_s is in negative half-period, M_1 turns on and the current only flows through M_1 but not C_1. When V_s is changing from the negative to the positive state, M_1 becomes cut off and the impedance looking in C_1 is very small. At the short duration, the current flows through the $R_1L_1C_1$ series circuit and forms an impulse in V_{x_p} [26]. The impulse is shown in Fig.4-5 and the width is about 200ps. The small resistor R_2 is used for reducing ringing of the impulse.

Finally, in the 2nd-order derivative circuit, M_2 is driven only when its gate voltage is at positive edge. The cascode stage does not have current flow for the rest of the impulse period. The main second-order derivation function is implemented by the $R_pL_pC_p$ network. The trans-impedance of the RLC network in the s-domain is derived as

$$T(s) = \frac{V_{out\_p}(s)}{I_{ds3}(s)} = \frac{sR_pL_p}{R_p + sL_p + 1/sC_p} \tag{4-1}$$

If assuming the load impedance of R_p as 50Ω and choosing proper LC values which satisfy $R_p + sL_p << 1/sC_p$ with the UWB frequency range of interest, Equation (4-1) can be approximated by

$$V_{outp}(s) = s^2 R_p L_p C_p I_{ds3}(s) \tag{4-2}$$

The output voltage V_{out_p} represents the second derivative of the drain current I_{ds3}. Besides, to generate the opposite pulses at the same time for the differential correlator, another parallel path is connected an extra inverter to form a negative pulse for PMOS cascode stage. The negative impulse is shown in Fig.4-6. $R_nL_nC_n$ network is added for the same purpose for $R_pL_pC_p$ network. The final positive/negative waveforms are shown in Fig.4-7 and Fig.4-8.

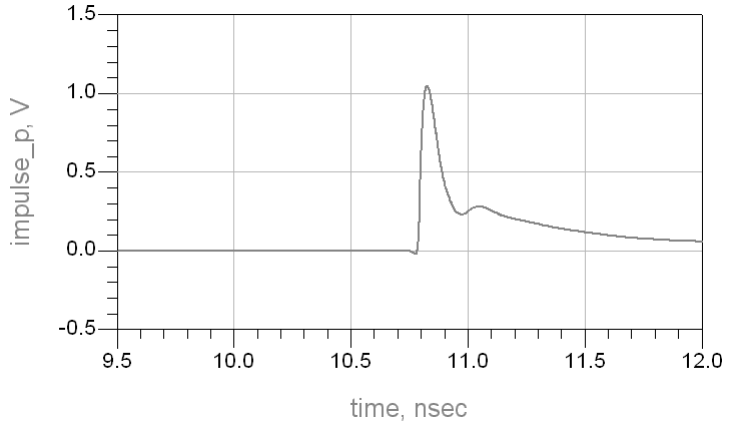


Figure 4-5 Simulation positive impulse generated in V_{x_p}

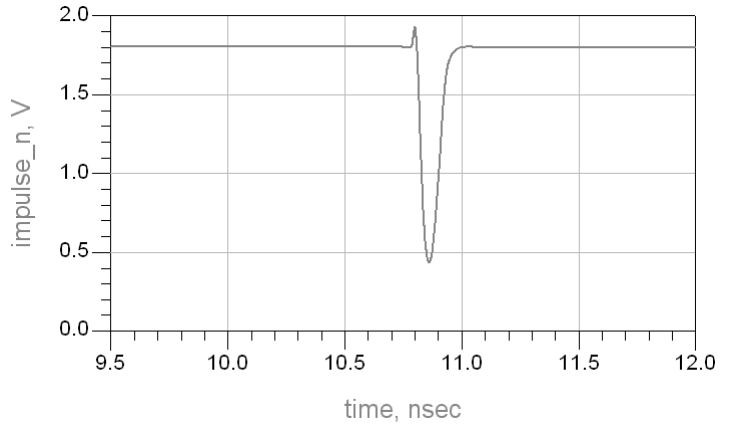


Figure 4-6 Simulation negative impulse generated in V_{x_n}

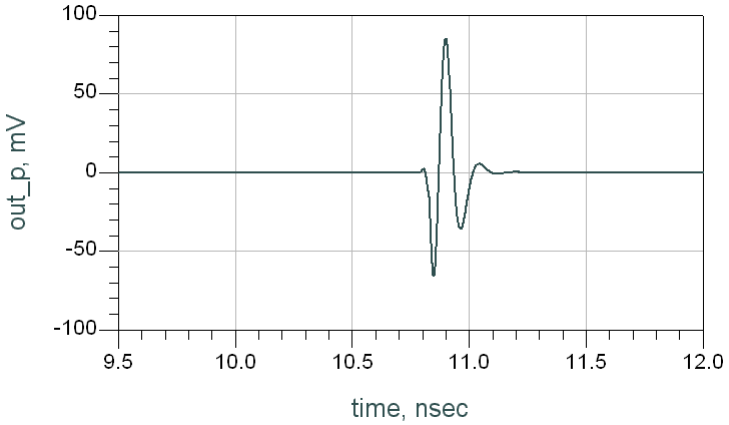


Figure 4-7 Simulation positive 2nd –order Gaussian pulse

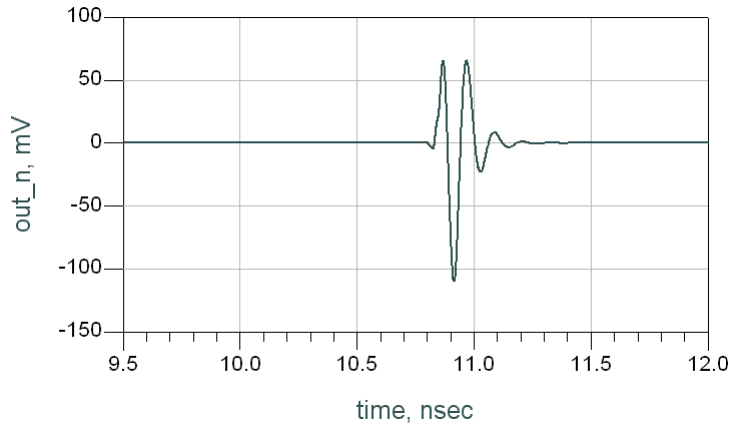


Figure 4-8 Simulation negative 2nd –order Gaussian pulse

4.3 Doubly-Integration, Inductorless, Wideband Correlator

In the previous chapter we have proposed a correlator based on a Gilbert-cell. With dominant pole at the internal node being cancelled, the bandwidth can be increased. However, as a result of the three stacked layer used in the configuration, the Gilbert cell always includes issues of complex pole-zero arrangements, low signal swing, in-band flatness issues as well as bias issues [27]. Due to the transistor operation mode, power consumption is another issue and a new multiplier configuration is need for efficient implementation of UWB systems. To accomplish this design, we apply the four-quadrant multiplier implementation, inductor-less technique, and bandwidth enhancement for the UWB correlator. The simplified block diagram is shown in Fig.4-9.

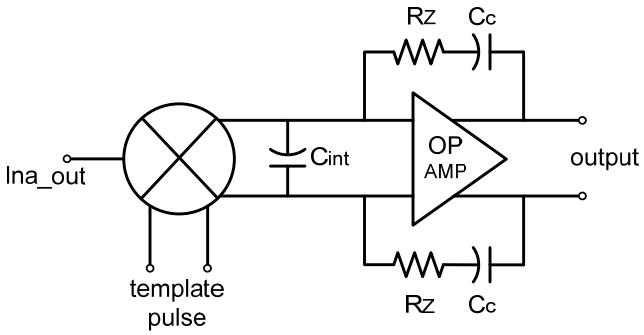


Figure 4-9 Simplified diagram of the proposed correlator

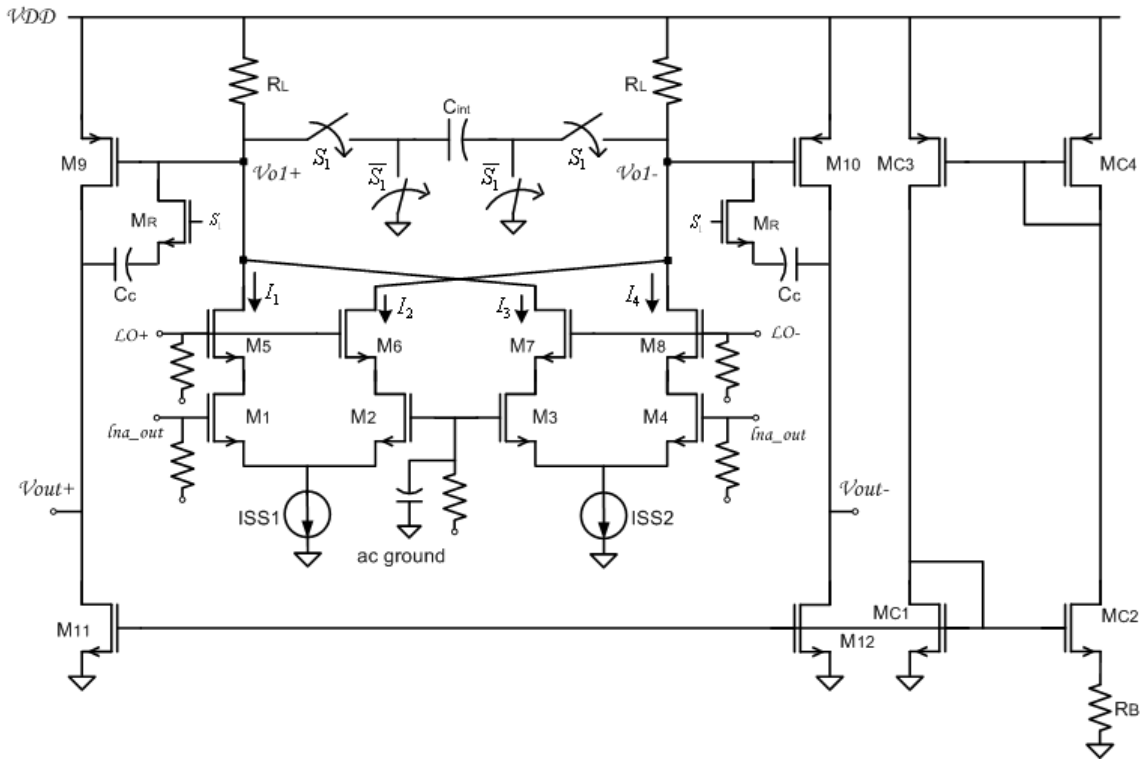


Figure 4-10 Schematic of the proposed correlator

A fully differential four-quadrant multiplier and doubly-integrated mechanism has been proposed in this design. The schematic of circuit is shown in Fig. 4-10. In order to avoid extra single-to-differential balun between the LNA and the correlator, the negative RF input terminal is connected a DC voltage reference and a bypass capacitor is added in it. NMOS M_1 to M_4 operate in triode region and this kind of current is $I_D = k_n\left[(V_{GS}-V_{tn})-\frac{V_{DS}}{2}\right]V_{DS}$. M_5 to M_8 operate in saturation region used as current followers. The output current can be presented as [28]

$$I_{out} = (I_1 + I_3) - (I_2 + I_4) = (I_1 - I_2) - (I_4 - I_3) \tag{4-3}$$

Moreover,

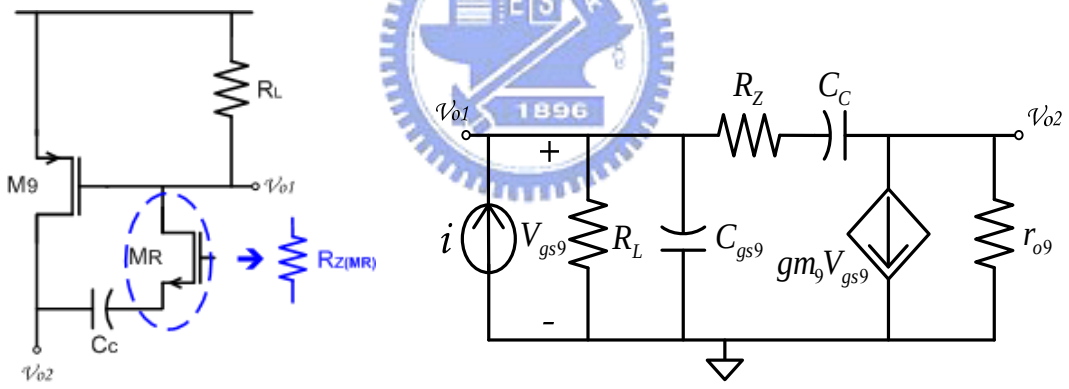
$$\begin{aligned} I_1 - I_2 &= k_n\left[V_X + v_x - V_t - \frac{v_{DSP}}{2}\right]v_{DSP} - k_n\left[V_X - v_x - V_t - \frac{v_{DSP}}{2}\right]v_{DSP} \\ &= 2k_n v_{DSP} v_x \end{aligned} \tag{4-4}$$

Similarly, $I_4 - I_3 = 2k_n v_{DSN} v_x$. According to the above equations we can get the output current I_{out}

$$I_{out} = 2k_n v_x \left(v_{DSP} - v_{DSN} \right) = 4k_n v_x v_y \tag{4-5}$$

Consequently, the output comprises the product of two input signals where $v_{DSP} = V_{DS} + v_y$, $v_{DSN} = V_{DS} - v_y$, V_{DS} is DC biasing when $v_x = v_y = 0$.

The differential outputs of local template pulses are generated by the pulse generator. The capacitor C_{int} is set up between the differential outputs of the quadrant multiplier. Switch S_1 resets the data at the later half-period waiting for the coming of the next data. The signal after first-time integration still has apparent drop and does not last for a long time, so we exploit zero-pole cancelling topology [29] to reach bandwidth extension and double integration simultaneously.



(a) (b)

Figure 4-11 (a) Illustration of frequency compensation skill with zero-pole cancelling (b) Small-signal equivalent model

From Fig.4-11, the method is realized by M_R and C_C. The appropriate C_C value and transistor size of M_R can be chosen for frequency compensation. Assume the transfer function $T(s) = \dfrac{V_{O2}(s)}{V_{O1}(s)}$, and if the zero frequency occurs, $V_{O2} = 0$. We can

get

$$gm_9 V_{gs9} = V_{gs9}(\frac{1}{R_Z} + sC_C) \tag{4-6}$$

$$\omega_Z = \frac{1}{(1/gm_9 - R_Z)C_C} = -\frac{gm_9}{(gm_9 R_Z - 1)C_C} \tag{4-7}$$

While R_Z is the equivalent linear resistor resulting from M_R operating in triode region, the value is

$$R_Z = R_{on(M_R)} = \frac{1}{\mu_n C_{ox}(W/L)_{M_R}(V_{gs} - V_{tn})_{M_R}} \tag{4-8}$$

According to these equations above, we can make the zero to cancel the dominate pole efficiently for bandwidth enhancement. Additionally, the second-time integration is accomplished simultaneously.

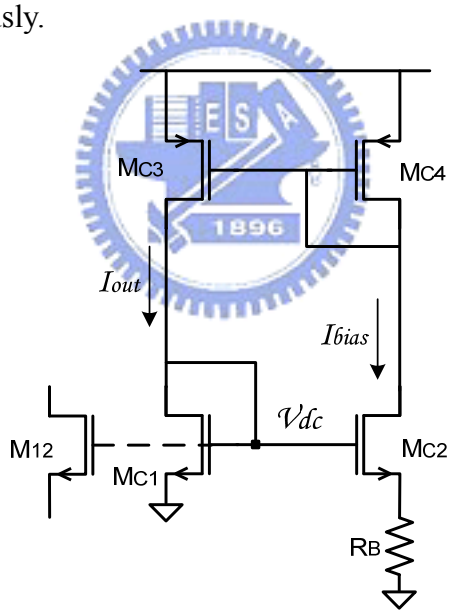


Figure 4-12 The biasing circuit for constant transconductance

In addition, to design a robust correlator, the active load of the operational amplifier must be of high stability. Therefore, a constant transconductance [30] circuit has been added to drive the active load, which is shown as Fig.4-12. The output DC voltage V_{dc} can be deduced as

$$V_{gsC1} = V_{gsC2} + I_{bias}R_B \tag{4-9}$$

$$\sqrt{\frac{2I_{bias}}{\beta(W/L)_{C1}}} + V_{tn} = \sqrt{\frac{2I_{bias}}{\beta(W/L)_{C2}}} + V_{tn} + I_{bias}R_B \tag{4-10}$$

$$I_{bias} = \frac{2}{\beta(W/L)_{C1}} \times \frac{1}{R_B{}^2}\left(1 - \sqrt{\frac{(W/L)_{C1}}{(W/L)_{C2}}}\right)^2 \tag{4-11}$$

$$\therefore\ V_{dc} = V_{gsC1} = \sqrt{\frac{2I_{bias}}{\beta(W/L)_{C1}}} + V_{tn} \tag{4-12}$$

$$= V_{tn} + \frac{2}{R_B\beta(W/L)_{C1}} \times \left(1 - \sqrt{\frac{(W/L)_{C1}}{(W/L)_{C2}}}\right) \quad \propto \frac{1}{R_B} \tag{4-13}$$

The coherent receiver needs for very precisely timing. For example, the clock timing for the pulse generator, integrator, and ADC is illustrated in Fig.4-13. In each period, once the clock rising edge for the pulse generator is synchronized with the received pulse, the multiplied pulse is then produced and the integrator is synchronized with the received pulse, starting integrating operation. A half period of time is used for integration, and the rest time is used for discharging. By the way, the tracking time of the ADC is about one quarter of period ahead of the discharging time, so a stable sampling can be achieved.

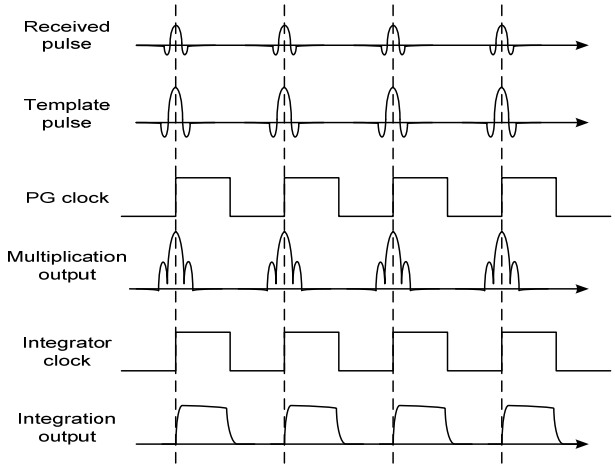


Figure 4-13 The clock timing of the receiver circuit

4.4 Layout Consideration and Simulation Results

Aspect for simulation, we replicate a second-order derivative of Gaussian pulse as the input signal. From Fig.4-14 it shows that the received weak signals can be amplified by the LNA with little distortion. It means that the LNA with transformer feedback matching has broadband characteristic. The voltage gain of LNA is around 17dB. The simulation of differential waveforms of the pulse generator is shown in Fig.4-15(a). An extremely narrow pulse width of 260ps is resulted and the peak value is 220mV, which is suitable for high data-rate transmission. The spectrum spread by pulse is also shown in Fig.4-15(b). The simulation correlated waveform is shown in Fig.4-16. The peak value is 125mV, rise time is close to 1.0ns, fall time is 1.6ns, and hold time is 3.2ns when pulse repetition rate is 110MHz. The spectrum of output waveforms only has two dominant signals, which are DC and 110MHz. The result indicates that the coherent architecture is a type of direct-conversion receiver.

As for the layout plan, short metal-line connection is the prior consideration because of avoiding uncertainly parasitic effects. Fig.4-17 shows the layout of the integrated circuit. The distance between the transformer of LNA and other transmission lines is away from 50um at least. This manner is for reducing large coupling effect. The layout of PG is located at the lower section of Fig. 4-17. The proposed correlator is an inductor-less circuit, so it can minimize the overall chip area. In order to measure output waveform by the oscilloscope, the output resistance must be 50 ohm. The architecture of open drain is used for the sake of measurement. Serial MIM capacitors which replace transmission lines not only add by-pass capacitance but also reduce parasitic influence of long metal lines. The overall area occupies 1.23mm×1.2mm including pads.

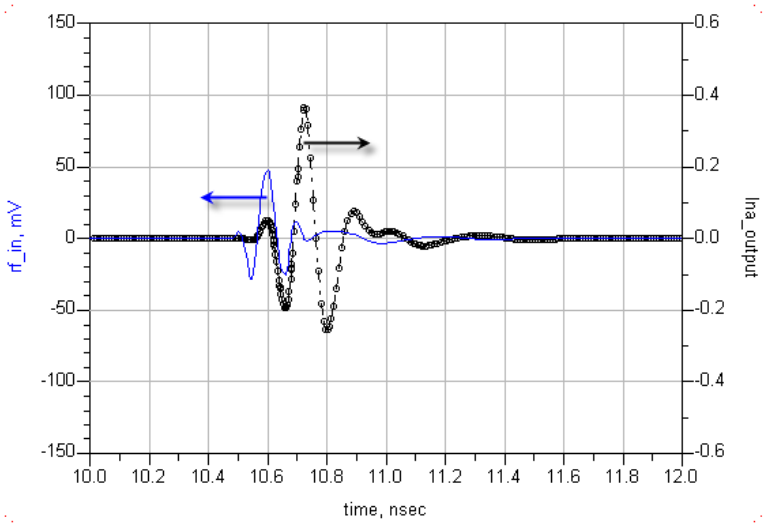
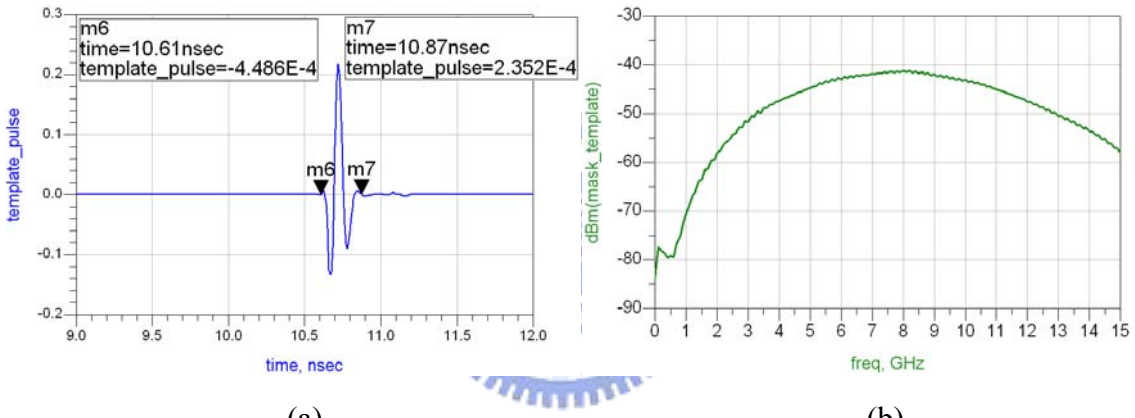


Figure 4-14 Received pulse and amplified pulse by LNA



(a) (b)

Figure 4-15 (a) Differential output of pulse generator (b) Spectrum allocation

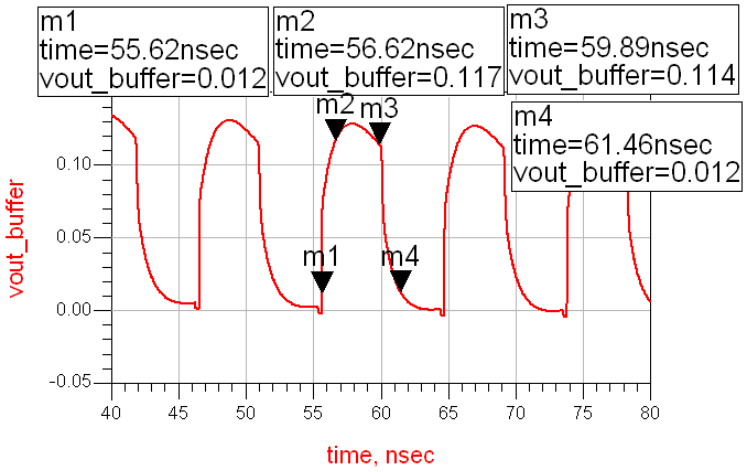


Figure 4-16 Output waveforms

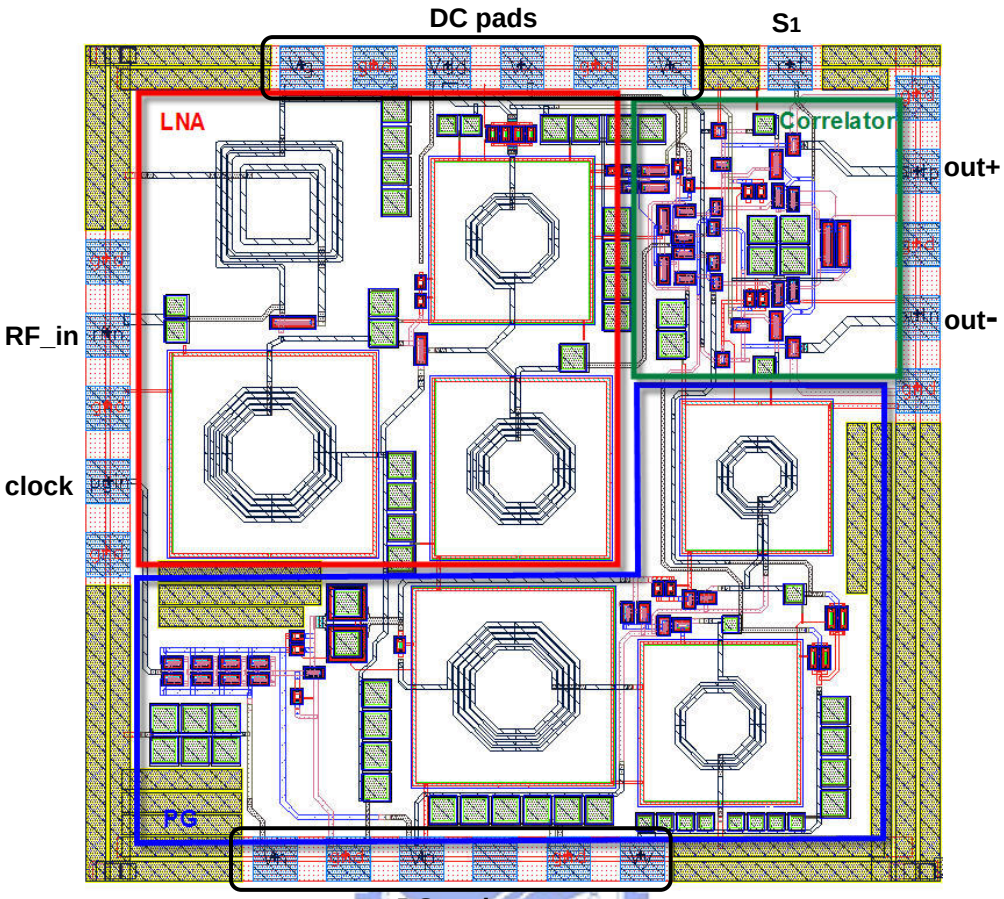


Figure 4-17 Layout of the proposed front-end receiver

4.5 Measurement Results

4.5.1 Measurement Environment

Referring to measurement consideration, we adopt on-wafer probing. The overall measurement environment is shown as Fig.4-18. The LNA input port is fed by the 2nd-order Gaussian pulses generated from a practical generator, whose photo and experimental waveform is shown in Fig.4-19. The clock signal which amplitude is ± 1.8V feeding the input port of the pulse generator. The switch port is connected to the clock signal which delay half a period of the clock of pulse generator. The pulse repetition rate is 110MHz at the overall demonstrative measurement. Besides, in order to measure the output waveform, the output buffer adopts the open-drain stage to match

50Ω. Thence we must add extra bias-tee at the output port. The bias tee is a three port network; RF is fed into one port and DC into another, while RF and DC depart together from the third port. The bias-tee needs large driving current for good matching.

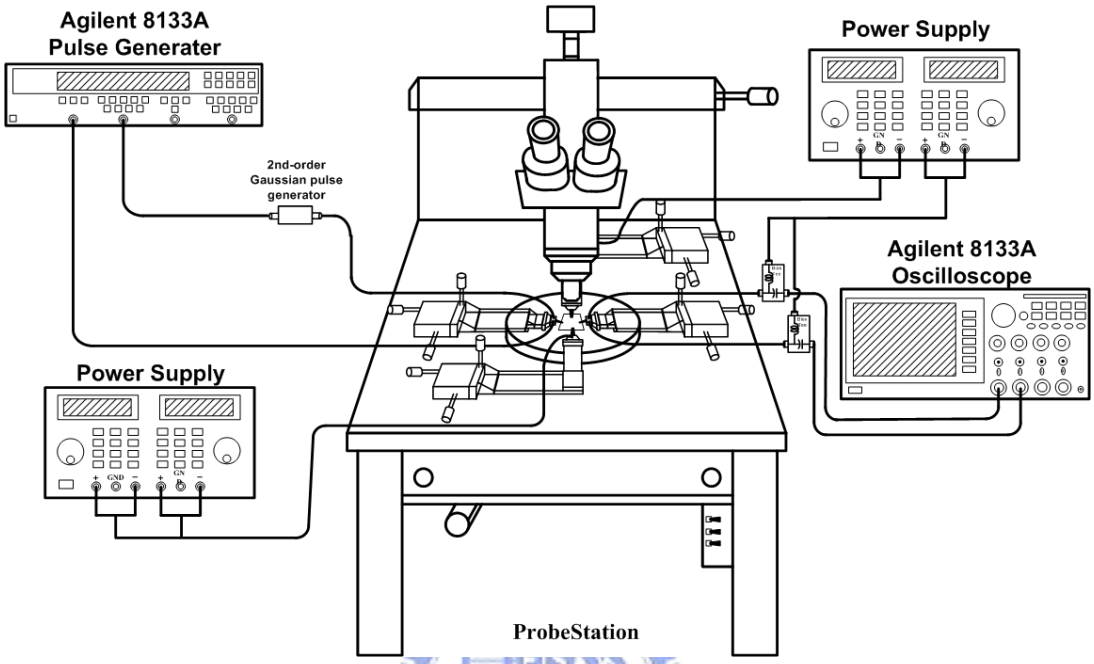
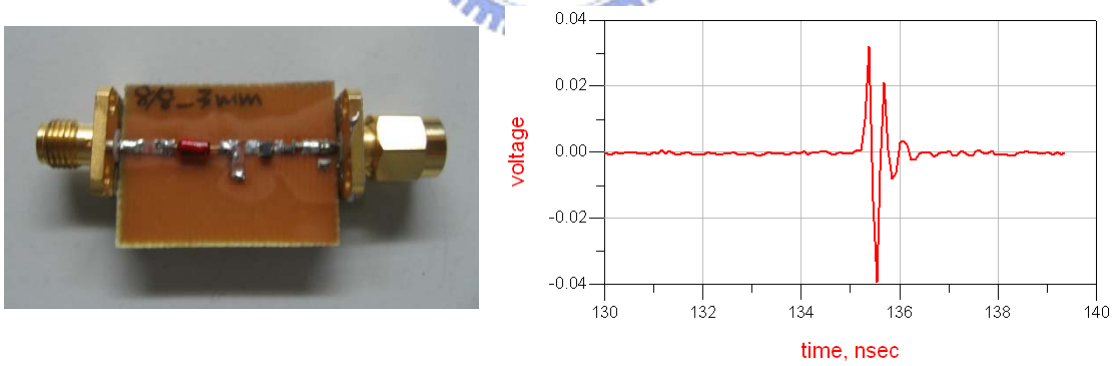


Figure 4-18 Diagram of measurement setup



(a) (b)

Figure 4-19 (a) Practical 2nd-order Gaussian pulse generator (b) Measured waveform

4.5.2 Measurement Results and Discussion

An integrated pulse based UWB receiver using the coherent architecture is fabricated by TSMC 0.18μm RF CMOS process. The die microphotograph is shown in

Fig.4-21 with chip size 1.48 mm^2 . The measured differential output waveform is shown in Fig.4-22. We observe that the rise time is around 1.8ns, the fall time is 1.3ns, and the hold time is 2.2ns. The peaked amplitude of output waveform is 140mV when the input peaked value is 40mV. Except from the pulse shaping circuit of the pulse generator and the output buffer, the core power consumption is 19.96mW with 110MHz pulse repetition rate. The summary of the simulation and measurement results is list in Table 4-1. It can be observed that the rise time of simulation is faster than practical experiment, but the fall time of simulation is slower than experiment. The reasonable explanation may be that the actual parasitic capacitance at the charging path is more than the predicted value and leads to large RC time constant. At the discharging path, these switches consisting of transistors are controlled by an independent signal, so the practical fall time is shorter than simulation. However, we can still demonstrate that the front-end receiver works functionally.

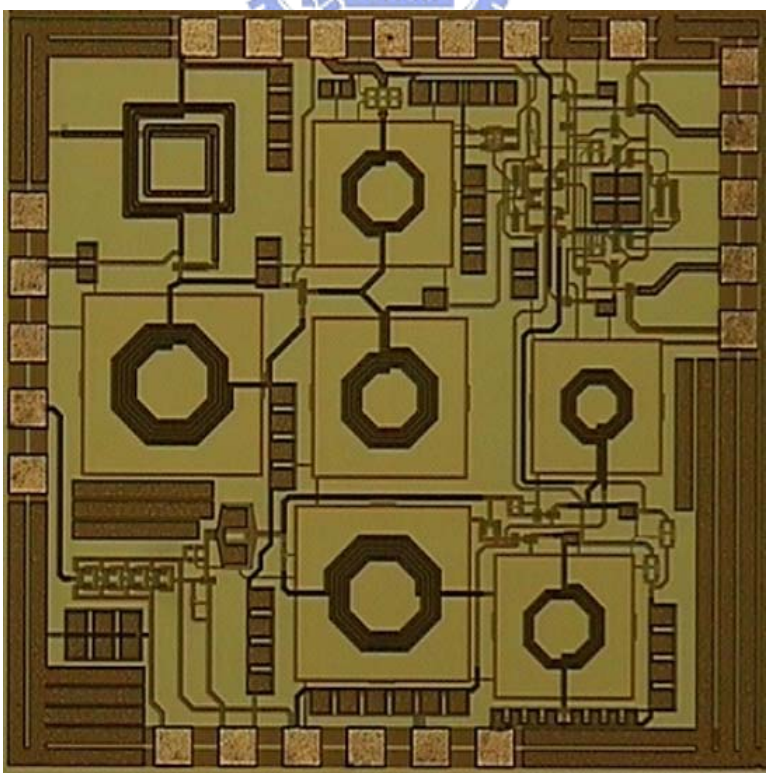


Figure 4-20 Microphotograph of the proposed front-end receiver

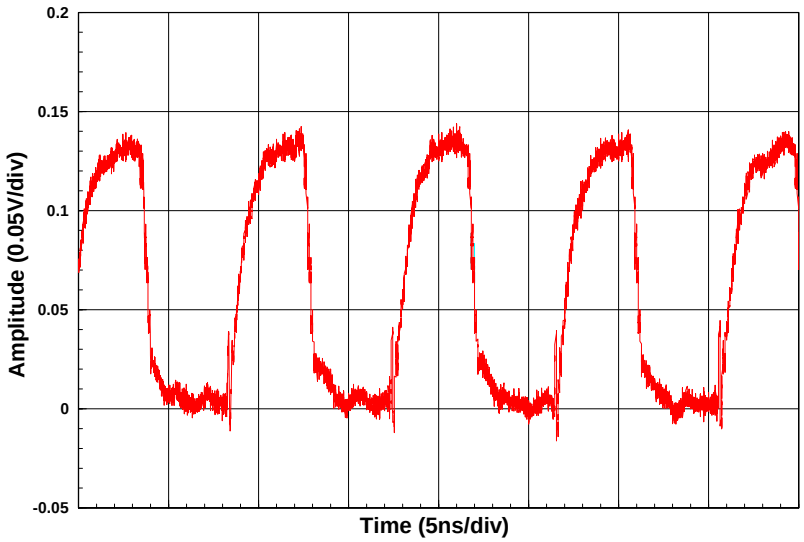


Figure 4-21 Measured output waveforms

Table 4-1 Comparison of simulation and measurement results of the receiver

	Simulation results	Measurement results
Technology	TSMC 1P6M 0.18μm	
Supply voltage(VDD)	1.8 V	
Operating frequency	~10GHz	
Pulse repetition rate	110 MHz	
Pulse width	260 ps	
Max. Vout amplitude	126 mV	140 mV
Rise time	1.0 ns	1.8 ns
Hold time	3.2 ns	2.2 ns
Fall time	1.6 ns	1.3 ns
Power consumption (core) @100MHz UWB pulse repetition rate	18.34 mW	19.96 mW
Chip area	1.228mm×1.205mm	

Chapter 5

Conclusion and Future Works

5.1 Conclusion

Ultra-wideband is a promising technique which possesses low power consumption and high data rate. Due to the outstanding characteristics of UWB, we focus on researching the receiver design and implementation. In Chapter 3, the proposed LNA and correlator used in UWB systems are introduced. The LNA exploits transformer feedback matching instead of the conventional matching method to achieve broadband matching and acceptable noise performance. As to gain stage, current-reuse technique reduces dissipation and obtains adequate gain simultaneously. The measured results show that S11, S21, S22 are similar to simulation results. The average NF is 4 dB. The minimum IIP3 is -5 dBm. It illustrates that the topology is feasible in UWB system. Referring to the correlator, the Gilbert multiplier is adopted and inductive peaking of the load stage is used for achieving wideband feature. Variable gain control is another feature at the correlator. Besides, double integration is used for longer hold time for circuits of the next stage. The practical measured results show that the rise time and hold time are inferior to simulation performance. The dynamic gain range of measurement is 36-89mV, which is also lower than simulation. The reason may be due to bond wire at each port or imperfect pulse source. But the performance has the trend to match the expectative result as well.

Finally, the integrated front-end receiver is presented in Chapter 4. The proposed front end of receiver which comprises a UWB LNA, a 2^{nd}-order derivative Gaussian pulse generator, and a wideband correlator is presented. The switched pulse generator is applied for reducing static power dissipation. Differential output is designed for the

purpose as template pulse of the receiver. The double integration correlator has long enough hold time for next stage, and the inductorless architecture can reduce the overall chip area and achieve broadband characteristic simultaneously. The proposed receiver front end had been integrated in a single chip by TSMC 0.18μm process. The measured results demonstrate that the front-end receiver can achieve a transmission rate over to 110Mb/s, and it conforms to the characteristic of the desired transmission rate in the IR-UWB communication systems.

5.2 Future works

IR-UWB communication systems have many unusual advantages compared with conventional communication systems, such as low complexity, low duty cycle, high immunity to other interference and high security. These features are much deserved to research for advanced specification. Although IEEE 802.15.3a standard is announced that the task group disbanded in 2006, but many industrial and academic organizations still go for investigation in this field. It can be expected that UWB systems can be accepted extensively in wireless-communication life. In the short term, we will develop toward chip integration by the advanced CMOS process. In this thesis, a prototype of the front-end receiver of IR-UWB systems is proposed. We hope that the achievement can provide a good design guide of IR-UWB communication systems.

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