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連續時間轉導電容式三角積分調變器之實現

Implementation of the continuous-time transconductor-capacitor Delta-Sigma modulator

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中 華 民 國 九 十 六 年 十 月

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摘要

由於近年來無線通訊蓬勃發展，因此適用於無線通訊中的類比數位轉換器也受到更大的矚目。一般無線通訊常爲窄頻通訊，爲了簡化架構通常希望類比到數位轉換器在頻帶內可有更高的抗雜訊能力。另一方面也希望能夠在低電壓、低功率下操作，因此，一個高解析度、低功率耗電且面積小的類比數位轉換器是很重要的。而三角積分類比數位轉換器就非常符合這個需求，因爲它在有限頻寬的限制下可以達到非常高的解析度。除此之外，類比所佔的成份也相對比較少且對製程漂移的影響也比較小。因此，近幾年來三角積分類比數位轉換器都扮演著非常重要的角色。

三角積分類比數位轉換器在不同的應用範圍下通常會有兩種種類，一種是離散時間三角積分類比數位轉換器，因爲它通常都是用交換電容的電路下實現，所以又稱爲交換電容三角積分類比數位轉換器。早期論文以離散時間三角積分類比到數位爲主，但是 2002 年以後，連續時間三角積分類比到數位則大量的被發表。原因爲連續時間三角積分通常對於運算放大器的要求比較寬鬆，它不需要在一個 clock 的時間下做處理，所以耗費功率比較低，而且具有 Anti-aliasing 的性質。

因此，爲了將連續時間三角積分類比數位轉換器的優點應用在通信的範圍內，此研究主題就是做出一個適用於 GSM 系統 200k 赫茲頻帶、取樣頻率 20MS/s 的低功率三階零點最佳化的連續時間轉導電容三角積分類比數位轉換器，以符合可攜式電子產品需要低消耗功率的趨勢。

晶片是以台積電 0.18 微米標準互補式金氧半導體製程所製造。在 200k 赫茲頻帶內的量測結果爲：最大訊號雜訊失真比爲 45dB，訊號雜訊比爲 47.8dB，動態範圍是 49dB，解析度爲 7.2 位元，與預測結果相差約 4 位元。

Implementation of the continuous-time transconductor-capacitor Delta-Sigma modulator

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Abstract

Because of the rapid growth of wireless communication, there has been more focus on analog-to-discrete converter (ADC) for wireless communication. Since the frequency is usually narrow-band in general wireless communication, in order to reduce the complexity of the architecture, we usually require the ADC has the ability of in-band anti-noise. Besides, it is important the ADC operates in low voltage, low-power, and small area. The delta-sigma (ΔΣ) ADC is very suitable for the application because they can achieve high accuracy for narrow band signals with few analog components and insensitivity to process and component variation.

Typically, there are two kinds of ΔΣ ADCs. The first one is the discrete-time (DT) ΔΣ ADC and the other is the continuous-time (CT) ΔΣ ADC. The DT ΔΣ ADC also called the switched-capacitor (SC) ΔΣ ADC because of using switched capacitors. The CT ΔΣ ADC obtains lots of attentions lately. Because the requirement of integrator is relaxed, it does not need to process signals within a clock time. This results in further power reduction.

In order to combine the advantages of the CT ΔΣ ADC system into low-power communication system, this research focuses on low power 20MS/s sample frequency 3-rd order zero optimization CT GM-C ΔΣ ADC for GSM communication system.

The chip has been fabricated by TSMC 0.18-um CMOS process. The measured peak SNDR is 45dB, SNR is 47.8dB and the DR is 49dB. The resolution is 7.2 bits that is 4 bits lower than prediction in 200k HZ signal band.

誌謝

隨著這份碩士論文的完成，兩年來在交大的求學生活也即將告一個段落，往後迎接著我的，又是另一段嶄新的人生旅程。本論文得以順利完成，首先，要感謝我的指導教授洪崇智老師在我兩年的研究生活中，對我的指導與照顧，並且在研究主題上給予我寬廣的發展空間。而類比積體電路實驗室所提供完備的軟硬體資源，讓我在短短兩年碩士班研究中，學習到如何開始設計類比積體電路，乃至於量測電路，甚至單獨面對及思考問題的所在。此外要感謝李育民教授、黃淑娟教授、陳科宏教授撥冗擔任我的口試委員並提供寶貴意見，使得本論文更為完整。也感謝國家晶片系統設計中心提供先進的半導體製程，讓我有機會將所設計的電路加以實現並完成驗證。

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吳國璽 于 交通大學工程四館 718 實驗室
2007.10.9

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CH1 Introduction

1.1 Research Motivation

Nowadays, the demand for the wide band communications is driving the advancement of the digital modulation techniques and the increasing complexity of circuits. For this purpose, the analog signal processing is replaced with the digital signal processing circuit in the receiver.

Besides this, the complexity and single-chip integration of the analog circuit in the receiver chain can also be implemented by a proper architecture. As shown in Fig.1.1, by pushing the A/D converters close to the antenna, the total analog components in the receiver chain will be reduced.

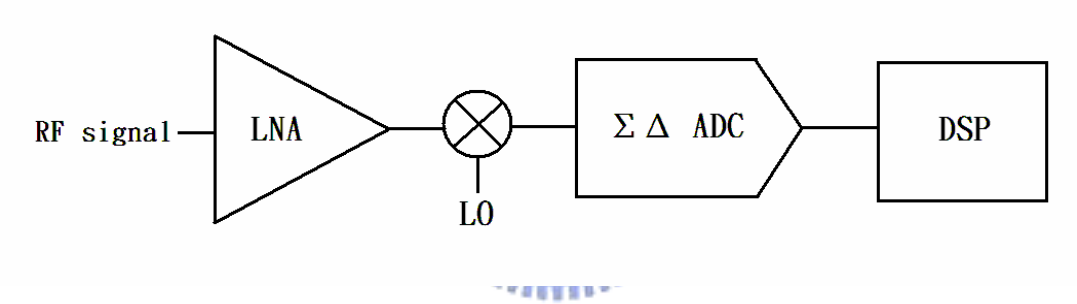


Fig 1. 1 Application of ΔΣ ADC in communication receiver

Many design challenges, however, exist when the A/D converters move close to the antenna. It is challenging to achieve high-resolution, low-voltage and low-power operation in high-performance communication systems. Without the switched -capacitor circuits in continuous-time delta-sigma ADCs, the requirements of the transconductance amplifiers(GM) are more relaxed and the power consumption of the GM are thus greatly reduced. In addition to this, the speed of the continuous-time circuits is not limited to the settling time of the charge, and the wide bandwidth is more easily attained. The over-sampling techniques with noise shaping strategy are widely used to implement the analog-to-digital interface between analog and digital domain in digital systems. This type of systems require high resolution or low power consumption. Sigma-delta data

converters have meaningful advantages over traditional Nyquist-rate counterparts. The anti-aliasing filter is usually in front of the switched capacitor circuits to avoid the aliasing effect. However the filter is not required in the continuous-time delta-sigma ADC, that further simplify the receiver design.

CH2 Problem Definition

2.1 Continuous-Time vs. Discrete-Time ΔΣ Modulators

The general structures of DT and CT ΣΔ modulators are shown in Figures 2.1 and 2.2 respectively.

In the following we will discuss the main advantages of CT ΣΔ modulators over their DT counterparts.

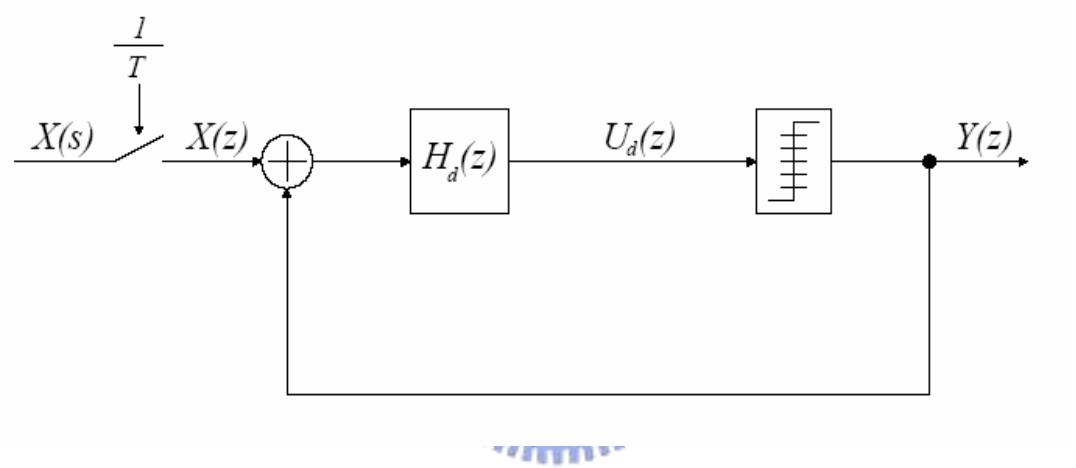


Fig 2. 1 Discrete-time ΔΣ modulator

Low Voltage Operation:

The continuously decreasing supply voltage of recent CMOS technologies is causing important limitations to the performances of switched-capacitor circuits. Switch-bootstrapping or switched-OPamp circuit techniques are now necessary in order to obtain sufficiently low on-resistances.

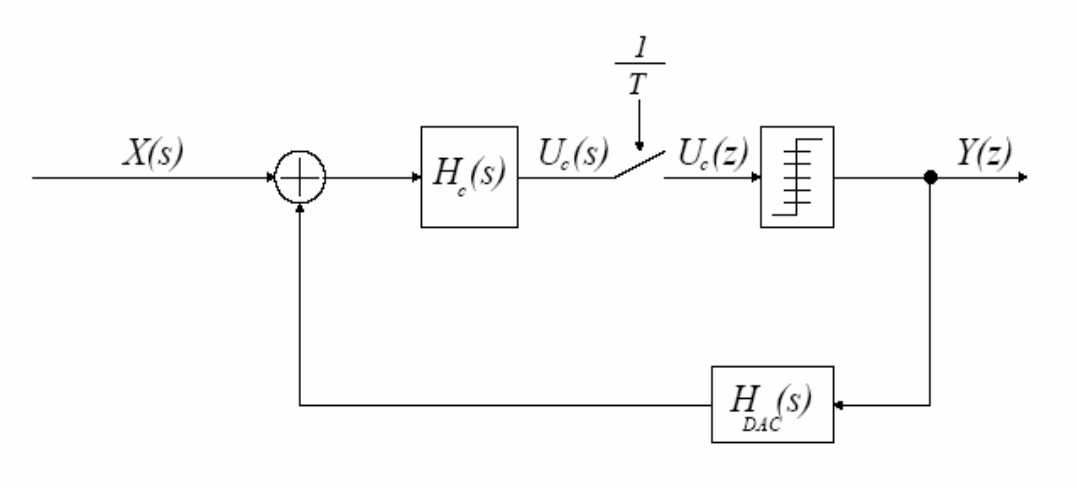


Fig 2. 2 Continuous-time ΔΣ modulator

Sampling Frequency:

In switched-capacitor circuits several errors occur while sampling the input signal. These errors are due to the switch non-linearity, charge injection, clock feedthrough and finite settling time. Sampling errors in switched-capacitor circuits limit the sampling frequency, fs, of DT ΣΔ modulators.

In CT modulators sampling occurs inside the ΣΔ loop, therefore sampling errors are shaped out of the frequency band of interest just like quantization noise.

Power Consumption:

In switched-capacitor circuits the unity gain frequency of operational amplifiers must be at least five times the sample rate. High quiescent current is then required to achieve high bandwith. On the other hand, unity gain frequencies of the integrators in the CT ΣΔ are usually lower than the sampling frequency.

Furthermore, since sampling occurs inside the ΣΔ loop, this strongly reduces:

. Thermal noise is aliasing in the frequency band of interest.

. Aliasing of out of band signals, so that the antialiasing filter may be eliminated.

It is then expected that for the same specifications, CT ΣΔ modulators will have lower

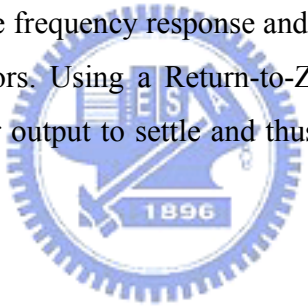
power consumption than their DT counterparts.

It has also been shown, in [1], that CT ΣΔ modulators are less sensitive to asynchronous substrate interference from neighboring digital circuitry than DT ΣΔ modulators. This will be an important issue for future SOC (System on Chip) design.

While DT ΣΔ modulators are insensitive to the shape of the feedback signal as long as full settling occurs, the main disadvantages of CT ΣΔ modulators are related to switching characteristics of the feedback signal:

Excess Loop Delay:

The delay in the feedback signal is mainly due to the comparator response-time. This delay has been found to alter the frequency response and degrade the signal-to-noise ratio (SNR) of the CT ΣΔ modulators. Using a Return-to-Zero (RZ) feedback signal gives enough time for the comparator output to settle and thus eliminates any influence of the comparator delay on the SNR.



DAC Output Rise and Fall Time Asymmetry:

Unequal rise and fall times of the DAC output current introduces harmonic distortion. The effect of this waveform asymmetry can also be highly attenuated by the use of a RZ feedback DAC.

Clock Jitter:

Clock jitter in feedback signal increases the noise level in the signal band. Unlike excess loop delay and DAC waveform asymmetry, clock jitter influence on the CT modulators cannot be attenuated by a RZ feedback signal.

After this discussion on the advantages and disadvantages of CT ΣΔ modulators compared to the DT ΣΔ modulators (summarized in tables 2.1 and 2.2), we believe that CT modulators will play an important role in recent and future CMOS technologies. This is mainly because of their advantages concerning low voltage, low power and high sampling frequency.

Table 2.1 Main advantages of continuous-time ΣΔ modulators over DT ΣΔ modulators

	DISCRETE-TIME ΣΔ	CONTINUOUS-TIME ΣΔ
Input Switch Resistance	$r_{ds} = \frac{1}{\beta(V_{gs}-V_t)}$	No input switches
Sampling Errors	Critical	Shaped out of band
Unity Gain Frequency	$f_T = 5 * f_s$	$f_T \leq f_s$
Thermal Noise Aliasing	Increases noise level	Highly attenuated
Anti-Aliasing Filter	Essential	May be discarded

Table 2.2 Main disadvantages of continuous-time ΣΔ modulators compared to DT ΣΔ modulators

	DISCRETE-TIME ΣΔ	CONTINUOUS-TIME ΣΔ
Excess Loop Delay	Low sensitivity	SNR degradation
Rise and Fall Time Asymmetry	Low sensitivity	Introduces harmonic distortion
Clock Jitter	Low sensitivity	Increases noise level

In the following, we will discuss the main difficulties and the different issues associated with the design and implementation of CT ΣΔ modulators.

2.2 Single-bit vs. multi-bits ΔΣ Modulators

The ADC resolution at a low OSR can be improved by using a higher-order loop filter, and/or by increasing the internal quantizer resolution. For single-bit, single-loop modulators, the integrator's gain must be reduced to preserve the loop stability. Therefore,

simply increasing the loop filter order at a low OSR will result in a poor SNR improvement.

Since multibit quantizers have a more linear gain than single-bit quantizers, the stability of multibit, single-loop SD modulators is significantly improved. As a result, more aggressive noise transfer function can be designed, with the benefit of extra dynamic range for every additional bits *n* of DR $\propto$ 20 log (2^n - 1) dB.

Alternatively, increasing quantizer resolution enables us to use a lower noise-shaping filter for a given OSR. Unfortunately, it is necessary to double the number of comparators for each additional bit of quantizer resolution. Obviously, this costs silicon area as well as

power dissipation and thus degrades the FOM for a given resolution In addition, multi-bits SD ADCs are sensitive to non-idealities such as mismatch in the feedback digital-to-analog converter (DAC), as these errors are added directly to the input signal and are thus not noise-shaped.

Nevertheless, deep-submicron technologies feature excellent matching characteristic as high as 11 bits or 12 bits of resolution. Hence, careful layout and design can fulfill linearity requirements of an internal-feedback DAC, provided that the SD ADC is lower than 12-bit resolution, which is typically the case for W-CDMA.

For a SD ADC's resolution that exceeds the matching possibilities of CMOS or Bi-CMOS, this problem must be addressed. The solution consists of using dynamic element matching (DEM).

DEM converts the DAC element errors to high frequency noise. Thereby, highly linear over-sampling DAC can be built with only moderate matching requirements for the DAC element.

DEM techniques have been developed since 1998, starting with randomization of the DAC elements. The methods are continuously improved with respect to implementation efficiency and order of shaping. Since the presentation of [2] in 1995 and the disclosure of the ADC design in 1997, these techniques have been well established in the sigma

delta design community, allowing efficient and robust implementation of sigma-delta ADC's with resolution of more than 14 bits and bandwidth beyond 1 MHz.

However, the single bit should be preferred to multi-bit SD ADCs when the conversion bandwidth is lower than 5 MHz (GSM, Bluetooth, W-CDMA) because they achieved better FOM and are less silicon area-consuming.

2.3 Active RC vs. GM-C filter ΔΣ Modulators

Active RC integrator has an amplifier in feedback loop and gives better **linearity performance** than a GM-C integrator. In a GM-C integrator, the transconductor is in open loop and hence you would expect lower linearity than an amplifier operating in a feedback loop.

In a CT sigma-delta (or for that matter any sigma-delta), the linearity of the overall system is limited by the linearity of the first stage and the linearity of the DAC connected to the first stage (higher OSR helps to suppress this requirement to some extent). The linearity of the subsequent stages is masked by the loop gain upto that stage, so the 2nd and 3rd stage does not have very stringent linearity requirements. Because of this reason, **it is preferable to have active-RC integrator as first stage**.

The main disadvantage of active-RC is that the **amplifier bandwidth** has to be high enough to operate in feedback configuration. In addition, it needs to have **enough gain** in the signal bandwidth to provide good linearity (linearity is related to gain at that frequency, **higher the amplifier gain** in the signal frequency, better is the linearity). The gm of GM-C integrator has lower gain bandwidth requirement since it operates in open loop and hence can consume lower power.

So in terms of power optimization, first stage has active-RC (higher power) and subsequent stages have GM-C (lower power). Overall, this arrangement gives best performance optimum power consumption.

However, linearity of the DAC connected to the first stage should be => linearity of the

first stage active-RC integrator.

Advantage of an all GM-C would be lower power at the cost of lower linearity. Input referred noise comparison cannot be generalized as it depends on the value of R in the active-RC integrator, but the R values can be adjusted such that input referred noise of active-RC integrator can be made lower than the GM-C integrator, which implies a higher dynamic range if active-RC integrator is used as the first stage.

2.4 Conclusion

The published SD ADCs for wireless applications have been reviewed for the 2002-2004 period. Since 2003, there has been a strong trend to increase the bandwidth conversion while keeping reasonable clock frequency. This means that the OSR tends to decrease.

As a result, multi-bit SD loops are preferred for bandwidth demanding applications such as WLAN. However, single-bit SD modulators are recommended for wireless applications that require less than 5 MHz conversion bandwidth because they offer better trade-offs for power, area and circuit complexity. Moreover **CT SD modulators** are suited for a **low-cost integration** because they provide anti-aliasing filtering without silicon-area penalty and can potentially operate with less power consumption than DT implementation. At least, **single loop topology is preferable in low-voltage, low-power designs** because it is less sensitive to analog circuit non-idealities, such as insufficient op-amp dc gain that tends to decrease at each CMOS technology node.

CH3 An Overview of Sigma Delta Data Converters

3.1 Introduction

This chapter reviews the basic concept of design the sigma-delta data converter. The discussion begins with a brief overview of data converter in the aspects of speed, resolution, and architecture. After this issue, the theories of how sigma-delta modulators work including sampling, quantization, over-sampling, and noise shaping will be discussed. Following the introduction, tradeoffs of various sigma-delta modulator architectures will be discussed.

3.2 Overview of Analog-to-Digital Data Converters

The operations of analog-to-digital data converters can be roughly separated into two steps: sampling and quantization. The process of sampling transforms continuous time analog signals into discrete time step-like signals. The process of quantization converts the step-like signals to a set of discrete levels. Then, these discrete levels signals can be coded and be transmitted into DSP units or digital systems.

3.2.1 Categories of Analog-to-Digital Data Converters

According to operation, speed, and accuracy, there are three categories of analog-to-digital converter shown in Fig.3.1. Each category is applied in different field. But the demarcation for some structures nowadays is a little blurred.

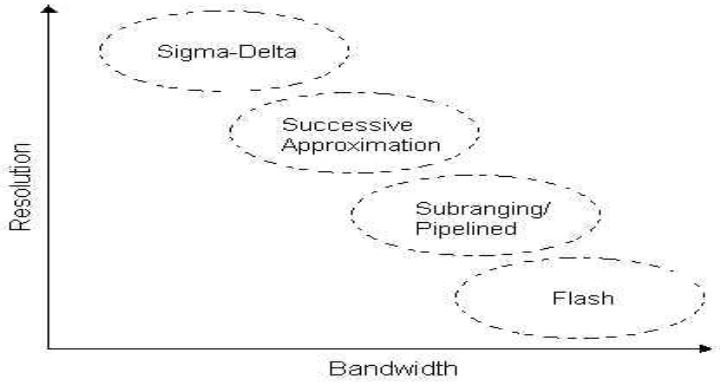


Fig 3. 1 A/D Converter technologies, resolution and bandwidth

3.2.2 Over-sampling Ratio (OSR)

The over-sampling ratio (OSR) of a data converter is defined as

$$OSR = \frac{f_s}{2 f_b} \tag{3.1}$$

where f_s is the sampling frequency and f_b is the signal bandwidth. When the OSR is equal to 1 ($f_s = 2 f_b$), it means the data converter is the Nyqist-rate data converter, however, when the OSR is great than 1, it means the data converter is the over-sampling data converter. The OSR is the important parameter for over-sampling data converters. The OSR increases the SNR by $(2n+1)\cdot 3\text{dB}$ or by $2n+1$ per octave, where n is the order of loop-filter.

The larger the OSR, the larger the sampling frequency when the signal bandwidth is fixed. Thus, it will need faster circuit and consume more power consumption. But the OSR need to keep as low as possible for high signal bandwidth consideration. In order to obtain the advantages of using noise- shaping strategy, the OSR should be at least 4 [3].

3.2.3 Signal to Noise Ratio (SNR) & Spurious Free Dynamic Range (SNDR)

The signal-to-noise ratio (SNR) of a data converter is the ratio of the signal power to the noise power, which measured at the output of the data converter. The maximum SNR that a converter can achieve is called the peak signal-to-noise ratio. Generally, the theoretical value of SNR for an N-bit Nyquist-rate ADC is given by

$$SNR = 6.02 \cdot N + 1.76 \quad dB \tag{3.2}$$

But for over-sampling ADC, the theoretical value of SNR is

$$SNR = 6.02 \cdot N + 1.76 + 10\log(OSR)\ dB \tag{3.3}$$

The signal to noise and distortion ratio (SNDR) of a data converter is the ratio of the signal power to the power of the noise plus the harmonic distortion components, which measured at the output of the data converter. The maximum SNDR that a converter can achieve is called the peak signal to noise and distortion ratio. Generally, SNDR is lower than SNR.

3.2.4 Spurious Free Dynamic Range (SFDR)

The spurious free dynamic range (SFDR) is defined as the ratio of rms value of amplitude of the fundamental signal to the rms value of the largest harmonic distortion component in a specified frequency range. SFDR may be much larger than SNDR of a data converter.

3.2.5 Dynamic Range at the input (DR)

The dynamic range is defined as the ratio between the power of the largest input signal which didn't significantly degrade the performance and the power of the smallest detectable input signal which is determined by the noise floor of converters.

3.2.6 Effective Number of Bits (ENOB)

For data converter, a specification often used in place of the SNR or SNDR is ENOB, which is a global indication of how many bits would be required to get the same performance as the converter. ENOB can be defined as follows:

$$ENOB = \frac{SNDR - 1.76}{6.02} \quad bits. \tag{3.4}$$

3.2.7 Overload Level (OL)

OL is defined as the relative input amplitude where the SNR is decreased by 6dB compared to peak SNR value.

3.3 Sampling Theorem

Naturally, signals transmitted in the air are analog whether they originate from. The analog signals need to be sampled to become the digital signals for suitability in processing in the digital system. Thus, sampling is a very important procedure in the front end of the overall system. How much information can be preserve from the original signals depend on how fine to sample the signals and deal. It is crucial to choose the sampling frequency with a fixed signal bandwidth. And the relationship between the sampling frequency, f_s, and the signal bandwidth, f_b, is shown as follows :

$$f_s \geq 2f_b \tag{3.5}$$

At least the sampling frequency must be greater than twice the input signal bandwidth to avoid aliasing. If f_s is smaller than twice the signal bandwidth, aliasing will occur at the output signal spectrum as shown in Figure 3.2.

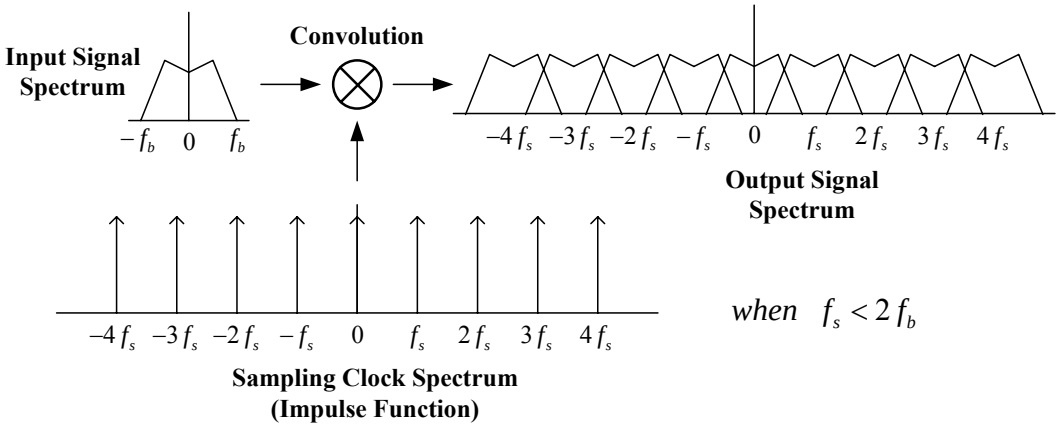


Fig 3. 2 Illustration of the aliasing of the sampling process $(f_s < 2f_b)$

To deal with these problems is increasing f_s to new sampling frequency f_{ns} in

order to match the equation. The frequency f_{ns} show be larger than $2f_b$ .This is more popular to deal with aliasing problems because there is no information of original input signal loss as shown in Figure 3.3. And just a low pass filter at the output is needed to recover the original signal.

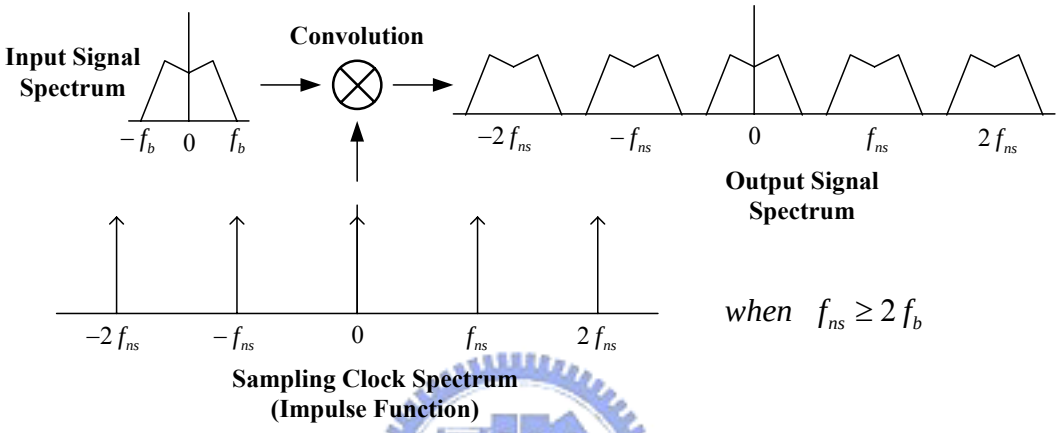


Fig 3. 3 Illustration of the aliasing of the sampling process ($2f_b \leq f_{ns}$)

3.4 Quantization Noise

The quantizer is the interface between analog and digital domain. Once the analog signals pass through the quantizer, the signals will be digitized and separated into several different levels. The space between two adjacent levels is called a step size, Δ. There are two types of quantizer. One is uniform, and another is non-uniform. In a uniform quantizer, the distance between two adjacent levels is uniform; otherwise it is a non-uniform quantizer.

The process of quantization introduces an error, q(n). The error is defined as the difference between the input signal, x(n), and the output signal, y(n). And it is called the quantization error. Figure 3.4 and Figure show the quantization process and assume the quantizer is uniform.

Many of the original results and insights into the behavior of quantization error are due

to Bennett [4]. Bennett first developed conditions under which quantization noise could be reasonably modeled as additive white noise. A common statement of the approximation is that the quantization error has the following properties, which we call it the "input-independent additive white-noise approximation" [5]:

a. q(n) is statistically independent of the input signal

b. q(n) is uniformly distributed in [-Δ/2, Δ/2]

c. q(n) is an independent identically distributed sequence or q[n] has a flat power spectral density (white).

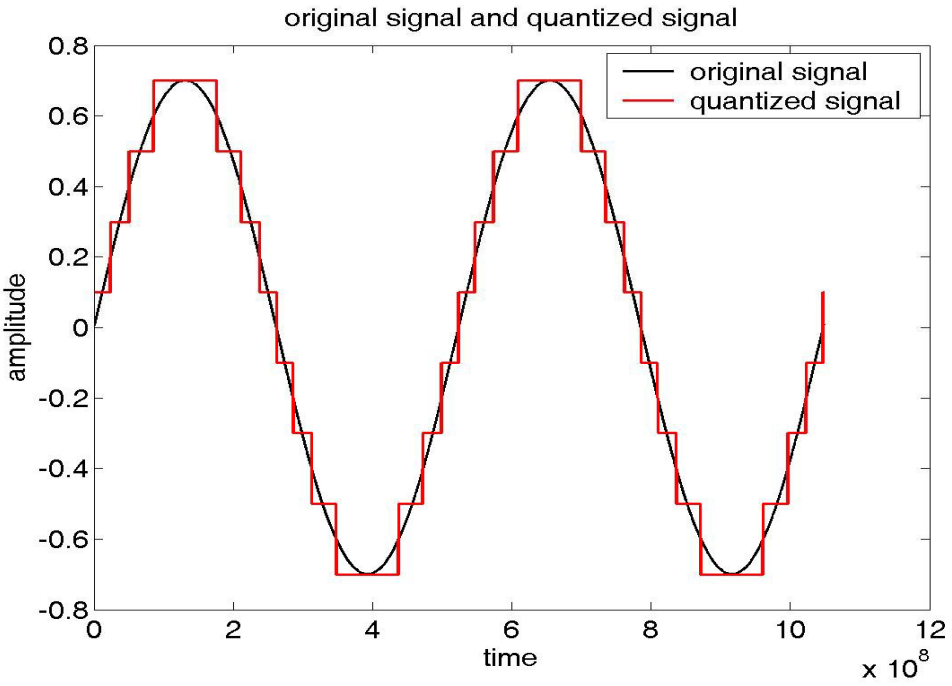


Fig 3. 4 Quantized signal

Since the quantization noise, q(n), is equal to y(n)-x(n), a quantizer can be modeled as shown in Figure 3.5 [6] . For a uniform quantizer, if the input signal does not overload, the quantization error will be bounded by ±Δ/2. If the Δ is very small, it is convenient and reasonable to assume the quantization noise is zero

mean and uniform distribution (Figure 3.6). The probability density function (pdf) of the quantization noise can be express as

$$f_Q(q) = \begin{cases} 1/\Delta, & -\Delta/2 \le q(n) \le \Delta/2 \\ 0, & \text{otherwise} \end{cases} \tag{3.6}$$

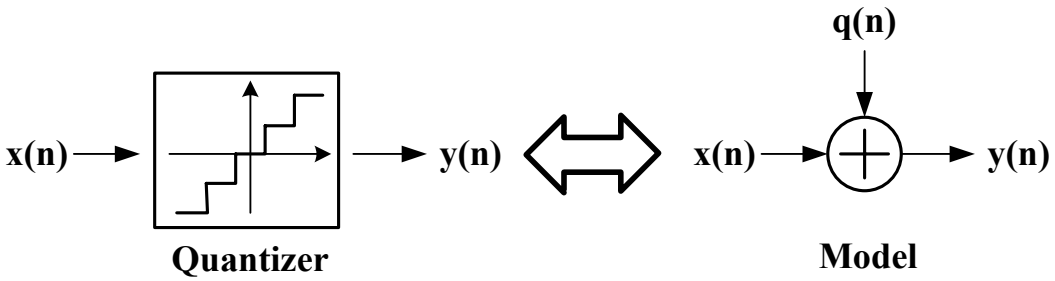


Fig 3. 5 Quantizer and its linear model

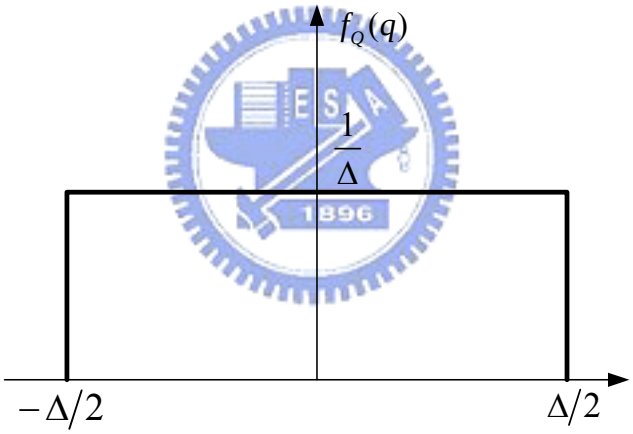


Fig 3. 6 The pdf of quantization noise

From Figure 3.6, the power of quantization noise can be shown as follows:

$$P_{Q,noise} = \frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} q^2 dq = \frac{\Delta^2}{12} \tag{3.7}$$

The power spectrum density of q(n), $S_Q(f)$, within the range of $\pm f_s$ calculated using the equation (3.8) is

$$P_{Q,noise} = \frac{\Delta^2}{12} = \int_{-f_s/2}^{f_s/2} S_Q(f)df \tag{3.8}$$

And we obtain the final result of $S_Q(f)$ as

$$S_Q(f) = \frac{\Delta}{12 f_s} \tag{3.9}$$

From equation (3.9) we show that power spectrum density is inversely proportional to sampling frequency shown in Figure 3.7. The larger the sampling frequency is, the less the noise amplitude is.

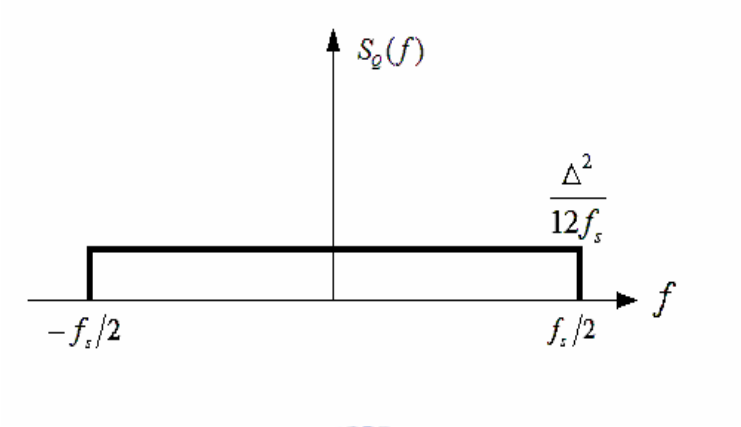


Fig 3. 7 Power spectrum density of q(n)

Assume the quantization signal is uniformly distributed over the range $\pm V_A$, and N is the bits per sample. The step size can be write as

$$\Delta = \frac{2V_A}{2^N} \tag{3.10}$$

According to the equations above, the SNR can be shown as

$$SNR = 10\log\frac{P_{signal}}{P_{Q,noise}} = 10\log(\frac{V_A^2/2}{\Delta^2/12}) = 6.02N + 1.76 \tag{3.11}$$

Equation (3.11) shows that increasing the number of bits per sample in the qunatizer increases the accuracy of the converter by 6dB for each extra bit.

3.5 Over-sampling Technique

Over-sampling is an important technique for sigma-delta ADCs. It can release the requirement of anti-aliasing filter. And it also can improve the resolution of a sigma-delta ADC. This improvement is achieved by over-sampling the signal. In other words, the sampling rate is much greater than Nyquist-rate. The definition of over-sampling ratio (OSR) is

$$OSR = \frac{2f_s}{f_b} \tag{3.12}$$

where f_s is the sampling frequency and f_b is the input signal bandwidth. Assuming the quantization noise is white noise. It means that noise power is uniformly distributed between $-f_s/2$ and $f_s/2$. It had shown that total amount of noise power injected into the quantized signals are the same whether they are over-sampling or Nyquist-rate conversions. But the distributions are different due to different sampling frequencies. Figure 3.8 shows the power spectrum density of quantization noise $S_Q(f)$ for conversion of Nyquist-rate (dotted line) sampling with sampling frequency, $f_{s,NR}$, and over-sampling (solid line) sampling with sampling frequency, $f_{s,OS}$, which is much greater than input signal bandwidth, f_b. The power spectrum density of input signal bandwidth for Nyquist rate is much greater than over-sampling.

The area of the both two rectangles meaning the total amount of noise power are the same and equal to $\Delta^2/12$. From Figure 3.8, it shows that the quantization noise power has spread to $f_{s,OS}/2$ and only a small fraction of quantization noise fall into the range of $-f_b$ and f_b. And the quantization noise outside the signal band will be attenuated by a digital low-pass filter as shown in Figure 3.9. Recollecting the quantization noise power

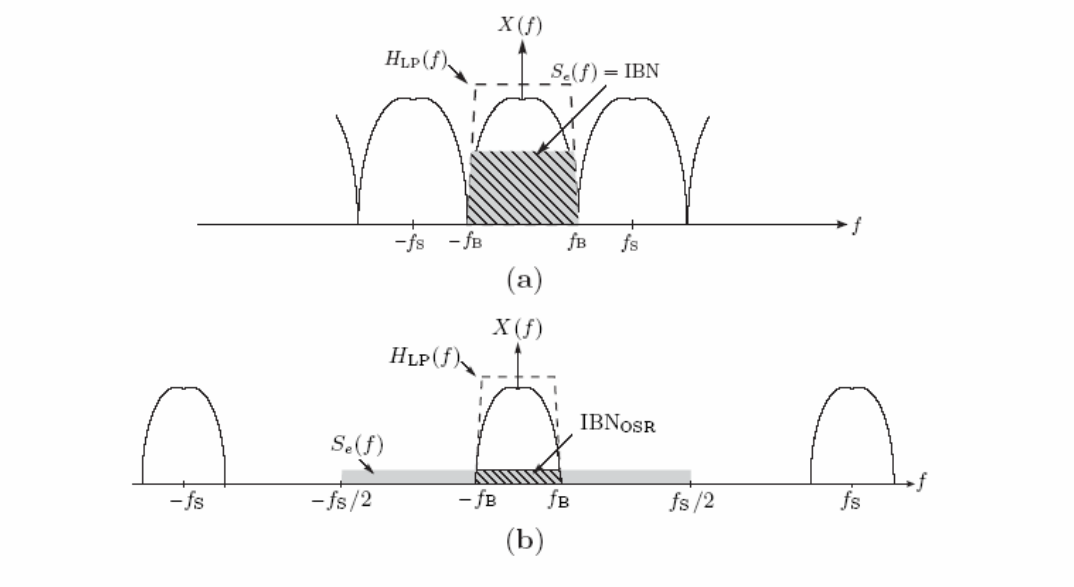
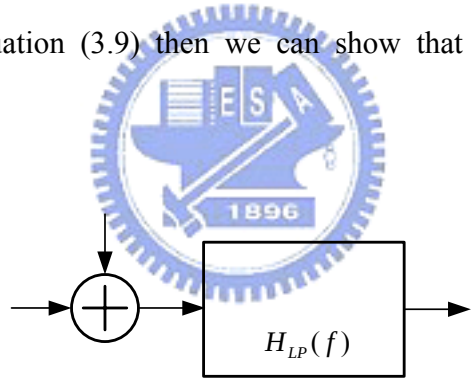
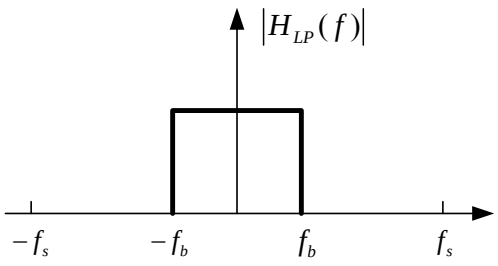


Fig 3. 8(a) Quantization noise power spectrum density for Nyquist-rate
(b) Over-sampling (solid line) conversion

spectrum density in equation (3.9) then we can show that the quantization noise is becoming



(a)



(b)

Fig 3. 9 (a) Over-sampling conversion with digital low-pass filter
(b)magnitude of frequency response of digital low-pass filter

$$P_{Q,noise} = \int_{-f_s}^{f_b} S_Q(f) \cdot |H_{LP}(f)|^2 df = \int_{-f_b}^{f_b} S_Q(f) df$$
$$= \frac{\Delta^2}{12 f_s} \cdot (2 f_b) = \frac{\Delta^2}{12} \cdot \frac{2 f_b}{f_s} \quad (3.13)$$

then we obtain

$$P_{Q,noise} = \frac{\Delta^2}{12} \cdot \frac{2 f_b}{f_s} = \frac{\Delta^2}{12} \cdot \frac{1}{OSR} \quad (3.14)$$

According equation (3.7), (3.10), (3.12) and (3.14), the SNR of over-sampling conversion is

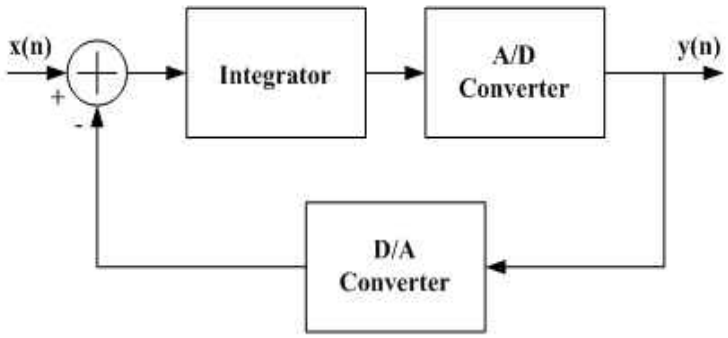
$$SNR = 10 \log\left(\frac{P_{signal}}{P_{Q,noise}}\right) = 10 \log\left(\frac{\frac{V_A^2}{2}}{\frac{\Delta^2}{12} \cdot \frac{1}{OSR}}\right) = 6.02N + 1.76 + 10 \log(OSR) \quad (3.15)$$

The first term of equation (3.15) denotes the contribution of N-bit quantizer and the last term is the enhancement of over-sampling technique. For every doubling the OSR, the SNR improve by 3dB corresponding to improve the resolution by 0.5 bit. Besides, since the resolution of N-bit quantizer is lower than overall resolution of system, it could reduce the complexity of analog circuit and power of overall system.

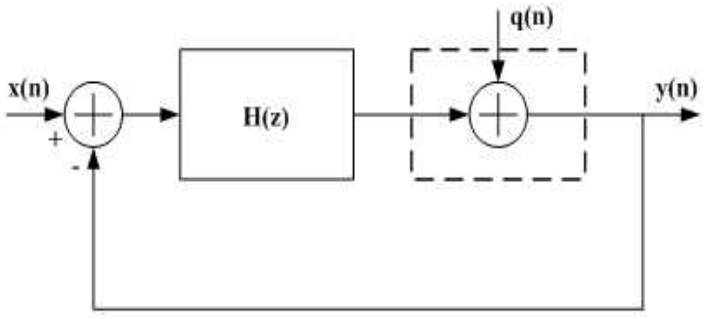
3.6 Noise Shaping

3.6.1 Architecture of noise shaping

A general noise-shaped sigma-delta modulator and its linear model have been shown in Figure 3.10.



(a)



(b)

Fig 3. 10 Block diagram of (a) a noise-shaped SDM and (b) its linear model

We can show that

$$y(n) = x(n-1) + q(n) - q(n-1) \tag{3.16}$$

After transforming equation (3.16) by *Z*-transform, we obtain

$$Y(z) = \frac{H(z)}{1+H(z)} X(z) + \frac{1}{1+H(z)} Q(z) \tag{3.17}$$

Then we can derive signal transfer function ($S_{TF}(z)$) by setting Q(z)=0

$$S_{TF}(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1+H(z)} \tag{3.18}$$

The same, we can derive noise transfer function ($N_{TF}(z)$) by setting X(z)=0

$$N_{TF}(z) = \frac{Y(z)}{Q(z)} = \frac{1}{1+H(z)} \tag{3.19}$$

The equation (3.17) will become

$$Y(z) = S_{TF}(z) \cdot X(z) + N_{TF}(z) \cdot Y(z) \tag{3.20}$$

The STF generally have all-pass or low-pass frequency response and the NTF have high-pass frequency response. In other words, the STF will be approximately unity over the signal band and the NTF will be approximately zero over the same frequency band. The quantization noise will be removed to high frequency band when using noise-shaping strategy [7]. The quantization noise over the frequency band of interest will be reduced and do not affect the input signal. This would improve the SNR significantly for overall system.

3.6.2 First-Order ΔΣ Modulator

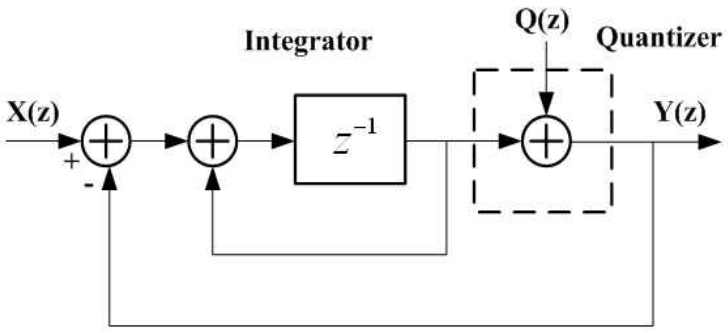


Fig 3. 11 The First-Order SDM

In Figure 3.11, it is a simple block diagram of the first-order SDM [8]. It includes an integrator and 1-bit quantizer. The noise-transfer function, $N_{TF}(z)$, should have a zero at DC. And zeros of $N_{TF}(z)$ are equal to poles of the $H(z)$ (ie., has a pole at z=1).

Therefore, the quantization noise will be high-pass filtered. In other words, the $H(z)$ will be small and the $N_{TF}(z)$ will large over the frequency band of interest. Thus, the discrete time integrator with a pole at DC can be expressed as

$$H(z)=\frac{1}{z-1}=\frac{z^{-1}}{1-z^{-1}} \tag{3.21}$$

According to equation (3.18) and (3.19) we obtain

$$S_{TF}(z)=\frac{H(z)}{1+H(z)}=\frac{z^{-1}/1-z^{-1}}{1+z^{-1}/1-z^{-1}}=z^{-1} \tag{3.22}$$

$$N_{TF}(z)=\frac{1}{1+H(z)}=\frac{1}{1+z^{-1}/1-z^{-1}}=1-z^{-1} \tag{3.23}$$

The total transfer function of system is

$$Y(z)=X(z)\cdot z^{-1}+Q(z)\cdot(1-z^{-1}) \tag{3.24}$$

From equation (3.24) we know the STF is just a delay and NTF is a high-pass filter. In another word, the output signal comprises the delayed input signal and high-pass filtered quantization noise. Now, we may consider the amplitude of the noise transfer function, $\left|N_{TF}(z)\right|$. Let $z=e^{j\omega T}=e^{j2\pi f/f_s}$, equation (3.23) will becomes

$$N_{TF}(z)=1-z^{-1}=1-e^{-j\omega T}=1-e^{-j2\pi f/f_s}$$

$$=\frac{e^{j\pi f/f_s}-e^{-j\pi f/f_s}}{2j}\cdot 2j\cdot e^{-j\pi f/f_s}$$

$$=\sin\left(\frac{\pi f}{f_s}\right)\cdot 2j\cdot e^{-j\pi f/f_s}$$

Then we obtain

$$\left|N_{TF}(f)\right|=2\sin\left(\frac{\pi f}{f_s}\right) \tag{3.25}$$

The quantization noise power over the signal band is shown as follows:

$$P_{Q,noise} = \int_{-f_b}^{f_b} S_Q(f) \cdot \left|N_{TF}(z)\right|^2 df = \int_{-f_b}^{f_b} \frac{\Delta^2}{12} \frac{1}{f_s} \left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^2 df \qquad (3.26)$$

Because $OSR \gg 1$ for over-sampling conversion, f_s would be much larger than f_b. Thus, $\sin(\pi f / f_s)$ can be approximated to $\pi f / f_s$. Equation (2.26) will become

$$P_{Q,noise} = \frac{\Delta^2}{12 f_s} \int_{-f_b}^{f_b} \left[2\left(\frac{\pi f}{f_s}\right)\right]^2 = \frac{\Delta^2}{12} \cdot \frac{\pi^2}{3} \cdot \left(\frac{2 f_b}{f_s}\right)^3 = \frac{\Delta^2 \pi^2}{36} \left(\frac{1}{OSR}\right)^3 \qquad (3.27)$$

Using the equation (3.10) and (3.27), we obtain the SNR of first-order SDM

$$\begin{aligned} SNR &= 10\log\left(\frac{P_{signal}}{P_{Q,noise}}\right) = 10\log\left(\frac{\frac{V_A^2}{2}}{\frac{\Delta^2\pi^2}{36}\left(\frac{1}{OSR}\right)^3}\right) = 10\log\left(\frac{\frac{\Delta^2 2^{2N}}{8}}{\frac{\Delta^2\pi^2}{36}\left(\frac{1}{OSR}\right)^3}\right) \\ &= 6.02b + 1.76 - 5.17 + 30\log(OSR) \text{ dB} \end{aligned} \qquad (3.28)$$

For every doubling the OSR, the SNR will improve by **9dB** (ie., resolution will increase 1.5 bits). This result can be compared with equation (3.15), the SNR only can improve by 3dB when over-sampling conversion do not use noise-shaping strategy. It will be **much efficiency** when using noise-shaping technique.

3.6.3 Second-Order ΔΣ Modulator

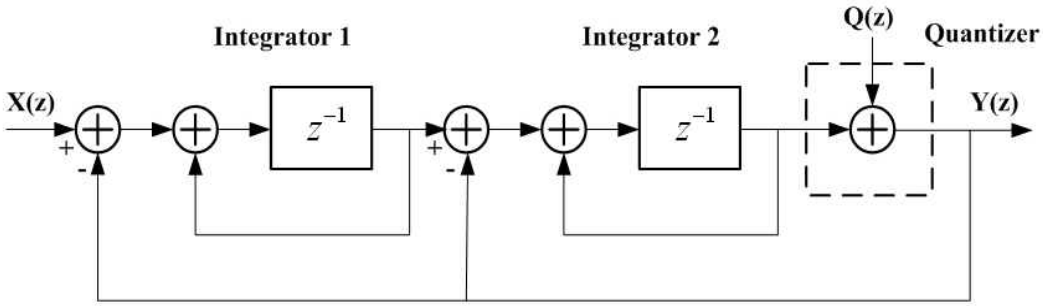


Fig 3. 12 The Second-Order SDM

In Figure 3.12, it is a block diagram of a second-order SDM. It is popular and widely used in SDM designing. It includes two integrators and a 1-bit quantizer. Its fundamental theorem is the same as the first-order SDM. Thus, the transfer function can be expressed as

$$Y(z) = X(z) \cdot z^{-2} + Q(z) \cdot (1 - z^{-1})^2 \tag{3.29}$$

And we can show the $S_{TF}(z)$ and $N_{TF}(z)$

$$S_{TF}(z) = z^{-2} \tag{3.30}$$

$$N_{TF}(z) = (1 - z^{-1})^2 \tag{3.31}$$

Thus we obtain the magnitude of N_{TF}

$$\left|N_{TF}(f)\right| = \left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^2 \tag{3.32}$$

The quantization noise power over the signal band is shown as following

$$P_{Q,noise} = \int_{-f_b}^{f_b} S_Q(f) \cdot \left|N_{TF}(z)\right|^2 df = \int_{-f_b}^{f_b} \frac{\Delta^2}{12} \frac{1}{f_s} \left[2\sin\left(\frac{\pi f}{f_s} \right) \right]^2 df$$

$$\approx \frac{\Delta^2}{12 f_s} \int_{-f_b}^{f_b} \left[2\left(\frac{\pi f}{f_s} \right) \right]^4 = \frac{\Delta^2}{12} \cdot \frac{\pi^4}{5} \cdot \left(\frac{2 f_b}{f_s} \right)^5 = \frac{\Delta^2 \pi^4}{60} \left(\frac{1}{OSR} \right)^5 \tag{3.33}$$

With the same method, we can obtain the SNR of the second-order SDM as

$$SNR = 10\log\left(\frac{P_{signal}}{P_{Q,noise}} \right) = 10\log\left(\frac{\frac{V_A^2}{2}}{\frac{\Delta^2 \pi^4}{60}\left(\frac{1}{OSR} \right)^5} \right) = 10\log\left(\frac{\frac{\Delta^2 2^{2N}}{8}}{\frac{\Delta^2 \pi^4}{60}\left(\frac{1}{OSR} \right)^5} \right)$$

$$= 6.02b + 1.76 - 12.9 + 50\log(OSR) \ \text{dB} \tag{3.34}$$

For every doubling the OSR, the SNR will improve by **15dB** (ie., resolution will increase 2.5 bits). This result can be compared with equation (3.15) and (3.28), the second-order SDM can provide more suppression over the same band, and thus more noise power outside the signal band. Figure 3.13 shows the phenomenon of using noise-shaping technique or not. For a fixed signal band, the case of no noise-shaping has the largest quantization power over the signal band. The second and the third are

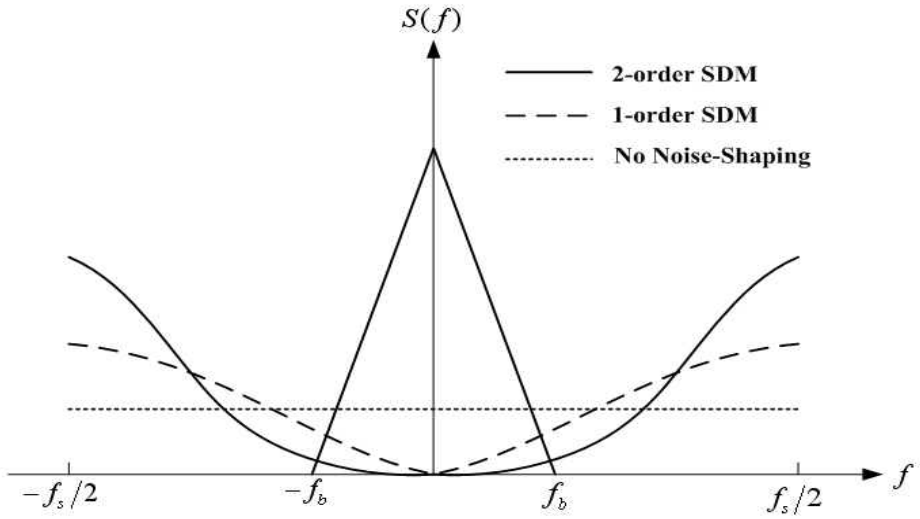


Fig 3. 13 Power spectrum density of 1st order, 2nd order noise-shaping and non noise-shaping strategy

the first-order SDM and the second-order SDM respectively. As the number of order increasing, the quantization noise power will decrease over the same signal band. The simulation result can show as Figure 3.14.

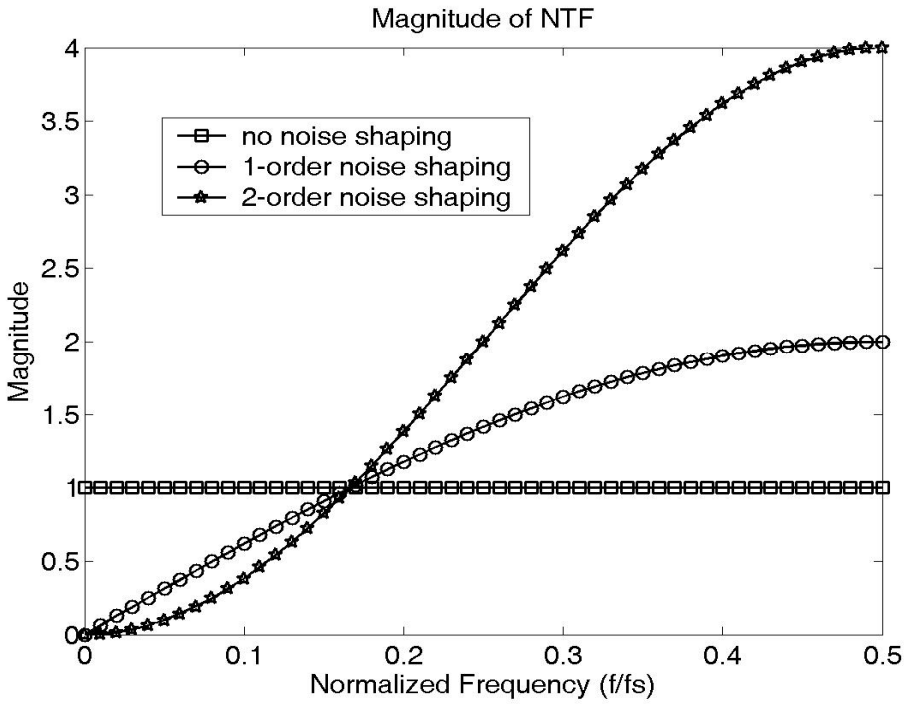


Fig 3. 14 Magnitude of NTF

3.6.4 Higher-Order ΔΣ Modulator

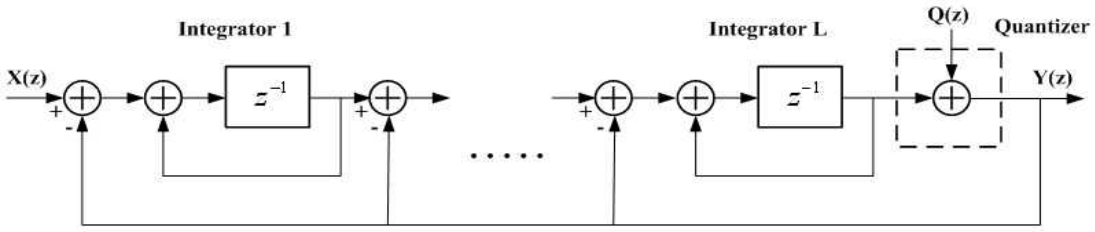


Fig 3. 15 The Higher-Order SDM

Higher-order SDM is divided into single-stage and multi-stage structures [9]. Figure 3.15 is the system block diagram of single-stage Lth-order SDM. Here, we will discuss the change of quantization noise and SNR when the number of order increases.

With the same approach, we obtain the noise-transfer function, N_{TF} ,of the Lth-order SDM as follows:

$$N_{TF} = (1 - z)^{L} \tag{3.35}$$

In a similar manner, the quantization-noise power over the signal band of the single-stage Lth-order SDM with N-bits quantizer is

$$P_{Q,noise} = \int_{-f_b}^{f_b} S_Q(f) \cdot |N_{TF}(z)|^2 \, df = \int_{-f_b}^{f_b} \frac{\Delta^2}{12} \frac{1}{f_s} \left[2\sin\left(\frac{\pi f}{f_s} \right) \right]^{2L} df$$

$$\approx \frac{\Delta^2}{12 f_s} \int_{-f_b}^{f_b} \left[2\left(\frac{\pi f}{f_s} \right) \right]^{2L} = \frac{\Delta^2}{12} \cdot \frac{\pi^L}{2L+1} \cdot \left(\frac{2 f_b}{f_s} \right)^{2L+1} \tag{3.36}$$

$$= \frac{\Delta^2 \pi^{2L}}{12(2L+1)} \left(\frac{1}{OSR} \right)^{2L+1}$$

Then the SNR of the single-stage Lth-order SDM is

$$SNR = 10\log\left(\frac{P_{signal}}{P_{Q,noise}}\right) = 10\log\left(\frac{\frac{V_A^2}{2}}{\frac{\Delta^2\pi^{2L}}{12(2L+1)}\left(\frac{1}{OSR}\right)^{2L+1}}\right)$$

$$= 10\log\left(\frac{\frac{\Delta^2 2^{2N}}{8}}{\frac{\Delta^2\pi^{2L}}{12(2L+1)}\left(\frac{1}{OSR}\right)^{2L+1}}\right)$$

Finally, we get the result

$$SNR = 6.02b + 1.76 + 10\log\left(\frac{\pi^{2L}}{2L+1}\right) + (20L+10)\log(OSR) \text{ dB} \qquad (3.37)$$

From equation (3.37), we know that for every doubling the OSR, the SNR will improve by (6L+3) dB (ie., resolution will increase L+0.5 bits). There are three ways to increase the SNR of a SDM. First, we can increase the bits of quantizer. The disadvantage is that multi-bit quantizer would induce harmonic distortion because of mismatch. Second, we can increase the number of order of a SDM. But it may have stability problem when the order is greater than 2. Third, increasing the OSR is the most popular way to improve the performance But for low power design, increasing

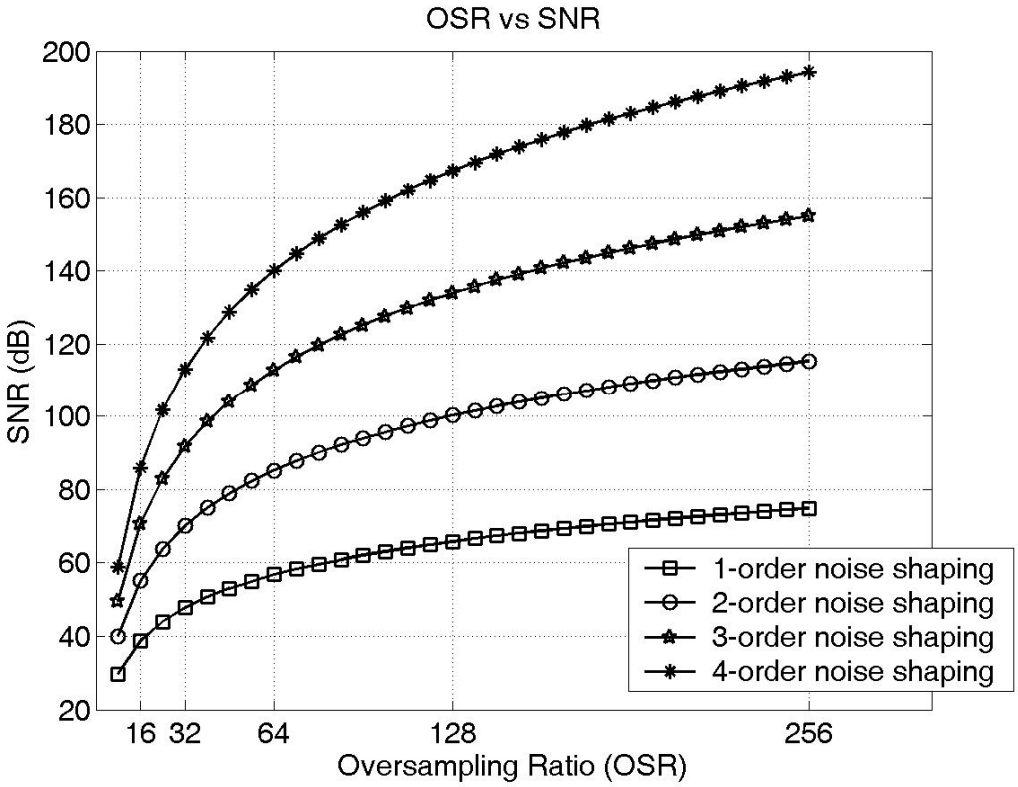


Fig 3. 16 Plot of SNR versus SDM

the OSR is not suitable because the requirement of the integrators, such as settling time, bandwidth, and slew rate will be increased. Beside, the power of decimation filter will also be increased because of high sampling frequency. Figure 3.16 is the SNR of SDM. This plot provides a tradeoff between order, OSR and the power dissipation.

3.6.5 System Analysis of ΔΣ Analog-to-Digital Converters

The system architecture for a typical over-sampling ADC is shown in Figure 3.17. The anti-aliasing filter is used to filter the out-of-band noise of original input signal to avoid noise folding into signal band. Then, the signal is sampled and held and applied to a SDM and output a 1-bit digital signal. Usually, the sample-and-hold usually combines with the SDM. These three blocks are belonging to analog domain. A decimation filter which contains a digital low-pass filter and a down-sampling not only suppresses the

out-of-band quantization noise but also down-sample the sampling frequency from f_s to Nyquist-rate [10]. Note that the digital low-pass filter here is like an anti-aliasing filter to limit signals to one-half the output sampling rate. The decimation filters generally are implemented using digital circuit technique in order to reduce the power dissipation and are easy to implement. Figure 3.18 shows the signal and spectra of each stage of over-sampling ADC [11].

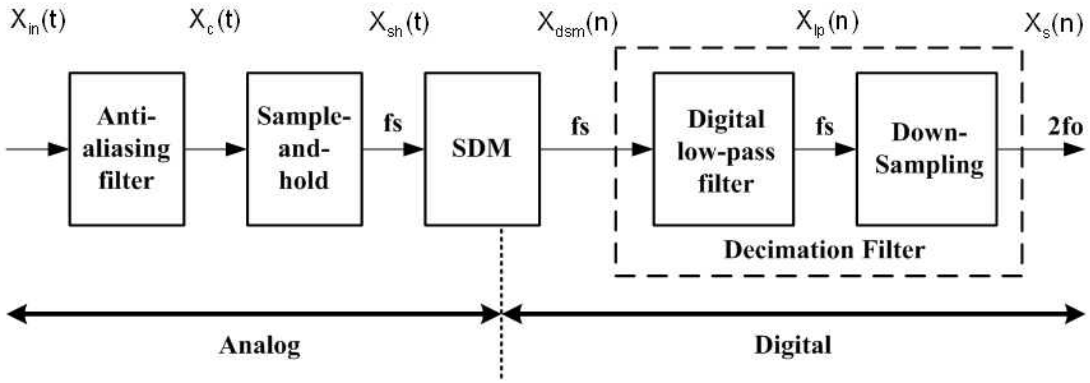


Fig 3. 17 Block diagram of an over-sampling A/D converter

3.7 Conclusion

In this chapter, we have introduced the basic principles of sigma-delta modulator. Among these, the most important is the properties of shaped quantization error. Here, various architectures of SDM such as single-loop and cascaded was introduced and compared. And then, the advantages and disadvantages of multi-bit quantizer was described and analyzed. In the final part of this chapter, we discuss how the signal and spectra change in different section of the over-sampling ADC and DAC. This would make us much clear about the operation of over-sampling system.

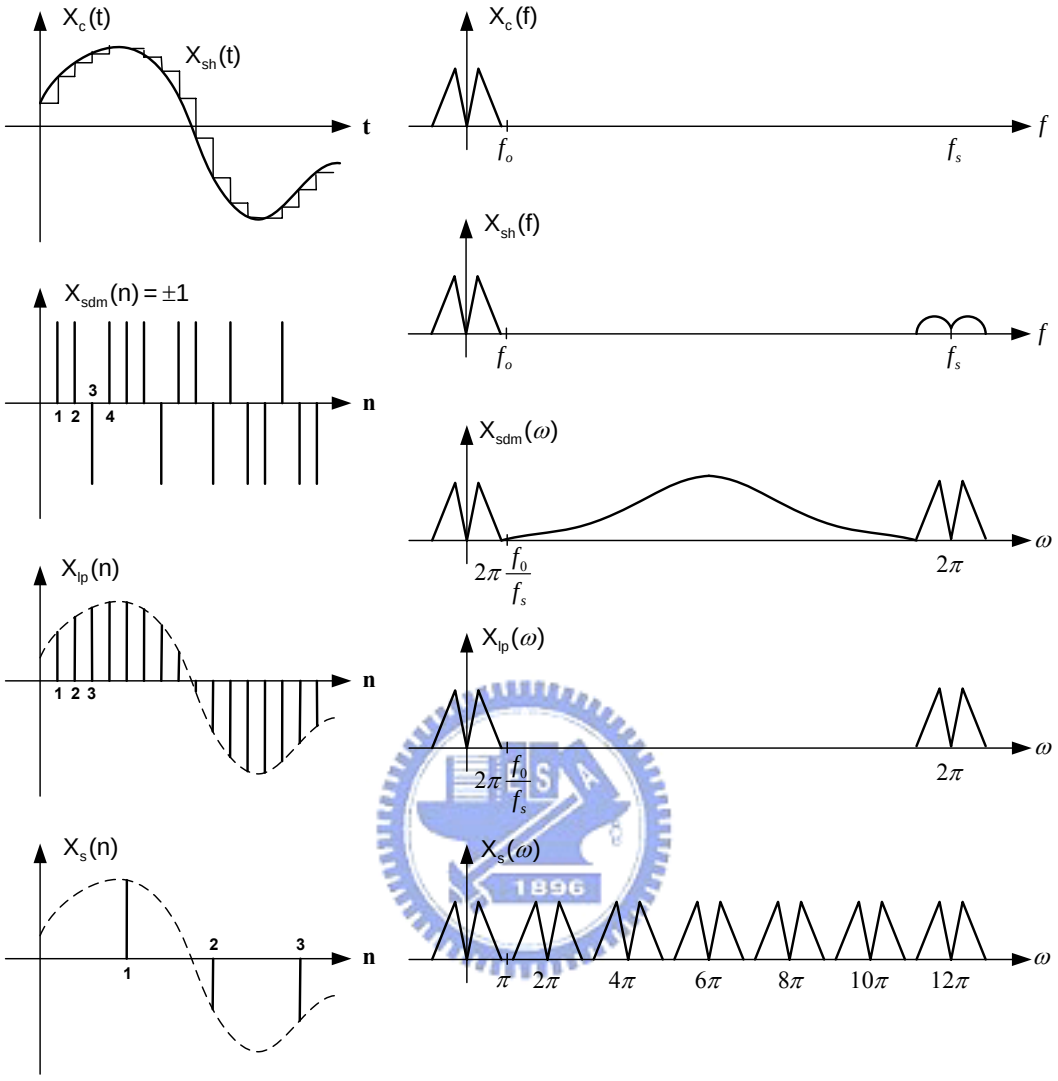


Fig 3. 18 Signal and spectra in an over-sampling ADC

CH4 Transformation of a Discrete-Time to Continuous-Time

4.1 Introduction

Early designs of continuous-time ΣΔ modulators were approximate, guided by the intuition that the general continuous-time integrators ω_0 should work for low-pass modulators and correspondingly the continuous-time resonators $\omega_O S/(S^2+\omega_O)$ for band-pass modulators. However, this simple assumption leads to implementation of an incorrect loop transfer function for a ΣΔ modulator. In this chapter it is shown that a continuous-time ΣΔ loop filter has to be designed according to the digital to analog converter (DAC) output waveform in the feedback path of the modulator. A simple explanation is that the continuous-time filter respond to an input signal continuously, unlike the SC filter in which an analog charge is supplied to the filter at a clock phase ϕ and the output analog voltage is ready at a clock phase $\overline{\phi}$. So a SC filter doesn't see the variations of the input signal during the clock period ϕ and $\overline{\phi}$. On the other hand, form the linear system theory the output of a continuous-time filter is the result of convolution of the filter response with the input signal in the time interval $t \in [-\infty, \infty]$.

4.2 The Impulse-Invariant Transform

A clock diagram of a continuous-time ΣΔ modulator is shown in Fig.4.1. Because of the presence of a sampler inside the loop (the quantizer is clocked, making for implicit sampling) the overall loop transfer function in a continuous-time modulator is really a discrete-time transfer function! In other words as shown in Fig. 4.2 the loop transfer function from the output of quantizer back to its input has an exact equivalent *z*-domain transfer function *H*(*z*). This doesn't mean that the waveforms inside the loop are sampled-data like the ones in a switched-*C* (discrete-time) modulator.

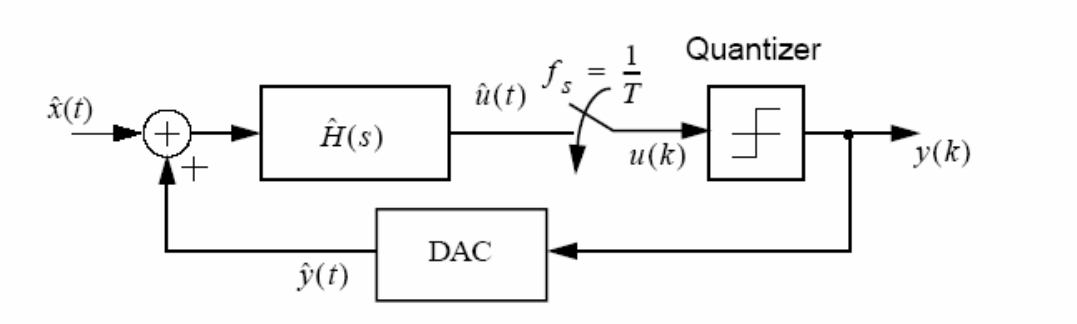


Fig 4. 1 continuous-time ΔΣ modulator

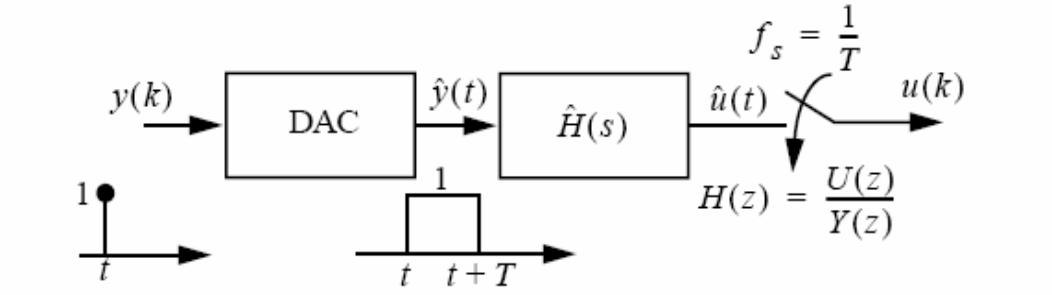


Fig 4. 2 ΔΣ open loop block diagram

However, the sample values of the continuous-time waveform at the input of the quantizer at the sample times define an exact discrete-time impulse response for the continuous-time loop. In order to clarify this statement a examples of a second-order low-pass ΣΔ modulators with loop transfer functions of $z^{-1}(2-z^{-1})/(1-z^{-1})^2$ is given here briefly. The loop impulse responses of these discrete-time systems and their corresponding continuous-time counterparts are shown in Fig. 4.3.

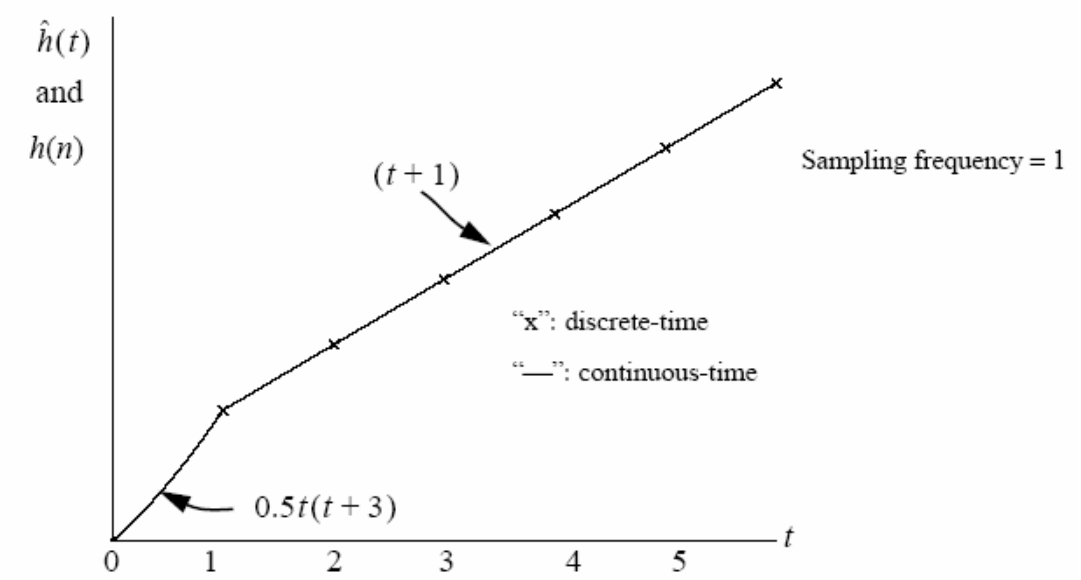


Fig 4. 3 Open-loop impulse response of the second-order low-pass modulator

As shown in these figures the open-loop impulse responses of the discrete-time loop filters match the samples of the impulse response of the continuous-time modulator loops. The continuous-time waveforms shown in Fig. 4.3 is actually the pulse responses of the continuous-time ΔΣ loop filter as depicted in Fig. 4.2. Detailed analysis of these examples is given in next Sec. 4.3.

The loop behavior is completely determined by what the sampler inside the loop sees at its sample times, and that can be written as a difference equation. So, if a designer wants to analyze the performance of a continuous-time ΔΣ modulator (*SNR* and stability), he/she should first derive the equivalent *z*-domain transfer function for the ΔΣ loop. Then further analysis can be done in the *z*-domain as for traditional discrete-time modulators. Therefore the noise-shaping behavior of "continuous-time" ΔΣ loops can be designed entirely in the "discrete-time" domain and the exact same noise-shaping behavior obtained for either continuous-time or discrete-time systems.

4.3 NRZ Transformation

The ΔΣ modulator of Fig. 4.1 is shown again in Fig.4.4 in more detail. The loop filter is represented by $\hat{H}(s)$ and the DAC transfer function by a zero-order-hold (*ZOH*) in

which p is the opening aperture. The non-return-to-zero(NRZ) DAC $p=T$ where T is a sampling period. Fig. 4.2 shows the ΔΣ signal path from the output of quantizer back to its input for a NRZ DAC.

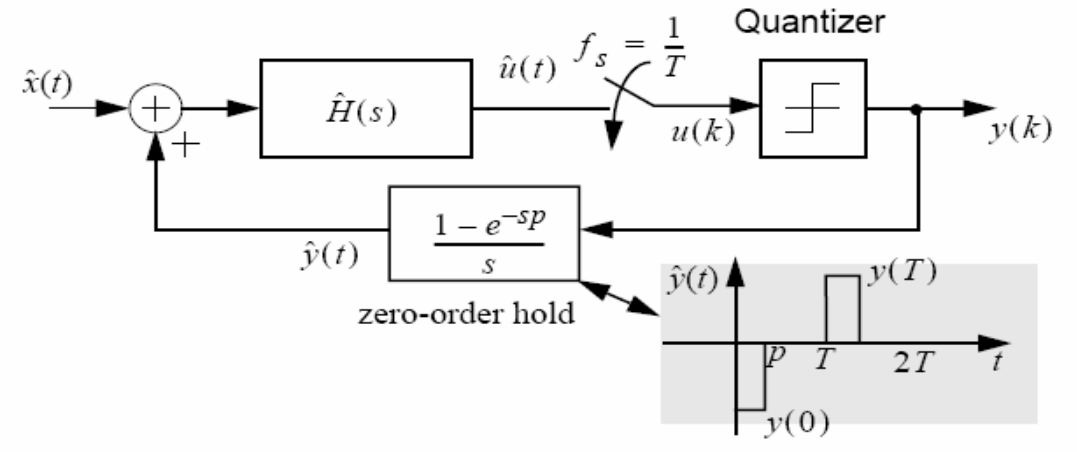


Fig 4. 4 A continuous-time ΔΣ modulator in S-domain

As can be seen from Fig. 4.2 the overall ΔΣ loop gain is a discrete-time function, so one can derive the exact discrete-time transfer function, $H(z)$, of the loop given the transfer functions of the continuous-time loop filter, $\hat{H}(s)$, and the *ZOH* as follows:

$$Z^{-1}\left[H(z)\right] = L^{-1}\left[\frac{1-e^{-sp}}{s}\hat{H}(s)\right]_{t=nT} \tag{4.1}$$

Equation (4.1) can be expressed in the time domain by

$$h(nT) = \left[R_p(t) * \hat{h}(t)\right]\Big|_{t=nT} = \left(\int_{-\infty}^{\infty} R_p(\tau)\hat{h}(t-\tau)d\tau\right)\Big|_{t=nT} \tag{4.2}$$

where $R_p(t)$, the impulse response of *ZOH*, is a pulse with width of p as shown in Fig. 4.4, $\hat{h}(t)$ is the impulse response of the continuous-time loop filter, $h(n)$ is the overall discrete-time impulse response of the loop, and $*$ denotes time convolution. Since $R_p(t)$

has a pulse waveform, (4.1) and (4.2) are known as the pulse invariant transformation.

Consider the case where $p=T$ corresponding to NRZ feedback pulse. Then the loop filter NRZ pulse response from (4.2) can be described as following:

$$h(t) = R_{NZ}(t) * \hat{h}(t) = \int_{-\infty}^{\infty} R_{NZ}(\tau)\hat{h}(t-\tau)d\tau = \begin{cases} \int_0^t \hat{h}(t-\tau)d\tau & 0 \le t < T \\ \int_0^T \hat{h}(t-\tau)d\tau & t \ge T \\ 0 & t < 0 \end{cases} \tag{4.3}$$

For a continuous-time loop filter with single-poles described in residue form by

$$\hat{H}(s) = \sum_{k=1}^{N} \frac{\hat{a}_k}{s - s_k} \tag{4.4}$$

the impulse response would be

$$\hat{h}(t) = \sum_{k=1}^{N} \hat{a}_k e^{s_k t} u(t) \tag{4.5}$$

Substituting $\hat{h}(t)$ into (4.3), we have

$$h(t) = \begin{cases} \int_0^t \left(\sum_{k=1}^{N} \hat{a}_k e^{s_k(t-\tau)} \right) d\tau = \sum_{k=1}^{N} \hat{a}_k e^{s_k t} \left[\int_0^t e^{-s_k \tau} d\tau \right] = \sum_{k=1}^{N} \frac{\hat{a}_k}{-s_k} e^{s_k t}(e^{-s_k t} - 1) & 0 \le t < T \\ \int_0^T \left(\sum_{k=1}^{N} \hat{a}_k e^{s_k(t-\tau)} \right) d\tau = \sum_{k=1}^{N} \hat{a}_k e^{s_k t} \left[\int_0^T e^{-s_k \tau} d\tau \right] = \sum_{k=1}^{N} \frac{\hat{a}_k}{-s_k} e^{s_k t}(e^{-s_k T} - 1) & t \ge T \end{cases} \tag{4.6}$$

Looking at samples of loop impulse response, $h(t)$, at sampling times *i.e.* $t=nT$ gives the discrete-time loop impulse response equivalent

$$h(nT) = \begin{cases} 0 & 0 \le t < T \\ \sum_{k=1}^{N} \frac{\hat{a}_k}{-s_k} e^{s_k nT}(e^{-s_k T} - 1) & t \ge T \end{cases} \tag{4.7}$$

The z-domain loop transfer function of the loop then can be derived from (4.7)

$$\begin{aligned} H(z) &= \sum_{n=-\infty}^{+\infty} h(n) z^{-n} = \sum_{n=1}^{\infty} \left(\sum_{k=1}^{N} \frac{\hat{a}_k}{-s_k} e^{s_k nT}(e^{-s_k T} - 1) \right) z^{-n} \\ &= \sum_{k=1}^{N} \left[\frac{\hat{a}_k}{-s_k}(e^{-s_k T} - 1) \sum_{n=1}^{\infty} e^{s_k nT} z^{-n} \right] \\ &= \sum_{k=1}^{N} \frac{\hat{a}_k}{-s_k} \cdot \frac{(1 - e^{s_k T}) z^{-1}}{1 - e^{s_k T} z^{-1}} \end{aligned} \tag{4.8}$$

There are some interesting properties in the pulse invariant transformation given in (4.6)-(4.8) which have to be addressed:

1) The first sample of the loop filter pulse response is zero (4.7). This is described by a delay factor which always exists in the numerator of the pulse invariant transformation function (4.8). This delay is related to the causality property associated with convolution of two ordinary signals which don't contain any impulse function $\delta(t)$ component. That's why, as will be seen in the transformation of any discrete-time $\Delta\Sigma$ loop filter to a continuous-time equivalent, one delay is always absorbed in pulse transformation.

2) The overall continuous-time loop response (4.6) is described by different functions in the regions of $0 \le t < T$ and $t \ge T$, where T is the sampling period. This has already been shown in Fig. 4.3 for second-order low-pass modulators. It should be noted that,

however, the overall loop response has continuity at *T*. The equivalent discrete-time loop filter (4.8) can be written as

$$H(z) = \sum_{k=1}^{N} \frac{a_k Z^{-1}}{1 - Z_k Z^{-1}} \tag{4.9}$$

where the new residue is

$$a_k = \frac{\hat{a}_k}{-s_k}(1 - e^{s_k T}) \cos^{-1} \theta \tag{4.10}$$

and the new pole is at $Z_k = e^{s_k T}$

Note that (4.9) is the NRZ pulse transformation of (4.4) rewritten here

$$\hat{H}(s) = \sum_{k=1}^{N} \frac{\hat{a}_k}{S - S_k} \tag{4.11}$$

This has the properties one would expect: a pole at $s = 0$ transforms to one at $z = 1$, and a pole at $s = j2\pi(f_s / 4)$ transforms to one at $z = j$.

To actually do the transform, we proceed as follows. First, we write $H(z)$ as a partial fraction expansion. Then we choose a DAC pulse shape. We can assume a perfectly rectangular DAC pulse of magnitude 1 that from α to β. It can be shown as equation (4.11) and Figure 4.5. This covers most types of practical DAC pulse. Finally,

$$\hat{r}(\alpha, \beta) = \begin{cases} 1, & \alpha \le t < \beta, \ 0 \le \alpha < \beta \le 1 \\ 0, & \text{otherwise.} \end{cases} \tag{4.11}$$

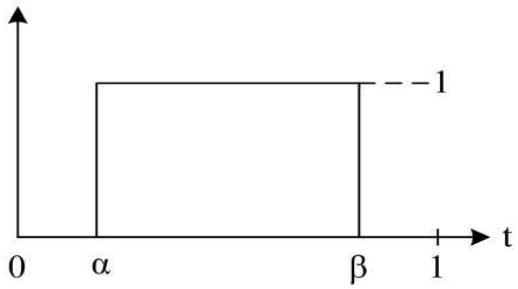


Fig 4. 5 The DAC pulse

We use Table 4.1 to convert each partial fraction pole from *z* to *s*. Then we will obtain the result of $\hat{H}(s)$. For example, if we use the DAC type, (α, β)=(0,1) in (4.11). And the transfer function is

$$H(z)=\frac{-2z+1}{(z-1)^2} \tag{4.12}$$

Table 4.1 s-domain equivalences for z-domain loop filter poles [12]

z-domain pole	Limit for $z_k=1$
$\frac{y_0}{z-z_k}$	$\frac{r_0}{s-s_k}$, $r_0=\frac{y_0}{\beta-\alpha}$
$\frac{y_0}{(z-z_k)^2}$	$\frac{r_1 s+r_0}{(s-s_k)^2}$, $r_0=\frac{y_0}{\beta-\alpha}$ $r_1=\frac{1}{2}\frac{(\alpha+\beta-2)y_0}{\beta-\alpha}$
$\frac{y_0}{(z-z_k)^3}$	$\frac{r_2 s^2+r_1 s+r_0}{(s-s_k)^3}$, $r_0=\frac{y_0}{\beta-\alpha}$ $r_1=\frac{1}{2}\frac{(\alpha+\beta-2)y_0}{\beta-\alpha}$ $r_2=\frac{1}{12}\frac{y_0}{\beta-\alpha}\left[\beta(\beta-9)+\alpha(\alpha-9)+4\alpha\beta+12\right]$

Then we write this in partial fractions yields

$$H(z) = \frac{-2}{z-1} + \frac{-1}{(z-1)^2} \tag{4.13}$$

Applying the first row of Table 4.1, we obtain

$$\hat{H}(s) = \frac{-2}{s} + \frac{-1+0.5s}{s^2} = -\frac{-1+1.5s}{s^2} \tag{4.14}$$

Then we had transformed the $H(z)$ to $\hat{H}(s)$ and obtain the new coefficients for continuous-time SDM.

4.3.1 Effect of Excess Loop Delay

Continuous-time SDM suffers a problem not seen in discrete-time design. That is the excess loop delay [13]. Excess loop delay arises because of **nonzero delay** between the quantizer clock edge and the time when a change in output bit is seen at the feedback point in the modulator. It arises because the nonzero switching time of the transistors in the feedback path. Its effect is severe if the sampling clock speed is an appreciable fraction of the maximum transistor switching speed.

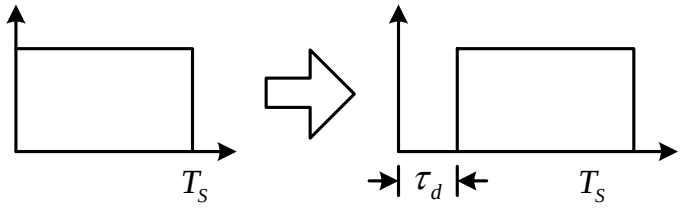


Fig 4. 6 Illustrations of excess loop delay on NRZ DAC pulse

We assume that excess loop delay can be expressed as a fraction of the sampling period

$$\tau_d = \rho_d T_S \tag{4.15}$$

In an actual circuit, the value of τ_d depends on the switching speed of the transistors

f_T, the quantizer clock frequency f_S, and the number of transistors in the feedback path n_t (as well as other things like the loading on each transistor). As a crude approximation, we could assume transistors switch fully at the maximum speed, i.e. after time 1/ f_T, in which case we could write

$$\rho_d = \frac{n_t f_S}{f_T} \tag{4.16}$$

τ_d could end up being a significant fraction of T_S depending on the parameters in (4.16). This is particularly likely in GHz-speed modulators built in a process with an f_T of a few tens of GHz. For example , a OSR of about 50 and 5MHz bandwidth Sigma-delta modulator ,which means we must clock at f_S =50(2*5)=500MHz. comparator output differential pair must switch. The DAC must also switch, and thus n_t=2. In a f_T =10GHz process, therefore, $\rho_d = \frac{2 \cdot 0.5}{10} = 10\%$ is the amount of excess delay predicted by (4.16).

We recall DAC pulses as rectangular with the form

$$\hat{r}(\alpha,\beta) = \begin{cases} 1, & \alpha \le t < \beta, \ 0 \le \alpha < \beta \le 1 \\ 0, & \text{otherwise.} \end{cases} \quad \text{in (4.11)}$$

Suppose we have assumed that we have an NRZ DAC with (α, β) = (0,1), and we have found the equivalent $\hat{H}(s)$ for a desired H(z) using Table 4.1 or MATLAB. If we use this filter in a system with delayed pulses as in Fig 4.6, then the system no longer has the same α and β. This means the equivalence between $\hat{H}(s)$ and H(z) is affected.

Then we are going to understand the effect of excess loop delay of DAC. Suppose we are designing a CT double integration modulator, and we have NRZ DAC pulse, then we would have found $\hat{H}(s)$ to be $\hat{H}(s) = -\frac{1+1.5s}{s^2}$.suppose further that we have excess loop delay τ_d, so that in actuality we have NR DAC pulse delayed by τ_d as in figure

4.6. In that case, we have (α, β) = (τ_d , τ_d +1). What is the equivalent H(z) for such an $\hat{H}(s)$ and DAC pulse?

The formulae in Table 4.1 only apply for a pulse with $\beta \leq$ 1, but once again, superposition comes to our rescue: it is possible to write a τ_d -delayed NRZ pulse as

$$\hat{\Upsilon}_{(\tau_d,1+\tau_d)}(t)=\hat{\Upsilon}_{(\tau_d,1)}+\hat{\Upsilon}_{(0,\tau d)}(t-1) \tag{4.17}$$

That is the linear combination of a DAC pulse from τ_d to 1 and a one-sample -delayed DAC pulse form 0 to τ_d as shown in figure 4.7.

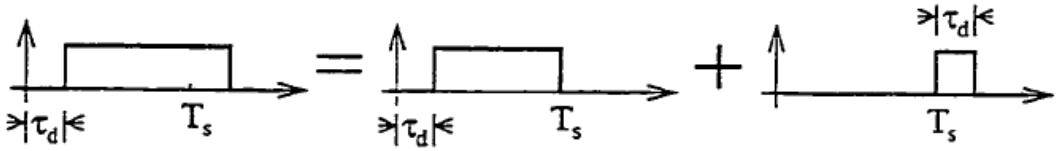


Fig 4. 7 The delayed NRZ pulse as a linear combination

Writing $\hat{H}(s)$ in partial fractions gives

$$\hat{H}(s)=\frac{-1.5}{s}+\frac{-1}{s^2} \tag{4.18}$$

Applying Table 4.1 to each term of (4.18), for each of the two DAC pulses in (4.17), yields

$$\frac{-1.5}{s} \rightarrow \frac{-1.5(1-\tau_d)}{z-1}+z^{-1}\frac{-1.5\tau_d}{z-1} \tag{4.19}$$

$$\frac{-1}{s^2} \rightarrow \frac{(-0.5+\tau_d-0.5{\tau_d}^2)z+0.5(-1+{\tau_d}^2)}{(z-1)^2}$$

$$+z^{-1}\frac{\tau_d(-1+0.5\tau_d)z-0.5{\tau_d}^2}{(z-1)^2} \tag{4.20}$$

Adding (4.19) and (4.2) gives

$$H(z,\tau_d)=\frac{(-2+2.5\tau_d-0.5\tau_d{}^2)z^2+(1-4\tau_d+\tau_d{}^2)z+(1.5\tau_d-0.5\tau_d{}^2)}{z(z-1)^2} \quad (4.21)$$

We can quickly verify that for τ_d =0, (4.21) turn into (4.12). However, for $\tau_d \neq 0$, the equivalent H(z) is no longer (4.12).

The key point is, excess delay always **alters the numerator coefficients of the equivalent H(z)**, and it turns out that using rectangular pulses yields simulation results that are similar to those found using more realistic pulse shapes.

4.3.2 Root locus of effect of Excess Loop Delay

The easiest way to grasp the effect of excess delay is to linearize the quantizer and look at the stability of the noise transfer function. There is, however, the gain of a one bit quantizer isn't well-defined. That is, we could insert a positive gain k immediately

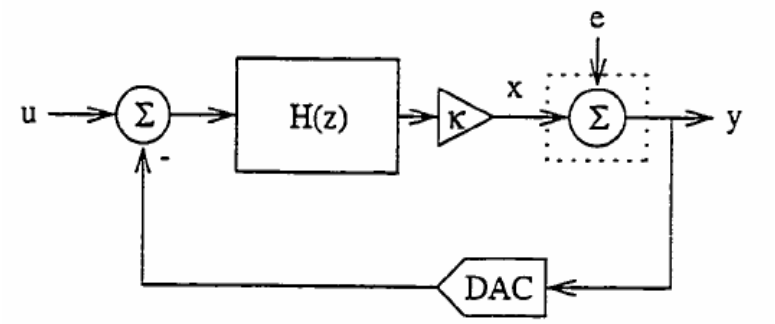


Fig 4. 8 Linear SDM with one-bit quantizer arbitrary gain k.

in front of the quantizer and not affect the performance of the circuit—quantizer

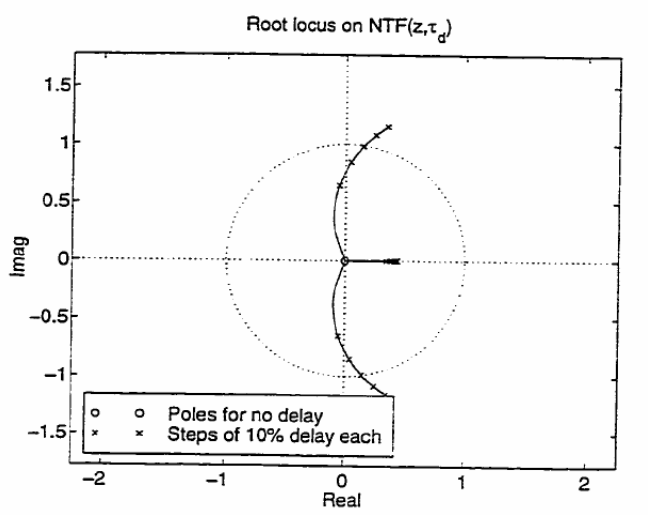


Fig 4. 9 Effect of loop delay on root locus of NTF (z, τ_d)

inputs would be scaled, but their signs remain unchanged, hence the sequence of ± 1 would be identical. Making k explicit is usually done in the linear model as shown in figure 4.8, which results in NTF(z, τ_d)=(1+kH(z, τ_d))$^{-1}$. Figure 4.9 shows that for k=1 and increasing ρ_d , the poles of NTF(z, τ_d) move towards the unit circle, eventually moving outside at $\rho_d \approx 0.31$. Any choice of k >0 shows a similar movement of poles from their initial positions towards the unit circle; this implies modulator stability worsens as delay increases.

CH5 Implementation of Low-Power GM-C Continuous-Time SDM

5.1 Introduction

In this chapter, we will introduce the implementation of a 3rd-order continuous-time GM-C sigma-delta modulator. In section 1, we will show the behavior simulation of the SDM. In section 2, we will discuss the circuit level design of the GM-C SDM. In section 3, we will show the performance and layout of the SDM.

5.2 Behavior Simulation

5.2.1 Determine the coefficients for CRFB structure

The first step in the design of a ΣΔ modulator is the selection of the NTF. The modulator order, the number of quantization levels, and the low-pass or band-pass are all design parameters.

We have two methods to determine the coefficients for ΣΔ in Z-domain.

METHOD 1:

The MATLAB have freeware tool to get coefficients by the Delta-Sigma Toolbox. Although it is based on filter design to determine loop filter structure, user doesn't necessary to understand algorithmic details before making use of the toolbox. A complete reference manual for this freeware toolbox, including instructions for obtaining it, may be found in MATLAB web or reference [14].

The function which synthesizes the NTF is *synthesizeNTF*. The first two arguments to *synthesizeNTF* specify the order of the NTF and the over-sampling ratio, while the third argument(opt) is a flag which specifies whether or not the NTF zeros are to be optimized

for maximum attenuation of quantization noise in the band of interest. Optional fourth and fifth arguments specify the NTF's out-of-band (Hinf) and ,for band-pass modulators, $\|H\|_\infty$ defaults to 1.5. Likewise, since the center frequency was not specified, f_0 defaults to zero. The default value of *synthesizeNTF* function as following below:

ntf = synthesizeNTF (order=3,OSR=64,opt=0,H_inf=1.5,f0=0)

Use of *synthesizeNTF* 's optional arguments is illustrated in Fig.5.1, which contains both the MATLAB code for designing the NTF of a low-pass modulator.

```
order = 3;
OSR = 64;
opt = 1;
H = synthesizeNTF (order, OSR, opt);
plotPZ(H);
f = linspace (0, 0.5, 1000);
z = exp(2i*pi*f);
plot(f, dbv(evalTF(H,z)));
```

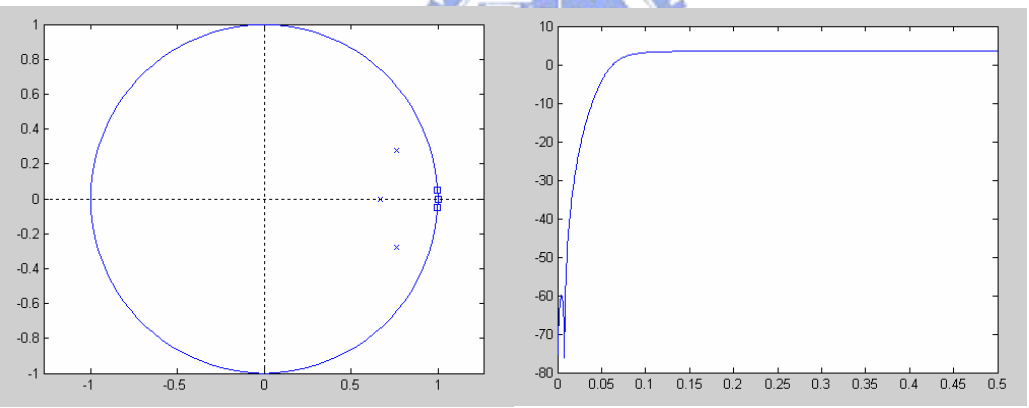


Fig 5. 1 MATLAB code for creating a low-pass NTF.

After studying the function *synthesizeNTF*, we will learn two instructions *realizeNTF* and *scaleABCD*. The coefficients returned by *realizeNTF* are those of an unscaled modulator, i.e. a modulator whose internal states occupy an unspecified range. In order to restrict the state range to known values, dynamic-range scaling must be performed. Dynamic-range scaling can be applied to any linear system on a state-by-state basis, which means the internal state is scaled down by *k* times to reduce all incoming branches signal, and make up for the attenuation so introduced by multiplying all out-going branches by the same factor *k* times.

The toolbox function scaleABCD uses simulations to determine the required scaling factors for each state of a delta-sigma modulator. The modulator is simulated with inputs of various amplitudes in order to determine the maximum stable input amplitude (umax) as well as the maximum value that each state achieves for input amplitudes up to umax. The ABCD matrix of the modulator is then subjected to dynamic range scaling so that the maximum value of each state equals the specified limit (xlim, which defaults to 1). The toolbox function mapABCD then translates the scaled ABCD matrix back into the coefficients for the chosen topology.

Then we are going to determine to SDM coefficients step-by-step by the toolbox function we studied. Below we design a OSR = 50, order = 3 ,1 bit and scale the state to 0.2 modulator, the result is shown if Fig 5.2.

```
H = synthesizeNTF (3, 50, 1);
Form = 'CRFB';
[a,g,b,c] = realizeNTF(H,form);
b(2:end) = 0;
ABCD = stuffABCD(a,g,b,c,form);
[ABCD umax] = scaleABCD(ABCD,2,0.2);
[a,g,b,c] = mapABCD(ABCDs,form);
```

i	a_i	g_i	b_i	c_i
1	0.15656	0.01021	0.15656	0.28933
2	0.24871	0	0	0.23195
3	0.13235	0	0	4.2017

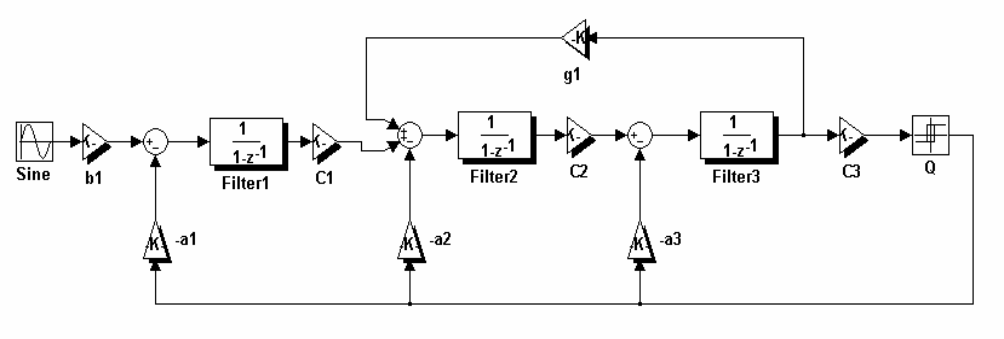


Fig 5. 2 MATLAB code with coefficient and CRFB structure

The form in MATLAB code is the loop filter structure. If form is 'CIFB' to be means cascade-of-integrator (CI) filters and feedback (FB) DAC. There are four topologies which supported by toolbox CIFB, CIFF, CRFB and CRFF.

METHOD 2:

To use behavioral simulation result of the modulator is by SIMULINK. First setting all of the OP or GM gains to be required value (ex: 40dB) and the over-sampling ratio, and use loop code to sweep all coefficients like a_i b_i c_i and g_i. We can get a nice set of coefficients relative to highest SNR.

5.2.2 Transfer coefficient from discrete-time to continuous-time

When we get coefficients in Z-domain, next step is to transfer it to time-domain. It should be depend on the instruction "*d2cm*" in MATLAB. For example, we have a discrete-time sigma-delta in Fig 5.3, then use *d2cm* to transfer coefficients to time domain.

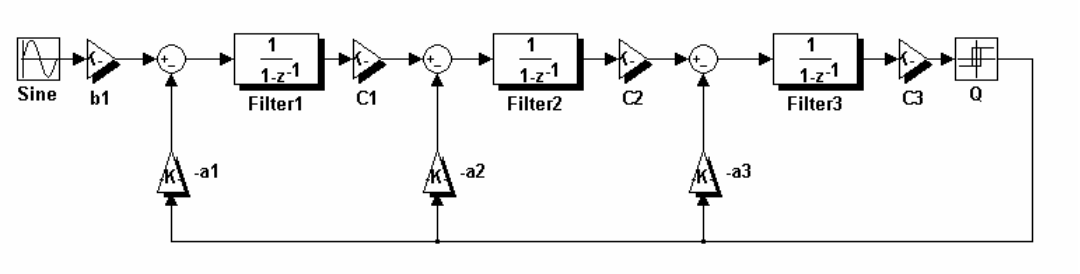


Fig 5. 3 A CIFB ΔΣ structure

We first calculate the loop filter transfer function H(z), and get the numerator and denominator of H(z). If we set the value c1 = 0.2, c2 = 0.3, c3 = 0.4, a1 = -1, a2=-1 and a3= -1 in Fig 5.3, then will get the transfer function H(z) is

$$H(z) = \frac{-0.4z^2 - 0.92z - 0.304}{(z-1)^3} \tag{5.1}$$

Then use MATLAB built-in functions *d2cm* to transfer H(z) to $\hat{H}(s)$. We type

[num , den] = d2cm([-0.4 -0.92 -0.304],[1 -3 3 -1], 1)

d2cm is the discrete-to –continuous conversion routine of the control toolbox. The first two arguments are the numerator and denominator of H(z) in descending powers of z, while the third argument is the sample period Ts. MATLAB returns

num = 0 -0.0813 -0.0960 -1.6240

den = 1.0000 -0.0000 0.0000 -0.0000

which are the numerator and denominator of $\hat{H}(s)$ in descending powers of s in other words, $\hat{H}(s) = (-0.0813s^2 - 0.096 - 1.624)/s^3$.

Using SIMULINK structure the continuous time sigma-delta is shown in Fig 5.4.

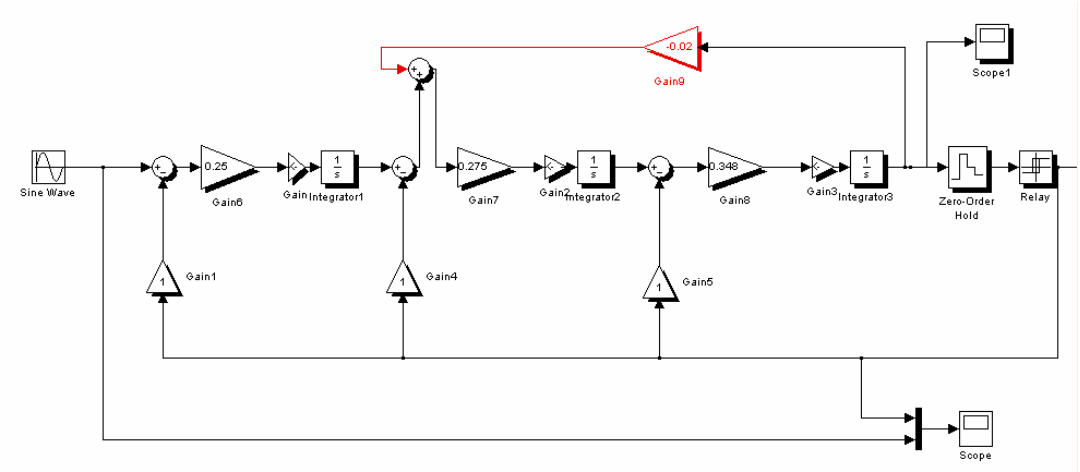


Fig 5. 4 CRFB continuous-time ΔΣ in time domain

The time-domain output data is shown in Figure 5.5 and the plot of power spectrum density is shown in Figure5.6.

Fig 5. 5 The time-domain output data

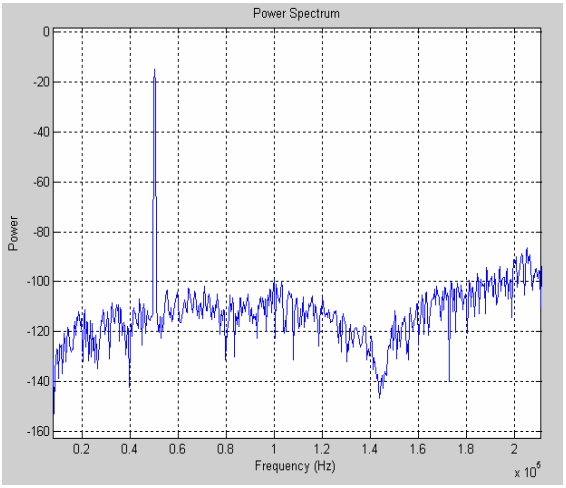


Fig 5. 6 The power spectrum of output data

5.2.3 Optimization of the NTF zeros

For example, the first step in finding an optimal second-order modulator is to find the second-order NTF which yields the highest SQNR (signal to quantization-noise ratio), or equivalently, the NTF which minimizes the in-band noise. For high values of OSR, the magnitude of NTF(z)=$(1-z^{-1})^2/A(z)$ in the passband is approximately $k\omega^2$. By shifting the NTF zeros from z = 1 to z = $e^{\pm j\alpha}$, the magnitude of the NTF in the passband becomes $k(\omega-\alpha)(\omega+\alpha)=k(\omega^2-\alpha^2)$. The integral of the square of this quantity over the

passband is a measure of the in-band noise, and can be minimized by choosing α such that

$$I(\alpha) = \int_0^{\omega_B} (\omega^2 - \alpha^2)^2 \, d\omega \tag{5.2}$$

is minimized. The solution to this optimization problem can be obtained by differentiating I(α) with respect to α, and equating the result to 0. This gives

$$\alpha_{OPT} = \omega_B / \sqrt{3} \tag{5.3}$$

Since the ratio I(0) / I(α opt) = 9/4, the expected SQNR improvement is 10 log(9/4) = 3.5dB. Using the same method to calculate high order optimization NTF, the NTF with degrees from 1 to 6 is shown in Table 5.1.

Table 5.1 The zero placements for minimum in-band noise

N	Zero locations	SQNR improvement
1	0	0 dB
2	$\pm 1/\sqrt{3}$	3.5 dB
3	$0, \pm\sqrt{3/5}$	8 dB
4	$\pm\sqrt{3/5 \pm \sqrt{(3/7)^2 - 3/35}}$	13 dB
5	$0, \pm\sqrt{5/9 \pm \sqrt{(5/9)^2 - 5/21}}$	18 dB
6	$\pm 0.23862, \pm 0.66121, \pm 0.94911$	23 dB

5.3 Circuit level Simulation

From the system level simulation, we can predict and obtain the system performance roughly. There are many ideal components in the system level simulation. But for circuit level implementation, there are more detail considerations in the design. We will discuss

the circuit level implementation of each component for the 3-order continuous-time SDM. For low-power application the single loop architecture as shown in Figure 5.7.

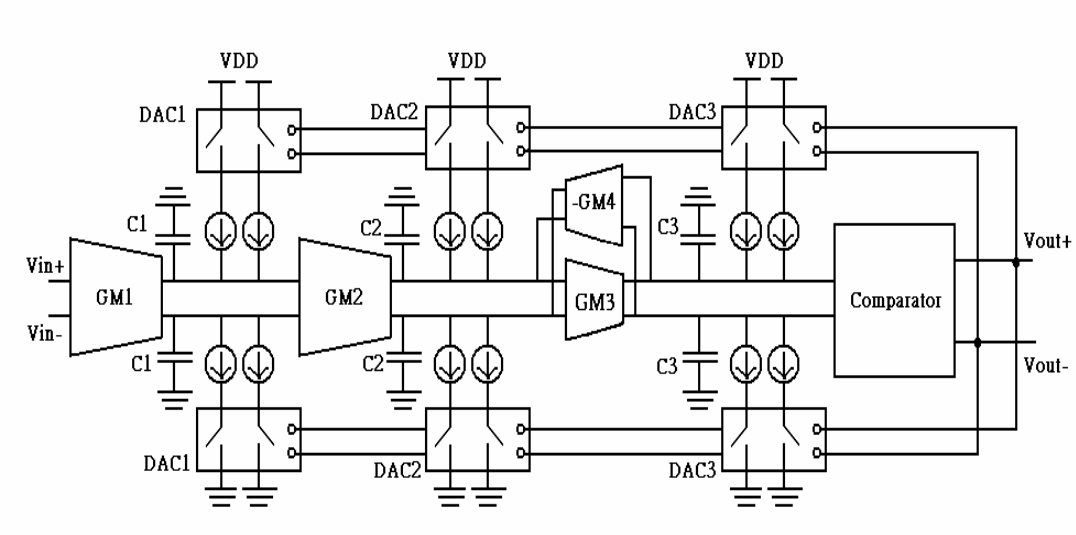


Fig 5. 7 Implementation of third-order GM-C continuous-time SDM

5.3.1 GM cell

The major contributor of the ΣΔ modulator overall power dissipation is the first GM-C integrator when using single-loop architecture. Therefore, optimizing the performance of amplifier for what we need is very important. A proper circuit can save a substantial amount of power consumption. The specification of the first integrator influences the overall system performance very much. The finite DC-gain, distortion, and noise of the first integrator reduce performance of the entire ADCs since these errors add directly to the input signal.

Besides, the non-ideal effect of finite op dc gain is the most widely-studied. An ideal integrator has a DT transfer function F(z)=1 / (z-1); it can be shown that an integrator built from an op amp with dc gain A_0 results in a transfer function

$$F(z) = \frac{1}{z - p(1 - 1/A_0)} \qquad (5.4)$$

where p is a constant. Finite op gain causes leaky integration: the NTF zeros are moved

off the unit circle towards z = 0, which reduces the amount of attenuation of the quantization in the baseband and therefore worsens SNR.

A good rule of thumb which applies to both DT and CT ΣΔ is that the integratiors should have $A_0 \geq OSR$, the oversampling ratio[16]. If this holds, the SNR will be only about 1 dB worse than if the integrators had infinite dc gain [17]. Because the OSR is about 20MHz / (2*200kHz) = 50, we will let A_0 is 50 (34dB).

Let us consider the common drain amplifier in Fig. 5.8(a), frequently used as a voltage buffer. If body effect is neglected the circuit follows the input voltage with a dc level shift, i.e., Vo=V_{GS1}+Vi, where V_{GS1} is the source-to-gate voltage of transistor M1. . Concerning large-signal behavior, this circuit is able to sink a large current from the load, but its

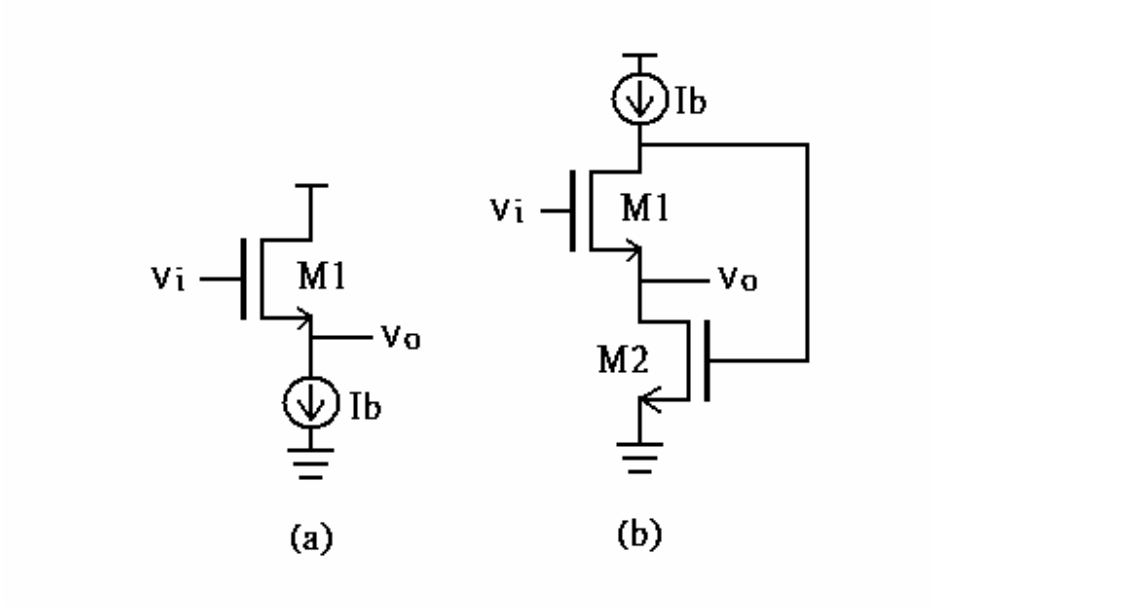


Fig 5. 8 (a) Common-drain amplifier (voltage follower) (b) FVF.

sourcing capability is limited by the biasing current source. A drawback of this circuit is that current through transistor M1 depends on the output current, so that V_{GS1} is not constant and, hence, for resistive loads, the voltage gain is less than unity. A similar problem occurs with capacitive loads at high frequencies. The circuit in Fig. 5.8(b) also operates as a source follower where the current through transistor M1 is held constant, independent on the output current. It could be described as a voltage follower with shunt feedback. Neglecting body effect and the short-channel effect, V_{GS1} is held constant, and

voltage gain is unity. Unlike the conventional voltage follower, the circuit in Fig. 5.8(b) is able to source a large amount of current, but its sinking capability is limited by the biasing current source I_b. **The large sourcing capability is due to the low impedance at the output node**, which is (see derivation below) approximately ro=1/(gm1gm2ro1) , where gm_i and ro_i are the transconductance and output resistance of transistor , respectively.

The FVF GM is shown in Fig.5.9.The gain-bandwidth, phase-margin and GM plot are shown in Figure 5.10 and the complete simulation of the GM results is shown in Table. 5.2.

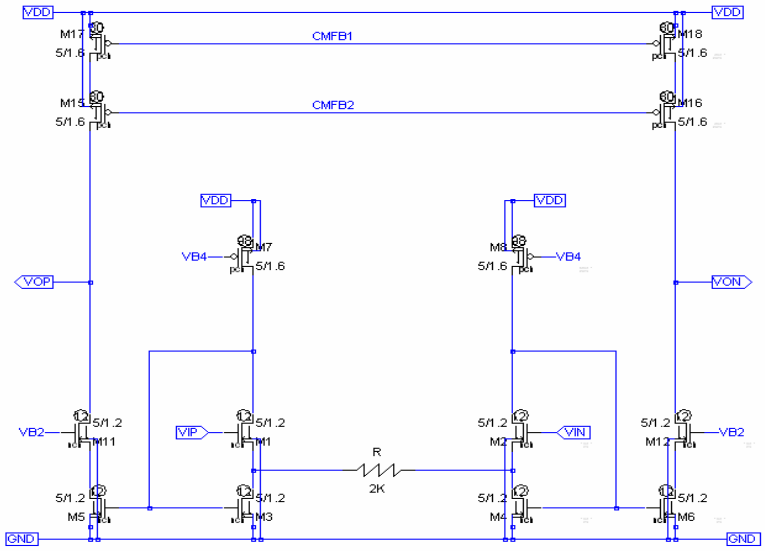


Fig 5. 9 Schematic of FVF GM

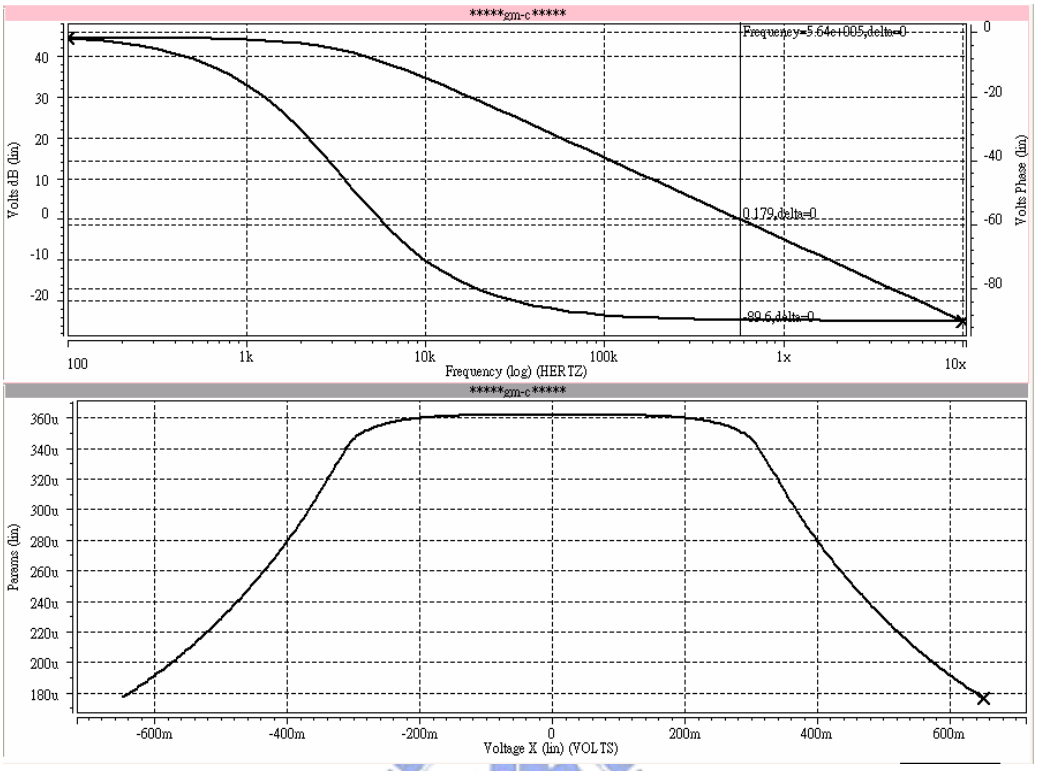


Fig 5. 10 Gain-bandwidth, phase-margin and GM of FVF

The distortion magnitude of the second and third integrator will be attenuated through the loop filter of the ΣΔ modulator with OSR for the second integrator and OSR^2 for the third integrator [18]. For this integrator is sown in Fig.5.11 that design the linearity requirement of the second integrator is equal to 3 dB to obtain the performance

of the modulator (SNR=70 **dB) .** When we suppose that the DAC is perfectly linear. The GM-C integrator used in this design is shown in Fig.5.11. The open-loop gain and the

transconductance of the G,-cell are given by equation (5.5).

$$GM = \frac{1}{\frac{2}{gm1} + R} \qquad (5.5)$$

Table 5.2 Specification of the first amplifier

Parameters	*Simulation Result*
DC gain	44 dB
Phase Margin	90.4 degree
Unity Gain Frequency	564 kHz(Cload=40pf)
GM	360μA/V
Max. diff input	600mV
Power Dissipation	520μW
Technology	Standard TSMC 0.18μm 1P6M

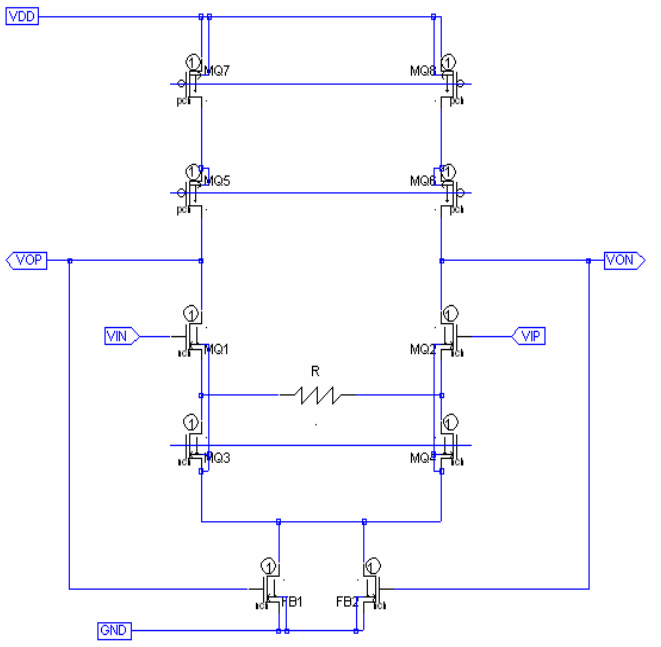


Fig 5. 11 Schematic of 2nd, 3rd source degeneration GM

Assuming a sinusoidal input signal Uin = Vin .sin(ωt), the third harmonic distortion of the GM-C integrator due to input devices is calculated in Eq(5.6).

$$HD_3 \approx \frac{\beta^3 \cdot I_{DS5}(R \cdot \sqrt{\beta \cdot I_{DS5}} + 1)}{32(\beta \cdot R \cdot I_{DS5} + \sqrt{\beta \cdot I_{DS5}})^4} \cdot V_{in}^2 \qquad (5.6)$$

The noise power of the integrator will be noise shaped with OSR^3 for the second integrator and with OSR^5 for the third integrator.

5.3.2 Comparator

The comparator circuit is depicted in Figure5.12. This circuit is similar to the current-mode comparator presented in [19]. Its offset current is about 0.2uA in simulation. At its inputs, current mirrors, biased with the same current as the 3rd integrator, copy the input signal to a clocked CMOS cross coupled latch. The non-overlapping clock signal required for the sampling signal CLK and the latch enable signal, responsible for the validation of the comparator output, is shown in figure 5.13.

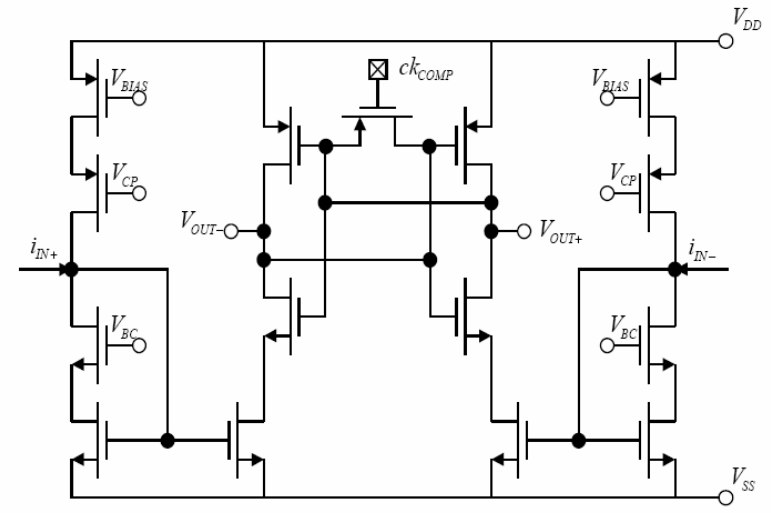


Fig 5. 12 Current-Mode Comparator.

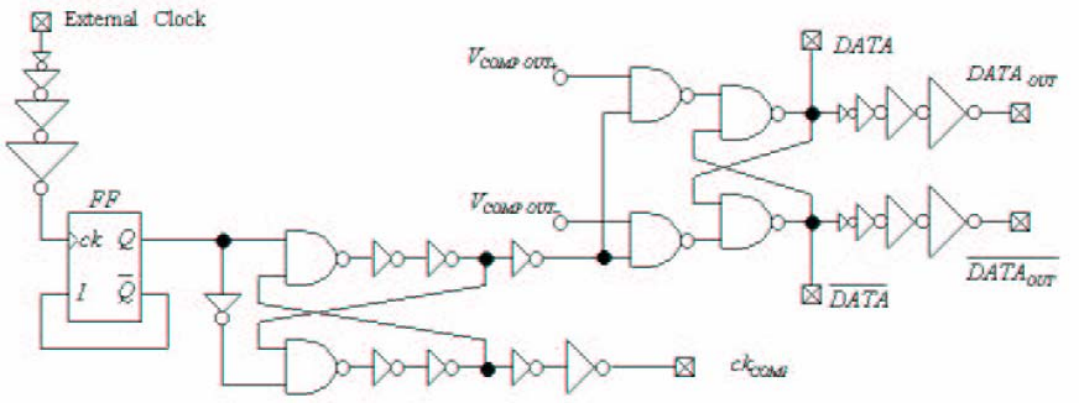


Fig 5. 13 Comparator latch and sampling clock

5.3.3 Feedback DAC

The single-bit current-steering DAC in the feedback loop of the CT ΣΔ modulator is explained in Fig 5.14(a) (b).

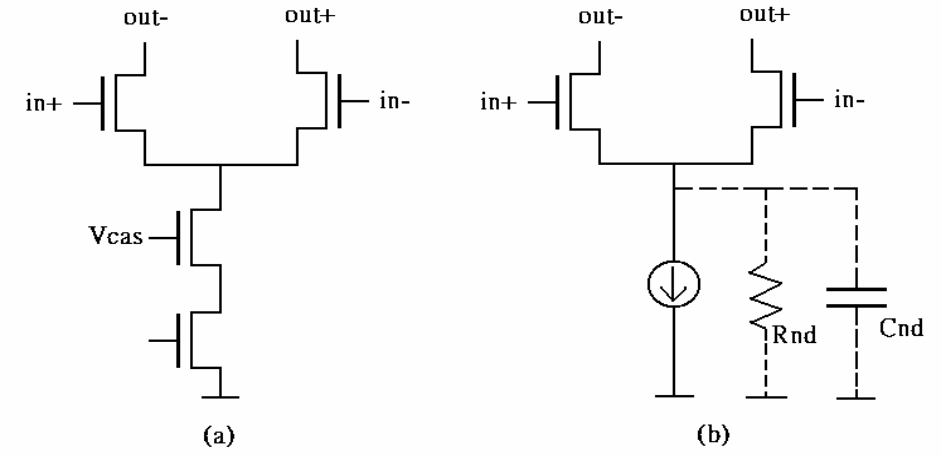


Fig 5. 14 (a) The cascade transistors DAC. (b) DAC with ideal current source.

The DAC outputs of the switches are connected to the output nodes of the GM-C integrator. The impedance of the current source is made finite by placing a parallel resistor Rnd across it. The output impedance of the DAC is

$$R_{out}(f) = \frac{R_{nd}(g_m r_O)_{switch}}{(1 + j2\pi \frac{f}{f_d}) \cdot (1 + j2\pi \frac{f}{f_{nd}})} \quad (5.7)$$

The value of the fd is dominant pole generated by GM-C. The impedance of the current source Rnd defines the value of the output impedance, as shown in Fig 5.14(b). At the same time, it puts the location of the non-dominant pole

$$f_{nd} = \frac{1}{2\pi \cdot R_{nd} C_{nd}} \quad (5.6)$$

A higher value of Rnd increases the dc output impedance of the D/A converter, but lowers the non-dominant pole and hence the phase margin of the integrator. This tradeoff is illustrated in Fig. 5.15[20]. The lower limit for the output impedance is put by the dc gain requirement. In this case, a DAC output resistance of at least Rout (GM-C) is required to limit the leakage of in-band quantization noise. On the other hand, a lower limit of five times the integrator GBW is set on the non-dominant pole frequency. Both constraints define a working area for the design of the DAC.

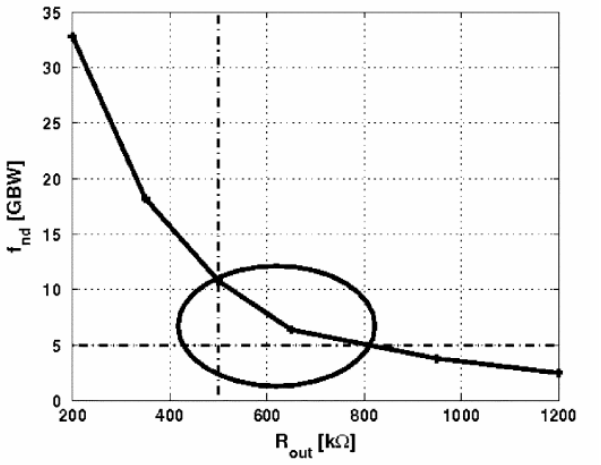


Fig 5. 15 Tradeoff between dc output resistance and the non-dominant pole. [20]

In general, the cascade transistor has rather small dimensions in order to limit Cnd. This is because the current transistor output impedance is in general already high. In this way, fnd can be placed at a sufficient distance from the integrator GBW.

5.4 Simulation Result

Fig 5.16 is the plot of simulation in time-domain. And Fig 5.17 is the plot of power spectrum of the proposed continuous-time GM-C SDM. The sampling rate is 20MS/s and input signal frequency is 39k Hz. The SFDR is 69.3 dB, SNR is 70.1dB and SNDR is 71.2 dB.

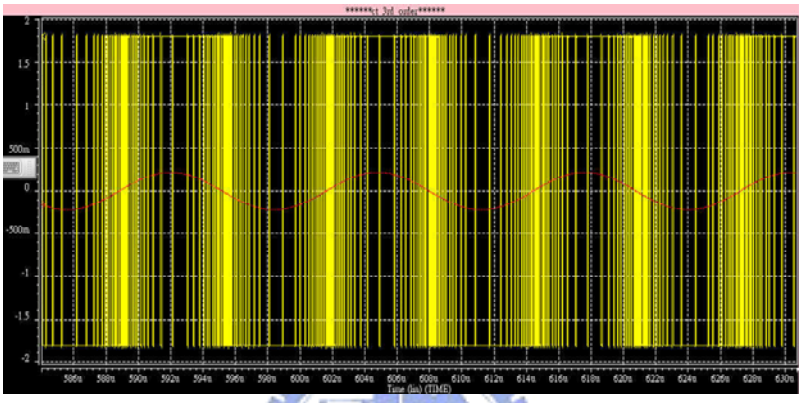


Fig 5. 16 The simulation of continuous-time GM-C SDM in time-domain.

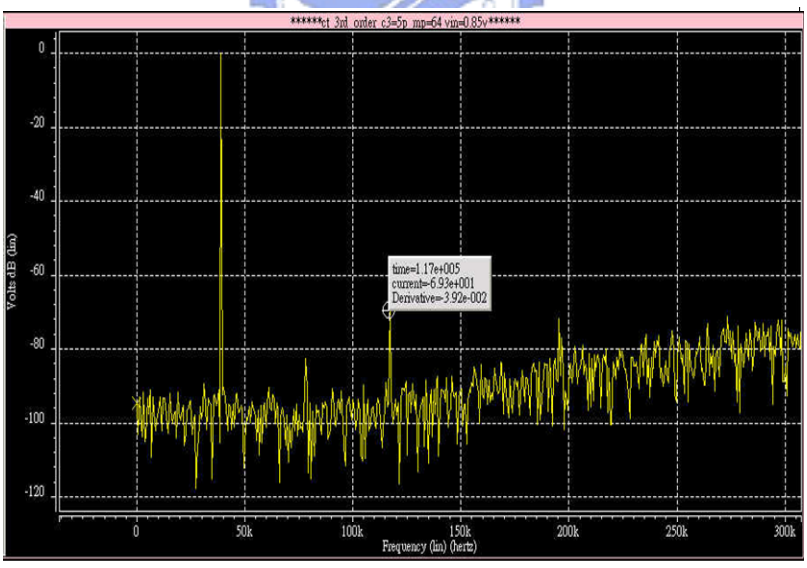


Fig 5. 17 The power spectrum of continuous-time GM-C SDM.

The all parameters of CT GM-C SDM are in table 5.3.

Table 5.3 The specification of the continuous-time GM-C SDM.

Parameters	*Simulation Result*
Technology	TSMC 0.18 μ m Mixed-Signal
Supply voltage	1.8V
Input range	0.3V
Chip size	635.6um*1046.82um
Sample frequency / Signal bandwidth	20MHZ/200kHz
SNR/SFDR/SNDR	70.9dB/69.3dB/68.4dB
Resolution	11.53 bits
Power Dissipation	0.978mW

5.5 Layout level design

After the circuit level design, the real physical implementation is referred as the layout level. There are many detail problems to consider in layout level such as parasitic effect, component mismatch, noise consideration and ESD protection…etc. To avoid such problems, we use some technique for layout level design. (1) Use multi-finger transistors to avoid high gate parasitic resistance. (2) Use component summarization and dummy cell to improve components matching. (3) Use guard ring to prevent parasitic problems. The layout diagram is present in Figure 5.18 and the layout size is 635.6um*1046.82um.

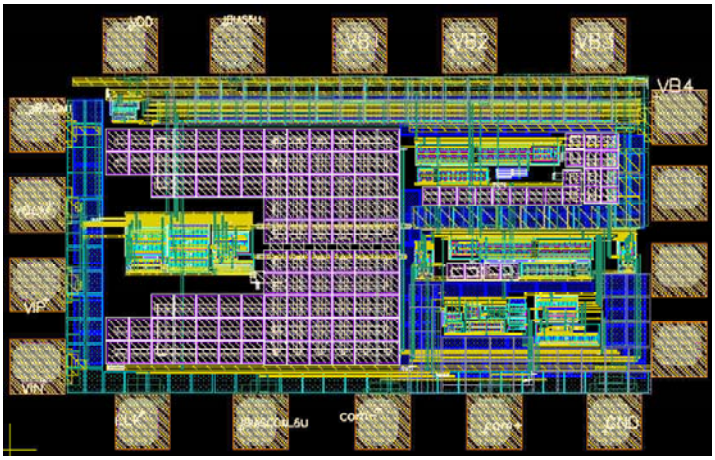


Fig 5. 18 Diagram of SDM layout

CH6 Test Setup and Experimental Results

This 3-order continuous-time SDM has been fabricated by TSMC 0.18-μm CMOS Mixed-Signal process with one poly and six mental. In this chapter, we present the testing environment, including the component circuits on the DUT (device under test) board and the instruments. The measured results are presented in this chapter, too.

6.1 Measuring equipment

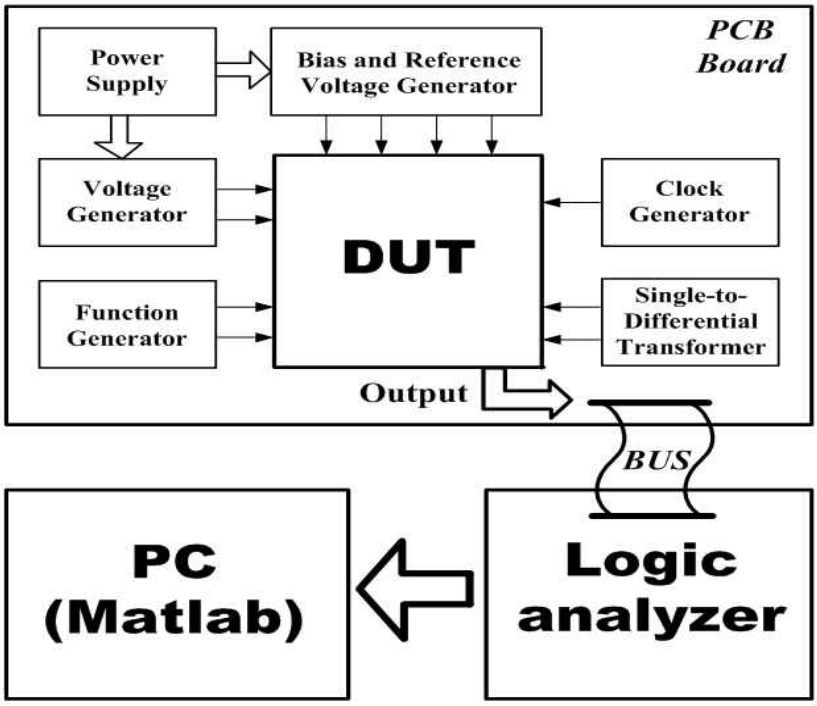


Fig 6. 1 Experimental testing setup

Figure 6.1 shows the whole measurement process and the testing setup used to measure the performance of the proposed SDM. We adopt a PC (for MATLAB processing), an oscilloscope, two power supplies, a function generator and a pulse generator. The testing printed circuit board (PCB) contains voltage regulator, clock generator, single to differential transformer circuit, and the DUT. The supply voltages for regulators are supplied by the 9V batteries and the input signal and clock are provided by the function generators Agilent 33250A as shown in Figure 6.2. The digital output signals

will be fed into the logic analyzer Agilent 16702B as shown in Figure 6.3. And we can show the output waveform by the oscilloscope Agilent 54832D as shown in Figure 6.4. Finally, the data will be loaded into the PC and be analyzed with MATLAB to obtain the specification of the proposed SDM.

Fig 6. 2 Function generator Agilent 33250A

Fig 6. 3 Logic analyzer Agilent 16702B

Fig 6. 4 Oscilloscope Agilent S4832D

6.2 Power supply regulators

The supply voltages are generated by LM317 adjustable regulators as shown in Figure 6.5. The capacitor C1 is added to improve the transient response and capacitor C2 is the bypass capacitor. The output voltage of the Figure 6.5 can be expressed as

$$V_{out} = 1.25 \cdot \left(1 + \frac{R2}{R1}\right) \cdot I_{ADJ} \cdot R2 , \qquad (6.1)$$

where I_{ADJ} is the DC current that flows out of the adjustment terminal ADJ of the regulator.

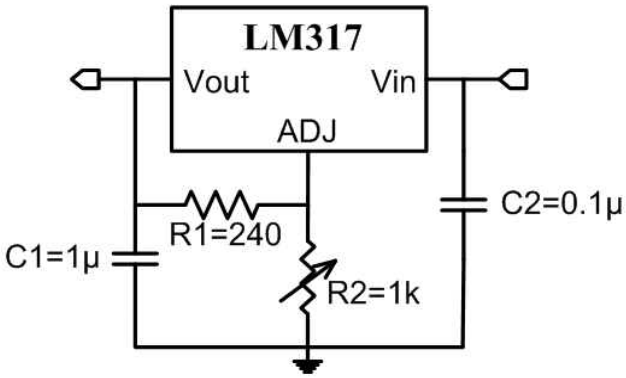


Fig 6. 5 Power supply regulator

6.3 Input terminal circuit

A function generator can only provide AC component of input signal and the input signal is single-end. So we need the input terminal circuit which combined single-to-differential transformer circuit and AC couple circuit as shown in Figure 6.6. Because we can't ensure the common mode voltage is that we need, we need the adjustable resistances to tune the voltages. The splitter can split single-end signal to differential-end signal input+ and input-.

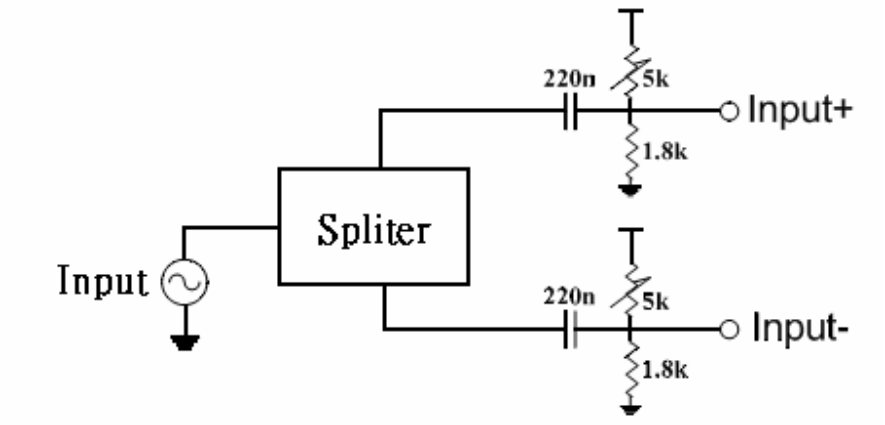
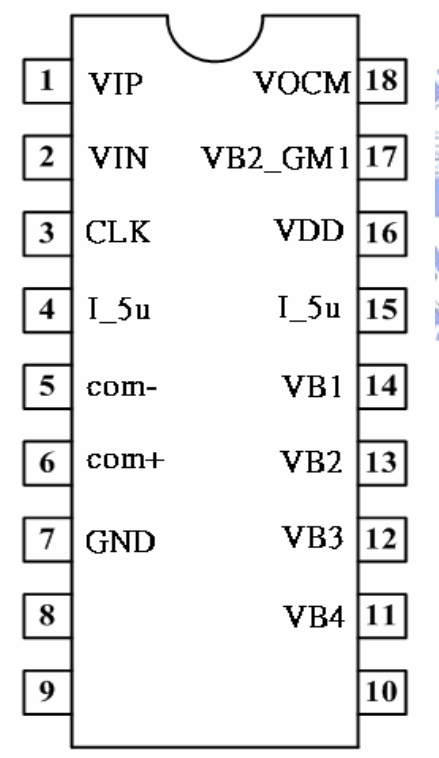


Fig 6. 6 Input terminal circuit

6.4 Pin configuration and testing board



Pin	Name	I/O	Describe
1	VIP	In	Input Signal (0°)
2	VIN	In	Input Signal (180°)
3	CLK	In	System clock input
4	I_5u	In	Bias current 5uA
5	OUT-	Out	Output Signal (0°)
6	OUT+	Out	Output Signal (180°)
7	GND	-	DUT Ground
8	NC	-	No connection
9	NC	-	No connection
10	NC	-	No connection
11	VB4	In	Bias Voltage
12	VB3	In	Bias Voltage
13	VB2	In	Bias Voltage
14	VB1	In	Bias Voltage
15	I_5u	In	Bias current 5uA
16	VDD	-	DUT Supply Voltage
17	VB2	In	Bias Voltage
18	VOCM	In	Common mode voltage

Fig 6. 7(a) Pin configuration diagram and (b) Pin assignment

Figure 6.7 presents the pin configuration and lists the pin assignments of the experimental SDM. Figure 6.8 shows the photograph of the testing DUT board.

6.5 Performance evaluations of SDM

This proposed SDM chip has fabricated by TSMC 0.18 μm technologies. It was powered by 1.8 V supply. A 60 kHz sine wave is applied and the clock rate is 20MHz while the corresponding bandwidth is 200 kHz. The time-domain analysis is measured by an oscilloscope (Fig 6.9).

Fig 6. 8 Photograph of the SDM DUT board

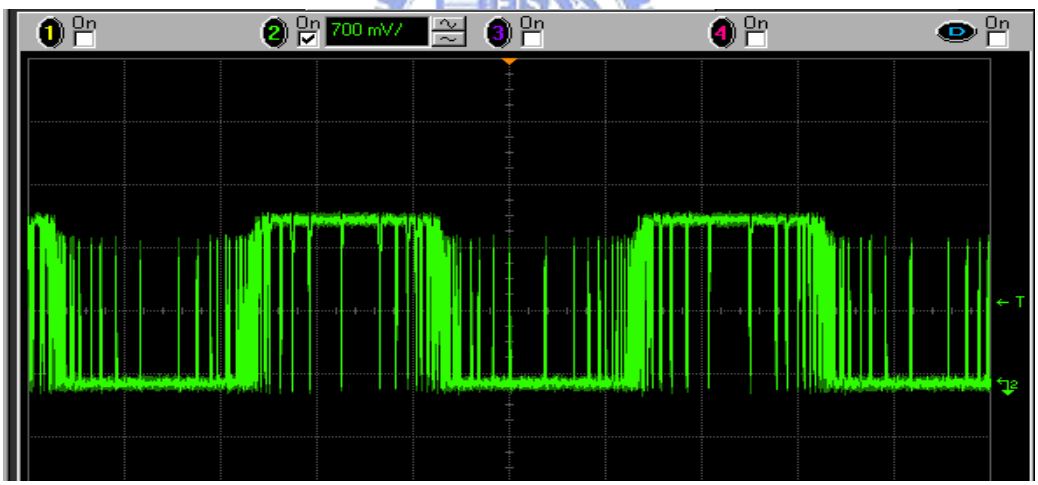


Fig 6. 9 Measurement result of output waveform

Fig 6.10 shows the measured spectrum. The input signal frequency is 60 kHz and the signal bandwidth is 200 kHz. The output bit streams can be recorded with a logic analyzer, so that the data can be processed with MATLAB. The fast Fourier transformation with 16384 points was used.

Figure 6.11 shows the SNDR versus normalized input signal. The peak SNDR and DR are 45dB and 49dB, respectively. This corresponds to a resolution of 7.2 bits. The power consumption is only 0. 98mW. The complete measured performance summary of the third-order SDM is given in Table 6.1.

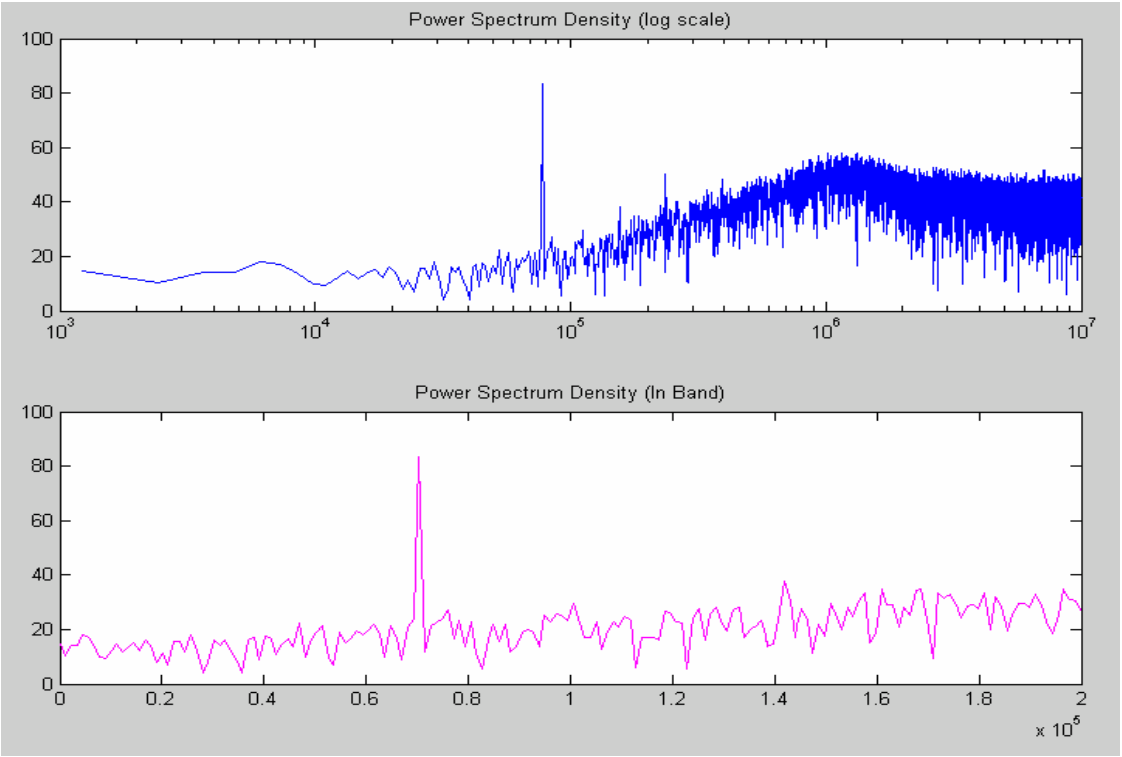


Fig 6. 10 Measured output spectrum

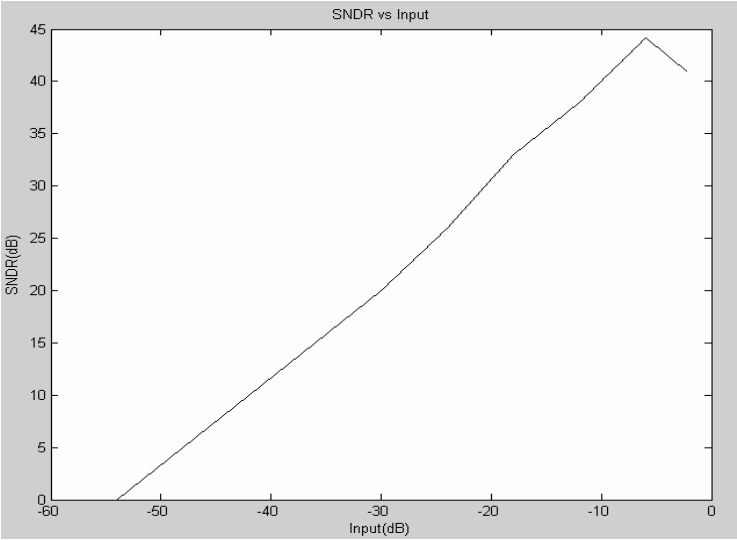


Fig 6. 11 Plot of SNDR versus normalized input signal

Table 6.1 Summary of measured results of the SDM

Specification	*Measured Results*
Signal Bandwidth	200 kHz
Sampling Frequency	20 MHz
Dynamic Range	49 dB
Peak SNDR	45 dB
Peak SNR	47.8 dB
Resolution	7.2 bits
Area	0.635*1.046mm^2
Power Dissipation @ 1.8V	1.85 mW(include output buffer)
Technology	Standard TSMC 0.18μm 1P6M

6.6 Summary

The design of third-order continuous-time SDM was completed. It took the design considerations described in Chapter 5 into account. The original resolution was predicted to achieve 11.2bits. The measured result shows that the actual performance is 7.2bits. The possible reasons of performance decay are that the output buffer is too small can not push output pad, that cause the noise floor too high and the 3-rd harmonic signal too large. And the mismatch of input differential signal is also the possible reason which causes the performance decay.

CH7 Conclusions

This thesis presents the basic concepts for SDM including quantization noise, noise shaping strategy, and system overview of SDM are introduced. The expected 70 dB SNR is in GSM communication application.

A systematic design approach for DT-to-CT transformation of the ΔΣ modulators based on the Impulse-invariant has been proposed. The proposed technique is general and well-design in MATLAB. Using MATLAB SDM toolbox is easily to get coefficient in time-domain. The GM-C integrator can save more power than RC integrator, and use FVF GM to simplify the filter design. The optimize NTF in 3-rd order SDM improve 8dB SNQR. After system level simulation for building the behavior model to understand the characteristics of SDM and determine the specification, the circuit level and layout level design are presented.

In the thesis, a low power continuous-time SDM with GM-C integrator is fabricated in TSMC CMOS 0.18 μm standard process. The measured resolution is 7.2 bits, 200 kHz bandwidth, and the measured power consumption is only 0.98 mW for a 1.8V supply. The integrator circuit was designed using the method described in chapter 5.The influence of circuit design parameter and non-ideal effect like amplifier gain and distortion on overall SDM has been studied.

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