Improved RF Power Performance in a 0.18-μm MOSFET Which Uses an Asymmetric Drain Design

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***Abstract*—We have fabricated 0.18-μm asymmetric MOSFETs using a foundry-standard 1P6M process, without making any process modifications. In comparison with a conventional 0.18-μm MOSFET, the asymmetric MOSFET design leads to a 64% improvement in the saturated output power and 8 dB better adjacent channel power ratio. The improvement in the RF power performance of these MOS transistors suggests that they should be suitable for medium power amplifiers.**

***Index Terms*—Asymmetric, lightly doped-drain (LDD), MOS, RF Power.**

I. Introduction

THE technology evolution and down-scaling of Si MOSFETs have produced continuing improvements in the RF gain, cutoff frequency (f_t), maximum oscillation frequency $(f_{\max})$, and RF noise figure [1]–[4]. However, the down-scaled devices show little improvement in the RF output power, which is limited by the low drain breakdown voltage. A transistor design, termed Lateral Diffused MOS (LDMOS), has been proposed to improve the RF output power, by increasing the drain breakdown voltage. However, the RF performance of an LDMOS device comes at the expense of a relatively large on-resistance, and low f_t and $f_{\max}$ [5]–[8]. Additional processing steps and masks are also needed for LDMOS, when compared with standard CMOS. To address this issue, we have previously proposed an asymmetric-lightly doped-drain (LDD) MOSFET which can increase the drain breakdown voltage and RF output power [12]. However, it is unclear if the improved RF power performance of such an asymmetric-LDD MOSFET can be further improved at shorter gate lengths with higher operation frequencies. In this letter, we report on the performance of an asymmetric MOSFET having a 0.18-μm gate length. This asymmetric-LDD MOSFET has been fabricated within a conventional foundry process. The output power of the asymmetric-LDD MOS transistor has been found to increase by as much as 64% at 2.4 GHz under saturated power conditions. This performance is better than or comparable with the data of other MOS transistors for high-frequency power applications [5]–[10] with additional advantage without making any process modifications.

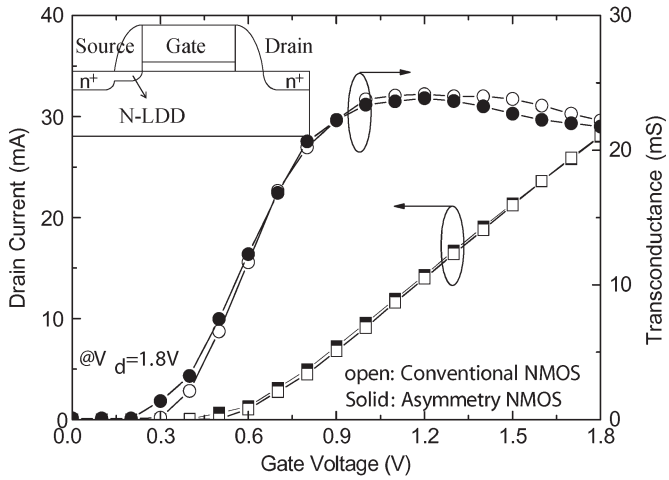

Fig. 1. I_d–V_d and g_m–V_d characteristics of conventional and asymmetric-LDD 0.18-μm RF MOSFETs.

II. Experimental Details

A foundry-standard 0.18-μm CMOS process was accessed in this letter. The asymmetric-LDD MOSFET used the n^+ ion-implantation blocking mask to cover in the drain extension under the spacer. A detailed device structure can be found elsewhere [12]. With this design, a wide depletion region is formed under the spacer on the drain side. This feature increases the transistor breakdown voltage, which is important for RF power amplifiers. We designed 10-gate-finger 0.18-μm MOSFETs with a 5-μm overall width—this helped decrease the gate resistance. For comparison, conventional 0.18-μm MOSFETs with the same RF layout were also included on the chip. The S-parameters were measured, up to 26.5 GHz, using an HP8510C network analyzer. The RF power characterization was carried out by on-wafer measurements at 2.4 GHz using an ATN load-pull system, where the input and output impedance matching conditions were selected to optimize the output power.

III. Results and Discussion

In Fig. 1, we show the I_d–V_g and g_m–V_g characteristics, where the schematic diagram of this device structure is also

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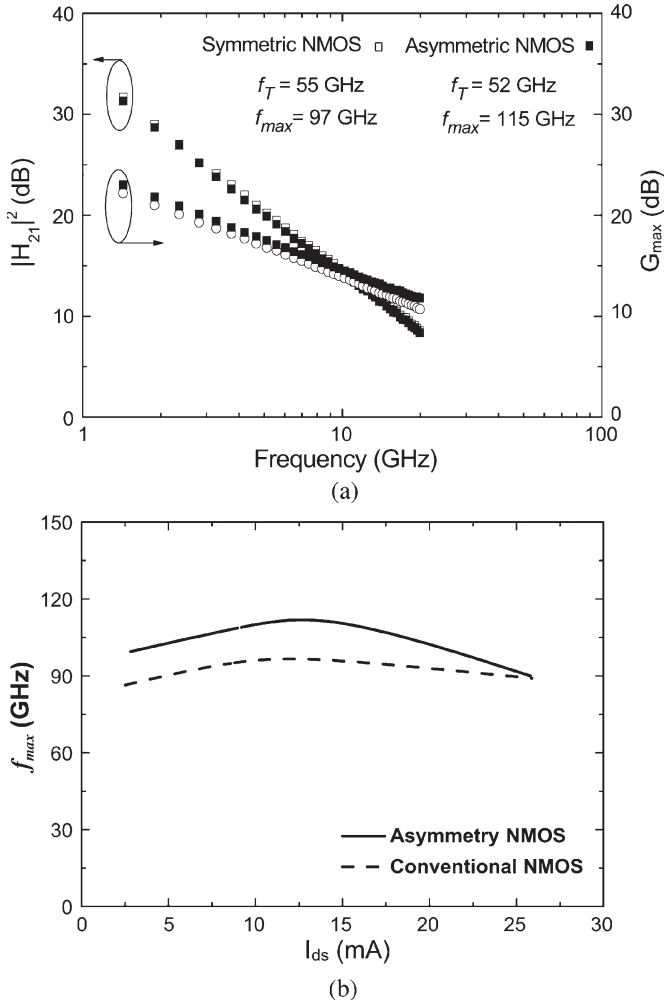

Fig. 2. (a) Measured $|H_{21}^2|$ and $G_{\max}$ characteristics for the conventional and Asymmetry 0.18-μm RF MOSFETs at $V_{\rm ds}$ of 1.8 V. (b) $f_{\max}$ as a function of $I_{\rm ds}$.

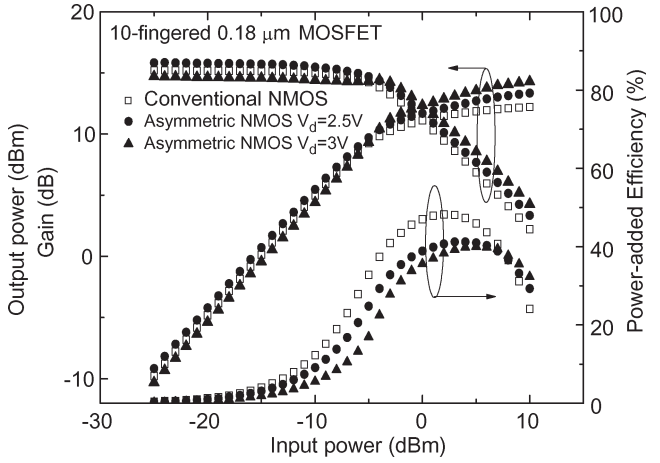

Fig. 3. RF output power and PAE for the conventional and asymmetric-LDD 0.18-μm RF MOSFETs at 2.4 GHz.

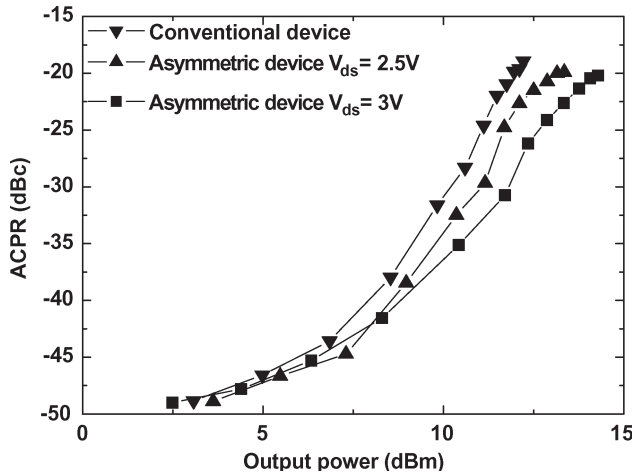

Fig. 4. Measured ACPR versus output power data for the conventional and asymmetric-LDD 0.18-μm RF MOSFETs at 2.4 GHz.

inserted. For both the asymmetric-LDD and conventional devices, the measured peak g_m of $\sim$490 mS/μm was almost the same. The drain breakdown voltage at $V_g = 0$ V($BV_{\rm dss}$) was increased from 3.5 V in the conventional MOSFET to 6.9 V in the asymmetric device, at the same 0.18-μm gate length. Thus, the asymmetric device allows a higher drain bias of 3 V or twice that (6 V) for the RF power swing. This large improvement in $BV_{\rm dss}$ is due to the wide depletion region under the spacer region, and between drain and substrate—all this is similar to features of bipolar transistors.

Fig. 2(a) shows the current gain ($|H_{21}^2|$) and power gain ($G_{\max}$) as a function of frequency, for both conventional and asymmetric-LDD MOSFETs. A cutoff frequency f_t of 52 GHz was obtained from the measured S-parameters for the asymmetric-LDD MOS device. This compares well with the 55-GHz value found for the conventional MOSFET. This high f_t in the asymmetric-LDD MOS device occurs because the inversion electrons transit the wide depletion region, under large reverse-biased voltage, with a high saturation velocity. The asymmetric-LDD device shows an $f_{\max}$ of 115 GHz which exceeds the 97-GHz value of the conventional MOSFETs. This is due to smaller feedback capacitance on the drain side ($C_{\rm gd}$) [13] in the LDD structure. The dependence of $f_{\max}$ on $I_{\rm ds}$ is shown in Fig. 2(b), where higher $f_{\max}$ of asymmetric-LDD MOS device than conventional MOSFET is obtained at wide $I_{\rm ds}$ condition.

The variation of the output power and power-added-efficiency (PAE), as a function of the input power, is shown in Fig. 3 for both device designs. The dc bias point of the conventional MOS transistor was at $V_{\rm gs} = 1.2$ V and $V_{\rm ds} = 1.8$ V—the maximum g_m conditions. At 2.4 GHz, the output power increases from 0.33 W/mm for the conventional device to 0.43 (30%) or 0.54 (64%) W/mm for the asymmetric-LDD device at $V_{\rm gs} = 1.2$ V and $V_{\rm ds} = 2.5$ or 3 V, respectively, under saturation power conditions. The PAE for the asymmetric-LDD devices was 41% (drain efficiency of 52%) which is close to the values for the conventional design. The slightly lower PAE of the asymmetric-LDD MOSFET is due to the larger drain series resistance. The high RF power density is attractive for power amplifier designs [14].

An important RF power characteristic is the adjacent channel power ratio (ACPR), as shown in Fig. 4. The ACPR measurement was standard W-CDMA with QPSK modulation from ROHDE and SCHWARZ SMIQ06B signal generator. The calibration was done by ATN on-wafer load pull system. The

TABLE I
COMPARISON OF LDMOS AND ASYMMETRY MOSFET PUBLISHED DATA WITH THAT FROM THIS LETTER
(*CALCULATE FROM P_{1dB}; **4-dB COMPRESSION; **6-dB COMPRESSION)

	f_t (GHz)	f_{max} (GHz)	BV_{dss} (V)	Power (W/mm) @ Freq.	PAE (%) @ Freq. &V_D	Drain Eff. (%) @ Freq. &V_D	Device
[5]	31	47	15.5	0.21 1.8GHz	48 1.8GHz, 3.6V	75 1.8GHz, 3.6V	0.3 μm LDMOS
[6]	18	-	15	-	60 0.9GHz, 12V	-	0.18 μm LDMOS
[7]	15	38	45	0.25* 1.9GHz	41 2.4GHz, 12V	46 2.4GHz, 12V	0.15 μm LDMOS
[8]	32	26	14	0.092 0.9GHz	53 0.9GHz, 3.5V	71 0.9GHz, 3.5V	0.3 μm LDMOS
[9]	25	11	5.4	0.1** 2.4GHz	39 2.4GHz, 2.5V	45 2.4GHz, 2.5V	0.24 μm CMOS
[10]	140	100	3.2	0.353*** 2.4GHz	43 3GHz, 1.5V	46 3GHz, 1.5V	90 nm CMOS
This Work	55	97	3.5	0.33 2.4GHz	48 2.4GHz, 1.8V	60 2.4GHz, 1.8V	0.18 μm Conventional MOS
	52	115	6.9	0.54 2.4GHz	41 2.4GHz, 3V	52 2.4GHz, 3V	0.18 μm Asym. MOS

asymmetric device showed as high as 8 dB better improvement at the peak PAE. The improved linearity arises from the decreased interaction between gate and drain contacts, indicated by the smaller $C_{\rm gd}$, compared with the conventional device. Thus, better output power density and linearity are attainable in the asymmetric device. The data is summarized in Table I, where the RF performance of the asymmetric-LDD MOSFET is better than or compared with other LDMOS [5]–[10] devices with added merit without any process modifications.

IV. CONCLUSION

The low drain breakdown voltage of conventional CMOS transistors is a major limitation for their RF power performance. This can be improved by more than 60% by using an asymmetric-LDD design, and with 8 dB better linearity. These devices can be manufactured in a standard CMOS logic process.

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