國 立 交 通 大 學

電信工程學系

碩 士 論 文

針對 Giga-Hertz
基底雜訊抑制的主動保護電路

An Active Guarding Circuit for Giga-Hertz Substrate Noise Suppression

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指導教授：李育民 博士　　Dr. Yu-Min Lee

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中華民國九十六年六月

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摘　　要

爲了改善 p 型守護環狀結構在高頻的效果，本論文提出一個針對 Giga-Hertz 基底雜訊的主動保護電路。此電路利用了雜訊去耦和反向前饋方式。提出的反向前饋電路藉著引入一個零極點和一個振幅調節方式，能夠有效使抑制基底雜訊達到 Giga-Hertz。此電路不僅提供了去耦路徑，而且檢測出雜訊程度並傳遞到振幅調節器執行雜訊相消。經由 0.13-μm CMOS 製程進行電路實作，藉著應用推出的主動保護電路，頻率從直流到 1GHz 被動 p 型守護環狀結構的抑制能力能夠被改善多於 14dB 以上。

An Active Guarding Circuit for Giga-Hertz Substrate Noise Suppression

Student:Chien-Lung Wang Advisor:Dr. Yu-Min Lee

Co-Advisor:Dr. Kuei-Ann Wen

ABSTRACT

In order to improve p+ guard-ring performance for high frequency substrate noise suppression, this thesis presents an active guarding circuit employing noise decoupling and inversion feedback for substrate noise suppression in high frequency up to GHz. Proposed inversion feedback circuit can efficiently suppress high frequency substrate noise up to GHz range by introducing a zero and an amplitude controller. The noise decoupling circuit not only provides a decoupling path, but also senses the noise level for the amplitude controller to perform noise cancellation. By applying the proposed active guarding circuit implemented in 0.13um CMOS process, the noise suppression of passive guard ring can be improved more than 14dB in the frequency range from DC to 1GHz.

誌謝

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最後，感謝默默支持我的母親和祖父母以及弟弟。你們不斷的支持與鼓勵，讓我覺得更需要努力來回報你們。

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Chapter 1

Introduction

The drive for lower cost, smaller size and more features has motivated the combining of analog circuits with digital subsystems. However, continuous down-scaling of CMOS technology has leaded VLSI design to “System-on-Chip” (SOC) design, a single chip solution for both digital and analog circuits. Examples are single chip cameras, cellular phones, and handheld computers or new generations of combined telecommunication systems that include analog, digital signal processing circuitry. The analog circuits needed at the interface between the electronic system and the continuous-valued outside world are also being integrated on the same die for motivations of price and performance. However, this single chip solution is facing the problem of analog performance degradation due to impact of digital switching noise, also called substrate noise. This substrate noise comes from digital circuit, as digital circuit switches in the common substrate. The substrate noise will couple to analog circuit on the common substrate and influence sensitive analog circuit integrity. Hence such integration causes substrate coupling noise resulting in the degradation of signal integrity. Substrate noise generation and coupling in ICs has been thoroughly

identified as one of these bad affairs. This situation becomes even worse as the supply voltage lowers, and the operation frequency increases, especially when the components are placed more densely on a chip. Such as wireless system on chips, mixed-signal on the same die will only exacerbate the issue.

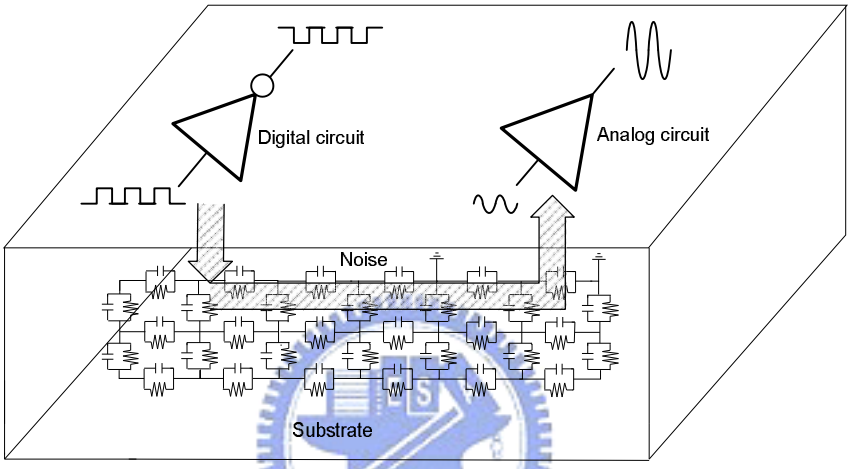


Figure 1 Illustration of substrate noise coupling from a digital circuit to analog circuit

Substrate noise from the digital logic gates travels through the supply lines and the conductive silicon substrate, as depicted in Fig. 1, degrading the performance of sensitive RF/analog circuits. In order to allow more integration without interfering from each component, we have to deal with substrate noise.

1.1 Mechanism of Substrate Noise Coupling

Having known how a cause of substrate noise, the only thing left to discuss is mechanism of substrate noise coupling. An important background is needed to

understand how substrate noise couple and where coupling paths are. This section will discuss, substrate noise coupling through substrate contacts, capacitive coupling and transmission of substrate noise

1.1-1 Coupling Through Substrate Contacts

The body of a transistor in a CMOS circuit is typically tied to a well-defined bias voltage. Generally, the body of the PMOS transistor is connected to the positive power supply voltage and the body of the NOMS transistor is connected to ground. In a uniformly doped substrate, the body of the NMOS transistor is the substrate surrounding the transistor channel. The biasing contacts of the NMOS transistors are directly connected to the substrate.

Consider a device where a digital circuit and an analog circuit share the same substrate. In digital standard cells, substrate contacts are normally present for latch-up reasons. Therefore, the number of substrate contacts which illustrated in Fig.2 can be large in a digital design. Accordingly, the digital ground has formed a very low impedance path to the substrate surface within the region of the digital circuit [1].

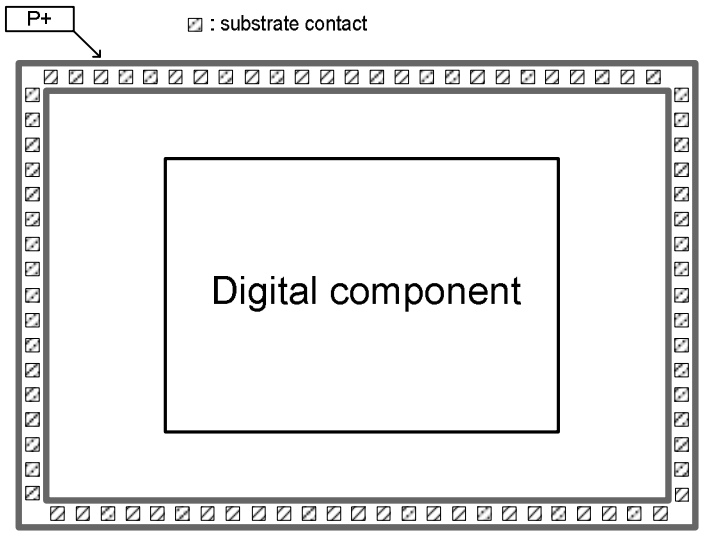


Figure 2 Substrate contact of digital ground

Therefore, any voltage fluctuation on the digital ground is also present in the substrate region of the digital circuit. This noise injection mechanism is normally the dominant one in digital integrated circuits [1]. If the substrate contacts in the analog region have a low impedance path to the analog ground, this causes the substrate noise, in the analog region, to be present on the analog ground. If power supplies of analog and digital circuit are connected together, a sufficiently high power supply rejection ratio (PSRR) of the analog circuit is required to prevent lowered performance degradation.

1.1-2 Capacitive Coupling

The nodes in a circuit on a chip are capacitively coupled to the substrate by interconnects and parasitic PN-junctions. A capacitive coupling can both inject and

receive substrate noise. However, the main contribution to substrate noise normally originates from the noise injected via substrate contacts [1].There are two types of coupling ways：The first is capacitive coupling of interconnects；The second is capacitive coupling of PN-junctions.

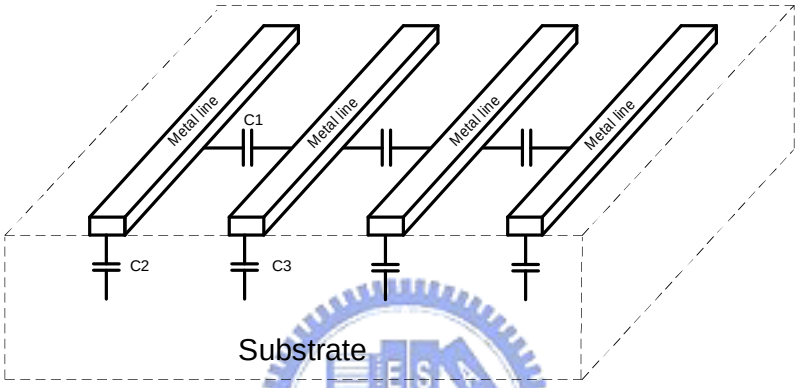


Figure 3 Capacitive coupling of two adjacent interconnects

In the first place on-chip interconnects are capacitively coupled to the substrate and adjacent interconnects as illustrated in Fig. 3. The capacitive coupling between the two interconnects and the substrate is modeled with three capacitors (C1, C2, and C3). The capacitive coupling of interconnects depends on, e.g. which metal layer interconnects are located in, the length and the width of interconnects and the distance to other objects, e.g. interconnects, diffusion area, etc. However, interconnects in the lower metal layers couple more to the substrate than interconnects in the upper metal layers. Analog and digital circuits are normally placed in separate regions of the silicon. Therefore, direct coupling between analog and digital interconnects is rarely

the case, only when digital and analog circuit use common power voltage line. From this remarks one general point becomes very clear. The main coupling is through the substrate.

In the second place, the different doping regions in MOSFETS form parasitic diodes. For example each PN-junction in an NMOS transistor forms a diode as illustrated in Fig. 4.

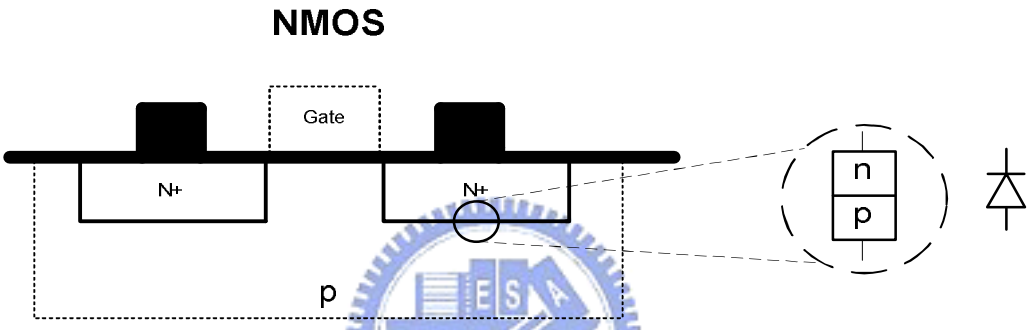


Figure 4 NMOS-transistor with parasitic PN-junction

In CMOS circuit the PN-junctions are usually reverse biased. The parasitic capacitance of a reversed biased PN-junction is nonlinear and voltage-dependent. This capacitance can be approximated to

$$C = \frac{A}{\left[\frac{2}{qe_{si}} V_{bi}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)\right]^{1/2}\left(1-\frac{V_D}{V_{bi}}\right)^m}$$

[2]. A is the area of the PN-junction, V_{bi} is the built in voltage, and V_D is the voltage over the diode. The doping levels for the p region and the n region are denoted as N_A and N_D, respectively. The gradient coefficient is denoted m, q is the elementary charge, and e_{Si} is the permittivity if silicon. Due to the PN-junction, both

the drain and the source of a MOSFET are capacitively coupled to the bulk in CMOS circuit.

1.1-3 Transmission of substrate noise

Substrates play the role of coupling of noise from one device to another. Over the past few years a considerable number of studies have been made on substrate model. Although a large number of studies have been made on substrate model, what seems to be lacking, however, is the accurate model and parasitic value of resistance and capacitance for any frequency and manufacture. To understand the occurrence of substrate coupling, it is important to determine the dominant mechanisms for current flow in the substrate. Substrate model usually can be constructed with resistance and capacitance parallel or series connection.

1.1-4 Effect of receiving substrate noise

MOSFETS have four terminals. The drain current is mainly controlled by the gate source voltage. In analog circuits implemented in CMOS most of the transistors are normally biased in the saturation region. A first order approximate of a long channel

NMOS transistor in the saturation region is

$$I_D = \frac{m_n C_{ox}}{2}\frac{W}{L}\left(V_{GS} - V_{tn}\right)^2\left(1 + lV_{DS}\right) \quad (1.1)$$

$$V_{th} = V_{th0} + g\left(\sqrt{V_{SB} + 2f_F} - \sqrt{2f_F}\right) \quad (1.2)$$

In (1.1) and (1.2) it is seen that the drain current is affected by the threshold voltage (V_{th}), which is dependent of the source body voltage. This effect is known as the body effect. Any voltage fluctuation in the body of a circuit can result in a drain current fluctuation, and further influence NMOS I-V characteristic. Hence, the body effect which is the conjunction of substrate noise may degrade the performance of analog circuit.

1.2 Substrate Noise Suppression Technique and Circuit

Over the past few years a considerable number of studies have been made on substrate noise suppression. A great deal of effort has been made on substrate noise reduction method, what seems to be lacking, however, is the ability for wide band frequency cancellation. Then the purpose here is to explore a little further into substrate noise reduction methods for earlier physical and circuit methods and other

techniques.

1.2-1 Physical methods

A guard ring surrounding the noise receiver or sensitive analog contacts is shown in Fig.5 [3]. The p+ guard ring is connected to the ground pads using a low-ohmic contact.

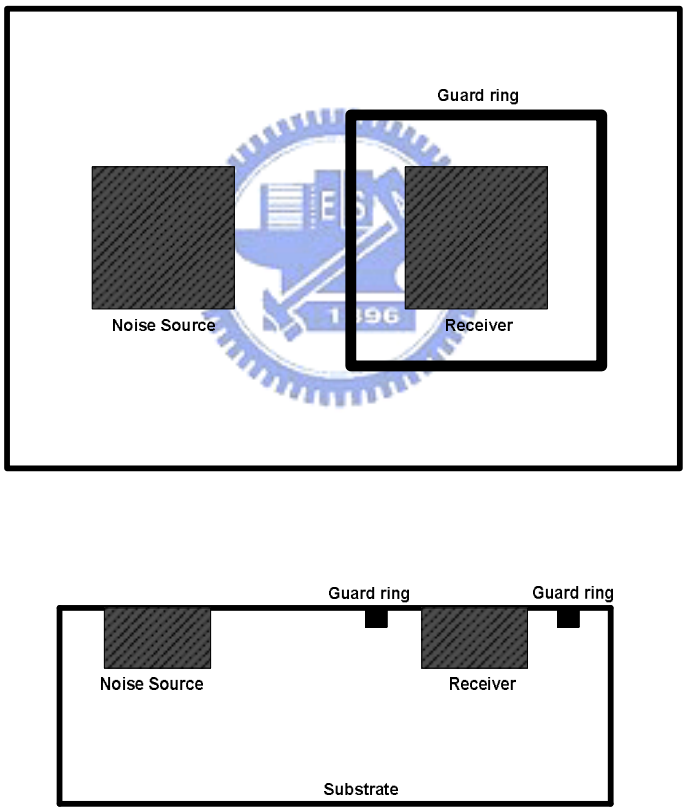


Figure 5 Layout and cross-section of Guard ring surrounding the receiver contact [3]

The ring is a surface-region heavily doped with the majority-carrier doping and is intended to form a Faraday shield around any sensitive device needs to be protected against substrate noise. Guard ring provides the lower impedance path to ground

compare to other paths for substrate noise in chief and the guard ring steers the substrate currents to signal ground. Substrate noise in a sensitive circuit can be reduced if a guard ring is inserted in between a noisy circuit and a noise sensitive circuit. It is one of the most commonly used isolation schemes and seems to be the best suited for preventing crosstalk at operating frequencies. In other case of most modern CMOS technologies use a heavily-doped p+ substrate to diminish latch-up susceptibility. However, the lower resistivity of the substrate creates unwanted paths between various devices in the circuit, thereby corrupting sensitive signals. The guard ring even provides a lower impedance path to ground, but the ratio of heavily-doped substrate and guard ring is not more than the ratio of lightly-doped substrate. From this viewpoint one may say that the guard ring maybe not efficiency for substrate noise suppression, but it is sure to have some isolation ability.

Often theses guard rings are supplemented by placing annular n-type regions around their peripheries as shown in Fig.6 [5]. The n-well guard diffusion acts to detach the sensitive analog circuit by interrupting the low resistance channel-stop implant and forcing the substrate current to flow through the high resistance bulk.

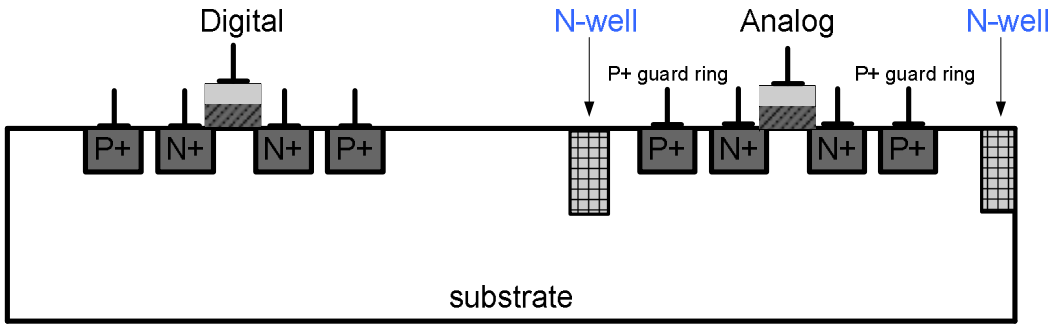


Figure 6 Guard-ring supplemented by placing annular n-type regions around peripheries [5].

This way breaks the low resistance path for the substrate noise current by forming a reverse-biased p-n junction and provides better isolation by forcing the current to flow through the more resistance p^- substrate. In [5], simulation indicate that an n-well guard diffusion, which breaks the p^+ channel stop implant, has almost no effect because most of the substrate current flows in the heavily doped bulk and not in the channel-stop diffusion near the die surface. On the other hand, the simulation show that n-well guard rings are effective when most of the induced substrate current flows through the p^+ field implant region close to the wafer surface of p^- substrate.[3] There are usually good performances by using method of p^+ guard ring and n-well guard ring together for low frequency below 1 GHz. From GHz to far frequency, this performance decreases rapidly like an exponential decay. Beyond this frequency the isolation is degraded as frequency increases due to the capacitive nature of the substrate behavior that kicks in beyond the cutoff frequency.

Another approach, shown in Fig.7, consists of etching a gap between analog and

digital circuits from the back of the wafer. Using an inexpensive mask, a trench can be etched using potassium hydroxide, KOH, from the backside of the wafer all the way to the under-surface of the field oxide, resulting in a structure like a trench. [6]. Experiments show that an interference coupling of 35dB above the noise floor is completely removed when a gap is etched around the analog circuit. The issue of the approach is the need for and extra mask processing causes extra cost and process cycle time.

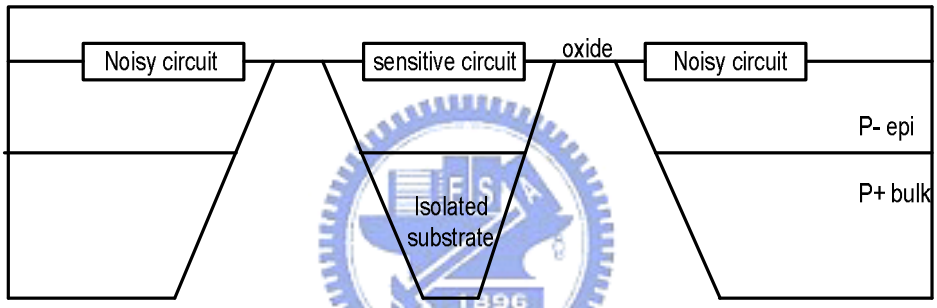


Figure 7 Using KOH to form a trench to protect sensitive circuit [6]

The essentiality of this method must be carefully considered in the design of SOC because the cost for total processing cost.

Then other papers published the buried substrate shield to go a step further protect sensitive device. The buried substrate shields can be categorized in three major types. The first is Faraday shield [7]; the second is dielectric shield [8]; the third is junction shield [9]. Firstly, a highly conductive layer under the switching devices may provide a low-impedance path to ground for the substrate noise. However, if used improperly, this low-impedance path may also cause noise coupling between neighboring devices

[7]. Fig.8 shows layout and cross-section of this way. An experiment done in [7] shows the effectiveness of this method. Results of the test structure are presented in Table.1.

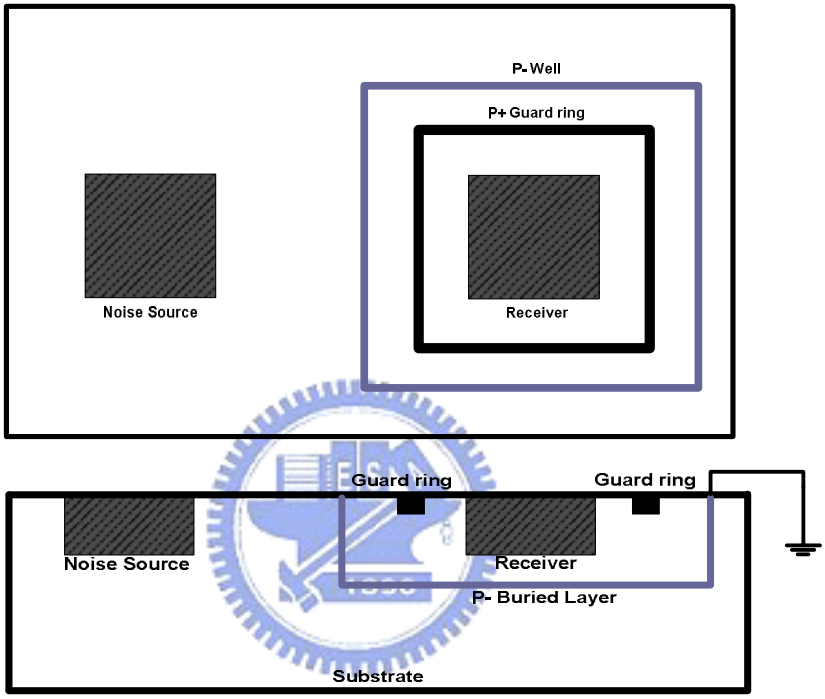


Figure 8 Faraday Shield Layouts and Cross-Section [7]

Method	With deep contacts	Without deep contacts
Without buried layers	N /A	248mV_{pp}
Buried layers only under the digital section	105mV_{pp}	183mV_{pp}
Buried layers only under the analog section	75mV_{pp}	232mV_{pp}
Buried layers only under all circuitry	26mV_{pp}	165mV_{pp}

Table 1 Comparison of the Different Implementations of Buried Layer [7]

Secondly, dielectric isolation is used to isolate the nodes from substrate. This

approach physically increases the impedance between the injector and the receiver by increasing the resistivity of the substrate that surrounds either of the two nodes. This method is implemented in Silicon-On- *Insulator* (SOI). In these substrates, bulk silicon is isolated from the thin active surface silicon layer, by means of buried oxide layer. The layout and cross-section of this method is shown in Fig.9. This method provides very good isolation, but it adds to processing costs, since it requires the use of special silicon substrate [8].

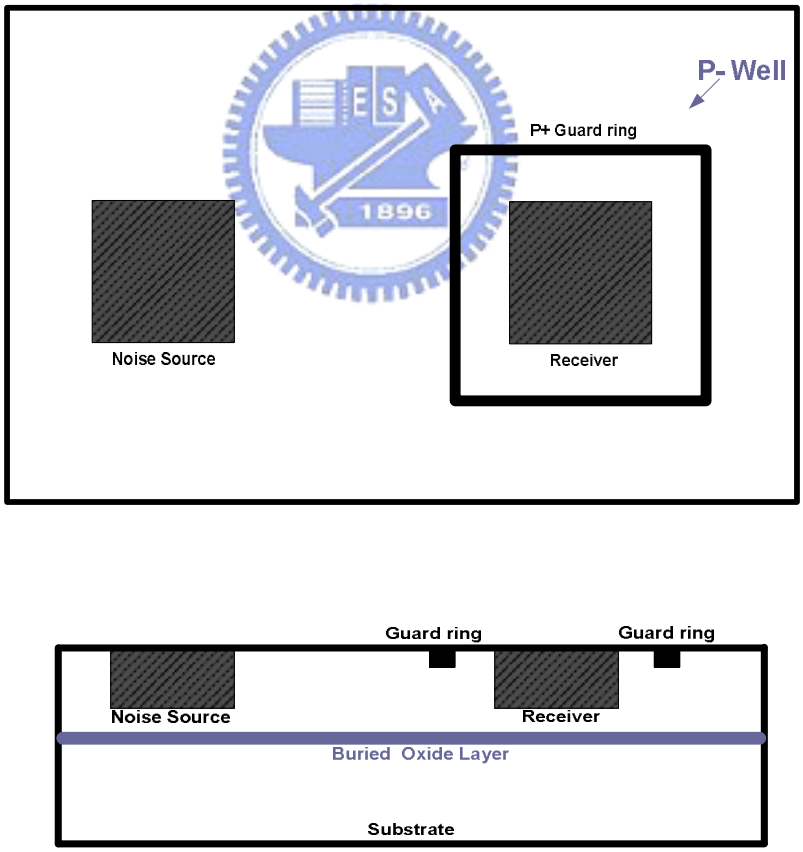


Figure 9 Junction Shield Layouts and Cross-section [8]

Thirdly, a buried minority-type of carrier enclosure around the device plays the role of an isolator. Fig.10 shows cross-section and layout of junction shield. Comparison

between junction shield and dielectric shield is pointed out in Table.2 and showed in Fig.11 [9].

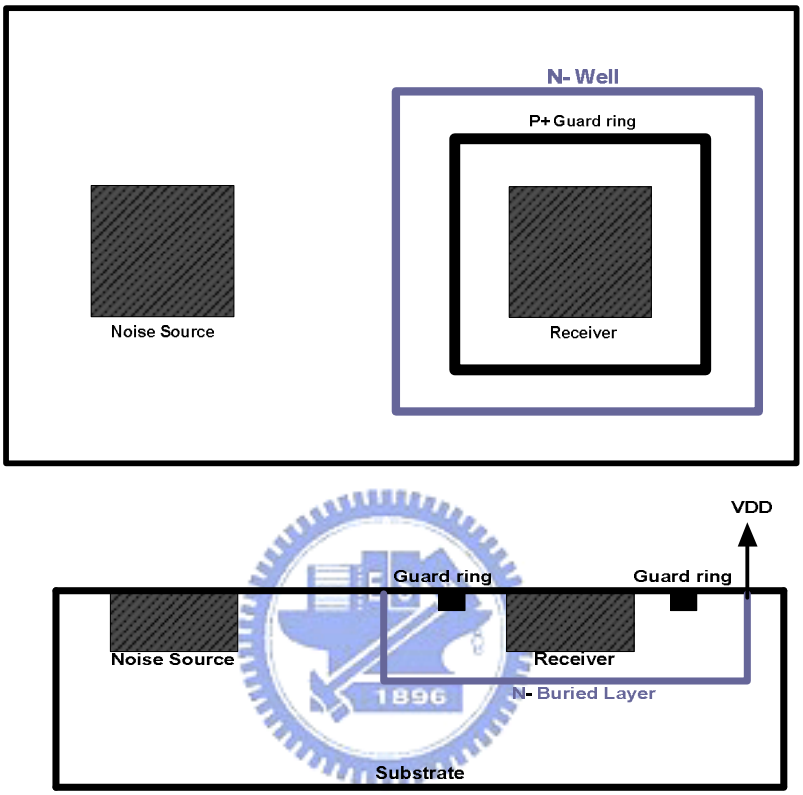


Figure 10 Junction Shield Layouts and Cross-section [9]

Frequency	Dielectric (SOI) Shield	Junction Shield
100MHz	-66 dB	-55dB
200MHz	-54 dB	-51 dB
400MHz	-48 dB	-46 dB
700MHz	-49 dB	-41 dB
1000MHz	-48 dB	-37 dB

Table 2 Comparison between Junction Shield and Dielectric Shield [9]

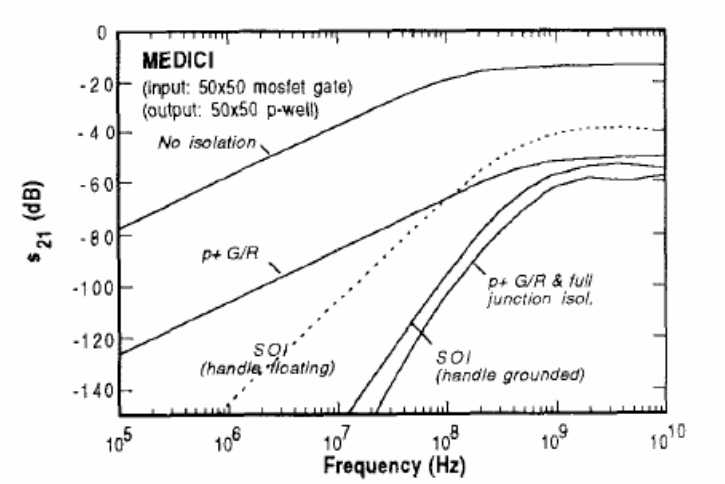


Figure 11 Simulation Result of Comparison between Junction Shield and Dielectric Shield Done by Medici [5]

In [10], this paper reports the effect of using a p-minus substrate guard ring (psub GR) structure to reduce substrate noise coupling. The structure of cross section and magnitude of S21 versus frequency are showed in Fig.12 and Fig.13. It was found that integrating the psub GR into conventional GR designs can improve substrate noise isolation capabilities of conventional p+ guard rings and n-well guard rings by -15dB and -5dB, respectively.

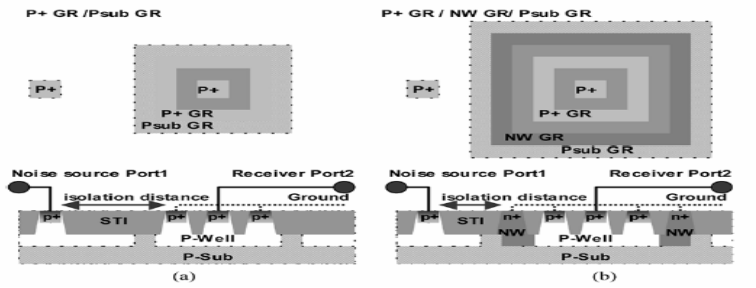


Figure 12 Cross section of psub GR inserted into (a) p+ guard ring scheme (b) Conventional NW GR with p+ guard ring scheme [10]

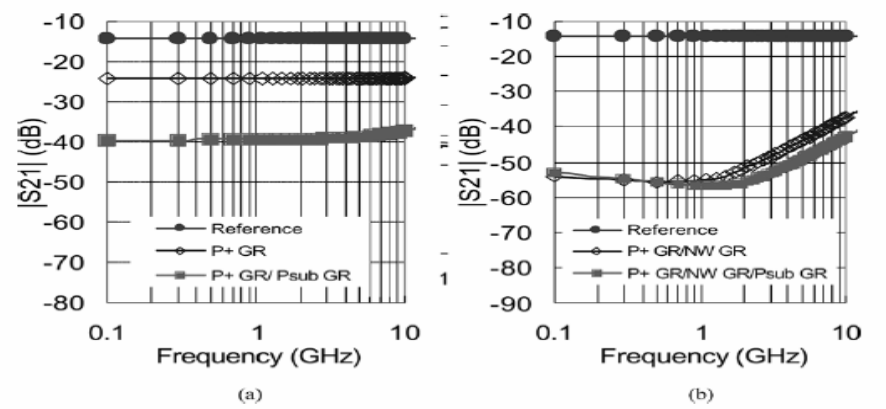


Figure 13 Magnitude of S21 versus frequency at an isolation distance of 10um for reference (without any GR) [10]

From results above, although psub GR improve conventional guard ring, it creates a high resistance surrounding in the receiver port. It will increase latch-up risk in the real application. The parasitic bipolar transistors and resistors create a parasitic silicon-controlled rectifier, or SCR. The schematic for the SCR and its behavior are shown in Fig.14.

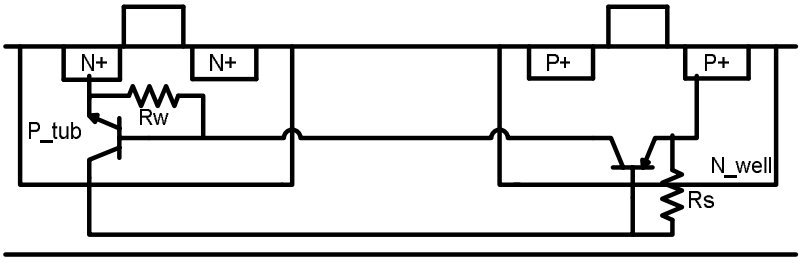


Figure 14 Parasitic that cause latch-up

The switching point of the SCR is controlled by the values of the two power supply resistances R_s and R_w. Because of p-minus increased R_s, the less stray current through the tub is required to cause a voltage drop across the parasitic resistance that can turn on the associated transistor. Then the current flowing through it floods the

tubs and prevents the transistors form operating properly.

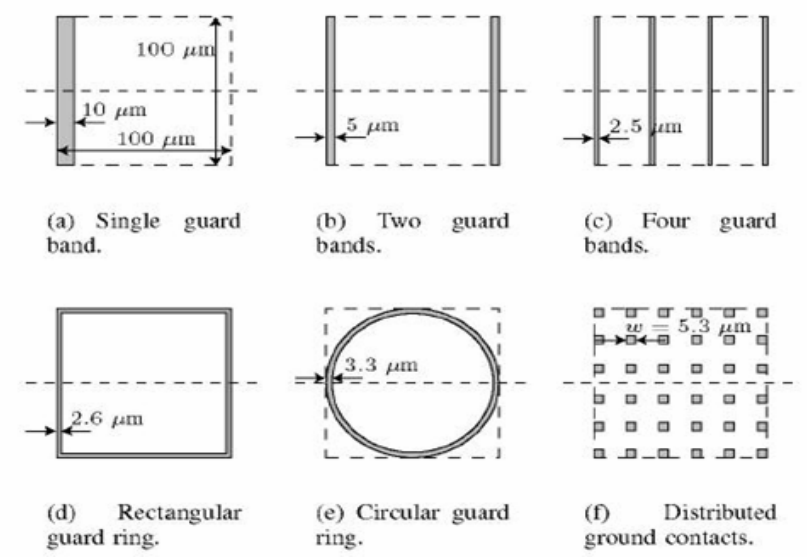
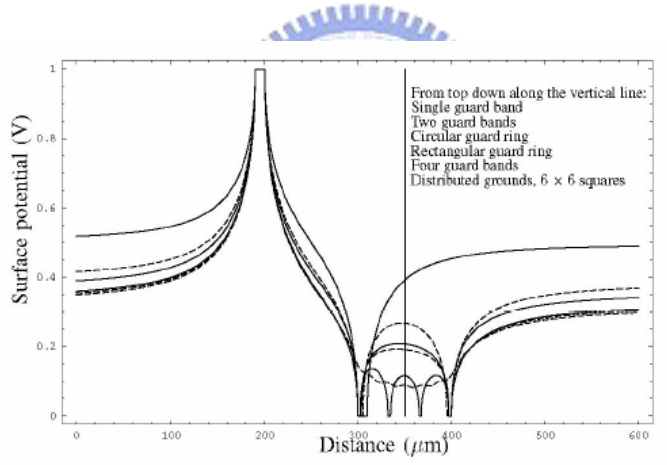
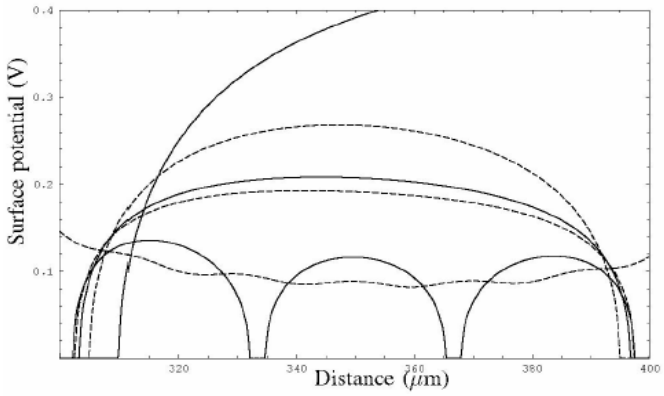


Figure 15 Schematic layout of different grounding structure [11]



(a)



(b)

Figure 16 The surface potential along the center line through the aggressor ground structure (a) Surface potential illustrating the local and global effects of the ground structure (b) Magnification of the surface potentials inside the ground structure [11]

Two conclusions can be drawn from Fig. 15. First, it is better to distribute the grounded areas in order to reduce the total ground resistance shown in Fig 16. Second, the local surface potential is reduced by distributing the ground contacts. It is represented that its structure provides a similar ideal ground.

In [12], band connection employed in active cancellation circuits for effective reduction of digital substrate noise is proposed. Excess cancellation by those band connections is more effective for noise reduction in a guard ring than a cancellation by the two bands. The active cancellation circuit shown in Fig. 17 employs an amplifier with a relatively small finite gain. In order to reduce substrate noise into a guard ring, noise is detected at a detection band. A cancellation signal is generated by inverting and amplifying the detected noise. The noise in a guard ring is canceled out by the cancellation signal. For design of an active cancellation a circuit, a design guideline that noise at the center of a guard ring is made equal to zero have been proposed [12].

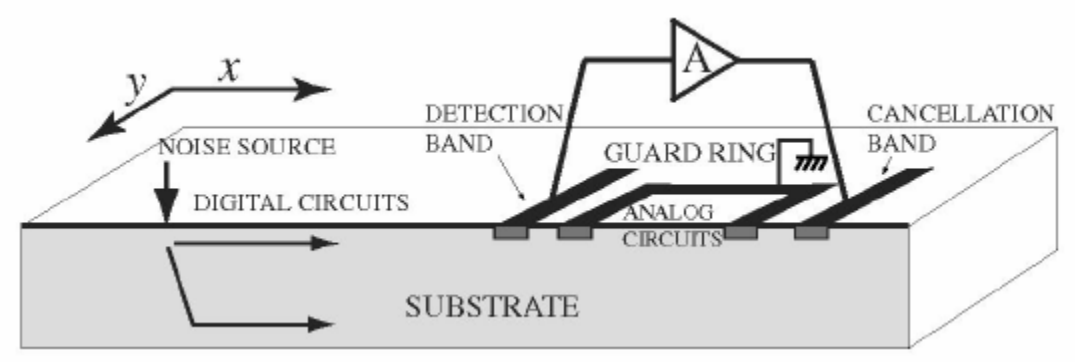


Figure 17 Active cancellation circuit [12]

Using an optimum gain in an active cancellation circuit, a simulation result of a noise characteristic on a surface of a substrate along the x-axis is illustrated in Fig 18 where the vertical axis shows the noise magnitude normalized with an input noise and a negative magnitude means an inverted noise is observed. The noise on a guard ring is zero since a guard ring is grounded.

Because of using inverting and amplifying, the noise is about zero at the center of a guard ring and fluctuates in the analog area. Thus the noise characteristic in a guard ring is approximately odd-symmetrical with respect to the center of a guard ring.

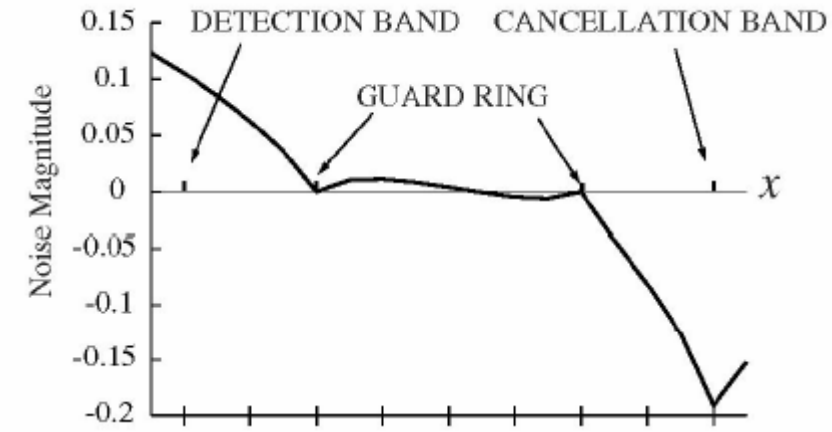


Figure 18 Noise characteristic on a substrate surface in the conventional active cancellation circuit. [12]

Fig. 19 shows a layout of bands and band connection and a guard ring and corresponding noise characteristics. Since a noise between detection band and a guard ring is positive and that near a cancellation band is negative from the characteristic. A noise current gathering at the band placed between a detection band and a guard ring passed to another added band and does little below an analog portion. Thus propagating into analog circuits becomes smaller.

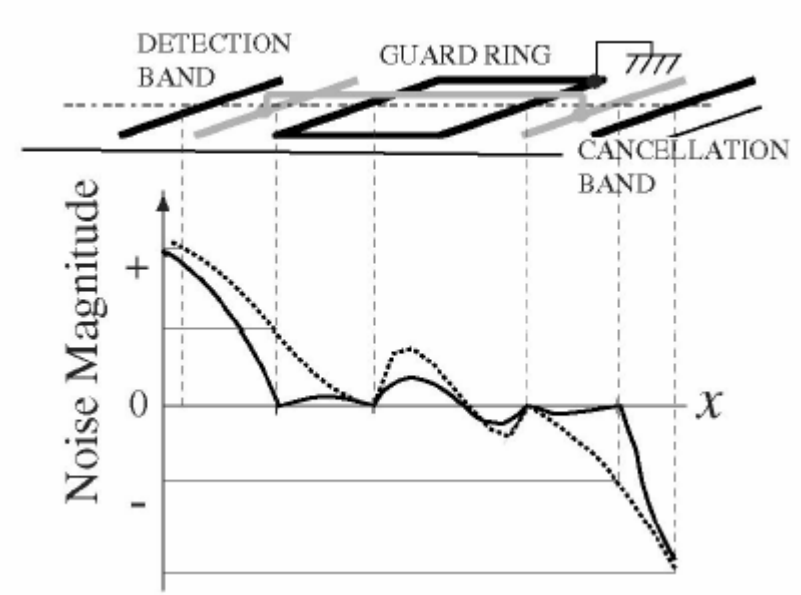


Figure 19 Noise characteristic when two bands are used [12]

1.2-2 Active circuit noise reduction methods

Passive methods may not be effective enough under noisy situation and may cause condition like latch-up and cause a large number bankroll. However active methods

have higher noise suppression level and compensate ability than physical methods.

The resonant forward-biased guard ring diodes for suppression of substrate noise are proposed in [13], seen in Fig.20.

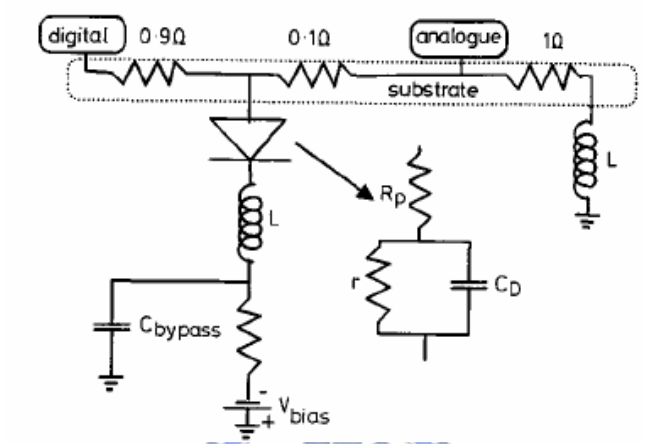


Figure 20 Model of coupling through substrate in a mixed-mode circuit showing guard-ring diode [13]

The paper has verified that by creating a band-pass filter, using the inductance of the bond wire and the capacitance of a forward biased diode, the substrate noise can be reduced [13]. In other words, the resonance creates a very low impedance path to ground that suppresses the substrate noise. The frequency of the filter is adjusted by changing the current through the diode and its capacitance. These components form a band-pass filter, the resonant-frequency of which depends on diode current and is given by ：

$$w_o = \frac{1}{\sqrt{L.t\,.I / 25\Omega}} \tag{1.3}$$

Where L is inductance of the bound wire, τ is the transit time and I is diode current. Fig.21 shows substrate noise voltage in two different circuits of with forward-biased guard-ring and circuit without forward-biased guard-ring.

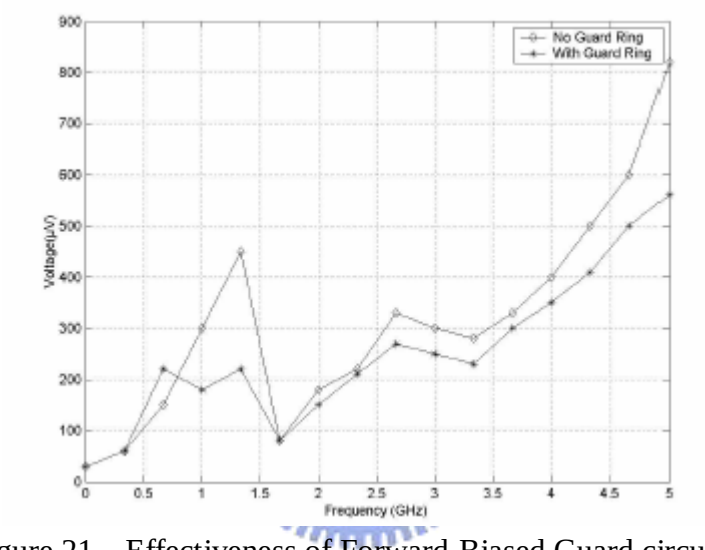


Figure 21 Effectiveness of Forward-Biased Guard circuit [13]

In [14], this study is based on linear feedback loop theory. Consider a typical mixed-signal design composed of an analogue portion and a digital portion. The digital portion of the circuit consists of m different noise sources, and the analogue portion of the circuit consists of n different noise receivers. Let S denote the noise source set and N denote the set of noise receivers. At any given time r, the amount of noise received at the ith noise receiver r_i, can be calculated by $r_i(s) = \Sigma_{j=0}^{m} s_j(s) * H_j(s)$. If a negative feedback back loop is added to the system as Fig.22 shows and we

assume that the $H_i(s)$ are close enough to be replaced by a single $H(s)$, the noise r_i can be expressed as

$$r_i(s) = \Sigma_{j=0}^{m} \frac{s_j(s) * H(s)}{(1 + F(s)H(s))} \tag{1.4}$$

Where $H(s)$ is the transfer function of the substrate and $F(s)$ is the gain of the negative feedback loop. The noise to be measured form the noise sensor will be reduced to $1/(1+F(s)H(s))$ of the original noise value if a negative feedback loop with sufficient gain-band-width product can be implemented in the system.

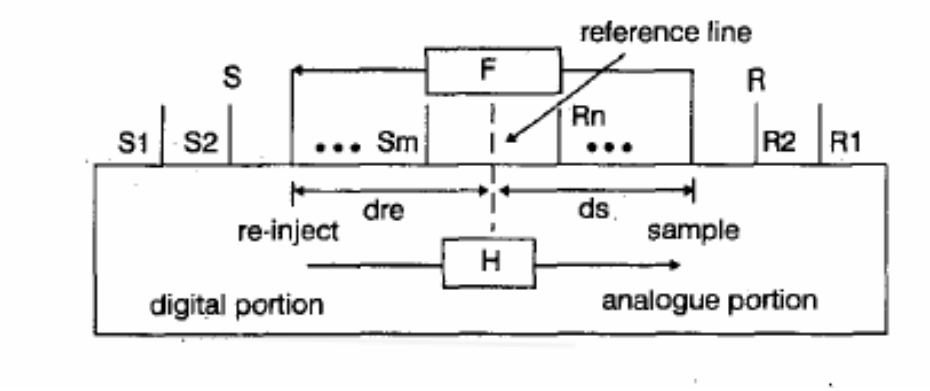


Figure 22 Linear system model for analyzing substrate coupling noise with feedback loop [14]

An active guard band filters to suppress substrate coupling noise has been introduced [15]. An active guard band filter creates a feedback loop using the substrate resistance as a feedback factor. It introduces an ac coupling configuration,

seen in Fig. 23. CB1 and CB2 were p+ guard bands or guard rings that were resistively coupled to the substrate. Capacitor C2 was inserted between GB1 and the input of the amplifier to detect the AC components of the substrate noise. Capacitor C1 was inserted between the output of the amplifier and GB2 to supply an AC noise cancellation signal.

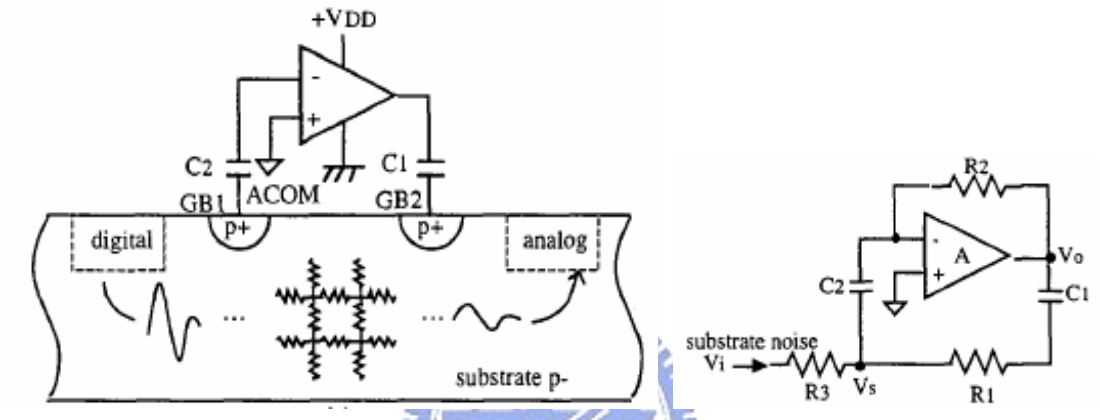


Figure 23 Ac coupling in the on-chip active guard band filter configuration and simplified circuit model [15]

The substrate was represented by resistance R1 and R3. Resistance R2 connected between the input and output node of the amplifier made the dc operating point stable. The noise suppression ratio could thus be estimated by using the ratio of Vs to Vi expressed by

$$\frac{V_s}{V_i} = \frac{(1+sC_1R_1)(1+A+sC_2R_2)}{\left\{1+s(C_1R_1+C_1R_3+C_2R_3)+s^2C_1C_2R_3(R_1+R_2)\right\}A}$$

$$= \frac{(1 - s/z_1)(1 - s/z_2)(1 + A)}{(1 - s/p_1)(1 - s/p_2)A} \tag{1.5}$$

Since R_1 and R_3 were almost equal, the zero and pole frequencies are expressed as $w_{z1} = \frac{1}{C_1 R_1}, w_{z2} = \frac{1+A}{C_2 R_2}$ and $w_p = \frac{1}{\sqrt{C_1 C_2 R_1 (R_1 + R_2)}}$. Since R_1 and R_3 are smaller than R_2, w_{z1} is always larger than w_p. However, if A is sufficiently large, the substrate noise can be suppressed to $\frac{1}{A}$ above w_{z1} to the amplifier open-loop gain bandwidth w_A.

It is found that the conventional AC coupling technique will require large coupling capacitances which will disable an on-chip implementation of the circuit. In this paper [16], an active guard band circuit based on a signal cancellation using its opposite signal is shown in Fig.24. Since the substrate resistances are symmetrical, the transfer function from node s to nodes g and d will be

$$\frac{v_g}{v_s} = \frac{v_d}{v_s} = \frac{v_s + v_c}{2}$$

$$= \frac{v_s - v_s}{2} = 0$$

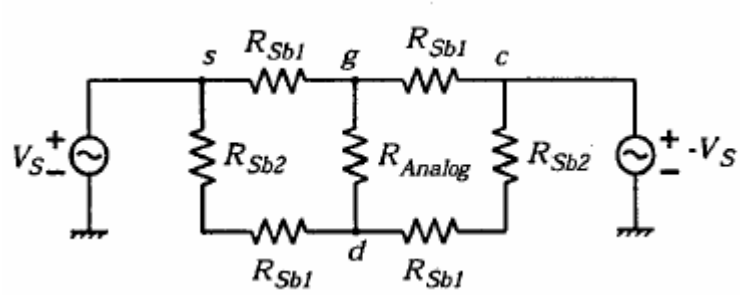


Figure 24 Basic of active noise guard band cancellation technique [19]

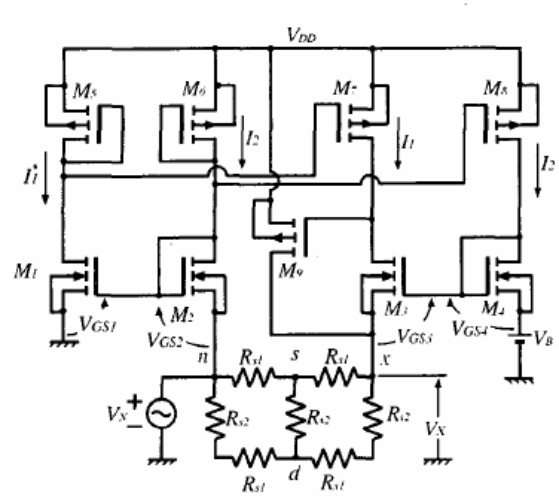


Figure 25 Active guard band circuit using DC coupling technique [16]

A basic circuit is shown in Fig. 25. Firstly, assume that a noise source V_N, which causes voltage fluctuation of substrate level, is detected at node n. Let the drain current of transistors M_6 and M_2 be I_2.At this time, when the drain current of M_1 is I_1 and M_5, M_6, M_7, M_8 have equal aspect ratios, then both drain currents of M_3 and M_4 will be equal to I_1 and I_2,respectively. Thus their gate-source voltages will be equal to V_{GS1} and $V_{GS2,}$ respectively. Here the relation between gate-source voltages of transistors M_1 and M_2 is given by Equ.12 and the relation between V_{GS3} and V_{GS4} can be expressed as Equ.13.

$$V_{GS1} = V_{GS2} + V_N \tag{1.6}$$

$$V_X + V_{GS3} = V_B + V_{GS4} \tag{1.7}$$

Because $V_{GS3}=V_{GS1}$ and $V_{GS4}=V_{GS2}$.Eq.13 can be written into

$$V_X + V_{GS1} = V_B + V_{GS2} \tag{1.8}$$

Substituting (1.6) into (1.8) gives

$$V_X + V_{GS1} = V_B + V_{GS1} - V_N \tag{1.9}$$

$$V_X = V_B - V_N \tag{1.10}$$

and

$$V_S = V_D = \frac{V_B}{2} = \frac{V_N + V_X}{2} \tag{1.11}$$

Since V_B is a constant voltage reference, negative V_N will appear at the output node V_X. This means that the substrate noise can be suppressed.

For active method, active decoupling circuit [17] is proposed by using decoupling capacitor to suppress substrate noise. Its capacitance, C, is multiplied by the gain, A (w), through the Miller effect. Its active decoupling compared with conventional capacitor decoupling shows in Fig.26. The decoupling effect in terms of the noise level with and without decoupling is shown in Fig.27.

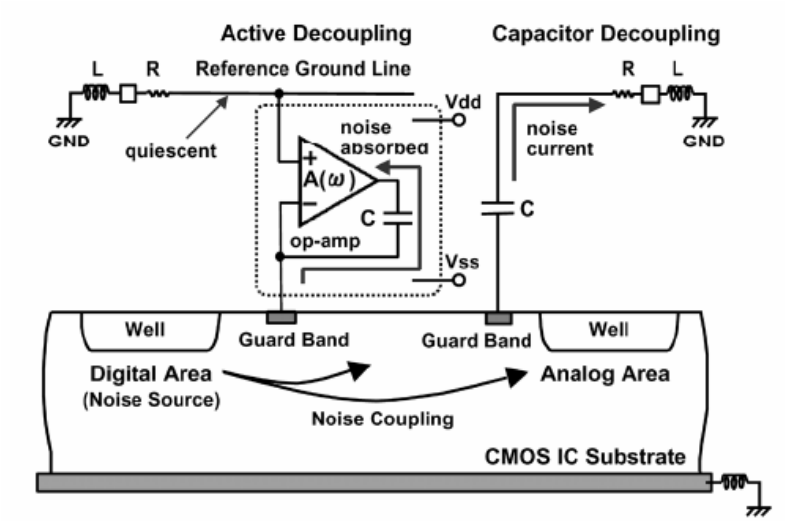


Figure 26 Content of on-chip active decoupling and capacitor decoupling [17]

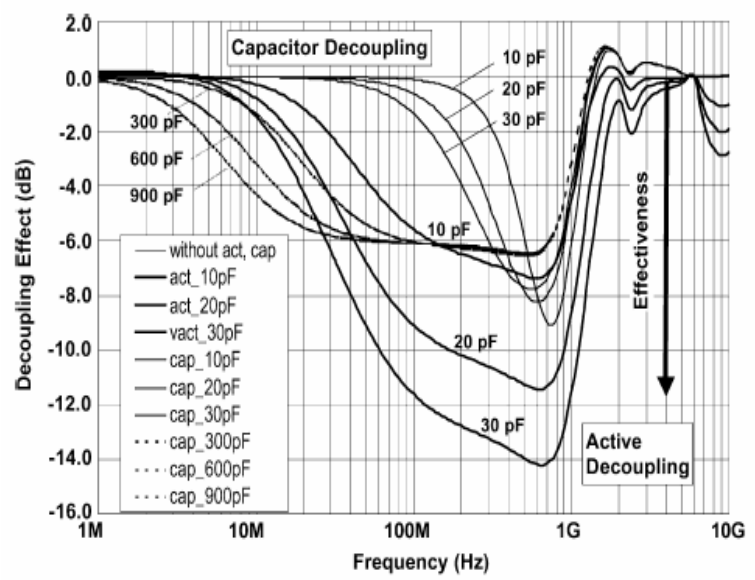


Figure 27 Simulated decoupling effect [17]

In [18], this study demonstrates a feed-forward active substrate noise canceling technique using a power supply di/dt detector. Since the substrate is tied to the ground line, the substrate noise is closely related to the ground bounce which is caused by di/dt when inductance is dominant on the ground line impedance. This active canceling technique detects the di/dt of the power supply current and injects an

anti-phase signal into the substrate so that the di/dt proportional substrate noise is cancelled out. A block diagram of the feed-forward active substrate noise canceling system is shown in Fig. 28. The ground noise is caused by the power supply di/dt and L_{gnd}. Since the substrate noise is proportional to the di/dt, the di/dt detector inverted output has anti-phase against the substrate noise. If the anti-phase signal is injected into the substrate, it can cancel the original substrate noise.

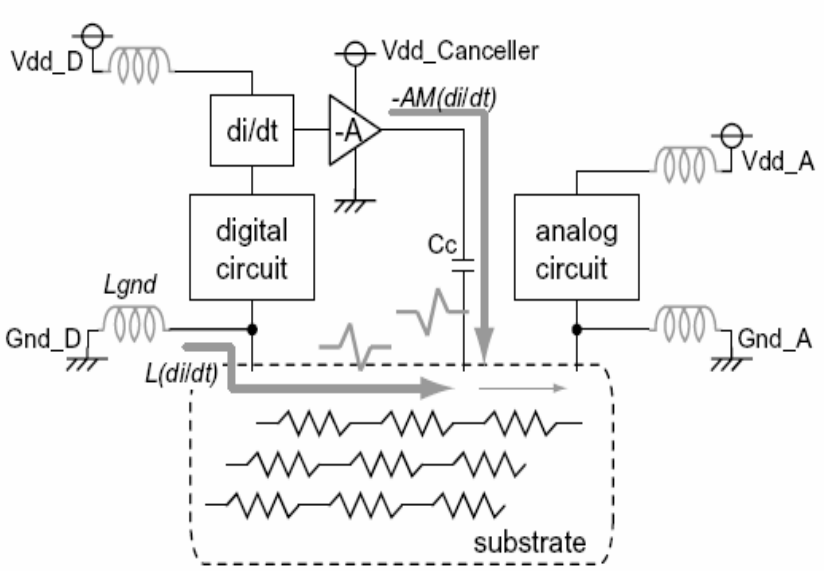


Figure 28 Structure of feed-forward active substrate noise cancellation [18]

1.2-3 Summary

Over the past few years, many literatures have been devoted to the study of substrate noise for sources of digital noise, the propagation path to the sensitive analog/RF portions, the modeling of the substrate, the amount of noise coupling, as

well as suppressing substrate noise methods. Here this dissertation focuses on substrate noise suppression. Many techniques have been investigated to alleviate this problem for suppressing substrate noise as shown in appendix. Among them, either passive or active method is used. For the passive method, different guard ring types are proposed [3], [5-12]. For the active method, feed-back [14], feed-forward [5-19], [20] and also [17] are proposed.

Among those techniques, passive methods [3], [5-10] may not be effective enough under noisy situations and may require either special substrate materials or extra implant/mask processing, which increase cost and process cycle time. In [10], it will increase latch-up risk in the real application and is not effective in higher frequency. In [11], these predictive physical researches are valuable reference materials for circuit designers implementing protection structures for reducing substrate noise. Other research [12] provides an idea using physical method for enhancing ability of active guard band circuit and total suppression ability for substrate noise suppression. Nevertheless such bands located between a guard ring and a cancellation band make a load impedance of an amplifier in an active band. As a result, a problem of increasing an output current of the amplifier arises.

On the other hand, although active methods have higher noise suppression level, there are several limitations and drawbacks still. For example, in [15], [16], and [19]

and [20], the frequency response and the delay of the amplifier restricts the bandwidth of the noise being cancelled, so that the noise reduction ratio is not enough for practical applications and the effective noise suppression bandwidth is only about 100MHz. In [21], although a high noise suppression bandwidth as 400MHz is achieved by employing a high bandwidth SIGE HBT amplifier, the hetero-junction bipolar technology is not suitable for the SOC design. In [18], the higher noise suppression bandwidth as 600MHz is achieved by using power supply di/dt detector, however, the di/dt device needs mutual inductor to detector. Therefore, this method needs large area. Finally, in [17] an active decoupling circuit is designed for a wide operation frequency from 40MHz to 1GHz, but it requires a power-consuming high gain amplifier and also an area-consuming on-chip capacitor as large as 10-30pF to obtain a noise suppression level of 6-14dB at most. The summary table of active methods is shown in Table.3. Because these methods based on different substrate situation, the isolation ability can't be compared.

Reference	Technique	Bandwidth	Isolation	Power	Area
[21]	0.8um	10M-400M	-12 ~ -3dB	13.5mW	
[16]	0.6um	1M-100M	-13 ~ -11dB	>3mW	Only MOS
[18]	0.35um	100M-600M	-1.6 ~ -3.8dB	>3.3mW	>238500um^2
[17]	0.13um	40M-1G	-6dB (max) -14dB (max)	9.9mW	>10000um^2 >30000um^2

Table 3 Summary table of active methods

1.3 Motivation

In terms of physical level method, its drawback are increasing processing costs and area and not effective for high frequency. Furthermore existing circuits are designed for low frequency and does not perform well for wide operation frequency to reach Giga-Hertz. At present these active circuits require large power and area.

Accordingly, the thesis proposes a new substrate noise suppression circuit with active guarding technique that employs noise decoupling and inversion feedback to reduce and suppress the substrate coupling noise. This circuit needs only a few active devices (PMOS and NMOS), and no capacitors or inductors are needed. Therefore, with proper design, the area required for this active guarding circuit can be very small, and the power consumption is very small.

1.4 Organization

The organization of this thesis is overviewed as follows. Chapter 2 describes active guarding technique of noise decoupling and inversion feedback and how to design the noise suppression circuit. The circuit design and optimization will be described in the same chapter. Chapter 3 shows the implementation and performance results and measurement. Chapter 4 concludes with a summary of contributions and suggestions for future work.

Chapter 2

Active Guarding Circuit Design and Optimization

2.1 Active Guarding Technique

The proposed active guarding technique is shown in Fig.29. The noise source is assumed to be a distance away and its current flows through both the surface and the deep portion of the substrate to the sensitive analog circuit. The active guarding circuit is in different well from the sensitive analog circuit. In addition, the substrate model is both resistive and capacitive for high frequency characteristics.

The proposed active guarding circuit composed of noise decoupling and inversion feedback is inserted by two contact rings between the noise source and the sensitive analog circuit. These two contact-rings named sense and feedback are applied to perform noise decoupling and inversion feedback. The noise current flowing through the sense ring is sensed and averaged then decoupled to the active guarding circuit. After that, the active guarding circuit re-injects an amplitude-controlled phase-inversed noise current into the substrate to cancel the substrate noise. Therefore,

with the proposed active guarding circuit, only little noise current and only a few transistors can reach better performance for the guarded analog circuit and the area is small.

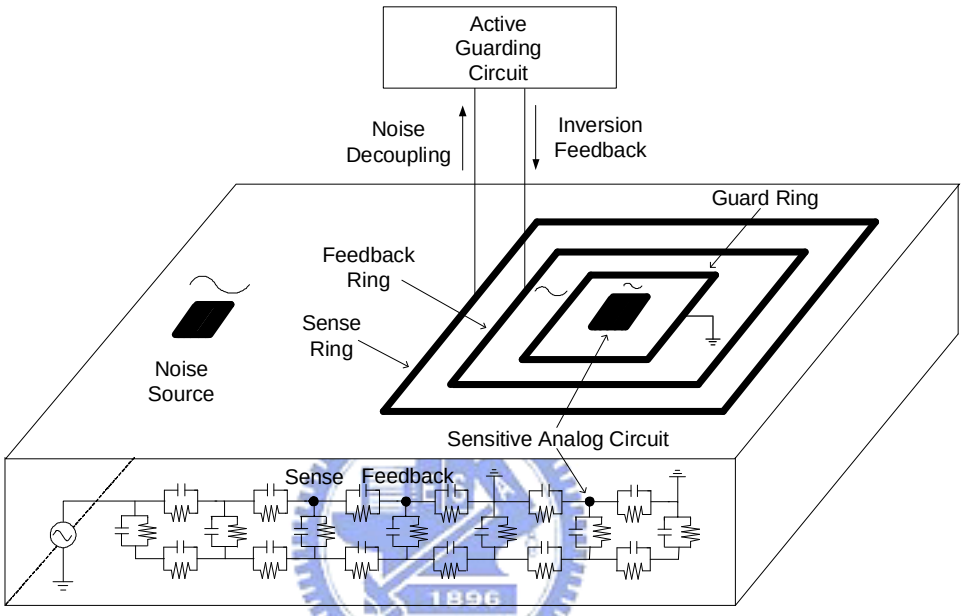


Figure 29 The proposed active guarding technique

2.1-1 Noise Decoupling

As shown in Fig. 30(a), for the noise current that flows through the substrate to the sensitive analog circuit, a low impedance path is created for noise decoupling. The noise current is drained away to the noise decoupling path of the active guarding circuit. Therefore, the effective noise current that flows toward the sensitive analog circuit is reduced. In Fig.30 (a), assume the noise current that flows into the input

node is I_{in}, the input impedance of the proposed circuit is Z_{in_ckt}, and the equivalent impedance of the substrate network at the circuit input node is Z_{in_sub}.

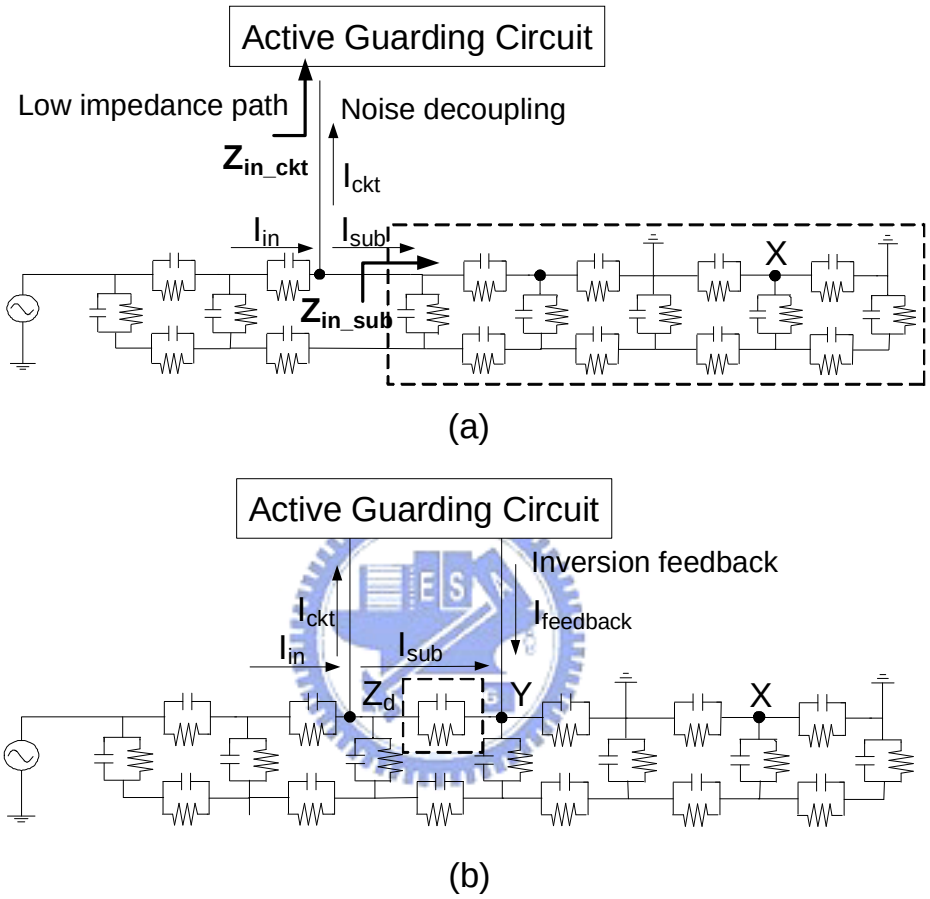


Figure 30 Concepts of active guarding technique
(a) Noise decoupling, (b) Inversion feedback

By applying the low impedance path of Z_{in_ckt} on the substrate network, the original noise current is separated into two parts, I_{ckt} and I_{sub}, which are expressed as

$$I_{ckt} = \left(\frac{Z_{in\_sub}}{Z_{in\_ckt} + Z_{in\_sub}} \right) \times I_{in} \qquad (2.1)$$

$$I_{sub} = \left(\frac{Z_{in\_ckt}}{Z_{in\_ckt} + Z_{in\_sub}} \right) \times I_{in} \qquad (2.2)$$

where I_{ckt} presents the current that being drained away by the active guarding circuit while I_{sub} presents the noise current that flows to the analog circuit. Since the effective noise current that flows toward the sensitive analog circuit is lowered by a fraction of $Z_{in\_ckt}/(Z_{in\_ckt} + Z_{in\_sub})$, the noise level at the concerned node X is effectively reduced.

Furthermore, under a given substrate model, Z_{in_sub} is considered as a known parameter. Therefore, the only design parameter in equation (2.1) and (2.2) is Z_{in_ckt}, the input impedance of the proposed circuit. The smaller the Z_{in_ckt} is, the more noise current will be drained away from the substrate and the smaller noise level will affect the analog circuit to be protected. However, in actual circuit implementation using MOS transistors Z_{in_ckt} cannot be arbitrarily small. The smaller Z_{in_ckt} is, the larger the MOS transistor size is required, leading higher power consumption. The design example of proper transistor size will be discussed in later section.

2.1-2 Inversion Feedback

Assume the Z_d in Fig. 30(b) is very small which can be realized in layout level (i.e. to set the sense and feedback ring very close). Most of the noise current I_{sub} will flow to

the feedback node rather than to the deep portion of substrate and then to the node X. The simplified inversion feedback mechanism of the active guarding circuit is depicted in Fig. 31.

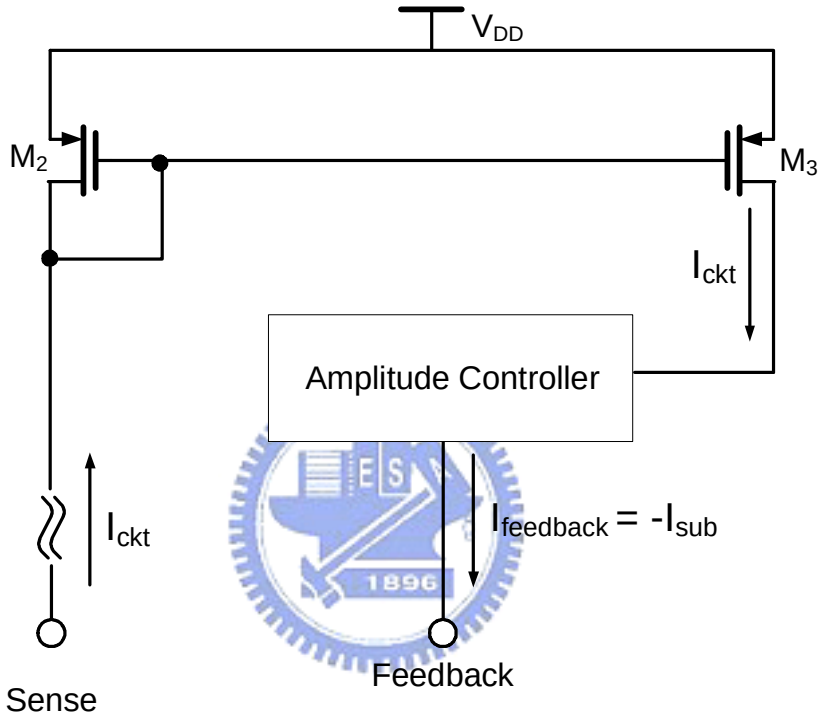


Figure 31 Inversion feedback mechanism

In order to inverse the phase of the noise current sensed from the circuit input, a current mirror is applied. The phase-inversed noise current is sent to an amplitude controller to keep the magnitude of the feedback current the same as I_{sub}. Finally, the magnitude-matched and phase-inversed feedback current is re-injected to the substrate to cancel the substrate noise current at the feedback node Y.

To design the amplitude controller, the current gain AC(s) of the controller can be

determined using following equation

$$I_{ckt} \times A_C(s) = I_{sub}$$
$$\Rightarrow A_C(s) = \frac{I_{sub}}{I_{ckt}} = \frac{Z_{in\_ckt}}{Z_{in\_sub}} \quad (2.3)$$

However, high frequency inversion feedback performance is limited by the bandwidth of the current mirror and the amplitude controller. When noise frequencies are higher than the designed bandwidth, the losses and phase shifts will degrade the noise suppression performance.

2.2 Circuit Design and Optimization

Fig. 32 shows the schematic of the proposed active guarding circuit. The input common-gate transistor M_1 creates a low impedance path for the sense node and the impedance value is $1/g_{m1}$. Unlike other designs [21] that use the common source configuration as the input stage to sense the substrate noise voltage from gate, M_1 not only senses the noise current but also drains it away leading to lower noise level for cancellation in the later stage.

To drain most of the noise current, the input impedance, $1/g_{m1}$ should be designed

as small as possible. However, smaller $1/g_{m1}$, indicates larger transistor size $(W/L)_1$, which consumes large area and power. To determine the proper size of M_1, the noise suppression improvement per milli-Watt power consumption as the numbers of the width increment of M_1 from 40μm is studied.

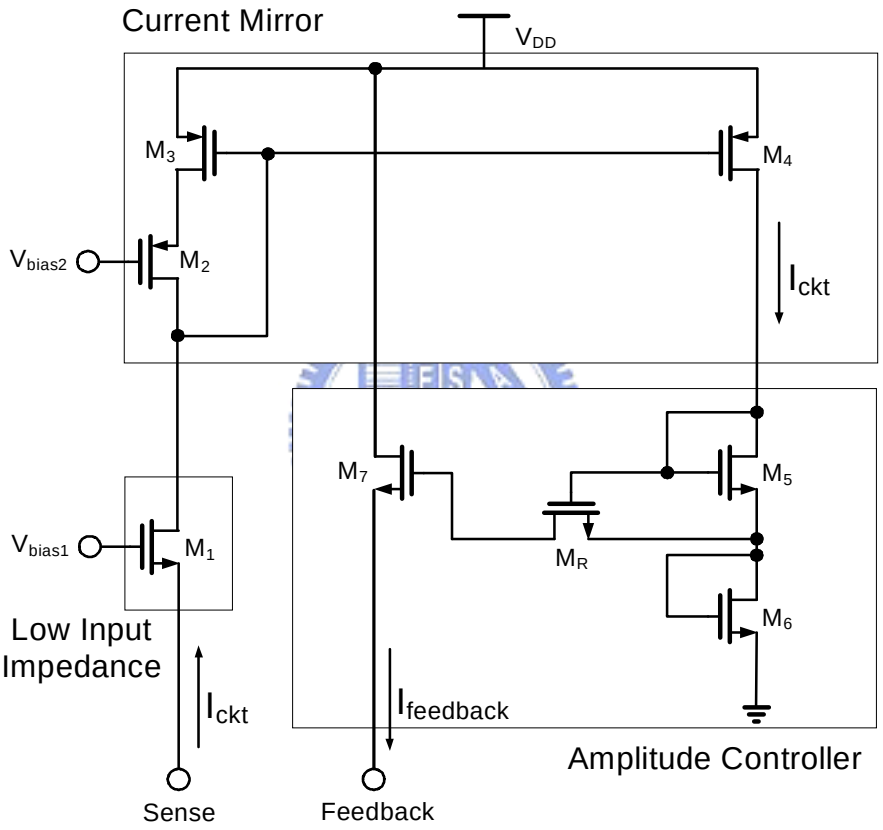


Figure 32 Proposed Active Guarding Circuit

Figure.33 shows almost no further improvement of noise suppression is achieved after the M_1 width exceeds 400μm when the noise frequency is 1GHz. The 7^{th} increment of MOS width, i.e. 320μm is chose as the width of M_1, since the improvement is less than 1dB/mW for width larger than 320μm.

To realize the inversion feedback mechanism, transistor M_2~M_7 and MR are added to construct the current mirror and the amplitude controller.

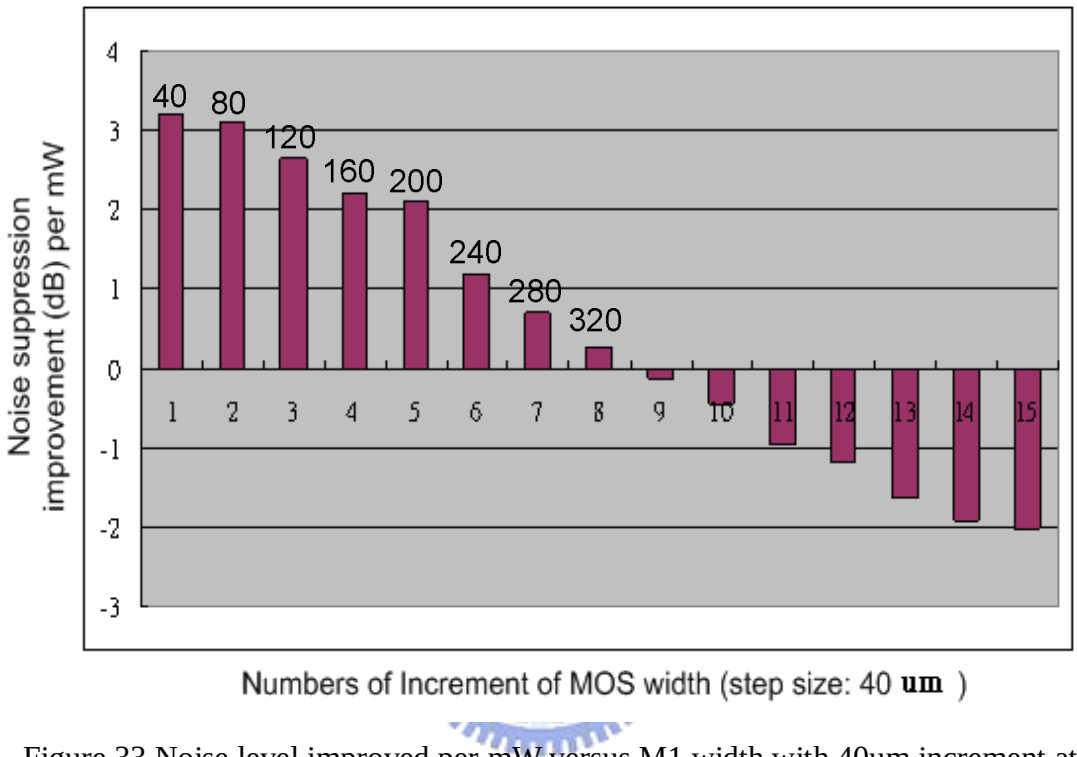


Figure 33 Noise level improved per mW versus M1 width with 40um increment at 1GHz

M_4 copies and reverses the phase of the noise current I_{ckt}. The phase-inversed current is sent to the amplitude controller composed of M_5~M_7 and M_R. The current is converted to voltage via diode-connected M_5 and M_6. The transconductance stage M_7 adjusts the current gain and converts the voltage back to current to re-inject the current into the substrate.

2.2-1 Bandwidth Extension

To improve the noise suppression at high frequencies, a zero is introduced by inserting a triode-region transistor M_R to extend the effective bandwidth of the active guarding circuit. Introducing of M_R creates a zero and a pole [22] which can be expressed as

$$Z_R = -\frac{g_{m_6}}{g_{m_5} + g_{m_6}} \times \frac{1}{RC_{gdR}}, \qquad P_R = -\frac{1}{RC_{gdR}} \tag{2.4}$$

where R presents the resistance value of M_R and C_{gdR} is the parasitic capacitance of M_R.

Moreover, the bandwidth of the active guard circuit can be extended by designing the zero Z_R to be closed to the dominant pole P_D of the circuit without M_R. The bandwidth is extended until P_R becomes to affect the frequency response. The dominant pole P_D of the circuit without M_R can be approximated as

$$P_D \cong -\frac{1}{R_X (C_X \parallel C_P)} \tag{2.5}$$

where $R_X = r_{o4} \parallel [1/g_{m_5} + 1/g_{m_6}]$, r_{o4} is the output resistance of M_4. $C_X = C_5 + [C_6 \parallel (C_{gs7} + C_{sub}) \parallel C_{gd7}]$, C_5 and C_6 are the parasitic capacitance of M_5 and M_6, and C_{sub} is the equivalent capacitance of substrate seen from the source of M_7.

$C_P = C_{gd4} + (C_{gs4} \| C_{gs3} \| C_{gd1} \| C_{gd2})$.

2.2-2 Amplitude Controller

Fig. 34 shows the equivalent circuit of the amplitude controller. Transistor M_5 and M_6 are modeled as resistor $1/g_{m5}$, $1/g_{m6}$ with their parasitic capacitance C_5, C_6. MR is modeled as a resistor R with its gate-drain parasitic capacitance C_{gdR} and gate-source parasitic capacitance C_{gsR}. And M_7 is a simply transconductance stage.

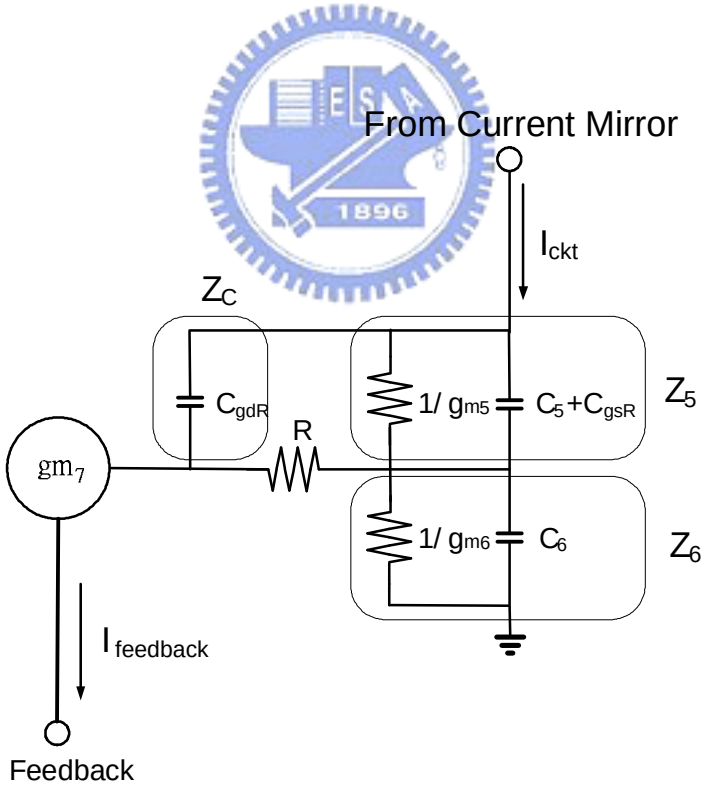


Figure 34 Equivalent circuit of the amplitude controller

Equation (2.6) shows the transfer function of $I_{feedback} / I_{ckt}$. The small-signal current

gain $A_C(s)$ of the amplitude control circuit can be designed using following equations

$$A_C(s) = \frac{I_{feedback}}{I_{ckt}} = \left(\frac{RZ_5}{R + Z_5 + Z_C} + Z_6 \right) \times g_{m_7} \tag{2.6}$$

For low frequency current gain, i.e. $A_C(0)$ can be obtained

$$A_C(0) = \frac{I_{feedback}}{I_{ckt}} = \frac{g_{m_7}}{g_{m_6}} \tag{2.7}$$

Refer to equation (2.3) and (2.7), the current gain can be determined as shown in (2.8).

$$A_C(0) = \frac{I_{sub}}{I_{ckt}} = \frac{1/g_{m_1}}{R_{in\_sub}} = \frac{I_{feedback}}{I_{ckt}} = \frac{g_{m_7}}{g_{m_6}} \tag{2.8}$$

As a result, for a given R_{in_sub} and $1/g_{m1}$, the ratio of g_{m7}/g_{m6} is designed to match the current of $I_{feedback}$ and I_{sub}.

Chapter 3

Implementations and Layout

3.1 Simulation Setup

In order to simulate circuit performance in substrate, a substrate model must to be established. UMC provided 130nm substrate noise isolation p+ to p+ characterization and simple structure report and is shown in Fig 35[23]. Therefore, the substrate model used in the dissertation is built by simulating the model structure shown in Fig 37 (a) to fit the p+ guard ring characteristic in Fig 36.

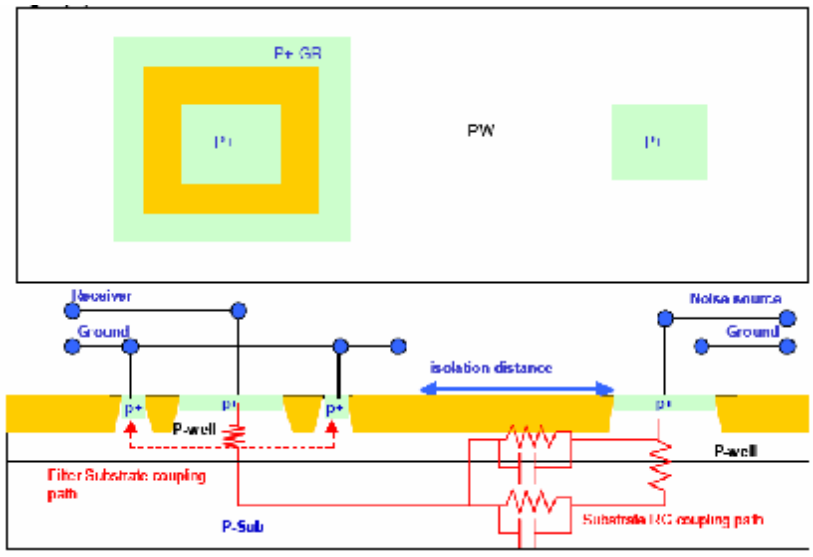


Figure 35 Schematics of the reference p+ guard ring, schemes used in the substrate noise characterization [23].

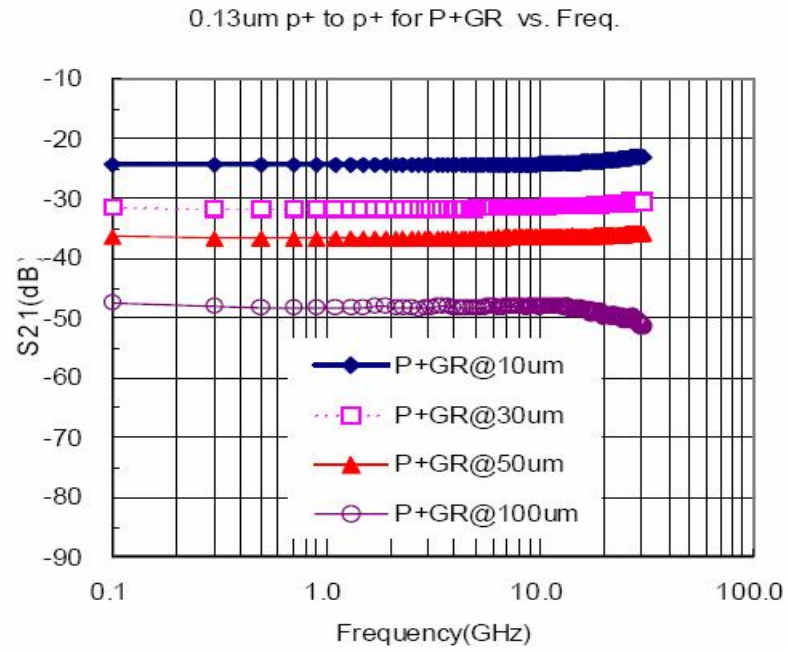
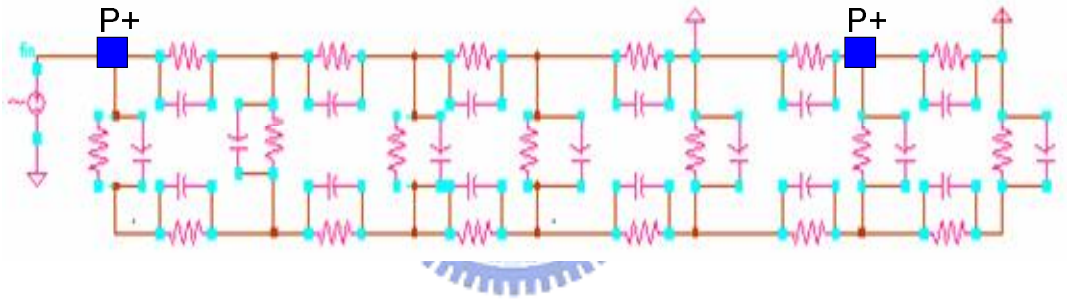
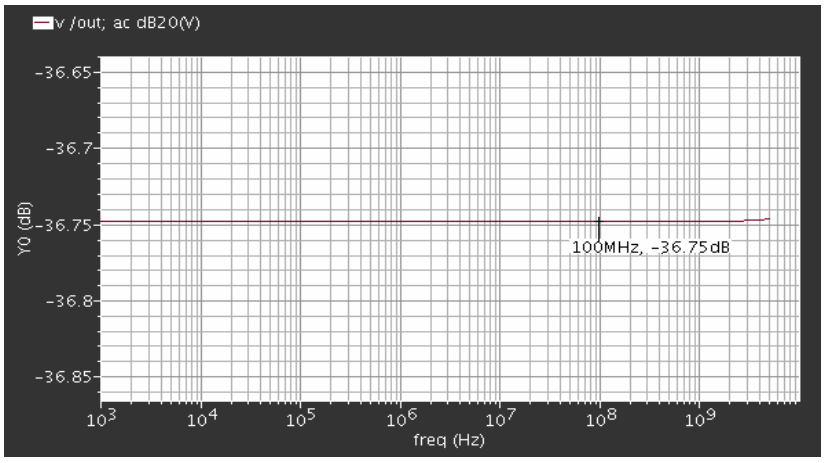


Figure 36 Isolation performance of P+GR schemes vs. frequency for different isolation distance [23].



(a)



(b)

Figure 37 (a) Substrate model structure and (b) Simulation result

To demonstrate the performance of the proposed active guarding circuit, we

compare substrate noise suppression of the circuit (Sample A) and the passive guard ring (Sample B), and the simulation setup is shown in Fig.38. Therefore, when circuit is switched on and off, the simulation results can be compared to show the isolation result provided by active guarding circuit.

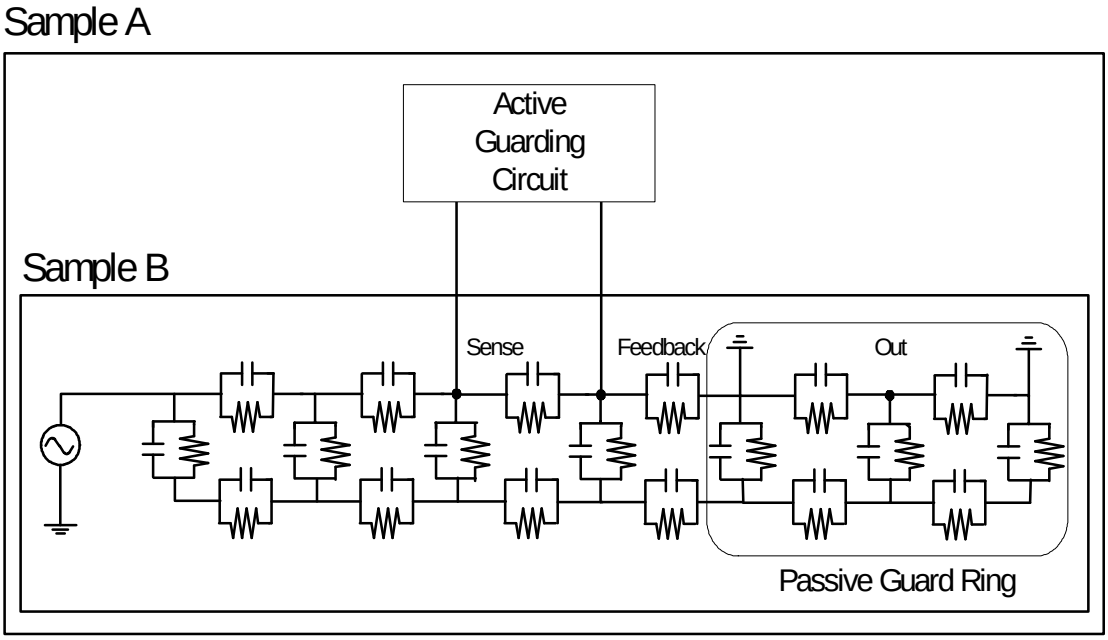


Figure 38 Simulation setup of the proposed active guarding circuit

3.2 Measurement Environment

In order to measure active guarding performance, the noise source contact connects to ESG signal generator and receiver connects to spectrum analyzer. Using one tone signal and showing output in the spectrum analyzer to measure the circuit performance with the guarding circuit switched on or off. Fig.39 shows measurement

setup.

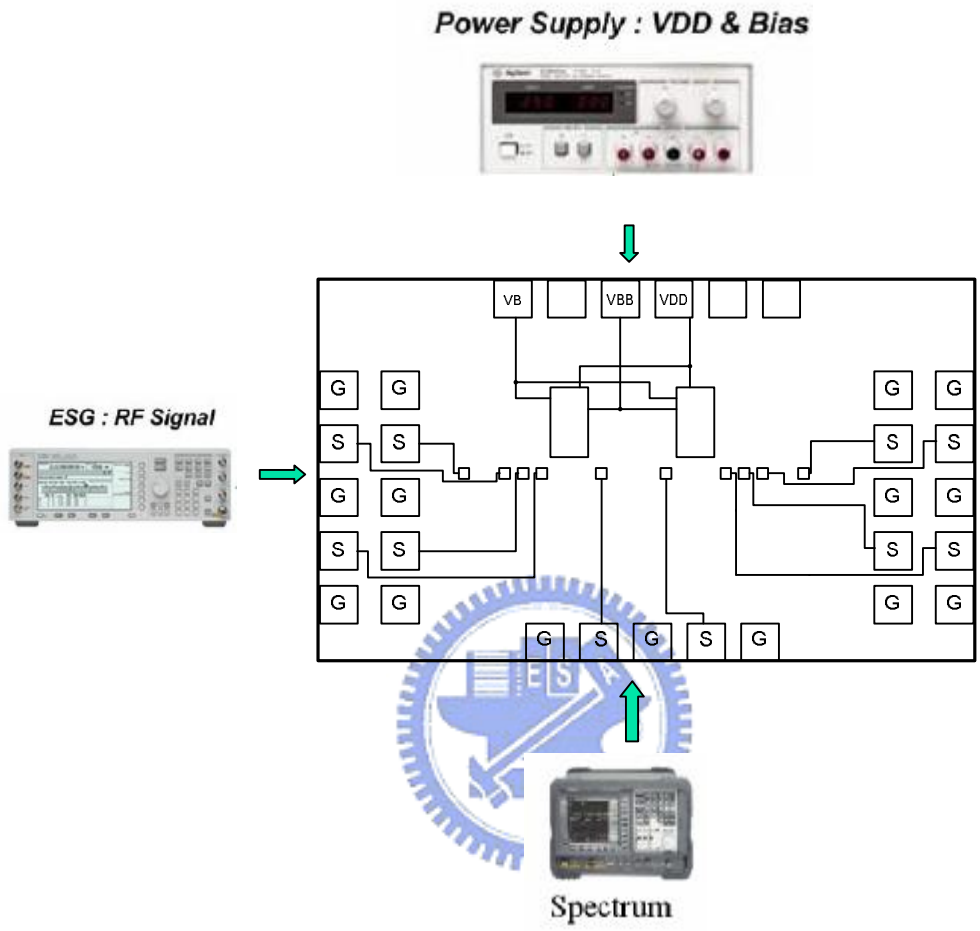


Figure 39 Measurement setup

3.3 Implementation and simulation results

3.3-1 First implementation

Two implementations were done. The former includes an extra capacitor as shown in Fig 40. Due to the extra capacitor, this circuit performs different from the circuit

discussed in previous chapter. The capacitor would shift the introducing pole to low frequency location and decrease performance. The circuit layout is shown in Fig 41. Five different distances from the noise source to the guarding circuit are considered to measure the substrate suppression capacity in Fig.42. C_0 serves as the receive contact and C_1~C_5 serve as the noise source inputs. The simulation of DUT1 is shown in Fig 42. The circle symbol (•) of trace indicates isolation of guard ring and the pulse symbol (+) of trace indicates the improved performance of the active guarding ckt compared with guard ring. The measurement results are shown in Fig.43.

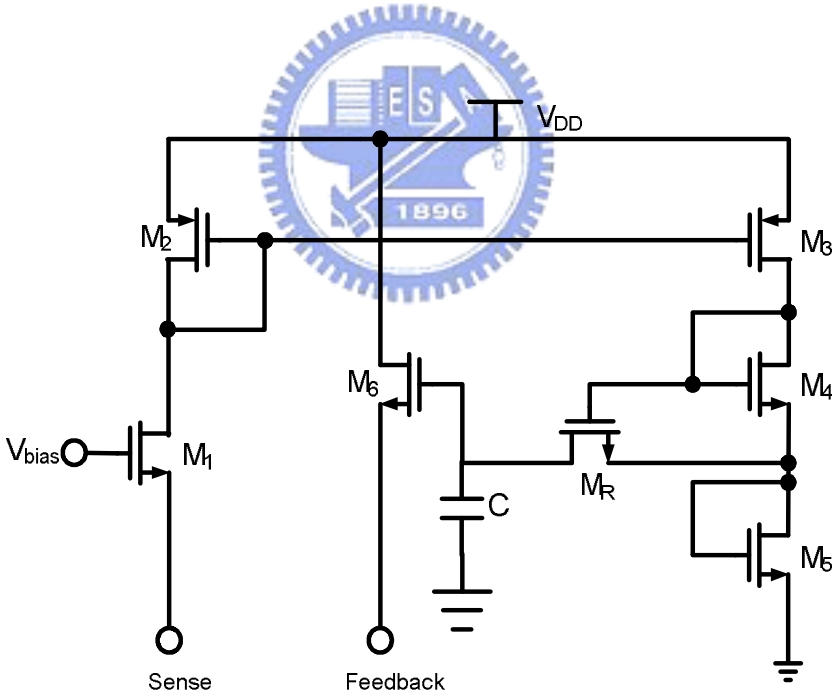


Figure 40 Previous Active Guarding Circuit

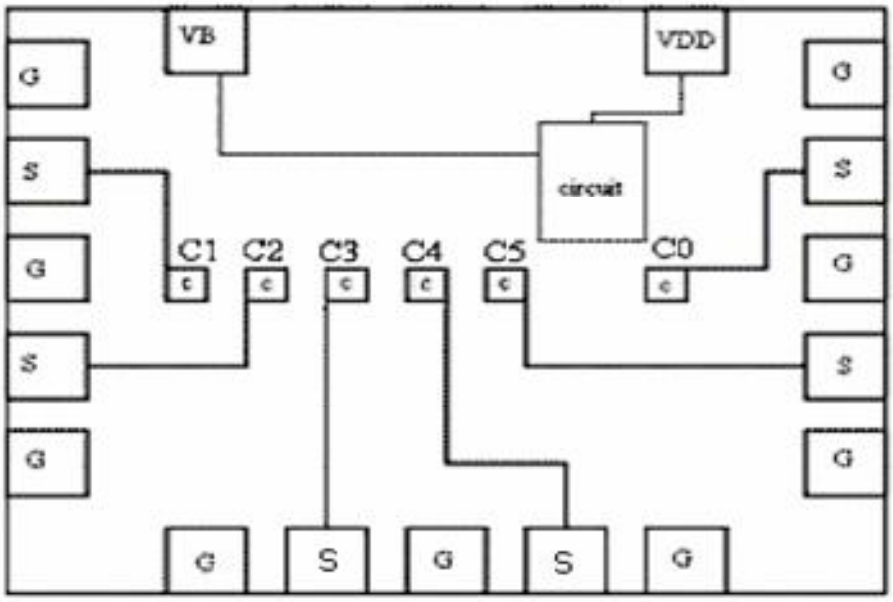


Figure 41 Previous circuit layout placement

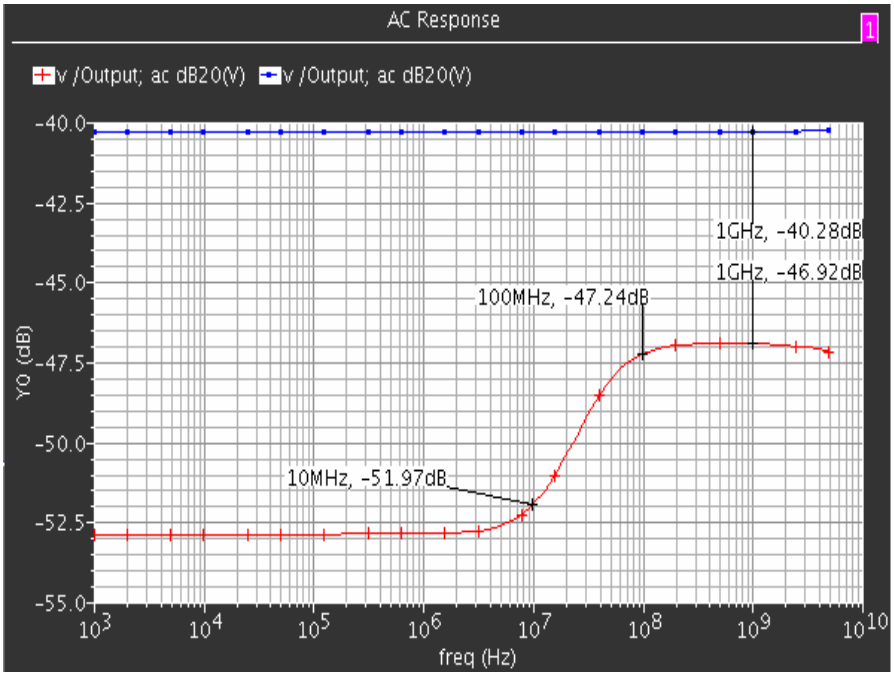


Figure 42 Previous circuit simulation result

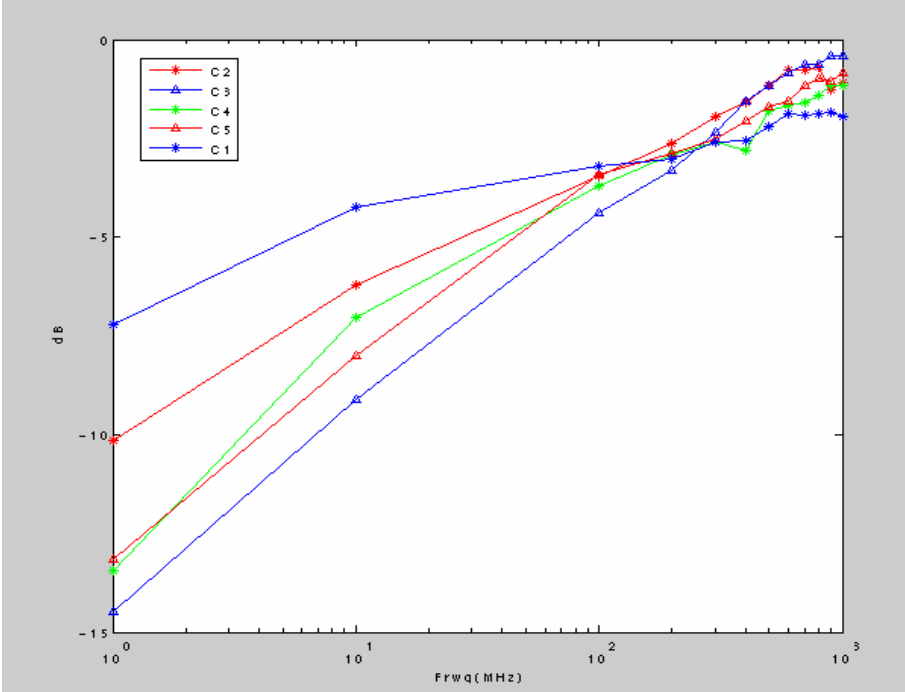


Figure 43 Previous circuit measurement result data arrangement

From Fig.43, it shows that the measurement and simulation results are not matched. The mismatch may due to inaccurate substrate model, improper substrate model resistance and capacitor values, circuit layout or circuit bias. Observe the circuit layout, a 0.28 um wide VDD line in transistor M_7 shown in Fig.44, because 0.28um VDD line would not tolerate more than 1mA current. Open VDD line is simulated to verify. The cross symbols of trace indicate the VDD line cut off in Fig.45. Fig.45 show in higher frequency trajectory is similar to measurement data result. But in low frequency two trajectories of simulation and measurement data are similar. The mismatch in lower frequency may due to ac couple below 20MHz in the spectrum analyzer. Therefore, in the second implementation, the spectrum must be adjust dc couple and add dc block to receive low frequency couple and circuit provides a

suitable VDD line for the second measurementation.

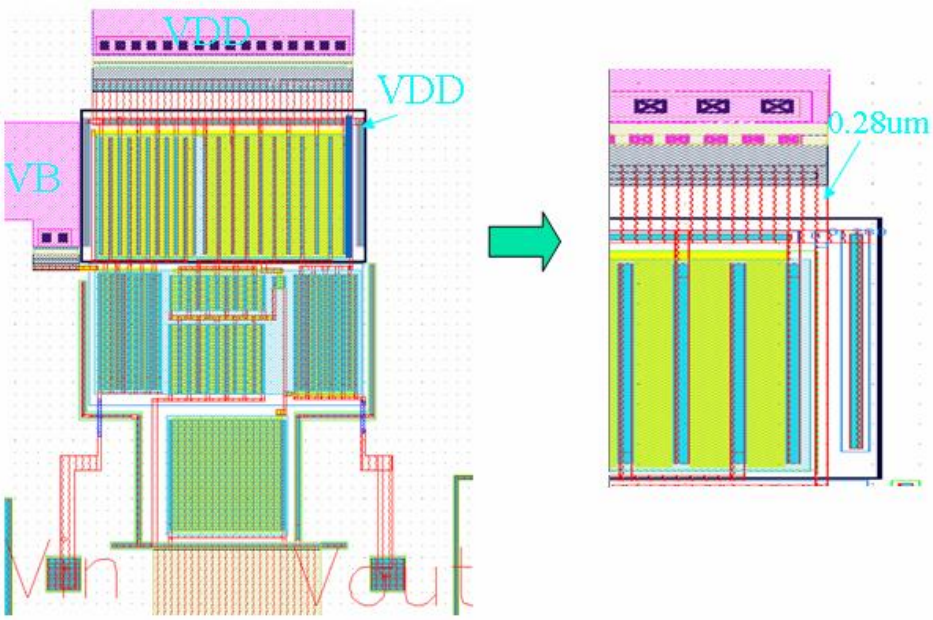


Figure 44 The layout of small VDD line width

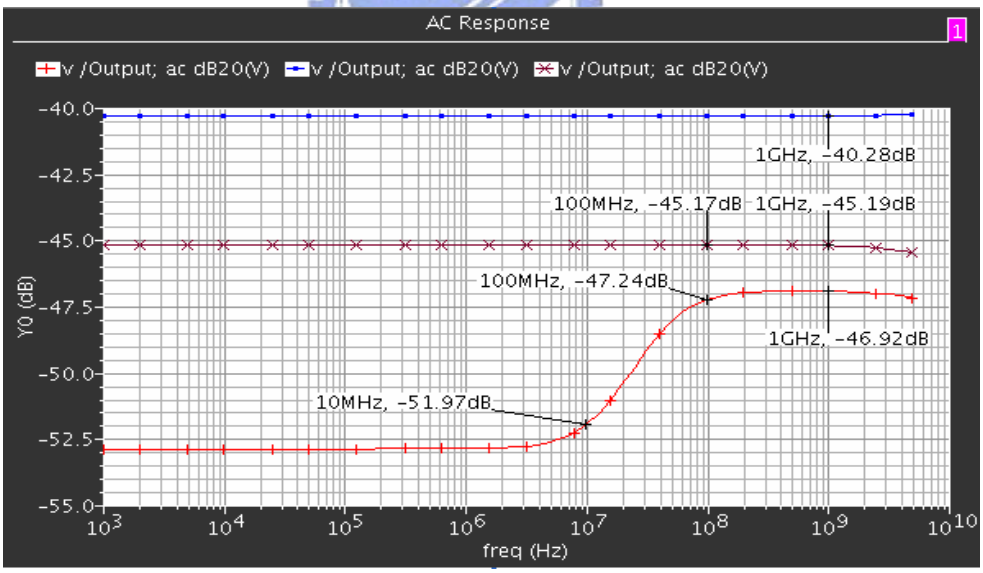


Figure 45 Simulation result

3.3-2 Second implementation

Fig.46 shows the noise suppression level of both the passive guard ring and the active guarding circuit with passive guard ring. The cross symbol of trace indicates the isolation when the active guarding circuit turned off. And thus other trace indicates the isolation when it turned on. The result shows that more than 14dB improvement of noise suppression is achieved by the active guarding circuit compared with guard ring in the frequency range from DC to 1GHz. The total power consumption is about 2.86mW

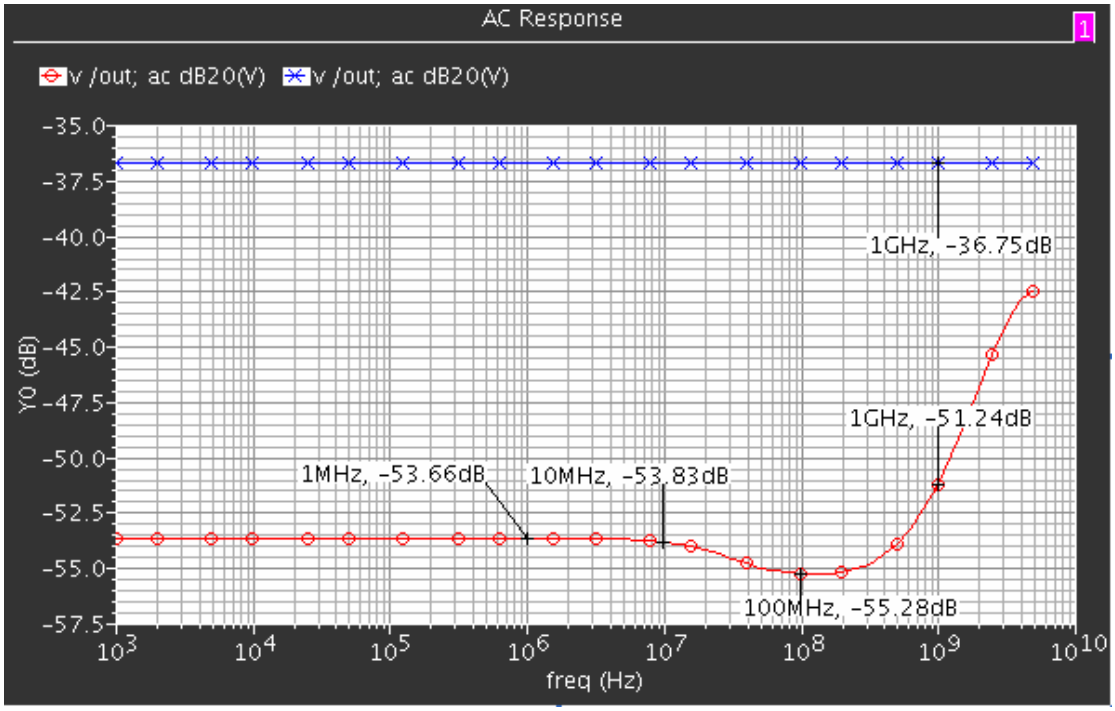


Figure 46 Simulation results of noise suppression versus frequency for both passive guard ring and the active guarding circuit

The circuit layout of active guarding circuit is shown in Fig.47 and circuit layout area is only 1386 um^2. The total layout area is 1.32 mm^2 shown in Fig.48. The total layout placement use four input source nodes and one receiver node which use bigger

p+ contact. The areas of noise source and receiver p+ contact region are both 7.4 x 13 um^2 which is referred to 0.13 um UMC Logic 1P8M Process Substrate NOISE Isolation P+ to P+ Characterization Report. The isolation distances are varied from 15um to 100um. This placement is referred to the situation similar to 0.13 um UMC Substrate NOISE Isolation P+ to P+ Characterization Report all the same. This layout placement is shown in Fig.49 and two different receiver contacts with guard ring and without guard ring are applied, the comparison of pre- and post-layout simulation is shown in Fig.50. The plus and cross symbol of traces show the pre- and post- layout simulation of the active guarding circuit. And the comparison table is shown in Table.4. Fig 51 shows the noise suppression as the noise level at the sense node increases from 0.1mV to 100mV at 1GHz. The 1-dB degradation points of the noise suppression for 1GHz are about 88mV.

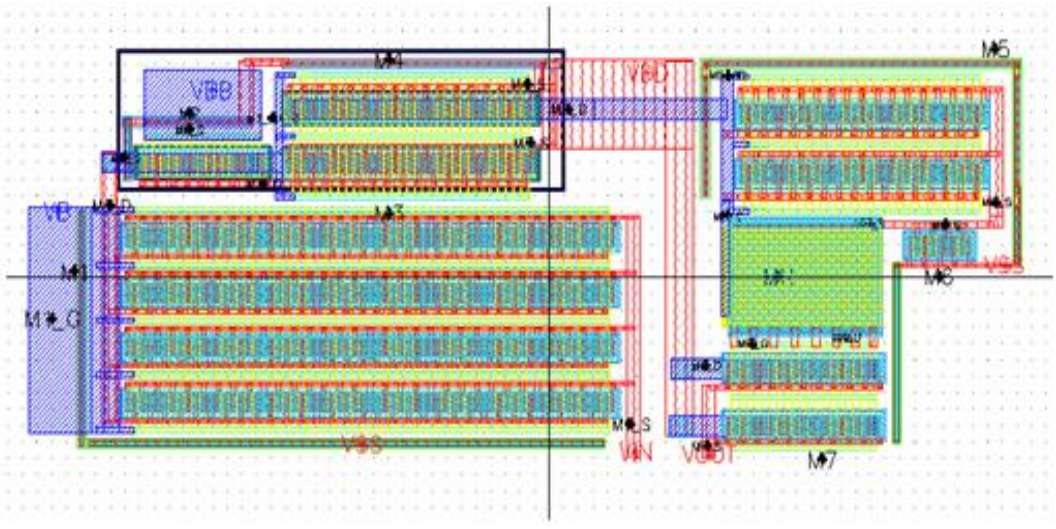


Figure 47 Layout of active guarding circuit

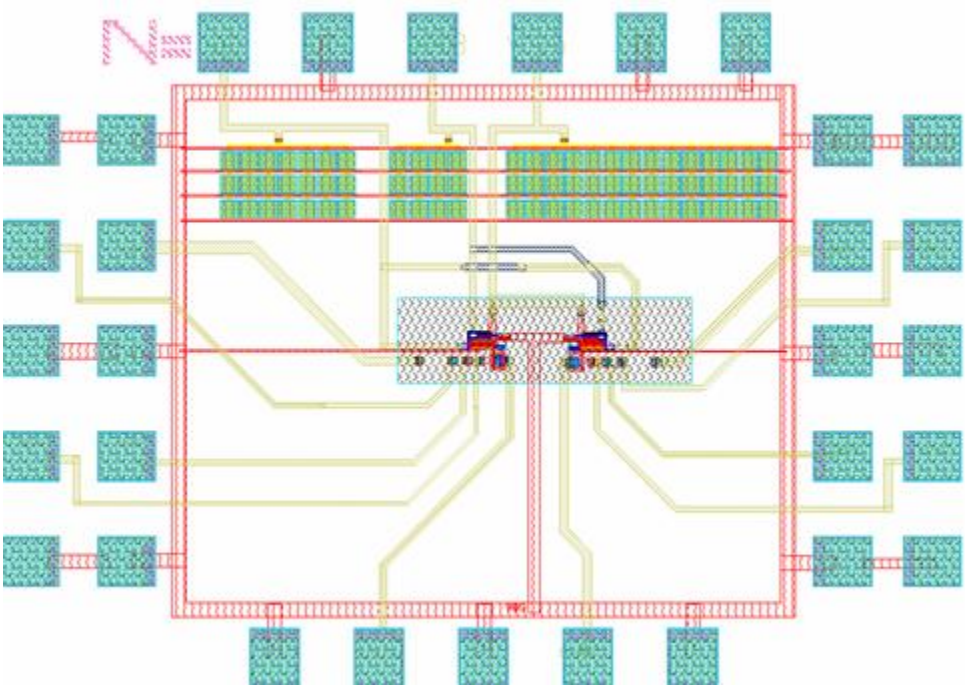


Figure 48 Total chip layout

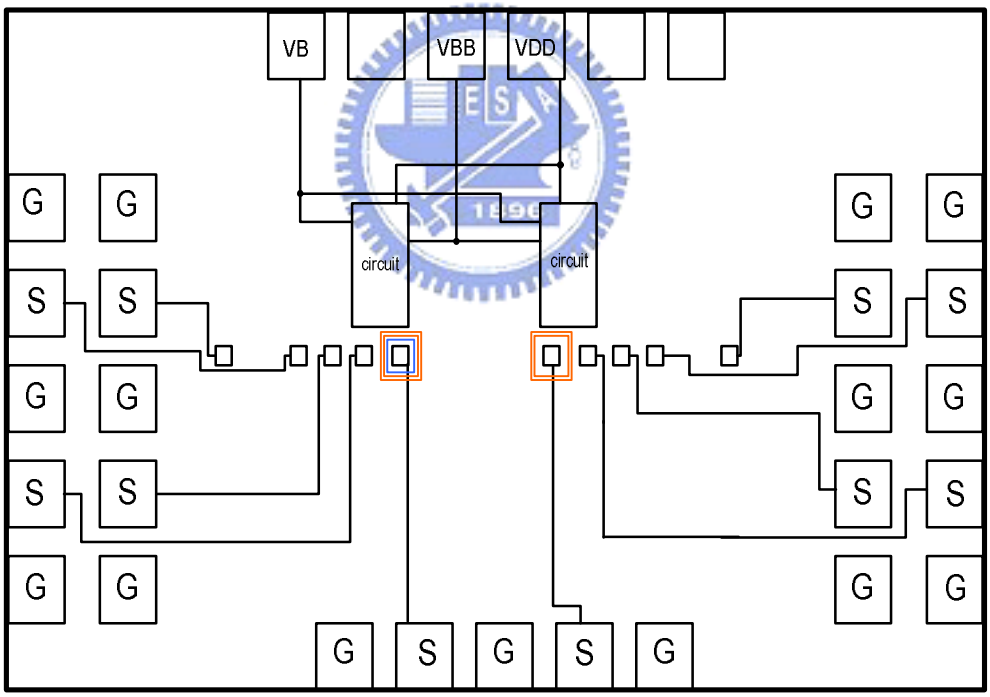


Figure 49 Layout Placement

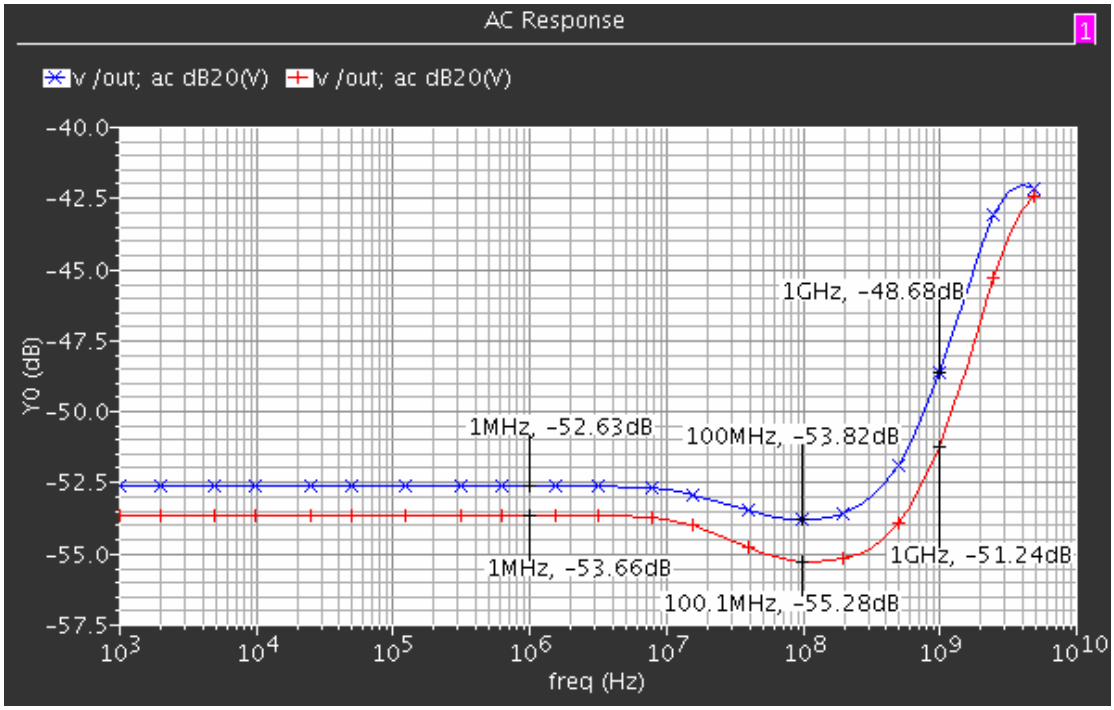


Figure 50 The comparison of pre-simulation and post-simulation

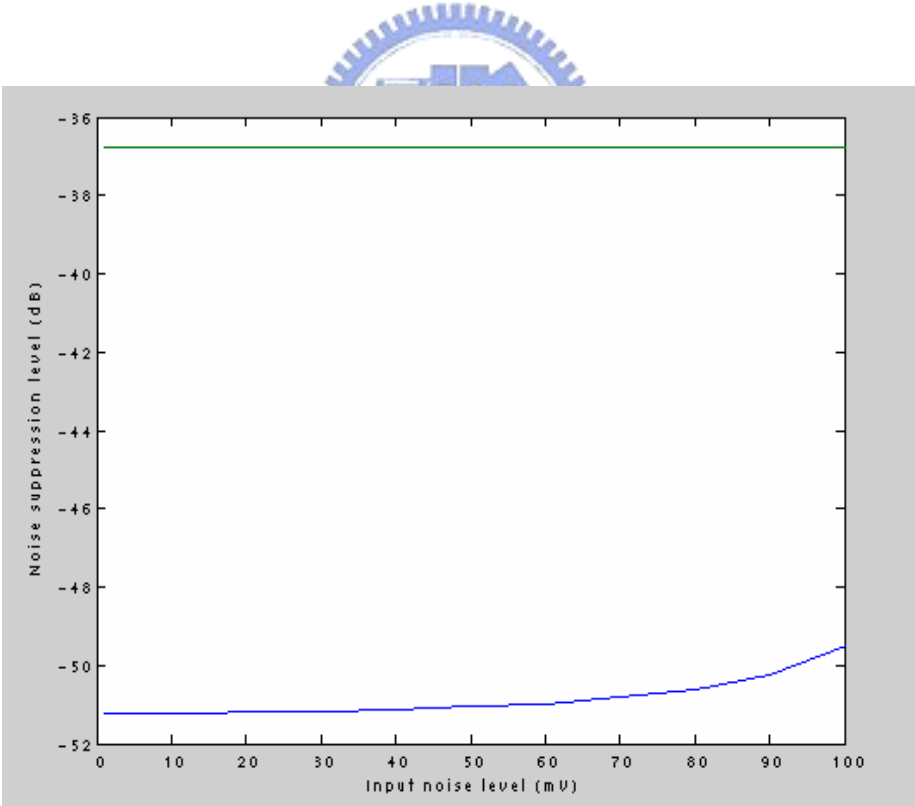


Figure 51 Noise suppression versus input noise level at 1GHz for both passive guard ring and the active guarding circuit.

	Technique	Bandwidth	Isolation	Power	Area
[21]	0.8um (SiGe)	10M - 400M	-20(max) ~ -3dB	13.5mW	
[16]	0.6um	DC - 100M	-13 ~ -11dB(sim)	>3mW	Only MOS
[18]	0.35um	100M-600M	-1.6~-3.8dB (measurement)	>3.3mW	238500um^2
[17]	0.13um	40M - 1G	-6dB (max)(sim) -14dB (max)(sim) -3.17dB(max) (measurment)	9.9mW	>10000um^2 (one capacitor) >30000um^2 (three capacitor)
Proposed work	**0.13um**	**DC - 1GHz**	**-15~-14dB(sim)**	**2.86mW**	**~ 1386um^2 (Only MOS)**

Table 4 Comparison table

Chapter 4

Conclusions and Future Work

4.1 Conclusions

An active guarding circuit for giga-hertz substrate noise suppression has been implemented in UMC 0.13 CMOS process. With the proposed active guarding circuit, substrate noise suppression of passive guard ring can be improved more than 14dB in the frequency range from DC to 1GHz. And Low power and small chip area is realized with the proposed active guarding circuit for substrate noise suppression. As a result, this active guarding circuit is suitable for noisy environment with high noise frequency up to GHz.

4.2 Future work

As for the future work, I will focus on the current mirror of active guarding circuit. As described in chapter 2, the current mirror pole would be settling down higher more than P_R frequency. The pole position will decrease performance for higher frequency suppression shown in circle symbol of Fig.52. Therefore, high frequency inversion feedback performance is limited by the bandwidth of the current mirror and the amplitude controller. This circuit can be improved from current mirror to achieve better performance in high frequency.

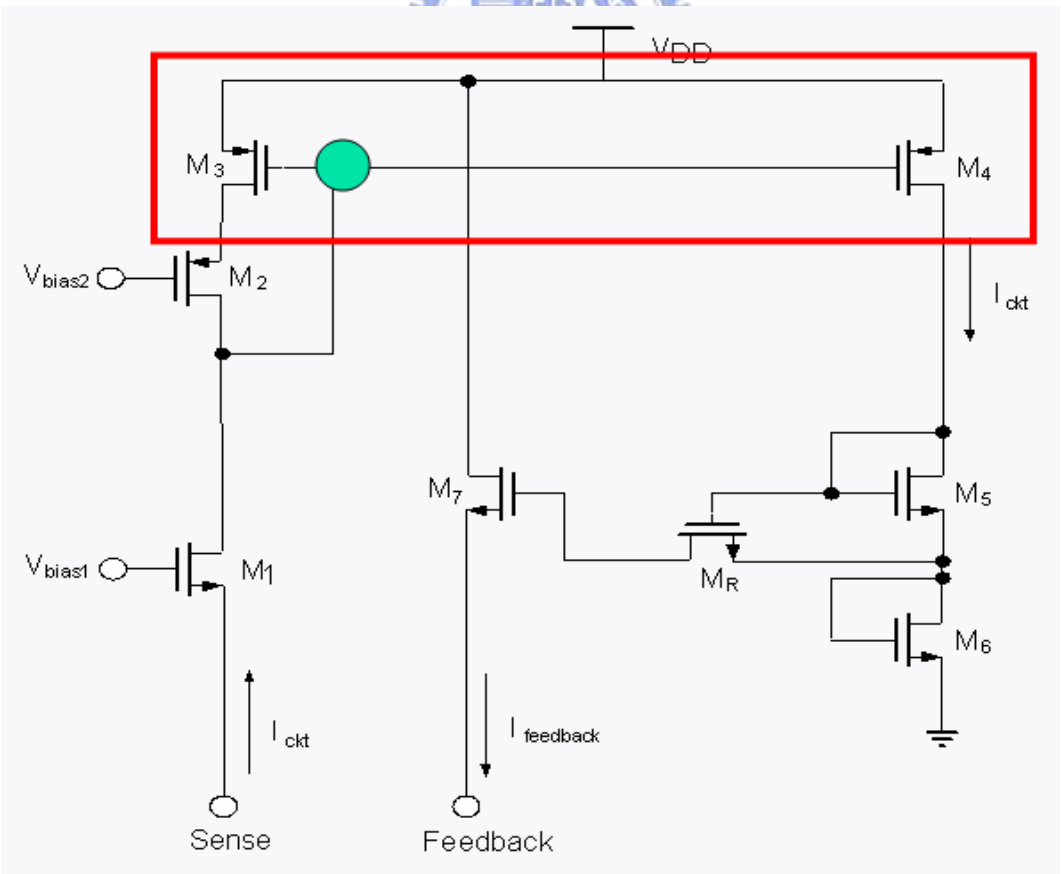


Figure 52 Current mirror pole

Bibliography

[1] M. van Heijningen, J. Compiet, P. Wambacq, S. Donnay, M.G.E. Engels, and I. Bolsens, "Analysis and experimental verification of digital substrate noise generation for epi-type substrates," IEEE J. Solid-State Circuits, vol. 35, pp. 1002-1008, 2000

[2] X. Aragones, J. L. Gonzalez, F. Moll and A. Rubio, Analysis and solutions for switching noise coupling in mixed-signal ICs, USA, 1997.

[3] E. Charbon et al.,"Substrate Noise Analysis and Optimization for IC Design," Kluwer Academic Publishers, 2001.

[4] Behzad, Razavi, Design of Analog CMOS Integrated Circuits International Edition 2001

[5] K. Joardar, "A simple approach to modeling cross-talk in integrated circuits," IEEE J. Solid-State Circuits, vol. 29, no. 10, pp. 1212-1219, Oct. 1994.

[6] P. Basedau, and Q. Huang, "A post processing method for reducing substrate coupling in mixed-signal integrated circuits," Symposium on VLSI Circuits '95, Digest of Technical Papers, 41, 1995.

[7] X. Aragones, et al., "Analysis and Solution for Switching Noise Coupling in Mixed-Signal ICs," Kluwer Academic Publishers, 1999.

[8] E. Charbon et al., "Substrate Noise Analysis and Optimization for IC Design," Kluwer Academic Publishers, 2001.

[9] K. Joardar, "Signal Isolation in BiCMOS Mixed Mode Integrated Circuits," IEEE Proc. of the Bipolar/BiCMOS Circuits and Technology Meeting, pp.178-181, 1995.

[10] Tsun-Lai Hsu Yu-Chia Chen Hua-Chou Tseng Liang, V. Jan, J.S, "psub guard ring design and modeling for the purpose of substrate noise isolation in the SOC era, " IEEE Electron device letters, vol. 26, no. 9, 2005

[11] Simon Kristiansson, Fredrik Ingvarson, and Kjell O. Jeppson, “Properties and Modeling of Ground Structures for Reducing Substrate Noise Coupling in ICs,” IEEE International Symposium on Circuits and Systems, 2006.

[12] Hiroto Suzuki, Kazuyuki Wada, and Yoshiaki Tadokoro, “Band connections in active cancellation circuits against digital substrate noise, ” ICCAS 2006

[13] L. Forbes et al., “Resonant Forward-biased Guard-ring Diodes for Suppression of Substrate Noise in Mixed-mode CMOS Circuits,” IEE Electronics Letters, vol. 31, pp. 720-721, Apr. 1995.

[14] T. Liu, J. D. Carothers, and W. T. Holman, “A negative feedback based substrate coupling noise reduction method,” in Proc. 12th Annu. ASIC/SOC Conf., 1999, pp. 49–53.

[15] K. Makie-Fukuda and T. Tsukada, “On-chip active guard band filters to suppress substrate-coupling noise in analog and digital mixed-signal integrated circuits,” in Symp. VLSI Circuits Dig. Tech. Papers, pp. 57–60, Jun. 1999.

[16] S. Takagi, R.A. Nicodimus, K. Wada, and N. Fujii, “Active guard band circuit for substrate noise suppression,” Proc. IEEE International Symp. on Circuit and Systems, vol.1, pp.548-551, May 2001.

[17] Toshiro Tsukada, Yasuyuki Hashimoto, Kohji Sakata, Hiroyuki Okada, Koichiro Ishibashi, “An On-Chip Active Decoupling Circuit to Suppress Crosstalk in Deep Sub-Micron CMOS Mixed- Signal SoCs,” IEEE Int. Solid-State Circuit Conf. Dig. Tech Papers, pp.160–161, Feb. 2004.

[18] Toru Nakura, Makoto Ikeda, Kunihiro Asada, “Feedforward Active Substrate Noise Cancelling Technique using Power Supply di/dt Detector,” in JSAP/IEEE Symposium on VLSI Circuits, pp.284–287, June 2005.

[19] N. R. Agung, S. Takagi, and N. Fuji, “Improving the immunity to substrate noise using active noise cancellation circuit in mixed-signal integrated circuits,” Proc. 2002 Asia-Pacific Conference on Circuits and Systems, vol.1, pp135-140, Oct. 2002.

[20] R. A. Nicodimus, S. Takagi, and K. Wada, “Active Shield Circuit for Digital

Noise Suppression in Mixed-Signal Integrated Circuits," *IEICE Trans. Fundamentals*, Vol. E88–A, pp. 438-443, Feb. 2005.

[21] W. Winkler, and F. Herzel, "Active Substrate Noise Suppression in Mixed-Signal Circuits Using On-Chip Driven Guard Rings," in *Proc. IEEE Custom Integrated Circuits Conf.*, May 2000, pp. 357-360.

[22] A. Rusznyak, "Filtering current mirror," *IEE Proc. Circuits, Devices and Systems*, vol. 149, no. 4, pp. 218-220, Aug. 2002.

[23] 0.13 um Logic 1P8M Process Substrate NOISE Isolation P+ to P+ Characterization Report for FAB8D form UMC.

Publication List

1. Hao-Ming Chao, **Chien-Lung Wang**, Wen-Shen Wuen, and Kuei-Ann Wen, "An Active Guarding Circuit for Giga-Hertz Substrate Noise Suppression," accepted by European Microwave Integrated Circuits Conference, April 2007

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論文題目 ： An Active Guarding Circuit for Giga-Hertz Substrate Noise Suppression

針對 Giga-Hertz 基底雜訊抑制的主動保護電路