Chapter 1 Introduction

1.1 overview of the ota

The transconductor is widely used in analog and mixed-signal systems. Based on the voltage-to-current converter, we can build the multiplier, the Gm-C filter, the voltage-controlled oscillator (VCO), and the continuous-time sigma delta modulator [1]-[4].

For rail-to-rail circuit, it means that the input common-mode voltage can be extended from one supply rail to the other rail [5]. The input common-mode voltage range of the traditional differential pair will be limited by the threshold voltage of MOS transistor. We should note that only an n-channel (p-channel) differential pair cannot process signals with low (high) common-mode voltage, and a solution is to combine n-channel and p-channel differential pairs in parallel. However, the overall transconductance will not be a constant in the whole rail-to-rail range of the complementary input stage. Fig. 1.1 shows the relationship of the input common-mode voltage with respect to the overall transconductance. As the common-mode voltage is low, the n-channel differential pair will turn on. On the other hand, as the common-mode voltage is high, the p-channel differential pair will work. When the input common-mode voltage is in the middle value, both the p-channel and n-channel differential pair will turn on, and the transconductance is

doubled. Thus, it is hard for the traditional complementary differential pairs to keep the total transconductance being a constant value. Besides, the research also shows the transconductance of the traditional complementary differential pairs will be affected by temperature and process variation, and the deviations of around 12% from its nominal value would be obtained.

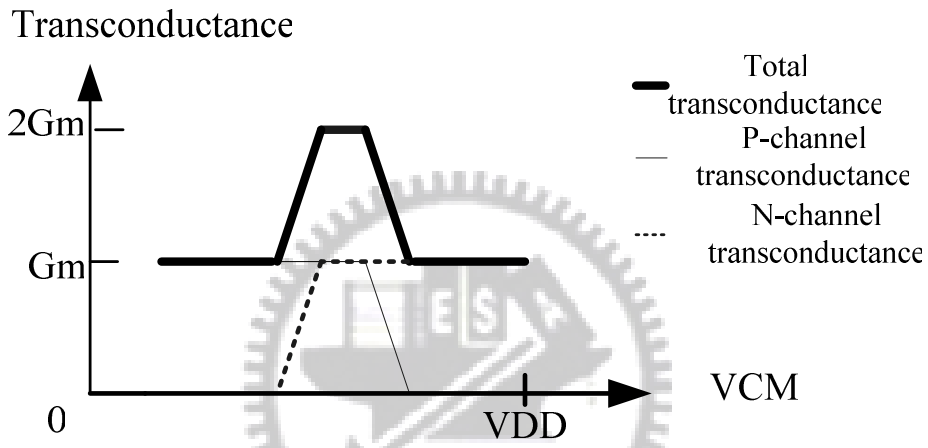


Fig. 1.1 The total GM of the n-channel and p-channel differential pair.

1.2 overview of the filter

In the natural world, the quality of the signal might be influenced by noise. Hence, in order to remove the disturbance of noise, we must develop filters. In 1915, the basic concepts of the electric filter were developed independently by Wagner in Germany and Campbell in the United States. Up to now, filter theory and implementation techniques have been developed to a high degree of perfection. Here we will present some popular technologies that can realize analog filters. For example active RC filter, switched-capacitor, and Transconductance-C Filter.

The active RC filter is very popular technology to realize analog filter. Accuracy of the resistance value is hard to achieve due to process variation. Moreover, this design uses a large amount of resistors which consumes chip area.

The SC filters use the same method as the active RC methods to obtain cutoff frequency. Different from the active RC filter, SC filters use switches, capacitors and clock frequency to replace the resistance. It wastes the area of layout because we have to supply another clock frequency circuit.

The GM-C filter is an analog filter technique that performs good frequency responses of the signal transfer functions. Analog filters do not require extra processing steps, as compared with active-RC filters, and their frequency tuning is easily achieved using dc bias voltage or current.

1.3 Motivation

With the development of the third-generation (3G) wideband code-division multiple-access (WCDMA) wireless cellular networks, the need for low-cost, low power consumption, and high integration is becoming important for the commercial development of 3G mobile handsets. A direct-conversion receiver IC was designed for the WCDMA mobile systems. By using the WCDMA systems, the speed of the transmission of data would be promoted substantially. The direct-conversion receiver architecture with the proper use of silicon process, circuit design techniques and architecture implementation represents a promising system solution for high integration platforms for 3G handsets. Figure 1.1 shows the architecture of the

WCDAM direct-conversion receiver system[10,11], and we will put emphasis on the channel select filter in the thesis. In past days, the channel select filter wasn't included in the entire chip, but now, in a IF receiver IC, channel selectivity is achieved at baseband by on-chip low-pass filters. In order to achieve the integration of the system-on-chip(SOC), the development of the active filter have become the key point of the research.

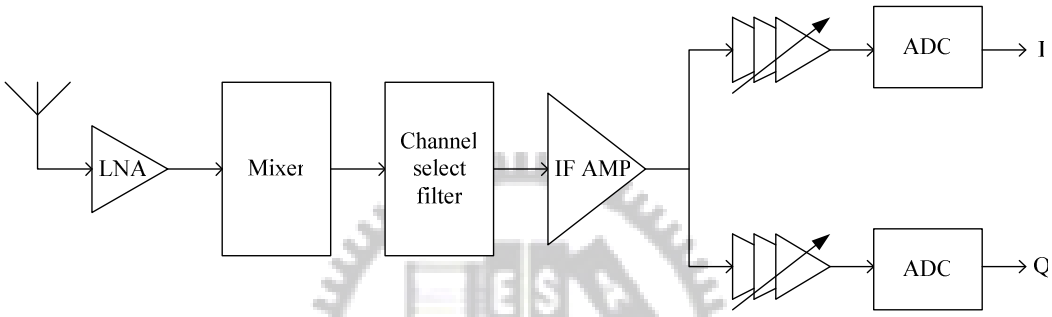


Figure 1.2 Direct-conversion WCDMA receiver system.

Chapter 2

An Overview of Rail-to-rail transconductor

2.1 Introduction

In this thesis, we will review how the rail-to-rail transconductors with constant GM and constant slew rate works. Also we will talk about drawbacks of these circuits.

2.2 Overview of the Rail-to-rail transconductor

We will suppose different input common-mode voltage from low to high to analysis rail-to-rail transconductors. We often divide the whole rail-to-rail voltage into three parts and most of the rail-to-rail transconductors will have turning point. In all the rail-to-rail structure, we will discuss the low input voltage, the middle input voltage and high input voltage. The turning point happens at differential pair's switching and always in the middle of the rail-to-rail voltage.

2.2.1 PMOS differential pair + NMOS differential pair structure

First of all, the typical techniques which are used to keep constant GM have been introduced in [6]. The first method is regulating tail current of input pairs, including one-time current mirror, three-times current mirrors, square root current control and current switches. The circuit is showed in figure2.1. The W/L ratio of M1, M2, M3, M4 should be satisfied the equation (2.1).

$$\mu_n C_{ox} \frac{W}{L}_{(M1M2)} = \mu_p C_{ox} \frac{W}{L}_{(M3M4)} \tag{2.1}$$

When input voltage is low the p-type differential pair will on, and the tail current will be 4I. If input common-mode voltage is in middle value both n-type and p-type differential pair will on and the tail current of the two differential pairs are I. If input common-mode voltage is high, the tail current of n-type differential pair will be 4I. By table 2.1 we can easily realize that the GM will be a constant.

Unfortunately, the dc current will be doubled when input common-mode voltage is in high or low value. Slewing value will have variations. The research also shows the transconductance will be easily affected by temperature and process variation, and the deviations of around 12% from its nominal value would be obtained.

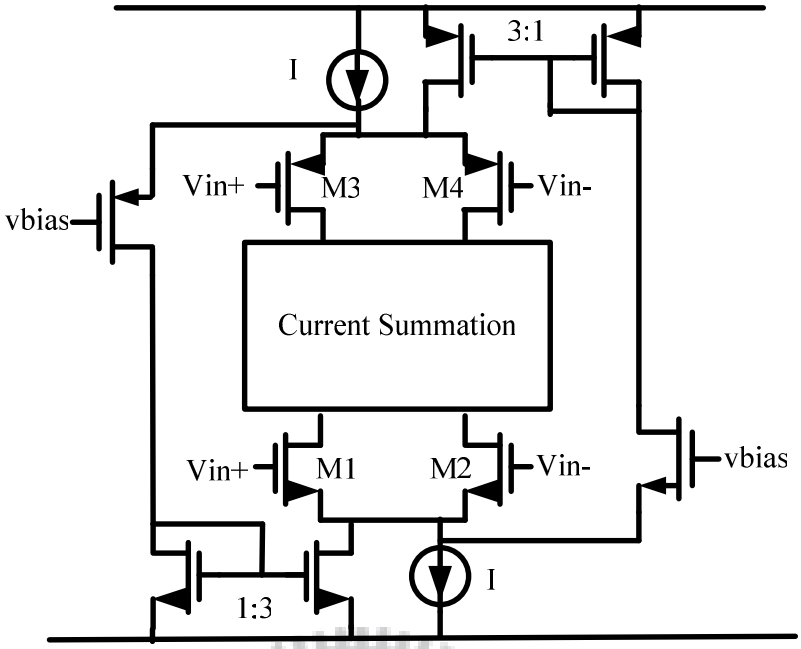


Figure 2.1 rail-to-rail ota

TABLE 2.1 the GM of the rial-to-rail ota

Input common-mode Voltage	***DC current***	***GM***
Low	4I	$GM = 2\sqrt{\mu_n C_{ox} \frac{W}{L} 4I}$
Medium	2I	$GM = 2\sqrt{\mu_n C_{ox} \frac{W}{L} I} + 2\sqrt{\mu_p C_{ox} \frac{W}{L} I}$
high	4I	$GM = 2\sqrt{\mu_p C_{ox} \frac{W}{L} 4I}$

2.2.2 Level shift NMOS differential pair + NMOS differential pair

structure

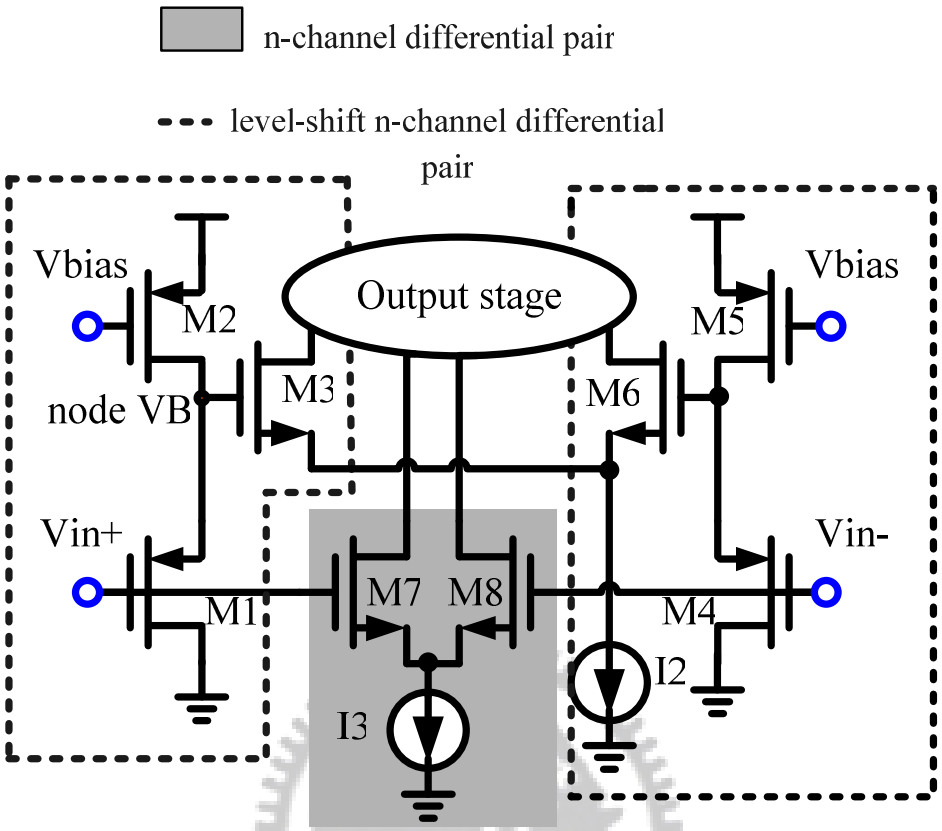


Figure 2.2 rail-to-rail ota

Then, a modified rail-to-rail input stage in [7] is shown in Fig. 2.2 An n-channel differential pair composed by transistors M7 and M8 and a level-shift n-channel differential pair composed by transistors M1 to M6 are used. The n-channel differential pair works as a traditional n-channel differential pair, and the other n-channel differential pair followed by a level-shift circuit works as a traditional p-channel differential pair. The W/L ratio of M3 M6 M7 M8 is all the same. The voltage of node b will be:

$$V_{(nodeb)} = Vin + \sqrt{\frac{I_{(m2)}}{k_{(m1)}}} \tag{2.2}$$

V(node b) should be bigger than the threshold voltage of the nmos, even input common-mode voltage (Vin) is zero. We can easily control the value of V(node b) by

tuning the gate voltage of M2. Although the level-shift circuit can shift the input common-mode voltage from a low value to a higher one, the voltage at node b will reach to the supply rail and transistors M1 is turned off when a high input common-mode voltage is applied. However, needless to say, the rail-to-rail input stage in Fig. 2.2 provides neither a constant small-signal nor a constant large-signal behavior.

Feedforward section (FF section) is designed to keep the constant of transconductance and the dc current of the input stage. In such a way, ideally, exactly constant small-signal and large-signal behaviors of the overall circuit are obtained. Fig. 2.3 is the rail-to-rail input stage with Feedforward section.

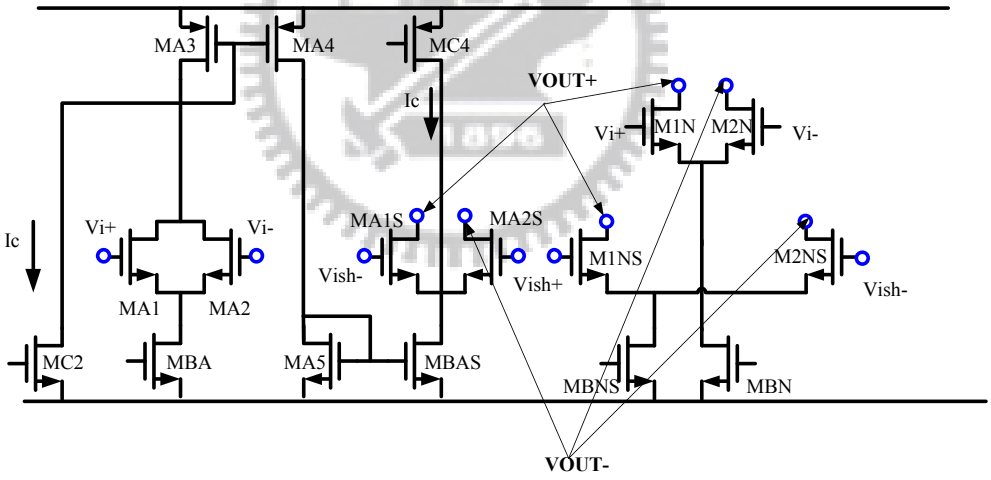


Figure 2.3 rail-to-rail ota

If input common-mode voltage close to ground, the current source transistors MBA and MBN are cut off. The small-signal and the dc current behaviors of the rail-to-rail input stage only contribute by the differential pair M1NS–M2NS which is biased with a current equal to I_B.

In the middle voltage range, both input pairs (M1N–M2N and M1NS–M2NS) are active and give the same transconductance and limiting current contributions. However, a current equal to I_B is provided to the input pair MA1S–MA2S of the FF section, which cancels out the limiting current and transconductance contribution of one of the differential pairs of the input stage. Therefore, the small and large-signal responses of the stage in the middle input common-mode voltage range are maintained equal to the corresponding values for low input common-mode voltage levels.

Finally, for input common-mode voltage values close to vdd, the bias current of the input source followers (MS2, MS4) becomes zero and the FF stage and the input pair M1NS–M2NS give no contribution to the output. Thus, the only differential pair active is M1N–M2N, and the small and large-signal behaviors of the stage are the same as in the above considered operating regions. In addition, the small and large-signal behaviors are also maintained constant in the input common-mode voltage interval where the differential input pairs go from full operation to cutoff or vice versa. Indeed, when the current source MBN is in the triode region, the current source MBA of the FF canceling stage also operates in the same bias conditions, and the current through MBAS turns out to be identical to the current through MBN. Therefore, the current contribution of the input pair M1N–M2N is perfectly canceled out by the contribution of the differential pair MA1S–MA2S, since they have the same aspect ratios and are biased exactly with the same current level. As stated above, the variation in the small- and large-signal behaviors in the region close to vdd arises when the current source transistors MS2 and MS4 of the source followers go into the triode region. In the proposed scheme, this fact affects the differential pairs M1NS–M2NS and MA1S–MA2S in the same way, so that their contributions are

perfectly canceled out. Fig.2.4 shows the GM of this circuit.

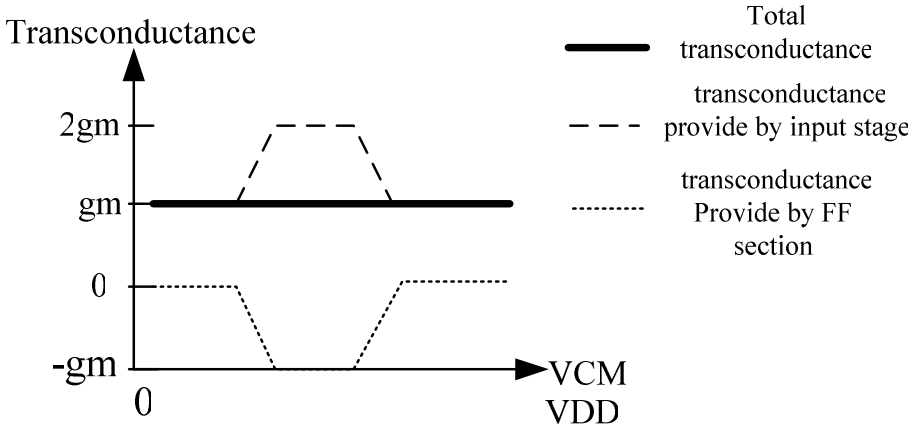


Figure 2.4 GM of the rail-to-rail ota

From Fig.2.4 we can understand that

(transconductance provide by input stage) – (transconductance Provide by FF section) = Total transconductance

This structure can increase the deviation performance of the transconductance when both of the differential pairs have the same aspect ratio. It makes two differential pair have the same characteristic. The transconductance will not affected by temperature and process variation. However, the FF section is too complicated. Its waste a lot of area and power on FF section.

2.2.3Differential pairs that work in the weak inversion

Usually, the main differential pairs of transconductance works in the saturation region. Working in the saturation region can make sure the GM of the transconductance will be big stable. Surely, the tail current has direct proportion to GM. And GM has direct proportion to the unity-gain frequency of the ota circuit which is given by

$$f_u = \frac{GM}{2\pi C_L} \tag{2.3}$$

C_L is the capacitor of the output stage. GM is defined Iout/Vin

In the other words, GM value is the most important parameter in transconductance design. But the main differential pairs that work in saturation region cost more power than others. Especilly a rail-to-rail transconductance costs twice power consumtion than a normal one. In modern circuit design low power is another important thing. We need two differential pairs to confirm the transconductance can operate in the rail to rail range.

From [12] this research makes a contrast between transistors that work in saturation region and weak region. So we can notice that the mos works in the weak inversion region is a very good choice in the low power and low distortion circuit design. The only drawback of the differential pair that works in the weak inversion is low speed. The speed will be limited by the tail current.

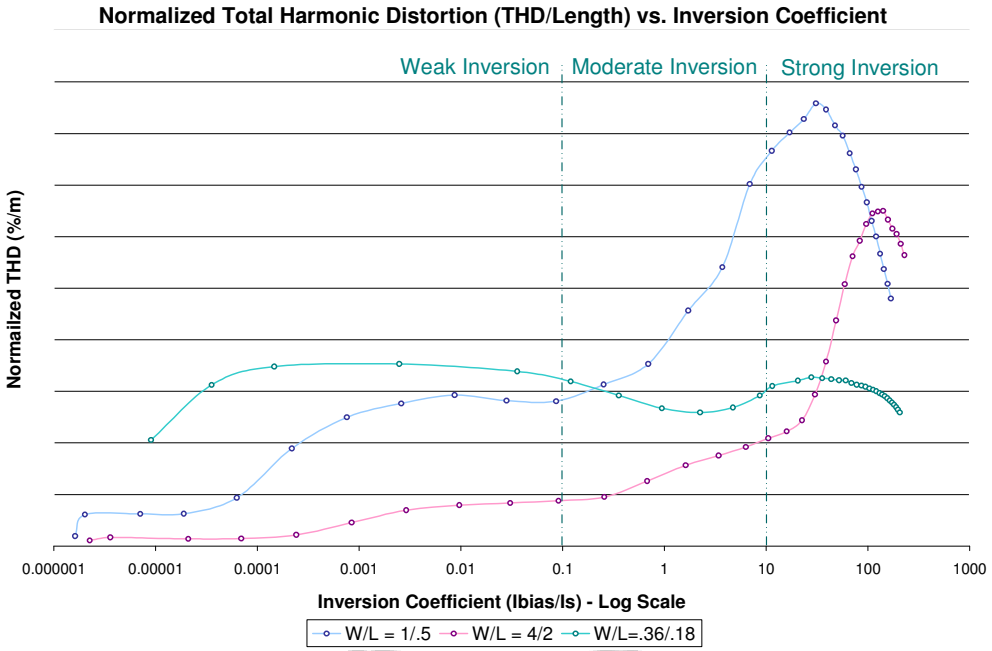


Figure 2.5 Total Harmonic Distortion in different region [3]

Table 2.2 weak inversion vs Saturation region

	Weak Inversion	Saturation region
Advantages	Lowest power dissipation	Relatively fast
	Low distortion	
	Lower threshold voltages	
Disadvantages	Relatively slow	Increasing distortion
		High power dissipation

In [8] and [9], a rail-to-rail input stage with constant GM and constant slew rate is introduced. Both of them use a p-type differential pair and a level shift p-type differential pairs that we discuss in last section. In order to keep constant transconductance, they make the main differential pair working in the weak inversion region.

We usually assumed that the device turns off abruptly as V_{GS} drops blew V_{TH}. Actually, for $V_{GS} \fallingdotseq V_{TH}$ a weak inversion layer still exists and some current flows from drain to source[13]. The equation of the drain current and the V_{GS} can be express as:

$$I_D = I_0 \exp \frac{V_{GS}}{\zeta V_t} \tag{2.4}$$

I_D is drain current and other factors have their usually meanings. Fig. 2.4 shows the relationship of I_D and V_{GS}. Here we have another problem. We have to keep the differential pair that works in the weak inversion region. We can control the tail current of the differential pair to make sure the differential pair works in the weak inversion.

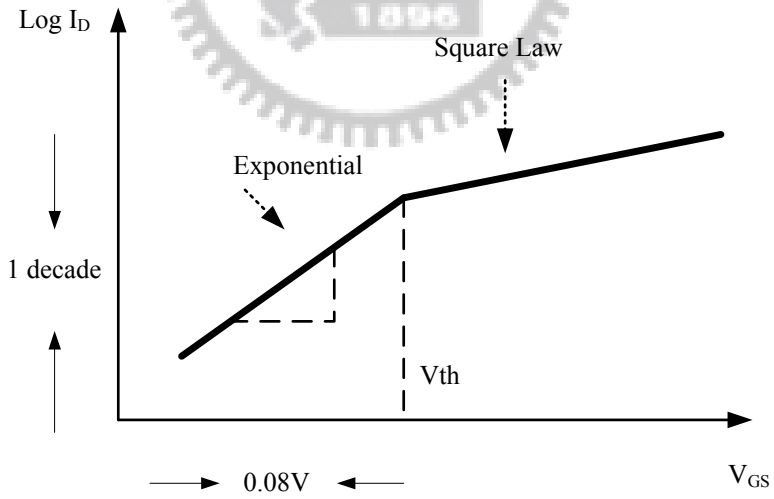


Figure 2.6 MOS subthreshold characteristics

From equation (2.4) we can infer the transconductance is

$$gm = \frac{\partial I_D}{\partial V_{GS}} = \frac{I_D}{\zeta V_t} \tag{2.5}$$

$$gm = \frac{I_D}{\zeta V_t} = \frac{I_{tail}}{2nV_t} = \frac{I_2}{2nV_t} + \frac{I_3}{2nV_t} \tag{2.6}$$

By (2.5) (2.6) the constant transconductance can be obtained by keeping the sum of the tail currents of input pairs to be equal. Figure2.6 shows the I2 and I3 which shows in (2.6).

Unfortunately, in Figure 2.6 [8] when the input common-mode voltage is low, the level-shift circuit turns off and part of the tail current will flow through the followed differential pair(M5,M6), and thus the transconductance is varied.

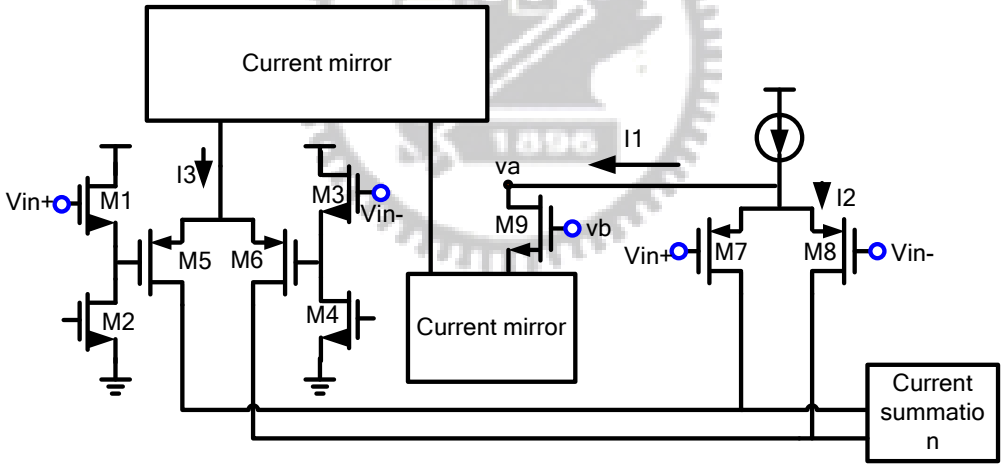


Figure 2.7 input stage with current control

In the other words, when the common mode voltage is low M1 M3 will cut off. The source of the M1 will drop to zero. M5 and M6 will operate at low input common-mode voltage. But ac signal can not pass to M5 and M6. Because of M1 and M3 will cut off. It makes the transistors M5 and M6 will not provide the GM. Fig 2.8 shows the gm value in the rail-to-rail range without any solution.

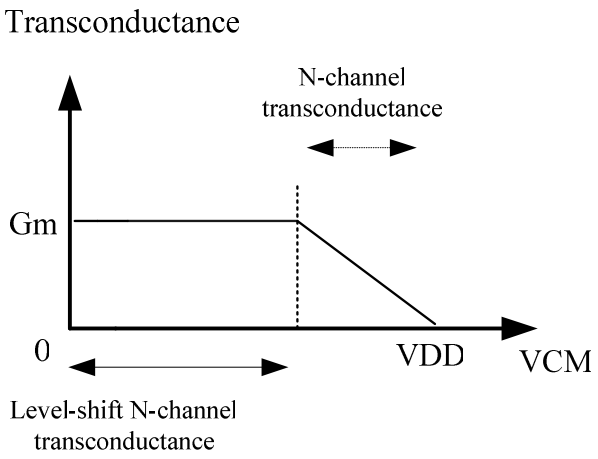


Figure 2.8 the GM of the different input common mode voltage without detect circuit

In order to solve this problem a current switch transistors M9 is used. when VA ≤VB+|Vthp|, I1=0, I2=I, all current flow through M7 and M8, M5 and M6 turn off. When VA ≥VB+|Vthp| with input common mode voltage increasing, I1>0, I2<I, M5, M6, M7 and M8 will all operate. At this time, level shifter should also operate. Input common mode voltage continues increasing until all current flow through M5and M6, as a result, i1=I, i2=0, M7 and M8 will turn off. VB is a key parameter, which requires M9 should turn on before M3 and M4 turn off, and after voltage level shifters operate.

Since VA will change with input common mode voltage change, total current I will not be constant. As a result, transconductance gm, total GM will fluctuate. This circuit uses too many current mirrors. Current mirror can not perfectly copy the tail current. That also makes the total GM fluctuate. The fluctuation of the GM is about 4%. And they use another tail current control circuit to overcome the fluctuation. And the power and the area of chip will be waste.

TABLE 2.3 The Transconductance in Different Input Common-Mode Voltage

Input common-mode voltage	GM provider	GM
Low	p-channel differential pair(M7 M8)	$GM = \frac{I_{tail}}{2nV_t} = \frac{I_2}{2nV_t}$
Middle	level-shift p-channel and p-channel differential pair.	$GM = \frac{I_{tail}}{2nV_t} = \frac{I_2}{2nV_t} + \frac{I_3}{2nV_t}$
High	p-channel differential pair(M5 M6)	$GM = \frac{I_{tail}}{2nV_t} = \frac{I_3}{2nV_t}$

Another paper [9] presents the similar structure, and the different is the current switch M9. Paper [9] uses a sensing circuit to detect. It is better than the current switches because the value of the vb is hard for us to define.

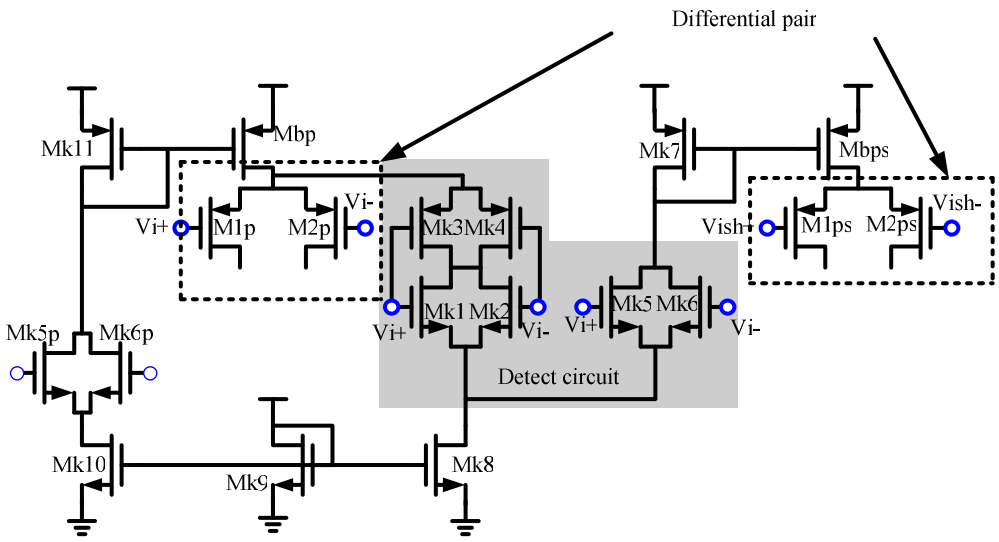


Figure 2.9 input stage with current control

The main idea is using the transistors MK1 MK2 MK3 MK4 MK5 MK6 to control the level-shift differential pairs. It is better than current switches that we talk about before because we don't have to choice a suitable voltage of vb. The value of the voltage vb might be amended in different situation.

We apply this minimum current circuit as shown in Fig.27 (MK1-MK4) between two current sources which provide the tail current of two input differential pairs. The value of this current source is equal to the minimum of the effective tail currents IBP and IBPS. To obtain this minimum current we use the principle indicated in Fig. 2.7 If a CMOS current source and IBPS are equal to Itail. The current Ix (current of MK1-MK4) is also equal to Itail. If the common input voltage approaches the upper supply rail, MK5 will go out of saturation and will consequently provide less current. This will result in a lower effective tail current for the M1P-M2P input differential pair IBP . Therefore, IBP will be smaller than IBPS and Ix will be equal to IBP. Thus,

a decrease of IBP results in the same decrease of Ix. Because the sum of Ix and IBPS remains equal to 2Itail (delivered by MK6), IBPS has to increase by the same amount.

Circuit that in [8], [9] have the same problem is too many current mirror. The matching of the current mirror is the most important condition to keep the constant GM. Unfortunately, the tail current can not perfect copy. And the current mirror will waste addition power and layout area.

Chapter 3

Design of ota

3.1 Introduction

Base on the previous research, a rail-to-rail transconductance with constant GM and constant DC current is designed. In this circuit we use a level-shift noms and an nmos differential pairs that operate in weak inversion. The detect circuit that uses to keep constant GM in high common-mode voltage will redesign. Here we try to create a detection circuit in the input part to replace the detection circuit that makes in the current source.

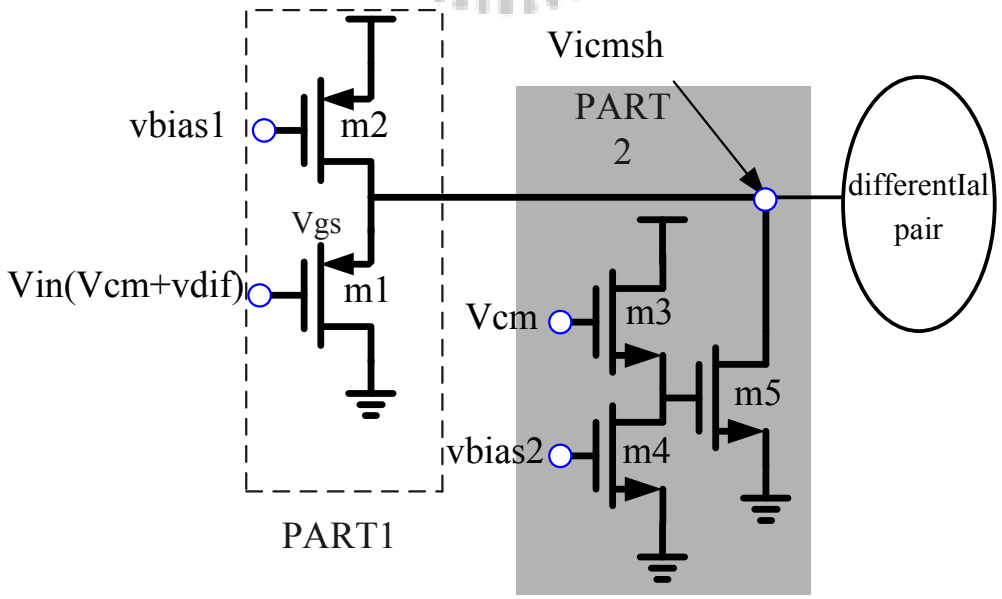


Figure 3.1The modified level- shifter with a Vcm detection circuit.

3.2Modified the transconductance

The original level-shift will not work in the high common-mode voltage. In order to make sure that the n-channel and a level-shift n-channel differential pair can operate correctly. It makes the GM can not be a constant in high common-mode voltage. Here we change the design of the level-shift n-channel differential pair. Fig. 3.1 shows the proposed level-shift circuit. PART1 is the conventional source follower, and PART2 is a VCM detection circuit. PART2's structure is used to turn off the main differential pair when the input common-mode voltage is too high. The detection circuit is composed by an n-type source follower that is composed by transistor M3 and M4 and a switch transistor M5. M3 and M4 are used to shift a negative voltage. It makes the switch transistor M5 can turn off the PART1's level-shift in the high common-mode voltage level as our wish. The circuit operation under different input common-mode range is analyzed as follows:

When the input common-mode voltage is low, the detection circuit in PART2 will turn off. On the other hand, the circuit in PART1 shifts the input voltage to a higher value, and the Vgs voltage of transistor M1 should be high enough to turn on the main differential pair. We can easily control the Vgs voltage of transistor M1 by tuning the gate voltage of M2, and thus the voltage at Vicmsh can be controlled.

When input common-mode voltage is in the middle value, transistor M3 would be turn on, and transistor M5 is designed to be turned off. Thus, the VCM detection circuit in PART2 would not effect the overall circuit operation. Similarly, transistor M1 and M2 work as the input common-mode voltage is low.

When the input common-mode voltage is high, transistor M5 will turn on and the current from transistor M2 will go through transistor M5. Then, the voltage at Vicmsh would be smaller than the overdrive voltage of the followed differential pair, and thus the main differential pair will turn off. In the other words, before the Vicmsh up to the supply rail, the detection circuit turns off the followed differential pair by reducing the value of Vicmsh.

TABLE 3.1 The Transconductance in Different Input Common-Mode Voltage

Input common-mode voltage	GM provider	GM
Low	level-shift n-channel differential pair	$GM = \frac{I_{tail}}{2nV_t} = \frac{I_2}{2nV_t}$
Middle	level-shift n-channel and n-channel differential pair.	$GM = \frac{I_{tail}}{2nV_t} = \frac{I_2}{2nV_t} + \frac{I_3}{2nV_t}$
High	n-channel differential pair.(level-shift n-channel will be turned off by detect circuit)	$GM = \frac{I_{tail}}{2nV_t} = \frac{I_3}{2nV_t}$

Fig. 3.2 shows a test of the proposed level-shift circuit. We apply a sinusoidal input signal with a rail-to-rail swing range at the gate of transistor M1. Thus, the Vicmsh voltage will drop to zero at high input voltage range. When input common-mode

voltage is low or middle range, the voltage is followed well. The turning point of the voltage can be changed by the different bias. Fig. 3.3 shows the final implementation of the rail-to-rail transconductor. The current summation block is designed by the well known folded cascade structure.

Some details should be noticed to design the proposed level-shift circuit.

1. The Vgs of M1 should be high enough to turn on the main differential pair when the input common mode voltage is zero.
2. When the input common-mode voltage is high, we have to make sure all the current from transistor M2 will go through transistor M5. Thus, the aspect ratio of transistor M5 should be much larger than transistor M1.
3. The total transconductance can be tuned by controlling the value of current source Itail. This is important to the filter design.
4. Because the differential pairs would work in the weak inversion region, the current source should be

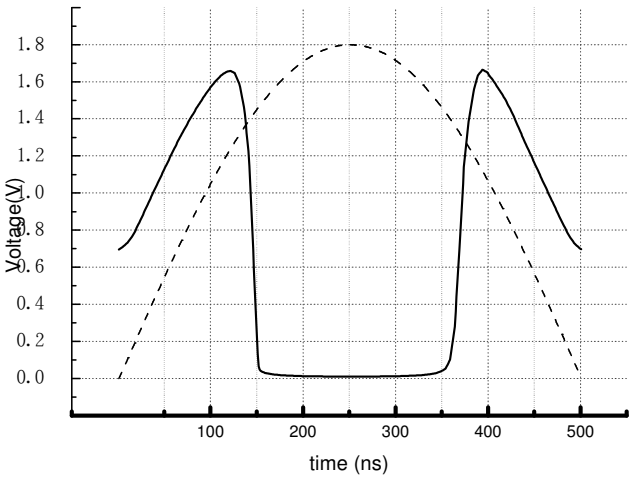


Fig. 3.2 Simulation resof the proposed level-shift circuit.

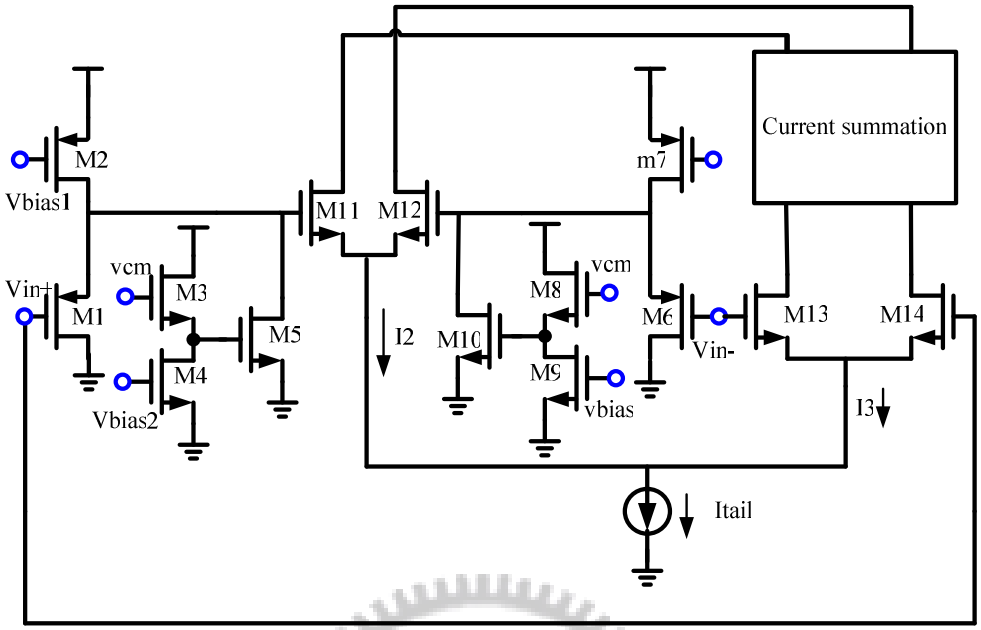


Fig. 3.3 rail-to-rail transconductor

3.3Linearity of differential pairs

3.3.1 THD

If a sinusoidal waveform is applied to a linear time-invariant system, it is known that the output will also be a sinusoidal waveform at the same frequency, but possibly with different magnitude and phase values. However, if the same input is applied to a nonlinear system, the output signal will have frequency at harmonics of the input waveform, including the fundamental harmonic. For example, if the input signal is a 1-MHz sinusoidal waveform, the output signal will have power at the fundamental, 1

MHz, as well as at the harmonic frequencies, 2MHz, 3MHz, and so on. The total harmonic distortion (THD) of a signal is defined to be the ratio of the total power of the second and higher harmonic components to the power of the fundamental for that signal. In units of dB, THD is found using the following relation:

$$\mathrm{THD} = 10\log\left(\frac{V_{h2}^{\,2} + V_{h3}^{\,2} + V_{h4}^{\,2} + \cdots}{V_f^{\,2}}\right) \tag{4.25}$$

where Vf is the amplitude of the fundamental and Vhi is the amplitude of the ith harmonic component. Sometimes THD is presented as a percentage value as follow:

$$\mathrm{THD} = \frac{\sqrt{V_{h2}^{\,2} + V_{h3}^{\,2} + V_{h4}^{\,2} + \cdots}}{V_f} \times 100\% \tag{4.26}$$

It should be noted that the THD value is almost always a function of the amplitude of the input signal level, and thus the corresponding signal amplitude must also be reported. Also, for practical reasons, typically the power of only the first few (say, the first 5) harmonics are included since the distortion components usually fall off quickly for higher harmonics.

3.3.2 THD in saturation region

The differential pairs that work in the saturation region followed square-law relation between drain current Id and gate source voltage Vgs that is showen in the figure 3.4, and the equation is shown in (3.1).

$$I_{DS} = \frac{1}{2} K (V_{gs} - V_t)^2 \tag{3.1}$$

Where $K = \frac{1}{2} \mu_0 C_{ox} \frac{W}{L}$

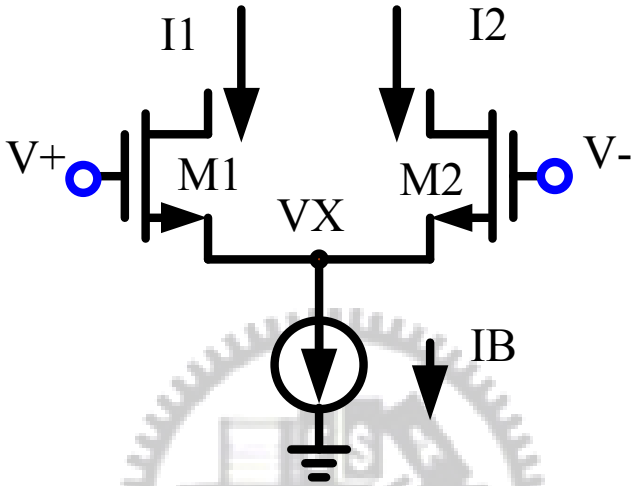


Fig. 3.4 differential pairs

IB is the drain current of the differential pairs that is provided by a current source with high impedance. I1 is drain to source current of M1. I2 is drain to source current of M2. V+ V- is the input voltage. I1+I2=IB and I1-I2=Iout. Usually we will see VX of the fig 3.4 as a virtual ground. Actually if Vid=(V+ - V-) is large the supposition of VX should be change. According to the square-law we can get (3.2) and (3.3). From equation (3.2) and (3.3) we can get equation (3.4) and (3.5).

$$I_1 = K\left[(V_+ - V_x) - V_{th}\right]^2 \tag{3.2}$$

$$I_2 = K\left[(V_- - V_x) - V_{th}\right]^2 \tag{3.3}$$

$$\sqrt{\frac{I_1}{K}} = (V_+ - V_x) - V_{th} \tag{3.4}$$

$$\sqrt{\frac{I_2}{K}} = (V_- - V_x) - V_{th} \tag{3.5}$$

Let (3.4)-(3.5) we get (3.6)

$$\sqrt{\frac{1}{K}}(\sqrt{I1} - \sqrt{I2}) = V_+ - V_- = Vid \tag{3.6}$$

$$I1 + I2 = IB \tag{3.7}$$

We can get equation (3.8) by (3.6) and (3.7)

$$I_{out} = \sqrt{1 - (\frac{Vd}{2V_{ds(sat)}})^2} \times \sqrt{2KI_B} \times Vid \tag{3.8}$$

Where $V_{ds(sat)} = V_{gs} - V_t$

Equation (3.8) is different from the equation that we usually used in the saturation region. The non-linear term will occur when the VX is not as virtual ground. This is because Vid is large. If Vid is small we can ignore the non-linear term. And we can use taylor expansion to analyze the equation (3.8).

$$gm = \frac{1}{2}(\sqrt{2I_BK} - \frac{3}{2\sqrt{2}}\frac{K^{\frac{3}{2}}}{\sqrt{I_B}}V_{id^2}.....) \tag{3.9}$$

We can find THD from the equation (3.9). The even harmonic distortion components appear at the outputs with the same amplitude and same phase, and they ideally cancel each other when the differential output current is processed[14]. So if the differential pairs are perfectly matching the even harmonic distortion components will be canceled. Usually the THD3 will be the index of the non-linear system. From equation we can realize that the Vid will be multiplication in each term. Vid is always less than 1V. So THD5 will much less than THD3. So THD3 is the most important non-linear term.

3.3.3 THD in weak inversion region

If the differential pair works in the weak inversion the non-linear term will be changed. The function of the mos that works in the weak inversion is shown in (3.10).

$$I = I_o \exp \frac{V_{gs}}{nV_t} \tag{3.10}$$

The same as the differential pair that works in the saturation region. If Vid=(V+ - V-) is large the supposition of node VX should be change. Here we can use (3.10) to express I1 and I2.

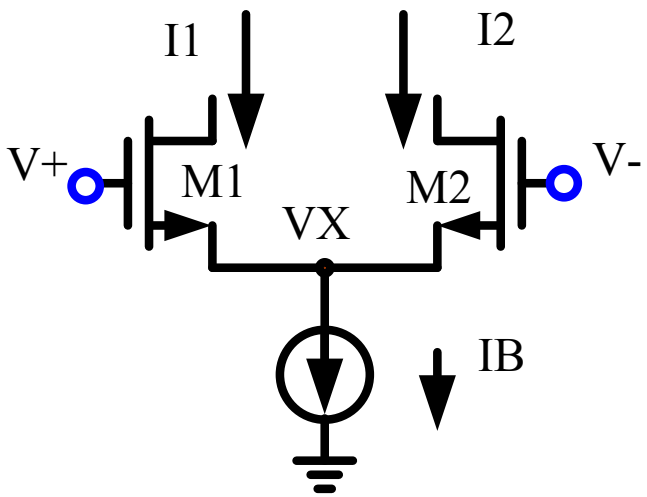


Fig3.5 differential pair

$$I_1 = I_0 \exp\frac{V_+ - V_x}{nV_t} \tag{3.11}$$

$$I_2 = I_0 \exp\frac{V_- - V_x}{nV_t} \tag{3.12}$$

(3.11)/(3.12) we can get (3.13)

$$\frac{I_1}{I_2} = \exp\frac{V_+ - V_-}{nV_t} = \exp\frac{Vid}{nV_t} \tag{3.13}$$

$$I1 + I2 = IB \tag{3.14}$$

By (3.13) and (3.14) we can get

$$I_1 = \frac{I_B}{(1+\exp\frac{Vid}{nv_t})}\exp\frac{Vid}{nv_t} \tag{3.15}$$

$$I_2 = \frac{I_B}{(1+\exp\frac{Vid}{nv_t})} \tag{3.16}$$

Where I1-I2=Iout

$$I_{OUT} = I_1 - I_2 = \frac{I_B}{(1+\exp\frac{Vid}{nv_t})}(\exp\frac{Vid}{nv_t} - 1) \tag{3.17}$$

From(3.17) finally we will find(3.18)

$$I_{OUT} = I_1 - I_2 = I_B \tanh\frac{Vid}{2nvt} \tag{3.18}$$

As the differential pair works in the weak inversion that we talked, equation (3.18) use taylor expansion to analyze the equation

$$\tanh\frac{Vid}{2nvt} = \sum_{n=1}^{\infty}\frac{B_{2n}4^n(4^n-1)}{(2n!)}\left(\frac{Vid}{2nvt}\right)^{2n-1} \tag{3.19}$$

Where B_{2n} is

n	0	1	2	3	4	5	6	7	8	9	10	11	12	13
Bn	1	-1/2	1/6	0	-1/30	0	1/42	0	-1/30	0	5/66	0	-691/2730	0

So the expansion will be

$$I_{OUT} = I_B \tanh\frac{Vid}{2nvt} = I_B\left[\frac{Vid}{2nvt} - \frac{1}{3}\left(\frac{Vid}{2nvt}\right)^3 + \frac{2}{15}\left(\frac{Vid}{2nvt}\right)^5 - \frac{7}{315}\left(\frac{Vid}{2nvt}\right)^7 .....\right] \quad (3.20)$$

From (3.20) we will find that the tail current will be the most important variable in (3.19). The total harmonic distortion (THD) will be influenced by the tail current of the differential pairs. The relationship of I_B and THD is direct proportion. The bigger I_B brings bigger THD. It will effect the correction of the gm. Also the tail current of the differential pair effects the gm value. The relationship of I_B and THD is direct proportion, too. So we have a trade off between GM value and THD. Otherwise the THD still be influenced by input signal Vid as the differential pair that works in the saturation region. We have to limit the value of the Vid to keep the total harmonic distortion.

Finally if the input signal Vid is small the $\tanh\frac{Vid}{2nvt} \cong \frac{Vid}{2nvt}$ can see Iout as

$$I_{OUT} = I_1 - I_2 = I_B\frac{Vid}{2nvt} \quad (3.21)$$

Equation (3.21) shows the same result as (2.6).

Chapter 4

Design of Continuous-Time Gm-C Filters

4.1 Fundamental Concepts of Analog Filters

A filter is a two port that shapes the spectrum of the input signal in order to obtain an output signal with the desired frequency content. Thus, a filter has a passbands where the frequency components are transmitted to the output and stopbands where they are rejected. The oldest technology for realizing filters makes use of inductors and capacitors, and the resulting circuits are called passive LC filters. Today, in order to miniaturize the size of filters, inductors cannot be used because their size cannot be reduced to a level compatible with modern integrated electronics. Therefore, there has been considerable interest in finding filter realizations that do not require inductors. The inductors can be avoided if we have access to gain. Therefore, the only passive components we need are resistors and capacitors, and gain is provided by operational amplifiers or operational transconductance amplifiers (OTAs). Such filters are referred to as active filters, sometimes more specifically as analog active filters to distinguish them from digital filters. Signals in analog active filers are normally continuous functions of time, sometimes sampled, whereas in digital filters signals are digitized. In modern communication systems, both analog signals and

digital signals must be processed. Often both analog and digital circuits and filters must be implemented together on the same integrated circuit chip for so-called mixed-mode signal processing.

4.2 LC Ladder Simulation by Signal-Flow Graphs

4.2.1 Introduction of LC Ladder Filters

Although the subject of this thesis is the design of active filters, we shall discuss some details concerning the design of passive LC filters. As the name implies, an LC filter is a lossless transmission network consisting of only inductors and capacitors. In normal operation, the network is embedded between a resistive source and a resistive load as shown in Figure 4.1, and Figure 4.2 shows the ladder topology. A lossless ladder is a circuit structure where all components apart from source and load resistors are lossless, that is, they are inductors and capacitors that dissipate no energy. Passive LC ladders have an inherent advantage over active filters in terms of their sensitivity to component tolerances. With the growing pressure towards microminiaturization, inductors were found to be too bulky so that designers started to replace passive RLC filters by active RC circuits where gain, obtained from operational amplifiers, together with resistors and capacitors in feedback networks, was used to achieve complex poles.

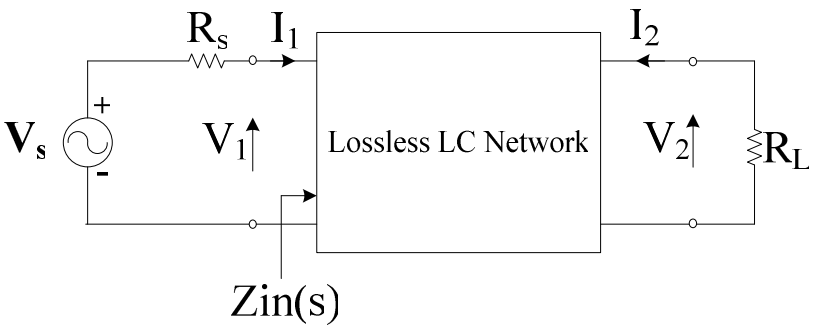


Figure 4.1 Resistively terminated lossless twoport.

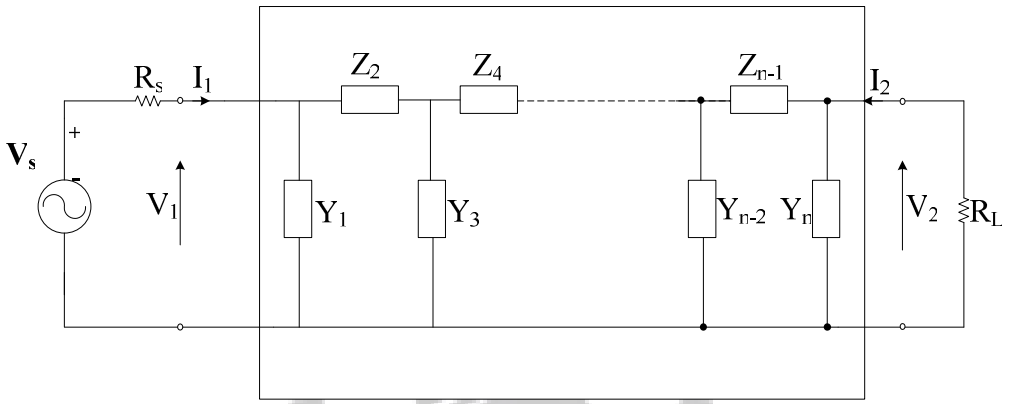


Figure 4.2 Resistively terminated ladder structure.

4.2.2 LC Ladder Simulation by Signal-Flow Graphs

Lossless filters designed for maximum power transfer have the best possible passband sensitivities, and such circuits are normally realized as LC ladders. A considerable amount of effort has been devoted in recent years to the development of active circuits which in one way or another simulate performance of passive ladders and thereby inherit their good sensitivity performance. Ladder simulations can be classified into two groups: operational simulation and element substitution. Both methods start from an existing LC prototype ladder; operational simulation endeavors to represent the internal operation of the ladder by simulating the equations describing

the circuit's performance, i.e., Kirchhoff's voltage and current laws and the I-V relationships of the ladder arms. Fundamentally, this procedure is based on simulating the signal-flow graph (SFG) of the ladder where all voltages and all currents are considered signals which propagate through the circuit.

4.3 Third-Order Low-Pass GM-C Filter

First of all we have to show how the ota circuit that used in the gm-c filter. The basic idea of the gm-c filter is using ota to replace the resistance and inductance.

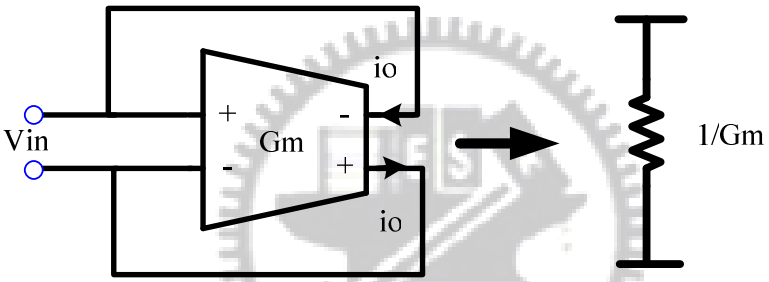


Figure 4.3 uses Gm replace resistance

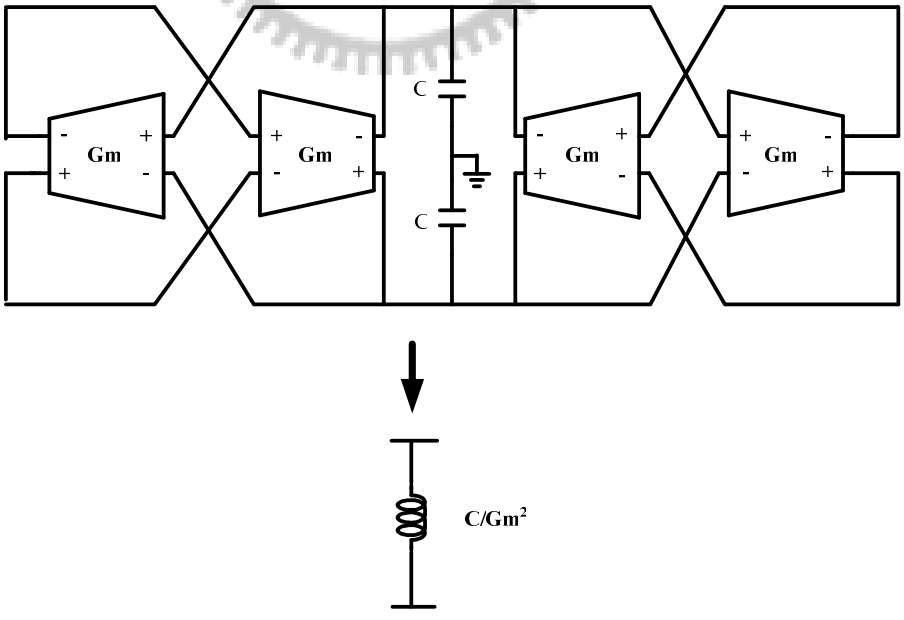


Figure 4.4 uses Gm and capacitance to replace inductance

Figure 4.5 shows a third-order low-pass LC-ladder prototype filter. By using signal-flow graph methods, it can be transformed into a third-order low-pass gm-C filter which consists of eight identical differential-input OTAs and six capacitors. And Figure 4.6 shows the final GM-C filter.

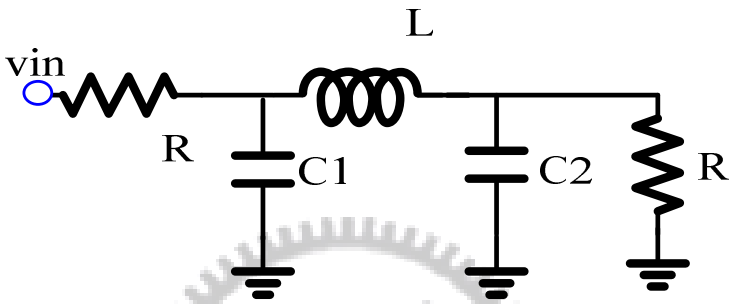


Figure 4.5 third-order LC lowpass filter

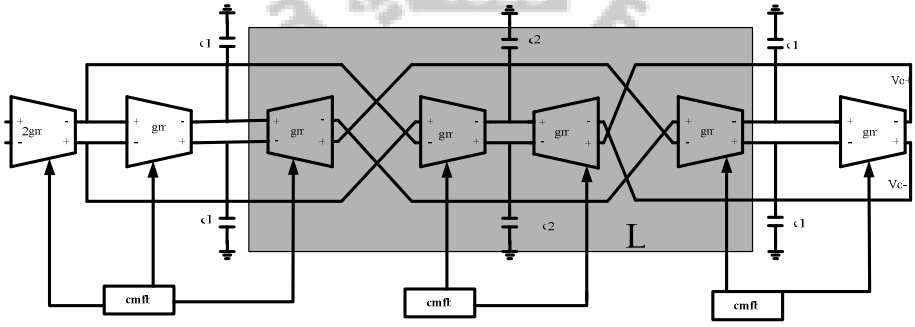


Figure 4.6 third-order GM-C lowpass filter

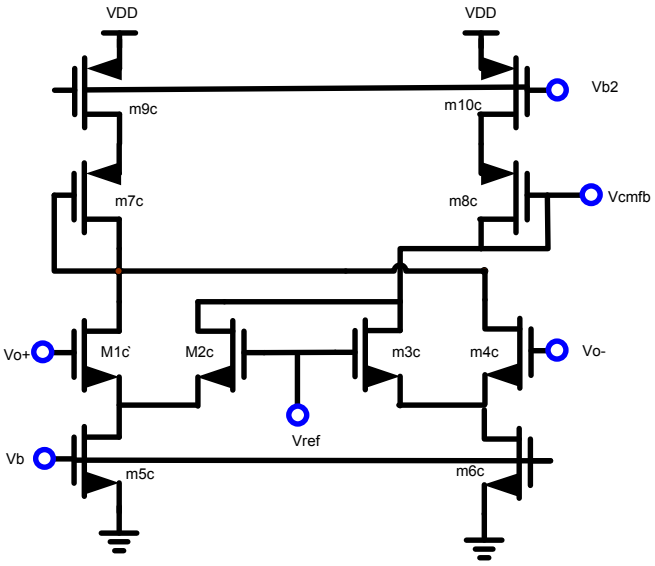


Figure 4.7 common mode feedback

Figure 4.7 shows the CMFB circuit. It connects at the output node of the rail-to-rail input stage. CMFB circuit is used to lock the output voltage of the ota. Voltage Vref is the expect voltage of the ota output node.

Chapter 5

Simulation and measurement

5.1 Introduction

In this thesis, we discuss the simulation results of ota and the filter. And we will discuss the measure result.

5.2 Simulation Results of the OTA

Fig. 5.1(a) shows the transconductance with respect to the input common-mode voltage from one supply rail to another one. We can see the transconductance fluctuation is less than ± 3%.

The gap in the middle of the input common voltage level happens when the level shifter differential pair turns off. In the chapter 3 we talked about the operation of the rail-to-rail ota. In Fig3.1 we see M5 as a perfect switch. Actually the same as other mos, M5 will operate in the weak inversion region. The DC current of M5 that works in the weak inversion is much less than M5 works in the saturation region. So let us review the operation of M5. When the common-mode voltage is high M5 is turn on the voltage of node Vicmsh will drop to ground. But if the common-mode voltage is

not high enough, M5 might operate in the weak inversion. There will be a small current pass through M5. The current will not big enough to turn off the transistor M1. But the shifted voltage will be influenced. This makes the signal might be slightly decrease. And when the common mode voltage approaches the tuning point the total GM will slightly decrease.

We can control the location by tuning the gate voltage of transistors M4 and M9. In Fig.5.1(b) shows that the gap occurs at a higher input common-mode voltage when we increase the gate voltage of transistor M4. Actually we can control the gap from the common-mode voltage 0.9 V to 1.1 V. This can make sure the gap will not influence the transconductance in the middle of the common-mode voltage.

Fig. 5.2 shows the gain and phase of the transconductor. The gain is around 42 dB, and the phase margin is 86 degree. And fig 5.2 (a)(b)(c) shows the gain and phase of the transconductor in different situation such as TT SS FF.

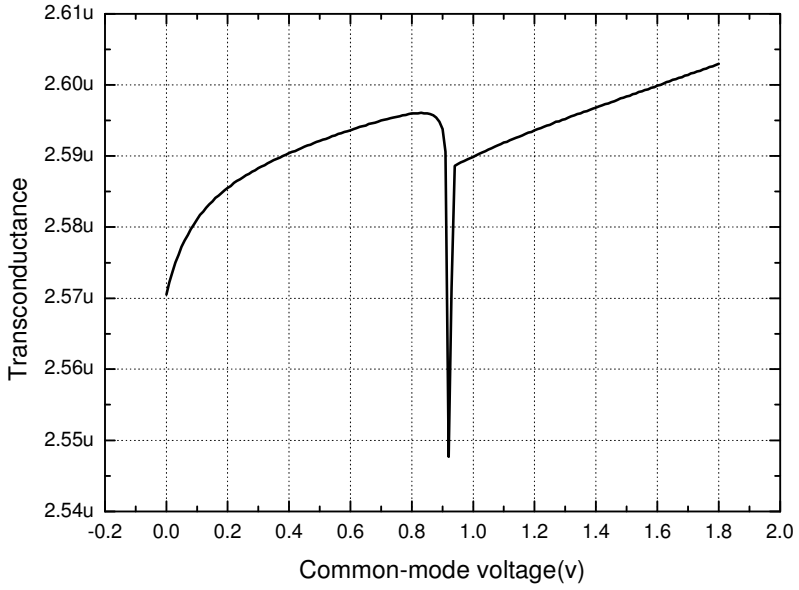


Figure 5.1(a) GM in different common-mode voltage

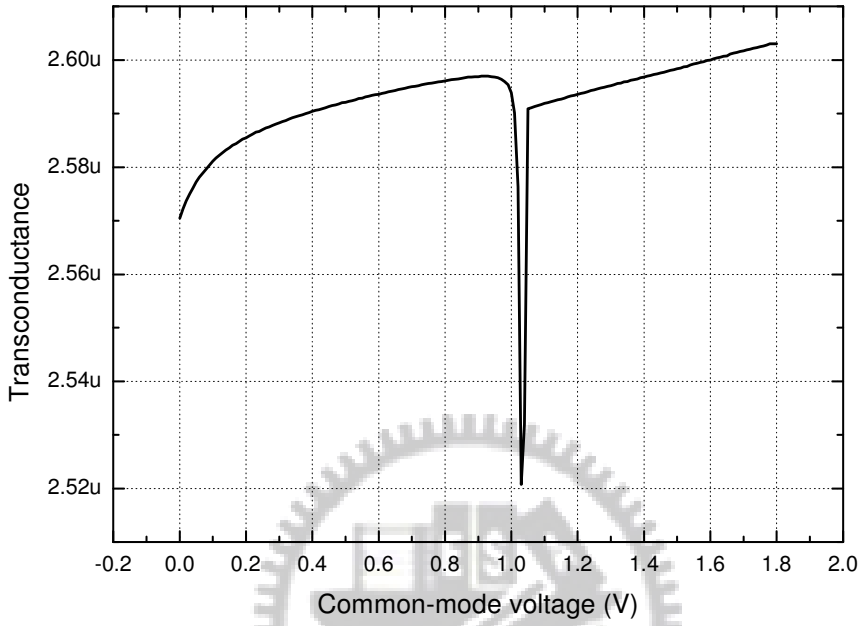


Figure 5.1(b) GM in different common-mode voltage

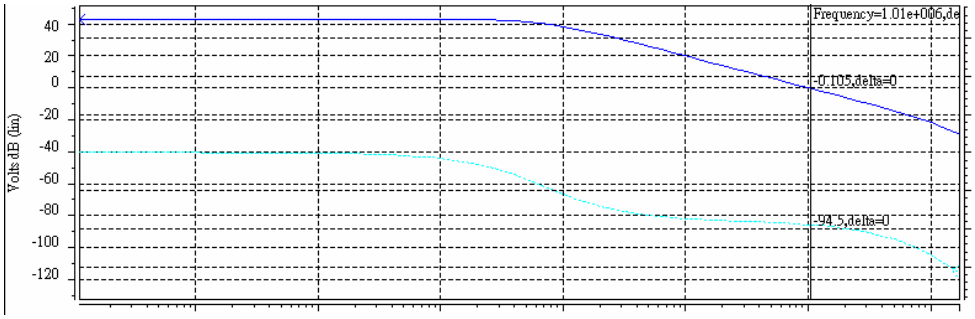


Figure 5.2(a) gain and phase of the transconductor

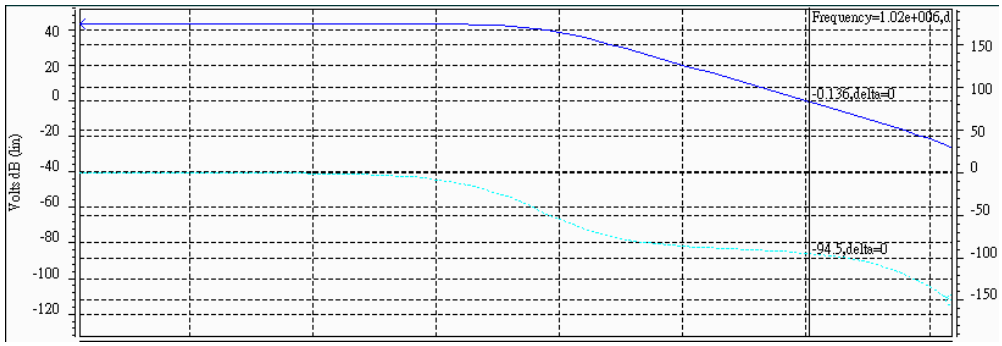


Figure 5.2(b) gain and phase of the transconductor

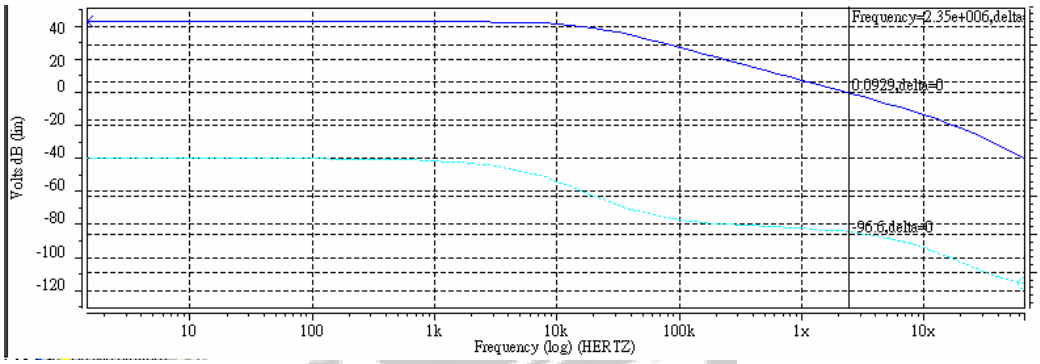
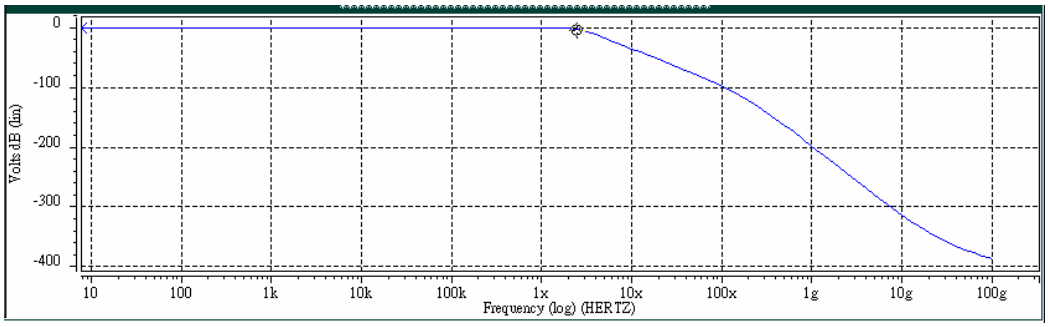


Figure 5.2(c) gain and phase of the transconductor



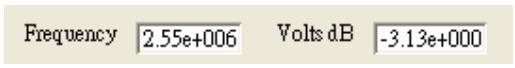


Fig. 5.3 cut off frequency of the filter

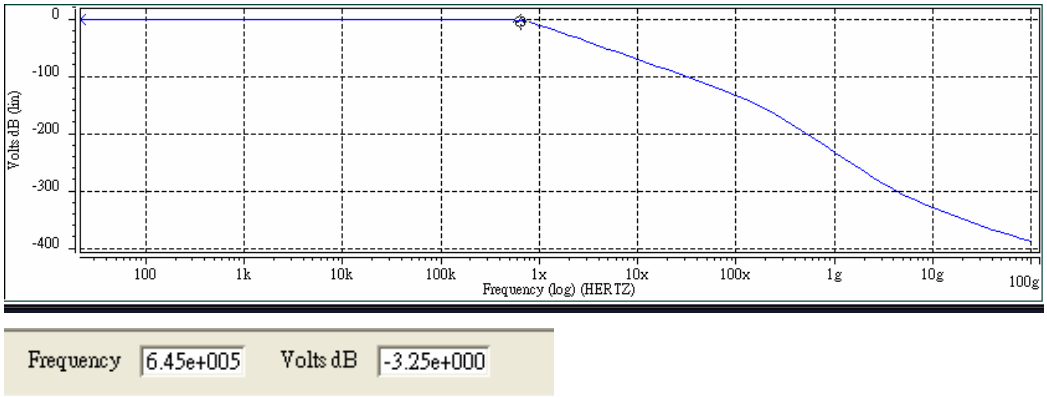


Fig. 5.4 cut off frequency of the filter

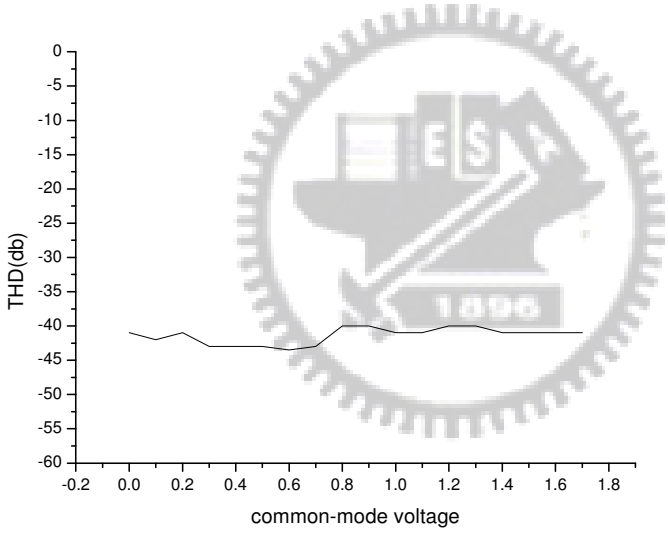


Fig. 5.5 THD in different common-mode voltage

And Fig. 5.3 shows the frequency response of the filter. The cutoff frequency can be tuning from 500k-3MHz. Fig 5.5 shows the THD of filter when the input signal is 750KHz 300mVpp and the common-mode voltage is from 0 to 1.8.

5.3 layout of the OTA and filter

Fig 5.6 shows the layout of the ota and the filter. Each of the ota output node will connect to a common mode feed back that is used to make sure the voltage of output node is correct, and every transistor in the output operates in the right region.

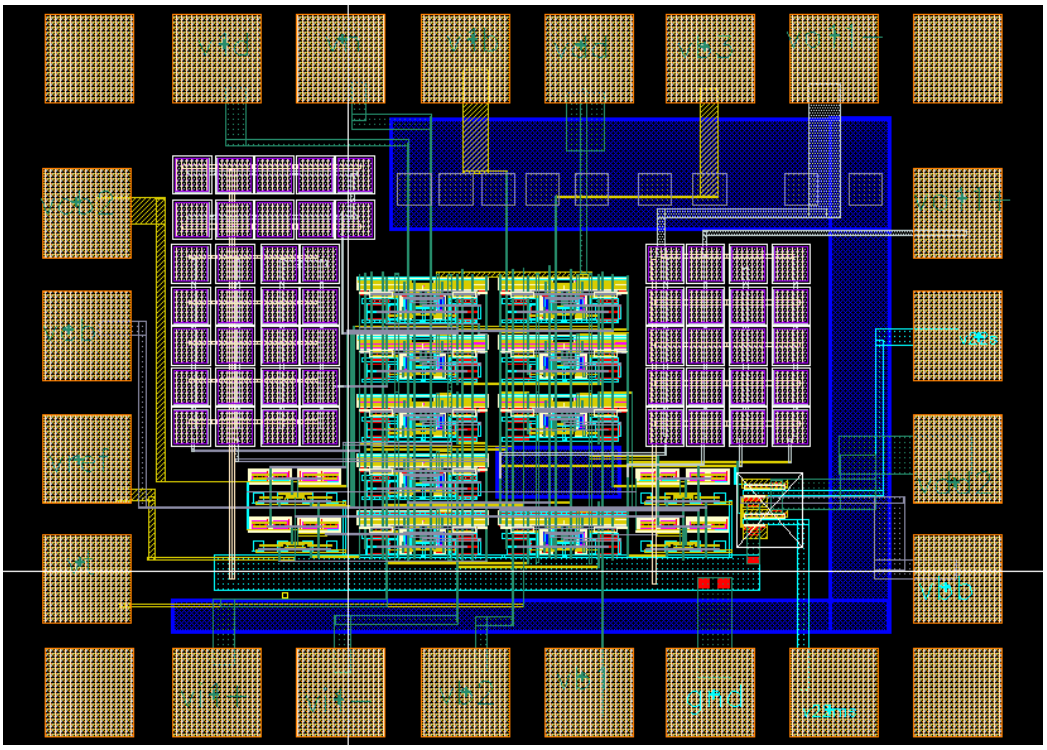


Fig 5.6 layout of the filter

5.4 measurement of the filter and OTA

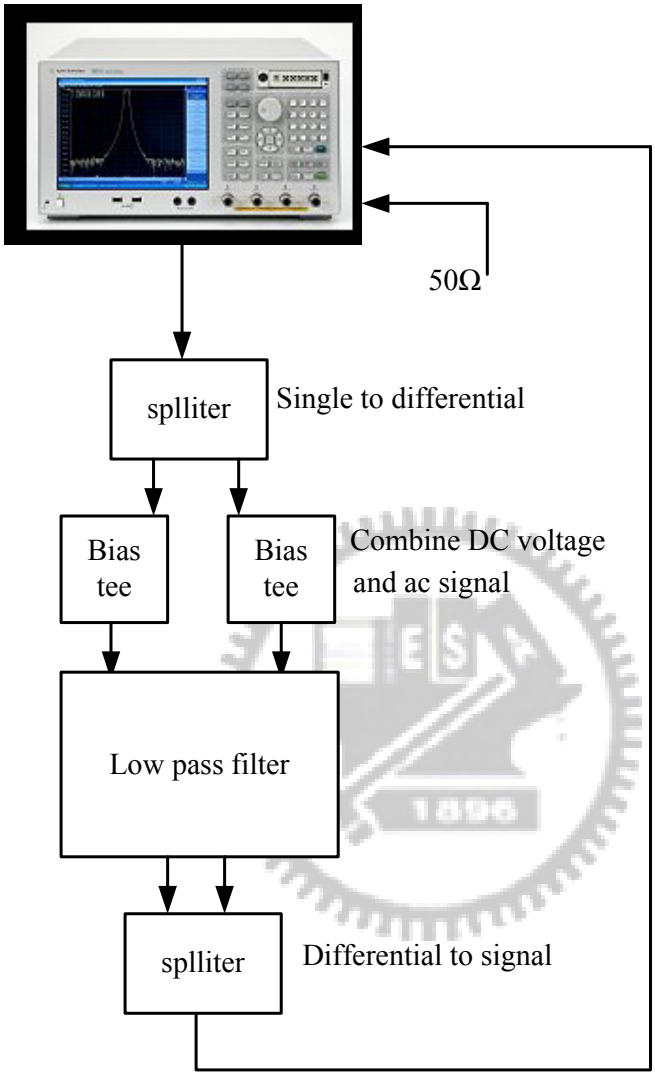
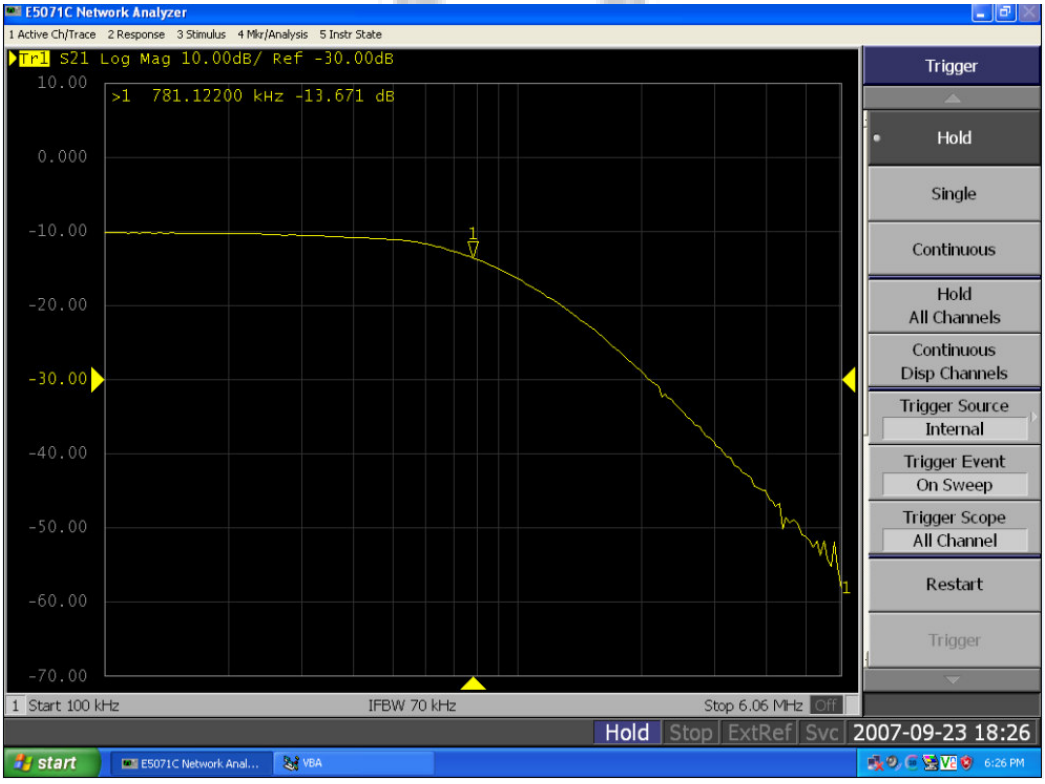


Fig 5.7block diagram of the measuring the frequency response

First of all, we have to talk about the output stage of the filter. Because of the 50Ω resistor that builds up in the instrument. The 50Ω resistor will influence the signal. The transfer function of the filter will be reduce by the 50Ω resistor. In the other words, the transfer function of the filter should be start at the 0dB if there is no 50Ω resistor. The 50Ω resistor will cause the start of the transfer function decrease and the

start of the transfer function will reach -50 dB. And the noise flow is about -60 dB. So it is hard for us to measure the correct graph of the filter. So in the output of the filter, we create a source follower with huge current to push the 50Ω resistor in the network analyzer. The mos size of the source follower should be big enough to push the 50Ω resistor. As the Fig 5.5 shown, that is the block diagram of the measuring the frequency response. We can measure S21 to get the frequency response of the filter. The splitter is used to exchange the single input signal into differential ones. And the bias tee is used to combine a DC voltage and the ac signal. And the splitter that connects at the port 2 is used to combine differential signals in a single one.



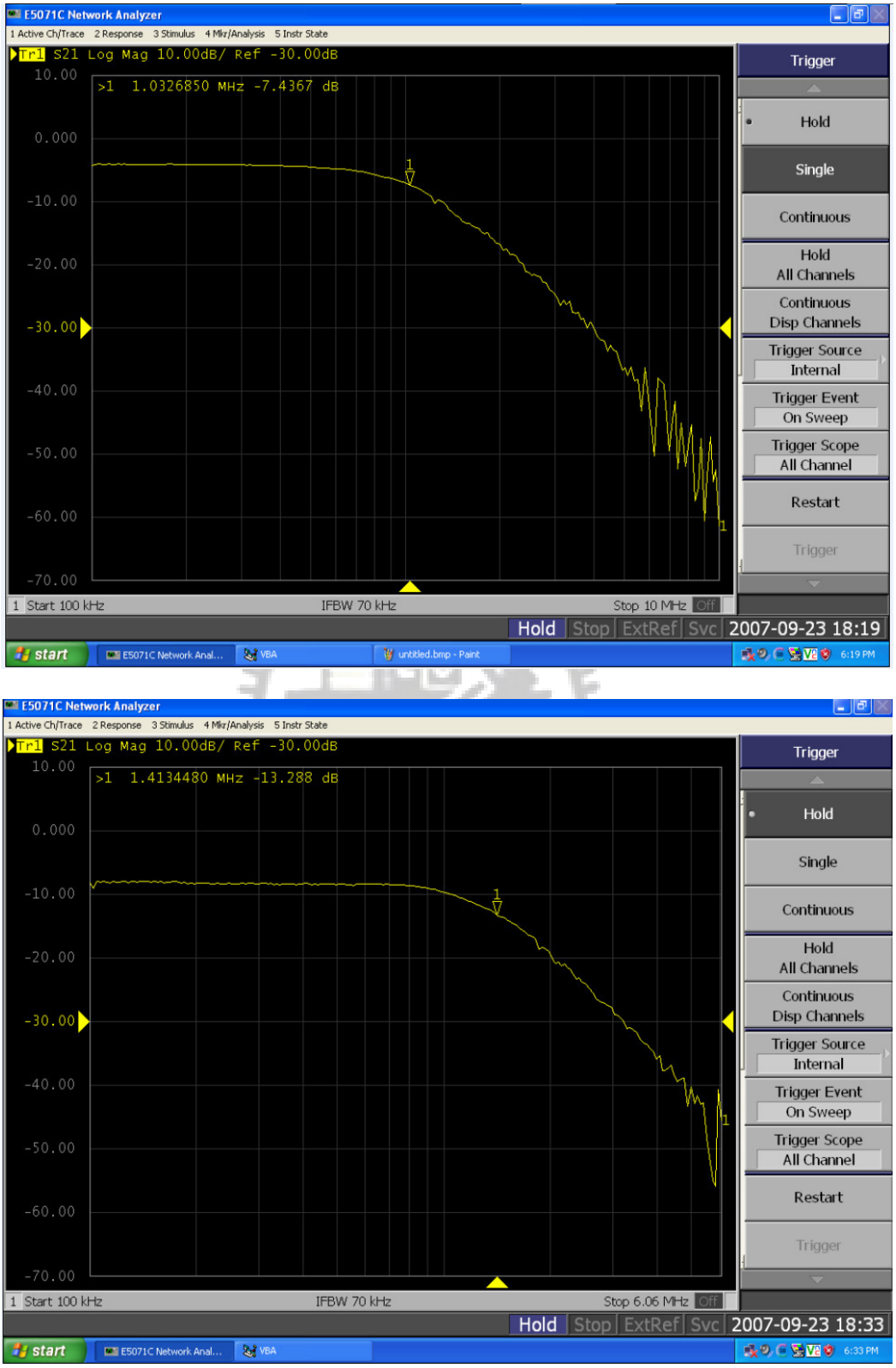


Fig5.8(a)(b)(c) differential cut off frequency of the filter

Fig 5.8(a)(b)(c) shows the differential cut off frequency of the filter. We can control

the cut off frequency of the filter by tuning the tail current of the differential pairs.

Then we will discuss the measurement of the Total Harmonic Distortion. Signal generater uses to generate the sin signal with 750 Khz 300mVpp. The splitter is used to exchange the single input signal into differential ones. And the bias tee is used to combine a DC voltage and the ac signal. And the splitter that connects at the port 2 is used to combine differential signals in a single one. And will get the THD3 of the filter.

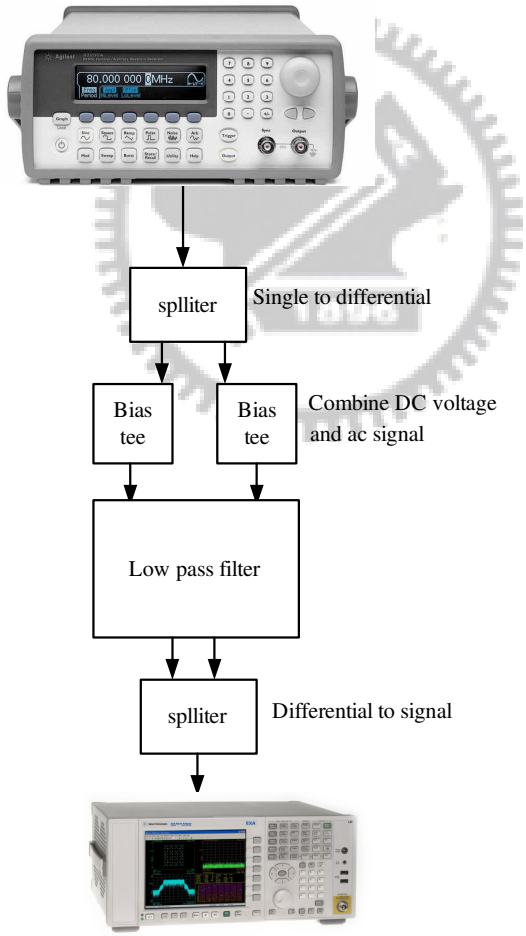


Fig 5.9 block diagram of the measuring the THD

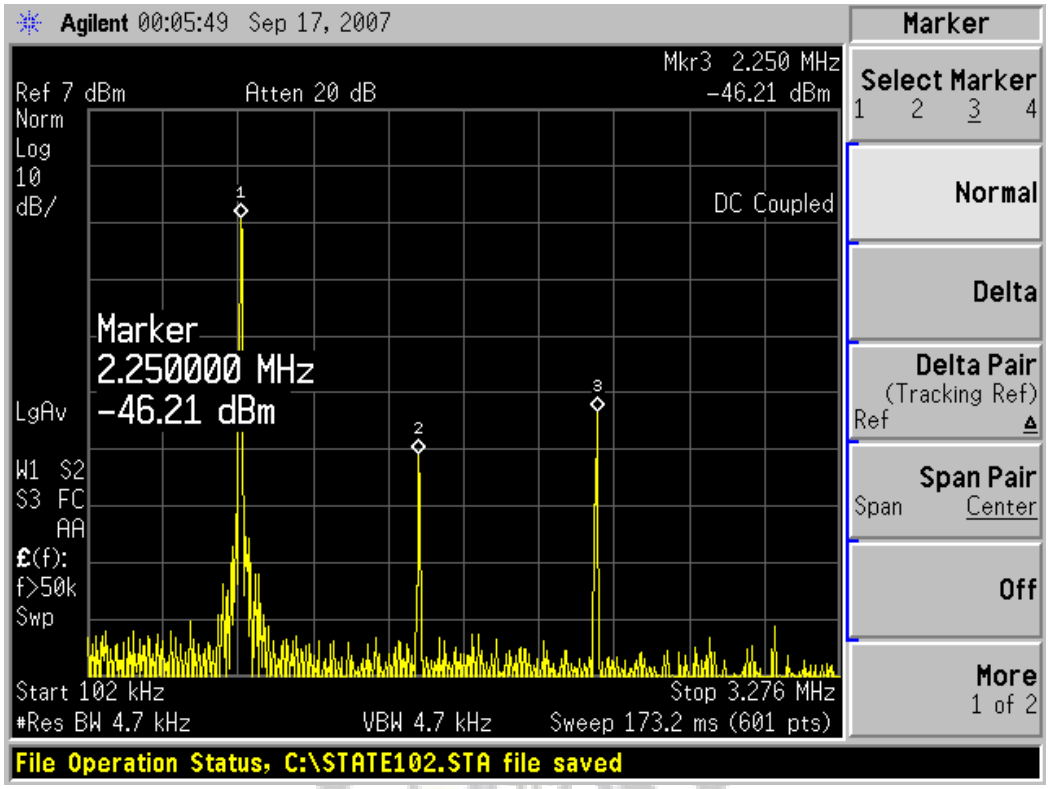


Fig 5.10 THD of the filter

In the simulation THD2 is not visiable. But the THD2 might occur because of the unsymmetrical layout. And THD3 is a little higher than the simulation result.

Finally we measure the GM of the ota. Fig5.11 shows the GM of the ota in different common-mode voltage. We find that the fluctuation of GM is small. Fig5.12 shows the different voltage of vbias2 in Fig3.1. From 5.11 and 5.12 we can find the gap in the middle of the common-mode voltage is movable. And the totle fluctuation of gm is about ±3%.

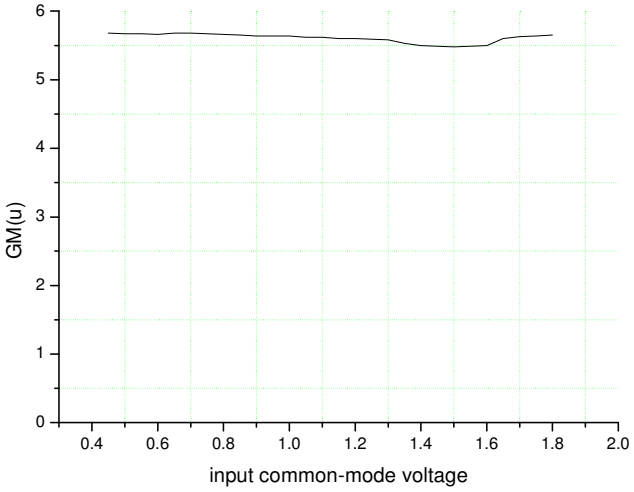


Fig 5.11 the fluctuation of GM

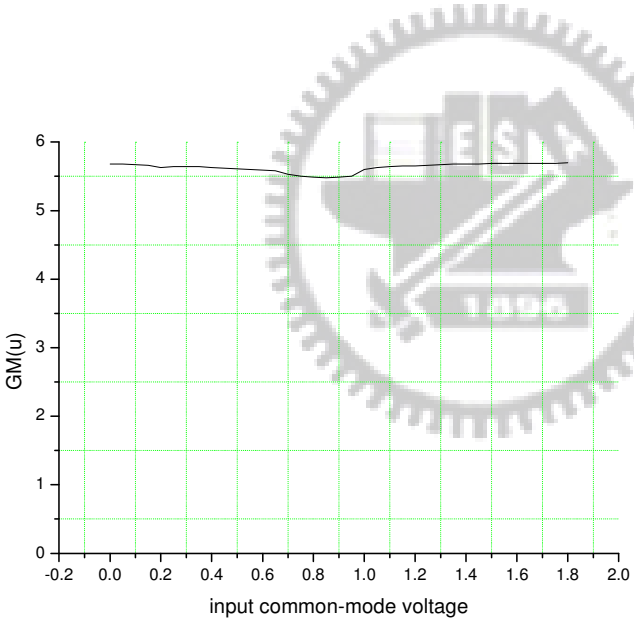


Fig 5.12 the fluctuation of GM

Chapter 6

Conclusion

A rail-to-rail input stage and a third-order Low-Pass GM-C Filter for analog applications has been presented. The proposed level-shift circuit is useful and simple. The level-shift n-channel differential pair with VCM detection circuit is used to replace the p-channel differential pair in particular situation. The fluctuation of the total transconductance is less than ± 3%. Table 6.1 shows the performance of the third order GM-C filter with rail-to-rail input stage.

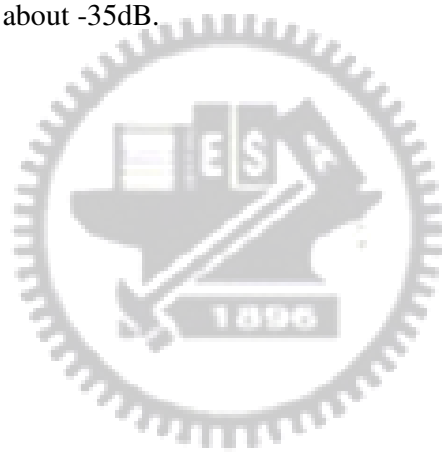
Table 6.1

Process	Tsmc0.18 CMOS
Supply voltage	1.8v
power	2-3mW
Chip area	0.24mm^2
ICMR	0-1.8
Cutoff frequency	0.75-1.5MHz
GM fluctuation	Less than 3%
THD in 750KHz 300Vpp	-35dB

Finally, we will talks about the filter. The range of the cutoff frequency is decrease

in the measurement. This might be caused by the parasitic capacitance. Moreover the tail current of the differential in the measure is hard to refinedly control. This also makes the decreasing of the cutoff frequency.

And the THD2 is much bigger than expect. This might be the mismatch of the layout. And there is another infer: the input signal that we import to the filter is already mismatch. Because of the splitter is not a prefect circuit that changes the signal into differential ones. And the cutoff frequency of the GM-C filter is 0.75MHz to 1.5MHz. The power dissipation of the GM-C filter is less than 4mW. The total harmonic distortion of the filter is about -35dB.



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