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晶圓上微波測試結構之設計與去嵌

Design and De-Embedding of On-Wafer Microwave Test Structures

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摘要

在本論文中，我們針對晶圓上元件特性分析提出一有系統的微波測試結構設計與去嵌方法。首先，一種具長度可尺寸化之雜散去嵌技術將被提出以用於矽場效電晶體的散射參數與雜訊特性分析。基於傳輸線理論與串級架構，此方法使用平面型開路、短路及穿透等標準結構來估算雜散網路對於元件特性的影響。其中，具基底遮蔽之開路與短路結構可以被用來模擬針墊的雜散效應，而穿透結構則可被用以有效率地移除位於場效電晶體閘極、汲極與源極端的內連線雜散效應。其次，一種適合用於全域元件模型化之具幾何形狀可尺寸化之雜散去嵌技術亦被提出。此方法結合了雙埠網路的串級與並聯架構，且只需一個反射與一個穿透的標準結構即可以移除場效電晶體周圍具任意長寬尺寸的饋送網路。接著，我們更將可尺寸化之雜散去嵌方法運用到製程監測結構的射頻元件特性分析方面。借助於遮蔽技術的使用，能將基底耦合效應降低並提高內連線的可尺寸化特性。最後，一通用於射頻元件特性分析與製程監測的微型化測試結構亦被提出。此一新型的佈局設計能將內連線上的電壓降減少至最低，並能防止元件遭受到電容性耦合效應。此設計分別只需用到傳統晶圓上測試結構與切割線內測試結構所佔面積的百分之三十六與四十。為驗證本研究中所提出的測試結構與去嵌技術，場效電晶體元件與相關去嵌結構均被設計並製作於標準互補式金氧半製程中，且利用雙埠微波量測系統分析至數百億赫茲頻段以上。而全波電磁模擬計算也被用來輔助測試結構的設計工作並驗證內連線的可尺寸化與網路合併特性。相較於目前工業標準的開路-短路去嵌技術，本文所提之系統化去嵌方法顯得非常節省面積與時間，且同時也保持著高準確度。而本文提出之微型化測試結構亦被證實能得到與傳統測試結構相近之射頻特性。

Design and De-Embedding of On-Wafer Microwave Test Structures

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Abstract

In this dissertation, we propose a systematic methodology of designing and de-embedding RF/microwave test structures for on-wafer device characterization. First, a length-scalable parasitic de-embedding technique for *S*-parameter and noise characterization of silicon MOSFETs is presented. Based on transmission-line theory and cascade configurations, this method uses planar open, short, and thru standards to estimate the effects of parasitic networks on the device characteristics. The substrate-shielded open and short standards can be used to simulate the probe-pad parasitics, and the thru standard can be used to efficiently remove the interconnect parasitics in gate, drain, and source terminals of the MOSFET. Second, a geometry-scalable parasitic de-embedding technique suitable for global device modeling is presented. This method combines the cascade and parallel configurations of two-port networks, and it uses only one reflect and one thru standard to remove the feeding networks with arbitrary geometry surrounding the MOS transistors. And then, we further apply the scalable de-embedding method to process monitoring test structures for RF device characterization. With the utilization of shielding technique, the substrate coupling can be reduced and the interconnect scalability can be improved. Finally, a miniature test structure for RF device characterization and process monitoring is also proposed. This new layout design can minimize the voltage drop across interconnects and can prevent the capacitive coupling to devices. It consumes only 36 % and 40 % chip area of the conventional on-wafer and in-line test structures, respectively. To validate the proposed test structures and de-embedding schemes, the MOSFETs and corresponding de-embedding structures were designed and fabricated in standard CMOS processes and characterized up to several tens of GHz with two-port microwave measurement systems. Full-wave electromagnetic simulations were also performed to design the test structures and to verify the interconnect scalability and network combinations. Compared with the industry-standard open-short method, the proposed methodology is much more area-efficient and time-saving, while still maintaining high accuracy. The RF characteristics of the proposed miniature test structure are shown to be in excellent agreement with those of the conventional ones.

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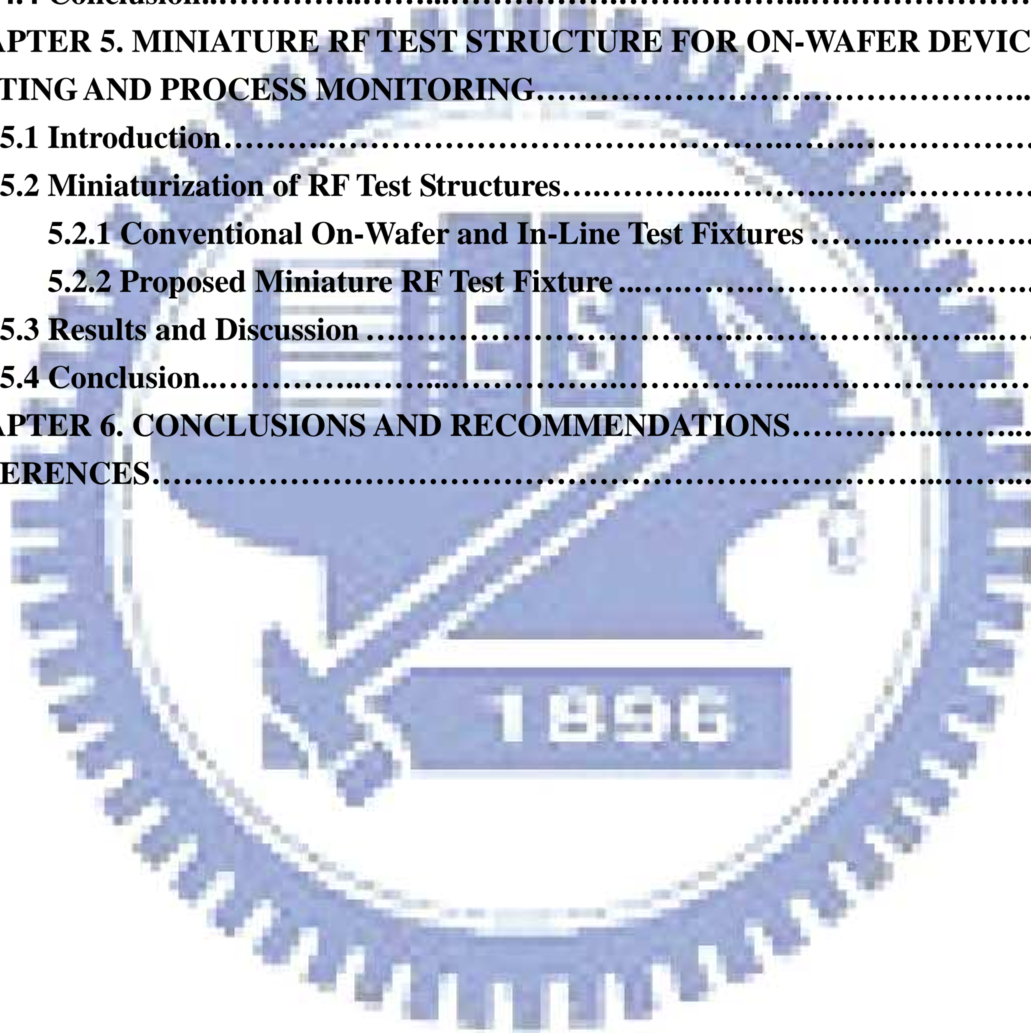

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