# CHAPTER 1. INTRODUCTION

## 1.1 Purpose of Research

With the downscaling of device channel length in the deep-submicrometer CMOS process, the accuracy of the on-wafer measuring and de-embedding techniques has become an extremely important issue for the device characterization and modeling in the RF/microwave regime. Since the fabrication of the precise 50-Ω load or well-defined 50-Ω transmission lines is still difficult in the current IC technologies, the classical calibration procedures, such as short-open-load-thru (SOLT), line-reflect-reflect-match (LRRM), and thru-reflect-line (TRL) calibrations, are impractical for the wafer-level measurements conducted on silicon substrates. For this reason, the de-embedding techniques have been frequently utilized in conjunction with the on-wafer calibration procedure to remove the unwanted parasitics. As shown in Fig. 1.1, after removing the error boxes composed of the RF test set, cables, and probes by using a ceramic impedance standard substrate (ISS), the reference planes can be shifted to the probing planes. To further obtain the intrinsic device characteristics of the device under test (DUT), the error boxes composed of the probe pads and interconnections should be subtracted by using on-wafer de-embedding standards. Although many de-embedding methods have been presented over the past years [1]-[13], most of these studies have focused on the problems of the parasitic estimation and correction.

Little research has been done to reduce the chip-area consumption and characterization time of a de-embedding procedure.

## 1.2 Review of Literature

In previous researches, several physics-based de-embedding techniques based on lumped equivalent-circuit models have been developed and extensively utilized over the years [1]-[7]. These physical equivalent-circuit models consist of probe-pad and interconnect parasitics connected in parallel-series configurations. For example, as shown in Fig. 1.2, the current industry-standard open-short de-embedding [2] uses one open and one short to reproduce and remove the admittance and impedance of the feeding networks, respectively. After de-embedding the parasitic elements in admittance ($Y$) and impedance ($Z$) domains, the external parasitic effects can be significantly reduced. However, as the device is operated at microwave frequencies and/or its interconnect length is considerable, these lumped-circuit assumptions may be invalid due to the distributed nature of the test fixtures. Recently, a de-embedding methodology based on microwave network analysis was developed to model the fixtured DUT in cascade configurations [8]. As shown in Fig. 1.3, it uses one open and two thru dummy structures to subtract the pad and interconnect parasitics and does not require any lumped circuit. The physics- and cascade-based de-embedding methods mentioned above can be used to extract the intrinsic device performance, however, they still

consume considerable chip area and testing time for parasitic extraction.

## 1.3 Major Findings and Contributions

In this dissertation, we propose a systematic methodology of designing and de-embedding microwave test structures. This proposed methodology is accurate, area-efficient, and time-saving. The main contributions of this study are summarized as follows:

1) A length-scalable de-embedding method, which combines the transmission-line theory and cascade configurations, for on-wafer *S*-parameter and noise characterization of MOS transistors is developed.
2) A novel geometry-scalable de-embedding method, which combines the cascade and parallel configurations of two-port networks, for global device modeling is proposed.
3) The application of scalable de-embedding method to process monitoring test structure for RF characterization is demonstrated, for the first time.
4) A new compact layout, which is suitable for both on-wafer testing and in-line process monitoring, is presented to reduce the chip area of RF test structures.

## 1.4 Content and Organization

To substantiate the proposed design and de-embedding schemes, the test structures

fabricated in standard CMOS technology were characterized with two-port microwave measurement systems. Moreover, full-wave electromagnetic (EM) simulations were accomplished to validate the test structures and interconnect scalability. This dissertation is composed of six chapters, and the rest of it is organized as follows. In Chapter 2, a length-scalable de-embedding method for on-wafer *S*-parameter and noise characterization of single device is developed. In Chapter 3, a geometry-scalable de-embedding method for on-wafer microwave characterization of both single and multiple devices is proposed. Chapter 4 describes the application of scalable de-embedding method to process monitoring test structure for RF device characterization. Chapter 5 presents a miniature test structure for both on-wafer testing and in-line process monitoring. Finally, Chapter 6 concludes this study.

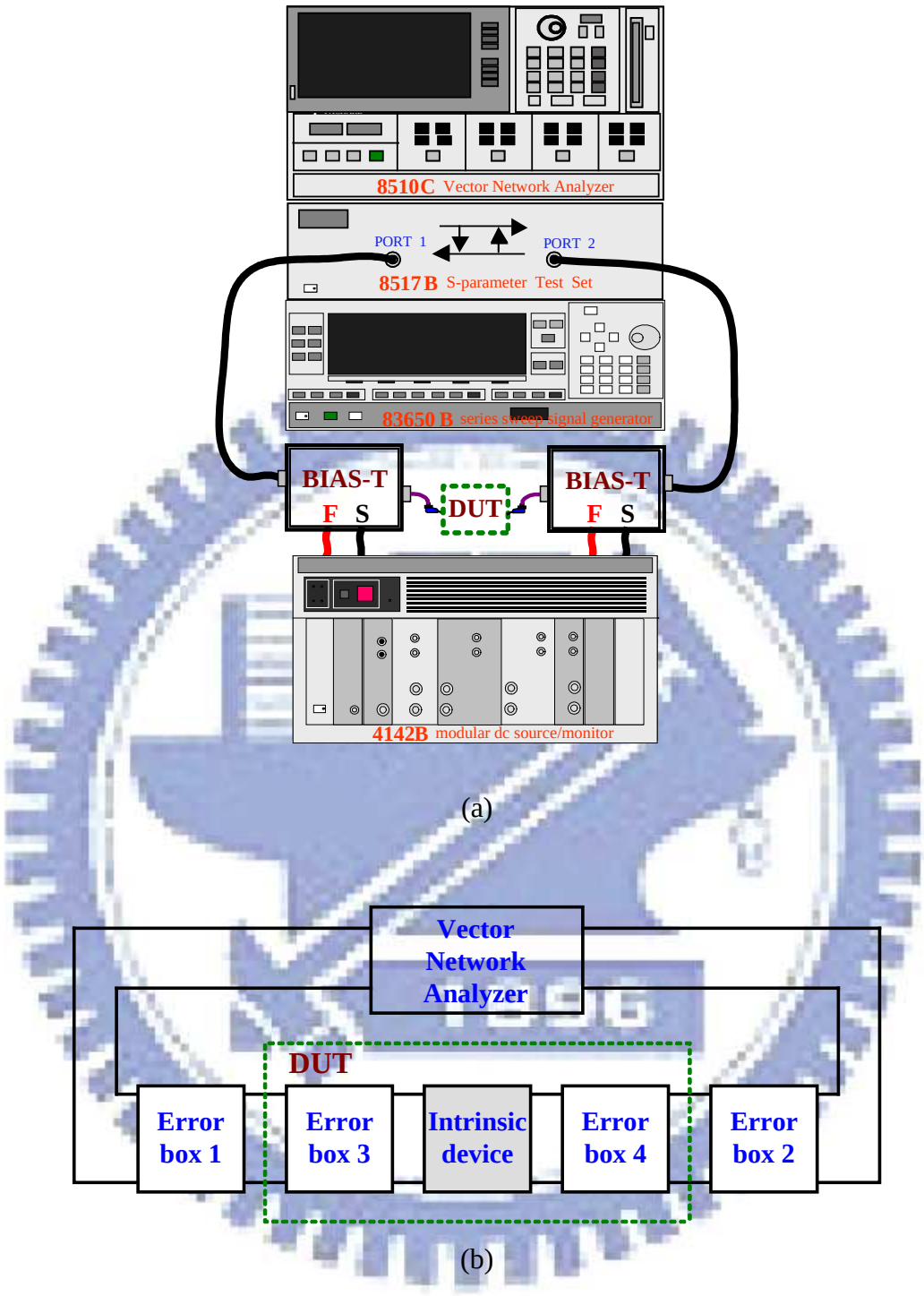
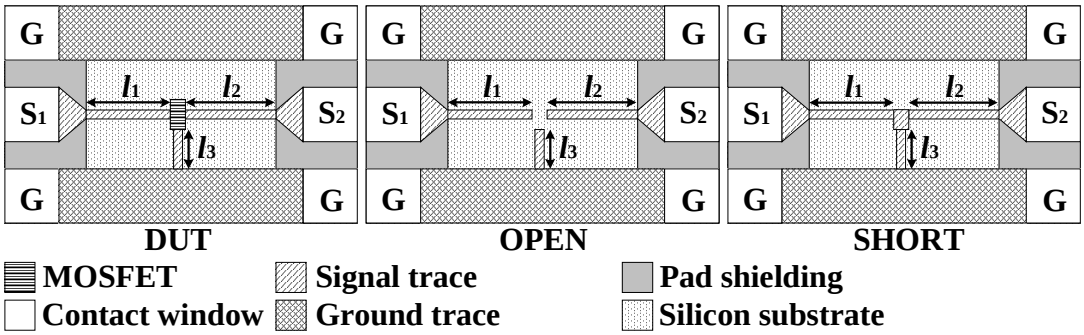



Fig. 1.1 Illustration of on-wafer *S*-parameter measurement. (a) Microwave measurement system. (b) Equivalent representation. The error boxes 1 and 2 represent the parasitic networks composed of the RF test set, cables, and probes for ports 1 and 2, respectively. The error boxes 3 and 4 represent the input/output feeding networks composed of the probe pads and interconnections of a fixtured device.

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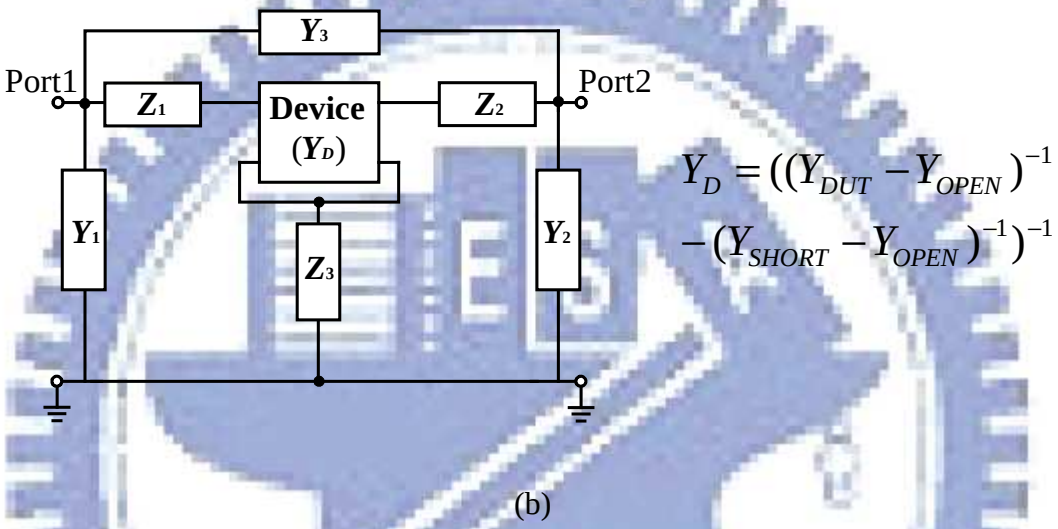


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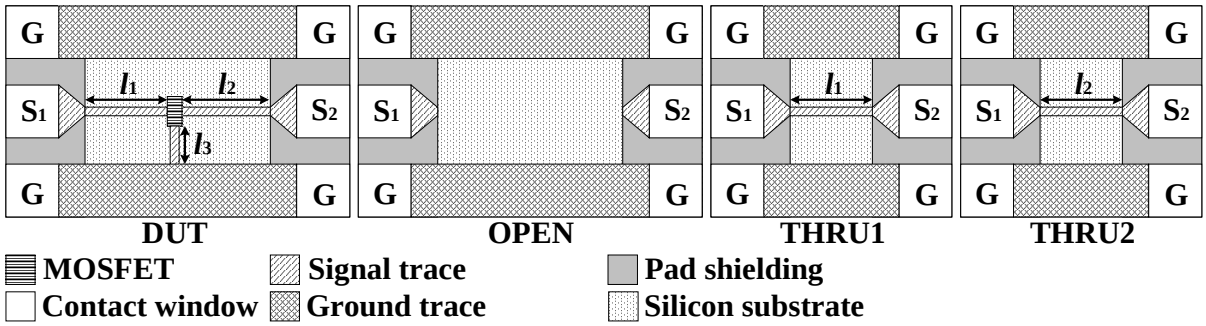
Fig. 1.2 Physics-based open-short de-embedding method [2]. (a) DUT and its corresponding dummy structures. (b) Schematic diagram.

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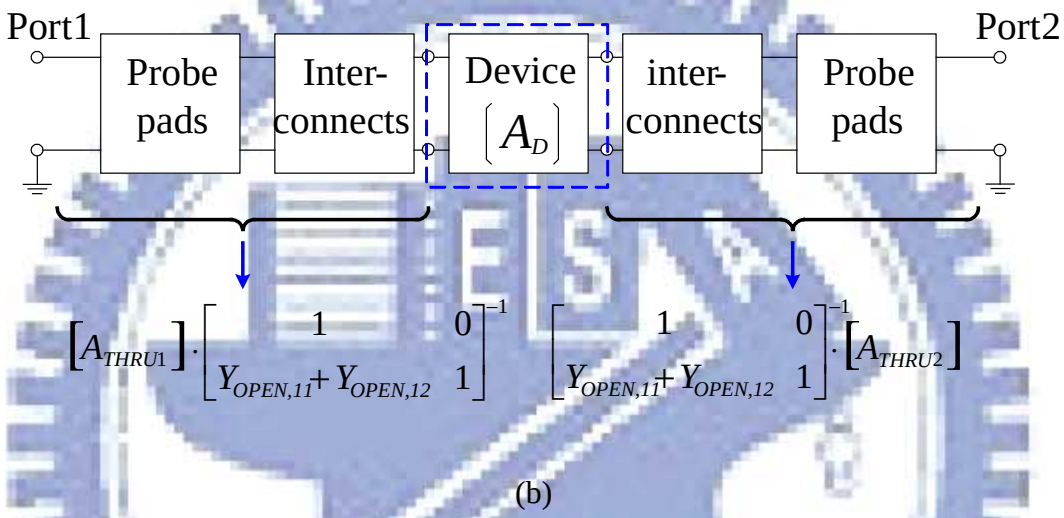



(b)

Fig. 1.3 Cascade-based de-embedding method [8]. (a) DUT and its corresponding dummy structures. (b) Schematic diagram.

# CHAPTER 2. LENGTH-SCALABLE PARASITIC DE-EMBEDDING METHOD FOR ON-WAFER MICROWAVE CHARACTERIZATION OF MOSFETS

## 2.1 Introduction

With the progress of CMOS process technology, device unity-gain frequency has reached the range from RF to millimeter-wave frequencies. For the design of silicon-based radio-frequency integrated circuits (RFICs) and monolithic microwave integrated circuits (MMICs) in future low-cost systems, on-wafer characterization of the RF/microwave devices would become an extremely important task. Since reliable device models call for precise measuring technique, the fixtured devices and corresponding de-embedding standards on silicon bulk should be carefully designed to reproduce and remove the external parasitics. In general, a three-terminal MOSFET (with its source and bulk tied together) is connected in a common-source configuration for high-frequency device characterization. Thus, its external parasitics mainly come from the probe pads, interconnects, and lossy silicon bulk. To extract the intrinsic device characteristics from microwave measurements, much research effort has been focused on this subject and several de-embedding methods have been presented over the past years. The open de-embedding method [1] was first demonstrated to remove the shunt admittance of the probe pads with an open standard. The open-short

de-embedding [2] was developed to further subtract the series impedance of the probe pads and interconnects by employing an additional short standard. Although there are other de-embedding techniques to accomplish the parasitic subtraction [3]-[7], the open-short de-embedding procedure is still the current industry standard. The physics-based de-embedding methods mentioned above utilize lumped-circuit models to simulate the external parasitics in series-shunt/shunt-series configurations. Recently, a de-embedding method based on cascade configuration [8] was presented. It uses open and thru standards to subtract the pad admittance and interconnect parasitics and does not require any lumped-circuit representation. Moreover, several efficient cascade-based de-embedding methods for *S*-parameter [9]-[11] and noise parameter measurements [12] were also developed to minimize the chip area for test fixtures.

In this chapter, we aggressively combine the physics-based and cascade-based de-embedding techniques to propose a length-scalable de-embedding method for on-wafer *S*-parameter and noise parameter characterization. With the utilization of the bulk-shielded technique [13], the open and short standards can be used to accurately remove the pad parasitics of the DUT. Based on transmission-line theory, the thru standard can be used to efficiently reproduce the interconnect parasitics in gate, drain, and source terminals of a MOSFET. To substantiate the proposed method, the MOS transistor and its corresponding de-embedding standards were fabricated using a standard CMOS technology and

characterized up to 40 GHz.

## 2.2 Length-Scalable De-Embedding Theory

### *2.2.1 On-Wafer Test Fixtures*

As illustrated in Fig. 2.1, the on-wafer test fixture is designed to mount the device with the probe pads, interconnects, and ground reference. Both DC and AC sources can be guided to the DUT through bias-T networks, cables, and probes. In general, the gate and drain of the MOS transistor are connected to input and output ports while the source and bulk are tied together to ground. Here we introduce the shielding technique to prevent the bulk leakage and port-to-port coupling [13]. It should be noted that the interconnects do not employ shielding layer for more general discussion. The shielded open and short standards can be used to accurately simulate the parasitics of the probe pads. After taking away the pad parasitics of the thru standard, the per-unit-length transmission-line parameters can be extracted to reproduce and de-embed the interconnect parasitics in gate, drain, and source terminals of a MOSFET.

### *2.2.2 Fixture Modeling and Scaling*

To de-embed the unwanted parasitics of the DUT, the parasitic networks composed of pad and interconnect elements should be precisely reproduced from the open, short, and thru standards. Fig. 2.2(a) exhibits the semi-distributed model for the fixtured MOSFET. Here the

shielding technique is employed to improve the scalability of probe-pads [13]. The probe-pad parasitics, which include the shunt admittance and series impedance, can be evaluated from the open and short standards shown in Figs. 2.2(b)-(c). The chain scattering matrices of the probe-pad parasitics in port 1 and port 2 are

$$[T_{PAD1}] = [T_{OPEN1}][T_{SHORT1}] \tag{2.1}$$

$$[T_{PAD2}] = [T_{SHORT2}][T_{OPEN2}] \tag{2.2}$$

where

$$[T_{OPENi}] = \begin{bmatrix} \frac{3+S_{OPEN,iim}}{2+2S_{OPEN,iim}} & \frac{1-S_{OPEN,iim}}{2+2S_{OPEN,iim}} \\ \frac{-1+S_{OPEN,iim}}{2+2S_{OPEN,iim}} & \frac{1+3S_{OPEN,iim}}{2+2S_{OPEN,iim}} \end{bmatrix}, \quad i = 1, 2 \tag{2.3}$$

$$[T_{SHORTi}] = \begin{bmatrix} \frac{3-S_{SHORT,ii}}{2-2S_{SHORT,ii}} & \frac{-1-S_{SHORT,ii}}{2-2S_{SHORT,ii}} \\ \frac{1+S_{SHORT,ii}}{2-2S_{SHORT,ii}} & \frac{1-3S_{SHORT,ii}}{2-2S_{SHORT,ii}} \end{bmatrix}, \quad i = 1, 2 \tag{2.4}$$

$$S_{SHORT,ii} = \frac{1-S_{OPEN,iim}+3S_{SHORT,iim}+S_{OPEN,iim}S_{SHORT,iim}}{1+3S_{OPEN,iim}-S_{SHORT,iim}+S_{OPEN,iim}S_{SHORT,iim}}, \quad i = 1, 2. \tag{2.5}$$

It should be mentioned that $S_{OPEN,iim}$ and $S_{SHORT,iim}$ are the measured reflection coefficients at port $i$ of the open and short standards, respectively.

As shown in Fig. 2.2(d), the thru standard can be modeled as the probe pads and interconnect in cascade connection. Consequently, the intrinsic interconnect characteristics can be expressed as

$$[T_{INT}] = [T_{PAD1}]^{-1}[T_{THRU}][T_{PAD2}]^{-1} \tag{2.6}$$

where $[T_{INT}]$ and $[T_{THRU}]$ are the chain scattering matrices of the intrinsic interconnect and thru standard, respectively. Converting the chain scattering matrix $[T_{INT}]$ to scattering matrix $[S_{INT}]$, the characteristic impedance $Z_C$ and the propagation constant γ of the intrinsic interconnect can be calculated using [14]

$$Z_C = \pm Z_0 \sqrt{\frac{(1+S_{INT,11})^2 - (S_{INT,21})^2}{(1-S_{INT,11})^2 - (S_{INT,21})^2}} \tag{2.7}$$

and

$$\gamma = \frac{1}{l}\ln\left(\frac{1-(S_{INT,11})^2 + (S_{INT,21})^2}{2S_{INT,21}} \pm \Delta\right) \tag{2.8}$$

where $Z_0$ is the impedance of the of the network analyzer, $l$ is the interconnect length, and

$$\Delta = \left(\frac{(1-(S_{INT,21})^2 + (S_{INT,11})^2)^2 - (2S_{INT,11})^2}{(2S_{INT,21})^2}\right)^{\frac{1}{2}}. \tag{2.9}$$

Based on the above results, the interconnect parasitics with arbitrary line length ($l_1$, $l_2$, and $l_3$ in Fig.2.1) of a fixtured MOSFET can be efficiently reproduced from the chain scattering matrix of a lossy transmission line

$$[T_{INTi}] = \begin{bmatrix} \frac{e^{\gamma l_i} - e^{-\gamma l_i}\Gamma^2}{1-\Gamma^2} & \frac{(e^{\gamma l_i} - e^{-\gamma l_i})\Gamma}{1-\Gamma^2} \\ \frac{(e^{-\gamma l_i} - e^{\gamma l_i})\Gamma}{1-\Gamma^2} & \frac{(1-\Gamma^2)^2 - (e^{\gamma l_i} - e^{-\gamma l_i})^2\Gamma^2}{(1-\Gamma^2)(e^{\gamma l_i} - e^{-\gamma l_i}\Gamma^2)} \end{bmatrix}, \; i = 1, 2, 3 \tag{2.10}$$

where $\Gamma = (Z_0 - Z_C)/(Z_0 + Z_C)$.

### *2.2.3 S-Parameter De-Embedding Theory*

The main procedure for the proposed scalable *S*-parameter de-embedding is illustrated in Fig. 2.3. Once the interconnect parasitics are calculated, the parasitic networks surrounding a fixtured MOSFET can be expressed as

$$[T^1] = [T_{OPEN1}][T_{SHORT1}][T_{INT1}] \tag{2.11}$$

$$[T^2] = [T_{OPEN2}][T_{SHORT2}][T_{INT2}] \tag{2.12}$$

$$[T^3] = [T_{INT3}]. \tag{2.13}$$

And then, the chain scattering matrices $[T^1]$, $[T^2]$, and $[T^3]$ can be converted to their scattering matrices $[S^1]$, $[S^2]$, and $[S^3]$. We can now apply microwave network theory to shift the reference planes to the terminal planes of the intrinsic device network. The detailed de-embedding procedure is summarized as follows:

5) Subtract the parasitic networks in input and output ports ($[S^1]$ and $[S^2]$) using

$$[S''] = ([G] \cdot ([S'] - [E])^{-1} \cdot [F] + [H])^{-1} \tag{2.14}$$

where $[S']$ is the measured two-port scattering matrix of the DUT, and $[E]$, $[F]$, $[G]$, and $[H]$ are the diagonal matrices defined as

$$[E] = diag(S_{11}^1, S_{11}^2) \tag{2.15}$$

$$[F] = diag(S_{12}^1, S_{12}^2) \tag{2.16}$$

$$[G] = diag(S_{21}^1, S_{21}^2) \tag{2.17}$$

$$[H] = diag(S_{22}^1, S_{22}^2). \tag{2.18}$$

6) Convert the two-port scattering matrix [$S''$] to three-port scattering matrix [$S'''$] using [15]

$$[S'''] = \begin{bmatrix} S_{11}'' + \frac{\kappa_{11}\kappa_{12}}{4-\kappa} & S_{12}'' + \frac{\kappa_{11}\kappa_{21}}{4-\kappa} & \frac{2\kappa_{11}}{4-\kappa} \\ S_{21}'' + \frac{\kappa_{22}\kappa_{12}}{4-\kappa} & S_{22}'' + \frac{\kappa_{22}\kappa_{21}}{4-\kappa} & \frac{2\kappa_{22}}{4-\kappa} \\ \frac{2\kappa_{12}}{4-\kappa} & \frac{2\kappa_{21}}{4-\kappa} & \frac{\kappa}{4-\kappa} \end{bmatrix} \tag{2.19}$$

where $\kappa = S_{11}'' + S_{12}'' + S_{21}'' + S_{22}''$, $\kappa_{11} = 1 - S_{11}'' - S_{12}''$, $\kappa_{12} = 1 - S_{11}'' - S_{21}''$, $\kappa_{21} = 1 - S_{22}'' - S_{12}''$, $\kappa_{22} = 1 - S_{22}'' - S_{21}''$.

7) Subtract the remaining parasitic networks from the source terminal using

$$[S] = ([G'] \cdot ([S'''] - [E'])^{-1} \cdot [F'] + [H'])^{-1} \tag{2.20}$$

where [$S$] is the de-embedded three-port scattering matrix of the DUT, and [$E'$], [$F'$], [$G'$], and [$H'$] are the diagonal matrices defined as

$$[E'] = diag(0,0,S_{11}^3) \tag{2.21}$$

$$[F'] = diag(1,1,S_{12}^3) \tag{2.22}$$

$$[G'] = diag(1,1,S_{21}^3) \tag{2.23}$$

$$[H'] = diag(0,0,S_{22}^3). \tag{2.24}$$

8) Convert the de-embedded three-port scattering matrix [$S$] to two-port scattering matrix [$S^D$] using [15]

$$[S^D] = \begin{bmatrix} S_{11} - \frac{S_{13}S_{31}}{1+S_{33}} & S_{12} - \frac{S_{13}S_{32}}{1+S_{33}} \\ S_{21} - \frac{S_{23}S_{31}}{1+S_{33}} & S_{22} - \frac{S_{23}S_{32}}{1+S_{33}} \end{bmatrix}. \tag{2.25}$$

### *2.2.4 Noise Parameter De-Embedding Theory*

Figure 2.4 shows the test structures and suggested model for line-scalable noise de-embedding. The *ABCD* matrices of the probe pads are

$$[A_{PAD1}]=\begin{bmatrix} 1 & Z_{PAD} \\ Y_{PAD} & 1+Y_{PAD}Z_{PAD} \end{bmatrix}, \tag{2.26}$$

and

$$[A_{PAD2}]=\begin{bmatrix} 1+Y_{PAD}Z_{PAD} & Z_{PAD} \\ Y_{PAD} & 1 \end{bmatrix}. \tag{2.27}$$

It should be noted that $Y_{PAD} = Y_{OPEN,11}$ and $Z_{PAD} = Z_{SHORTD}$, where $Z_{SHORTD} = (Y_{SHORT,11} - Y_{OPEN,11})^{-1}$, and $[Y_{OPEN}]$ and $[Y_{SHORT}]$ are the *Y*-parameters of the open and short converted from the *S*-parameter measurements. The thru dummy can be modeled as the probe pads and interconnect in cascade connection and its pad parasitics can be de-embedded using $[A_{INT}] = [A_{PAD1}]^{-1}[A_{THRU}][A_{PAD2}]^{-1}$, where the superscript "–1" denotes the inverse of the matrix, and $[A_{INT}]$ and $[A_{THRU}]$ are the *ABCD* matrices of the intrinsic interconnect and thru dummy, respectively. Consequently, the scalable interconnect parameters, such as characteristic impedance $Z_C$ and propagation constant γ, can be evaluated as in [14]. Based on the above results, the parasitic effects of the input/output interconnects and dangling leg with arbitrary line length ($l_1$, $l_2$, and $l_g$) of a fixtured MOSFET can be efficiently reproduced from the *ABCD* matrices of a lossy transmission line

$$[A_{INTi}]=\begin{bmatrix} \cosh\gamma l_i & Z_C \sinh\gamma l_i \\ \frac{1}{Z_C}\sinh\gamma l_i & \cosh\gamma l_i \end{bmatrix}, \; i = 1, 2, g. \tag{2.28}$$

The proposed noise de-embedding procedure is detailed as follows.

1) Measure the *S*-parameters $[S_{DUT}]$, $[S_{OPEN}]$, $[S_{SHORT}]$, and $[S_{THRU}]$ of the DUT, open, short,

and thru, respectively.

2) Measure the noise parameters $NF_{min}^{DUT}$, $R_n^{DUT}$, and $Y_{opt}^{DUT}$ of the DUT and calculate the correlation matrix $[C_A^{DUT}]$ as in [16].

3) Convert $[S_{OPEN}]$ and $[S_{SHORT}]$ to their *Y*-matrices $[Y_{OPEN}]$ and $[Y_{SHORT}]$, respectively, and calculate the *ABCD* matrices $[A_{PAD1}]$ and $[A_{PAD2}]$ of RF pads from (2.26) and (2.27).

4) Extract the intrinsic interconnect parameters using $[A_{INT}] = [A_{PAD1}]^{-1}[A_{THRU}][A_{PAD2}]^{-1}$ and calculate the interconnect characteristic impedance $Z_C$ and propagation constant $\gamma$ as in [14].

5) Calculate the *ABCD* matrices $[A_{INT1}]$, $[A_{INT2}]$, and $[A_{INTg}]$ of the interconnects and dangling leg as in (2.28).

6) Calculate the *ABCD* matrices $[A_{IN}]$ and $[A_{OUT}]$, which are respectively the parasitic networks at input and output ports, from $[A_{IN}] = [A_{PAD1}]\,[A_{INT1}]$ and $[A_{OUT}] = [A_{INT2}]\,[A_{PAD2}]$.

7) Convert $[S_{DUT}]$ to its *ABCD* matrix $[A_{DUT}]$ and calculate the *ABCD* matrix $[A_D]$ of the MOSFET with dangling leg using $[A_D] = [A_{IN}]^{-1}\,[A_{DUT}]\,[A_{OUT}]^{-1}$.

8) Convert $[A_D]$ and $[A_{INTg}]$ to *Z*-matrix $[Z_D]$ and *Y*-matrix $[Y_{INTg}]$, respectively.

9) Calculate the *Z*-matrix $[Z_{MOS}]$ of the MOSFET without dangling leg from $[Z_{MOS}] = [Z_D] - [Z_{LEG}]$, where $[Z_{LEG}]$ is

$$[Z_{LEG}] = \begin{bmatrix} 1/Y_{INTg,11} & 1/Y_{INTg,11} \\ 1/Y_{INTg,11} & 1/Y_{INTg,11} \end{bmatrix}. \tag{2.29}$$

10) Convert $[Z_{MOS}]$ to $[A_{MOS}]$, where $[A_{MOS}]$ is the *ABCD* matrix of the intrinsic MOSFET.

11) Convert $[A_{IN}]$ and $[A_{OUT}]$ to their impedance matrices $[Z_{IN}]$ and $[Z_{OUT}]$, respectively.

12) Calculate the noise correlation matrices $[C_Z^{IN}]$, $[C_Z^{OUT}]$, and $[C_Z^{LEG}]$ from $[C_Z^{IN}] = 2kT\mathrm{Re}([Z_{IN}])$, $[C_Z^{OUT}] = 2kT\mathrm{Re}([Z_{OUT}])$, and $[C_Z^{LEG}] = 2kT\mathrm{Re}([Z_{LEG}])$.

13) Convert $[C_Z^{IN}]$ and $[C_Z^{OUT}]$ to their chain matrices $[C_A^{IN}]$ and $[C_A^{OUT}]$ using $[C_A^{IN}] = [T^{IN}]$ $[C_Z^{IN}]$ $[T^{IN}]^H$ and $[C_A^{OUT}] = [T^{OUT}]$ $[C_Z^{OUT}]$ $[T^{OUT}]^H$, where the superscript "*H*" denotes the Hermitian conjugate of the matrix, and $[T^{IN}]$ and $[T^{OUT}]$ are the transformation matrices [16].

14) Calculate the correlation matrix $[C_A^D]$ of the MOSFET with dangling leg as $[C_A^D] = [A_{IN}]^{-1}([C_A^{DUT}] - [C_A^{IN}])([A_{IN}]^H)^{-1} - [A_D][C_A^{OUT}][A_D]^H$ [8].

15) Convert $[C_A^D]$ to its impedance representation $[C_Z^D]$ using $[C_Z^D] = [T^D]$ $[C_A^D]$ $[T^D]^H$, where $[T^D]$ is the transformation matrix [16].

16) Calculate the correlation matrix $[C_Z^{MOS}]$ of the MOSFET without dangling leg as $[C_Z^{MOS}] = [C_Z^D] - [C_Z^{LEG}]$.

17) Convert $[C_Z^{MOS}]$ to its chain matrix $[C_A^{MOS}]$ using $[C_A^{MOS}] = [T^{MOS}]$ $[C_Z^{MOS}]$ $[T^{MOS}]^H$, where $[T^{MOS}]$ is the transformation matrix [16].

18) Calculate the intrinsic noise parameters $NF_{min}$, $R_n$, and $Y_{opt}$ from the noise correlation matrix $[C_A^{MOS}]$ using

$$NF_{\min} = 1 + \frac{1}{kT}\left(\mathrm{Re}(C_{A12}^{MOS}) + \sqrt{C_{A11}^{MOS}C_{A22}^{MOS} - (\mathrm{Im}(C_{A12}^{MOS}))^2}\right) \tag{2.30}$$

$$R_n = \frac{C_{A11}^{MOS}}{2kT} \tag{2.31}$$

and

$$Y_{opt} = \frac{\sqrt{C_{A11}^{MOS} C_{A22}^{MOS} - (\mathrm{Im}(C_{A12}^{MOS}))^2} + j\,\mathrm{Im}(C_{A12}^{MOS})}{C_{A11}^{MOS}} \tag{2.32}$$

## 2.3 Results and Discussion

To validate the length-scalable de-embedding theory, the DUT and its corresponding de-embedding structures were fabricated using a standard five-metal-layer CMOS process. The NMOS transistor with the dimensions of channel length ($L_g$) = 0.24 μm and channel width ($W_g$) = 160 μm (5 μm × 32 fingers) was connected in a two-port ground-signal-ground (GSG) configuration. The lengths of the 10-μm wide interconnects between the probe pads and the transistor are $l_1$ = $l_2$ = 50 μm and $l_3$ = 42 μm. The on-wafer noise and *S*-parameter measurements were accomplished with an ATN NP5B Noise Parameter Measurement System, and an Agilent 8510C Vector Network Analyzer (VNA), respectively. The SOLT procedure was used to calibrate the measurement systems.

### *2.3.1 S-Parameter Characterization*

Figure 2.5(a) shows the resistance and inductance of short standards, and Fig. 2.5(b) shows the conductance and capacitance of open standards extracted as

$$R_{PAD} = \mathrm{Re}(Z_{PAD}) \tag{2.33}$$

$$L_{PAD} = \mathrm{Im}(Z_{PAD})/\omega \tag{2.34}$$

$$G_{PAD} = \mathrm{Re}(Y_{PAD}) \tag{2.35}$$

$$C_{PAD} = \mathrm{Im}(Y_{PAD}) / \omega \tag{2.36}$$

where $\omega$ is the angular frequency. Here we compare the small test fixtures to the large ones, which are respectively typical for active and passive device characterization, to examine the scalability of probe pads. The open and short standards show approximately identical pad admittance and impedance over a wide range of frequency, respectively. These results indicate that the capacitive coupling and conductive leakage between the two ports of open and short standards can be neglected, and also the fixture size can be reduced to 100 um (or even less) by employing the grounded metal shield. Then, the shielded open and short standards can be used to accurately subtract the probe-pad parasitics of both thru standard and DUTs. Figure 2.6 shows the interconnect parameters as functions of frequency calculated from the *S*-parameter measurements based on transmission-line theory [14]

$$R_{INT} = \mathrm{Re}(\gamma Z_C) \tag{2.37}$$

$$L_{INT} = \mathrm{Im}(\gamma Z_C) / \omega \tag{2.38}$$

$$G_{INT} = \mathrm{Re}(\gamma / Z_C) \tag{2.39}$$

$$C_{INT} = \mathrm{Im}(\gamma / Z_C) / \omega . \tag{2.40}$$

The interconnect parameters are extracted from thru standards using the conventional scalable de-embedding method [9] and the proposed method, respectively. Here the interconnect length of small thru standards is set to 200 μm to mitigate the effects of forward

coupling on short interconnects [9]. As shown in Fig. 2.6(a), the per-unit-length resistance and inductance de-embedded using the scalable de-embedding method exhibit higher values over that using the proposed method. Figure 2.6(b) shows that both the conductance and capacitance display close results. Besides, the per-unit-length resistance and inductance of small and large thru standards de-embedded using the proposed method are in good agreement. It is because the proposed method introduces the short standard to further takes into account the resistance and inductance of the probe pads, which are neglected in the conventional cascade-based de-embedding methods [8]-[12]. Accordingly, the proposed method can be used to accurately extract the interconnect parameters for scalable parasitic de-embedding. When frequency enters the millimeter-wave regime, the scalability of thru standard, especially the per-unit-length conductance, becomes worse while the scalability of open and short standards still remains good. This issue is mainly due to the lossy silicon network and can be improved by employing the shielding technique [13]. However, care must be taken to prevent the electromagnetic coupling from device to the shielding plane.

Figures 2.7 and 2.8 demonstrate the magnitudes and angles of two-port *S*-parameters for the fixtured MOSFET biased at $V_{DS}$ = 2 V and $V_{GS}$ = 1.065 V ($I_{DS}$ = 20 mA), respectively. These results are de-embedded using standard open-short de-embedding [2], conventional scalable de-embedding methods [9], [11], and proposed method. As the operation frequency increases, the raw measurements tend to deviate from the de-embedded results. The parasitic

effects on device characteristics are considerable, especially at high frequencies, and should be appropriately removed. The scalable method [9] considers only the effects of pad admittance and interconnect parasitics in input (gate) and output (drain) ports and this assumption results in a significant inaccuracy. The scalable method [11] further subtracts the interconnect parasitics in grounded (source) port and thus substantially improve the de-embedding accuracy As we discussed in previous subsection, the proposed method can extract the probe-pad parasitics and interconnect parameters more precisely than the conventional scalable de-embedding methods [9], [11] do by employing an additional short standard. Consequently, as shown in Figs. 2.7 and 2.8, the proposed method shows the best consistency between itself and the industry-standard open-short method.

### *2.3.2 Noise Parameter Characterization*

Figure 2.9 shows the measured and de-embedded noise parameters as a function of frequency. These results indicate that the intrinsic noise parameters obtained from the proposed method also agree well with those from the standard open-short method. They also demonstrate the parasitics of the dangling leg can affect the noise characteristics of a MOS transistor, especially for equivalent noise resistance ($R_n$) and optimized input reflection coefficient ($\Gamma_{opt}$) at higher frequencies.

Based on the above results, the proposed line-scalable de-embedding method can be used to efficiently and accurately extract the intrinsic characteristics of the MOSFETs.

## 2.4 Conclusion

In this chapter, a length-scalable *S*-parameter and noise de-embedding method for two-port on-wafer MOSFET characterization has been presented and verified. The proposed method combines the physics-based and cascade-based de-embedding techniques to comprehensively model the parasitic networks surrounding a fixtured MOS transistor. The substrate-shielded open and short standards are used to subtract the pad parasitics and the thru standard is used to subtract the interconnect parasitics in gate, drain, and source terminals of the MOSFET. Both the fixture scalability of de-embedding standards and the de-embedding accuracy are validated up to 40 GHz. The de-embedded results substantiate that the proposed method is accurate and efficient for characterizing the silicon-based devices.

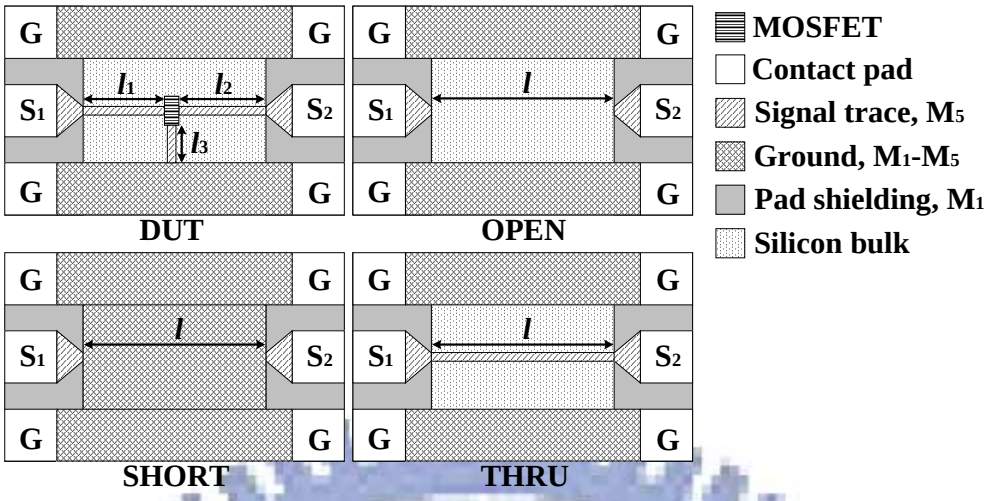



Fig. 2.1 Illustration of the on-wafer fixtured device and corresponding de-embedding standards for length-scalable de-embedding method.

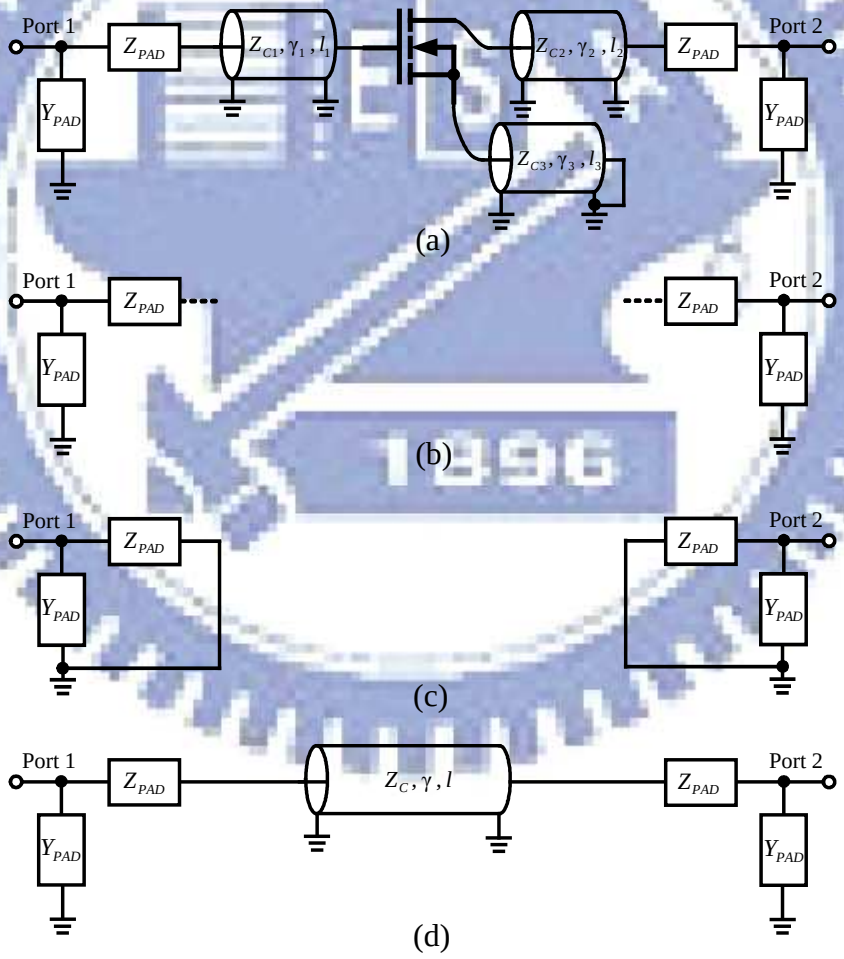



Fig. 2.2 Suggested parasitic models for the on-wafer test structures. (a) DUT. (b) Open standard. (c) Short standard. (d) Thru standard.

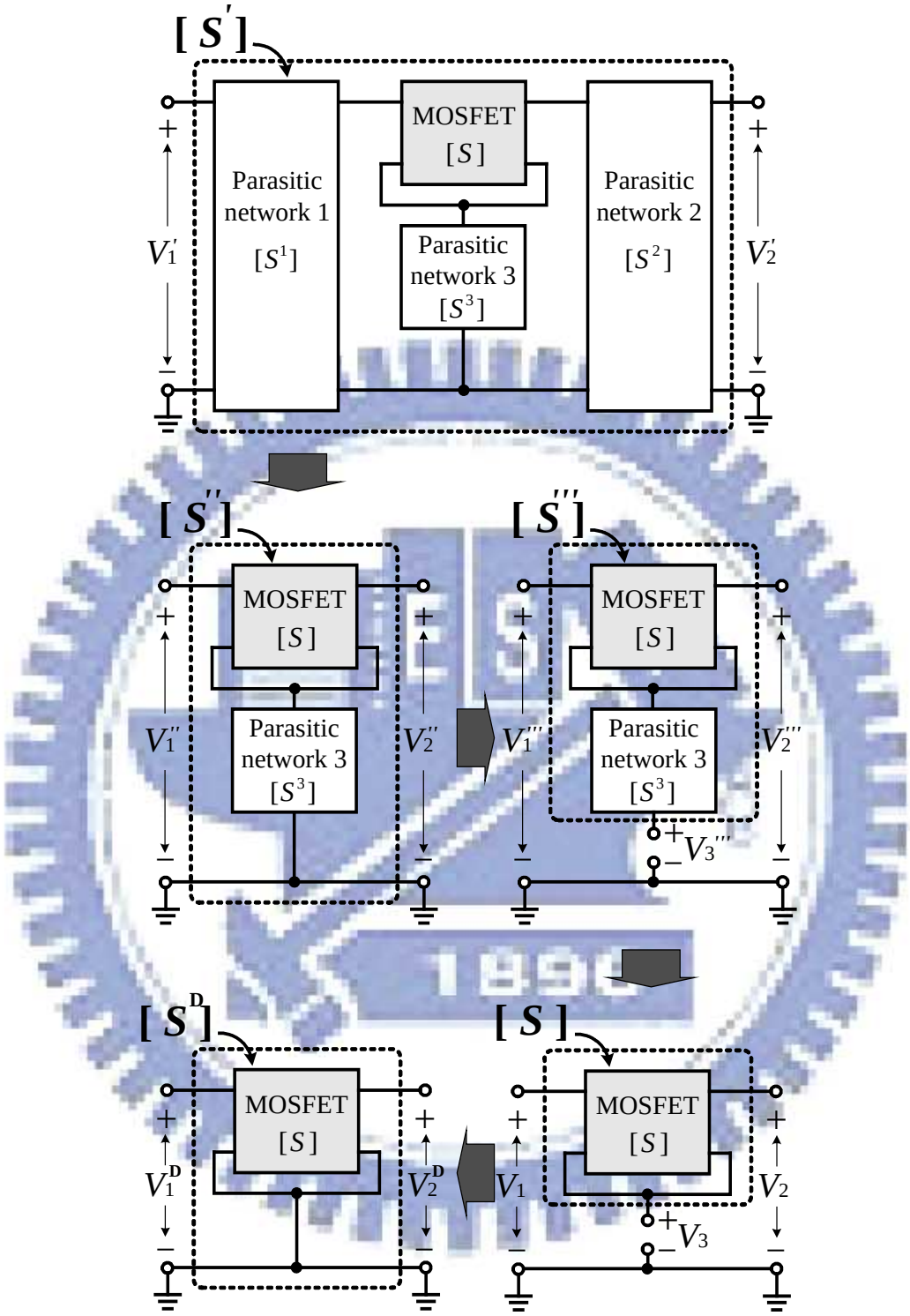



Fig. 2.3 Main procedure for length-scalable de-embedding method.

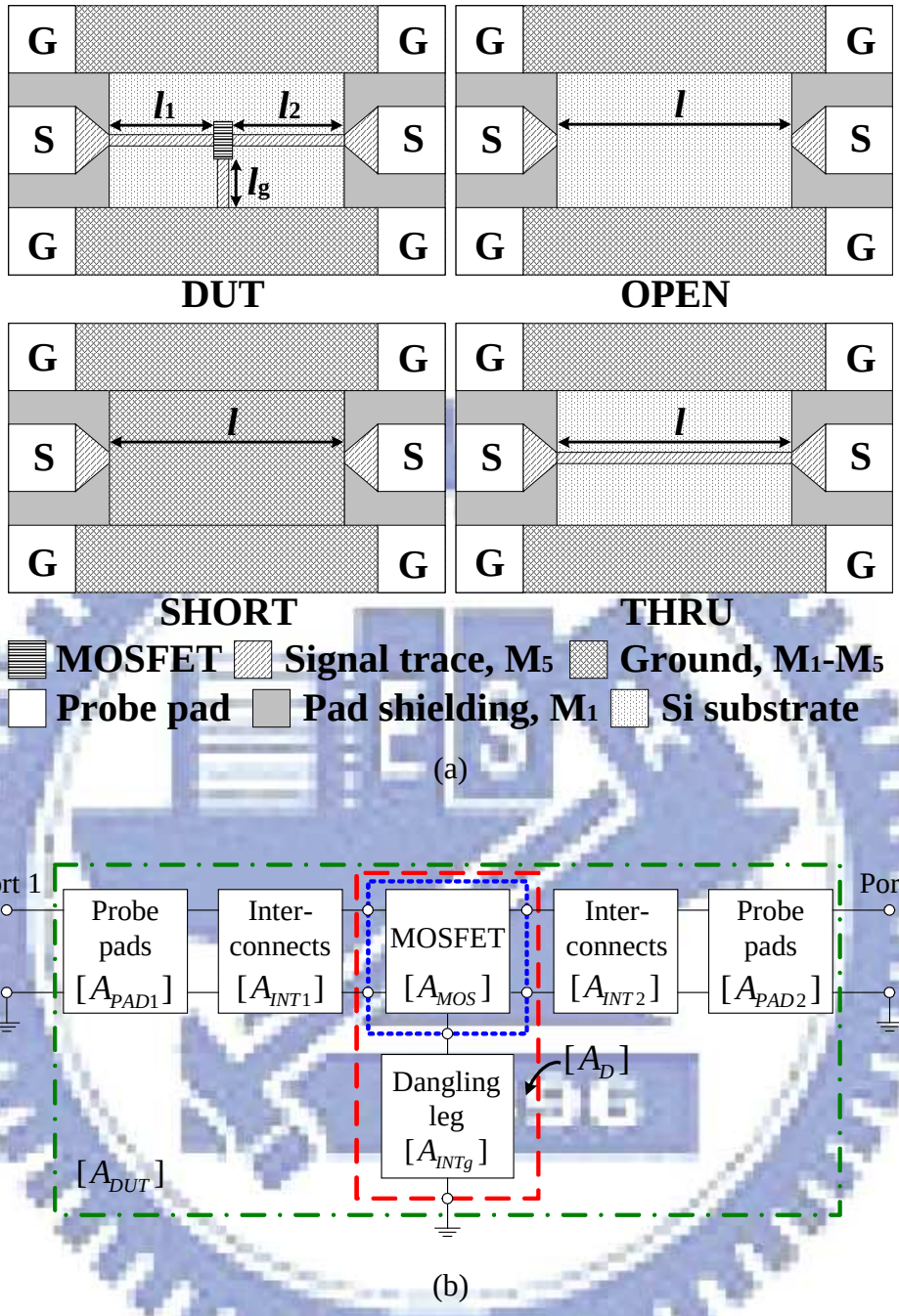



Fig. 2.4 Length-scalable noise de-embedding. (a) DUT and de-embedding structures. (b) Suggested parasitic model for the DUT.

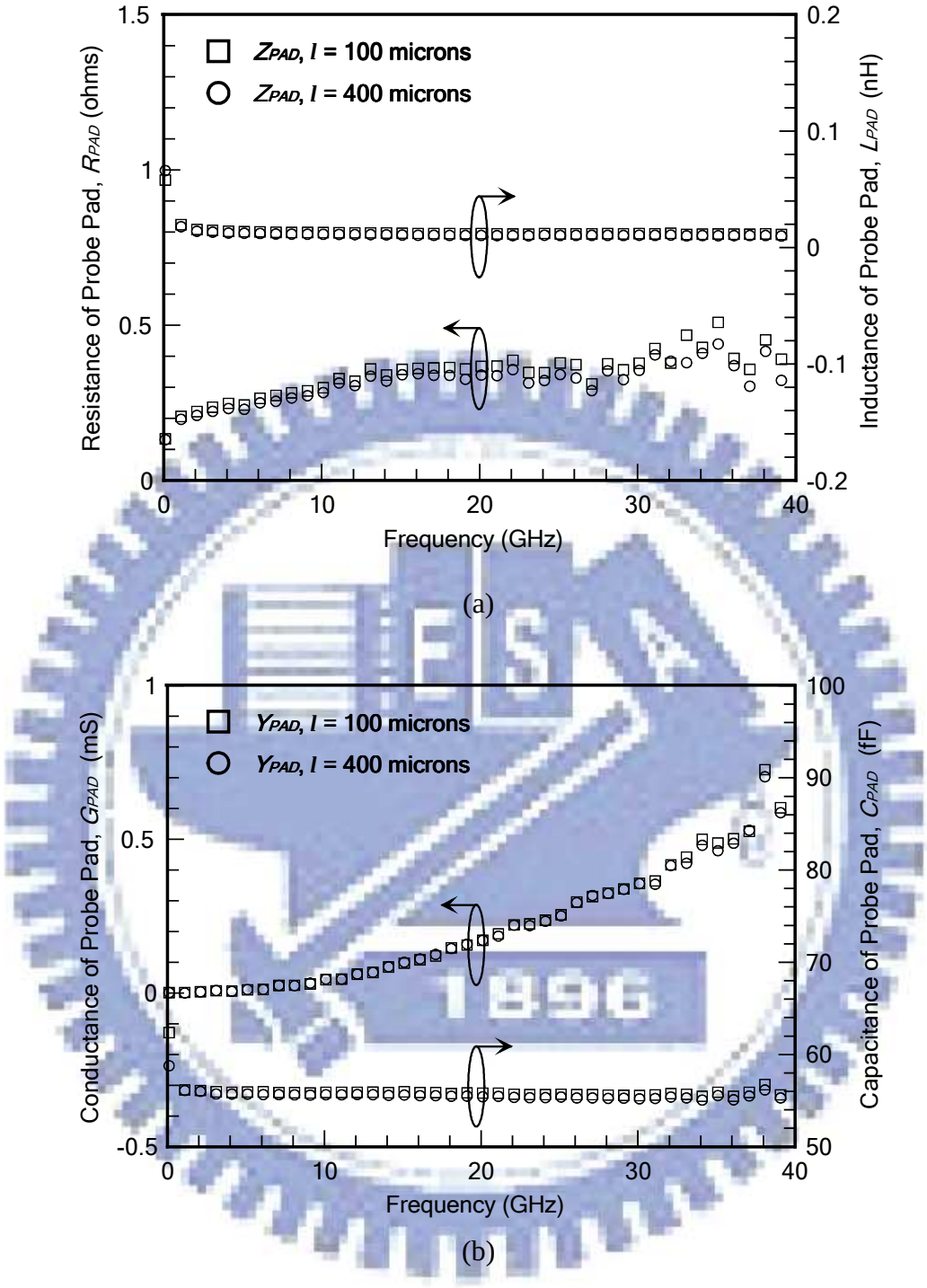



Fig. 2.5 Scalability of open and short standards. (a) Pad resistance and inductance extracted from small ($l$ = 100 μm) and large ($l$ = 400 μm) short standards. (b) Pad conductance and capacitance extracted from small ($l$ = 100 μm) and large ($l$ = 400 μm) open standards.

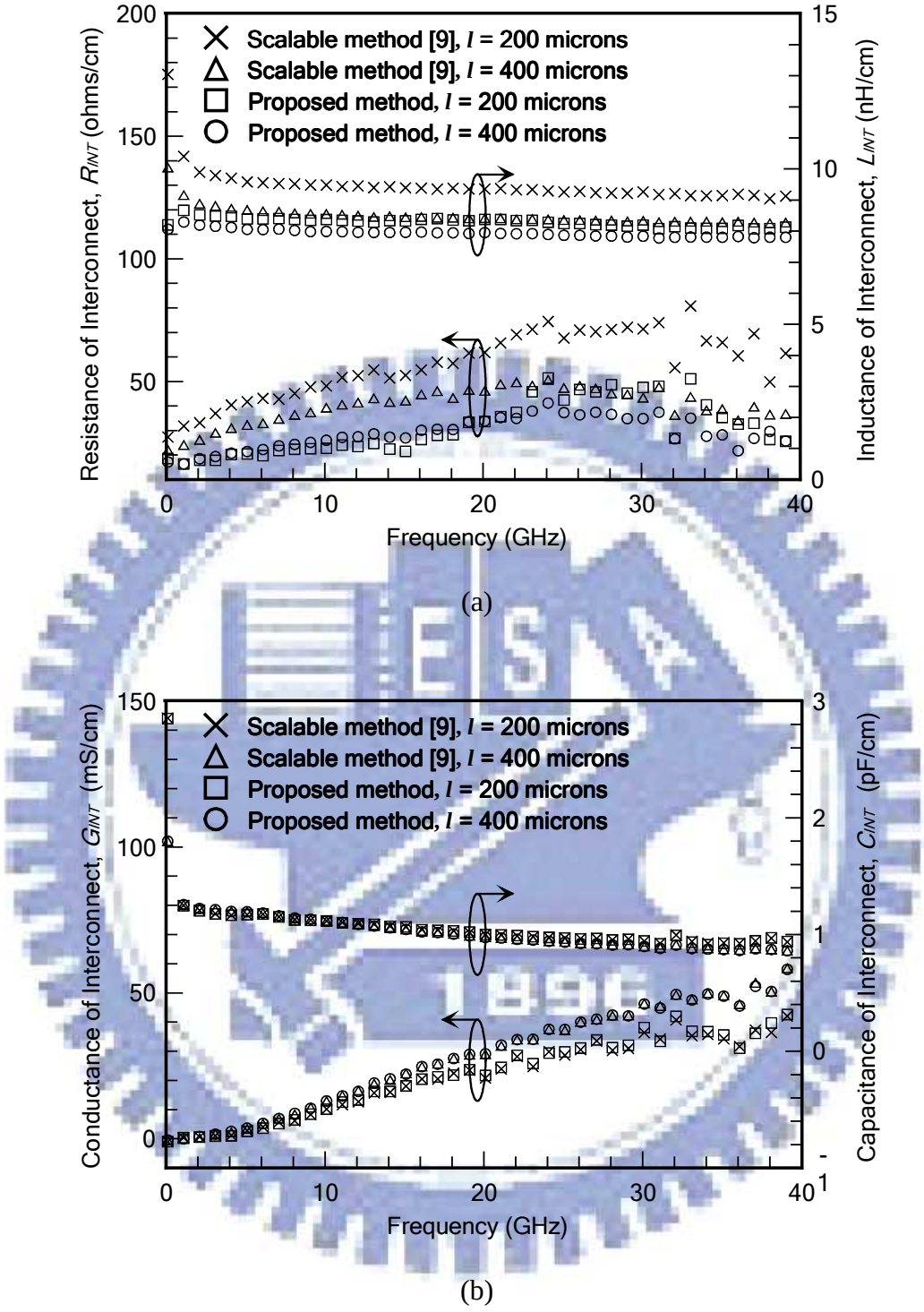



Fig. 2.6 Scalability of thru standards. (a) Per-unit-length interconnect resistance, inductance, (b) conductance, and capacitance extracted from small ($l$ = 200 μm) and large ($l$ = 400 μm) thru standards using conventional scalable method [9] and proposed method.

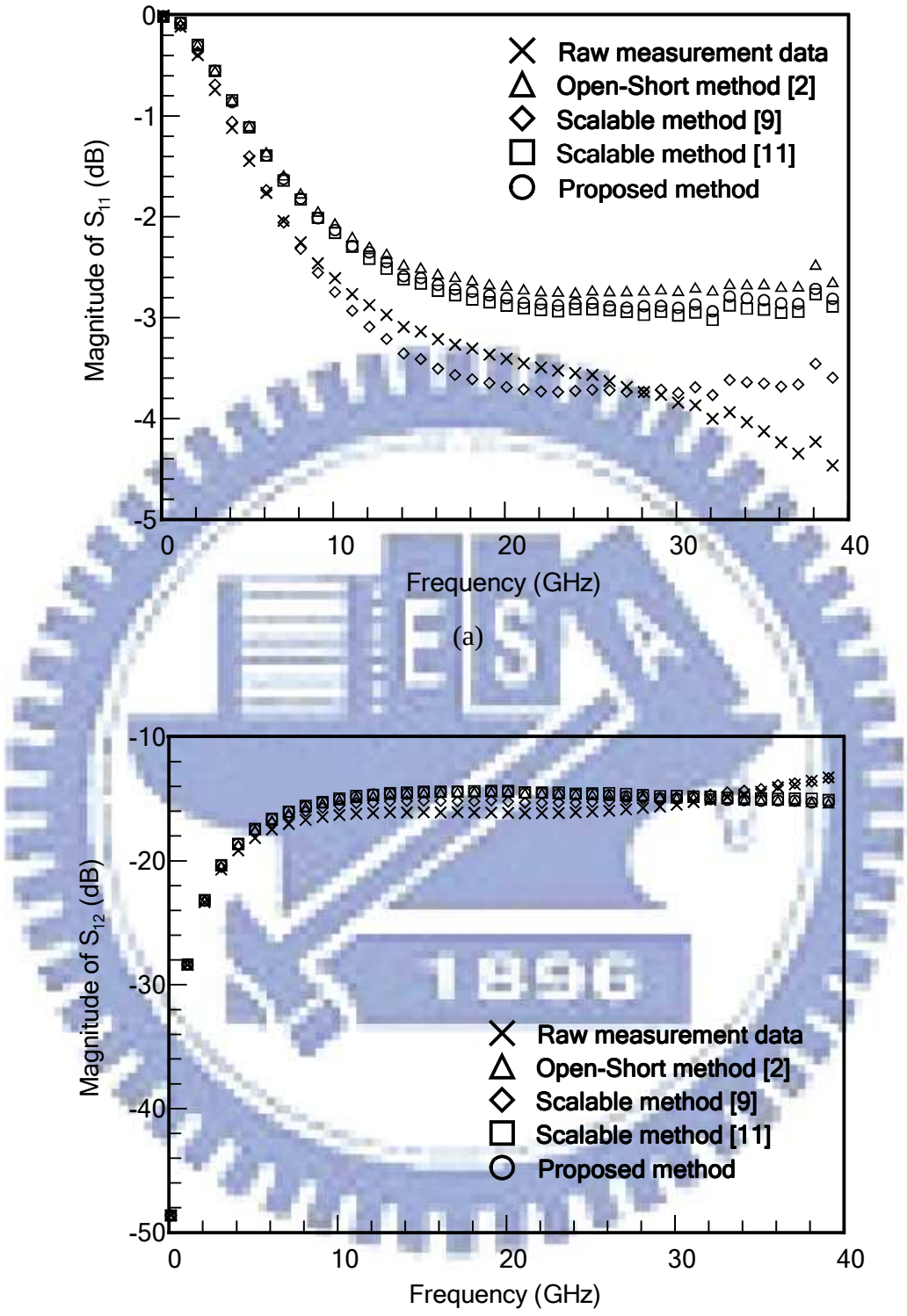



Fig. 2.7 Magnitudes of measured and de-embedded *S*-parameters of the fixtured MOSFET biased at $V_{GS}$ = 1.065 V and $V_{DS}$ = 2 V ($I_{DS}$ = 20 mA). (a) $S_{11}$. (b) $S_{12}$. (c) $S_{21}$. (d) $S_{22}$.

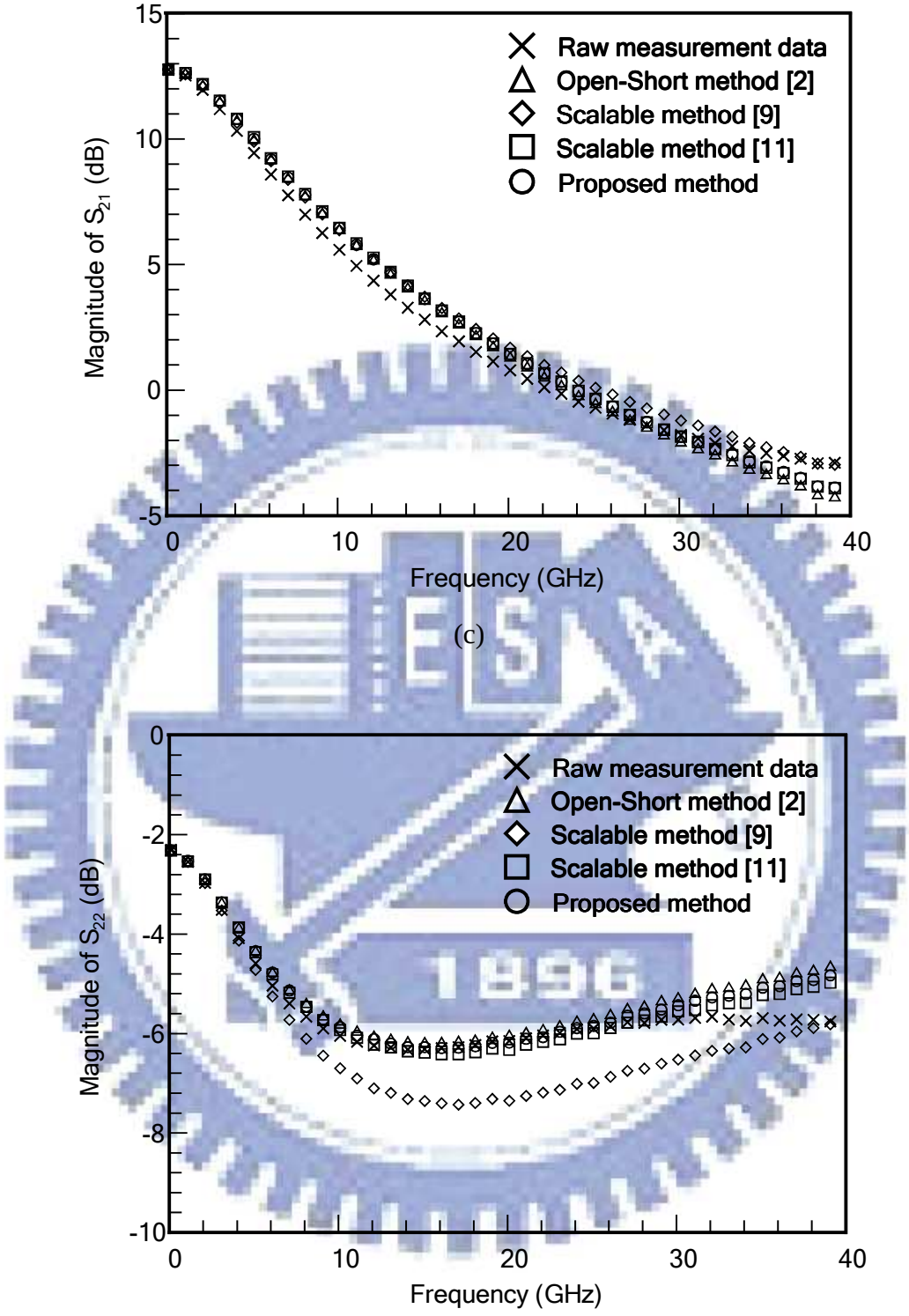



Fig. 2.7 Magnitudes of measured and de-embedded *S*-parameters of the fixtured MOSFET biased at $V_{GS}$ = 1.065 V and $V_{DS}$ = 2 V ($I_{DS}$ = 20 mA). (a) $S_{11}$. (b) $S_{12}$. (c) $S_{21}$. (d) $S_{22}$.

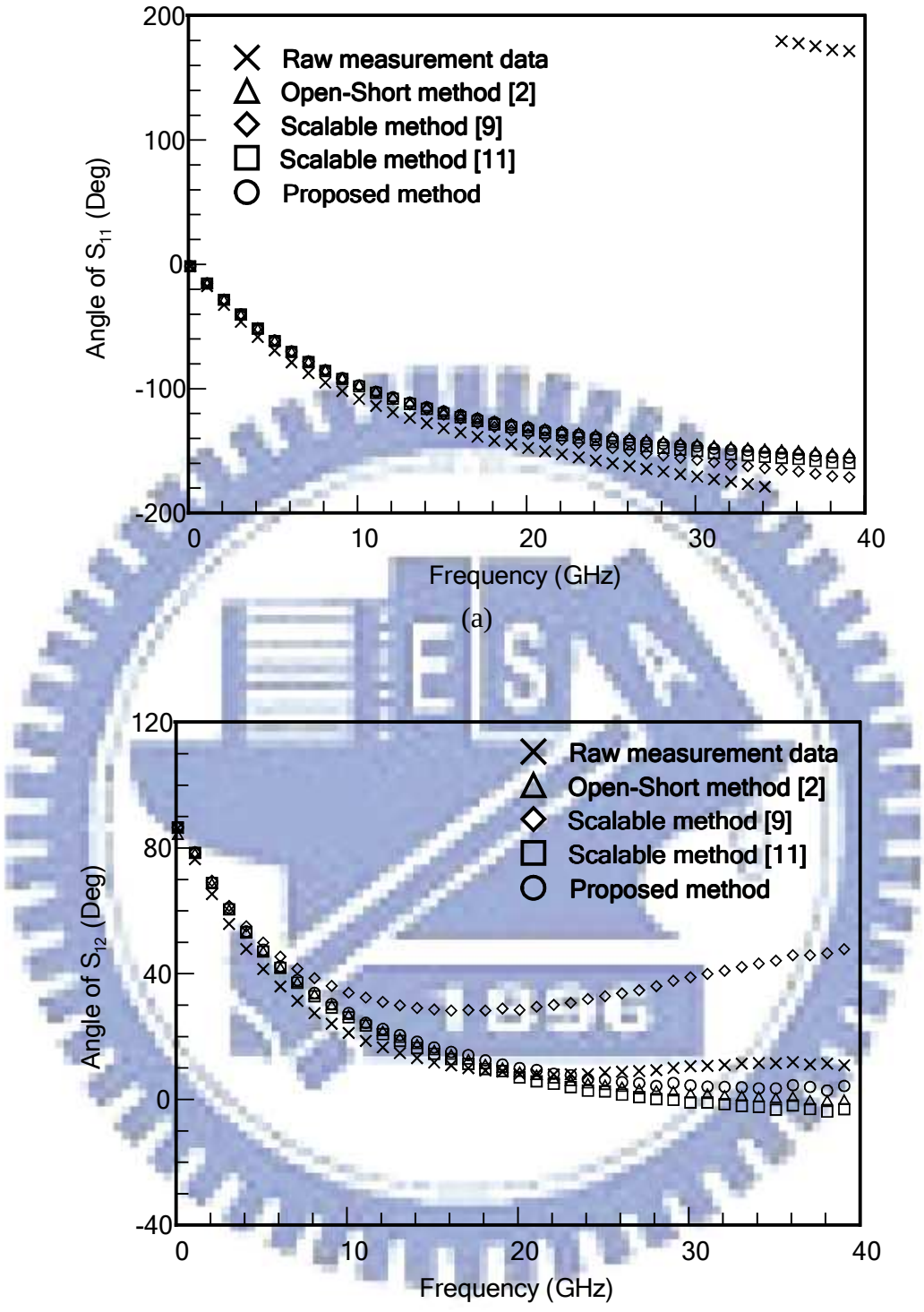



Fig. 2.8 Angles of measured and de-embedded *S*-parameters of the fixtured MOSFET biased at $V_{GS}$ = 1.065 V and $V_{DS}$ = 2 V ($I_{DS}$ = 20 mA). (a) $S_{11}$. (b) $S_{12}$. (c) $S_{21}$. (b) $S_{22}$.

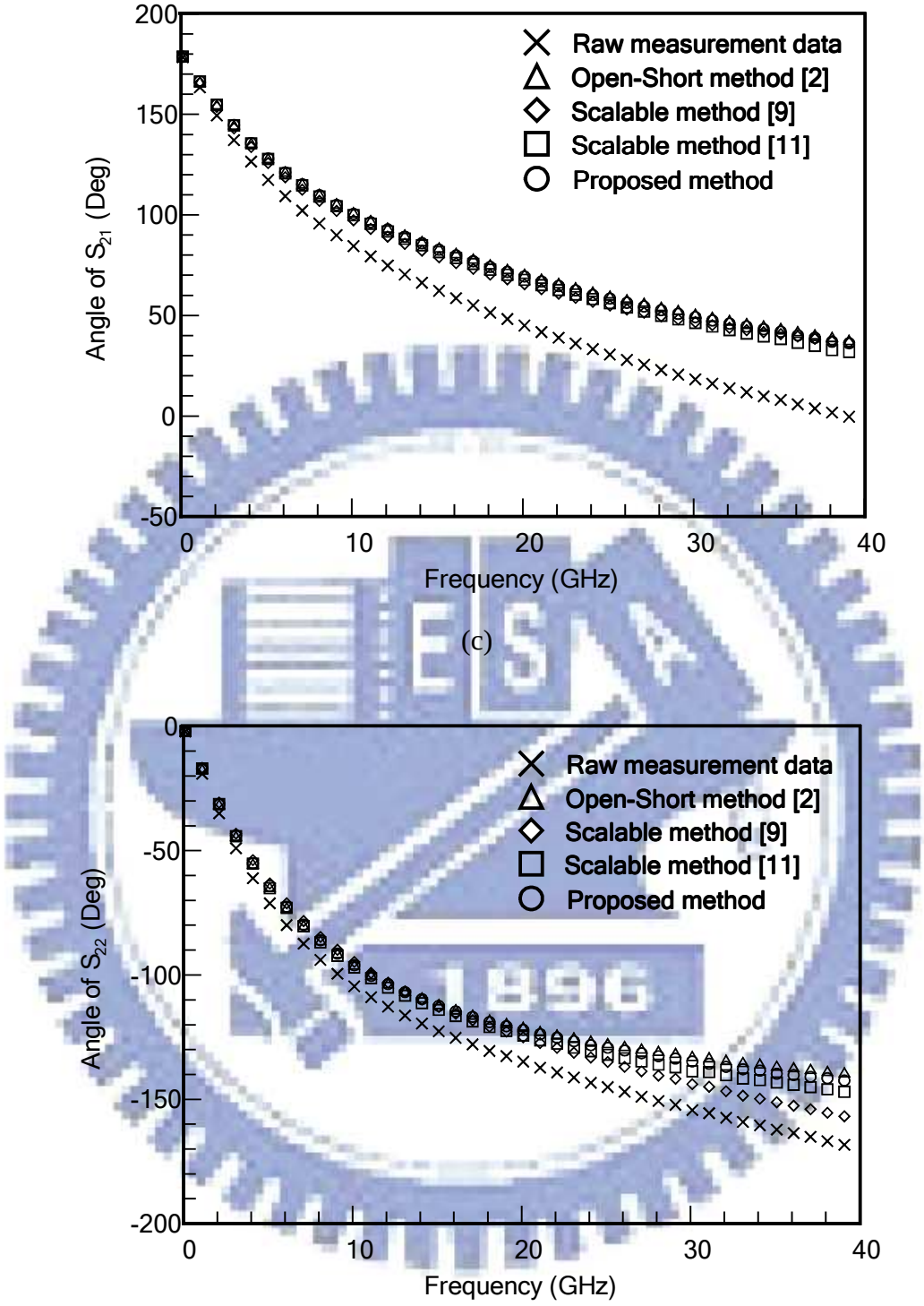



Fig. 2.8 Angles of measured and de-embedded *S*-parameters of the fixtured MOSFET biased at $V_{GS}$ = 1.065 V and $V_{DS}$ = 2 V ($I_{DS}$ = 20 mA). (a) $S_{11}$. (b) $S_{12}$. (c) $S_{21}$. (b) $S_{22}$.

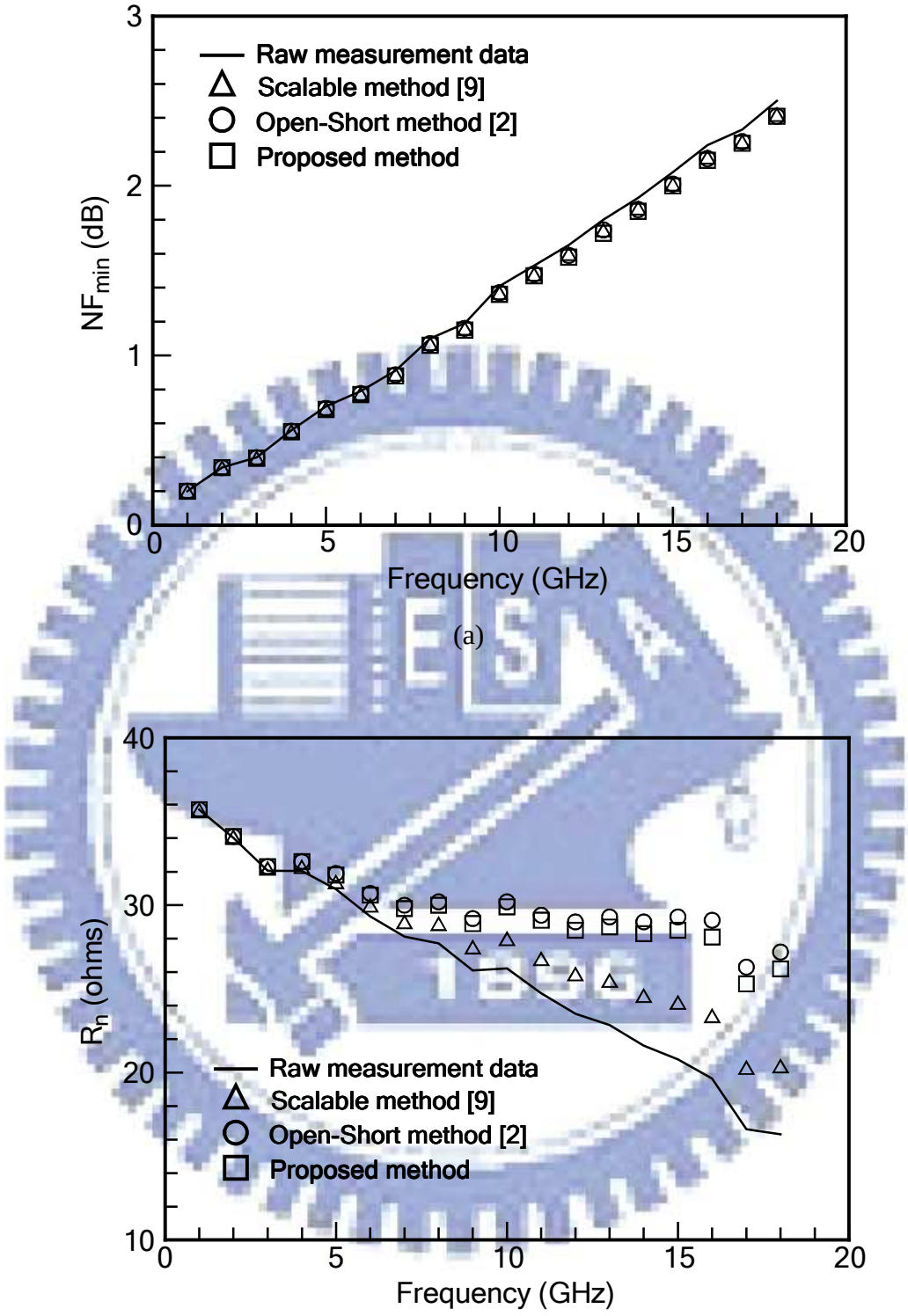



Fig. 2.9 Measured and de-embedded noise parameters of the fixtured MOSFET biased at $V_{GS}$ = 1.065 V and $V_{DS}$ =2 V ($I_{DS}$ = 20 mA). (a) $NF_{min}$ (b) $R_n$ (c) $|\Gamma_{opt}|$ (d) $\angle\Gamma_{opt}$ obtained from raw data, conventional de-embedding methods, and proposed method.

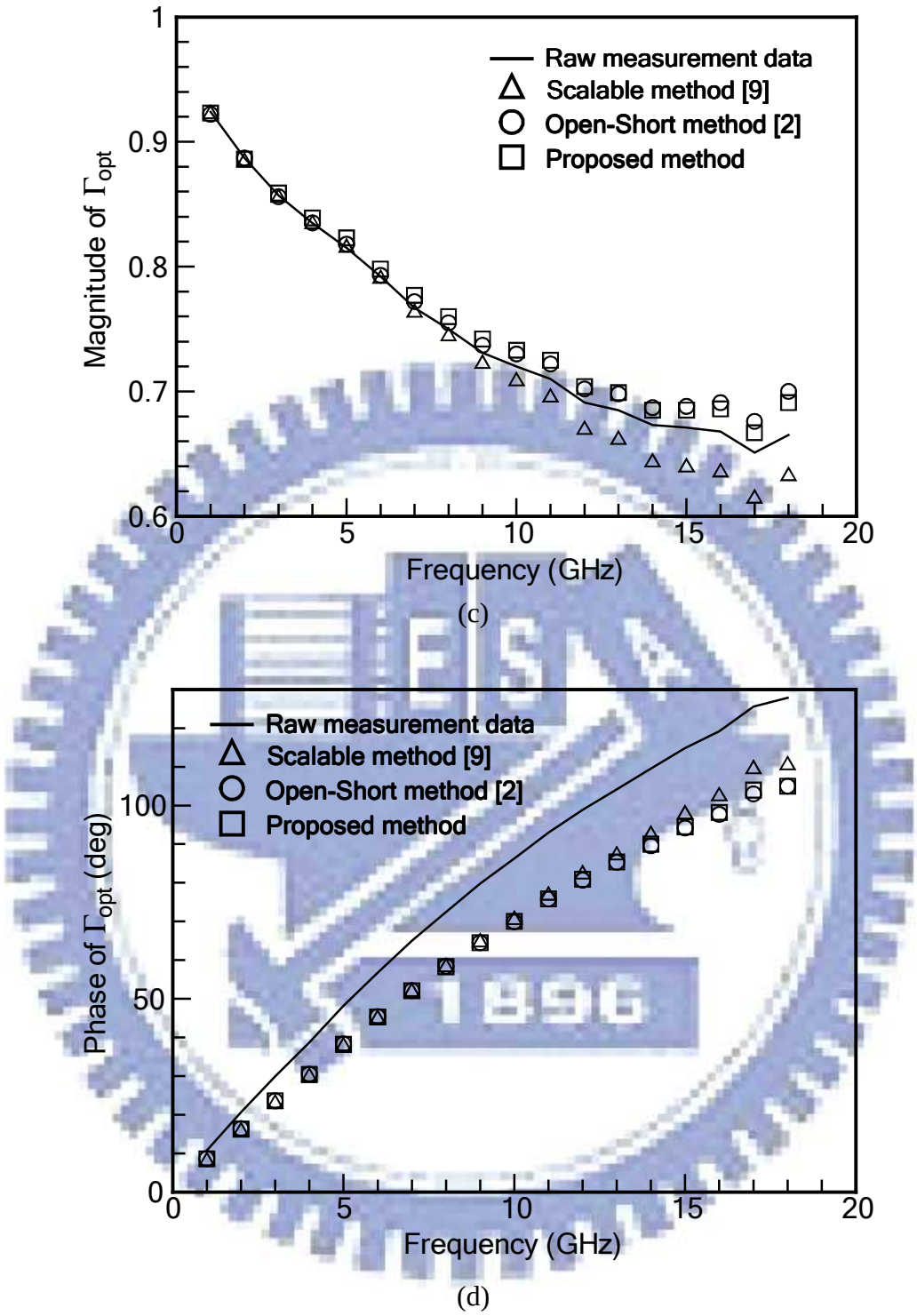



Fig. 2.9 Measured and de-embedded noise parameters of the fixtured MOSFET biased at $V_{GS}$ = 1.065 V and $V_{DS}$ =2 V ($I_{DS}$ = 20 mA). (a) $NF_{min}$ (b) $R_n$ (c) $|\Gamma_{opt}|$ (d) $\angle\Gamma_{opt}$ obtained from raw data, conventional de-embedding methods, and proposed method.

# CHAPTER 3. GEOMETRY-SCALABLE PARASITIC DE-EMBEDDING METHOD FOR ON-WAFER MICROWAVE CHARACTERIZATION OF MOSFETS

## 3.1 Introduction

The design of silicon-based RFICs and MMICs requires reliable process technology and foundry design kits. Device modeling and parasitic extraction are significant issues for circuit design to minimize the failures and frequency shifts. Since reliable RF models call for accurate wafer-level microwave characterization of active and passive components, testing methodologies and modeling test keys should be carefully developed to evaluate the intrinsic device characteristics. To extract the intrinsic device parameters from microwave measurements, much research effort has been focused on this particular subject. Although much work has been done to date, most research has focused on the accuracy of the parasitic estimation and correction [1]-[8]. In this chapter, we attempt to propose a systematic parasitic de-embedding procedure to minimize the chip area and characterization time in a mass-production line. With the utilization of the shielding technique, the reflect and thru dummy structures can be used to calculate the parasitics of probe pads and the transmission-line parameters of interconnects, respectively [13]. Based on the transmission-line theory and microwave network analysis, the proposed method can generate

the parasitics of feeding networks with arbitrary geometry to efficiently and accurately de-embed the parasitic effects of the fixtured MOS transistors with various gate dimensions and multiplier factors. To validate this geometry-scalable de-embedding theory, MOS transistors and de-embedding structures were fabricated using a UMC 0.13-μm CMOS process, and full-wave electromagnetic simulations were carried out.

## 3.2 Geometry-Scalable De-Embedding Theory

### *3.2.1 On-Wafer Test Fixtures*

Fig. 3.1 illustrates the on-wafer test fixtures, which contain a DUT and its corresponding dummy structures, for the proposed de-embedding theory. The design of RF test keys for global device modeling must cover the complete physical device dimensions, such as channel length, channel width, finger number, multiplier factor, etc. Therefore, both single- and multi-transistor ($T_1$–$T_M$) test fixtures should be employed to extract the device characteristics, multiplier effects, and proximity effects. In general, the gate and drain of the MOSFET are, respectively, connected to the input and output port, while the source and silicon substrate are tied together to the ground reference. In our design, the source of the MOSFET is connected to the ground shield beneath the signal traces to form a microstrip-like transmission line, and thus the parasitics of the dangling leg between the transistor and the ground plane can be eliminated by simply using a two-port model [11], [17]. Here the ground shield not only

improves the substrate isolation, but also provides good fixture scalability [13] and interconnect scalability [9] for the proposed geometry-scalable de-embedding method. The substrate-shielded reflect structure, which consists of a simple open at the input port and a simple short at the output port or vice versa, is used to remove the parasitics of the GSG pads [13]. A thru dummy with an *N*-conductor interconnect ($I_1$–$I_N$) is used to evaluate the transmission-line parameters for subtracting the interconnect parasitics of the *M*-transistor test fixtures. It should be noted that the multi-conductor thru is employed, instead of a single-conductor one, to mitigate the step-discontinuity effects of the pad-to-interconnect interface [18].

Fig. 3.2(a) shows the semi-distributed parasitic model based on the cascade and parallel configurations for the modeling test keys. The parasitic components $Y_{PAD}$ and $Z_{PAD}$, which can be replicated from the reflect structure in Fig. 3.2(b), are the shunt admittance and series impedance of the probe pads, respectively. Since here the shielding technique is applied, the multi-conductor interconnect can be modeled as isolated transmission lines in parallel with each other. As shown in Fig. 3.2(c), after subtracting the probe-pad parasitics of the *N*-conductor thru dummy, the transmission-line parameters of a single-conductor interconnect calculated using the network analysis can be employed to de-embed the parasitic effects of the interconnects with arbitrary geometry.

### *3.2.2 Combination of Microwave Networks*

As mentioned in the previous subsection, both the cascade and parallel combinations of two-port networks would be utilized to establish the de-embedding procedure. In this case, it is convenient to characterize the fixtured transistors using the *ABCD*-parameter representation. The combination of two *ABCD* matrices defined in terms of the total voltages and currents is shown in Fig. 3.3. For the cascade connection of two two-port networks, the overall *ABCD* matrix is equal to the product of the individual *ABCD* matrices [19], namely

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A_C & B_C \\ C_C & D_C \end{bmatrix} \begin{bmatrix} V_3 \\ I_3 \end{bmatrix} \tag{3.1}$$

where

$$\begin{bmatrix} A_C & B_C \\ C_C & D_C \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix}. \tag{3.2}$$

Consequently, the embedding and de-embedding of two-port networks can be accomplished by multiplying a given matrix by a matrix and by an inverse of matrix, respectively.

Similarly, the overall *ABCD* matrix of the two-port networks connected in parallel can be expressed as

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A_P & B_P \\ C_P & D_P \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \tag{3.3}$$

where

$$\begin{bmatrix} A_P & B_P \\ C_P & D_P \end{bmatrix} = \begin{bmatrix} \dfrac{A_1B_2 + B_1A_2}{B_1 + B_2} & \dfrac{B_1B_2}{B_1 + B_2} \\ C_1 + C_2 + \dfrac{(A_1 - A_2)(D_2 - D_1)}{B_1 + B_2} & \dfrac{D_1B_2 + B_1D_2}{B_1 + B_2} \end{bmatrix}. \tag{3.4}$$

Consider the case of multi-conductor interconnects shown in Figs. 3.1 and 3.2. The input/output feeding networks are equally divided into *M* microstrip-like transmission lines with appropriate line separation, and as a result, the overall *ABCD* matrix of the *M* identical two-port networks oriented in parallel can be derived based on (3.4) as

$$\begin{bmatrix} A_P & B_P \\ C_P & D_P \end{bmatrix} = \begin{bmatrix} A & \dfrac{B}{M} \\ MC & D \end{bmatrix} \tag{3.5}$$

where *A*, *B*, *C*, and *D* are the *ABCD* parameters of each single-conductor microstrip.

According to the network analysis mentioned above, the parasitics of the MOSFET test structures modeled in the cascade and parallel configurations can be evaluated and then de-embedded.

### *3.2.3 De-Embedding Procedure*

As shown in Fig. 3.2, the *ABCD* matrices of the probe-pad parasitics for ports 1 and 2 are respectively

$$[A_{PAD1}] = \begin{bmatrix} 1 & Z_{PAD} \\ Y_{PAD} & 1 + Y_{PAD}Z_{PAD} \end{bmatrix} \tag{3.6}$$

and

$$[A_{PAD2}] = \begin{bmatrix} 1 + Y_{PAD}Z_{PAD} & Z_{PAD} \\ Y_{PAD} & 1 \end{bmatrix}. \tag{3.7}$$

It should be noted that $Y_{PAD} = Y_{REFLECT,11}$ and $Z_{PAD} = 1/(Y_{REFLECT,22} - Y_{REFLECT,11})$, where

[$Y_{REFLECT}$] is the admittance matrix of the reflect dummy. The thru dummy can be modeled in cascade connection and its pad parasitics can be subtracted by using [$A_{INT}$] = [$A_{PAD1}$]$^{-1}$[$A_{THRU}$][$A_{PAD2}$]$^{-1}$, where [$A_{THRU}$] and [$A_{INT}$] are the *ABCD* matrices of the thru dummy and the *N*-conductor interconnect without probe-pad parasitics, respectively. Accordingly, the transmission-line parameters of the *N*-conductor interconnect, such as characteristic impedance $Z_C$ and propagation constant $\gamma$, can be evaluated as in [9]. Here we have that

$$[A_{INT}] = \begin{bmatrix} \cosh\gamma l & Z_C \sinh\gamma l \\ \frac{1}{Z_C}\sinh\gamma l & \cosh\gamma l \end{bmatrix}. \tag{3.8}$$

Based on the above results, the parasitic effects of the input/output interconnects with arbitrary line length ($l_1$ and $l_2$) for an *M*-transistor test fixture can be efficiently calculated from the *ABCD* matrix of an *N*-conductor thru, and thus

$$[A_{INTi}] = \begin{bmatrix} \cosh\gamma l_i & \frac{NZ_C}{M}\sinh\gamma l_i \\ \frac{M}{NZ_C}\sinh\gamma l_i & \cosh\gamma l_i \end{bmatrix}, \; i = 1, 2. \tag{3.9}$$

The detailed de-embedding procedure is summarized as follows:

19) Measure the *S*-parameters [$S_{DUT}$], [$S_{REFLECT}$], and [$S_{THRU}$] of the DUT, reflect, and thru, respectively.

20) Convert [$S_{REFLECT}$] to its admittance matrix [$Y_{REFLECT}$], and calculate the *ABCD* matrices [$A_{PAD1}$] and [$A_{PAD2}$] of probe pads from (3.6) and (3.7).

21) Extract the intrinsic interconnect parameters using [$A_{INT}$] = [$A_{PAD1}$]$^{-1}$[$A_{THRU}$][$A_{PAD2}$]$^{-1}$ and

calculate the characteristic impedance $Z_C$ and propagation constant γ as in [9].

22) Calculate the *ABCD* matrices [$A_{INT1}$] and [$A_{INT2}$] for the input/output interconnects from (3.9).

23) Calculate the *ABCD* matrices [$A_{IN}$] and [$A_{OUT}$], which are respectively the input and output feeding networks, from [$A_{IN}$] = [$A_{PAD1}$][$A_{INT1}$] and [$A_{OUT}$] = [$A_{INT2}$][$A_{PAD2}$].

24) Convert [$S_{DUT}$] to its *ABCD* matrix [$A_{DUT}$] and calculate the *ABCD* matrix [$A_D$] of the intrinsic MOSFETs using [$A_D$] = [$A_{IN}$]$^{-1}$[$A_{DUT}$][$A_{OUT}$]$^{-1}$.

25) Convert [$A_D$] to its *S*-parameters [$S_D$].

## 3.3 Results and Discussion

To verify the proposed de-embedding theory, MOS transistors and the corresponding de-embedding structures were fabricated using a 0.13-μm eight-metal-layer CMOS process. The NMOS transistors with the dimensions of gate length ($L_g$) = 0.13 μm, gate width ($W_g$) = 4 μm, number of fingers ($N_f$) = 16, and multiplier factor ($M$) = 1, 2, 4, and 8 were connected in a two-port GSG configuration. The multi-conductor interconnects with the dimensions of line length ($l_1$ and $l_2$) = 41 μm, line width ($W$) = 6 μm, and line separation ($S$) = 7.5 μm were designed with the EM simulations and placed between the probe pads and transistors. The DC and RF measurements of the on-wafer test structures were performed on an Agilent 4142B Modular DC Source/Monitor and an Agilent 8510C VNA, respectively. Before starting the *S*-parameter measurements, the measurement system was calibrated using the

LRRM calibration procedure.

### *3.3.1 Electromagnetic Simulations*

In this subsection, the full-wave EM simulations based on the method of moment (MoM) were performed to design the feeding networks. As shown in Fig. 3.4, four two-port microstrip geometries were simulated: single-conductor microstrip and shunt microstrips on a silicon substrate and on a ground shield. Figs. 3.4(a) and 3.4(b) show the simulated characteristic impedance as a function of frequency for a single microstrip on a silicon substrate and a ground shield, respectively. In these configurations, the line width was kept constant at 6 μm and the line length (*l*) was varied from 50 μm to 1000 μm. It is shown that both of the two single-conductor microstrip structures show excellent interconnect scalability over a wide range of frequency. In practice, the interconnect scalability would be degraded by improper parasitic de-embedding [9], and therefore here the interconnect length of the thru dummy was set to about 300 μm to mitigate the parasitic effects as well as save the chip area. Figs. 3.4(c) and 3.4(d) display the simulated characteristic impedance as a function of frequency for unshielded and substrate-shielded shunt microstrips, respectively. The line length and line width were held constant at 300 μm and 6 μm, respectively, and the line separation (*S*) was altered from 5 μm to 100 μm. As the line separation increases, the impedance of the unshielded shunt microstrips becomes lower because of the increasing of the effective line width, while the substrate-shielded ones show approximately identical

impedance. These results indicate that the shunt microstrips can be divided into isolated two-port networks by the use of the ground shielding and careful design of the microstrip geometry. Here a line separation of 7.5 μm was adopted according to the transistor size and arrangement.

Based on the above findings, we can efficiently replicate and de-embed the parasitics of the shielded feeding networks with arbitrary line length and number of lines.

### *3.3.2 Microwave Measurements*

Fig. 3.5 shows the layout of the fabricated modeling test keys and dummy structures for the industry-standard open-short de-embedding [2] and the proposed method. In this work, a two-conductor thru is selected to mitigate the step-discontinuity effects of the pad-to-interconnect junction and to generate the interconnect parasitics. Fig. 3.6 compares the characteristic impedance calculated based on (3.9) to that measured from the thru dummies with various numbers of lines ($N$ = 1, 2, 4, and 8). It can be seen that the calculations match well with the measurements. Fig. 3.7 demonstrates the two-port $S$-parameters of the MOSFET test fixtures with various multiplier factors ($M$ = 1, 2, 4, and 8) biased at $V_{GS}$ = 1.2 V and $V_{DS}$ = 1.2 V. These results are de-embedded using the open-short method and the proposed one. As we can see, the results obtained from the two different methods are in excellent agreement over the entire frequency range. As a result, the proposed geometry-scalable de-embedding methodology can be used to accurately extract the intrinsic

characteristics of the silicon-based device. The chip area and the characterization time also can be significantly reduced since only two dummy structures would be implemented on a wafer.

## 3.4 Conclusion

In this chapter, a geometry-scalable parasitic de-embedding method for two-port on-wafer MOSFET characterization has been presented and verified. The proposed de-embedding method based on the transmission-line theory and microwave network analysis uses only two substrate-shielded dummy structures to replicate and de-embed the parasitic networks surrounding the fixtured MOSFETs. Both the interconnect scalability and the de-embedding accuracy of the proposed method are validated up to 30 GHz. The de-embedded results substantiate that the proposed method is accurate and efficient for evaluating the intrinsic device characteristics.

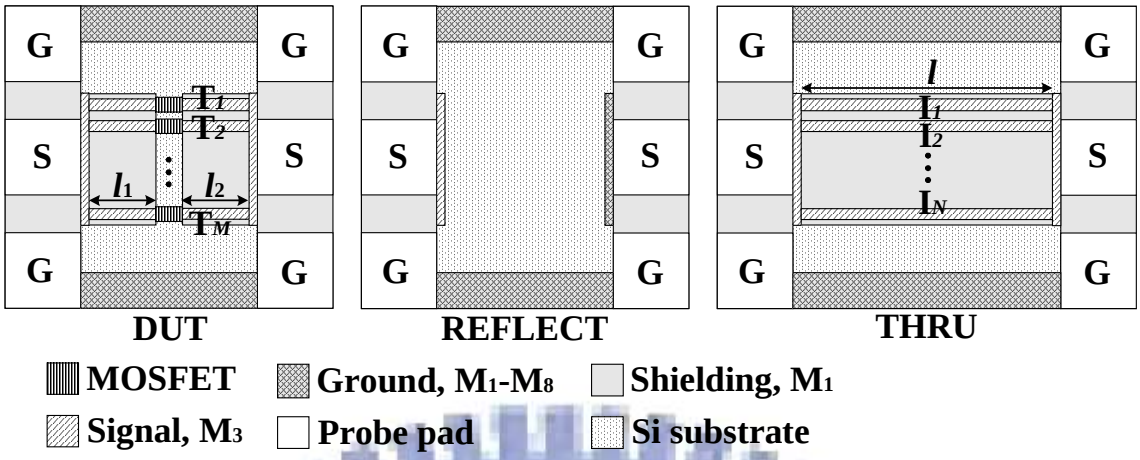



Fig. 3.1 Illustration of the on-wafer MOSFET test structure and corresponding dummy structures for proposed geometry-scalable de-embedding method.

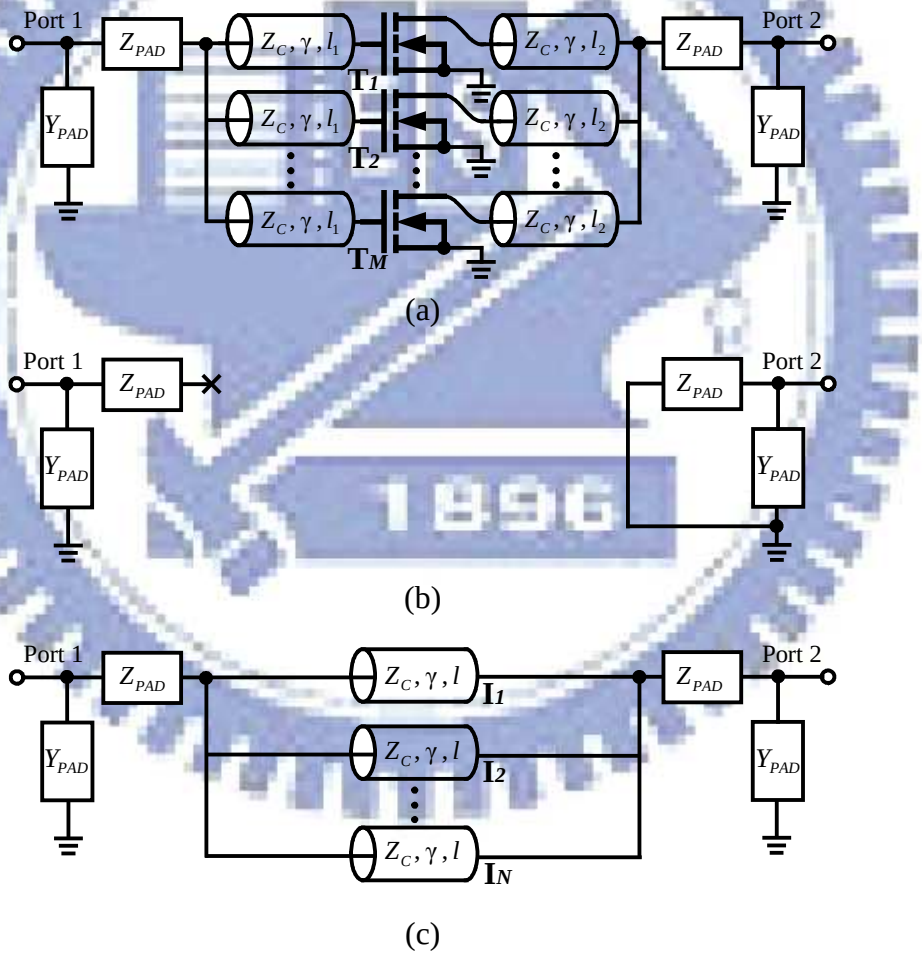
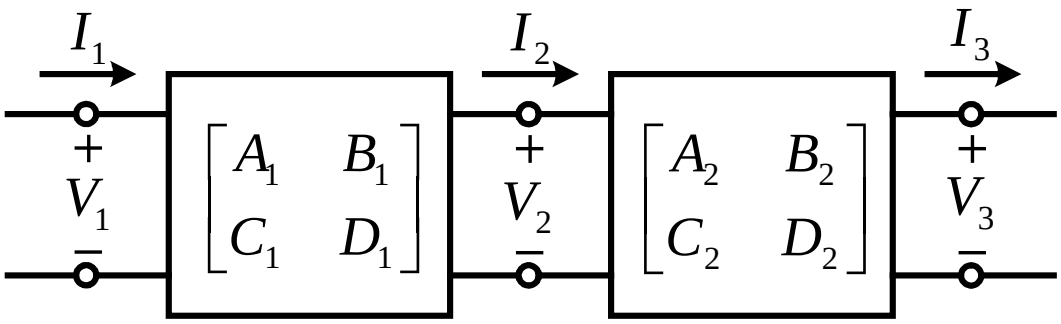
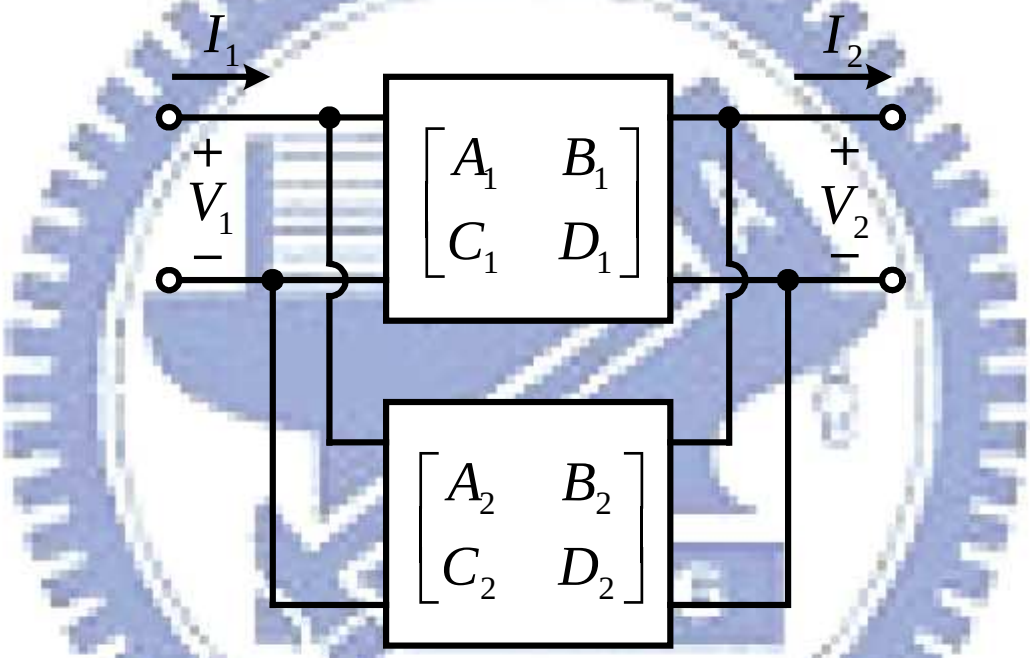



Fig. 3.2 Suggested parasitic models for the proposed on-wafer test structures. (a) DUT. (b) Reflect dummy structure. (c) Thru dummy structure.




(a)




(b)

Fig. 3.3 Combination of two-port networks. (a) Cascade connection. (b) Parallel connection.

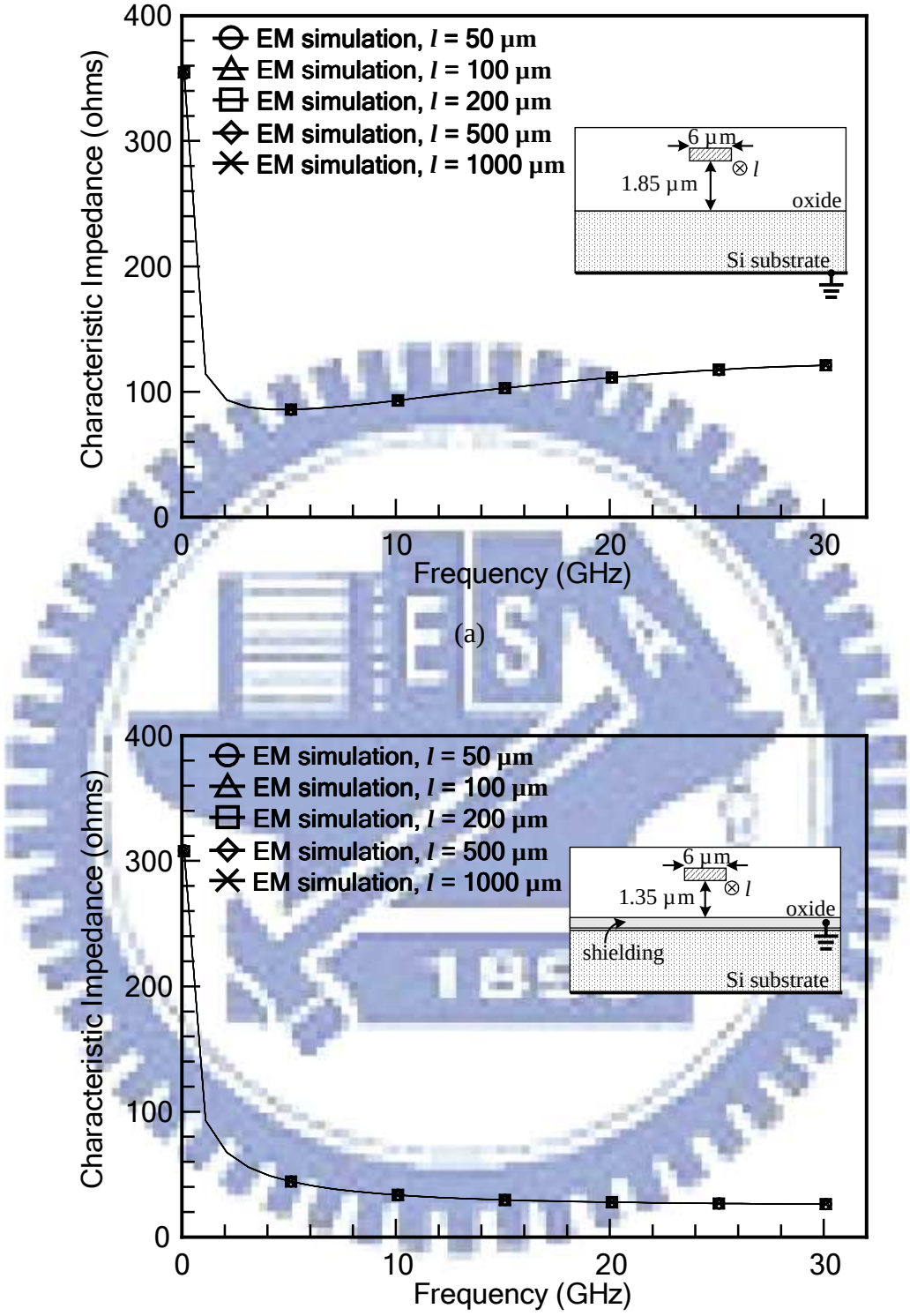
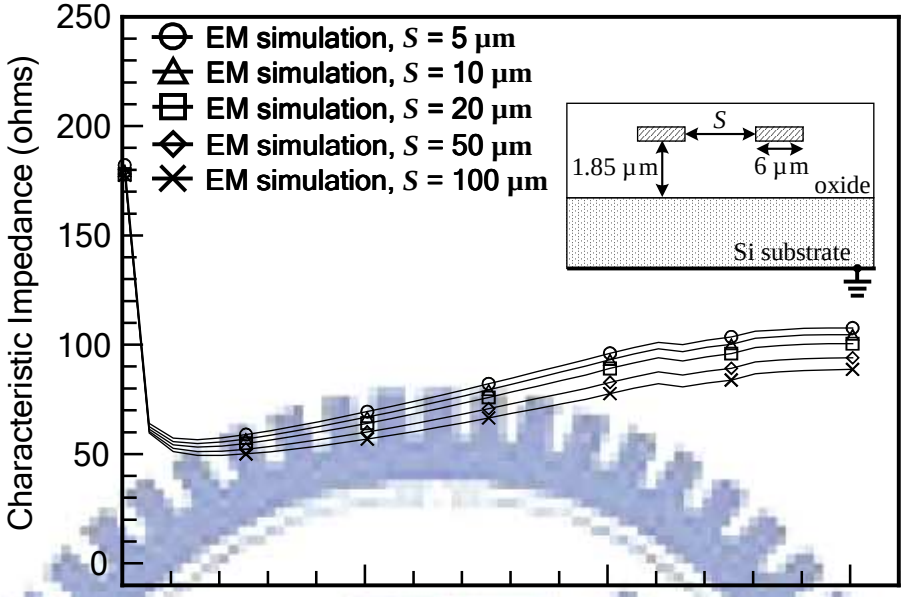
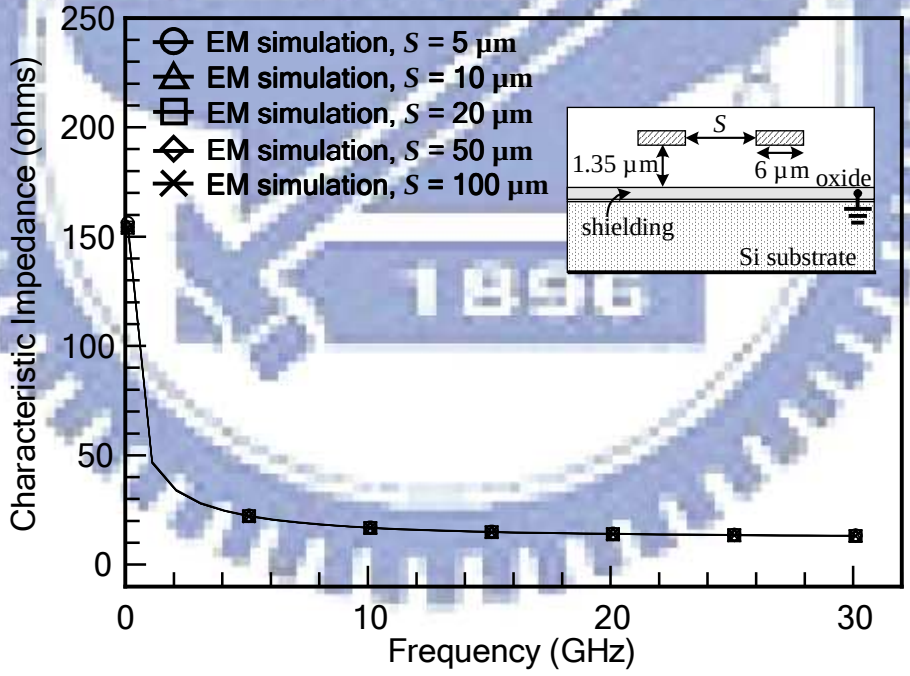



Fig. 3.4 EM-simulated characteristic impedance versus frequency for different guided wave structures. (a) Single microstrip without shielding. (b) Single microstrip with shielding. (c) Shunt microstrips without shielding. (d) Shunt microstrips with shielding.




(c)




(d)

Fig. 3.4 EM-simulated characteristic impedance versus frequency for different guided wave structures. (a) Single microstrip without shielding. (b) Single microstrip with shielding. (c) Shunt microstrips without shielding. (d) Shunt microstrips with shielding.

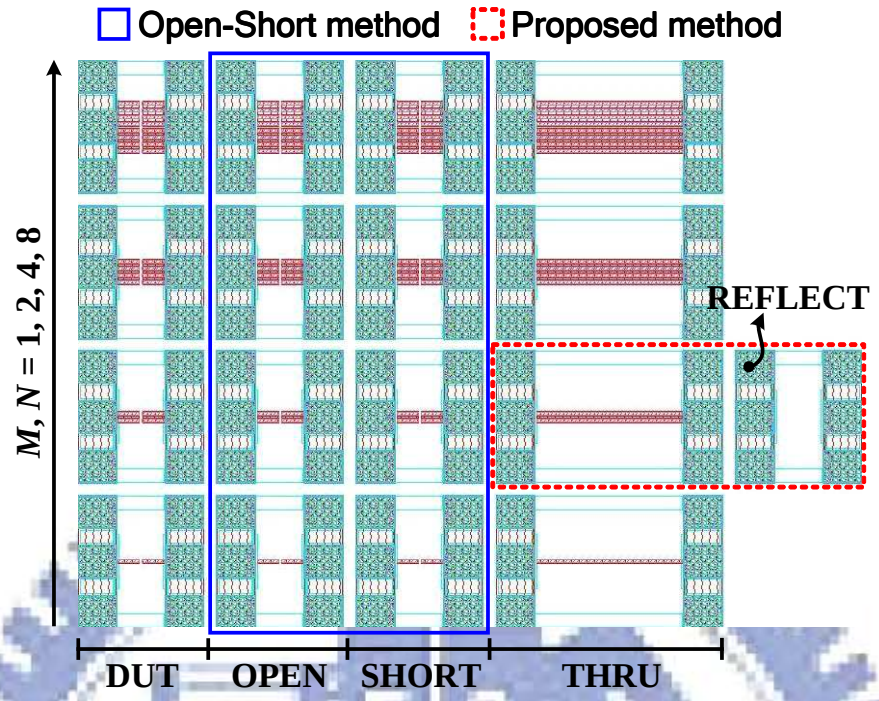



Fig. 3.5 Layout of the on-wafer MOSFET test structures and de-embedding structures for the open-short method [2] and proposed method.

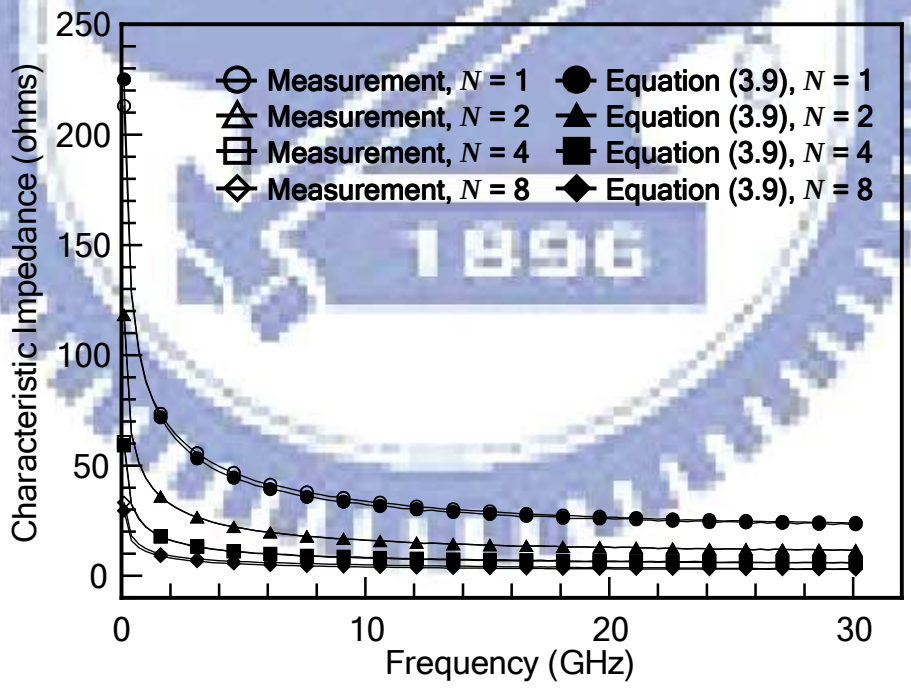
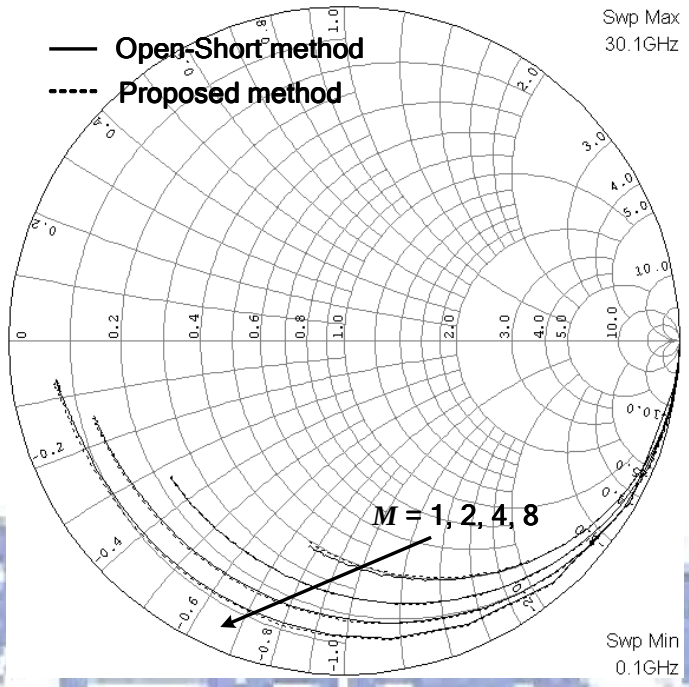
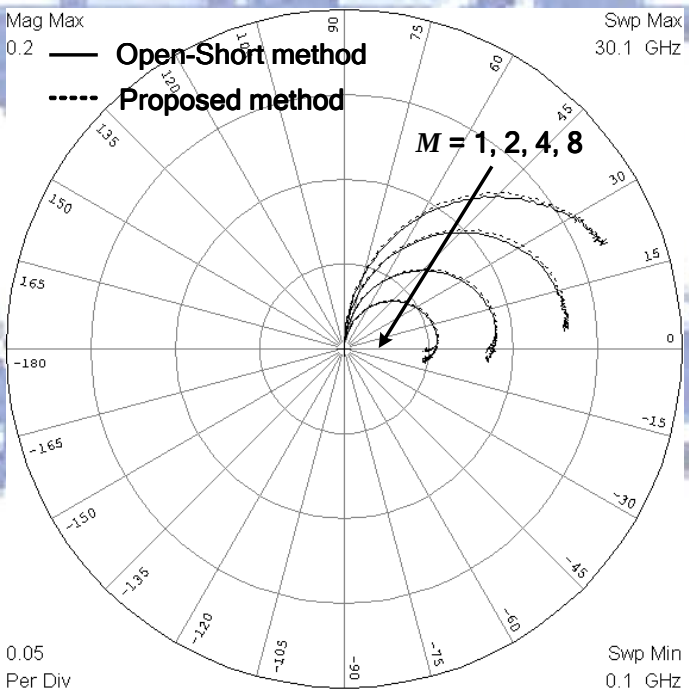



Fig. 3.6 Measured and calculated characteristic impedance versus frequency for thru dummy structures with different numbers of lines ($N$ = 1, 2, 4, and 8). The pad parasitics of thru dummies were removed.

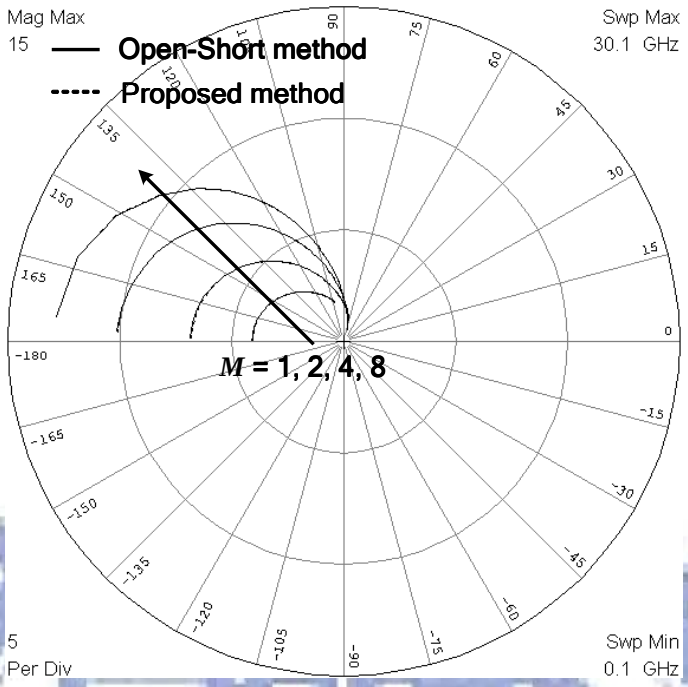



(a)

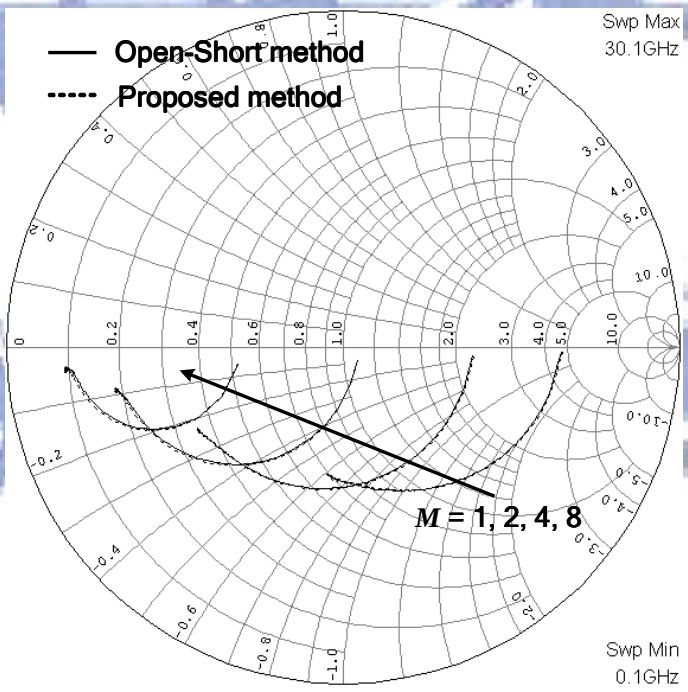



(b)

Fig. 3.7 De-embedded *S*-parameters of the fixtured MOSFETs with different multiplier factors ($M$ = 1, 2, 4, and 8) biased at $V_{GS}$ = 1.2 V and $V_{DS}$ = 1.2 V. (a) $S_{11}$. (b) $S_{12}$. (c) $S_{21}$. (d) $S_{22}$.




(c)




(d)

Fig. 3.7 De-embedded *S*-parameters of the fixtured MOSFETs with different multiplier factors ($M$ = 1, 2, 4, and 8) biased at $V_{GS}$ = 1.2 V and $V_{DS}$ = 1.2 V. (a) $S_{11}$. (b) $S_{12}$. (c) $S_{21}$. (d) $S_{22}$.

# CHAPTER 4. APPLICATION OF THE SCALABLE DE-EMBEDDING TECHNIQUE TO PROCESS MONITORING TEST STRUCTURES FOR RF DEVICE CHARACTERIZATION

## 4.1 Introduction

Device variations in an RF CMOS process are one of the most important issues for the fabrication and the design of silicon-based RFICs. Since circuit design calls for reliable and high-yield CMOS process to minimize the failures and frequency shifts, the relationships between the circuit designers and the process engineers should be intensified to make one-pass circuit design possible. As shown in Fig. 4.1, the conventional on-wafer test structures are usually laid out in the east-west configuration to characterize the RF devices. To monitor a process, the GSG probe pads of the test structures should be placed within a scribe line between two adjacent dies [20]-[21]. Therefore, the total width of the proposed in-line test structures typically should not exceed 100 μm. In addition, the corresponding de-embedding structures must be carefully designed to eliminate the parasitic effects of the probe pads and input/output access lines surrounding the device. In this chapter, we further apply the scalable de-embedding method [9] to the in-line test structures for process monitoring. The corresponding open and thru dummy structures within the scribe line are designed using the full-wave EM simulations. With the utilization of the shielding technique

[13], the electromagnetic energy can be localized along the microstrip-like access lines so that the substrate coupling can be reduced and the interconnect scalability can be improved. To verify the proposed in-line test structures, we measured the high-frequency characteristics of the devices fixtured in a die and in a scribe line, respectively. The DUTs and the de-embedding structures were fabricated using a standard CMOS process and characterized up to 20 GHz. We found that the proposed in-line test structure is very suitable for process monitoring and is capable of characterizing various devices in a scribe line.

## 4.2 RF Test Structures

### *4.2.1 On-Wafer and In-Line Test Fixtures*

As illustrated in Figs. 4.1 and 4.2, the on-wafer and in-line test fixtures are designed to mount the devices with the probe pads and interconnects. To monitor a process, the conventional on-wafer test fixture should be inserted into a scribe line and thus its GSG probe pads should be rearranged to access the device. The shielding technique is employed to isolate the silicon substrate. To investigate the effect of substrate coupling on the characteristics of test structures, the full-wave electromagnetic simulation based on the method of moment was also accomplished. As shown in Fig. 4.3, the forward coupling $Y_{FC}$ (= $-Y_{12}$) of open dummy decreases as the distance ($l$) between two signal pads increases. It is seen that the forward coupling can be mitigated by employing the bottom shielding. Besides,

the pad admittance $Y_{PAD}$ (= $Y_{11}$+$Y_{12}$) of the shielded open dummy is greater than that of the unshielded one due to the larger capacitance of the shielded open dummy.

### *4.2.2 Interconnect Characteristics*

Here the MOSFETs of the on-wafer and in-line test fixtures are laid out as close to the ground plates as permissible to minimize the parasitics of the dangling leg in source terminal [17]. However, care must be taken when determining the space between signal and ground traces to ensure the microstrip-like field distribution along the interconnects. Once the electromagnetic wave is propagated along the input/output interconnects within the limited space of the in-line test fixture, the substrate coupling between the signal and ground traces would be considerable and should be also taken into account for the analysis. To simplify this task, the bottom metal ($M_1$) can be connected to the ground pads to shield the lossy silicon substrate. Consequently, both substrate leakage and port-to-port coupling can be significantly mitigated [13]. Fig. 4.4 shows the effect of substrate coupling on the characteristic impedance. The unshielded interconnects with various signal-to-ground spacing ($S_g$) show different characteristic impedance while the shielded ones display close results. It is because the signal-to-ground spacing of the unshielded interconnects determines the field distribution along the interconnects and thereby affects the interconnect characteristics. These results also indicate that the shielding technique can be used to reduce the spacing between signal and ground traces and the consumption of chip area. As shown in Fig. 4.5, good interconnect

scalability over wide ranges of interconnect length and operation frequency is achieved by employing the bottom shielding.

As shown in Fig. 4.6, to remove the unwanted parasitics of the MOSFET test fixture, the parasitic networks composed of pad admittances and interconnect elements should be replicated from the open and thru dummies. Since here the shielding technique is employed, the equivalent-circuit model for the open dummy structures can be simply expressed as two independent input admittances. And the thru dummy structures can be modeled as shunt admittances and a lossy transmission line in cascade configuration. After scaling the interconnect parameters of the thru dummy, we can generate the parasitic networks of the input/output interconnects for de-embedding [9].

## 4.3 Results and Discussion

A 0.35 μm four-metal-layer RF CMOS process was used to fabricate the on-wafer and in-line MOSFET test fixtures. The NMOS transistors with the dimensions of channel length ($L_g$) = 0.35 μm and channel width ($W_g$) = 40 μm (5 μm × 8 fingers) were connected in a two-port common-source configuration. The line lengths of the 10-μm wide interconnects between pads and transistor are

On-wafer test fixture: $l_1$ = 95 μm, $l_2$ = 92 μm

In-line test fixture: $l_1$ = 195 μm, $l_2$ = 192 μm

where $l_n$ is the length of the interconnect at port $n$.

The interconnect lengths between the signal pads of the on-wafer and in-line thru dummy structures are 210 μm and 410 μm, respectively. The DC measurements of the MOSFET test fixtures were performed in the Kelvin connections with an Agilent 4142B Modular DC Source/Monitor, and the two-port *S*-parameter measurements were accomplished with an Agilent 8510C VNA and Cascade Microtech Infinity GSG probes. Before starting *S*-parameter measurements, the measurement system was calibrated using the SOLT calibration procedure.

The interconnect parameters $Z_C$ and $\gamma$ as functions of frequency can be extracted from the *S*-parameter measurements based on [14]. As shown in Fig. 4.7, the differences in characteristic impedance and the propagation constant between the on-wafer and in-line thru dummies are negligible and thus the interconnect scalability is guaranteed. This is because that here the shielding technique is applied to confine the electromagnetic energy in the vicinity of the microstrip-like interconnects. Moreover, the effect of contact resistance was mitigated by using the Infinity microwave probes [22], and the effects of step discontinuity [18] were also reduced by properly designing the junctions between the signal pads and the interconnects. Fig. 4.8 demonstrates the reflection coefficients ($S_{11}$ and $S_{22}$) and transmission coefficients ($S_{12}$ and $S_{21}$) of the on-wafer and in-line MOSFET test fixtures de-embedded using the standard open-short and scalable method, respectively. It is shown that the results obtained from the two different structures using two different de-embedding methods are in

excellent agreement over the entire frequency range. Based on the above results, the proposed scalable de-embedding method can be applied to the process monitoring test structures, and can be utilized to accurately and efficiently calculate the intrinsic parameters of both active and passive DUTs.

## 4.4 Conclusion

In this chapter, the shield-based scalable de-embedding method has been applied to the RF CMOS process monitoring test structures. With the application of shielding technique, full-wave EM simulations, and careful design of the pad-interconnect junctions, good interconnect scalability of both on-wafer and in-line thru devices can be achieved and the subtraction procedure of the external parasitics of DUTs can be simplified. The de-embedded RF characteristics of the proposed in-line process monitoring test structures agree well with that of the conventional on-wafer test structures. Compared with the standard open-short de-embedding method, the shield-based scalable de-embedding method used in process monitoring test structures also shows reliable results.

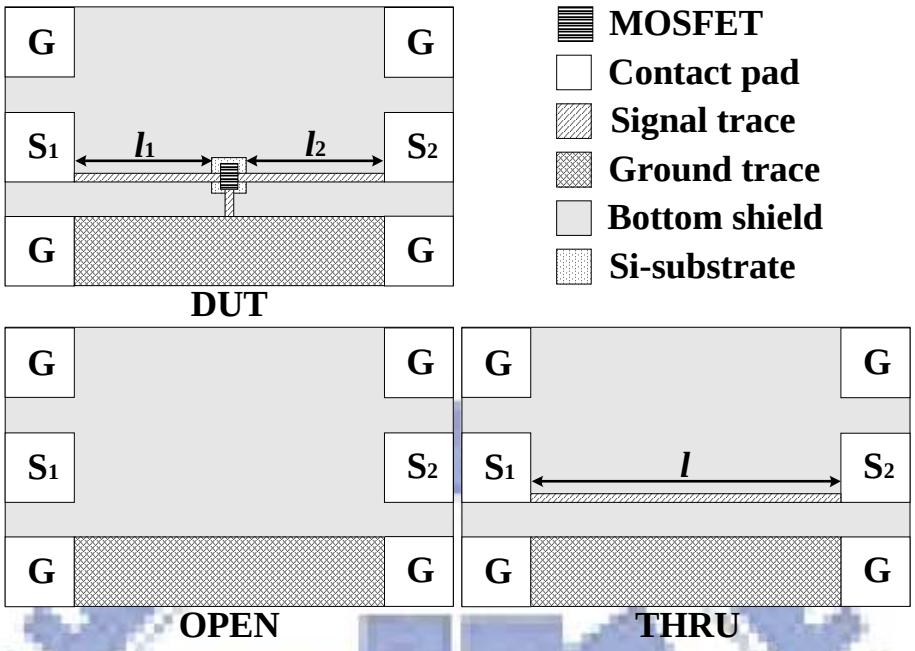



Fig. 4.1 Illustration of the conventional on-wafer test structures.

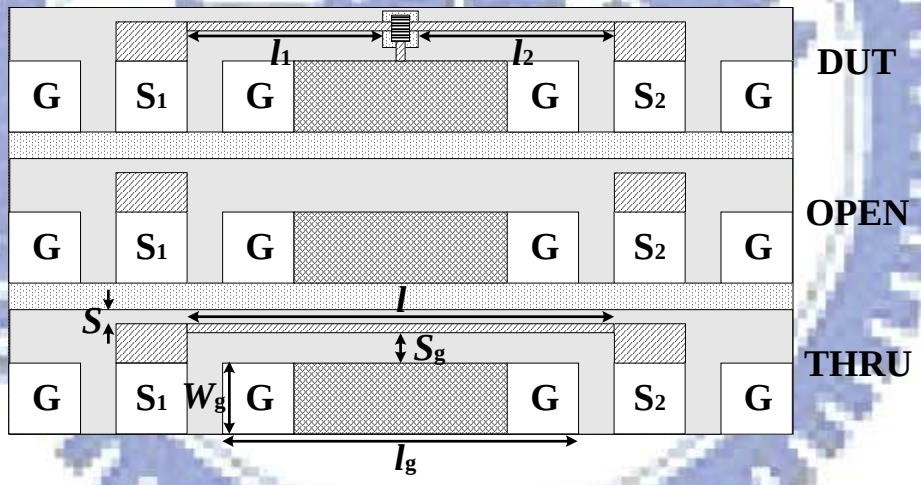



Fig. 4.2 Illustration of the proposed in-line process monitoring test structures.

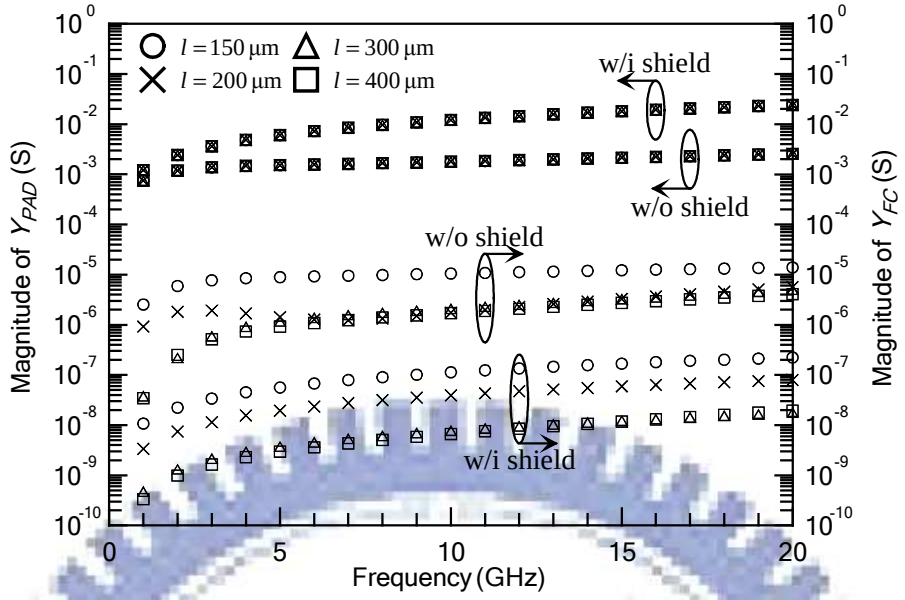



Fig. 4.3 EM-simulated forward coupling $Y_{FC}$ and pad admittance $Y_{PAD}$ of shielded and unshielded open dummy structures ($l$ = 150 – 400 μm).

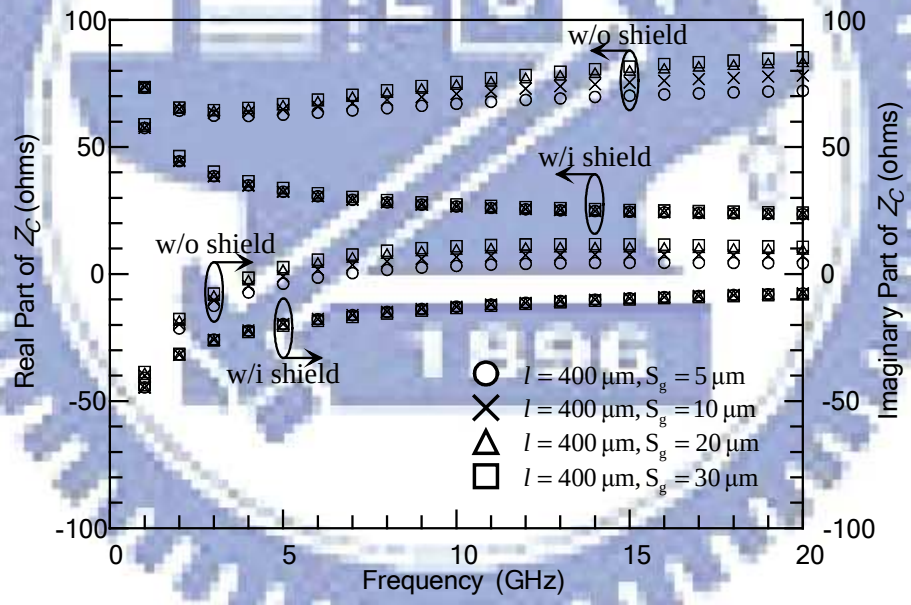



Fig. 4.4 EM-Simulated characteristic impedance ($Z_C$) of shielded and unshielded interconnects ($S_g$ = 5 – 30 μm).

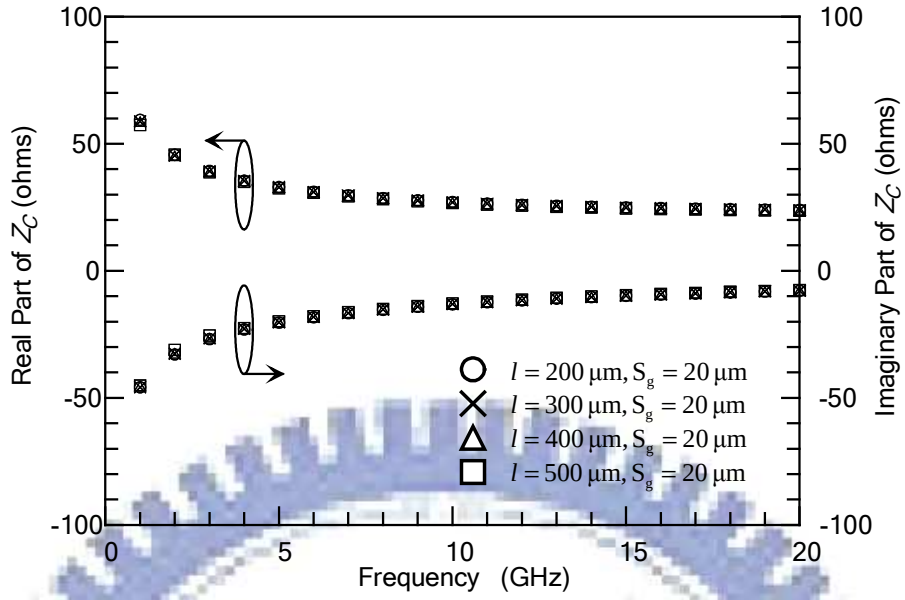



Fig. 4.5 EM-Simulated characteristic impedance ($Z_C$) of shielded interconnects ($l$ = 200 – 500 μm).

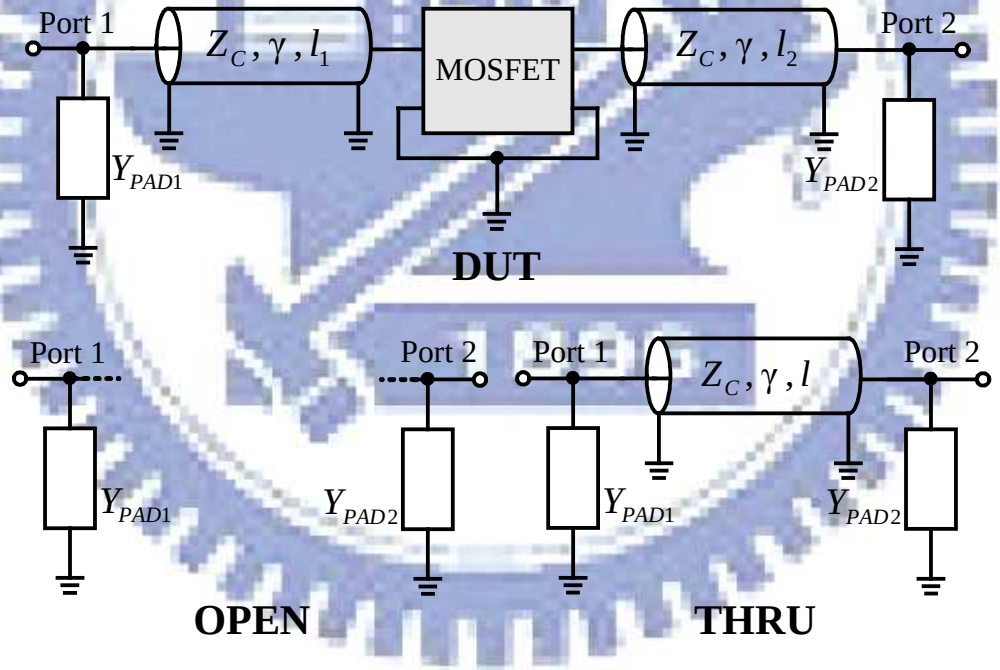



Fig. 4.6 Suggested parasitic models for the RF test structures.

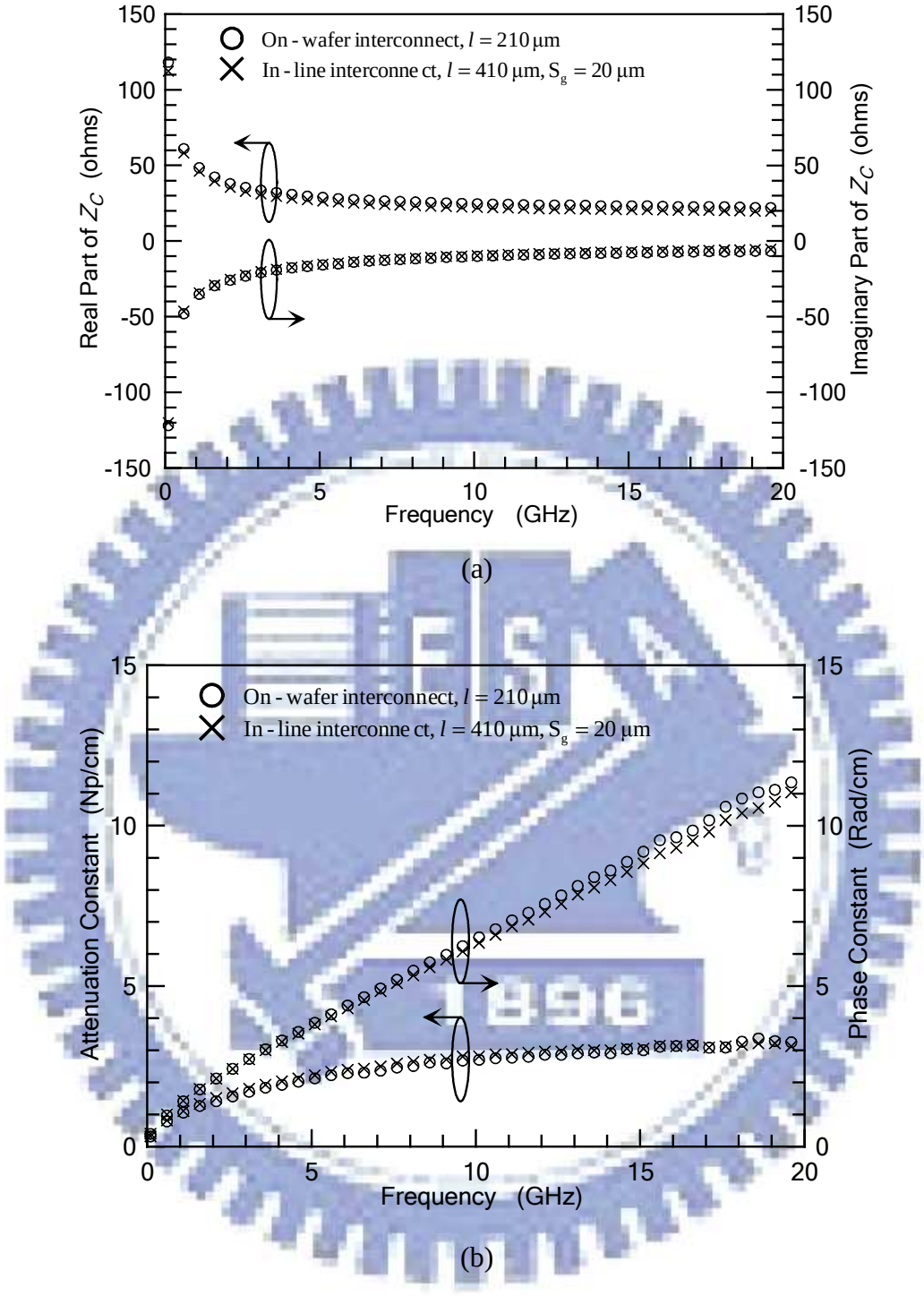



Fig. 4.7 Interconnect parameters of the conventional on-wafer and proposed in-line thru dummy structures extracted using the scalable de-embedding method. (a) Complex characteristic impedance. (b) Complex propagation constant.

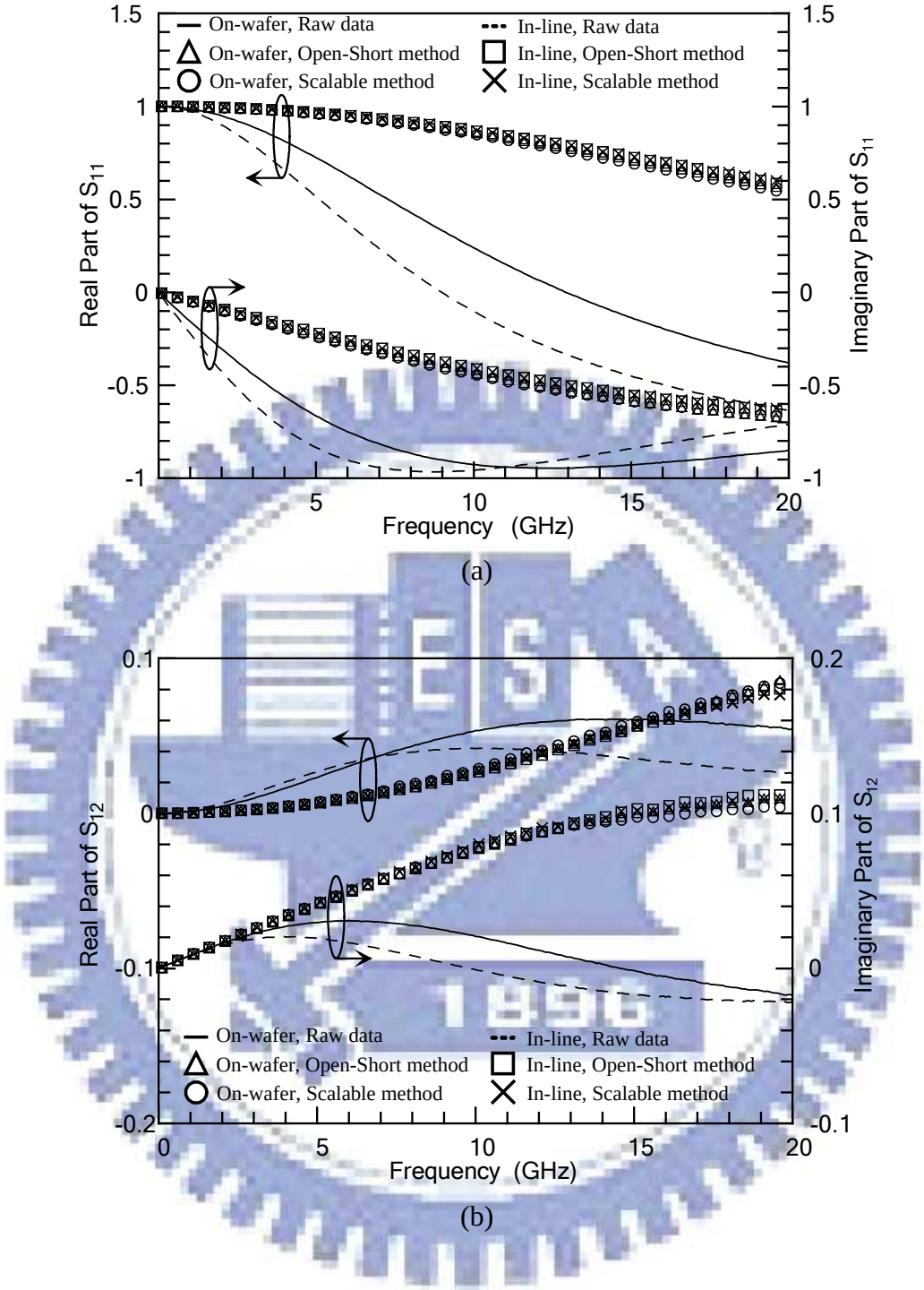



Fig. 4.8 *S*-parameters obtained from the conventional on-wafer and proposed in-line test structures using scalable de-embedding method and open-short de-embedding method. (a) $S_{11}$. (b) $S_{12}$. (c) $S_{21}$. (d) $S_{22}$. The MOSFET was biased at $V_G = V_D = 2$ V.

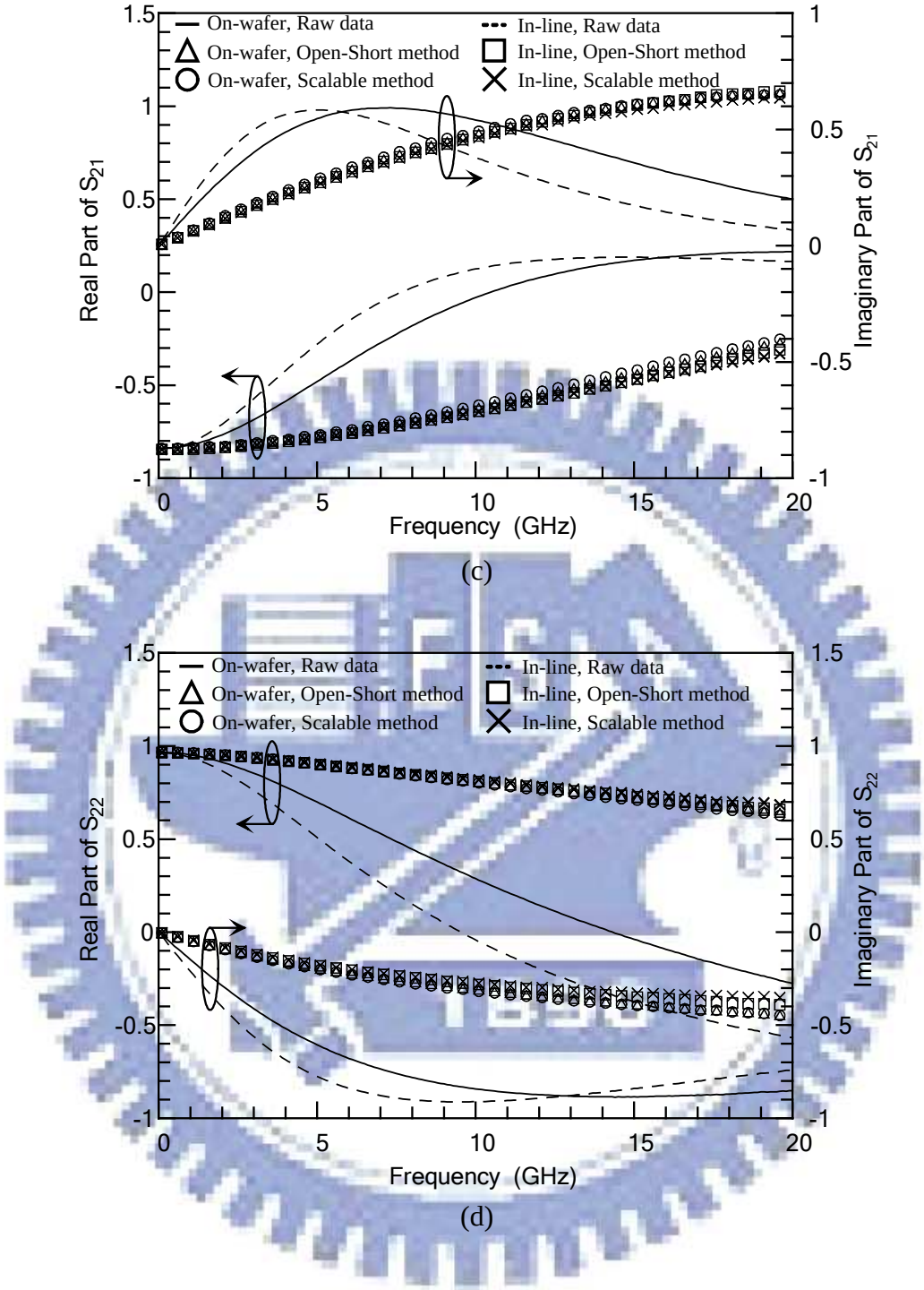



Fig. 4.8 *S*-parameters obtained from the conventional on-wafer and proposed in-line test structures using scalable de-embedding method and open-short de-embedding method. (a) $S_{11}$. (b) $S_{12}$. (c) $S_{21}$. (d) $S_{22}$. The MOSFET was biased at $V_G = V_D = 2$ V.

# CHAPTER 5. MINIATURE RF TEST STRUCTURE FOR ON-WAFER DEVICE TESTING AND PROCESS MONITORING

## 5.1 Introduction

With the progress of CMOS process technology, device unity-gain frequency has reached the microwave regime and beyond. It has become more and more significant for process engineers and circuit designers to characterize the silicon-based devices at such high frequencies. As shown in Fig. 5.1(a), a conventional on-wafer RF test structure is usually laid out in the east-west configuration. The microstrip-like interconnects are introduced to reduce the capacitive coupling between the device and probe pads. However, these access lines not only occupy considerable chip area, but also increase IR drop across them. In addition, the conventional on-wafer RF test structure is difficult to be inserted into the scribe line for process monitoring due to its specific configuration.

In previous literatures [20]-[21], the in-line RF test structures have been presented to monitor an RF CMOS process. As illustrated in Fig. 5.1(b), two GSG probe pads in these test fixtures are aligned in a row (or in a column) and thus can be placed within a scribe line. Although these in-line test structures are flexible and suitable for both on-wafer testing and process monitoring, they still consume much chip area and suffer from large IR drop and interconnect parasitics. Recently, an area-efficient RF test structure [23] was presented. As

shown in Fig. 5.1(c), this improved test structure rearranges the GSG probe pads to fit in a ground-signal-ground-signal-ground (GSGSG) probe and requires about 60 % of the chip area for a conventional on-wafer test structure. In this chapter, we propose a new compact layout to further reduce the chip area of RF test structures. As shown in Fig. 5.1(d), the MOS transistor is slightly off center to prevent the direct coupling from the signal pads to the device. Consequently, both the spacing between two GSG probe pads and the length of interconnect can be substantially reduced. By employing the shielding technique [13], the noise coupling through silicon substrate can be suppressed and the industry-standard open-short de-embedding method [2] can be used to accurately subtract the external parasitics surrounding the MOS transistor. This miniature RF test fixture consumes only 36 % chip area of a conventional on-wafer test structure and is suitable for characterizing and monitoring various devices such as MOSFETs, BJTs, varactors, capacitors, resistors, etc. To substantiate the proposed RF test structure, the MOS transistors and corresponding dummy structures were fabricated using a 90 nm RF CMOS process and characterized up to 30 GHz with a two-port *S*-parameter measurement system.

## 5.2 Miniaturization of RF Test Structures

### *5.2.1 Conventional On-Wafer and In-Line Test Fixtures*

As illustrated in Fig. 5.1(a), the conventional on-wafer RF test structure is designed to mount the devices with probe pads and interconnects. The gate and drain of a MOS transistor are respectively connected to the input and output signal pads while the source and bulk are tied together to the ground reference. Besides, the ground plane ($M_1$) is laid out as close to the MOS transistor as possible to minimize the IR drop and parasitic effects of the dangling leg in source terminal [17].

Figure 5.1(b) shows the conventional in-line test structure. To monitor a process, the on-wafer test structure should be inserted into a scribe line between two adjacent dies and hence its total width should be typically less than 100 μm [21]. Once the electromagnetic wave is propagated along the feeding networks within the in-line test fixture, the substrate coupling between the interconnects and ground traces would become considerable. To overcome this problem, the bottom metal layer can be connected to the ground reference to shield the semiconducting silicon substrate. As a result, both substrate coupling and port-to-port isolation can be significantly improved. As shown in Fig. 5.1(c), the GSGSG (or GSSG) RF probes also can be utilized to further reduce the length of interconnect [23].

### *5.2.2 Proposed Miniature RF Test Fixture*

Figure 5.2 shows the parasitic model of an RF MOSFET test structure. The shunt parasitics $Y_1$ and $Y_2$ are the admittances of probe pads and interconnects at the two ports, and $Y_3$ is the capacitive coupling between them. The series parasitics $Z_1$, $Z_2$, and $Z_3$ represent the

impedances of probe pads and interconnects in the gate, drain, and source terminals, respectively. Since here the shielding technique is introduced, the shunt and series parasitic networks surrounding a MOS transistor can be reproduced from the open and short dummy structures [2], [13] and subtracted out in *Y*- and *Z*-domains, respectively. For the design of RF MOSFET test structures, interconnects should be wide and short to reduce the IR drop across $Z_2$ and $Z_3$. As the spacing between two signal pads becomes shorter, however, care must be taken to avoid coupling from signal pads to the MOS transistor. Figure 5.3 shows that the measured probe-to-probe capacitance increases as the spacing between two face-to-face GSG probes decreases. This implies that the RF characteristics of a MOS transistor between two close signal pads will suffer from strong electric field and associated problems, which cannot be easily modeled.

To overcome these difficulties, we propose a miniature RF test structure suitable for on-wafer device testing and in-line process monitoring in this chapter. As illustrated in Fig. 5.1(d), the MOS transistor is located in an area between the signal and ground pads to prevent the electric field penetrating into the device. Therefore, the pad-to-pad spacing can be minimized and fixture size can be significantly reduced. Moreover, small signal pads (35 μm × 50 μm) and short interconnect (7 μm × 9 μm) are used to mitigate the coupling capacitance between pads as well as the voltage drop across interconnects. This miniature RF test fixture requires only 36 % and 40 % chip area of the conventional on-wafer and in-line test

structures, respectively, and it can be used for both device characterization and process monitoring.

## 5.3 Results and Discussion

A 90 nm nine-metal-layer RF CMOS process was used to fabricate the MOSFET test structures and de-embedding dummies. The NMOS transistors with the dimensions of channel length ($L_g$) = 90 nm and channel width ($W_g$) = 64 μm (4 μm × 16 fingers) were connected in a two-port common-source configuration. The DC and RF measurements of the on-wafer and in-line test fixtures were carried out on an HP 4142B Modular DC Source/Monitor and an Agilent 8510C VNA, respectively. Before *S*-parameter measurements, the system was calibrated up to 30 GHz using the SOLT. It should be noted that both DC and RF characteristics were measured with the same DUTs to mitigate the effects of process variation.

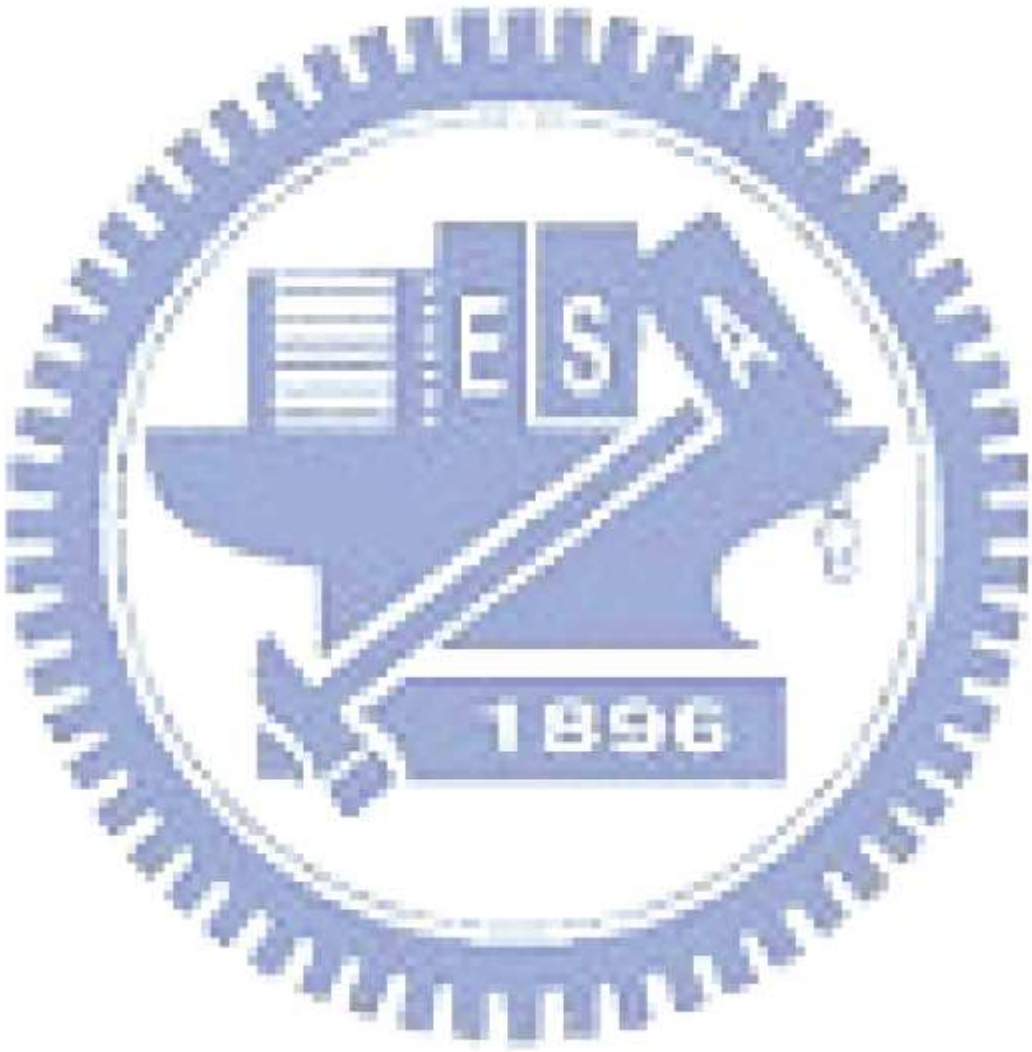
Figure 5.4 shows the measured DC $I_D$-$V_D$ curves of the on-wafer and in-line MOSFET test structures. Compared with the conventional test structures, the proposed miniature test structure demonstrates the highest drain currents under various gate/drain bias conditions. This indicates the IR drop across the interconnects will degrade the DC characteristics as well as the other parameters of the MOS transistors. Figure 5.5 displays the de-embedded reflection coefficients ($S_{11}$ and $S_{22}$) and transmission coefficients ($S_{12}$ and $S_{21}$) of the RF

MOSFET test fixtures. It is shown that the results obtained from the proposed RF test structure and the conventional ones, except the conventional in-line GSG structure, are in excellent agreement over the entire frequency range. This small inconsistency in the de-embedded *S*-parameters may be caused by the higher IR drop and/or the larger interconnect parasitics, which cannot be properly modeled by open-short de-embedding [8], of the conventional in-line GSG test structure. Figure 5.6 also shows no significant difference in gain-frequency response between the conventional and proposed test structures. Based on the above results, the proposed miniature RF test structure can be used to acquire reliable DC and RF characteristics of the MOSFETs and reduce the consumption of chip area. The fixture size of the proposed design is compact and could be further reduced, nevertheless, the pad size would be limited by the tip size and skating distance of the RF probe. Theoretically there is no lower limit for the pad-to-pad spacing that can be realized. However, care must be taken to ensure the probing consistency when two signal pads are placed as close as possible. For instance, the automatic measurement system can be applied to achieve good probing stability [24].

## 5.4 Conclusion

In this chapter, we propose a miniature RF test structure suitable for both device testing and process monitoring. With the application of shielding technique and careful design of the

probe pads and interconnects, the chip area of the proposed layout can be reduced to less than 40 % of the conventional ones. Compared with the conventional RF test structures, the proposed new design shows lowest voltage drop and consistent RF characteristics.



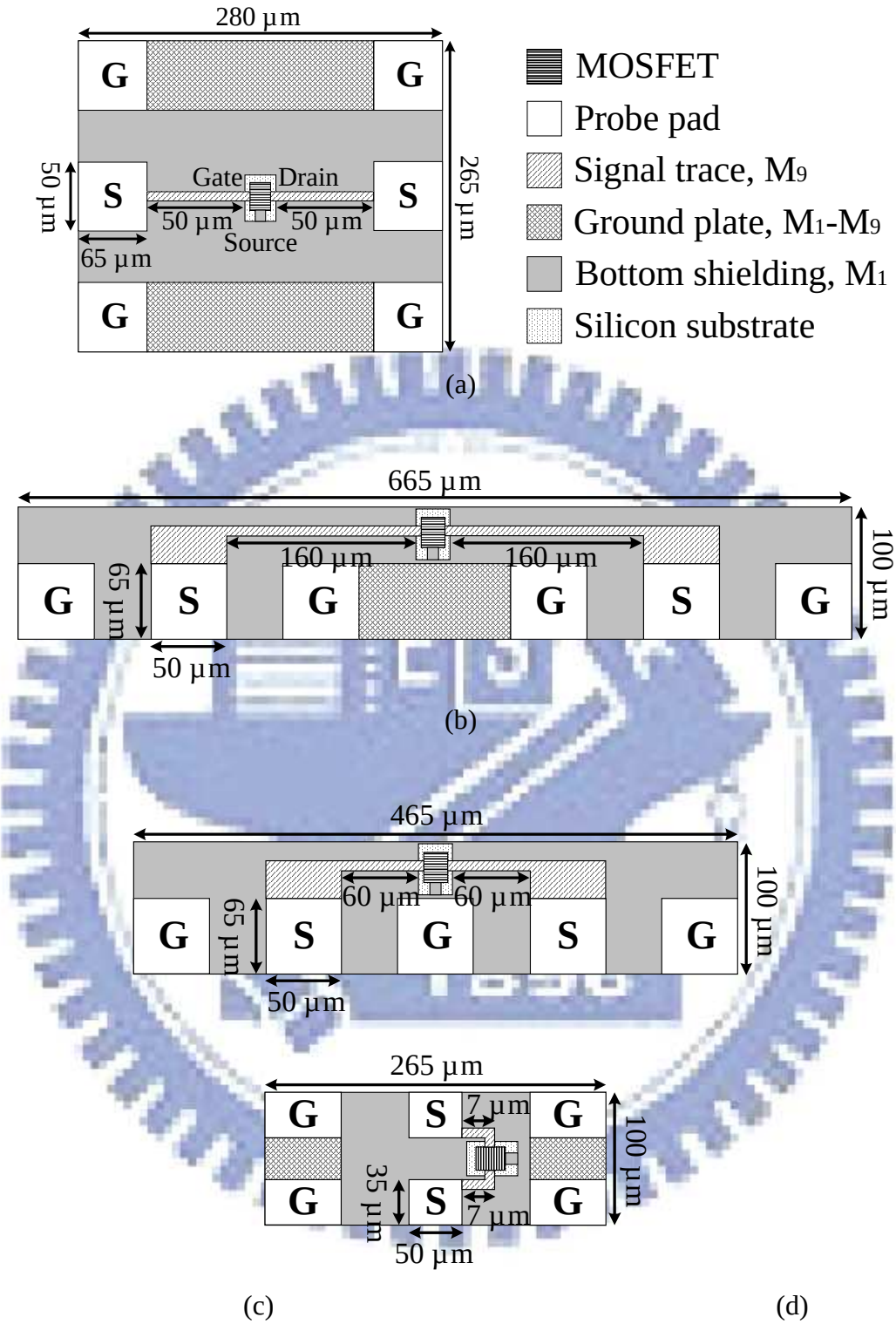



Fig. 5.1 Illustration of RF test structures for on-wafer device testing and in-line process monitoring. (a) Conventional on-wafer GSG test structure. (b) Conventional in-line GSG test structure. (c) In-line GSGSG test structure. (d) Proposed miniature GSG test structure. The width of interconnect is 9 µm and the estimated resistances of each interconnect for (a)-(d) are 0.27 Ω, 0.86 Ω, 0.32 Ω, and 0.04 Ω, respectively.

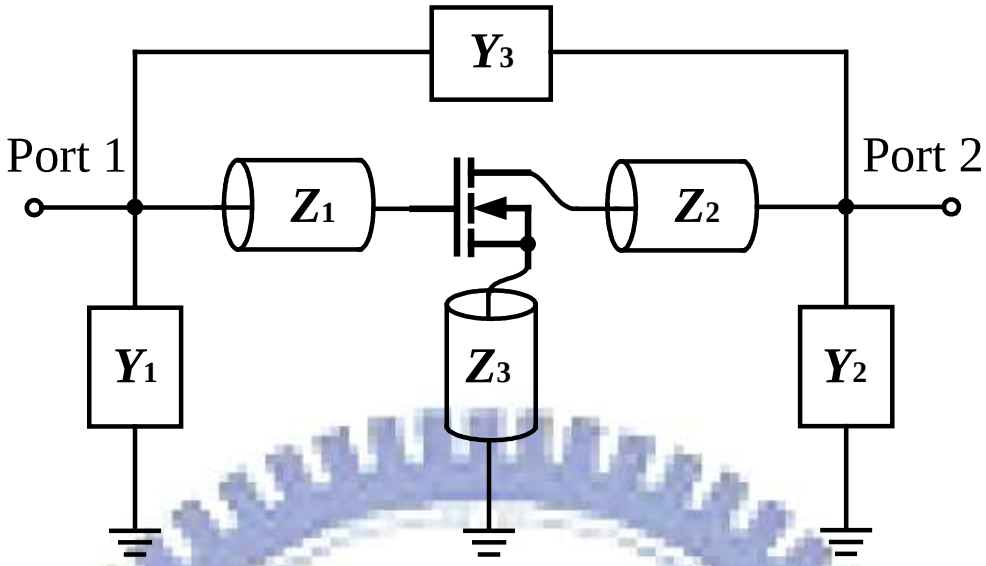



Fig. 5.2 Lumped equivalent-circuit representation of a fixtured MOS transistor for on-wafer device testing and in-line process monitoring.

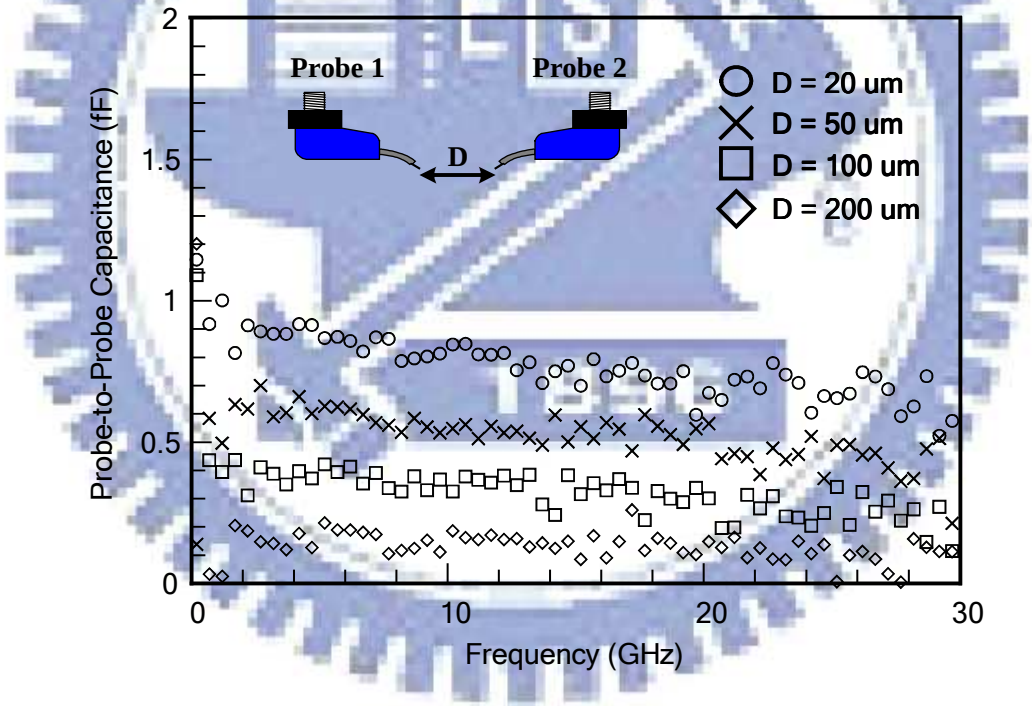



Fig. 5.3 Forward capacitive coupling between GSG RF Probes. Two Infinity probes were placed in air with different separation distances. The reference plane of each port was shifted to the probe tips using the short-open-load-thru calibration procedure.

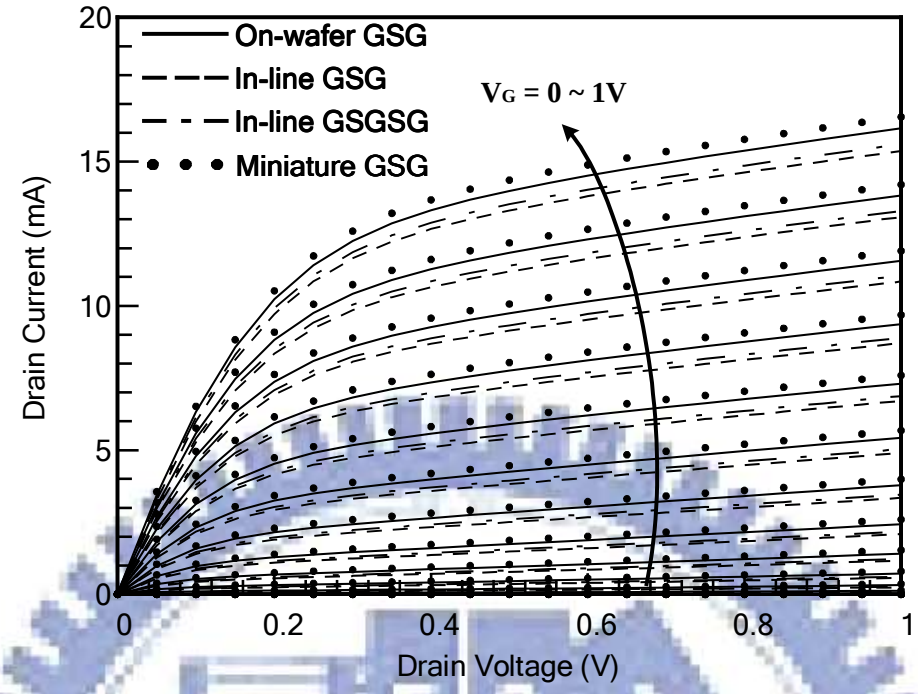



Fig. 5.4 DC characteristics obtained from the on-wafer and in-line MOSFET test fixtures. $I_D$-$V_D$ curves for $V_G$ = 0 – 1 V with 50 mV steps.

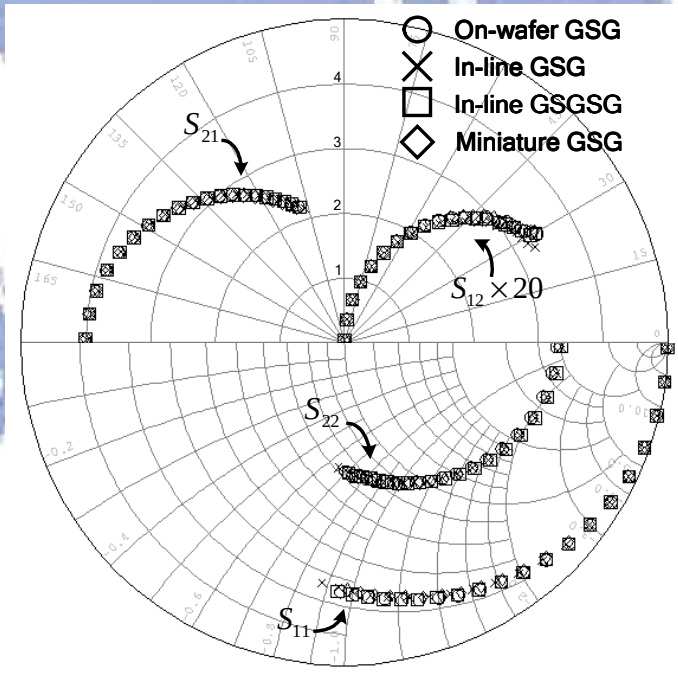



Fig. 5.5 *S*-parameters obtained from the on-wafer and in-line MOSFET test structures using standard open-short de-embedding method [2]. The MOSFETs were biased at $V_G$ = $V_D$ = 1 V and the *S*-parameters measurements were performed from 0.1 GHz to 30 GHz.

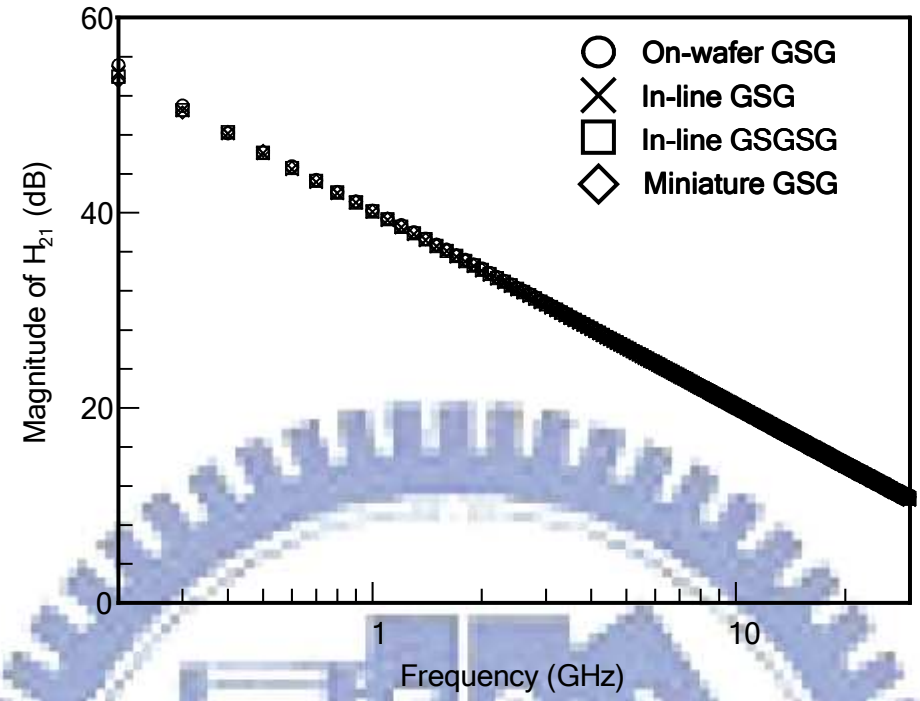



Fig. 5.6 Current gain $H_{21}$ as a function of frequency using standard open-short de-embedding method. The MOSFETs were biased at $V_G = V_D = 1$ V and the *S*-parameters measurements were performed from 0.1 GHz to 30 GHz.

# CHAPTER 6. CONCLUSIONS AND RECOMMENDATIONS

A systematic methodology of designing and de-embedding test structures for on-wafer microwave characterization has been developed and validated. In chapter 2, a length-scalable *S*-parameter and noise de-embedding method for on-wafer device characterization has been presented. The proposed method combines the physics-based and cascade-based de-embedding techniques to de-embed the parasitic networks in gate and drain terminals of a MOSFET. To further eliminate the parasitics of dangling leg in source terminal of the MOSFET, the microwave network analysis was also introduced to accomplish the two-port-to-three-port transformation for *S*-parameters. Both the fixture scalability of de-embedding standards and the de-embedding accuracy are verified up to 40 GHz. The de-embedded results indicate that the proposed method is accurate and efficient for characterizing silicon-based devices. In chapter 3, a geometry-scalable parasitic de-embedding method for characterizing multiple MOS transistors has been presented. The proposed method based on the transmission-line theory and microwave network analysis uses only two substrate-shielded dummy structures to de-embed the parasitic networks surrounding the global modeling test keys. Both the network combinations and the de-embedding accuracy of the proposed method are validated up to 30 GHz. These results indicate that the proposed method is accurate and efficient for evaluating the intrinsic device

characteristics of multiple devices. In chapter 4, the scalable de-embedding method has been applied to the RF CMOS process monitoring. With the application of shielding technique, EM simulations, and careful design of the in-line test structures, the intrinsic RF characteristics of the proposed in-line process monitoring test structures match well with those of the conventional on-wafer ones. In chapter 5, the RF test structure has been miniaturized for both device testing and process monitoring. The chip area of the proposed compact layout can be reduced to less than 40 % of the conventional ones.

Although the systematic microwave de-embedding approach for characterizing two-port devices proposed in this study is accurate, efficient, and flexible. The demand for future research work on wafer-level measuring techniques would still be evident. For example, the multi-port device characterization of coupled interconnects and devices requires reliable calibration and de-embedding techniques. In addition, the on-wafer device characterization in the millimeter-wave frequencies would be another tough challenge for RF engineers. Further studies should be conducted to extend this work to the multi-port and millimeter-wave device characterization