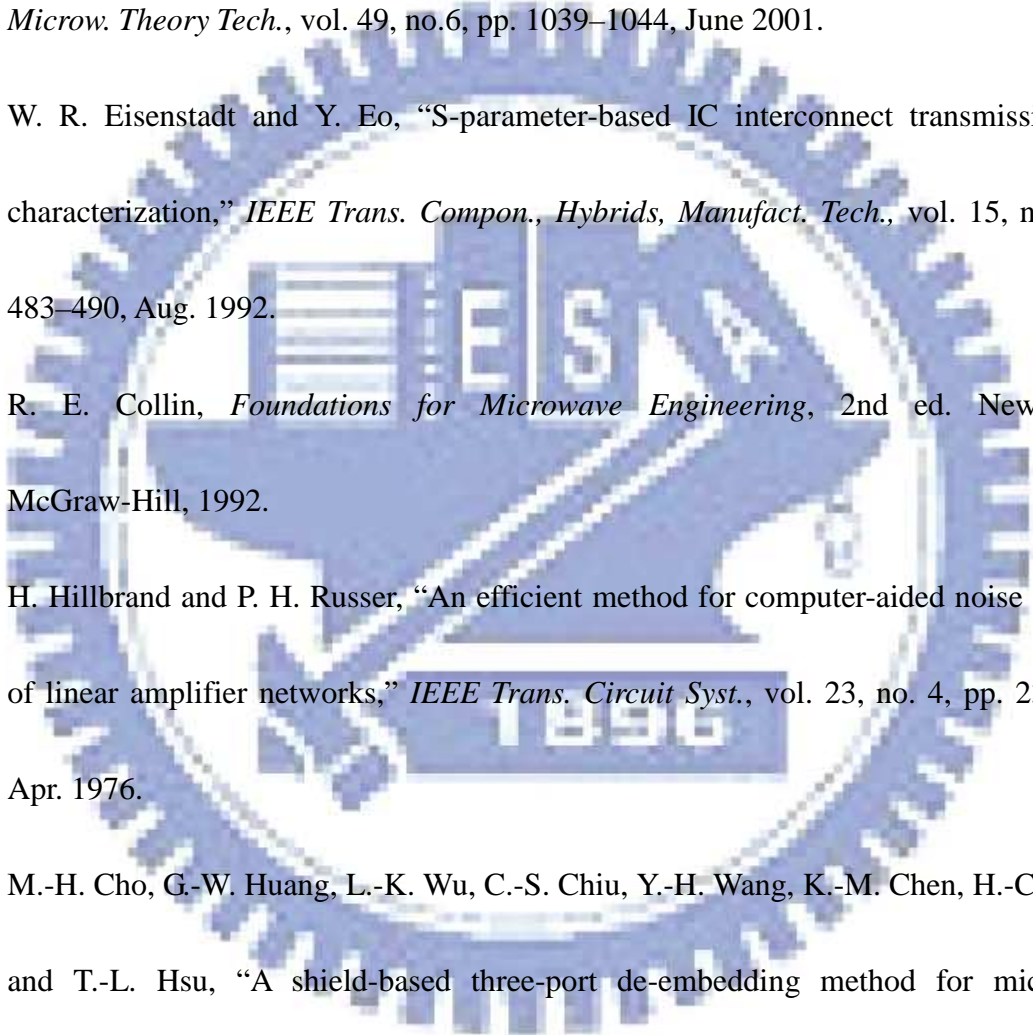


REFERENCES

- [1] P. J. van Wijnen, H. R. Claessen, and E. A. Wolsheimer, "A new straightforward calibration and correction procedure for "on-wafer" high-frequency S-parameter measurements (45 MHz–18 GHz)," in *IEEE Bipolar Circuits and Technol. Meeting*, Sept. 1987, pp. 70–73.
- [2] M. C. A. M. Koolen, J. A. M. Geelen, and M. P. J. G. Versleijen, "An improved de-embedding technique for on-wafer high-frequency characterization," in *Proc. IEEE Bipolar Circuits Technol. Meeting*, Sept. 1991, pp. 188–191.
- [3] H. Cho and D. E. Burk, "A three-step method for the de-embedding of high-frequency S-parameter measurements," *IEEE Trans. Electron Devices*, vol. 38, no.6, pp. 1371–1375, June 1991.
- [4] S. Lee, B. R. Ryum and S. W. Kang, "A new parameter extraction technique for small-signal equivalent circuit of polysilicon emitter bipolar transistors," *IEEE Trans. Electron Devices*, vol. 41, no.2, pp. 233–238, Feb. 1994.
- [5] T. E. Kolding, "A four-step method for de-embedding gigahertz on-wafer CMOS measurements," *IEEE Trans. Electron Devices*, vol. 47, no.4, pp. 734–740, Apr. 2000.
- [6] E. P. Vandamme, D. M. M.–P. Schreurs, and C. V. Dinther, "Improved three-step de-embedding method to accurately account for the influence of pad parasitics in

- silicon on-wafer RF test-structures,” *IEEE Trans. Electron Devices*, vol. 48, no. 4, pp. 737–742, Apr. 2001.
- [7] L. F. Tiemeijer and R. J. Havens, “A calibrated lumped-element de-embedding technique for on-wafer RF characterization of high-quality inductors and high-speed transistors,” *IEEE Trans. Electron Devices*, vol. 50, no. 3, pp. 822–829, Mar. 2003.
- [8] C.-H. Chen and M. J. Deen, “A general noise and S-parameter deembedding procedure for on-wafer high-frequency noise measurements of MOSFETs,” *IEEE Trans. Microw. Theory Tech.*, vol. 49, no.5, pp. 1004–1005, May 2001.
- [9] M.-H. Cho, G.-W. Huang, K.-M. Chen, and A.-S. Peng, “A novel cascade-based de-embedding method for on-wafer microwave characterization and automatic measurement,” in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.*, June 2004, pp. 1237–1240.
- [10] M.-H. Cho, G.-W. Huang, C.-S. Chiu, and K.-M. Chen, “Unified parasitic de-embedding methodology of on-wafer multi-port device characterization,” in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.*, June 2005, pp. 1307–1310.
- [11] M.-H. Cho, C.-S. Chiu, G.-W. Huang, Y.-M. Teng, L.-H. Chang, K.-M. Chen, W.-L. Chen, “A fully-scalable de-embedding method for on-wafer S-parameter characterization of CMOS RF/microwave devices,” in *Proc. IEEE RFIC Symp. Dig.*, June 2005, pp. 303–306.

- 
- [12] M.-H. Cho, G.-W. Huang, Y.-H. Wang, and L.-K. Wu, "A scalable noise de-embedding technique for on-wafer microwave device characterization," *IEEE Microw. Wireless Compon. Lett.*, vol. 15, no. 10, pp. 649–651, Oct. 2005.
- [13] T. E. Kolding, "Shield-based microwave on-wafer device measurements," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no.6, pp. 1039–1044, June 2001.
- [14] W. R. Eisenstadt and Y. Eo, "S-parameter-based IC interconnect transmission line characterization," *IEEE Trans. Compon., Hybrids, Manufact. Tech.*, vol. 15, no.4, pp. 483–490, Aug. 1992.
- [15] R. E. Collin, *Foundations for Microwave Engineering*, 2nd ed. New York: McGraw-Hill, 1992.
- [16] H. Hillbrand and P. H. Russer, "An efficient method for computer-aided noise analysis of linear amplifier networks," *IEEE Trans. Circuit Syst.*, vol. 23, no. 4, pp. 235–238, Apr. 1976.
- [17] M.-H. Cho, G.-W. Huang, L.-K. Wu, C.-S. Chiu, Y.-H. Wang, K.-M. Chen, H.-C. Tseng, and T.-L. Hsu, "A shield-based three-port de-embedding method for microwave on-wafer characterization of deep-submicrometer silicon MOSFETs," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 9, pp. 2926–2934, Sept. 2005.
- [18] C. Gupta and A. Gopinath, "Equivalent circuit capacitance of microstrip step change in width," *IEEE Trans. Microw. Theory Tech.*, vol. 25, no. 10, pp. 819–822, Oct. 1977.

- [19] G. Gonzalez, *Microwave Transistor Amplifiers: Analysis and Design*. 2nd ed. Englewood Cliffs, NJ: Prentice-Hall, 1997.
- [20] J. L. Carbonero, G. Morin, and B. Cabon, "A full automatic on-wafer high frequency measurement station in industrial environment for silicon devices," in *Proc. 45th ARFTG Conference Dig.*, May 1995, pp. 83-91.
- [21] C. B. Sia, B. H. Ong, K. M. Lim, K. S. Yeo, M. A. Do, J. G. Ma, and T. Alam, "A novel RFCMOS process monitoring test structure," in *Proc. IEEE Int. Conference on Microelectronic Test Structures*, Mar. 2004, pp. 45-50.
- [22] J. L. Carbonero, G. Morin and B. Cabon, "Comparison between beryllium-copper and tungsten high frequency air coplanar probes," *IEEE Trans. Microw. Theory Tech.*, vol. 43, pp. 2786-2793, Dec. 1995.
- [23] C.-S. Chiu, G.-W. Huang, D.-Y. Chiu, K.-M. Chen, M.-H. Cho, and S.-C. Wang, "A novel process-controlled-monitor structure suitable for RF CMOS characterization," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.*, June 2005, pp. 1299-1302.
- [24] G.-W. Huang, D.-Y. Chiu, K.-M. Chen, Y.-M. Deng, and S.-C. Wang, "An automatic program suitable for on-wafer characterization and statistic analysis of microwave devices," in *Proc. 61st ARFTG Conference Dig.*, June 2003, pp. 157-161.

PUBLICATION LIST

A. Journal Papers:

- [1] **M.-H. Cho**, R. Lee, A.-S. Peng, D. Chen, C.-S. Yeh, and L.-K. Wu, "Miniature RF Test Structure for On-Wafer Device Testing and In-Line Process Monitoring," *IEEE Transactions on Electron Devices*, vol. 55, No. 1, pp. 462-465, Jan. 2008.
- [2] **M.-H. Cho**, Y.-H. Wang, and L.-K. Wu, "Scalable Short-Open-Interconnect S-Parameter De-Embedding Method for On-Wafer Microwave Characterization of MOSFETs," *IEICE Transactions on Electronics*, vol. E90-C, No. 9, pp. 1708-1714, Sept. 2007.
- [3] **M.-H. Cho**, G.-W. Huang, Y.-H. Wang, and L.-K. Wu, "A Scalable Noise De-Embedding Technique for On-Wafer Microwave Device Characterization," *IEEE Microwave and Wireless Components Letters*, vol. 15, No. 10, pp. 649-651, Oct. 2005.
- [4] **M.-H. Cho**, G.-W. Huang, L.-K. Wu, C.-S. Chiu, Y.-H. Wang, K.-M. Chen, H.-C. Tseng, and T.-L. Hsu, "A Shield-Based Three-Port De-embedding Method for Microwave On-Wafer Characterization of Deep-Submicrometer Silicon MOSFETs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, No. 9, pp. 2926-2934, Sept. 2005.
- [5] **M.-H. Cho** and L.-K. Wu, "A Novel Electrically Tunable RF Inductor with Ultra-Low Power Consumption," to be published in *IEEE Microwave and Wireless Components Letters*.
- [6] **M.-H. Cho**, D. Chen, R. Lee, A.-S. Peng, C.-S. Yeh, and L.-K. Wu, "Geometry-Scalable Parasitic De-Embedding Methodology for On-Wafer Microwave Characterization of MOSFETs," submitted to *IEEE Transactions on Microwave Theory and Techniques*.

B. Conference Papers:

- [1] S. Kapur, D.E. Long, R.C. Frye, Y.-C. Chen, **M.-H. Cho**, H.-W. Chang, J.-H. Ou, and B.-C. Hung, "Synthesis of Optimal Baluns," 2007 *IEEE Custom Integrated Circuits Conference (CICC)*, Sept. 2007.
- [2] **M.-H. Cho**, Y.-H. Wang, G.-W. Huang, D. Chen, B.-C. Hung, C.-S. Chiu, and L.-K. Wu, "A Flexible De-Embedding Method for On-Wafer Noise Parameter Characterization of MOSFETs," submitted to 38th *European Microwave Conference (EuMC) 2008*.
- [3] **M.-H. Cho** and L.-K. Wu, "A Novel Electrically Tunable On-Chip Inductor with Close-to-Zero Power Consumption," submitted to 38th *European Microwave Conference (EuMC) 2008*.
- [4] **M.-H. Cho**, Y.-H. Wang, and L.-K. Wu, "Shield-Based Scalable De-Embedding Technique for Process Monitoring and Device Characterization," submitted to 38th *European Microwave Conference (EuMC) 2008*.

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