國 立 交 通 大 學

電信工程學系

博 士 論 文

側向擴散金氧半電晶體之多諧波失真模型及表面聲波氣體感測器之設計

Polyharmonic Distortion Model for LDMOS Device and SAW Gas Sensor Design

研 究 生：邱佳松 (Chia-Sung Chiu)

指導教授：吳霖堃 (Lin-Kun Wu)

中 華 民 國　九十八　年 七 月

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博士論文

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摘要

本論文主要針對主動元件在不同佈局結構、非線性模型與感測領域進行分析與應用。一般而言，半導體裡的主動元件，例如金氧半場效電晶體(MOSFET)或雙極性接面電晶體(BJT)，為無線通訊系統或感測系統中最重要的元件之一。其元件特性足以影響應用系統裡的整體表現、價格與穩定性。而在一般無線通訊領域或基地台等遠距離的發射器，大都以側向擴散金氧半電晶體(laterally-diffused MOS transistor)作為主要之放大元件。在本研究中，首先提出了側向擴散金氧半電晶體之新型佈局樣式，利用圓形佈局樣式以達到低開啟通道電阻(On-resistance)與小面積的元件佈局。依據實驗的量測結果，圓形的佈局樣式因有較小的寄生電容與較高之轉導增益，所以有較高的截止頻率(f_T)與最大震盪頻率(f_{max})。除了小訊號分析外，論文中也進行大訊號特性分析比較。而在研究的量測結果，與傳統佈局樣式比較之下，圓形佈局樣式亦有較佳之大訊號特性表現。

除了功率元件佈局設計外，主動元件之非線性特性模型在設計與應用上也相形重要。在研究中，我們分析了多諧波失真模型，並且利用此模型模擬出主動元件的非線性

行為。經由晶圓級非線性向量網路分析儀所萃取出之多諧波失真模型，在1.9GHz的操作頻率點，射頻側向擴散金氧半電晶體的大訊號特性模擬結果與傳統功率量測的結果一致，並且無需另外進行電腦最佳化與曲線近似處理。

論文中的另一部分，我們利用了半導體中的主動元件與表面聲波(Surface acoustic wave, SAW)延遲線元件進行感測器之設計與分析。研究中針對了元件的特性，進行此感測器之電性測試與氣體感測結果分析。在感測的實驗結果中，表面聲波感測器在$50x10^3$ppm的酒精氣體濃度裡，其中心訊號有近10kHz的訊號漂移。研究的最後並針對感測元件與系統，提出改進及可能的發展方向。

Polyharmonic Distortion Motel for LDMOS Device and SAW Gas Sensor Design

Student: Chia-Sung Chiu Advisor: Dr. Lin-Kun Wu

Department of Communication Engineering

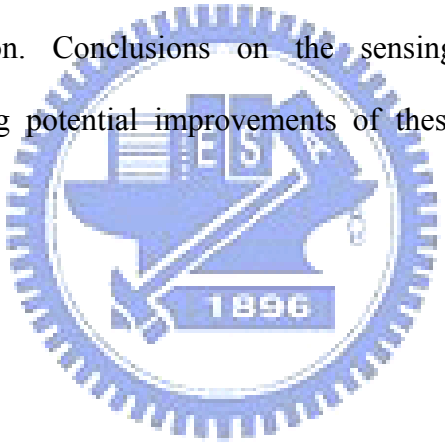
National Chiao Tung University

Abstract

This dissertation presents the layout design, nonlinear modeling and sensing application in terms of active device. The active device, such as MOSFET or BJT in semiconductor, is one of the most important components of a wireless communication or sensing system generally. It plays a significant part in determining the overall performance, cost, and reliability of these application systems. In the world of RF wireless communications, the base-stations and long range transmitters use silicon laterally-diffused MOS (LDMOS) high power transistors almost exclusively. To achieve lower on-resistance and a more compact device size, this study adopted an annular structure in the layout design. According to the measurement results, the smaller drain parasitic resistance in the annular structure could be the key factor for improving f_t and f_{max}. In additional to the small-signal analysis, the large-signal characteristics, such as power gain and power added efficiency, were also improved compared to the transitional structure of LDMOS.

In addition to high power device design, the behavior model of the nonlinear characteristics for active device is also crucial. In this study, we analyze the polyharmonic distortion model (PHD) and use this model to predict the nonlinear behavior of active device. By way of the PHD model extracted using on-wafer nonlinear vector network analyzer (NVNA), the large-signal validation of this model also shows a good match with measurements at 1.9 GHz without optimization and curve fitting.

In another part of this thesis, we discussed and analyzed the sensor design completely using CMOS active device and SAW delay-line device. Their electrical characteristics are evaluated as well as vapor sensing results. The sensing experimental results show that the maximum oscillation frequency shift between gas on and off is approximately 10 kHz with 50 x 10^3 ppm alcohol vapor concentration. Conclusions on the sensing device and system, and recommendations concerning potential improvements of these components are discussed, finally.



誌　謝

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邱佳松 謹誌

于 新竹交通大學

中華民國九十八年七月

Contents

List of Figures

Chapter 1

Chapter 2

Chapter 3

Chapter 4

Appendix

List of Table

Appendix

Chapter 1

Introduction

1.1 Introduction

So far, the RF transistor plays a role in power amplifier, sensor or other application [1-6]. They usually are designed to handle high-power signals or use as high-speed switch. Like other semiconductor devices, they are made of materials such as silicon or germanium. There are several basic types of RF transistors in foundry process. Bipolar RF transistors consist of an N-type or P-type layer embedded between two layers. Both NPN and PNP configurations are available. MOSFET RF transistors are metal-oxide-semiconductor field effect transistors with a channel made of either an N-type or P-type substrate. The Lateral-Diffused MOS (LDMOS) transistors for microwave operation were demonstrated in 1972 [7]. They are traditionally used in switching applications for a high voltage device and first designed to the RF power application in the early 70's. A traditional RF LDMOS transistor is shown in Fig. 1.1.

The radio frequency (RF) power amplifier is one of the most important components of a wireless communication system. It plays a significant component in determining the overall performance, cost, and reliability of the wireless system. The progress made on their technology over the last few years now make them usable in systems, and hence, there is a

need for electrical model. Many topologies and solutions to extract models are reported in the literature [8-10].

In addition to wireless commutation application, the market for RF amplifier used in sensing system has grown rapidly in recent years [11-13]. Silicon based CMOS RF transistors have been used for sensor technologies in some areas like chemical, biological, and gas detection. Next generation device or circuit design will focus on increased sensor selectivity and sensitivity, reduction of both system size and cost, and improved detection times. However, when semiconductors are not the optimum materials for a particular sensor type, reaction part of the sensor can be separated from the semiconductor substrate to form the sensor usually (e.g., a surface-acoustic-wave reaction device fabricated in quartz and amplifier circuit designed in silicon). These approaches can lead to the possibility of integrating the sensors with reaction component and microelectronics circuits.

1.2 Motivation

By way of scaling down the gate length or the drift length, the performance can be obviously improved with lower on-resistance and higher transconductance. However these scaling approaches may restrict the high-voltage endurance during power amplifying operation. In the conventional LDMOS devices, these are a trade-off between the drain current and the breakdown voltage, as well as between the on-resistance and the breakdown

voltage. Some solutions have been presented in term of these trade-offs such as using a double-doped offset [14], or a step drift region [15], or even the strain structure [16]. Instead of the device process modification, the trade-off between the on-resistance and the breakdown voltage can also be solved by optimizing the layout design. In this thesis, three types of layout structures, fishbone, square-type, and annular-type, were investigated and compared for DC, high-frequency, and RF power characteristics. In addition, the device capacitances have large impact on device high-frequency performance and large-signal characteristic. The capacitance characterization and modeling of LDMOS transistors have been studied widely [17-19]. Therefore, this thesis also analyzes the capacitances of RF LDMOS transistor in varied structures.

Besides device cell optimization, the model fabrication is also the important role in circuit or system design. Several different models have been developed for both bipolar and FET devices [20][21]. However, many of the traditionally used models are not very suitable for RF power amplifier design. Analytical or compact models are commonly used, and consist of circuit models where some elements are non-linear. The parameters of this type model are generally determined by a series of small signal and DC measurements. But this is generally a time consuming process, and often is accurate only over a limited range of operation. This study presents the PHD large-signal model which solves the extrapolation problem because it is based on device X-parameter measurement under actual large-signal operation.

The numerous wafer-level sensor systems using active device and sensing component have been investigated for sensing application [22][23]. However, these design methods lack the flexibility of system tuning, and the reaction component in the sensor system is usually expendable. Therefore, this study we design an active circuit in standard process with a SAW device on quartz to fabricate a sensor and detect the alcohol vapor.

1.3 Dissertation Organization

In this section a brief outline of this dissertation will be given as following. Chapter 1 gives a brief introduction which introduces active device in different aspect and study motivation. Chapter 2 presents an annular-type layout structure of RF LDMOS. The DC, high-frequency and RF power performance were analyzed and compared to traditional structure. This chapter also presents the unusual behavior in capacitance of RF LDMOS with square and annular structures. Chapter 3 describes the theory of polyharmonic distortion model and show the measurement and simulation results of RF LDMOS transistor in annular structure. Chapter 4 presents the sensor circuit design using active device and SAW device. The fabrication of SAW devices and the related oscillating circuit using active device in CMOS process are investigated in this study. The final chapter summarizes this study.

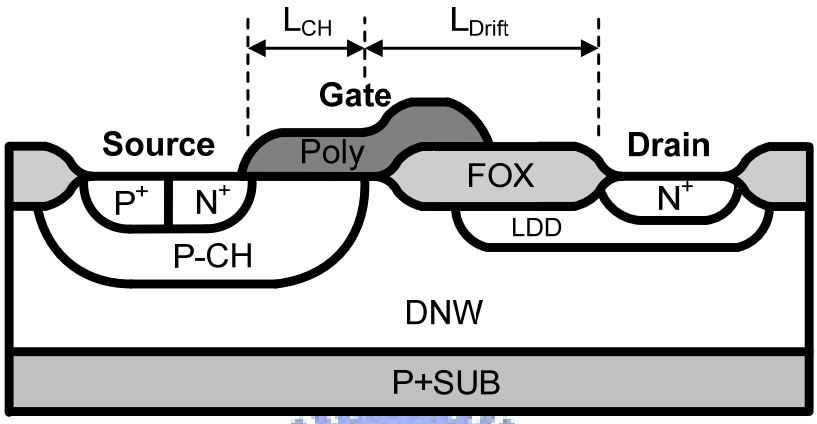


Fig. 1.1 A cross section of traditional high-power LDMOS transistor.

Chapter 2

Characterization of Annular-structure RF LDMOS

2.1 Introduction

Silicon laterally diffused metal oxide semiconductor (LDMOS) transistors have been of great interest due to their applications in RF amplifiers in wireless communication systems or base-stations [24]. LDMOS transistors provide several advantages, including high efficiency, low cost and good linearity capability on silicon substrates. Scaling down the gate length or the drift length of LDMOS transistors improves their performance by producing lower on-resistance and higher transconductance. However these scaling approaches may limit high-voltage endurance during power-amplifying operations.

In addition to scaling down the device or changing device processes, researchers have studied several transistor layout styles in their search for the best device performance [25]. These designs must deal with the tradeoff between layout area and reduced parasitic. The results presented in this study show that closed transistors offer many promising characteristics. The most widely used closed topology is the square-structure transistor as shown in Fig. 2.1. The square-structure transistor has lower on-resistance and higher transconductance, as described in [26]. However, square-structure corners contribute very little to the current drive but significantly increase the gate input capacitance [27]. If the

applied voltage is high with respect to the channel length, the electric field in the corners could break the device. In this case, a circle-type layout, called an annular structure in this paper, would be the optimum layout type for ensuring the most uniform current flow. However, some works are only published in a square shape or polygonal shape due to foundry process restrictions [28][29]. Besides, this study also performs the capacitance analysis. Due to the capacitance influence of the input and output of enclosed devices, which are significant in dynamic operation and have an impact on device high-frequency performance, many studies have been published on the capacitance characterization and modeling of LDMOS transistors [30-32].

2.2 Annular-structure RF LDMOS

2.2.1 Device Design and Fabrication

In this study, fabricates the annular-structure RF LDMOS transistors were fabricated using a 0.5 μm LDMOS process. The standard LDMOS layout consists of a source and a drain separated by a channel of width W and length L. An annular-structure LDMOS consists of a transistor with the source diffusion in the middle, encircled by the gate channel and the drain diffusion to achieve a lower ON-resistance [33]. The channel width for annular structure is the length of the curve lying at mid-channel.

Figures 2.2 and 2.3 show the die photo and single cell layout of an annular-structure LDMOS transistor. Figure 2.4 illustrates the schematic cross section of this device. The gate oxide thickness was 135 Å and the mask channel length (L_{CH}, shown in Fig. 1.1) was 0.5 μm. The drift length ($L_{Drift}=L_{OV}+L_{FOX}$) was 2.4 μm. The drain region was extended under the field oxide (FOX), consisting of a lightly doped N-well drift region and an N region with higher doses for on-resistance control. This design ties the source region and the p-body together to eliminate extra surface bond wires, reduce the source inductance, and improve the RF performance in a power amplifier [34]. This study optimizes the LDMOS transistor layout for high-frequency performance with a GSG structure adapted for on-wafer measurement.

2.2.2 DC Characteristics

Generally speaking, the DC characteristics of LDMOS are similar to the MOSFET. Nevertheless, at high drain voltages, the MOSFET suffers a breakdown caused by the high voltage across the oxide at the drain end of the gate, resulting in high gate-drain current flow. Another effect arising from the high electric field in this region is hot-carrier injection. However, in the LDMOS structures, these high-field effects are mitigated. The use of a lightly-doped n-type region at the drain end of the gate moves the heavily-doped drain contact region away from the high field region, and has a number of benefits. The lightly-doped semiconductor can support a high voltage, enabling the high RF voltage swing required for a

high-power device. The electric field in saturation at the drain edge of the gate is reduced, thereby reducing the hot-carrier injection and increasing the gate breakdown voltage [35].

The LDMOS transistor with larger L_{Drift} revealed a lower drain current and transconductance. Moreover, the breakdown voltage was higher with a larger L_{Drift} device. For a larger L_{Drift}, the higher resistance in the drift region results in a large voltage drop which increased the carrier velocity and go into the velocity saturation easily. The velocity saturation in the drift region is called "quasi-saturation" while intrinsic MOS is still in linear operation. This effect is generally observed at high gate voltages. When the device go into the quasi-saturation, the gate control ability decreases which limits the drain current level and delays the transition between linear and saturation region [36].

2.2.3 High-frequency Characteristics

Through small-signal equivalent circuit analysis of a MOSFET, we can realize the effect of device parameters on high-frequency characteristics easily. We adopted a simple equivalent circuit of the LDMOS by the method described in [37]. The equivalent circuit is shown in Fig. 2.5. After de-embedding the extrinsic parasitic resistances and the substrate-related parameters, the intrinsic components can be directly extracted from intrinsic Y-parameters by the following equations [38]:

$$C_{gd} = -\frac{1}{\omega}\mathrm{Im}(Y_{12}) \tag{2.1}$$

$$C_{gs} = \frac{\mathrm{Im}(Y_{11}) - \omega C_{gd}}{\omega} \cdot \left(1 + \frac{(\mathrm{Re}(Y_{11}))^2}{(\mathrm{Im}(Y_{11}) - \omega C_{gd})^2}\right) \tag{2.2}$$

$$C_{ds} = \frac{1}{\omega}\mathrm{Im}(Y_{22} + Y_{12}) \tag{2.3}$$

$$R_i = \frac{\mathrm{Re}(Y_{11})}{(\mathrm{Im}(Y_{11}) - \omega C_{gd})^2 + (\mathrm{Re}(Y_{11}))^2} \tag{2.4}$$

$$R_{ds} = \frac{1}{\mathrm{Re}(Y_{22})} \tag{2.5}$$

$$g_{m0} = \sqrt{((\mathrm{Re}(Y_{21}))^2 + (\mathrm{Im}(Y_{21}) + \omega C_{gd})^2) \cdot (1 + \omega^2 C_{gs}^2 R_i^2)} \tag{2.6}$$

$$\tau = \frac{1}{\omega}\arcsin\left(\frac{-\omega C_{gd} - \mathrm{Im}(Y_{21}) - \omega C_{gs} R_i \,\mathrm{Re}(Y_{21})}{g_m}\right) \tag{2.7}$$

The cutoff frequency (f_T) can be expressed in

$$f_T = g_m / 2\pi(C_{gs} + C_{gd}) \tag{2.8}$$

which is related to the intrinsic transconductance (g_m) and input intrinsic capacitances (C_{in} = C_{gs} + C_{gd}). The approximate maximum oscillation frequency (f_{max}) can be expressed as follows [39]:

$$f_{\max} \approx f_T \Big/ \sqrt{4g_{DS}R_g + 8\pi f_T C_{gd}(R_g + \alpha R_d)} \tag{2.9}$$

The drain-to-substrate junction capacitance (C_{jdb}) refers to the deep n-well (DNW) to p-usbstrate/p-body junction capacitance and this capacitance also has impact on f_{max}.

2.3 Annular-structure and Square-structure Comparison

2.3.1 Effective Transconductance Evaluation

The initial problem in an annular-structure LDMOS is the definition of the aspect ratio W/L, which is not as complicated as in standard devices. However, defining the width (W) of the annular structure is less straightforward. For example, the width (W) can either the length of the curve lying at mid-channel, or the drain/source diffusion perimeter.

This study extracts the experimental W/L values by comparing the I_D-V_{GS} characteristics of an annular-structure transistor and a standard transistor with the same L. The SPICE model can be used to extract W/L from the ratio of transconductances g_m as follows [40]:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = (\frac{W}{L})_{eff} \mu C_{ox} V_{DS}(1 + \lambda V_{DS}) \tag{2.10}$$

$$\left(\frac{W}{L}\right)_{eff}^{closed} = \left(\frac{W}{L}\right)_{eff}^{std} \frac{g_m^{closed}}{g_m^{std}} \tag{2.11}$$

where the superscripts ‘std’ and ‘closed’ refer to the standard geometries and closed structure (square/annular structure), respectively. As the effective aspect ratio of the standard transistor that was called fishbone structure was known, the aspect ratio of the square/annular structure can be determined.

Figure 2.6 shows the I-V characteristics of a LDMOS under static conditions. The DC characterization of the DUT was performed using an Agilent semiconductor parameter (4156C) analyzer. In saturation region, the annular structure shows a higher drain current and transconductance than the square structure. These are attributable to the larger equivalent W/L and smaller drain parasitic resistance. The effective annular structure width is 83.2 μm compared with fishbone structure (W = 80 μm). These results show that the annular structure has better DC performance than the square structure.

2.3.2 Capacitance versus V_{GS} and V_{DS}

This section extracts the gate-to-source/body capacitance (C_{GS} + C_{GB}) and gate-to-drain (C_{GD}) capacitance from the de-embedded S-parameters in the low-frequency range [41]. The other capacitance extraction method was performed in the Appendix 1. Figures 2.7 and 2.8 show the extracted C_{GS} + C_{GB} and C_{GD} of RF square-structure and annular-structure LDMOS transistors at room temperature. At V_{DS} = 1 V, both square and annular structures have similar curve traces because they share the same physical mechanism. In terms of the lateral

non-uniform doped channel in LDMOS, the drain end will be inverted prior to the source end, resulting in a peak in C_{GD}. As the drain voltage V_{DS} exceeds 5 V, the $C_{GS} + C_{GB}$ and C_{GD} all start to reveal distinct peaks. This is because the inversion charges are injected to the depleted area of the drift. Therefore, the C_{GD} and $C_{GS} + C_{GB}$ increase with increasing V_G, and the $C_{GS} + C_{GB}$ increases suddenly over the flat of the inversion area to reach the maximum at the onset of quasi-saturation [36]. The reason for this phenomenon is that a higher V_D leads to a higher V_G at the onset of quasi-saturation, and so the peaks shift to a higher V_G.

However, for the square structure, Fig. 2.7 shows a second peak in $C_{GS} + C_{GB}$ and C_{GD} at V_{DS} = 10 V. Figure 2.9 shows a uniform current distribution across the region from drain to source in annular structures. Because the corners of the drift of square structure show a lower current density than the edges, square-structure device must provide higher gate voltage to go into quasi-saturation. In other words, besides the first peak results from the edges of the square structure which went into the quasi-saturation region in advance, the second peak appears when the corners start to go into quasi-saturation at V_G is approximately 6.5 V when V_{DS} = 10 V.

2.3.3 High-frequency Characteristics and Power Performance

To characterize the high-frequency performance and determine the maximum cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) of annular-structure LDMOS

transistor, this study measures S-parameters on-wafer from 0.1 to 20 GHz using an Agilent performance network analyzer (E8361C) and then de-embeds them using the OPEN dummy [42]. The cutoff frequency and maximum oscillation frequency are the frequency where the current gain was 0 dB and the frequency where MSG was 0 dB, respectively. The measurement results of f_T and f_{max} for annular-structure LDMOS are shown in Fig. 2.10. At V_G = 2 V and V_D = 20 V, the cutoff frequency and maximum oscillation frequency are approximately 5 GHz and 12 GHz, respectively.

This study measured power performance using a load-pull system consisting of HP85122A and ATN LP1 at the cascade probe station, with the probe calibrated using a standard calibration substrate. Figure 2.11 shows the transducer power gain and efficiency of different layout structures. In the case of the load-pull measurement, the operating frequency was 1.9 GHz and the source and load impedances were biased at V_D = 20 V and V_G = 2.5 V, which are maximum cutoff frequency values. Figure 2.11 indicates a power gain of over 12 dB and an input power 7 dBm at the 1-dB compression point. The power added efficiency (PAE) at this point is over 20%. Figure 2.11 also shows that the annular structure had higher power gain and efficiency than the square structure. This result might be attributed to the larger equivalent transconductance of the annular structure.

2.4 Summary

Two types of layout structures of RF LDMOS transistors for DC, capacitance and power characteristics were investigated. The annular-structure LDMOS transistor had a better performance than the square structure without changing the process flow. The higher drain current in the annular structure LDMOS was due to less corner effect compared with square structure. According to the capacitance extraction results and power performances, the annular structure is superior to the square structure in layout type of LDMOS transistor.

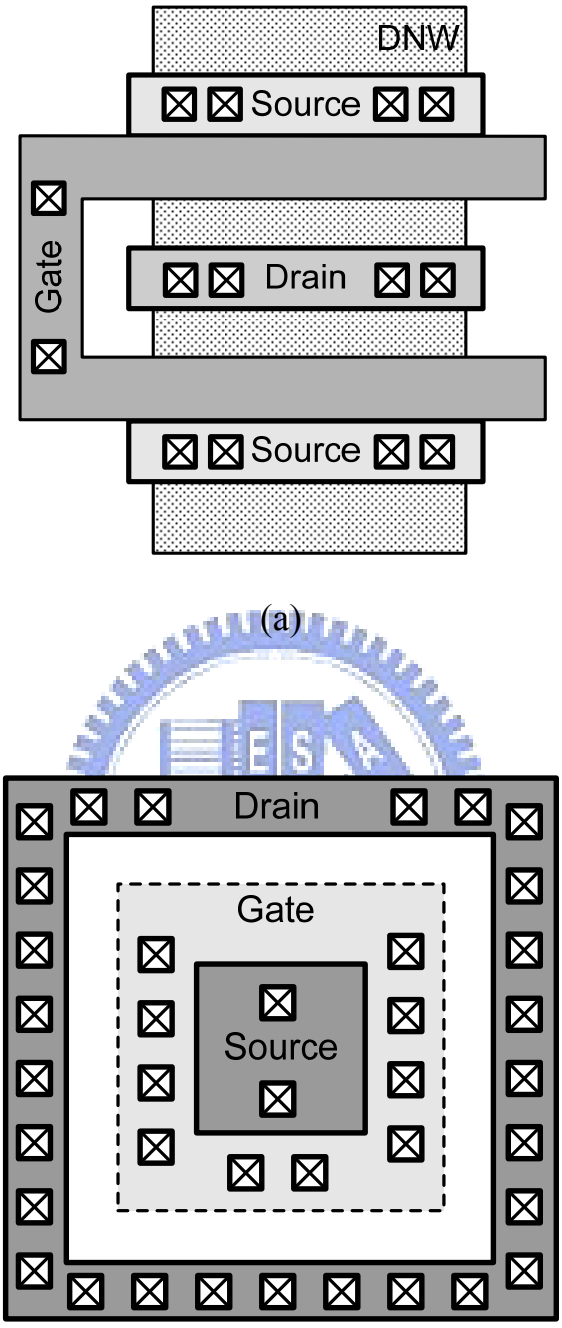


Fig. 2.1 The traditional LDMOS layout structure: (a) fishbone and (b) square.

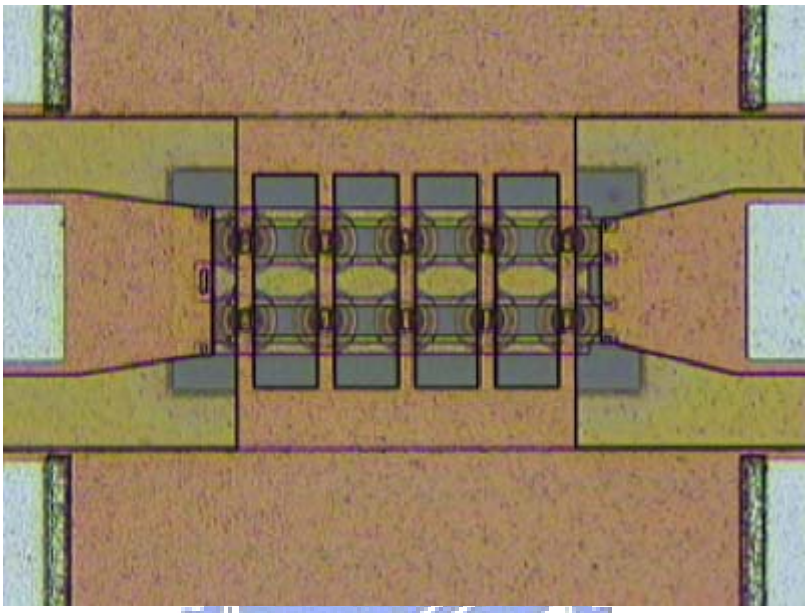


Fig. 2.2 The die photo of annular-structure RF LDMOS.

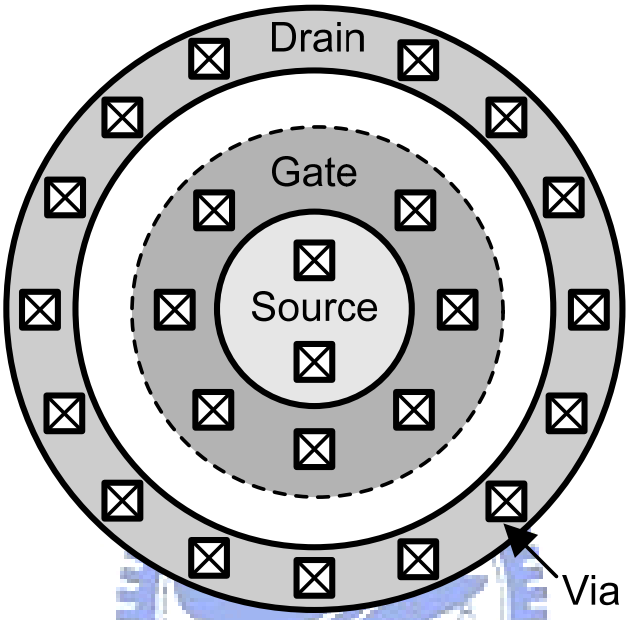


Fig. 2.3 The cell layout of the annular-structure RF LDMOS.

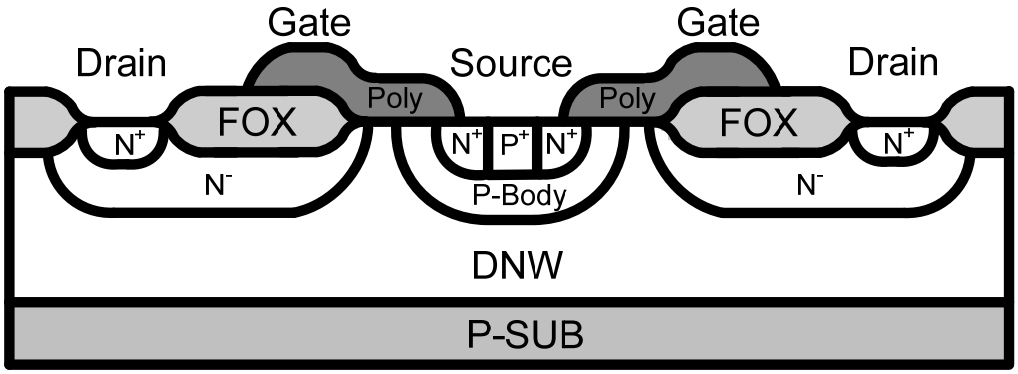


Fig. 2.4 Schematic cross section of the LDMOS transistor.

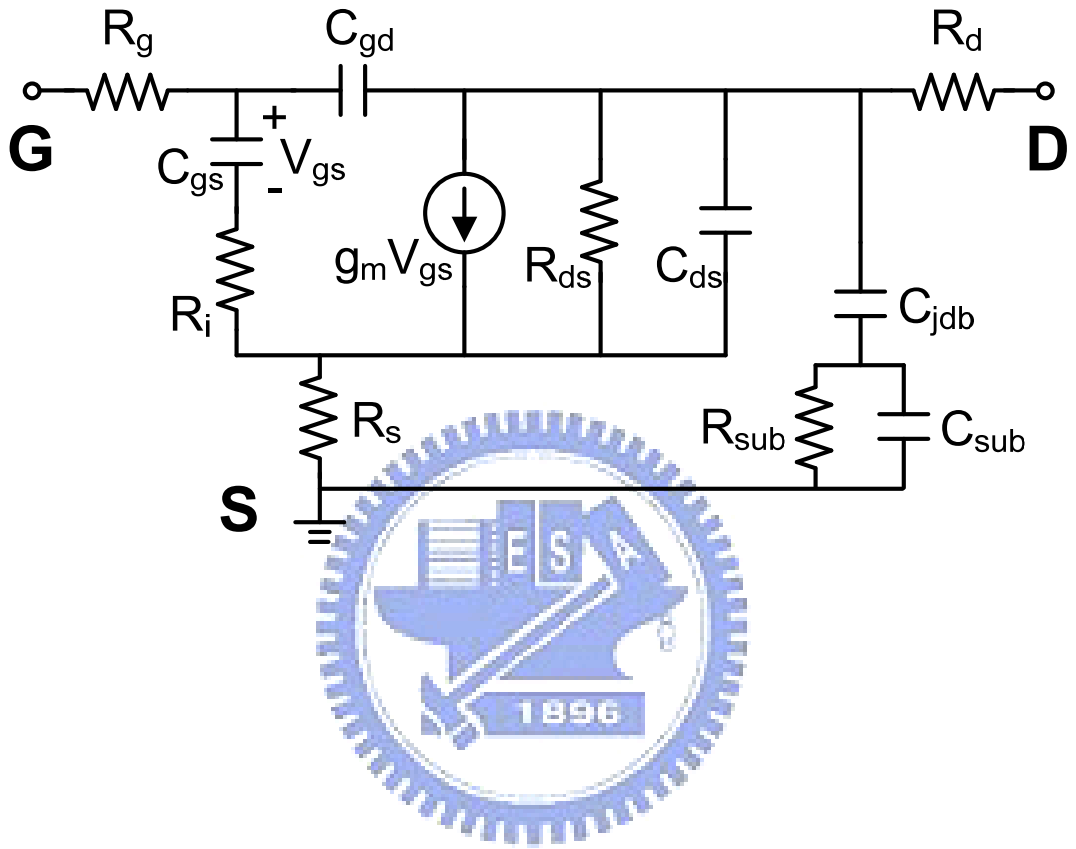
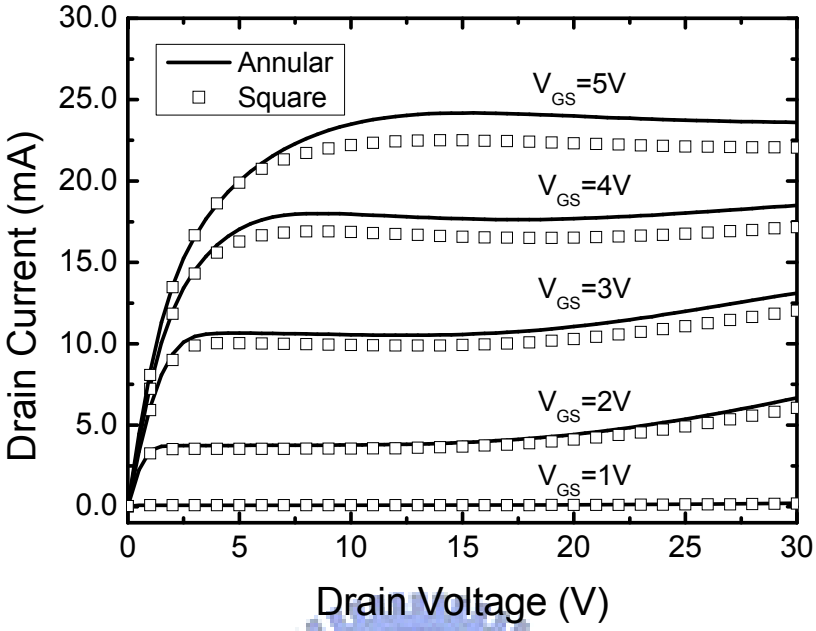
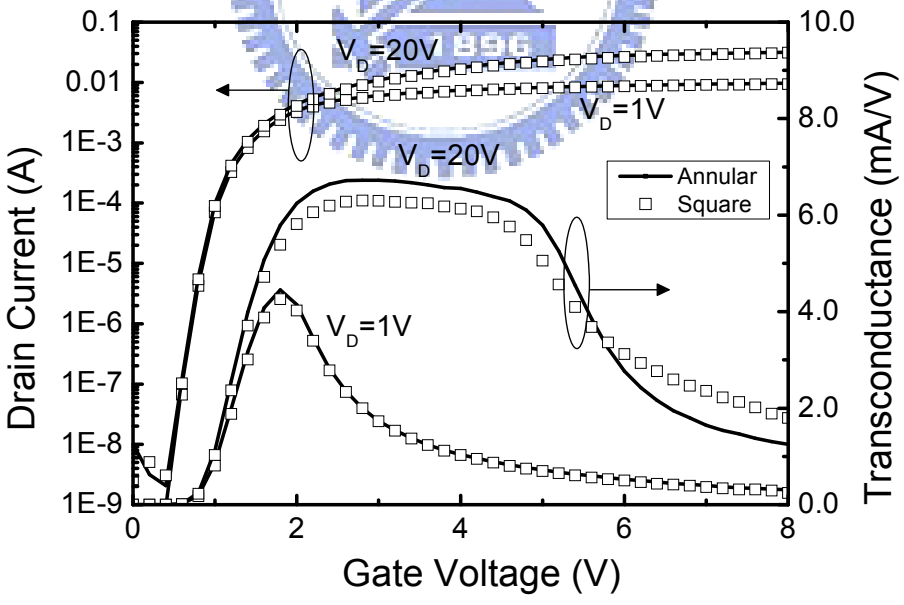


Fig. 2.5 A simple equivalent circuit model of the LDMOS.



(a)



(b)

Fig. 2.6 (a) Output and (b) subthreshold characteristics of LDMOS transistors for different layout structures.

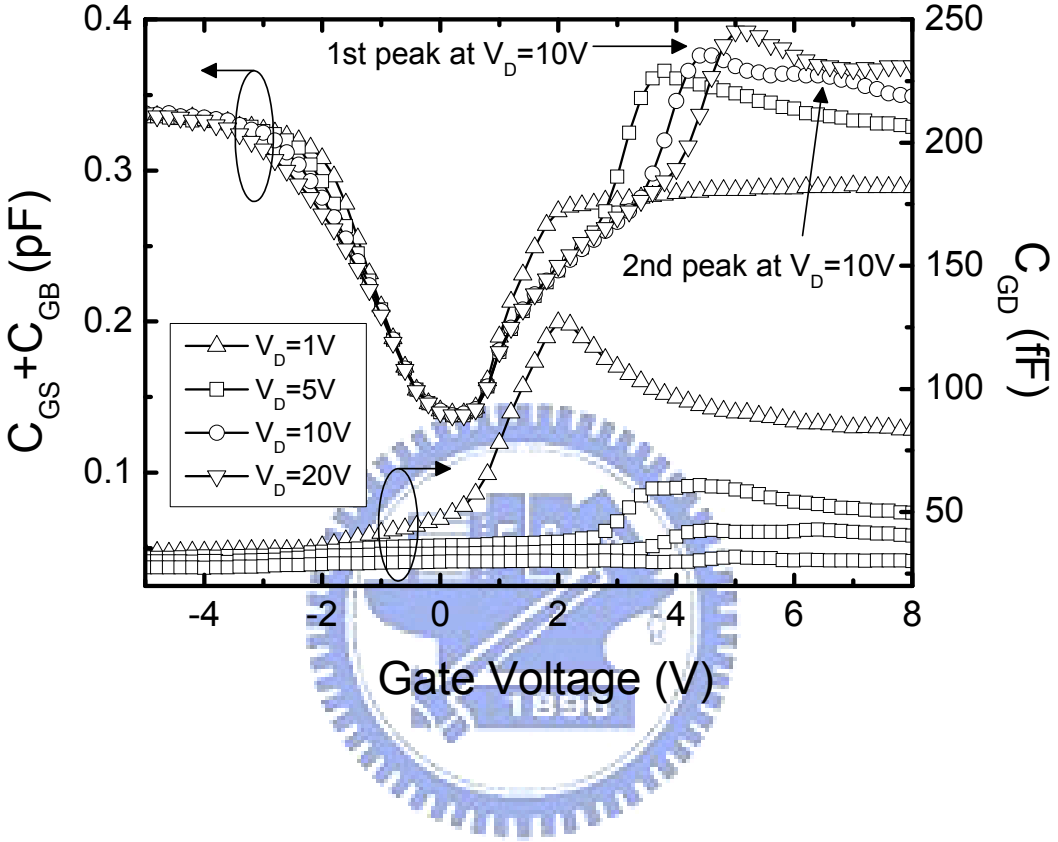


Fig. 2.7 Extracted C_{GS}+C_{GB} and C_{GD} versus gate voltage with different drain biases for square-structure LDMOS transistor.

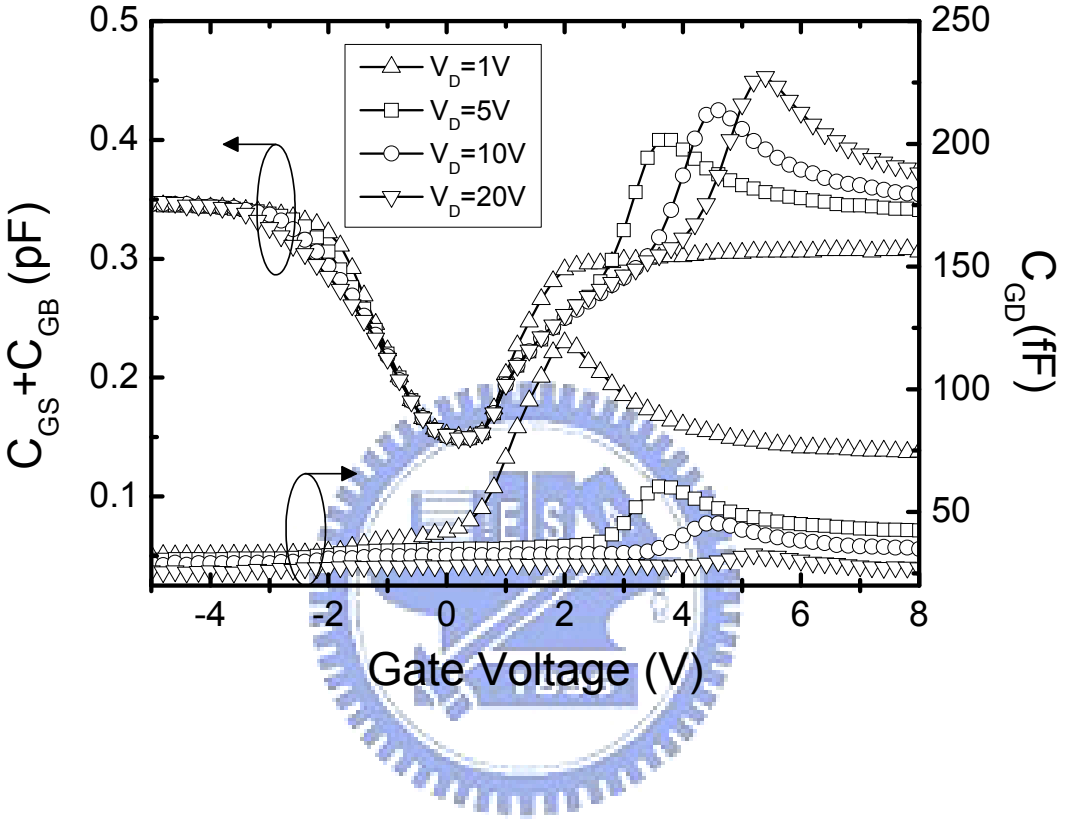
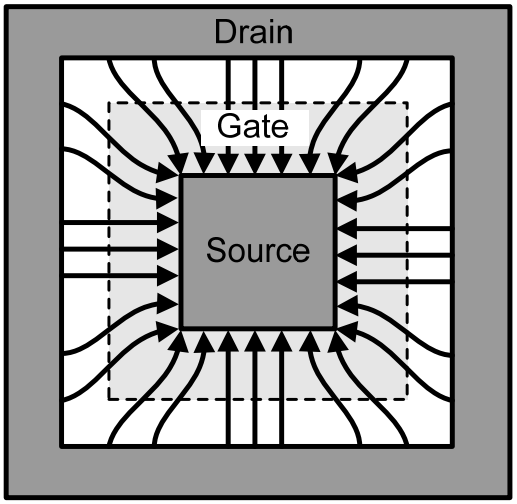
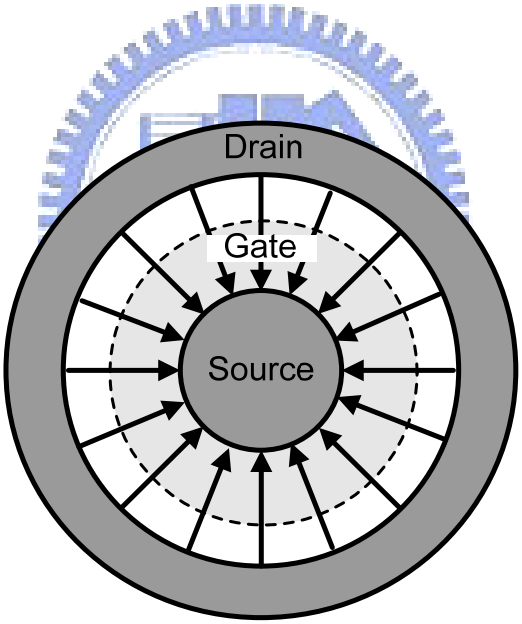


Fig. 2.8 Extracted $C_{GS}+C_{GB}$ and C_{GD} versus gate voltage with different drain biases for annular-structure LDMOS transistor.



(a)



(b)

Fig. 2.9 Schematic view of layout structure and current distribution in RF LDMOS. (a) square structure and (b) annular structure.

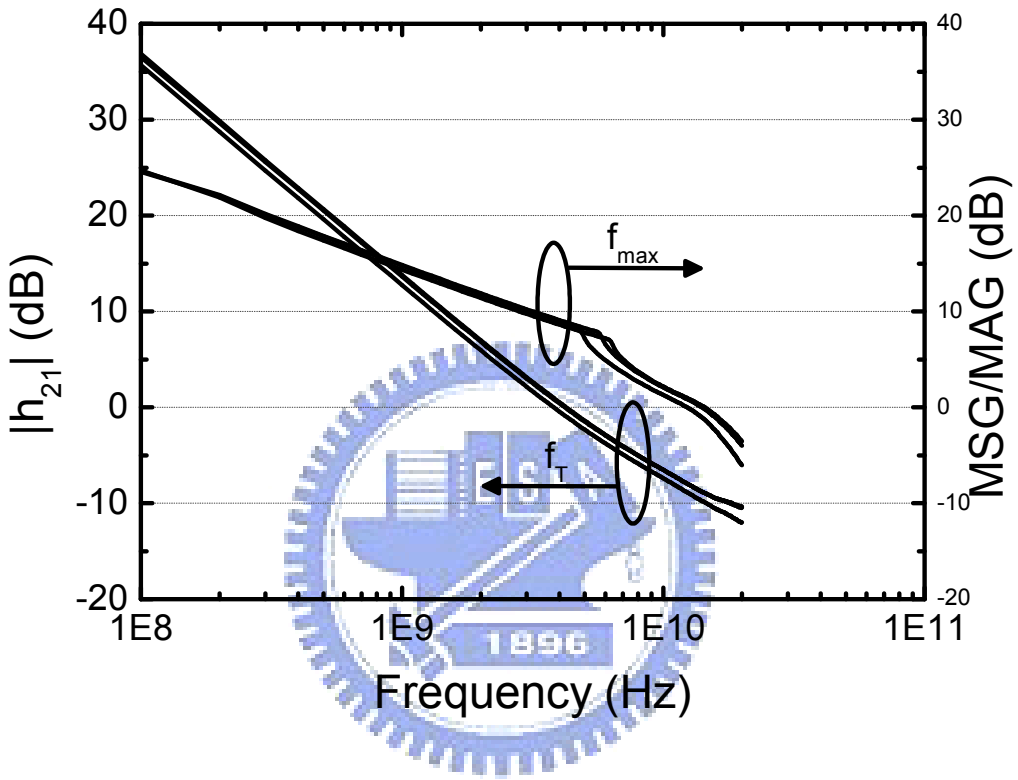


Fig. 2.10 Cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) of annular-structure LDMOS at V_D = 20V, and V_G = 1, 2, 3 V

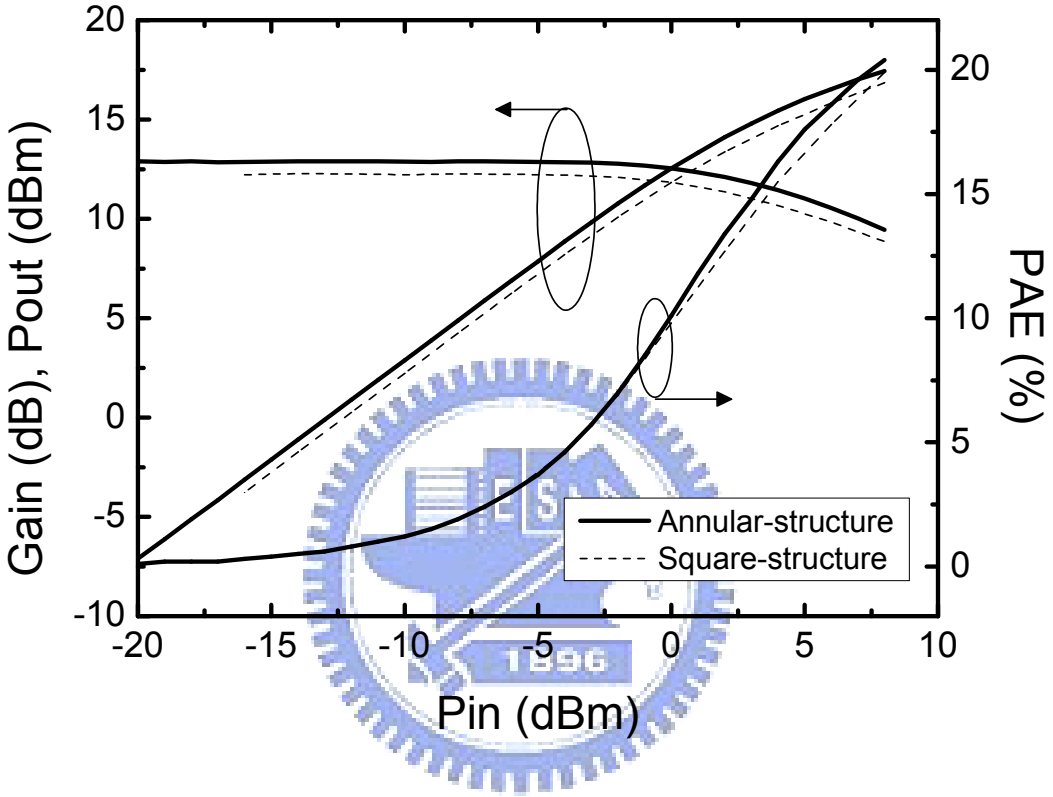


Fig. 2.11 Output power and efficiency versus input power at 1.9 GHz, V_D = 20V, and V_G = 2.5 V with different layout structure.

Chapter 3

RF Transistor PHD Modeling

3.1 Introduction

Modern communication systems are nowadays complex to permit complete simulation of the nonlinear behavior at the active device level. In addition to small-signal and parasitic analysis for active devices, linearity and power analysis are the most important factors in RF amplifiers because it leads to intermodulation distortion. This type of distortion creates undesired signals, similar to the operation signal, in the amplifier input. In particular, the third order intermodulation distortion (IMD3) must be minimized because it generates harmonics that interfere with the desired signal. As a result, many studies have been dedicated to developing large-signal models to predict the nonlinear behavior of active devices [43-46]. Though these nonlinear models can predict the large signal operation of active devices accurately using suitable equivalent circuits or mathematical equations, they may be unsuccessful in other kinds of active devices or foundry processes. Optimizing circuit performance and reducing product time to market for accurate large-signal models remains an essential.

An alternate way to construct a large-signal model is to use the measurement-based behavioral method proposed by [47], called the polyharmonic distortion (PHD) model. This

model is based on X-parameters, which are extensions of S-parameters with nonlinear components measured using a nonlinear vector network analyzer (NVNA) [48]. S-parameters are perhaps the most successful parameter ever. These parameters have the powerful property that the S-parameters of individual components are sufficient to determine the S-parameters of any combination of those components [49]. S-parameters are sufficient to predict its response to any signal, provided only that the signal is small amplitude or power. Despite the great success of S-parameters, they have several limitations. The S-parameters are defined only for linear systems, passive component, or systems behaving linearly with respect to a small signal applied around a static operating point at active device. In fact, all systems are nonlinear in real world. Sometimes, they generate harmonics and intermodulation distortion. Therefore, the S-parameter analysis technique doesn't apply to such systems. X-parameters include harmonic tone and intermodulation frequency component, and also the relationships between all those frequencies for given amplitude and frequency; therefore the X-parameters enable the engineer or system designer to acquire the complete spectrum or waveforms of nonlinear system [48]. Unlike S-parameters, the engineer could obtain the linear device behavior and nonlinear behavior about a large signal operation point from the X-parameters.

As discussed in a study [50], this measurement-based large-signal model facilitates amplifier design with RF simulation tool. Moreover, this study succeeds in calibrating the NVNA reference plane to probe tip. This study also presents the nonlinear behavior of RF

LDMOS transistors using the PHD model because the NVNA must calibrate the comb generator and power meter before large signal measurements.

3.2 Polyharmonic Distortion Model Theory

The waves of S-parameter are defined as linear combinations of the signal port voltage, V, and the signal port current, I, whereby the current quantity is defined as positive when traveling into the DUT. The incident and scattered wave are called the A-wave and the B-waves, respectively [49]. They are defined as follows:

$$A = \frac{V + Z_0 I}{2} \tag{3.1}$$

$$B = \frac{V - Z_0 I}{2} \tag{3.2}$$

The value of the characteristic impedance Z_0 is 50 Ω. This analysis aimed at PHD model will be working with nonlinear functional relationships between the wave quantities. This derived process of PHD model is very different from S-parameters that can only describe a linear relationship. The PHD model assumes that the discrete tone signals appeared on the incident as well as for the scattered waves. Furthermore, these discrete tones may appear at arbitrary frequency, as explained in [48]. For a given active device, determine the set of complex functions $F_{pm}(.)$ that correlate all of the relevant input components A_{qn} with the output

components B_{pm}, where q and p are from one to the number of signal ports, and m and n are from zero to the highest harmonic index. The mathematical equation expressed as

$$B_{pm} = F_{pm}(A_{11}, A_{12}..., A_{21}, A_{22},...) \tag{3.3}$$

Note that the complex functions $F_{pm}(.)$ are called the describing functions [51]. This mathematical equation is illustrated in Fig. 3.1. The spectral mapping (3.3) is a very general mathematical form; therefore the practical models can be developed in the frequency domain from this form. The PHD model is a special approximation of (3.3), which involves the linearization of (3.3) around the incident or scattered signal.

A first property is that $F_{pm}(.)$ describes a time-invariant system. This implies that applying an arbitrary delay to the input signals, the incident *A*-wave, always results in exactly the same time delay for the output signals, the scattered *B*-waves. In the frequency domain, applying a time delay is equivalent to add a linear phase shift (θ). Therefore, the complex function equation (3.3) can be expressed as

$$\forall \theta: \quad B_{pm}e^{jm\theta} = F_{pm}(A_{11}e^{j\theta}, A_{12}e^{j2\theta},...,\times A_{21}e^{j\theta}, A_{22}e^{j2\theta},...) \tag{3.4}$$

In the following, both of the properties discussed previously are exploited to derive the PHD

model equations. Because the (3.4) is valid for all values of θ, we can make equal to the inverted phase of A_{11} which is the incident fundamental. The choice is not unnatural for power transistor and power amplifier applications, since A_{11} is the dominant large-signal input component.

For expression elegance, the phasor P is introduced and is defined as

$$P = e^{+j\varphi(A_{11})} \tag{3.5}$$

Substituting $e^{j\theta}$ by P^{-1} in (3.4) results in

$$B_{pm} = F_{pm}(|A_{11}|, A_{12}P^{-2}, A_{13}P^{-3}, \ldots, \times A_{21}P^{-1}, A_{22}P^{-2}, \ldots)P^{+m} \tag{3.6}$$

The benefit of (3.6), compared to (3.3), is that the first input argument will always be a positive real number, that is to say, the amplitude of the fundamental component at the input port 1, instead a complex number.

The harmonic superposition principle is illustrated in Fig. 3.2. To keep the diagram simple and elegance, this PHD model derived thereafter only consider the presence of the A_{1m} and B_{2n} components and neglect the presence of the A_{2m} and B_{2n} components. The harmonic superposition principle is important concept to the PHD model. Linearization of (3.6) versus

all components in this equation besides the large signal A_{11} results in

$$B_{pm} = Kpm(|A11|)P^{+m} + \sum_{qn} G_{pg,mn}(|A_{11}|)P^{+m}\,\mathrm{Re}(A_{qn}P^{-n}) + \sum_{qn} H_{pg,mn}(|A_{11}|)P^{+m}\,\mathrm{Im}(A_{qn}P^{-n}) \tag{3.7}$$

whereby

$$K_{pm}(|A_{11}|) = F_{pm}(|A_{11}|,0,\ldots 0),$$

$$G_{pq,mn}(|A_{11}|) = \left.\frac{\partial F_{pm}}{\partial\,\mathrm{Re}(A_{qn}P^{-n})}\right|_{|A_{11}|,0,\ldots 0}$$

$$H_{pq,mn}(|A_{11}|) = \left.\frac{\partial F_{pm}}{\partial\,\mathrm{Im}(A_{qn}P^{-n})}\right|_{|A_{11}|,0,\ldots 0}$$

Note that the real and imaginary parts of the input arguments are considered as separate and independent parts. The PHD model equation is derived by substituting the real and imaginary parts of the input arguments in (3.7) by a linear combination of the input arguments and their corresponding conjugates. Since

$$\mathrm{Re}(A_{qn}P^{-n}) = \frac{A_{qn}P^{-n} + conj(A_{qn}P^{-n})}{2} \tag{3.8}$$

$$\mathrm{Im}(A_{qn}P^{-n}) = \frac{A_{qn}P^{-n} - conj(A_{qn}P^{-n})}{2j} \tag{3.9}$$

The (3.7) can be rewritten

$$B_{pm} = Kpm(|A11|)P^{+m} + \sum_{qn} G_{pg,mn}(|A_{11}|)P^{+m} \times \left(\frac{A_{qn}P^{-n} + conj(A_{qn}P^{-n})}{2} \right) + \sum_{qn} H_{pg,mn}(|A_{11}|)P^{+m} \times \left(\frac{A_{qn}P^{-n} - conj(A_{qn}P^{-n})}{2j} \right) \quad (3.10)$$

Rearranging (3.10), and then the simple PHD model equation as follows

$$B_{pm} = \sum_{qn} S_{pq,mn}(|A_{11}|)P^{+m-n}A_{qn} + \sum_{qn} T_{pq,mn}(|A_{11}|)P^{+m+n}conj(A_{qn}) \quad (3.11)$$

The $S_{pq,mn}(.)$ and $T_{pq,mn}(.)$ are defined as

$$S_{p1,m1}(|A_{11}|) = \frac{K_{pm}(|A_{11}|)}{|A_{11}|}, \quad (3.12)$$

$$T_{p1,m1}(|A_{11}|) = 0 \quad (3.13)$$

$$\forall\{q,n\} \neq \{1,1\} : S_{pq,mn}(|A_{11}|) = \frac{G_{pg,mn}(|A_{11}|) - jH_{pq,mn}(|A_{11}|)}{2} \quad (3.14)$$

$$\forall\{q,n\} \neq \{1,1\} : T_{pq,mn}(|A_{11}|) = \frac{G_{pg,mn}(|A_{11}|) + jH_{pq,mn}(|A_{11}|)}{2} \quad (3.15)$$

According to aforementioned PHD model deduction, to analyze the nonlinear behavior of RF LDMOS transistors quickly and accurately without equivalent circuit extraction and

optimization, the PHD model is a good way to analyze the nonlinear characteristics for active devices. The X-parameter in Agilent nonlinear vector network analyzer expression is given by (3.16).

$$B_{PK} = X_{PK}^{(F)}(|A_{11}|)G^{K} + \sum_{Q,L} X_{PK,QL}^{(S)}(|A_{11}|)G^{K-L} \cdot A_{QL} + \sum_{Q,L} X_{PK,QL}^{(T)}(|A_{11}|)G^{K+L} \cdot A_{QL}^{*} \quad (3.16)$$

Here the scattered and transmitted waves, B_{PK}, at port P at the K^{th} harmonic frequency, divided into three terms. The first term represents the large-signal response of the device to a single large-amplitude tone (A_{11}) at a given fundamental frequency, assuming match all ports at all harmonic frequencies. The second and third terms depict a linear non-analytic mapping of incident phasors at port Q and harmonic frequency index L into complex output phasors at port index P and harmonic frequency index K. The term G is the phase of the input large tone. The sum of this equation includes all ports and indicates the number of harmonics measured. The significance of expression (3.16) is the same with (3.11), and the (3.16) is read easily for reader. Consequently, the X-parameters in the PHD model are mathematically generalized

S-parameters, applicable to nonlinear and linear components under both large-signal and small-signal conditions.

3.3 RF Active Device Power Characteristics

3.3.1 Measurement Setup and On-wafer Calibration

This study used an Agilent Nonlinear Vector Network Analyzer (NVNA) capable of nonlinear calibration and measurements to extract the PHD model. Figure 3.3 illustrates this nonlinear measurement system. The system is based on a dual-source network analyzer (PNA-X) with two phase reference comb generators for phase calibration and a power meter and sensor for power calibration. This system also includes embedded application software and an interface for other instruments to automatically control X-parameter characterization and extraction. Using standard nonlinear analysis tool in Agilent Design System (ADS), the measured DUT X-parameters can be immediately used to simulate nonlinear figures of merit such as P_{1dB}, IP_3, time waveform and other power performance. Therefore, the on-wafer calibration of this system is very important to accurately acquiring the simulation results of active devices. The S-parameters of the GSG probes were measured before system calibration. This is because the NVNA phase and power calibration are just for the cable end, and not for the probe tips (Fig. 3.3 depicts the calibration reference plane). When finished the S-parameters, phase, and power calibration at cable end of the NVNA system with phase

stable coaxial cable, add up the S-parameters of probes to NVNA system; therefore, the calibration plane will shift to the probe tips. Figure 3.4 shows the actual hardware setup of NVNA system.

3.3.2 Linearity and Power Performance

The PHD model results agree well with the nonlinear behavior of the annular/square-structure LDMOS transistor with 80 μm width length at 1.9 GHz. The impedance of measurements results and extracted data are all at 50 ohm. Figure 3.5 and 3.6 show that the PHD model accurately predicts the measured transducer power gain and the third-order intermodulation (IM3) over a wide range of input power. Figure 3.7 represents a comparison between the measured and modeled (by means of the PHD model) time domain voltage waveforms at the terminals of the annular-structure RF LDMOS. Figures 3.8 and 3.9 measure gain contours by ATN LP1 and simulate the other using the ADS simulator. The simulating transducer gain contours for 80 μm width length in the annular structure agree with measurement data even at the maximum value far from the 50 ohm.

3.4 Summary

The nonlinear behavior of an annular structure LDMOS transistors using PHD model presented in this study. By way of the on-wafer NVNA measurement system, the nonlinear model via X-parameter provides a simple and direct way to get a large-signal model for power amplifier design. The linearity and power gain contour can be predicted using this model without any optimization and curve fitting.

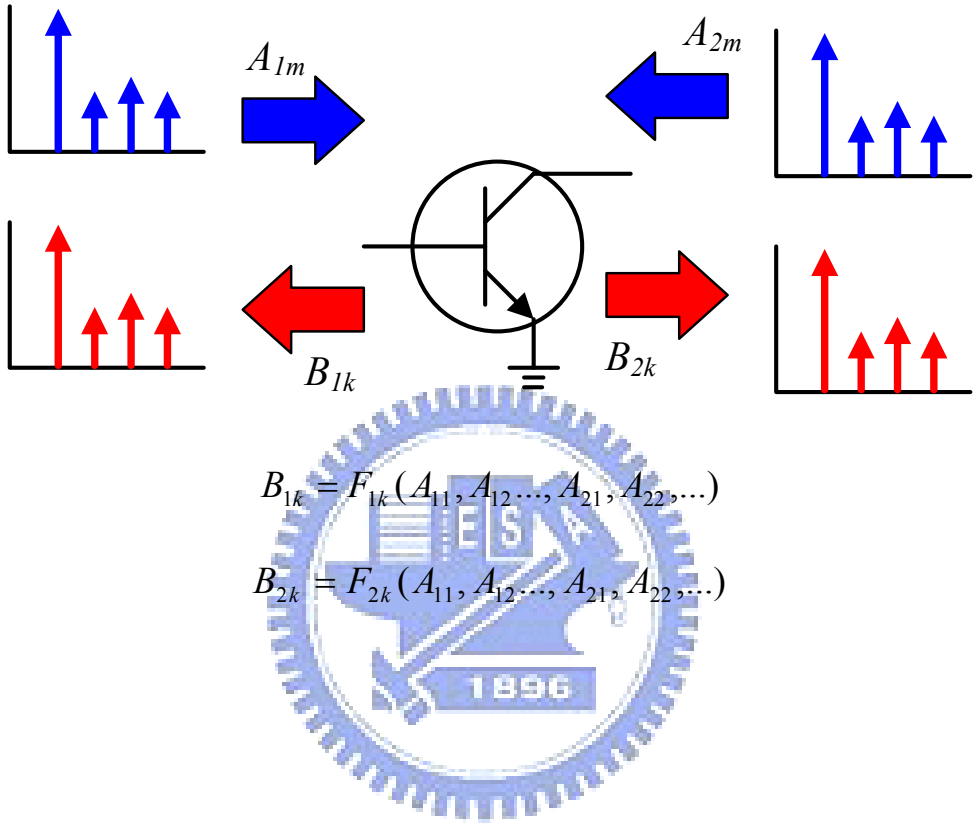


Fig. 3.1 The concept of describing functions.

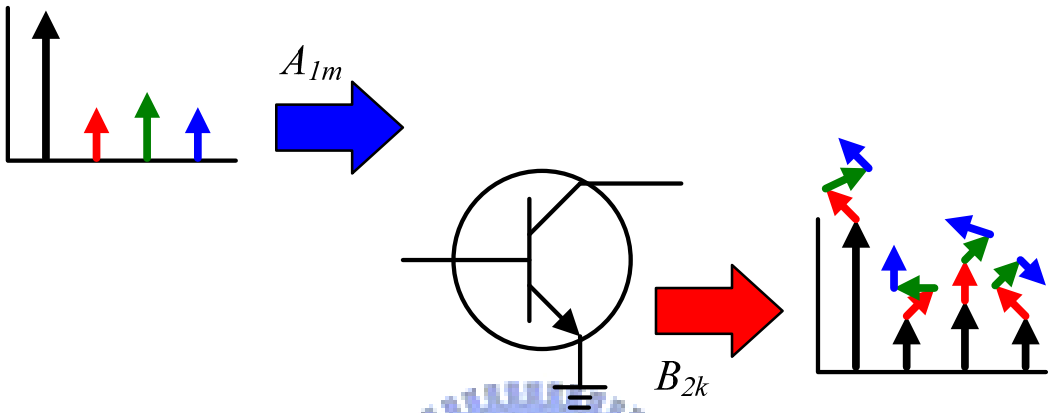


Fig. 3.2 The harmonic superposition principle.

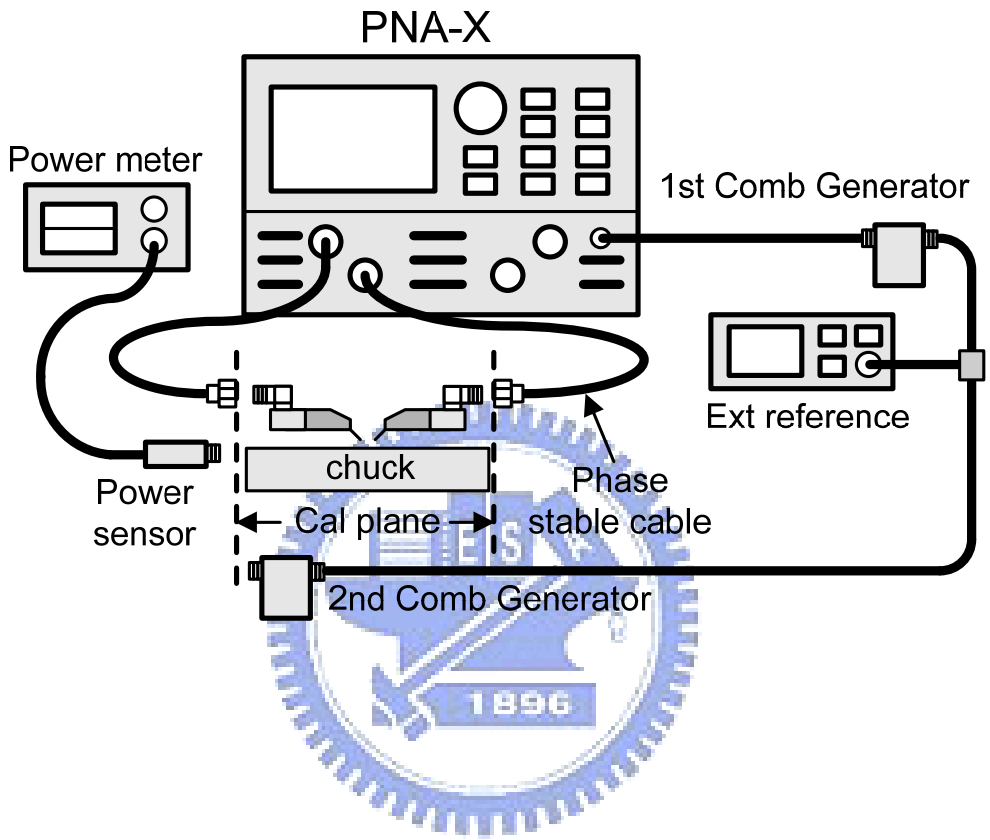


Fig. 3.3 On-wafer PHD model extraction system.

Fig. 3.4 Nonlinear vector network analyzer (NVNA).

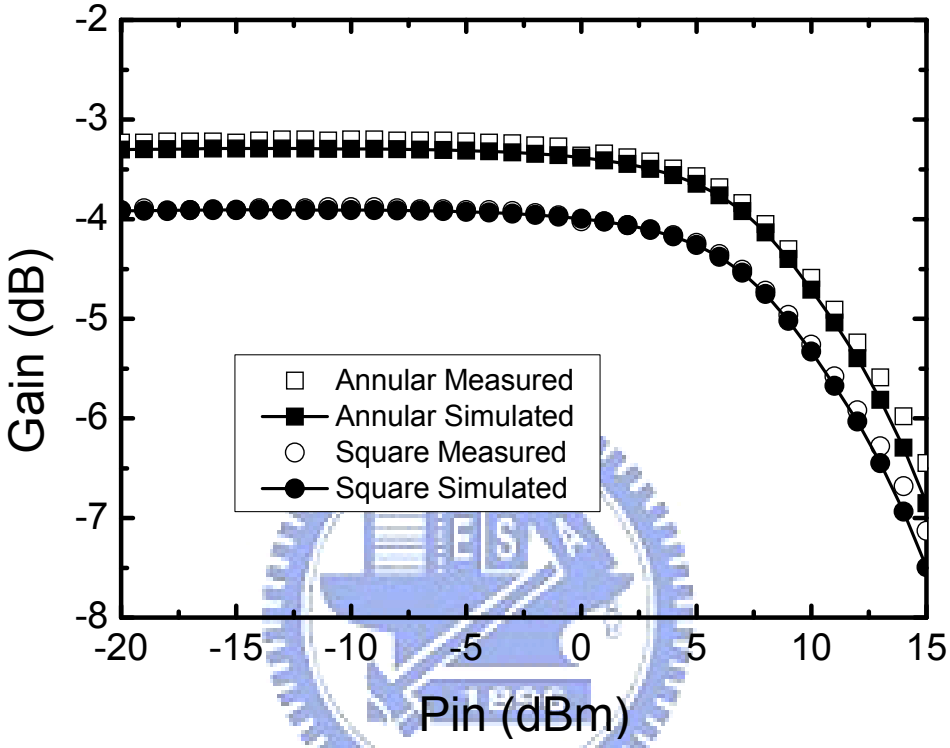


Fig 3.5 Measured and simulated results of the gain for annular-structure and square-structure LDMOS transistors with width 80 μm at 1.9 GHz.

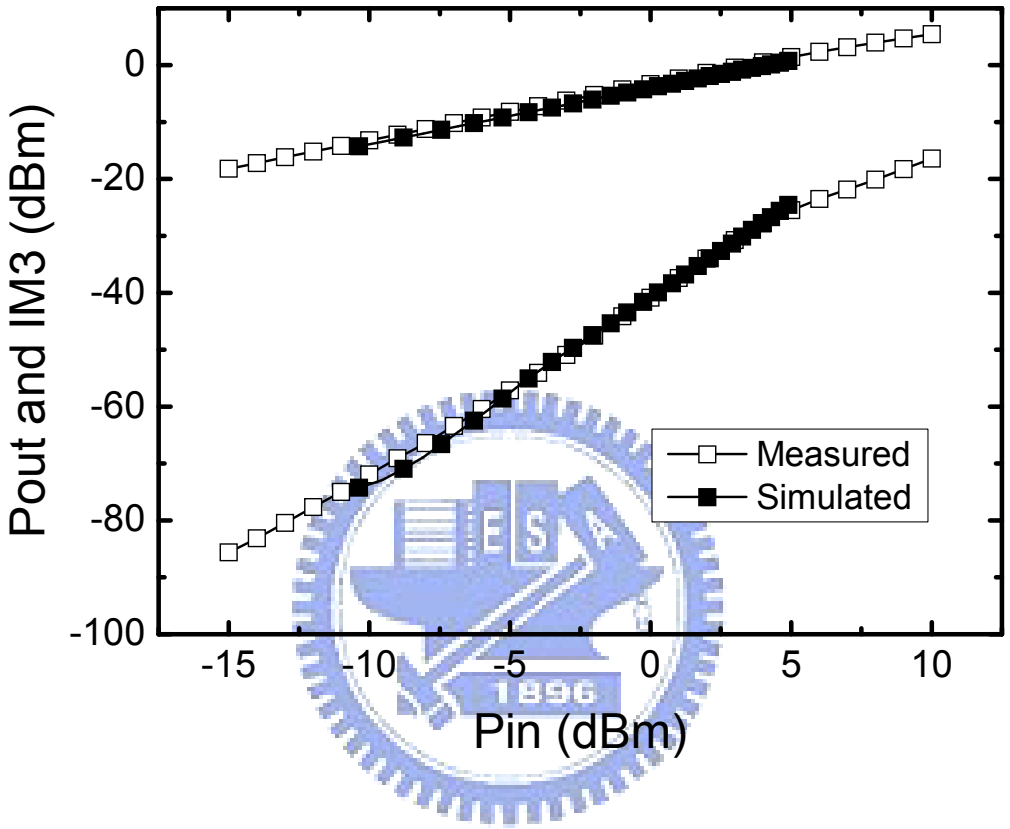
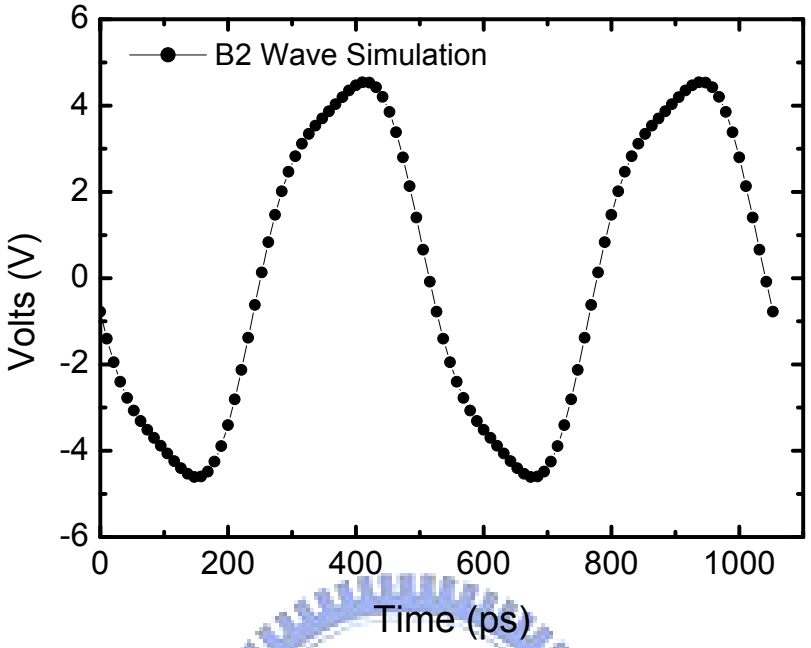
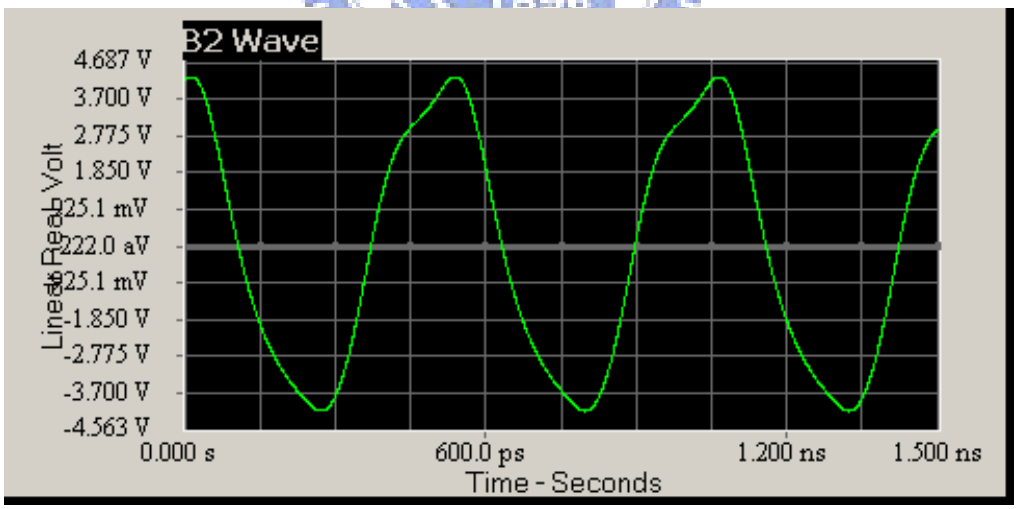


Fig. 3.6 Measured and simulated results of the IM distortion for annular-structure LDMOS transistors with total width length 80 μm at 1.9 GHz.



(a)



(b)

Fig. 3.7 (a) Simulated and (b) measured results of the B2 wave in time domain.

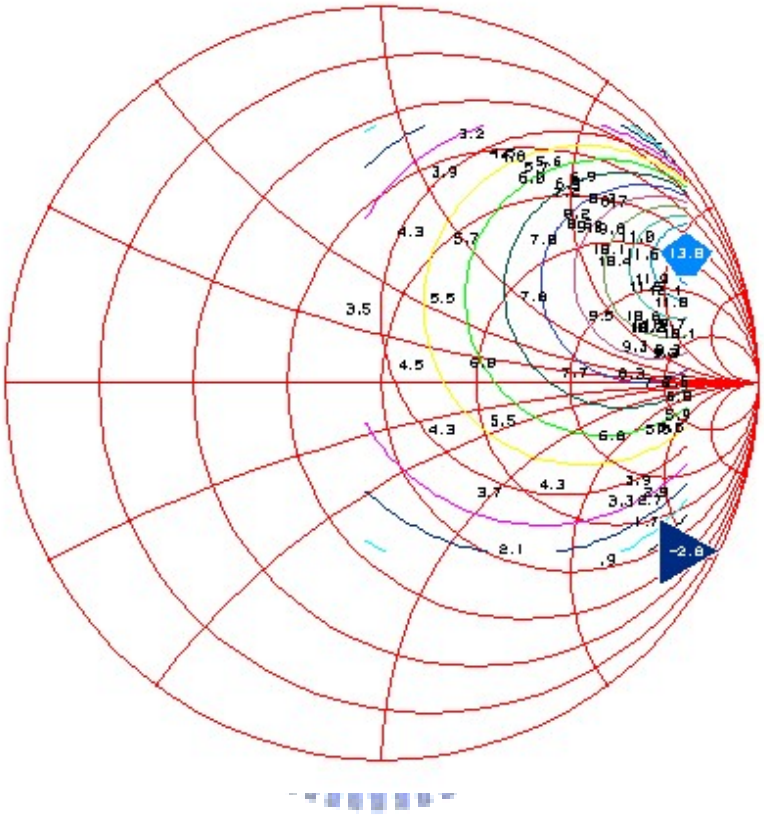


Fig. 3.8 Measured results of gain circle for annular-structure LDMOS transistors from load-pull system with total width length 80 μm at 1.9 GHz.

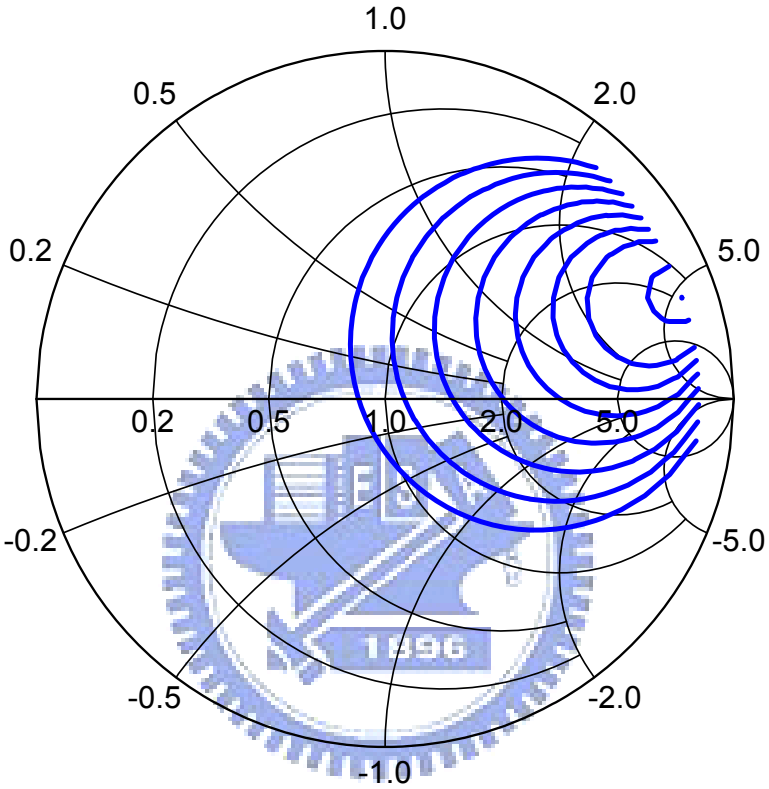


Fig. 3.9 Simulated results of gain circle for annular-structure LDMOS transistors from PHD model with total width length 80 μm at 1.9 GHz.

Chapter 4

Sensing Application

4.1 Introduction

The commercial market has rapidly grown for demanding various sensitive sensors in areas including chemistry, medicine and biology. Although surface acoustic wave (SAW) filters have seen much use in telecommunication, SAW-based sensors have recently emerged for many attractive features in medical and chemical applications [52][53]. The use of acoustic microsensor to detect the physical properties, such as mass loading and viscosity, provides the benefits of real-time electronic readout, compact size, robustness, and low cost. Monolithic integration of biosensors with existing microelectronics will allow biochemical detection system to be further miniaturized in mass production and enhanced with software-definable functions. Chemical sensing through the use of acoustic wave devices has long been available using ST-quartz as the piezoelectric material for generating acoustic wave. Vapor and gas sensors based on SAW oscillators have been progressing since Wohltjen reported the first studies in 1979 due to their high sensitivity and low production cost [54]. A SAW chemical or biological sensor is commonly realized by a polymer-coated delay-line resonator as the frequency control element in the feedback loop of an oscillating circuit.

Relative to sensing applications, using monolithic integration technology, have been demonstrated [55-58]. These studies developed to date only have a sensor system without any sensing experiments. Although these studies have developed a sensor system using silicon or GaAs process, these sensing performances lack some experiments to show its feasibility. Therefore, in order to modulize and miniaturize the sensing system, it is of great interest to develop chemosensor or biosensor systems by taking advantages of matured IC processing technologies and validate the sensor with sensing experiment in this research.

In this work, the fabrication of SAW devices and the related oscillating circuit using two-poly two-metal (2P2M) 0.35 um complementary metal-oxide-semiconductor (CMOS) process are investigated. Their electrical characteristics are evaluated as well as vapor sensing results. The SAW sensor with the CMOS circuitry is a potential candidate for the development of highly sensitive and low power microsensors.

4.2 Basic Sensing Mechanism

Although the acoustic wave detects any change of the mechanical or electrical boundary conditions on the piezoelectric substrate surface, it is mainly the mass loading effect that is used in chemical sensors. In this case, an appropriate measure for sensing is the fractional frequency shift $\Delta f/f_0$ caused by a change in the mass loaded onto the surface, where f_0 is the

operation frequency of oscillator without vapor adsorption. This fractional frequency shift can be given by [59]

$$\frac{\Delta f}{f_0} = C f_0 h \Delta\rho \tag{4.1}$$

where C is a frequency-independent constant, h denotes the thickness of the coating film that incorporates vapor molecules, and $\Delta\rho$ is the mass density change due to absorption.

The phase noise measurement is a typical way to determine whether the signal of oscillator that was designed as sensor is stable or not. High signal stability in the oscillator is important for differentiating sensing result. Phase noise is defined to quantify the fluctuations of signal in frequency domain, and expressed as the ratio of the single side-band power at a frequency offset $\Delta\omega$ from the carrier with a measurement bandwidth of 1 Hz to the carrier power. The phase noise can be theoretically expressed in the following equation:

$$L\{\Delta\omega\} = 10\log\left[\frac{2FkT}{P_{carrier}}\left(1+\frac{\omega_0}{2Q\Delta\omega}\right)^2\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right] \tag{4.2}$$

where k is the Boltzmann's constant, T is the absolute temperature, F represents an empirical parameter, $P_{carrier}$ is the output power of carrier, Q is the quality factor of the SAW device [60],

ω_0 is the oscillation frequency, $\Delta\omega$ is the offset frequency from the oscillation frequency and $\Delta\omega_{1/f3}$ is the corner offset frequency between the $1/f^3$ and the $1/f^2$ regions in the phase noise response. Equation (4.2) is simplified considerably in our case because SAW devices have an exceptional performance regarding flicker noise (1/f noise) [61]. Only if the amplifier is the dominant noise source will an increase in Q result in reduced oscillator flicker noise. Base on (4.2), improving the Quality factor of SAW device and increasing the power of oscillator appropriately will lower the phase noise to obtain an ideal oscillator for sensing purposes.

4.3 Circuit Design and Experiments

4.3.1 Device Design and Fabrication

A SAW Device having inter-digital transducers (IDT) on the quartz substrate in this study is a key component in the sensing circuit. When an electrical signal of a certain frequency is applied to the input IDT, the SAW is excited on the surface of the substrate because of its piezoelectric effect, and then the SAW propagates across the surface of the substrate toward the output IDT. Figure 4.1 shows the schematic layout of a two-port SAW device in this work. Two single-finger interdigitated transducers were fabricated on an ST-quartz substrate with a propagation direction perpendicular to the x-axis of the quartz. The electrodes were 1/4 wavelength wide and separated by 1/4 wavelength at the target center frequency. A predetermined 157 MHz SAW device whose λ is approximately 20 μm was then designed

with a delay path length of 10λ, and IDT length of 100λ, and uniform aperture width of 70 [62]. A wire-bonded SAW device in the metal can package is shown in Fig. 4.2(a). The SAW device with a metal cap is used to prevent gas disturbance from the ambient as shown in Fig. 4.2(b).

Early reported sensing experiments were conducted to measure the center frequency shift or phase shift of a SAW device using the vector network analyzer (VNA) to directly monitor the frequency response on the SAW device [63]. However, these sensing results by reading the VNA have shown less sensitivity and complicated VNA calibration in gas sensing. In this study, a CMOS-based oscillating circuit for a vapor sensor was accomplished. Before full circuit implementation, a summary of circuit design scheme is presented in Fig. 4.3. For an oscillator to be used in biochemical detection, a MOS amplifier with a feedback loop through the SAW delay line is designed. In order to meet Barkhausen criteria, the amplifier must provide sufficient gain at the target oscillator frequency to overcome the SAW insertion loss as well as the phase difference. Thus the oscillator successfully oscillates as long as the following conditions are satisfied:

$$G_a + (G_{B1} + G_{B2}) + L_s + (L_{M1} + L_{M2}) \geq 0 \tag{4.3}$$

$$\phi_a + (\phi_{B1} + \phi_{B2}) + \phi_s + (\phi_{M1} + \phi_{M2}) = 2n\pi \tag{4.4}$$

In the above equations, G_a, G_{B1}, and G_{B2} are the gain of the amplifier and buffer amplifiers as shown in Fig. 4.3; L_S, L_{M1}, and L_{M2} are the losses of the saw device and match circuits respectively; ϕ_a, ϕ_{B1}, and ϕ_{B2} are the phases of the amplifier and buffer amplifiers; ϕ_s, ϕ_{M1}, and ϕ_{M2} are the phases of the saw device and match circuits respectively. As changes occur due to mass loading or temperature, the oscillating frequency will change to maintain a multiple of 360° phase shifts in the oscillator loop. In the amplifier design, the enhancement load amplifier is chosen to avoid resistors. Therefore, the lowest phase noise will be achieved easily. Furthermore, the cascade buffer amplifier improves the isolation between input and output of an enhancement load amplifier. Thus an improved stable and stable gain will be obtained. Figure 4.4 illustrates the schematic of CMOS amplifier circuits and measurement result. The open-loop gain of the amplifier is above 20 dB at 157 MHz in Fig. 4.4(b).

The flow to accomplish a SAW sensing circuit is shown in Fig. 4.5. There are three major parts in the SAW sensing system including a SAW delay line sensor, a CMOS amplifier and matching networks. First, the SAW device has been designed and fabricated based on the required electrical properties as discussed in the previous section. After completing the SAW device, an amplifier was designed and tuned based on the center frequency and insertion loss of the SAW device. Next, the circuits of phase matching should be considered to compensate the SAW device and CMOS amplifier. For various sensing experiments and conditions, additional passive components were needed to achieve proper phase matching. While the chip

process was completed, the SAW device was wire-bonded with the amplifier in a PCB or metal-can package. The SAW delay line and amplifier were initially characterized by a network analyzer, respectively. A picture of the processed CMOS chip (1.3 x 1.3 mm^2) is shown in Fig. 4.6.

4.3.2 Sensing System

Sensing systems with closed chambers were proposed in some studies [63]. The chemical sensor was reported to successfully detect ethanol in previous literature [64][65]. Figure 4.7 shows the schematic of a simple sensing system in this study. The SAW device was hermetically sealed in the metal can package, as indicated in Fig. 4.2(b) to minimize the residual gas volume and reduce the reaction time. Alcohol vapor was diluted by dry nitrogen and flowed into the metal can package when the flow control valve in this system was turned on. Furthermore, the alcohol concentration was detected by infrared spectrophotometer (IR) system. When the valve was turned off, only pure dry nitrogen flowed into the metal can package. The gas flow rate was 100 sccm. All measured data, including those of the frequency shift, were acquired by data acquisition modules (DAQ), and then analyzed by a personal computer (PC).

4.4 Results and Discussion

In order to acquire the repeatable sensing results, it is important to analyze the quality of signal by phase noise measurement. The SAW oscillator was tested with a commercial spectrum analyzer with V_d = 3 V. The phase noise of the oscillator was measured by Agilent E5052A signal source analyzer. The operating frequency of the oscillator is 157.2 MHz as shown in Fig. 4.8. The phase noise of this oscillator is shown in Fig. 4.9. The achieved phase noise of the oscillator with SAW device is –150 dBc/Hz at 100 kHz offset. Comparing to the traditional oscillator design with inductance-capacitance (LC) tank, the oscillator with SAW device in this study has well phase noise value at 100 kHz due to the high-Q in SAW devices [66]. The excellent phase noise would stabilize the peak frequency drift in the oscillator. The power consumption was 70 mW and expected to be reduced if the SAW device is properly matched in its impedance and the RF amplifier is further optimized. A lower insertion loss in the SAW would be desirable for a low gain amplifier. In this work, the insertion loss of SAW device was about –20 dB.

After completing the SAW oscillator, the SAW device was tested in a gas sensing system. The sensor was exposed to 50 x 10^3 ppm of alcohol. A 600-s exposure time was used for each alcohol pulse. The alcohol sensing results by a thin polyepichlorohydrin (PECH) polymer film on a SAW device are demonstrated in Fig. 4.10. The alcohol molecules are absorbed into the PECH film on the SAW device. As alcohol molecules gradually diffuse into the PECH

film, the SAW oscillating frequency shifts because of mass loading effect. Consequently, the maximum oscillation frequency shift between gas on and off is approximately 10 kHz.

4.5 Summary

In this chapter, the monolithic integration of a SAW delay-line sensor and a 0.35 μm CMOS amplifier has been demonstrated for the organic vapor sensing application. The circuit scheme and design flow of the oscillator with a SAW device are also presented in this study. The gain and total power consumption of the amplifier are 20 dB and 70 mW, respectively. The phase noise of the SAW oscillator achieves −150 dBc/Hz at 100 kHz offset. The sensing experimental results show that the maximum oscillation frequency shift between gas on and off is approximately 10 kHz with 50 x 10^3 ppm alcohol vapor concentration. This compact integrated microsensor will be promising for future chemical and biological sensing applications.

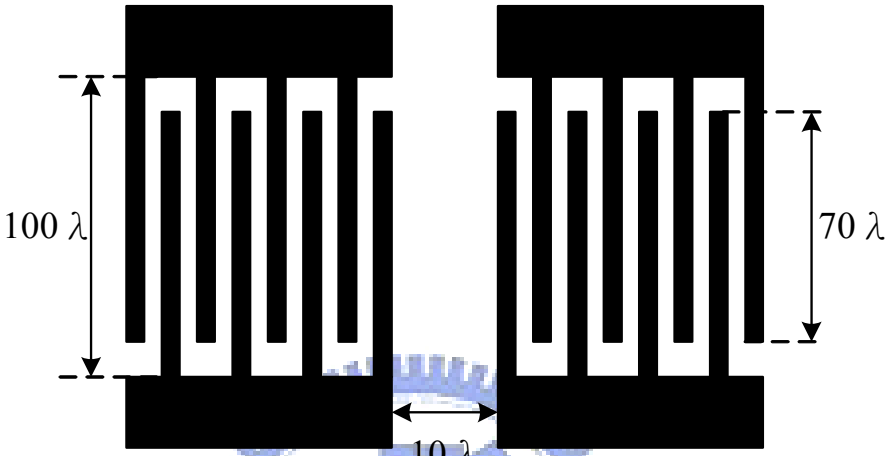


Fig. 4.1 A diagram of the sensor device.

(a)

(b)

Fig. 4.2 The photo of SAW device: (a) without cap and (b) with cap.

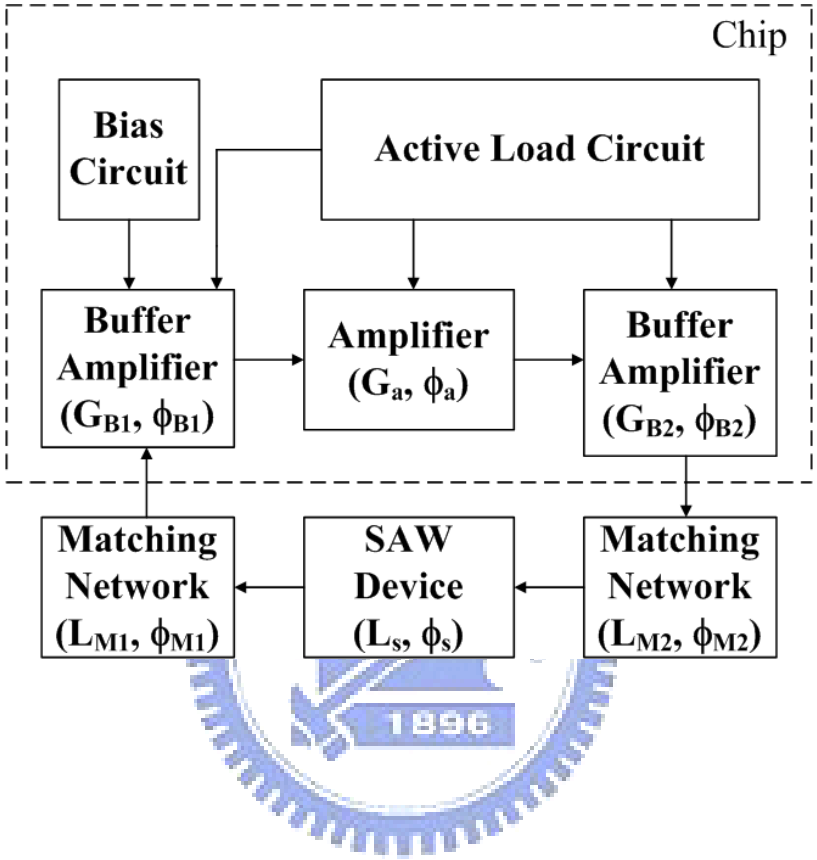
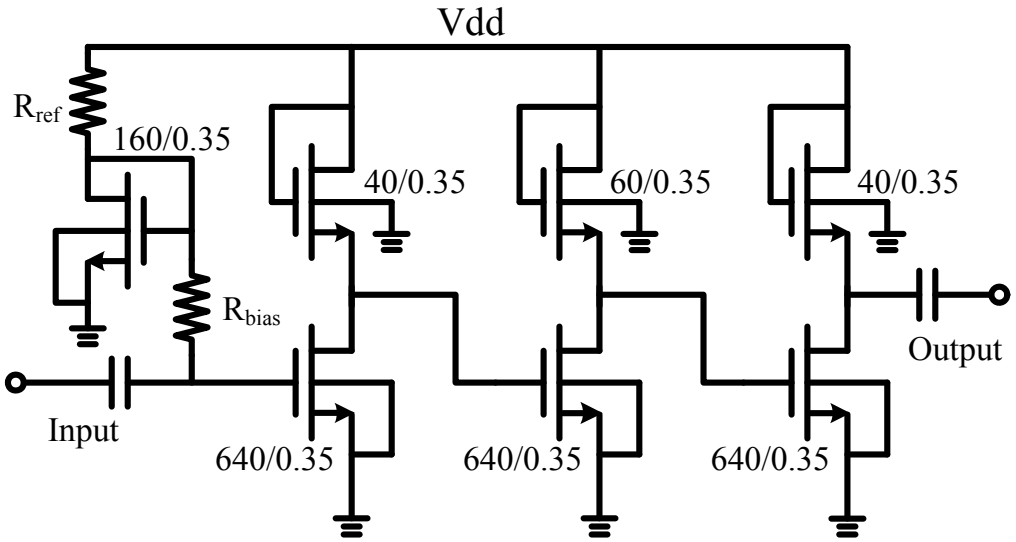
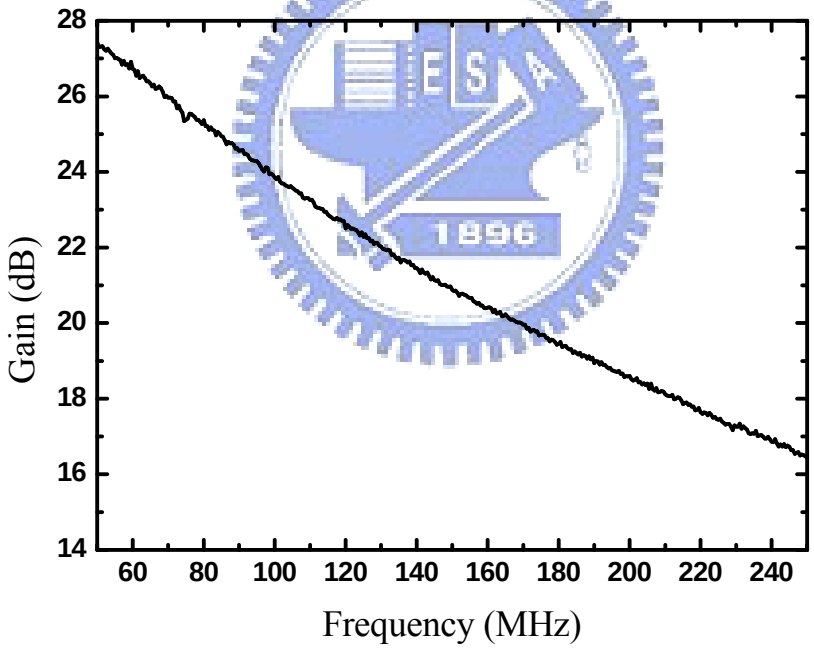


Fig. 4.3 The schematic of sensor system.



(a)



(b)

Fig. 4.4 Two port amplifier: (a) circuit schematic and (b) measurement result.

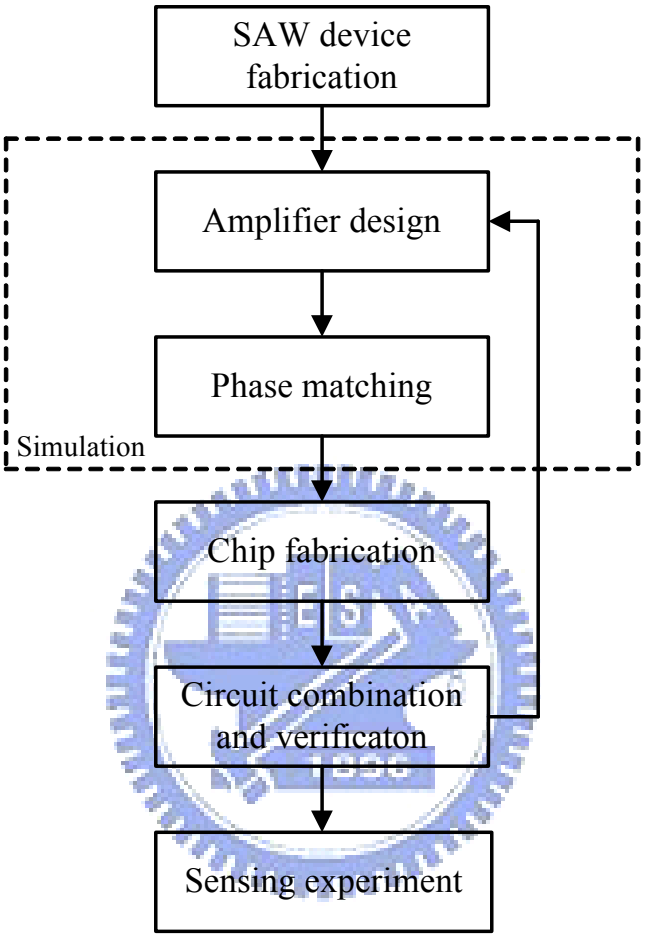


Fig. 4.5 The design flow of sensor circuit.

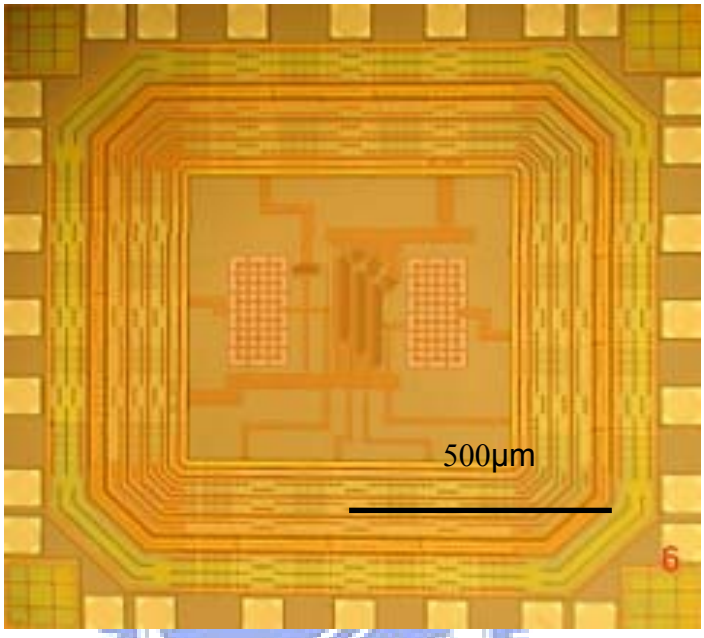


Fig. 4.6 The photo of the circuit.

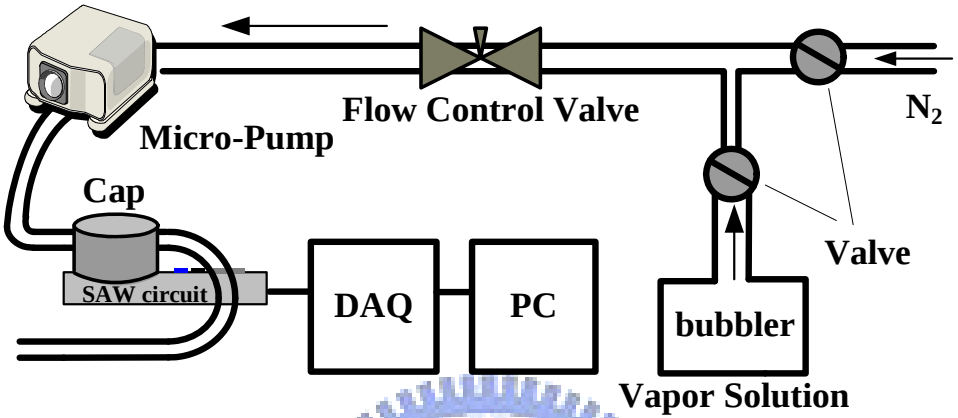


Fig. 4.7 Experimental sensing system in this study.

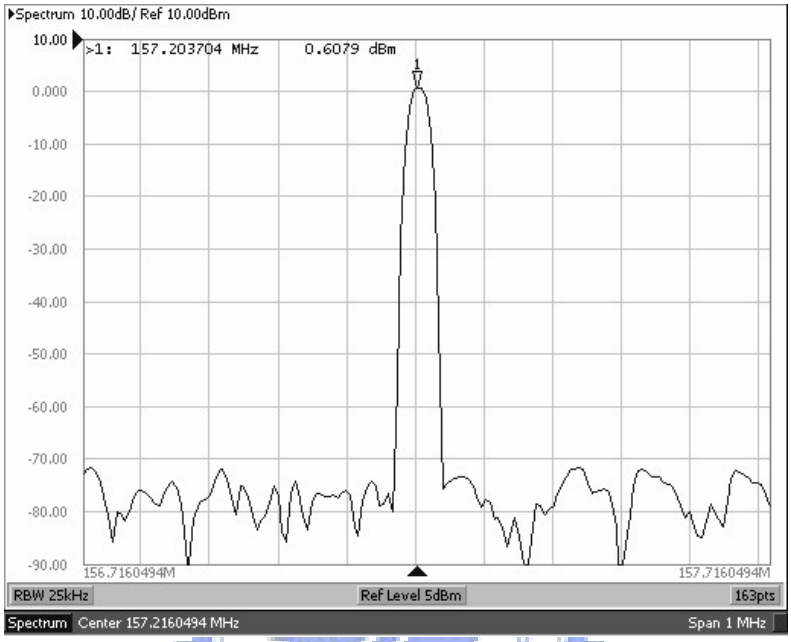


Fig. 4.8 The power measurement of oscillator.

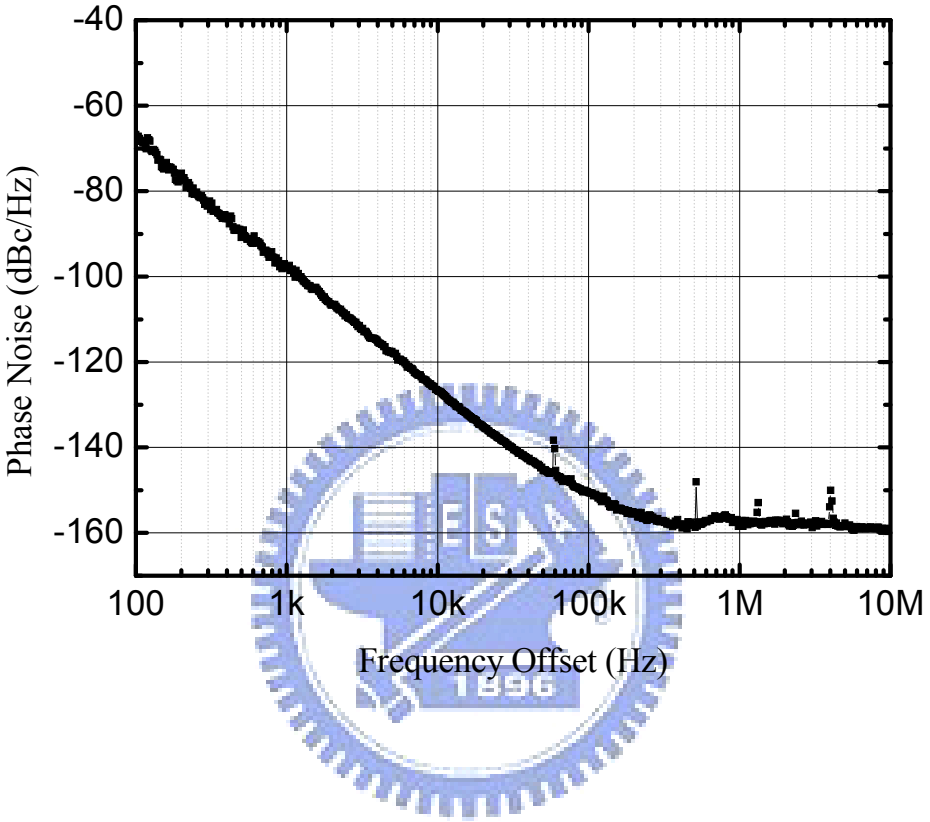


Fig. 4.9 The phase noise measurement of oscillator.

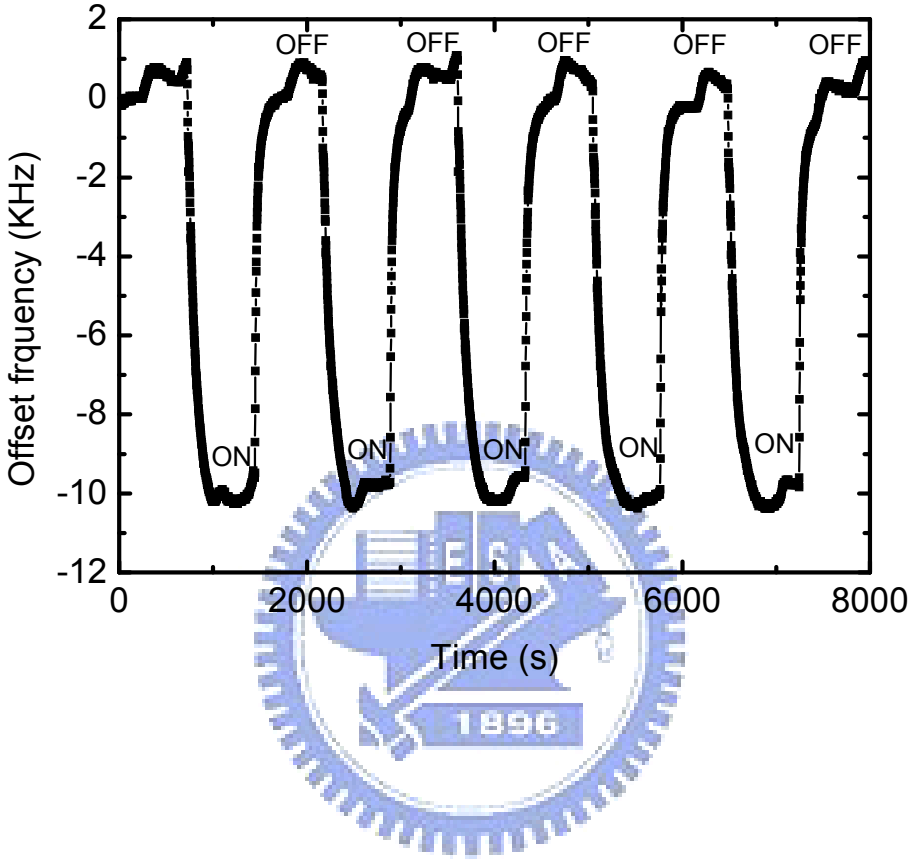


Fig. 4.10 Typical response of PECH film exposed to alcohol in pure N_2.

Chapter 5

Conclusion and Recommendations

5.1 Conclusion

The DC, AC, high-frequency, and RF power characteristics of LDMOS transistors with different layout design have been investigated in this study. This study also presents the sensing application using active device and SAW device. The annular structure of LDMOS transistors for RF applications was presented in this study. The annular structure had a better performance than the conventional structure, without altering the process flow. Without equivalent circuit optimization, RF performance curves for large-signal linearity and waveform of the LDMOS are verified. By way of the NVNA measurement system, the nonlinear model of LDMOS will be acquired easily and furthermore predict the large-signal behavior conveniently.

In chapter 2, annular and square structures were compared in terms of DC and AC, and power characteristics. The higher drain current and transconductance in the LDMOS with the closed structure (annular and square structure) were due to lower drain parasitic resistance. The cut-off frequency was also improved for the annular structure due to the lower drain parasitic resistance. This chapter was also present the effective width evaluation. By way of the evaluation process, the effective width of the closed structure can be calculated.

The PHD model composed of X-parameter was analyzed in chapter 3. The PHD model is a black-box frequency-domain, modeling, and simulation of driven nonlinear systems. This model can predict the nonlinear behavior of the active device, including the linearity, PAE, power contour and waveform. Using the NVNA measurement system, the nonlinear model via X-parameter provides a simple and direct way to get a large-signal model for power amplifier design. In this chapter, we also presented the nonlinear behavior of RF LDMOS using PHD modeling technique.

In chapter 4, a SAW delay-line reaction device and a CMOS amplifier has been demonstrated for the organic vapor sensing application. Sensing systems with closed chambers were also proposed in this study. The lower phase noise in this SAW sensor was due to the high-Q SAW delay-line reaction device. The sensing experimental results show that the maximum oscillation frequency shift between gas on and off is approximately 10 kHz with 50 x 10^3 ppm alcohol vapor concentration. This compact integrated microsensor will be promising for future chemical and biological sensing applications.

5.2 Recommendations for Future Work

Although the varied layout structures have been compared in terms of DC, capacitance and small-signal characteristics in this study, the simulation of these layout structures should be made more effort in the future. Using the high gamma impedance tuner with the NVNA system, the non-50Ω of PHD model for active device will be extracted accurately. Eventually, a complete measure-based large signal model for active device in any impedance can be built. In addition, the reliability issue of RF LDMOS is also an important study topic. Most of study looked into the various phases of the DC characteristics, and seldom study the RF or power characteristics. In the aspect of sensor application, the pattern recognition using neural network can be investigated in the future. By way of the neural network recognition system, the unknown vapor can be recognized correctly and accurately.

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Appendix 1. Capacitance extraction using time domain reflectometry

TDR is a well-established measurement method and commercial equipment is readily available. The TDR scope transmits a step function $V_{inc}(t)$ to the DUT through a transmission line. Due to the impedance mismatch between the transmission line and the DUT, some or all of the incident power may be reflected back as an echo $V_{ref}(t)$ and arrive back at the scope delayed by the travel time T_D.

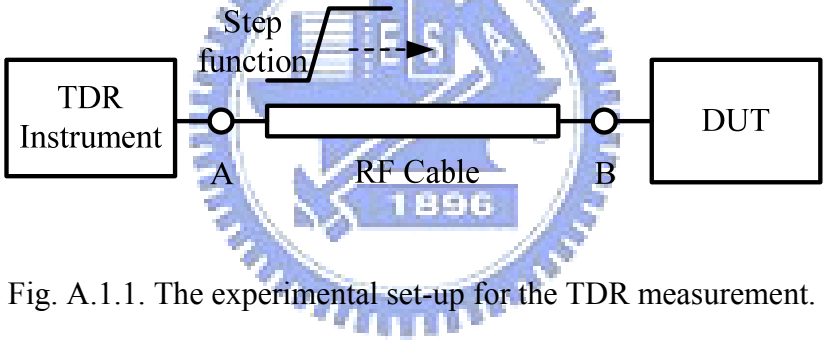

Fig. A.1.1. The experimental set-up for the TDR measurement.

Figure A.1.1 illustrates the basic TDR set-up. A TDR instrument is connected to the wafer-level device under test (DUT) via a RF cable and probe. The DUT is pad structure in this study. The signal (step function) is transmitted to the DUT by the TDR instrument with 35ps rise time. The instrument monitors both the transmitted and reflected waveforms as a function of time. Figure A.1.1 illustrates the waveform as seen at the input port (terminal B)

of the pad under test and at the port (terminal A) of TDR instrument. The data at terminal B is a capacitance component

The charging behavior of the capacitor is a measure of the stored charge in the capacitor. Intuitively, the area enclosed by the open (un-probing) waveform and the capacitor charging waveform represents the total stored charge at the end of the voltage step. In this case, the measure voltage waveform from the DUT in addition to the voltage waveform from reference, open end are used to calculate the capacitance using

$$C = \frac{1}{2Z_0 V_s} \int \left(V_{open}(t) - V_{DUT}(t) \right) dt \qquad \text{(A1.1)}$$

Where $V_{open}(t)$ is the open-circuit waveform; $V_{DUT}(t)$ is the capacitance waveform from the DUT, and V_s is the voltage of the step function. The integral represents the enclosed area of these two waveforms [1] [2].

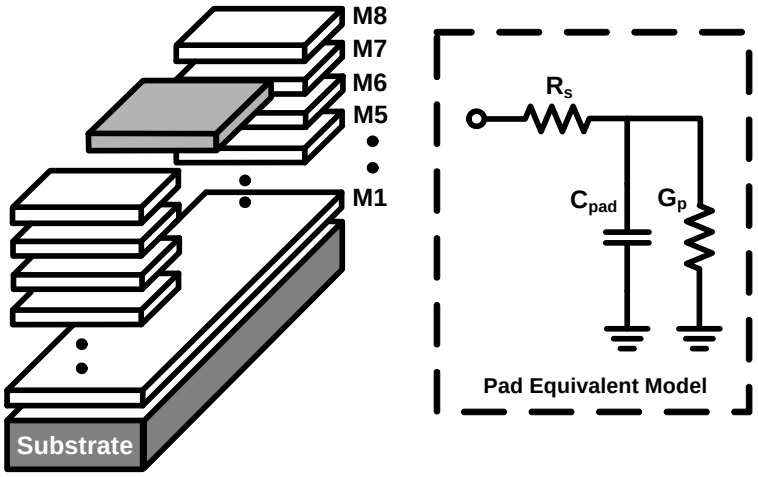

Fig. A.1.2. Single-Pad structure and equivalent model

Test structure used for capacitance extraction experiment in TDR measurement and polynomial curve fitting are shown in Fig. A.1.2. The RF compatible pad structure (GSG) was used in this study which includes 65x65 μm^2 single pad, face to face pads, and two pads with an interdigital capacitor in CMOS technology.

Figure A.1.3 shows the measurement system in this study. The Agilent 86100B sampling scope with 54754A TDR plug-in module was used. A fast rising step voltage pulse of about 35ps rise time generated by a pulse generator was propagated through a coaxial line system of characteristic impedance 50 Ω. The pad structure under test was placed at the end of the RF cable. The Cascade microtech S300 probe station and GSG probe was used in this measurement experiment due to the on-wafer probing.

In order to determine the closed area which enclosed by the DUT and open structure, the mathematical curve fitting method is needed. The curve fitting functions used in this study is polynomial fitting function. The curve fitting via polynomial function is through a set of X-Y data points and returns a table of polynomial cure coefficients, as well as, determines the best fit polynomial cure.

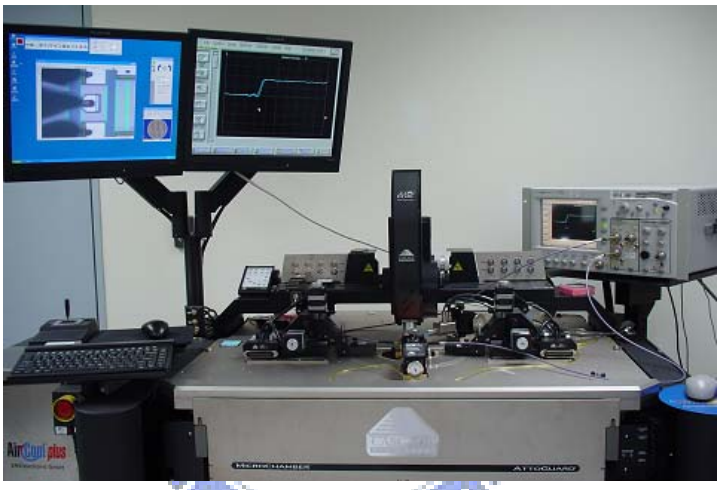

Fig. A.1.3. TDR on-wafer measurement system

To validate the accuracy of this method, capacitance extraction by vector network analyzer (VNA) is implemented to compare the data estimated via TDR instrument. Four DUTs are studied for VNA and TDR measurement with single pad (65x65 μm^2, 65x65 μm^2), two pads, and two pads with an interdigital capacitor. Figure A.1.4 shows the measurement results of open, single-pad, two-pads, and interdigital capacitance. If the capacitance of DUT increases, the waveform shifts toward the right side as shown in this Fig. A.1.4. By the mathematical

tool, the curve fitting result was shown in Fig. A.1.5. With the curve of Open and DUT fitted, capacitance can be calculated by the closed area between these two curves. Figure A.1.6 shows the capacitance extracted through scatter parameter at various DUTs. The measured capacitance by VNA and TDR are shown in Table A.1.1, respectively. It is noted that the capacitance is almost the same with the data through the VNA only if the capacitance is more and more larger.

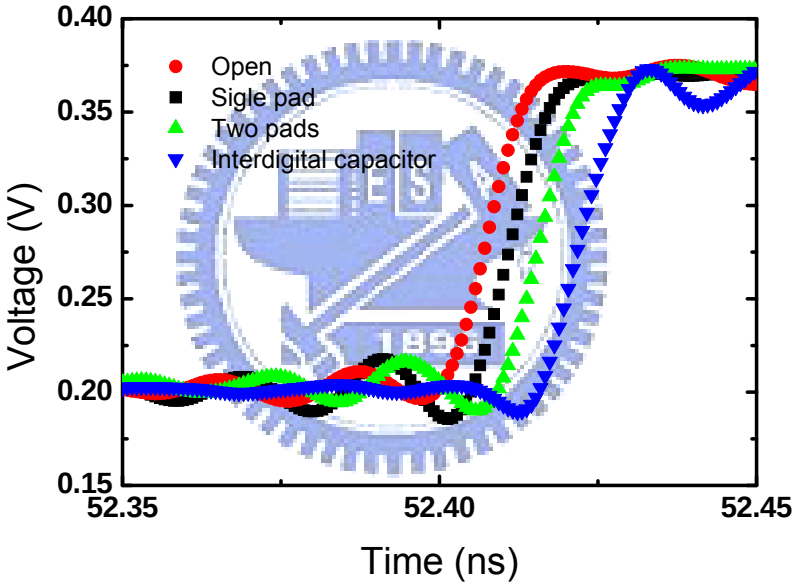

Fig. A.1.4. Measurement results (65x65 μm^2 pad, two pads, and interdigital capacitor) using TDR

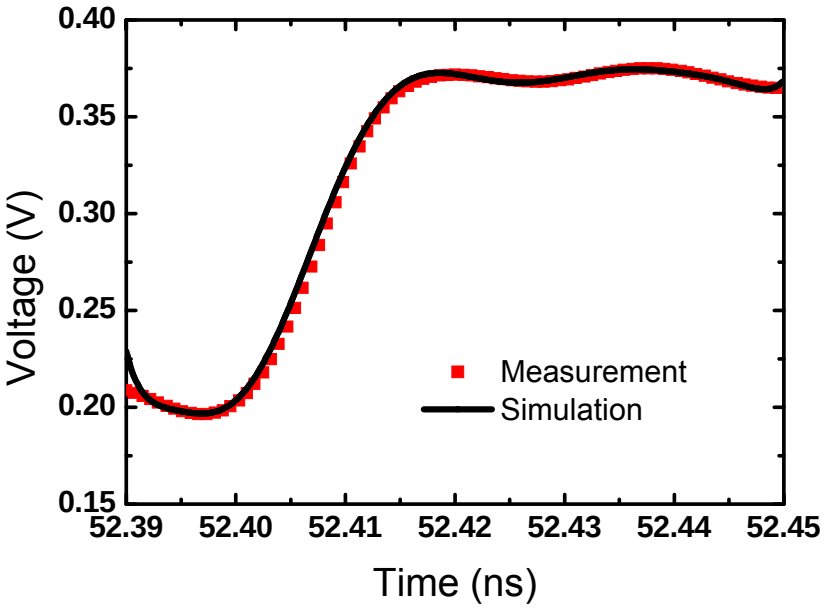

Fig.A.1.5. TDR measurement and curve fitting

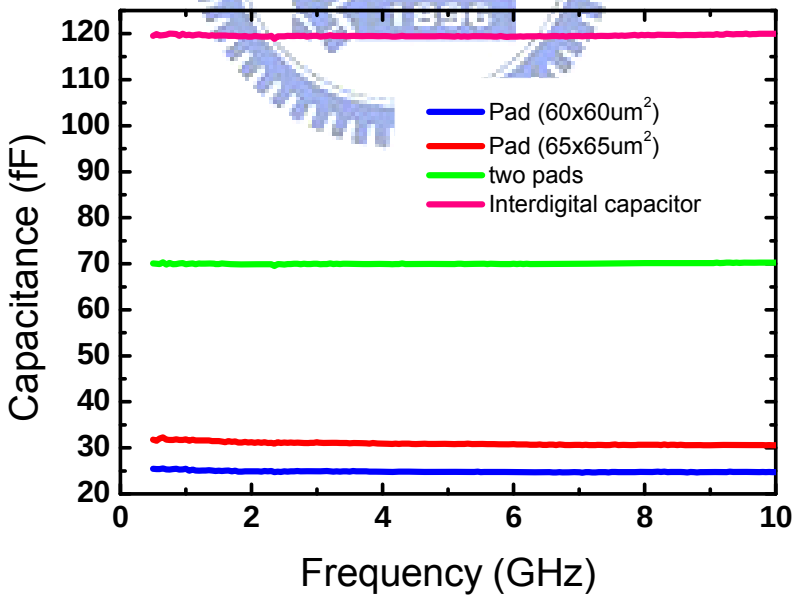

Fig. A.1.6. Capacitance extraction via s-parameter

Table A.1.1. Capacitance extraction via VNA and TDR. (unit: fF)

DUT	*VNA*	*TDR*
Pad (65x60μm^2)	25.1	22.5
Pad (65x65μm^2)	31.2	29.3
Two pads	70.1	68.6
Interdigital capacitor	119.6	120.8

Refenerce:

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Appendix 2. Describing function

A nonlinearity y(x,x') is excited by a sinusoidal input,

$$x = A\sin\omega t \tag{A2.1}$$

Then the output is expressible by the Fourier series expansion

$$y = (A\sin\omega t, A\omega\cos\omega t) = \sum_{n=1}^{\infty} A_n(A,\omega)\sin[n\omega t + \varphi(A,\omega)] \tag{A2.2}$$

and the sinusoidal-input describing function (DF), denote N(A, ω), is by definition

$$N(A,\omega) = \frac{\text{Phasor representation of output component at frequency } \omega}{\text{Phasor representation of input component at frequency } \omega}$$

$$= \frac{A_1(A,\omega)}{A} e^{j\varphi_1(A,\omega)} \tag{A2.3}$$

In other words, the definition of describing function is the complex fundamental-harmonic gain of nonlinearity in the presence of a driving sinusoid. The concepts of transfer magnitude and phase changes are actualized in this definition.

An equation for the DF in terms of y(x,x') is easily obtained. Multiplying both sides of Eq. A2.2. by either sin ω t or cos ω t, and integrating to determine the first Fourier coefficients, the relationships are showed

$$A_1\cos\varphi_1 = \frac{1}{\pi}\int_0^{2\pi} y(A\sin\omega t, A\omega\cos\omega t)\sin\omega t d(\omega t) \tag{A2.4}$$

$$A_1\sin\varphi_1 = \frac{1}{\pi}\int_0^{2\pi} y(A\sin\omega t, A\omega\cos\omega t)\cos\omega t d(\omega t) \tag{A2.5}$$

Multiplying (A2.5) by j, adding the two equations, and dividing both sides of the resultant equation by A, result in

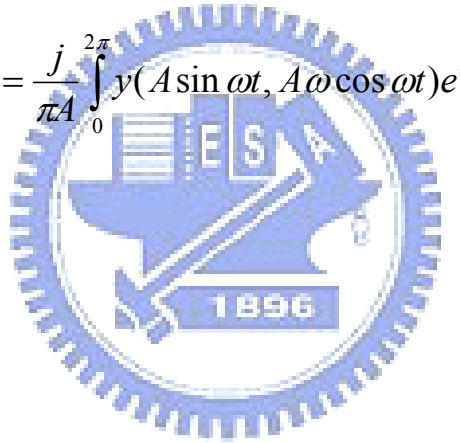
$$\frac{A_1}{A}e^{j\varphi_1} = \frac{j}{\pi A}\int_0^{2\pi} y(A\sin\omega t, A\omega\cos\omega t)e^{-j\omega t}d(\omega t) \qquad \text{(A2.6)}$$

where

$$e^{j\varphi} = \cos\omega t + j\sin\omega t$$

Comparing (A2.3) and (A2.6), the equation for the describing function in terms of the system nonlinearity becomes

$$N(A,\omega) = \frac{j}{\pi A}\int_0^{2\pi} y(A\sin\omega t, A\omega\cos\omega t)e^{-j\omega t}d(\omega t) \qquad \text{(A2.7)}$$



簡　　歷

姓　名： 邱佳松 (Chia-Sung Chiu)

性　別： 男

出生年月日： 民國 67 年 7 月 6 日

籍　貫： 台灣省台北縣

學　歷：

私立逢甲大學電子工程學系畢業(85年9月－89年6月)

私立中原大學電子工程學系碩士班(89年9月－91年6月)

國立交通大學電信研究所博士班(94年9月－98年6月)

經　歷：

國家奈米元件實驗室高頻技術組 助理研究員(92年1月~)

論文題目：

側向擴散金氧半電晶體之多諧波失真模型及表面聲波氣體感測器之設計

Polyharmonic Distortion Motel for LDMOS Device and SAW Gas Sensor Design