國 立 交 通 大 學
電 機 與 控 制 工 程 學 系

博 士 論 文

具輸入電流修飾與柔性切換特性的單級交流-直流轉換器

Single-Stage AC-DC Converters with Input Current Shaping and Soft-Switching Features

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指 導 教 授：張 隆 國 博 士

中華民國九十六年八月

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摘要

本論文旨在發展出具新穎性的單級交流-直流轉換電路以提升整體效能並符合成本效益，這些設計都是基於減低諧波污染的前提下所設計的，並可滿足如 IEC 61000-3-2 等電流諧波標準規範。

一般使用升壓型輸入電流修飾設計的的單級交流-直流轉換器常見的問題包括：開關電流應力過大並帶來額外的開關功率損失，以及使用電壓隨耦功因修正技術造成的輸入線電流失真。我們除了使用主動箝位的電路設計外，較新穎部分的解決策略分別為：改讓升壓電感在開關截止時做充磁以減緩開關導通時的電流應力和功率損耗；以及，輸入電流修飾子電路配合輸入線電壓的瞬間值自動調整其充磁時間，使得升壓電感的充磁電流得以補償放磁電流所造成的非線性失真，以此設計，輸入側的電流-電壓曲線可得到近乎線性的關係。

另一個需要面對的關鍵問題則是儲能電容電壓應力過大。本論文對此提出一個新型的單級交流-直流轉換器，此架構使用一反馳式與順向式整合型電路作為直流-直流輸出調整器。在此架構中，反馳式與順向式子轉換器分別被操作在連續導通模式與非連續導通模式之下。因此，在輕載的情況下，藉由抑止反馳式並維持順向式的正常運作即可利用非連續導通模式的輸出特性有效地抑制儲能電容電壓，並能保證在各種工作情況下都低於一般電容的最大電壓容忍值 450 V。

本文中所提出的技術皆已在泛用型輸入電源（90–260 Vrms）的測試條件下實證過，實驗結果證明本文所提出的設計可有效地解決電流應力過大、電壓應力過大與轉換效率不佳的問題。

Single-Stage AC-DC Converters with Input Current Shaping and Soft-Switching Features

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Abstract

This dissertation presents innovative techniques and solutions to simultaneously improve the performance and satisfy the cost-effective consideration for the single-stage input current shaping (S^2ICS) AC-DC converters. These designs are based on the consideration for limiting the line current harmonics, especially for meeting the stringent current harmonic regulations, such as IEC 61000-3-2.

For general S^2ICS converters employing boost-type input current shaping (ICS) cells, these circuits usually suffer from the relatively high switch current stress and line current waveform distortion caused by the voltage-follower control. To remedy these drawbacks, this dissertation presents a novel ICS technique for S^2ICS converters. Unlike the conventional single-stage designs, the proposed ICS scheme is intentionally arranged to be charged in the duty-off time. With this design, the switch current stress in the duty-on time is significantly mitigated and accordingly the power loss is reduced. Moreover, this design produces AC modulation effect on the charging time of the ICS cell so that the waveforms of the average charging current and average discharging current of the boost inductor can compensate each other automatically. Consequently, the input i-v curve has nearly linear relationship.

Another key issue of the S^2ICS technique is the high bulk capacitor voltage stress. This dissertation also presents a novel S^2ICS converter employing flyback-forward topology as the downstream DC-DC cell. In the proposed topology, the flyback and forward sub-converters are operated in CCM and DCM, respectively. Thus, by deactivating the flyback sub-converter and keeping the forward sub-converter supplying the output power, the bulk capacitor voltage at light load condition can be effectively suppressed and reliably maintained below the 450 V tolerance of commercially available electrolytic capacitors.

All the proposed techniques have been verified by prototype circuits under universal line voltage condition (90–260 Vrms). Experimental results show that the proposed designs can effectively address the main issues including high current stress, high voltage stress, and low conversion efficiency.

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于新竹交大

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CHAPTER 1

INTRODUCTION

1.1 Background

Conventionally, most of the power conversion equipment employs either diode rectifier or thyristor rectifier with a bulk capacitor to converter AC voltage to DC voltage before processing it. For example, Fig. 1.1(a) shows the circuit diagram of a diode-bridge rectifier. The diode bridge D_r rectifies the AC input voltage and the capacitor V_b smoothes out the resulting voltage to make it an almost pure DC waveform. The current drawn from the AC utility source, however, has a pulse-like non-sinusoidal waveform because the bridge diodes conduct current only when the rectified input voltage is equal to or greater than the bulk capacitor voltage. As a result, the input current waveform has narrow conduction angle and strong distortion, as shown in Fig. 1.1(b).

For any electrical equipment drawing power from the utility, power factor (PF) is a widely used term to evaluate the quality of input power accomplished. Obviously, the diode-bridge rectifier shown in Fig. 1 has a poor PF because of the non-sinusoidal input current. This current has a pulsating shape and thus contains large harmonic components that are injected into the utility supply. If vast numbers of such converters are used in industry, the harmonics injected in the utility will be so large that they will create a need for increasing volt-ampere ratings of utility equipment (i.e., transformers, transmission lines, and generators) and distort the utility voltage.

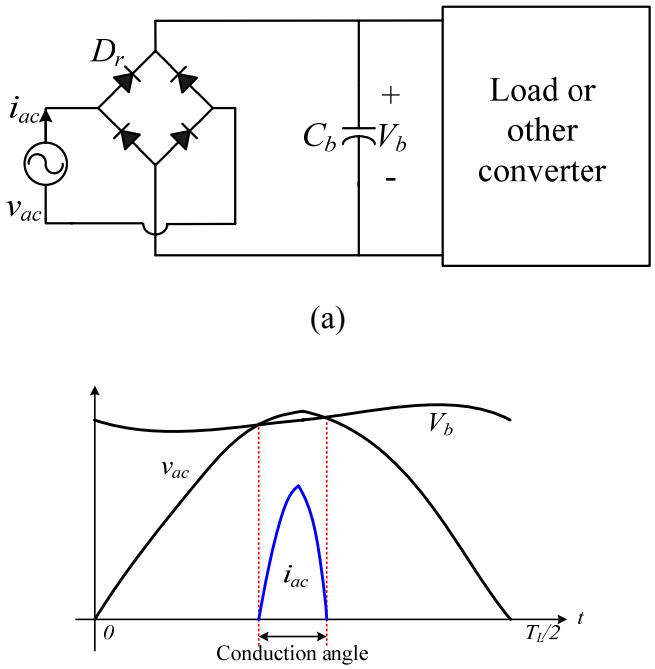


Fig. 1.1 Conventional diode-bridge rectifier: (a) circuit diagram and (b) key waveforms in a half line cycle.

Since a severely distorted AC utility voltage can damage sensitive electrical equipment, regulatory agencies around the world have established standards on the current harmonic content produced by electrical equipment [1]-[4]. Stricter regulatory agency standards on harmonic content have resulted in the demise in popularity of the simple diode-bridge rectifier as the front-end converter in electrical equipment. Meanwhile, more and more electrical equipment manufacturers are forced to improve or correct the input PF of products supplied by an AC utility source. To comply with the line harmonics standards, a variety of passive and active power factor correction (PFC) techniques have been proposed [5], [6]. The passive techniques normally use a simple line-frequency LC filter to both extend the current conduction angle and reduce the total harmonic distortion (THD) of the input current of the diode-bridge rectifier. Due to its simplicity, the passive LC filter could be the high efficiency and low cost PFC solution to meet the line current harmonics specifications in the low power

range [7]. However, the passive LC filter has a major drawback which is its heavy and bulky low-frequency filter inductor.

To reduce overall size and weight and increase the power quality further, the active PFC techniques have been introduced. In an active PFC converter, the filter inductor is operated at the switching frequency, which is normally in the 10 kHz to hundreds of kHz range. Therefore, the size and weight of the power converter can be significantly reduced by using a high-frequency inductor. The cost of the active PFC approach can also be lower than that of the passive filter approach if the conversion power increases. In general, the single-phase active PFC techniques can be divided into two categories: the two-stage approach and the single-stage approach [8], [9]. These two approaches are introduced in the following.

1.1.1 Two-Stage AC-DC Conversion Technique

The most popular implementation of active PFC is two-stage approach. In this method, an active PFC stage is adopted as the front-end to force the line current to track the line voltage, therefore achieving unity input PF. The PFC front-end stage converts the AC input voltage into DC voltage on a bulky energy-storage capacitor. Then a conventional DC-DC converter is used as the second stage to provide isolation and regulated output voltage.

Figure 1.2 shows an example circuit of the two-stage AC-DC converter. The first PFC stage can be a boost, buck-boost or flyback converter. Generally, the boost converter is the most popular topology. In the PFC stage, there is an independent PFC controller, which controls the PFC switch S_1 in order to achieve sinusoidal input current waveform [10]. Meanwhile, the PFC front-end stage also provides a loosely regulated high DC bus voltage V_b with small double line-frequency ripples. In general, V_b is loosely regulated around 380–400 V, even the line input voltage changes from 90 to 260 Vrms for the universal-line applications. V_b is also the input voltage of the downstream isolated DC-DC output converter, which pro-

vides a tightly regulated low output voltage V_o with a high bandwidth feedback control loop.

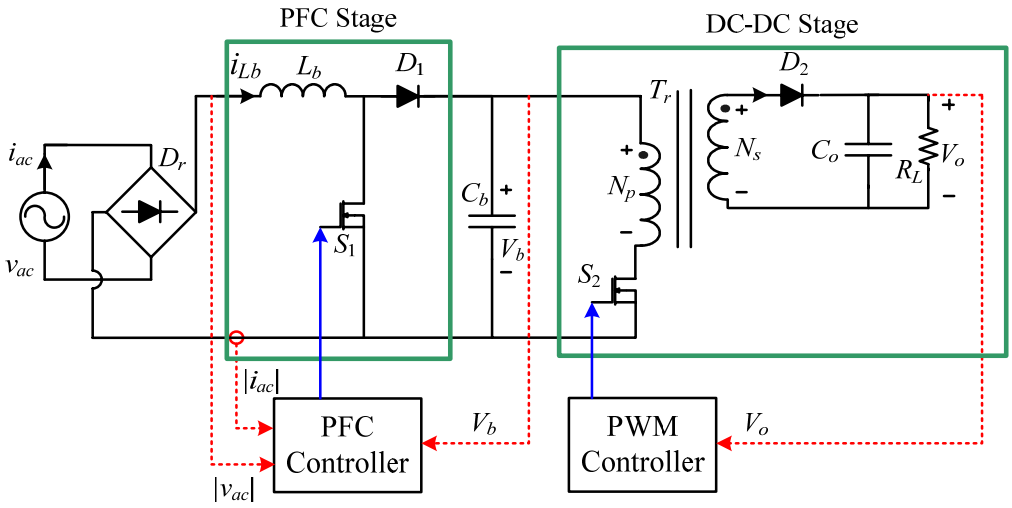


Fig. 1.2 Example circuit of the two-stage AC-DC converter.

The boost inductor in the PFC stage can be operated in several different conduction modes, such as discontinuous conduction mode (DCM), variable-frequency critical (boundary) conduction mode, and continuous conduction mode (CCM). In terms of control implementation, the DCM PFC approach requires the simplest control. The PFC switch S_1 is operated with a constant duty ratio and fixed switching frequency during a half line cycle, without sensing the input voltage or current [11], [12]. This provides a low cost solution for low power applications. The drawback of the DCM boost rectifier is its high input inductor current ripple, which causes high current stress on the semiconductor switch and requires a large electromagnetic-interference (EMI) filter. To reduce the input current ripple, the critical mode PFC provides an alternative solution with a slightly more complicated control circuit, for input power of up to 500–600 W. In the critical mode PFC, the boost switch is operated with a variable switching frequency in a half line cycle [13], which keeps the boost inductor operating at the boundary of DCM and CCM. The boost inductor current ripple has a peak value of twice that of the average input current. The variable frequency control also spreads the noise spectrum in the wide frequency range, which can further reduce the EMI filter size [14]. How-

ever, the wide switching frequency range causes difficulty in the optimal design of filter. Besides, the input current ripple is still large. To further reduce the current ripple and EMI filter size, the CCM PFC approach is widely adopted in the power range from hundreds of watts to several kilowatts. The CCM PFC performs very well, but it requires the most complicated control implementation [10].

In summary, the active two-stage PFC converter has good input PF and can be used in wide ranges of input voltage and output power. This technique is mature and the converter has good performance. However, it requires additional PFC power stage and PFC controller, so the component count, the circuit size and weight, and the total cost are increased.

1.1.2 Single-Stage AC-DC Conversion Technique

For low power applications, such as computer electronic products, the development trend is to rigorously pursue the reduction of size, weight, and cost. Thus, to reduce the added component count and cost of the PFC stage in the two-stage approach, cost-effective alternatives attempt to integrate the active PFC input stage with the isolated DC-DC converter. A number of single-stage PFC techniques have been proposed in recent years [15]-[41]. The main objective of this method is really input current shaping (ICS); thus, these circuits are also named as single-stage ICS (S^2ICS) converters.

In the S^2ICS converter, the PFC inductor is still necessary, but neither the PFC switch nor its controller is needed. The remaining controller is the pulse-width-modulation (PWM) controller, which focuses on the tight regulation of the DC output voltage. Meanwhile, the input PFC function can be automatically achieved. Fig. 1.3 shows how to integrate a boost PFC rectifier with a flyback DC-DC converter to obtain a S^2ICS AC-DC converter. When the DC-DC converter is operated in the steady state, the duty ratio of the PWM switch is almost constant during a half line cycle. Moreover, the line current can automatically track the line

voltage by operating the boost inductor in DCM and constant duty ratio, as mentioned in sub-section 1.1.1. This design concept is namely the voltage-follower PFC technique [11] or the self-PFC property [12]. Since the DCM boost switch S_1 and the DC-DC converter switch S_2 are both operated with constant duty ratio, these two switches can be integrated into one switch by using the same duty ratio and switching frequency [15]. Thus, it is possible to integrate a DCM boost PFC rectifier with a flyback DC-DC converter to get a S^{2}ICS AC-DC converter without the PFC switch and its controller.

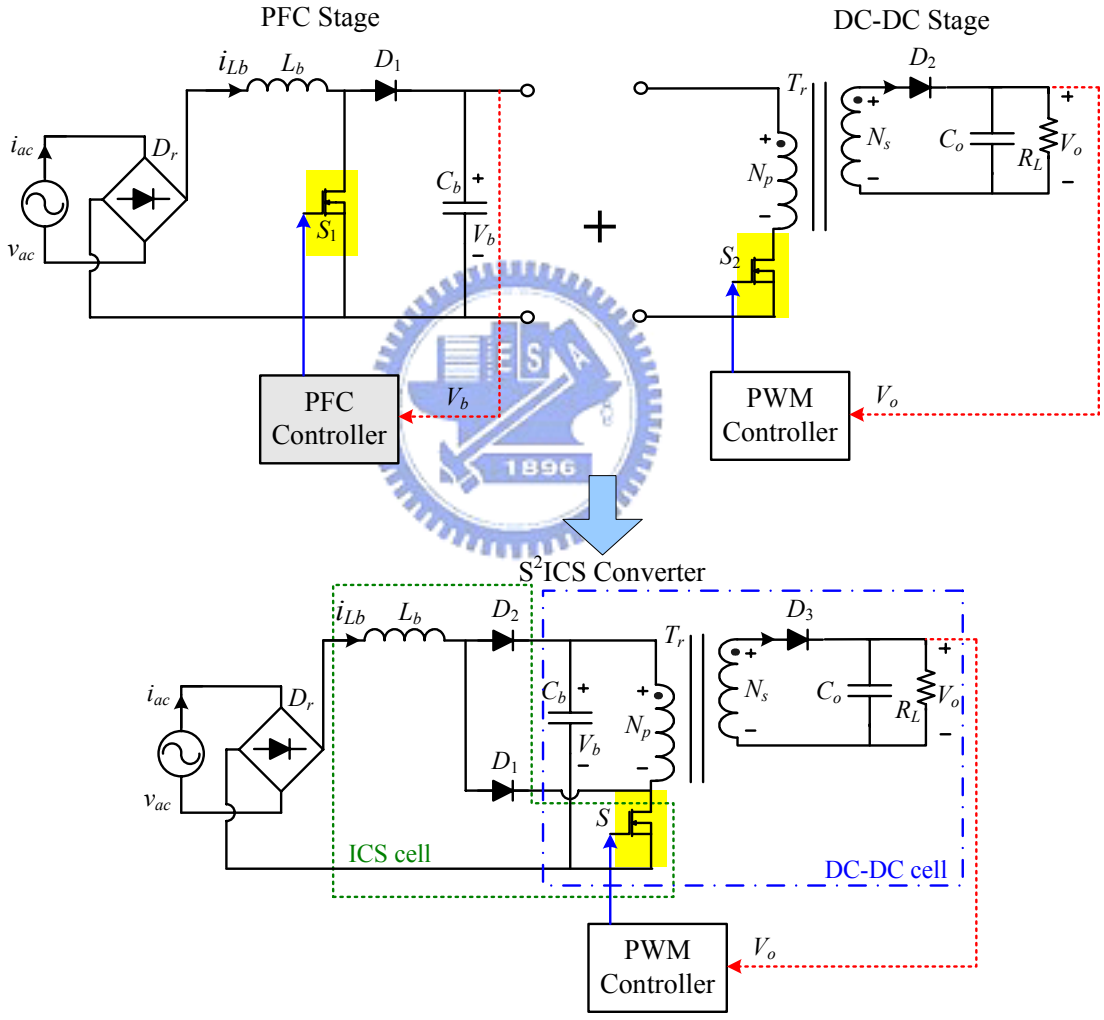


Fig. 1.3 Combining a DCM boost PFC front-end and a PWM DC-DC converter to obtain a S^{2}ICS AC-DC converter.

Generally, the input power factor of a S^{2}ICS converter is not unity, but its input current

harmonics are small enough to meet the current harmonic constraints, such as the IEC 61000-3-2 Class D. Since instantaneous AC input power always varies, an internal bulk capacitor C_b is needed to buffer the instantaneous difference between the varying input power and a constant output power such that the output voltage is regulated tightly and free of line frequency ripple. Unlike in the two-stage PFC converter, the bulk capacitor voltage V_b in the S^2ICS converter is no longer regulated and varies with the line voltage and load current since the control freedoms are reduced by integrating the PFC and DC-DC switches into one switch.

Moreover, the design of control circuit and power stage of the DC-DC cell is the same as that of a conventional switching-mode power supply. For the DC–DC regulator circuit, working in the CCM is usually the preferred mode of operation, due to the lower turn-off loss and smaller current stress on the semiconductor devices. Therefore, the combination of a DCM ICS cell and a CCM DC-DC cell is deemed to be ideal for S^2ICS converters. A general block diagram of S^2ICS converters is shown in Fig. 1.4. However, this approach has an undesirable feature: high bulk capacitor voltage stress at light load. It should be noted that this issue may become severe and critical while the situation with high line and light load occurs [33]. To explain why the bulk capacitor voltage arises while the load becomes light, Fig. 1.5 is given as follows. This figure shows the relationship between the average input power over a half line cycle $P_{in(ave)}$ and the duty ratio in the ICS cell, and between the average output power over a half line cycle $P_{o(ave)}$ and the duty ratio in the DC-DC cell.

Assume that the original value of the average input power and average output power is P_1. Since the DC-DC cell operates in CCM, the duty ratio will not change when the output power suddenly drops from P_1 to P_2. As shown by the solid curves of Fig. 1.5, it can be seen that the input power still stays in the original power P_1 due to the unchanged duty ratio D_1. Since P_1 is greater than P_2, the fact that the excess input energy will be stored in the bulk capacitor causes the bulk capacitor voltage to increase from V_{b1} to V_{b2}, as shown in the dashed

curves. Under constant output voltage control, the duty ratio will decrease from D_1 to D_2. Finally, new balance arrives, where $P_{in(ave)} = P_{o(ave)} = P_2$ and $V_b = V_{b2} > V_{b1}$. Consequently, the power balance at light load is reached at the penalty of significant bulk capacitor voltage stress. In the high line and light load condition for universal line applications, the generated bulk capacitor voltage could be as high as over 1000 V such that selection of switches and capacitors is limited and very costly [33], [49]. Thus, this drawback makes the single-stage designs impractical for the applications that require a universal input voltage of 90–260 Vrms and a wide range of load variation.

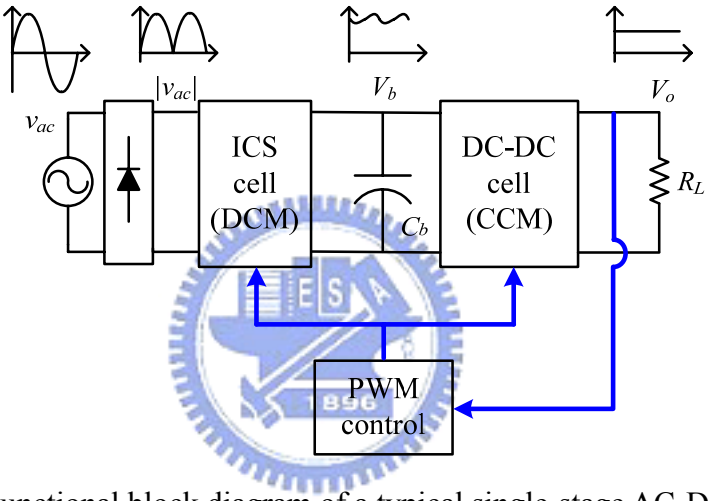


Fig. 1.4 Functional block diagram of a typical single-stage AC-DC converter.

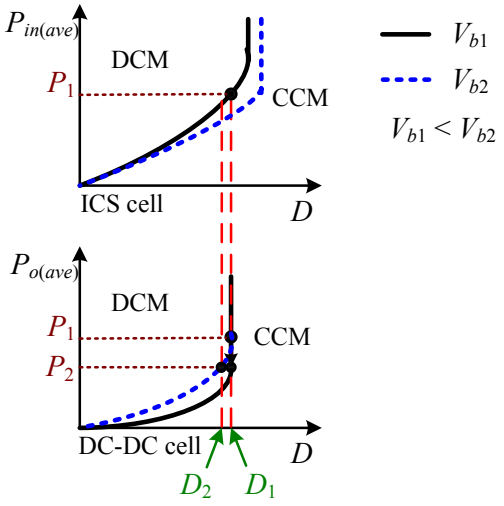


Fig. 1.5 Relationship between the average input power, average output power, and duty ratio for DCM ICS + CCM DC-DC.

1.1.3 Standards Regulating Line Current Harmonics

In the international society, some standards for the harmonic content of the line current of a power converter are published. As early as 1982, the International Electrotechnical Committee (IEC) published its standard IEC 555-2 [1], which was also adopted in 1987 as European standard EN 60555-2, by the European Committee for Electrotechnical Standardization (CENELEC). In 1995, standard IEC 555-2 has been replaced by standard IEC 1000-3-2 [2], and also adopted by CENELEC as European standard EN 61000-3-2.

Standard IEC 1000-3-2 applies to equipment with a rated current up to and including 16 Arms per phase which is to be connected to 50 Hz or 60 Hz, 220–240 Vrms single-phase, or 380–415 Vrms three-phase mains. The standard has been revised several times and a second edition was published in 2000 [3] with an amendment in 2001 [4]. Meanwhile, the standard was renamed as IEC 61000-3-2, which has become the most important and popular standard regulating line current harmonics. It should be noted that the limits do not apply for equipment with rated powers of 75W or less (it may be reduced to 50W in the future), other than lighting equipment.

The standard divides electrical equipment into four classes: A, B, C and D. The four classes include electrical equipment as follows:

Class A: Balanced three-phase equipment, household appliances (excluding equipment identified as class D), tools (excluding portable tools), dimmers for incandescent lamps and audio equipment. Equipment not specified in one of the other three classes should be considered as Class A equipment.

Class B: portable tools and arc welding equipment which is not professional equipment.

Class C: lighting equipment, including dimming device.

Class D: personal computers and personal computer monitors, and television receivers

(active input power equal or less than 600 W).

The converters proposed in this dissertation shall be applied in modern electronic products, such as personal computers, computer peripherals, and television receivers. All these electronic products' input power is less than 600W. Therefore, the experimental results will be criticized by employing the standard Class D. The current harmonics limits for Class D are shown in Table 1.1.

Table 1.1 Limits for Class D equipment in standard IEC 61000-3-2

Harmonic wave Order n	Maximum permissible harmonic current per watt (mA/W)	Maximum permissible harmonic current (A)
3	3.4	2.30
5	1.9	1.14
7	1.0	0.77
9	0.5	0.40
11	0.35	0.33
13	3.85/n	0.21
15≦n≦39		0.15×(15/n)

1.2 Motivation and Objectives

Theoretically, changing the two-stage scheme to single-stage scheme can substantially mitigate the cost and complexity of PFC AC-DC converter. However, the concept of single-stage design still has not been extensively adopted in today's power products. This is because there are still some of the existing technical challenges with respect to the development of viable S^2ICS AC-DC converters, such as high voltage stress, high current stress and low conversion efficiency, etc.

With the enforcement of newly issued international regulations, the cost-effective single-stage AC-DC conversion has become one of the hottest research areas in power electronics. This dissertation is intended to address the major technical issues in existing single-stage AC-DC converters and to give simple, reliable, efficient, and cost-effective solutions.

1.3 Dissertation Outline

This dissertation is composed of five chapters. The content of each chapter is briefly described as follows:

Chapter 1 introduces the background regarding the present power factor correction techniques and line current harmonics standard. It then lists the research motivations and objectives.

Chapter 2 offers a review for proposed techniques for the single-stage AC-DC converters and discusses various issues, trend and challenges.

Chapter 3 first introduces the mechanism of the proposed ICS technique. Then, a new flyback converter employing the proposed ICS scheme is presented. The content in this chapter contains circuit description, operation principle, circuit design procedure, and prototype experiment results. In addition, an extended circuit based on topology refinement is proposed for specific applications.

Chapter 4 deals with the problem regarding high bulk capacitor voltage stress at light load. A new flyback-forward converter with the modified ICS scheme proposed in Chapter 3 is presented. The mechanism and performance of the proposed approach for suppressing bulk capacitor voltage stress are discussed in detail. The content also covers several segments which are the same as in Chapter 3.

Chapter 5 summarizes the conclusions of this work and presents suggestions for further work in related research directions.

CHAPTER 2

REVIEW OF EXISTING SINGLE-STAGE AC-DC CONVERTERS

In the last decade, the heat wave of studying single-stage ICS AC-DC converters has resulted in hundreds of published papers. For single-stage AC-DC converters, the performance measures, such as efficiency, component count and circuit complexity, component voltage and current stresses, input current quality, etc., are largely dependent on the circuit topology. Thus, the main objective of this chapter is to present a topological study of the representative S^2ICS converters and find a topological relationship among various converters. This study can be used to topologically explain the main drawbacks of current S^2ICS converters and pursue potential topology variations to overcome the barriers that limit the application of S^2ICS converters.

2.1 Familiar Single-Stage Input Current Shaping (S^2ICS) Converters

The concept for S^2ICS AC-DC converters can be traced back to some early work presented in 1991 [18], [19]. In article [18], Kherulawa *et al*. proposed a single power stage with dual outputs, including the desired DC output and a boosting supply in series with the input, as shown in Fig. 2.1. Without active control of the boost supply, a reasonably good input current shape can be obtained due to the natural characteristics of the boost resonant circuit. This circuit is original but the component count is high. Takahashi *et al*. proposed another way to realize S^2ICS AC-DC converters, which cascades a boost ICS circuit with a DC-DC converter using one switch [19]. As shown in Fig. 2.2(a), a high frequency "dither source" is inserted between the input boost inductor L_b and the bulk energy-storage capacitor C_b. Since the dither

source introduces high-frequency pulsating voltage on L_b during one line cycle, the rectifier diode can conduct current even while the instantaneous input line voltage is much lower than the capacitor voltage V_b, as shown in Fig. 2.2(b). As a result, the input current conduction angle is significantly enlarged and the input current harmonics are reduced. This circuit presents an early form of the single-stage PFC method that integrates a boost PFC rectifier with a DC-DC converter in a cascade fashion.

So far, many papers have been presented about integrated single-stage AC-DC conversion techniques. In order to systematically understand the basic structure and specific performance of various converters, it is necessary to categorize the representative circuits published in recent years. Our survey will focus on the single-stage designs with boost-type ICS cells. From several points of view, including power flow paths, topology structures, and input current shapes, these circuits can be divided into the following categories as introduced in subsections 2.1.1–2.1.4.

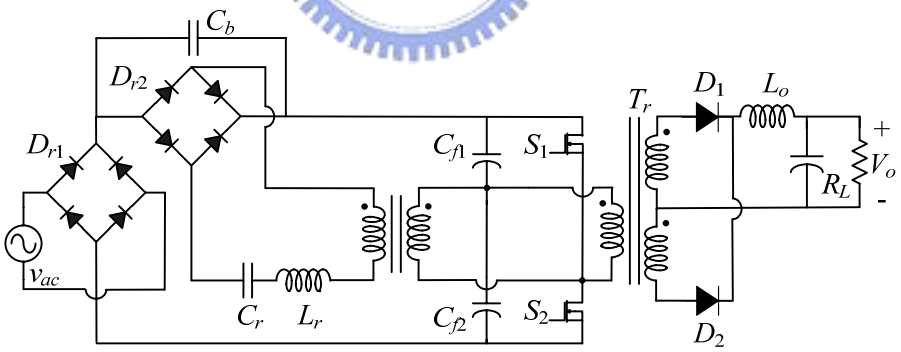
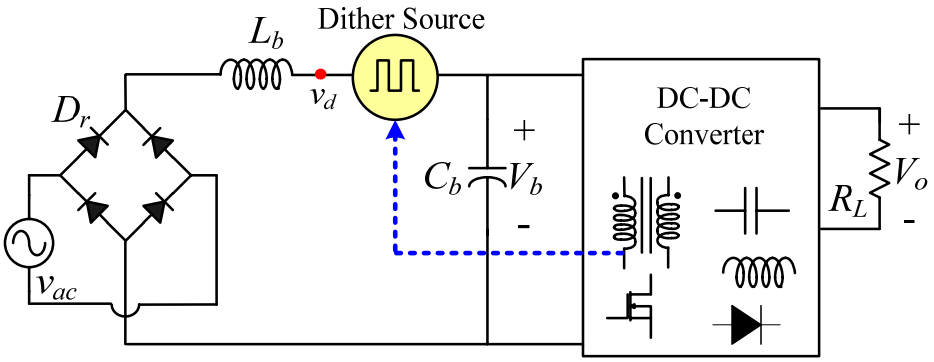
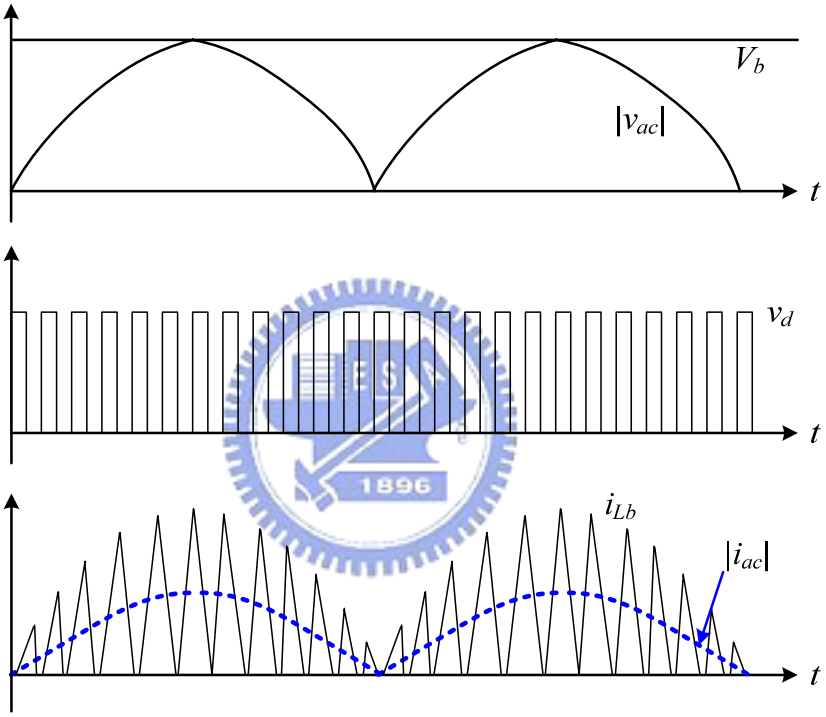


Fig. 2.1 Isolated S^2ICS technique using a two-output dual-control converter [18].



(a)



(b)

Fig. 2.2 General structure of "dither-rectifier" and its waveforms [19]:

(a) Circuit diagram, (b) conceptual waveforms.

2.1.1 S^{2}ICS Converters with Cascade or Parallel Power Processing Structure

Conventional single-stage AC-DC converters were derived from two-stage scheme and thus synthesized with a cascade method [15]. As shown in Fig. 2.3(a), the single-stage AC-DC converters have the dominant configuration integrating two circuit parts. The first part is derived from a boost-type circuit and has the automatic ICS function. The second part

is a DC-DC circuit with a bulk capacitor C_b placed between this circuit and the ICS cell. The downstream DC-DC cell is used to realize fine output regulation, isolation, and fast dynamic response. In terms of power transfer, the AC input power in such a design must first be transferred into the intermediate bulk capacitor C_b; this process is completed by the ICS cell. Then the power stored on the bulk capacitor C_b is processed again by the DC-DC cell to reach final output. The block diagram for explaining power transfer is shown in Fig. 2.3(b). This double power processing results in low conversion efficiency, which is the product of the efficiency of each functional cell.

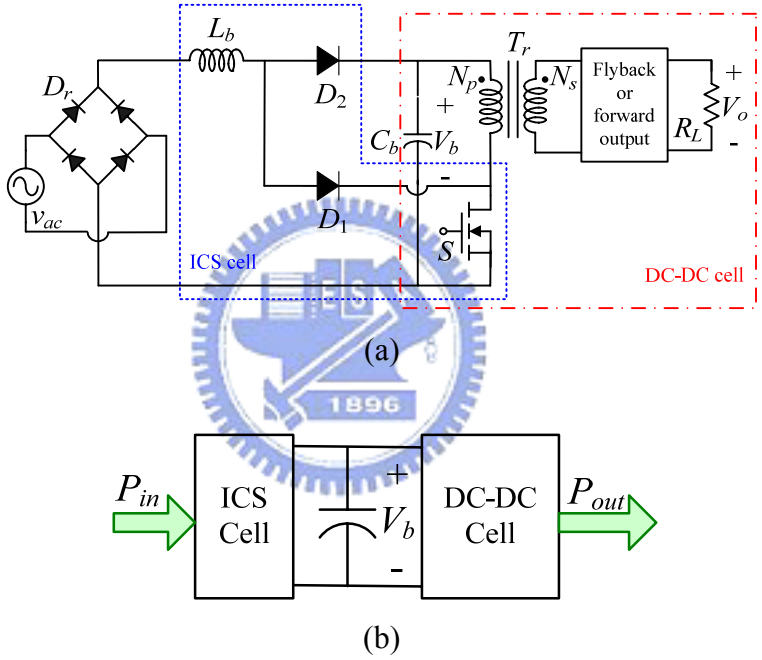
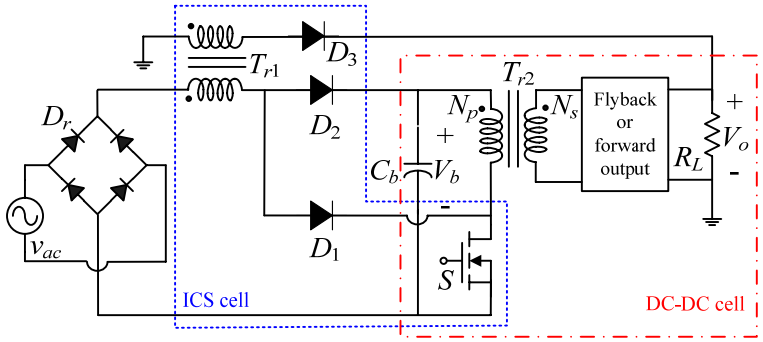


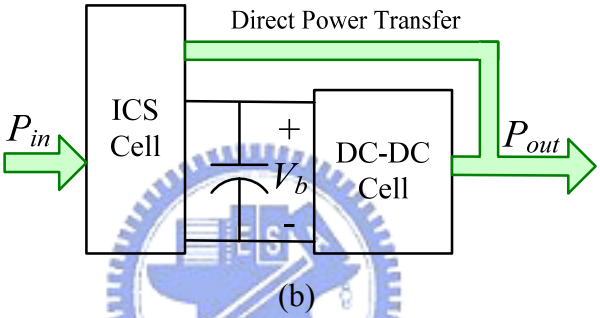
Fig. 2.3 S^{2}ICS converter with cascade power processing structure: (a) example circuit [15] and (b) power transfer block diagram.

In order to improve conversion efficiency, some new power transfer approaches have been proposed in [22]–[28] which allow a part of the input power to be processed only once and let the remaining input power to be processed twice while still achieving both high PF and tight output regulation. Those power transfer approaches provide a new way to achieve more efficient and higher power rating S^{2}ICS converters than the conventional double power

processing approach shown in Fig. 2.3. An example circuit of the direct power transfer approach is shown in Fig. 2.4(a) and its power transfer block diagram is shown in Fig. 2.4(b).



(a)



(b)

Fig. 2.4 S^{2}ICS converter with parallel power processing structure: (a) example circuit [25] and (b) power transfer block diagram.

2.1.2 S^{2}ICS Converters with Two-Terminal or Three-Terminal ICS Cells

With the consideration of ICS realization mechanism, the ICS circuits can be symbolized as two- or three-terminal cells [16], [17]. Each ICS cell contains a boost inductor L_b and two branches, as shown in the dotted rectangle in Fig. 2.5. The charging path P_{ch} is used to charge the boost inductor when the switch S is on. The discharging path P_{dis} is used to discharge the boost inductor and transfer the energy from the boost inductor to bulk capacitor or output when the switch S is off. The two paths are usually composed of diodes, capacitors, inductors, and extra windings of the transformer or their combinations.

In the implementation of the two-terminal ICS cell, the charging and discharging paths of

L_b are connected in parallel and inserted between the full-bridge rectifier D_r and the bulk capacitor C_b, as shown in Fig. 2.5(a). Notice that one winding coupled to the transformer of a DC-DC converter is contained in the charging path. The polarity arrangement of the additional winding intends the voltage across it being in opposition to the bulk capacitor voltage V_b during the duty-on time of switch S. Therefore, when the switch is on, the voltage across the winding can cancel the capacitor voltage V_b, so that the charging voltage of the boost inductor only includes the input voltage. The well-known magnetic-switch (MS) topology proposed in [20] is an example circuit, as shown in Fig. 2.6(a). In this converter, the charging and discharging paths use the same branch, namely, MS winding. Contrarily, in the example circuit shown in Fig. 2.6(b), the charging and discharging paths use the different branches [29].

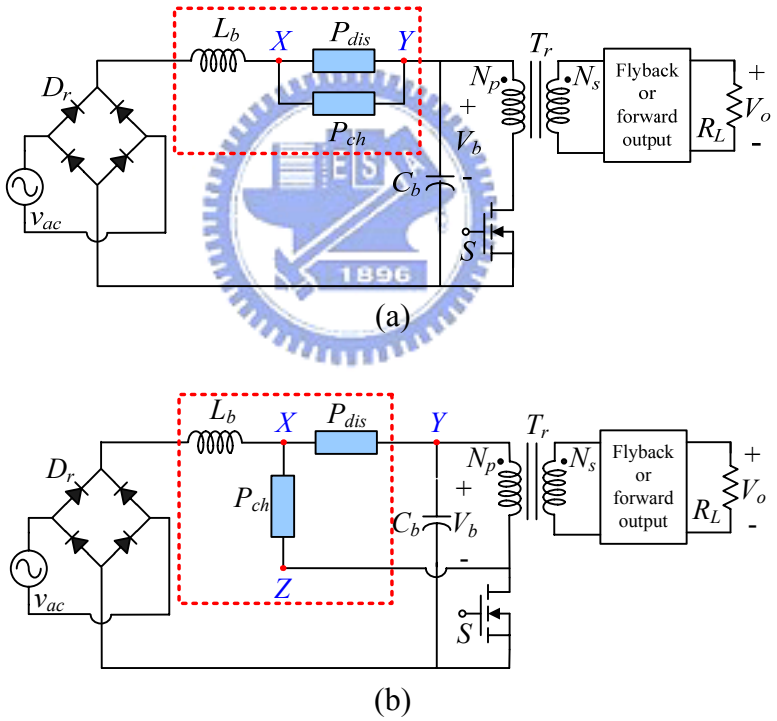
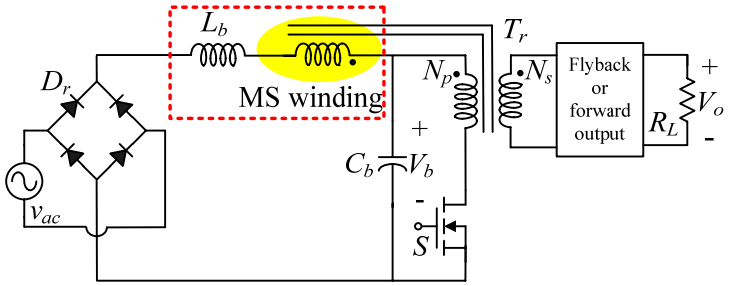
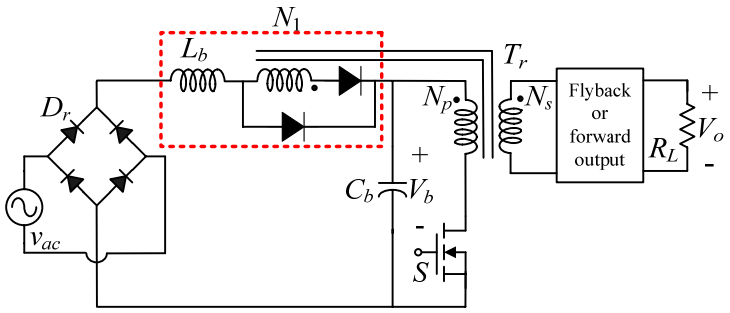


Fig. 2.5 Single-stage AC-DC converters with ICS cell of (a) two-terminal and (b) three-terminal.



(a)



(b)

Fig. 2.6 Example circuits of S^{2}ICS converter with two-terminal ICS cell: (a) the charging and discharging paths use the same branch [20] and (b) the charging and discharging paths use the different branches [29].

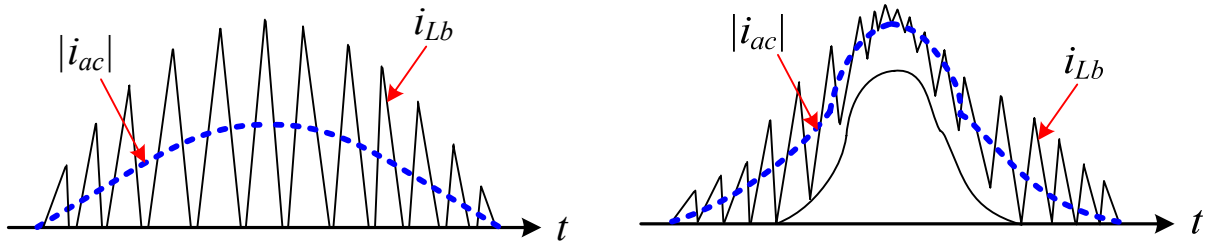
In the implementation of the three-terminal ICS cell, the boost inductor L_b is connected to the full-bridge rectifier D_r; the discharging path is connected to the bulk capacitor C_b; and the charging path is connected to switch S, as shown in Fig. 2.5(b). Therefore, the circuit configuration is named three-terminal. Similar to the two-terminal ICS cell, the boost inductor is charged by the input voltage when the switch is on, and discharged through the discharging path. The converter shown in Fig. 2.3(a) is an example circuit.

It is found that the two S^{2}ICS families are functionally equivalent and exhibit very similar performance although they are topologically different [16], [17]. For example, the converter shown in Fig. 2.6(b) is functionally equivalent to the one shown in Fig. 2.3(a) when the turns ratio of winding N_1 is the same as that of winding N_p.

2.1.3 S^{2}ICS Converters with DCM or CCM ICS Cells

In most of the existing S^{2}ICS converters, the ICS cells are operated in DCM to automatically achieve input PFC function. The mechanism is explained as follows. Since instantaneous AC input power always varies, a bulky capacitor is needed to buffer the instantaneous difference between the varying input power and a constant output power such that the output voltage is regulated tightly and free of line frequency ripple. Because the bulk capacitor is sufficiently large, the bulk capacitor voltage V_b can keep in the condition with small ripple. Thus, the switch duty cycle is almost constant during one line cycle in the steady-state, and the line current can automatically track the line voltage by operating the boost inductor in DCM, as shown in Fig. 2.7(a).

Although the concept of the basic DCM S^{2}ICS is very simple, it will introduce higher input inductor current ripple and more power loss due to the relatively high current stress. To reduce EMI filter size and improve conversion efficiency, several new CCM ICS techniques have been proposed in resent years [36]-[41]. Most of these methods are implemented by increasing the boost inductance or adding extra passive components to the DCM ICS cell. The corresponding input current waveforms are shown in Fig. 2.7(b). Although the line current generated by the CCM ICS cell is slightly deformed as compared to sinusoid, it has low harmonic components and can meet IEC 61000-3-2 Class D requirements.



(a) (b)

Fig. 2.7 Boost inductor current and its corresponding line current waveforms generated by (a) DCM ICS cell and (b) CCM ICS cell.

2.1.4 S^{2}ICS Converters with Current-Source or Voltage-Source ICS Cells

To achieve CCM boost inductor current, several CCM S^{2}ICS techniques have already been proposed in recent years [38]-[41]. Among them, there are two typical CCM S^{2}ICS techniques. Fig. 2.8 shows one type of CCM S^{2}ICS technique that incorporates an additional high-frequency inductor L_1. Fig. 2.9 shows another CCM S^{2}ICS technique with an additional high-frequency capacitor C_1. Since the inductor L_1 is comparable to a high-frequency current source, the circuits in Fig. 2.8 are named as current-source S^{2}ICS (CS-S^{2}ICS) converters. Similarly, since the capacitor C_1 is comparable to a high-frequency voltage source, the circuits in Fig. 2.9 are named as the voltage-source S^{2}ICS (VS-S^{2}ICS) converters. As shown in Figs. 2.8 and 2.9, each circuit utilizes an additional passive component, L_1 or C_1, on the original DCM S^{2}ICS to get continuous inductor current.

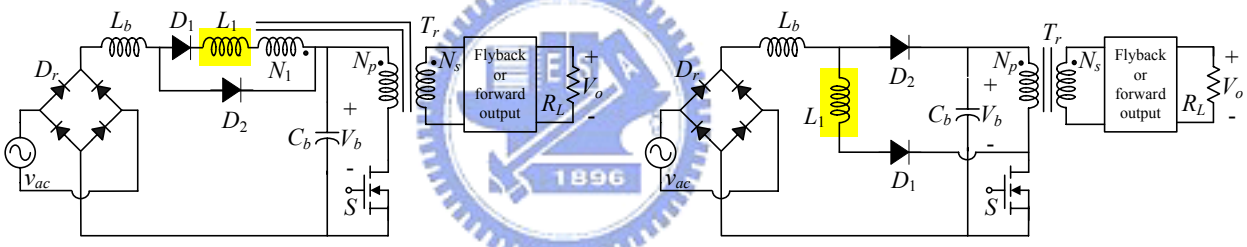


Fig. 2.8 Current-source S^{2}ICS Converters with ICS cell of (a) two-terminal and (b) three-terminal.

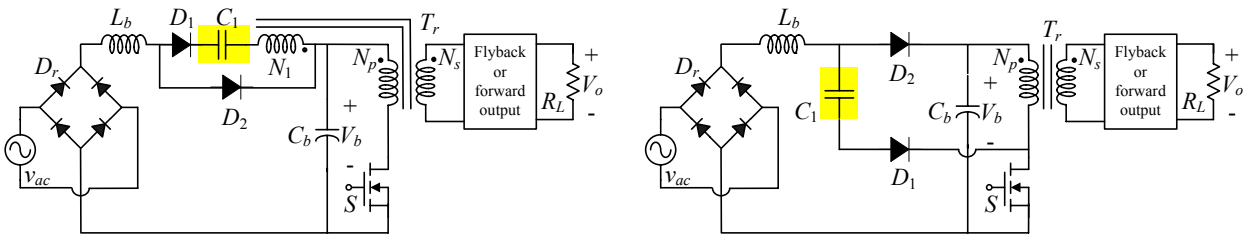


Fig. 2.9 Voltage-source S^{2}ICS Converters with ICS cell of (a) two-terminal and (b) three-terminal.

2.2 Main Issues of Single-Stage AC-DC Scheme

The underlining strategy of the single-stage AC-DC scheme is to design the converter that allows its PFC and DC-DC conversion circuits to share the same power switch with the same controller. From the above existing research efforts, we found that this kind of arrangement results in several main issues.

The first issue is the high current stress on the power switch since it handles current from both the AC mains and the bulk capacitor synchronously. Moreover, the ICS cell in a S^2ICS AC-DC converter normally operates in DCM to utilize its inherent current shaping capability; therefore, this issue becomes more deteriorated. Obviously, when compared with the conventional two-stage schemes, S^2ICS AC-DC converters have relatively high switch current stress. High current stress not only causes low conversion efficiency and high temperature rise, but also brings about annoying EMI issues.

The second issue is that the bulk capacitor voltage stress is critical since it is no longer regulated and increases while the input line voltage increases or load current decreases. This is because only a single control loop for the output voltage regulation, and the bulk capacitor voltage is determined by the input to output average power balance [33]. The high bulk capacitor voltage stress generally exists for most of S^2ICS converters, and this issue is more severe under high line and light load condition [49]. Thus, it is difficult to use S^2ICS converters for the applications that require a universal input voltage of 90–260 Vrms. Moreover, a high bulk capacitor voltage means high component rating, high cost and low conversion efficiency. For the commercial consideration, the maximum bulk capacitor voltage must be held below 450 V, so that a commercially available 450 V-rated electrolytic capacitor can be used safely.

2.3 Several Familiar Schemes to Alleviate Bulk Capacitor Voltage Stress

Many off-line power supplies must be able to have a universal-line input, which means

the power converter may be operated with the international utility voltage. For example, in the United States, the single-phase input voltage is in the 90–135 Vrms range, while the input voltage is in the 180–260 Vrms range in Europe. A wide line voltage range may pose an enormous challenge to designing S^2ICS converters, especially in alleviating bulk capacitor voltage stress. To suppress high bulk capacitor voltage stress, numerous methods have been presented [50]. In this section, four representative schemes to suppress bus capacitor voltage stress are analyzed and discussed. Through understanding the approaches of alleviating bus capacitor voltage stress, it is helpful to derive and develop new topologies of S^2ICS converters.

2.3.1 Variable-Frequency Control

The variable-frequency control was proposed in [49]. Since the voltage gain of the CCM DC-DC cell depends only on the duty ratio, and the voltage gain of the DCM boost-type ICS cell depends on the switching frequency rather than the duty ratio, it is possible to regulate the bulk capacitor voltage by a variable-frequency control. Clearly speaking, for the ICS cell operating in DCM with a constant duty ratio, the average input power is inversely proportional to the switching frequency, and the unbalanced power between the input and output decreases with the increase of switching frequency. The drawback of this approach is that large load variation range results in large range of variation in switching frequency. For a load change from 10% to full load, the switching frequency has to be 10 times that of the full load to remain the same bulk capacitor voltage. Such wide switching frequency variation has problems such as low conversion efficiency and difficulty in the optimal design of transformers and inductors.

2.3.2 Bulk Capacitor Voltage Feedback Concept

Fig 2.10 shows the modified BIFRED (Boost Integrated with Flyback Rectifier/Energy Storage/DC-DC converter) converter with the bulk capacitor voltage feedback [33]. In the modified scheme, an additional transformer winding N_1 is inserted in series with the boost inductor. The winding can feedback the bulk capacitor voltage when the boost inductor is charged, and the feedback depth depends on the bulk capacitor voltage level. The feedback depth will increase when the bulk capacitor voltage has an increasing trend. Thus, the input power can be automatically reduced to guarantee the balance between input and output average power. As a result, the bulk capacitor voltage is limited within a proper range.

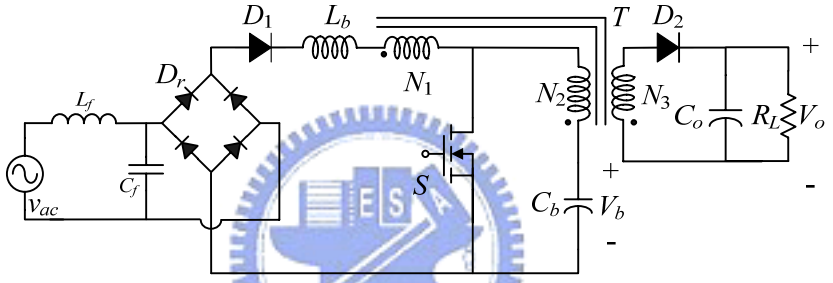


Fig. 2.10 BIFRED converter with bulk capacitor voltage feedback [33].

2.3.3 Parallel Power Processing

To reduce extra bulk capacitor voltage stress and extra switch current stress, a parallel power factor correction (PPFC) approach has been proposed [22]-[28]. The main advantage of this type of design is the clamped or slightly boosted bulk capacitor voltage since partial input power is processed only once and directly delivered to the output load rather than stored in C_b. The configuration shown in Fig. 2.11 is an example circuit [24], in which the additional flyback transformer T_{r1} is used to replace most functions of the boost inductor in a conventional S^2ICS AC-DC scheme and provide a path for direct power transfer. This scheme can be applicable to converters with wide input voltage and load ranges. However, the two transformers (T_{r1} and T_{r2}) with similar size and complex circuit structure make this topology less attractive

in low power applications, for which cost and size are often the dominant concerns.

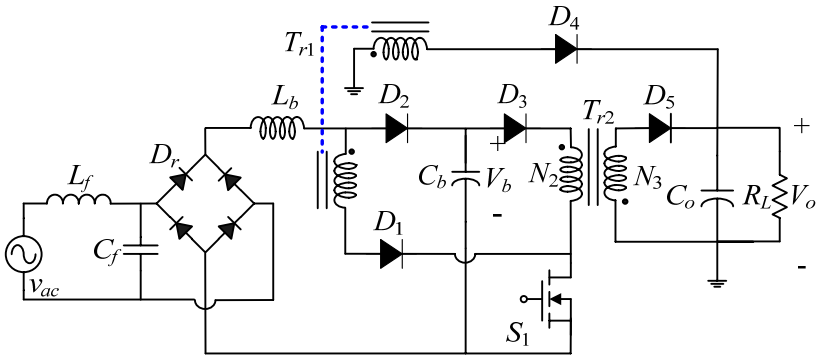


Fig. 2.11 Example circuit with parallel power processing [24].

2.3.4 Both Functional Blocks Operate in the Same Mode

As discussed in subsection 1.1.2, power imbalance between the input and the output in the operation combination of DCM ICS + CCM DC-DC will cause high voltage stress on the intermediate bulk capacitor. However, there is no high bulk capacitor voltage stress problem in the combinations with the same operating mode, either in DCM or in CCM for the two cells [33]. Taking the example of DCM ICS + DCM DC-DC, the duty ratio will automatically decrease while the load becomes light, as shown in Fig. 2.12. As a result, the average input power also decreases due to the decrease of duty ratio. The excess input energy reduces accordingly and the bulk capacitor voltage can be suppressed [51].

The technique of operating both functional blocks in the same mode is a practical and useful solution. However, the combination of DCM ICS + DCM DC-DC causes a low efficiency because of higher conduction loss and turn-off switching loss; the combination of CCM ICS + CCM DC-DC has relatively lower PF and higher distortion in input current as well as the larger boost inductor.

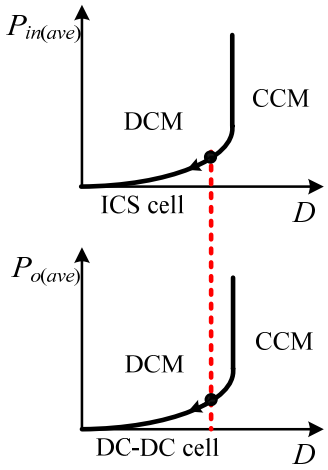


Fig. 2.12 Relationship between the average input power, average output power, and duty ratio for DCM ICS + DCM DC-DC [33].

2.4 Trend and Challenges

For AC-DC conversion, although unity PF is the ideal objective, it is not necessary to meet today's regulations with unity PF. For example, both IEC 555 and IEC 61000-3-2 allow the presence of harmonics in the line current [1]-[4]. This fact opens the door for the compromise techniques between quality and cost, which are capable of overcoming the above issues. Thus, to sum up briefly, the design optimization of a S^2ICS circuit needs to meet the following objectives:

(1) The input current harmonics must meet the IEC 61000-3-2 Class D specifications;

(2) The S^2ICS converter should have low bulk capacitor voltage stress in order to minimize the component ratings;

(3) The circuit structure should be simple to maintain lower cost for this converter than it is with the two-stage approach;

(4) The converter should have low switch current stress and good efficiency as well as keep V_b below 450 V in a wide line voltage range.

In summary, the major challenges of the S^2ICS research includes meeting current har-

monic specifications, limiting bulk capacitor voltage stress, reducing switch current stress, dealing with the universal-line input voltage range, all with minimum additional cost. How to understand, analyze, optimize and improve these S^2ICS converters has been a very interesting topic in recent power electronics research.

2.5 Concluding Remarks

A review of existing S^2ICS AC-DC converters is given in this chapter. For further comparing the system configuration and characteristics of the familiar S^2ICS converters, we summarize the classification of the representative reported single-stage circuits as shown in Table 2.1.

In addition, main issues such as high current stress, high voltage stress and low conversion efficiency in current S^2ICS AC-DC approaches are also presented and discussed in this chapter. To alleviate switch current stress, a new ICS technique is presented in Chapter 3. The proposed ICS scheme not only alleviates switch current stress in the duty-on time, but also provides a well current shaping function. Moreover, to suppress bulk capacitor voltage stress, a hybrid operated DC-DC converter is adopted in Chapter 4. This circuit can simultaneously achieve two functions including bulk capacitor voltage suppression while light load and high conversion efficiency while heavy load.

Table 2.1 Classification of the representative reported S^2ICS converters

Basis of classification	Category	Representative Circuits
Power processing structure	Cascade	[15], [31], [32]
	Parallel	[22]-[28]
Topology configuration of ICS cell	2-terminal	[20], [29], [30]
	3-terminal	[21], [23]-[28], [31]-[41]
Input boost inductor current waveform	DCM	[15], [21]-[23], [25]-[35], [51]
	CCM	[24], [36]-[41]
Topology configuration of ICS cell	CS-S^2ICS	[36]-[39]
	VS-S^2ICS	[40], [41]

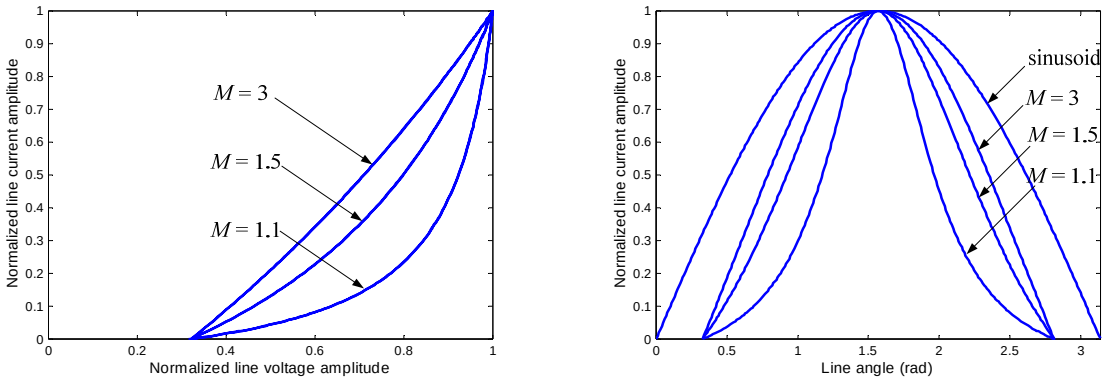
CHAPTER 3

ANALYSIS OF THE PROPOSED ICS TECHNIQUE AND THE APPLICAION TO FLYBACK CONVERTERS

For the single-stage designs with boost-type ICS cells, the line current actually being the average (or filtered) boost inductor current is composed of two components. The average charging current of the boost inductor has linear relation to the instantaneous line voltage, while the average discharging current of the boost inductor primarily has a quadratic characteristic against the instantaneous line voltage. Thus, the resultant input i-v characteristic curves are nonlinear as shown in Fig. 3.1(a) and the corresponding line currents have the deformed shapes as shown in Fig. 3.1(b), where M represents the ratio of the bulk capacitor voltage V_b to the peak line voltage $V_{ac(pk)}$. To improve this drawback, it is found that V_b should be designed to be as high as possible [11]. However, this will produce high voltage stress on the switch and the bulk capacitor. To remedy the problems described above, the charging time of the boost inductor in the proposed converter is designed to be inversely modulated by the line voltage, so that the i-v curve of the average charging current presents an opposite deformation characteristic to that presented by the i-v curve of the average discharging current. Consequently, the line current has the waveform analogous to the line voltage waveform.

In addition, since the ICS cell and DC-DC cell are driven by one common switch, both the boost inductor current and the transformer current simultaneously flow through the switch in the duty-on time, as shown in Fig. 3.2(b). As a result, the switch current stress is relatively high when compared with the conventional two-stage scheme. High current stress not only accompanies with increased power loss, but also brings about annoying EMI issues. To overcome this drawback, we adopt the concept of “interleaved operation” in the design of sin-

gle-stage AC-DC converters. Unlike the conventional single-stage designs, the proposed ICS scheme is intentionally arranged to be charged in the duty-off time, as shown in Fig. 3.2(c). With this design, the switch current stress in the duty-on time can be significantly reduced and correspondingly conduction loss can be relieved. This special ICS function can be implemented by using the technique of multi-winding of power transformer.



(a) (b)

Fig. 3.1 The line current distortion caused by the modulation effect of the boost inductor discharging time, where $M = V_b/V_{ac(pk)}$ and the dead angle of the line current is considered: (a) the input i-v characteristic curves and (b) the corresponding line current waveforms.

On the other hand, the common drawback of using the single-stage circuits is that the switching components often suffer from the relatively high voltage and current stress during switching, which increases the component rating and introduces more switching loss too. To further improve the performance of the proposed single-stage AC-DC converter, an active-clamp circuit with zero-voltage-switching (ZVS) function is added to the adopted converter. This circuit can lead to noticeable improvement on voltage spikes across the switches and significant reduction of electromagnetic noise generation [42]-[48].

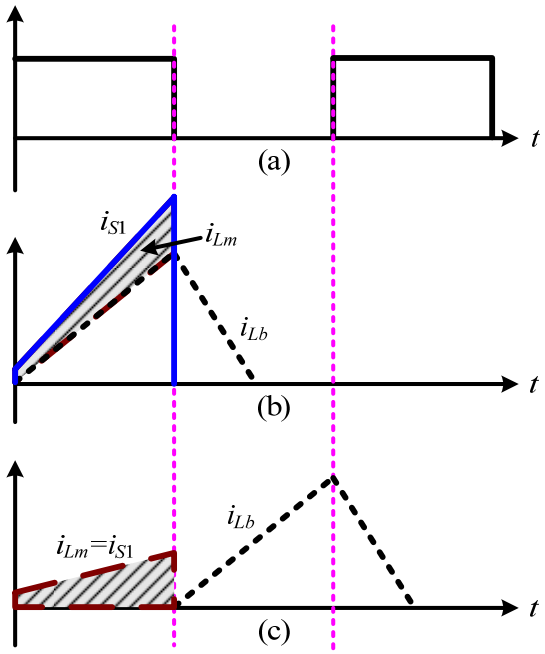


Fig. 3.2 Comparison of switch current stress: (a) PWM control signal of the switch, (b) switching current waveforms of the conventional ICS scheme and (c) switching current waveforms of the proposed ICS scheme.

3.1 Analysis of the Proposed Converter

3.1.1 Circuit Derivation and Configuration

Fig. 3.3 shows the circuit configuration of the proposed single-stage AC-DC converter. The proposed converter is based on a conventional active-clamp DC-DC converter with skilled modification in order to satisfy harmonic regulations and cost-effective consideration. In this converter, a multi-winding transformer T_r is employed. It includes three windings N_1, N_2, and N_3 with turns number n_1, n_2, and n_3, respectively, and the primary magnetizing inductance L_m. As shown in Fig. 3.3, the converter contains an ICS cell, mainly composed of the rectifier diode D_1, boost inductor L_b, winding N_1, and resonant inductor L_r. The diode D_1 is used to provide fast rectification and prevent the filter capacitor C_{in} from being charged by the reverse current of i_{Lb}. It is worth mentioning that the proposed converter has a special ICS de-

sign in which the undotted end of winding N_1 is intentionally connected to node X instead of node Y. There are two objectives for this design: charging the boost inductor in the duty-off time and reducing the size of the boost inductor. Through the winding N_1 with enough large turns, the voltage v_{N1} can force to charge L_b during the duty-off time since v_{N1} turns to negative. Therefore, only the transformer current flows through the main switch S_1 in the duty-on time and correspondingly the switch current stress can be reduced. Meanwhile, the resonant inductor L_r is arranged in the charging path of L_b so that L_r and L_b can provide the voltage-boost function together. Consequently, a small inductance for L_b is sufficient to achieve the DCM operation and it can be implemented by either an external inductor or leakage inductance of the transformer.

The ICS cell is then followed by an active-clamp DC-DC circuit which provides isolation and post-regulation function, as defined by the dotted-line box in Fig. 3.3. The DC-DC cell is designed to operate in CCM and can be implemented by a flyback or forward circuit. C_r represents the sum of the parasitic capacitances of main switch S_1 and auxiliary switch S_2. L_r represents an external inductor, which forms a series resonant circuit with C_r to enable soft-switching function. The resonant inductor L_r, the clamping capacitor C_c, and the auxiliary switch S_2 form the main part of the active-clamp circuit for limiting the turn-off voltage spike of S_1.

The control circuit can be implemented by a simple control loop, a common PWM controller, and a driver circuit. Moreover, main and auxiliary switches are driven complementary with small dead time in between to allow for ZVS.

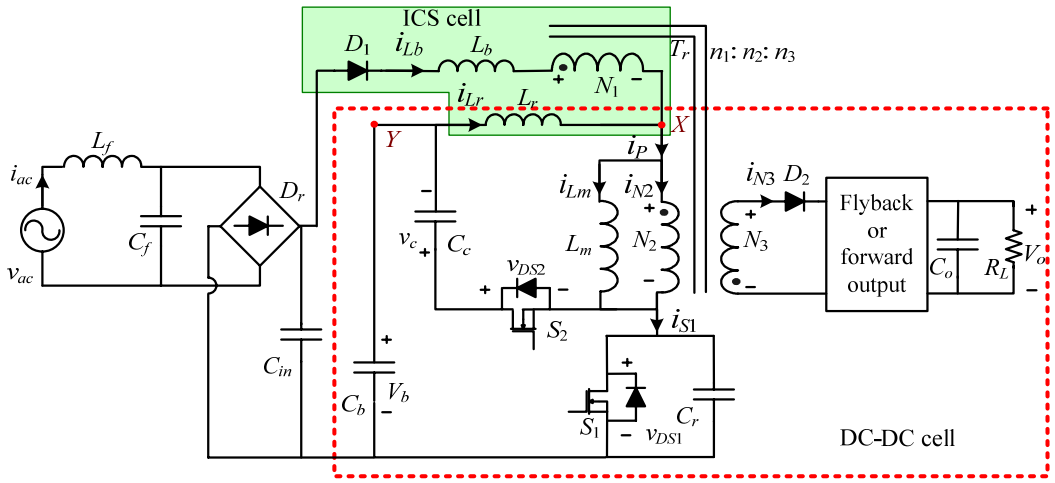


Fig. 3.3 Proposed single-stage soft-switching AC-DC converter.

3.1.2 Principle of Operation

In this subsection, the detailed operation of a flyback-type implementation with the proposed ICS scheme is introduced. To simplify the analysis, the following assumptions are made:

(i) The switching and conduction losses of the components are neglected;

(ii) The rectified line voltage $|v_{ac}|$ is considered constant during a switching period;

(iii) The bulk capacitor voltage V_b and the output capacitor voltage V_o are ripple-free DC in each half of a line cycle;

(iv) The leakage inductances of the transformer are neglected;

(v) An external inductor is employed for L_b.

According to the instantaneous magnitude of the rectified line voltage $|v_{ac}|$, the operation of the converter can be divided into two modes during a half line cycle, as shown in Fig. 3.4. When $|v_{ac}|$ is smaller than the boundary voltage V_{BD}, the converter operates in mode M_1, and during the remaining time it operates in mode M_2. Fig. 3.5 illustrates that five topological states exist in a switching period. Referring to the symbol definitions, topological states, and key waveforms shown in Figs. 3.3, 3.5, and 3.6, respectively, the detailed operation is ex-

plained as follows.

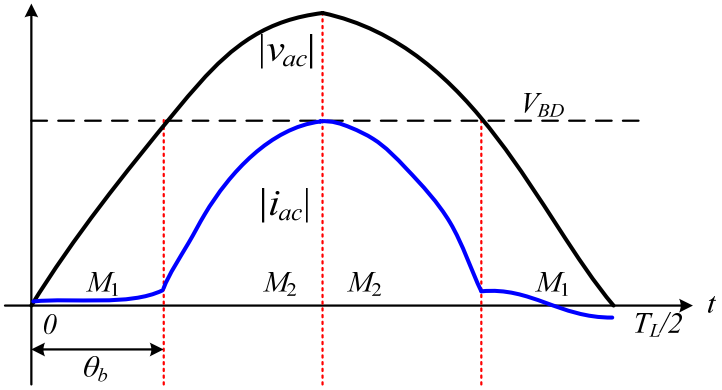


Fig. 3.4 Operation modes in a half line cycle.

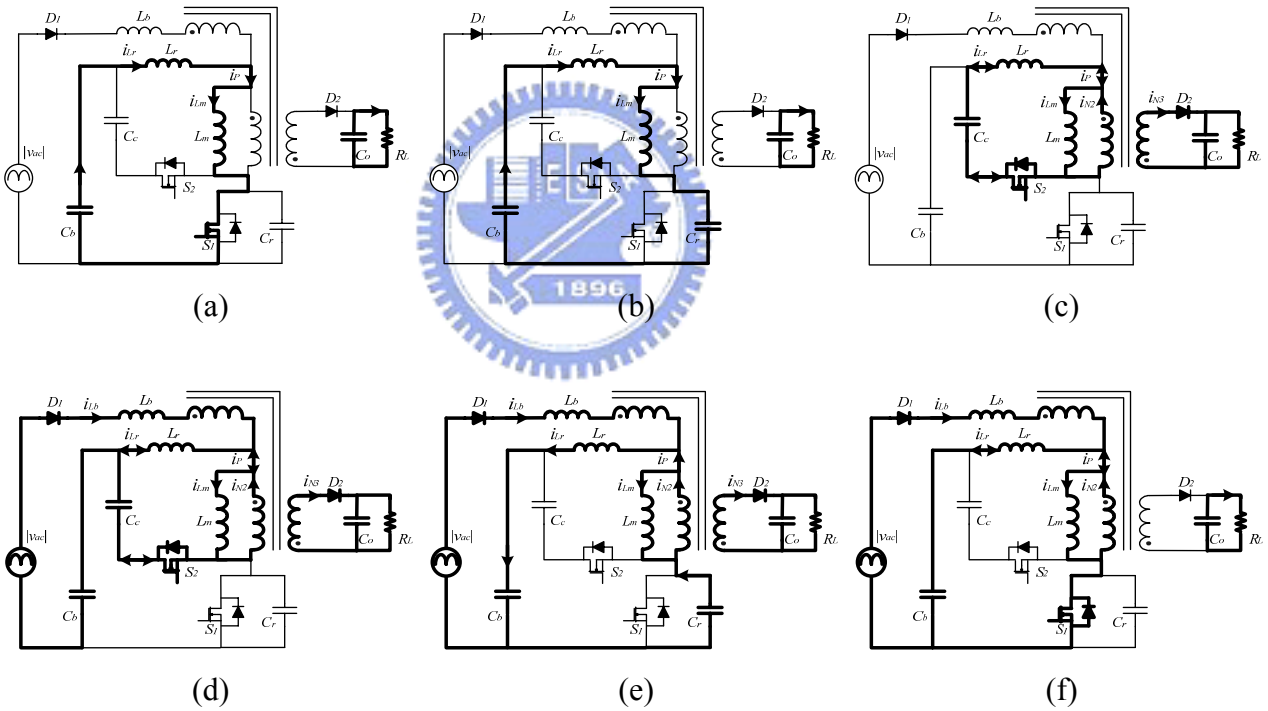


Fig. 3.5 Topological states of the proposed converter based on flyback topology: (a) State 1, (b) State 2, (c) State 3 for mode M_1, (d) State 3 for mode M_2, (e) State 4, and (f) State 5.

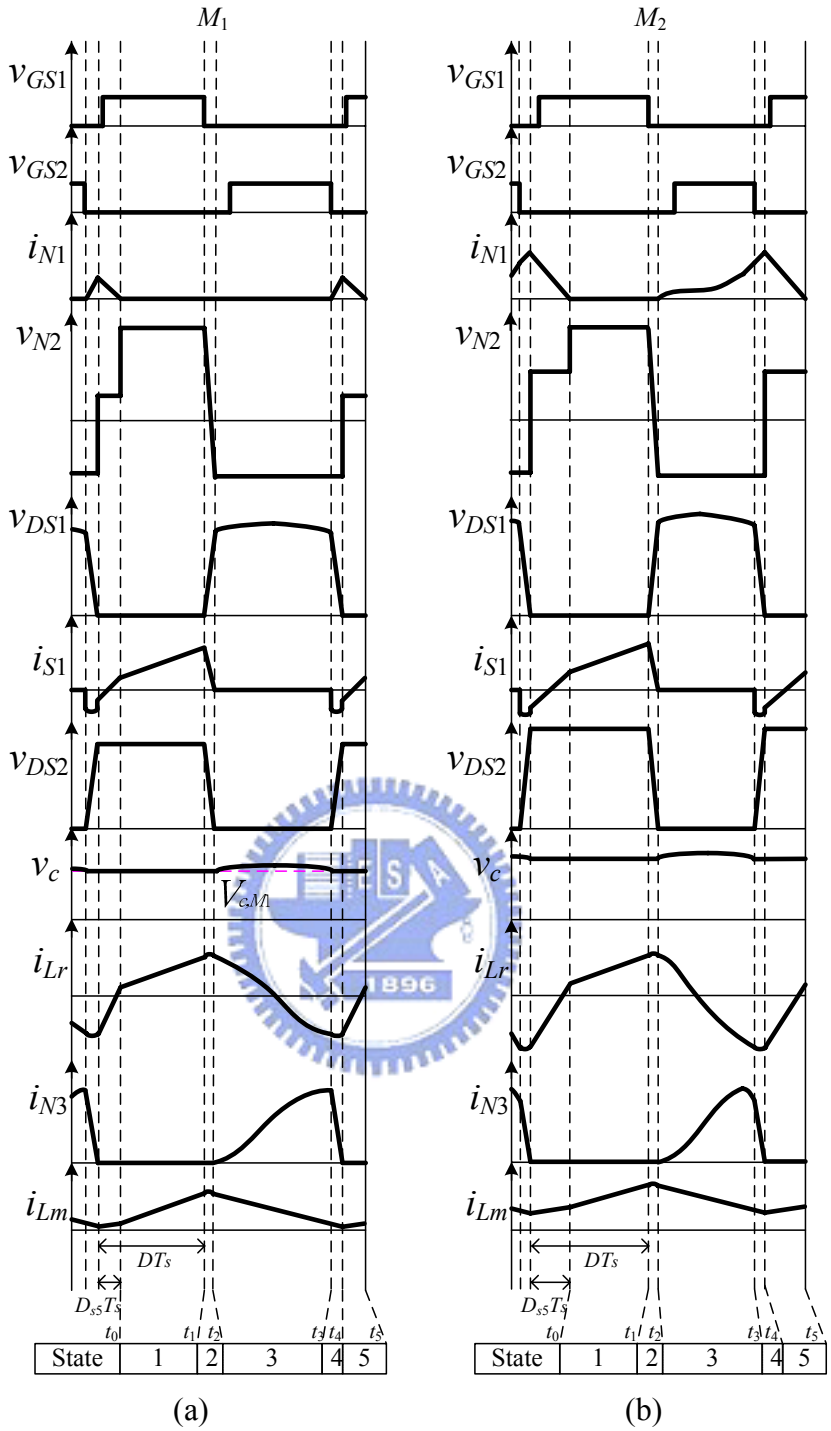


Fig. 3.6 Steady-state waveforms of the proposed converter in (a) mode M_1 and (b) mode M_2.

State 1 [Fig. 3.5(a), $t_0 \le t < t_1$]:

At t_0, S_1 is on and S_2 is off. The output rectifier D_2 is reverse biased. Both L_m and L_r are linearly magnetized as operating in a conventional flyback converter. This current flowing through L_r and L_m, i_p, can be written as:

$$i_P(t) = i_{Lr}(t) = i_{Lm}(t) = i_{Lr}(t_0) + \frac{V_b}{L_r + L_m} \cdot (t - t_0). \tag{3.1}$$

Thus, $i_p(t_1)$ can be obtained by

$$i_P(t_1) = i_{Lr}(t_0) + \frac{V_b}{L_r + L_m} \cdot (D - D_{s5})T_s. \tag{3.2}$$

where D is the duty ratio, $D_{s5}T_s = (t_5 – t_4)$, and T_s is the switching period. In this duration, the current flowing through L_b is zero.

State 2 [Fig. 3.5(b), $t_1 \le t < t_2$]:

At t_1, S_1 is turned off. C_r is rapidly charged by the magnetizing current i_{Lm} in this duration; thus, v_{DS1} rises linearly to reach $V_b + v_c(t_2)$ in a short time and is given by

$$v_{DS1}(t) = \frac{i_P(t_1)}{C_r} \cdot (t - t_1). \tag{3.3}$$

State 3 [Fig. 3.5(c) or 3.5(d), $t_2 \le t < t_3$]:

At t_2, v_{DS1} rises to the value that makes the body diode of S_2 start to conduct. In this duration, the transformer secondary voltage v_{N3} is sufficient to forward bias D_2. Therefore, the transformer primary voltage v_{N2} is clamped at $-V_o \cdot n_2/n_3$. Shortly, S_2 is turned on before i_p resonates to the negative direction; thus, ZVS of S_2 is achieved. In mode M_1, the line voltage is not large enough to generate i_{Lb}; thus, the resonant tank only includes L_r and C_c when neglecting the small C_r. The voltage and current along the resonant loop can be obtained by

$$i_P(t) = i_{Lr}(t) = A_1 \cdot \cos(\omega_1(t - t_2)) + B_1 \cdot \sin(\omega_1(t - t_2)) \tag{3.4}$$

and

$$v_c(t) = \frac{n_2}{n_3} V_o + A_1 Z_1 \cdot \sin(\omega_1(t - t_2)) - B_1 Z_1 \cdot \cos(\omega_1(t - t_2)) \tag{3.5}$$

where

$$A_1 = i_P(t_1), \quad B_1 = \frac{\frac{n_2}{n_3} V_o - v_c(t_2)}{Z_1}, \quad \omega_1 = \frac{1}{\sqrt{L_r C_c}}, \text{ and } \quad Z_1 = \sqrt{\frac{L_r}{C_c}}.$$

More concisely,

$$i_P(t) = C_1 \cdot \cos(\omega_1(t - t_2) - \varphi_1) \tag{3.6}$$

and

$$v_c(t) = \frac{n_2}{n_3} V_o + Z_1 C_1 \cdot \sin(\omega_1 (t - t_2) - \varphi_1) \tag{3.7}$$

where

$C_1 = \sqrt{A_1^2 + B_1^2}$ and the phase angle $\varphi_1 = \tan^{-1}\left(\frac{B_1}{A_1}\right) = \tan^{-1}\left(\frac{\frac{n_2}{n_3} V_o - v_c(t_2)}{Z_1 i_P(t_1)}\right)$.

During this state, the voltage across the primary winding N_2 is clamped at $-V_o \cdot n_2 / n_3$ by the secondary winding N_3, so the magnetizing current i_{Lm} decreases linearly as given by

$$i_{Lm}(t) = i_P(t_1) - \frac{V_o}{L_m} \cdot \frac{n_2}{n_3} \cdot (t - t_2). \tag{3.8}$$

And by employing Ampere's law, we can obtain that

$$n_1 \cdot i_{Lb} + n_2 \cdot i_{N2} + n_3 \cdot i_{N3} = 0. \tag{3.9}$$

Moreover, according to Fig. 3.3, the primary winding current i_{N2} can be obtained by

$$i_{N2}(t) = i_P(t) - i_{Lm}(t). \tag{3.10}$$

Employing (3.9), one can find the secondary winding current in mode M_1:

$$i_{N3}(t) = -\frac{n_2}{n_3} \cdot i_{N2}(t). \tag{3.11}$$

In mode M_2, the line voltage is higher than the boundary voltage V_{BD} and causes the current i_{Lb} to be generated. Therefore, the resonant tank is formed by L_r, L_b, and C_c. In such a design, the negative v_{N1} results in a partial energy of L_m being sent back to C_b through winding N_1. According to the topological state shown in Fig. 3.5(d), we obtain

$$i_P(t) = A_2 \cdot \cos(\omega_r (t - t_2)) + B_2 \cdot \sin(\omega_r (t - t_2)) = C_2 \cdot \cos(\omega_r (t - t_2) - \varphi_2) \tag{3.12}$$

and

$$\begin{aligned} v_c(t) &= \frac{n_2}{n_3} V_o + \frac{L_r\left(|v_{ac}(t)| + \frac{n_1}{n_3} V_o - V_b\right) - L_r L_b\left[-A_2 \omega_2 \cdot \sin(\omega_2 (t - t_2)) + B_2 \omega_2 \cdot \cos(\omega_2 (t - t_2))\right]}{L_r + L_b} \\ &= \frac{n_2}{n_3} V_o + \frac{L_r}{L_r + L_b}\left(|v_{ac}(t)| + \frac{n_1}{n_3} V_o - V_b\right) + Z_2 C_2 \cdot \sin(\omega_2 (t - t_2) - \varphi_2) \end{aligned}$$

(3.13)

where

$$A_2 = i_P(t_1),\ B_2 = \frac{L_b \frac{n_2}{n_3} V_o + L_r\left(|v_{ac}(t)| + \frac{n_1+n_2}{n_3} V_o - V_b\right)}{L_r L_b \omega_2} - \frac{v_c(t_2)}{Z_2},\ \ C_2 = \sqrt{A_2{}^2 + B_2{}^2},$$

$$\omega_2 = \sqrt{\frac{L_r + L_b}{L_r L_b C_c}},\ \ Z_2 = \sqrt{\frac{L_r L_b}{(L_r + L_b) C_c}}, \text{ and}$$

$$\varphi_2 = \tan^{-1}\left(\frac{B_2}{A_2}\right) = \tan^{-1}\left(\frac{L_b \frac{n_2}{n_3} V_o + L_r\left(|v_{ac}(t)| + \frac{n_1+n_2}{n_3} V_o - V_b\right)}{L_r L_b \omega_2 i_P(t_1)} - \frac{v_c(t_2)}{Z_2 i_P(t_1)}\right).$$

The detailed derivation of the above equations is shown in Appendix A. So far, by applying the operating principle obtained in State 3, the average charging current of the boost inductor in one switching period can be calculated. First, the boost inductor current i_{Lb} can be expressed as

$$i_{Lb}(t) = \frac{1}{L_r + L_b}\left[\left(|v_{ac}(t)| + \frac{n_1}{n_3} V_o - V_b\right)\cdot(t - t_2) + L_r\left(i_P(t) - A_2\right)\right] \tag{3.14}$$

where A_2, equivalent to $i_p(t_1)$, can also be expressed as follows:

$$A_2 = \left[\frac{n_1}{L_r + L_b}\left(|v_{ac}(t)| + \frac{n_1}{n_3} V_o - V_b\right)\frac{(1-D)T_s}{2} + \frac{n_2^2}{n_3}\frac{V_o}{L_m}\frac{(1-D)T_s}{2} + \frac{P_o}{V_o}\frac{n_3}{(1-D)}\right] \Big/ \left(n_2 + \frac{n_1 L_r}{L_r + L_b}\right) \tag{3.15}$$

where P_o is the output power. The detailed derivation of (3.15) is shown in Appendix B. By integrating (3.14) through the duty-off time and then dividing (3.14) by T_s, the average charging current of the boost inductor over one switching period is given by

$$i_{Lb,ch(ave)}(t) = \frac{1}{L_r + L_b}\left[\left(|v_{ac}(t)| + \frac{n_1}{n_3} V_o - V_b\right)\frac{(1-D)^2 T_s}{2} - L_r A_2 (1-D)\right]. \tag{3.16}$$

Additionally, i_{Lm} and i_{N2} are still ruled by (3.8) and (3.10) and i_{N3} can be calculated by em-

ploying (3.9):

$$i_{N3}(t) = -\frac{n_1 i_{Lb}(t) + n_2 i_{N2}(t)}{n_3}. \tag{3.17}$$

Employing KCL, the current i_{Lr} can be obtained as

$$i_{Lr}(t) = i_P(t) - i_{Lb}(t) = \frac{1}{L_r + L_b}\left[-\left(|v_{ac}| + \frac{n_1}{n_3}\cdot V_o - V_b\right)\cdot(t - t_2) + L_b i_P(t) + L_r A_2\right]. \tag{3.18}$$

Note that the interval between t_2 and t_3 is approximated to $(1–D)T_s$, since the two neighboring oscillation intervals of States 2 and 4 are very short as compared to the switching period.

State 4 [Fig. 3.5(e), $t_3 \le t < t_4$]:

At t_3, S_2 is turned off. C_c is disconnected and L_r, L_b, and C_r form a new high frequency resonant circuit. The transformer primary side current i_p resonates in the negative direction to discharge C_r; therefore, v_{DS1} decreases from $v_c(t_3)+V_b$ to zero. Within this state, v_{N2} turns to positive and results in D_2 being cut off. Since the down-slope of di_{N3}/dt is determined by the resonant speed, D_2 can be designed to switch softly to reduce the rectifier switching loss. Based on the operations shown in Fig. 3.5(e), we can obtain

$$i_P(t) = A_3\cdot\cos(\omega_3(t - t_3)) + B_3\cdot\sin(\omega_3(t - t_3)) = C_3\cdot\cos(\omega_3(t - t_3) - \varphi_3) \tag{3.19}$$

and

$$\begin{aligned} v_{Cr}(t) &= \frac{n_2}{n_3}\cdot V_o + \frac{L_b V_b + L_r\cdot\left(|v_{ac}(t)| + \frac{n_1}{n_3}\cdot V_o\right) - L_r L_b\omega_3\cdot\left(-A_3\cdot\sin(\omega_3(t - t_3)) + B_3\cdot\cos(\omega_3(t - t_3))\right)}{L_r + L_b} \\ &= \frac{n_2}{n_3}\cdot V_o + \frac{L_b V_b + L_r\cdot\left(|v_{ac}(t)| + \frac{n_1}{n_3}\cdot V_o\right)}{L_r + L_b} + Z_3 C_3\cdot\sin(\omega_3(t - t_3) - \varphi_3) \end{aligned} \tag{3.20}$$

where

$$A_3 = i_P(t_3),\quad B_3 = \frac{L_b V_b + L_r\cdot\left(|v_{ac}(t)| + \frac{n_1}{n_3}\cdot V_o\right)}{L_r L_b\omega_3} - \frac{\left(v_{Cr}(t_3) - \frac{n_2}{n_3}\cdot V_o\right)}{Z_3},\quad C_3 = \sqrt{A_3^{\,2} + B_3^{\,2}},$$

$$\omega_3 = \sqrt{\frac{L_r + L_b}{L_r L_b \cdot C_r}}, \quad Z_3 = \sqrt{\frac{L_r L_b}{(L_r + L_b) C_r}}, \text{ and}$$

$$\varphi_3 = \tan^{-1}\left(\frac{B_3}{A_3}\right) = \tan^{-1}\left(\frac{L_b V_b + L_r \cdot \left(|v_{ac}| + \frac{n_1}{n_3} \cdot V_o\right)}{L_r L_b \omega_3 i_P(t_3)} - \frac{v_{Cr}(t_3) - \frac{n_2}{n_3} \cdot V_o}{Z_3 i_P(t_3)}\right).$$

And the details of the above equations are shown in Appendix C. In this duration, i_{N2} and i_{N3} have the same expressions as (3.10) and (3.17), respectively. Besides, i_{Lm} is given by

$$i_{Lm}(t) = i_P(t_3) - \frac{V_o}{L_m} \cdot \frac{n_2}{n_3} \cdot (t - t_3). \tag{3.21}$$

Integrating the voltage across L_r yields

$$\begin{cases} i_{Lr}(t) = \dfrac{1}{L_r + L_b}\left[-\left(|v_{ac}(t)| + \dfrac{n_1}{n_3} \cdot V_o - V_b\right) \cdot (t - t_3) + L_b i_P(t) + L_r A_3\right] & \text{for } M_1 \\ i_{Lr}(t) = -i_{Lb}(t_3) + \dfrac{1}{L_r + L_b}\left[-\left(|v_{ac}(t)| + \dfrac{n_1}{n_3} \cdot V_o - V_b\right) \cdot (t - t_3) + L_b i_P(t) + L_r A_3\right] & \text{for } M_2 \end{cases} \tag{3.22}$$

Subtracting (3.22) from i_p yields

$$\begin{cases} i_{Lb}(t) = \dfrac{1}{L_r + L_b}\left[\left(|v_{ac}(t)| + \dfrac{n_1}{n_3} \cdot V_o - V_b\right) \cdot (t - t_3) + L_r \cdot (i_P(t) - A_3)\right] & \text{for } M_1 \\ i_{Lb}(t) = i_{Lb}(t_3) + \dfrac{1}{L_r + L_b}\left[\left(|v_{ac}(t)| + \dfrac{n_1}{n_3} \cdot V_o - V_b\right) \cdot (t - t_3) + L_r \cdot (i_P(t) - A_3)\right] & \text{for } M_2 \end{cases} \tag{3.23}$$

It should be noted that, for mode M_1, the current i_{Lb} is built up only in this short interval. Thus, the induced input current is much smaller than that induced in mode M_2.

State 5 [Fig. 3.5(f), $t_4 \le t < t_5$]:

At t_4, the body diode of S_1 begins to conduct. Shortly after time t_4, while the body diode of S_1 is conducting, S_1 is turned on to achieve ZVS operation. The bulk capacitor voltage V_b, much higher than v_{N2}, causes i_{Lr} to increase linearly. Simultaneously, since $|v_{ac}|$ is smaller than $v_{N1}+v_{N2}$, the boost inductor current i_{Lb} linearly decreases and becomes zero at time t_5 (= t_0). The above operation gives

$$i_{Lb}(t) = i_{Lb}(t_4) + \frac{|v_{ac}(t)| - v_{N1}(t) - v_{N2}(t)}{L_b} \cdot (t - t_4) \tag{3.24}$$

where

$$v_{N2}(t) = \frac{L_b V_b + \frac{n_1 + n_2}{n_2} L_r |v_{ac}(t)|}{\frac{L_r + L_m}{L_m} L_b + \left(\frac{n_1 + n_2}{n_2}\right)^2 L_r} \tag{3.25}$$

$$v_{N1}(t) = (n_1 / n_2) \cdot v_{N2}(t). \tag{3.26}$$

The derivation of (3.25) is shown in Appendix D. It is worth mentioning that the output power is fed directly from the line input by the utilization of winding N_1 in this state. By integrating (3.24) through the $D_{s5}T_s$ interval and then dividing (3.24) by T_s, the average discharging current of the boost inductor over one switching period is given by

$$i_{Lb,dis(ave)}(t) = \frac{D_{s5}^2 T_s}{2} \cdot \frac{\frac{n_1 + n_2}{n_2} V_b - \frac{L_r + L_m}{L_m} |v_{ac}(t)|}{\frac{L_r + L_m}{L_m} L_b + \left(\frac{n_1 + n_2}{n_2}\right)^2 L_r}. \tag{3.27}$$

3.1.3 Steady-State Analysis

Based on the circuit analysis of the proposed converter introduced in subsection 3.1.2, States 2 and 4 can be neglected in the steady-state analysis because these two intervals are very short as compared with the total switching period. By employing the voltage-second balance across L_m, one can obtain the following equation:

$$V_b \frac{L_m}{L_m + L_r} \cdot (D - D_{s5}) - \frac{n_2}{n_3} V_o \cdot (1 - D) + v_{N2} D_{s5} = 0. \tag{3.28}$$

Similarly, the voltage-second balance across L_r gives

$$V_b \frac{L_r}{L_m + L_r} \cdot (D - D_{s5}) - \left(V_c - \frac{n_2}{n_3} V_o\right) \cdot (1 - D) + (V_b - v_{N2}) \cdot D_{s5} = 0. \tag{3.29}$$

In mode M_1, since the D_{s5} is very small and can be neglected in the circuit analysis, the duty ratio in mode M_1 can be obtained from (3.28):

$$D_{M1} \approx \frac{V_o}{V_b \cdot \frac{L_m}{L_m + L_r} \cdot \frac{n_3}{n_2} + V_o}. \tag{3.30}$$

Adding (3.28) to (3.29), the clamp capacitor voltage in mode M_1 can be derived as

$$V_{c,M1} = \frac{D_{M1}}{1 - D_{M1}} V_b. \tag{3.31}$$

Moreover, according to (3.13), we can obtain the approximated expression of the clamp capacitor voltage in mode M_2 by neglecting the small oscillation term:

$$v_{c,M2}(t) \approx \frac{n_2}{n_3} V_o + \frac{L_r}{L_b + L_r} \cdot \left(\left| v_{ac}(t) \right| + \frac{n_1}{n_3} V_o - V_b \right). \tag{3.32}$$

Substitute (3.32) into (3.29) to replace V_c; thus, the addition of (3.28) and (3.29) yields

$$V_b \cdot D = \left[\frac{L_r}{L_b + L_r} \cdot \left(\left| v_{ac}(t) \right| + \frac{n_1}{n_3} V_o - V_b \right) + \frac{n_2}{n_3} V_o \right] \cdot (1 - D). \tag{3.33}$$

From (3.33), the time function of the duty ratio in mode M_2 is given by

$$D_{M2}(t) = 1 - \frac{V_b}{\frac{L_r}{L_r + L_b} \left(\left| v_{ac}(t) \right| + \frac{n_1}{n_3} V_o - V_b \right) + V_b + \frac{n_2}{n_3} V_o}. \tag{3.34}$$

Substituting (3.34) into (3.28), the time function of D_{s5} in mode M_2 is given by

$$\begin{aligned} D_{s5,M2}(t) &= (1 - D_{M2}(t)) \cdot \frac{\frac{L_m}{L_m + L_r} \cdot \left[\frac{L_r}{L_r + L_b} \cdot \left(\left| v_{ac}(t) \right| + \frac{n_1}{n_3} V_o - V_b \right) + \frac{n_2}{n_3} V_o \right] - \frac{n_2}{n_3} V_o}{\left(\frac{L_m}{L_m + L_r} V_b - v_{N2}(t) \right)} \\ &\approx \frac{V_b \frac{L_r}{L_r + L_b} \cdot \left(\left| v_{ac}(t) \right| + \frac{n_1}{n_3} V_o - V_b \right) \cdot \left[L_b + L_r \cdot \left(\frac{n_1 + n_2}{n_2} \right)^2 \right]}{\left[\frac{L_r}{L_r + L_b} \left(\left| v_{ac}(t) \right| + \frac{n_1}{n_3} V_o - V_b \right) + V_b + \frac{n_2}{n_3} V_o \right] \cdot L_r \frac{n_1 + n_2}{n_2} \cdot \left(\frac{n_1 + n_2}{n_2} V_b - v_{ac}(t) \right)} \end{aligned} \tag{3.35}$$

where the approximation comes from $L_m >> L_r$.

In addition, the boundary between modes M_1 and M_2 occurs just as $|v_{ac}(t)|$ is large enough to charge the boost inductor during State 3. Thus, from Figs. 3.5(c) and 3.5(d) and KVL, the

boundary voltage of modes M_1 and M_2, V_{BD}, is determined by

$$V_{BD} = V_{c,M1} + V_b - \frac{n_1 + n_2}{n_3} V_o . \tag{3.36}$$

The boundary angle θ_b shown in Fig. 3.4 can be calculated from (3.36):

$$\theta_b = \sin^{-1}\left(\frac{V_{c,M1} + V_b - \frac{n_1 + n_2}{n_3} V_o}{\left| V_{ac(pk)} \right|} \right) \tag{3.37}$$

where $|V_{ac(pk)}|$ is the peak rectified line voltage.

3.2 Design Considerations

The design specifications of the proposed converter are given as follows: input voltage range V_{ac} = 90–260 Vrms (60 Hz); output voltage V_o = 48 V; rated output power P_o = 100 W; switching frequency f_s = 100 kHz; conversion efficiency η =0.85.

The bulk capacitor voltage V_b is dependent on the line voltage and the output load. According to the empirical rule, the moderate value of V_b usually ranges between 1.1 and 1.2 times as high as $V_{ac(pk)}$. Moreover, to maximize the conversion efficiency, the duty ratio should be from 0.4 to 0.5 at low line since the low line is considered the critical case in this design. To ensure the proposed converter operating properly, the converter parameters are determined as follows.

(1) Determining the Turns Ratio n_2/n_3

Let $L_m >> L_r$. By using the same operation theory applied to a simple flyback circuit operating in CCM, the primary to secondary turns ratio n_2/n_3 can be approximately obtained as

$$\frac{n_2}{n_3} = \frac{V_{b,\min}}{V_o} \cdot \frac{D_{\max}}{1 - D_{\max}} . \tag{3.38}$$

(2) Determining the Transformer Primary Magnetizing Inductance L_m

To ensure that the flyback cell always operates in CCM, the inductance L_m must satisfy the following condition:

$$L_m > \frac{\left((1-D_{\min})\cdot V_o\right)^2 \cdot \eta}{2 f_s P_o} \cdot \left(\frac{n_2}{n_3}\right)^2 . \tag{3.39}$$

(3) Determining the Clamp Capacitor C_c

The resonant frequency determined by C_c and L_r should be sufficiently low so that the half resonant period $\pi\sqrt{L_r C_c}$ is greater than the duty-off time. Thus, the minimum value of C_c can be obtained as:

$$C_c > \frac{\left((1-D_{\min})\cdot T_s\right)^2}{\pi^2 L_r} . \tag{3.40}$$

According to the design specifications and (3.38), (3.39) and (3.40), the parameters n_2/n_3, L_m, and C_c are selected as 2.3, 318.4 μH, and 0.22 μF, respectively. Furthermore, the other converter parameters with special function, including L_b and L_r, are determined as follows.

(4) Determining the Boost Inductor L_b

To achieve self-PFC, the boost inductor must operate in DCM over the entire line cycle. Thus, the design must satisfy the condition of $D_{s5} < D$ in the whole line cycle. Since the critical boundary condition of CCM and DCM occurs at the lowest peak input voltage, the maximum boost inductance can be determined from (3.35):

$$L_{b,\max} = \frac{\left[\left(\frac{n_1/n_3 + n_2/n_3}{n_2/n_3}\right)^2 - K\right]\cdot L_r}{K-1} \tag{3.41}$$

where $K = \frac{D_{\max}}{1-D_{\max}} \cdot \left(\frac{n_1/n_3 + n_2/n_3}{n_2/n_3} \right) \cdot \left(\frac{\frac{n_1/n_3 + n_2/n_3}{n_2/n_3} \cdot V_{b,\min} - V_{ac(pk),\min}}{V_{ac(pk),\min} + V_o n_1/n_3 - V_{b,\min}} \right)$.

According to (3.41), we can plot the relationship between $L_{b,\max}$ and n_1/n_3 at V_{ac} = 90 Vrms for possible $D_{\max}$ and m (ratio of $V_{b,\min}/V_{ac(pk),\min}$), as shown in Fig. 3.7. It can be found that the increases in n_1/n_3 cause $L_{b,\max}$ to increase for fixed $D_{\max}$, m, n_2/n_3, and L_r.

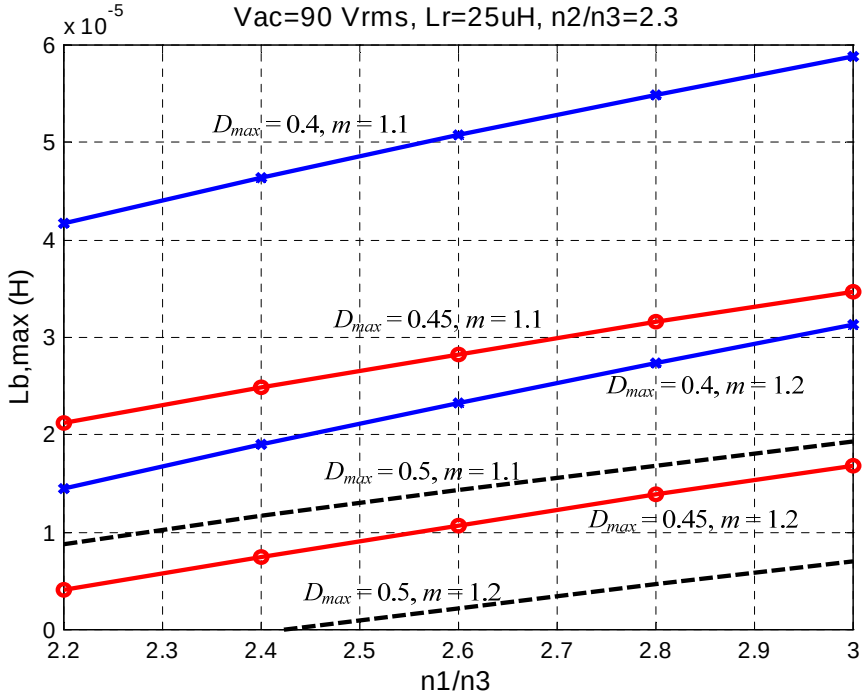


Fig. 3.7 The maximum boost inductance $L_{b,max}$ versus turns ratio n_1/n_3.

(5) Determining the Resonant Inductor L_r

According to the operating principle of State 4, to ensure the ZVS turn-on for S_1, the energy stored in the parallel of resonant inductor L_r and boost inductor L_b must be greater than the energy stored in the resonant capacitor C_r. Thus, for the given C_r contributed by the parasitic capacitances of S_1 and S_2, the following relationship should be guaranteed:

$$\frac{L_r L_b}{L_r + L_b} > \max\left(\frac{C_r \cdot \left(V_{b,\max} + \frac{n_2}{n_3} V_o \right)^2}{\left(i_{s1,M1}(t_3) \right)^2}, \frac{C_r \cdot \left[\frac{n_2}{n_3} V_o + \frac{L_r}{L_r + L_b} \cdot \left(V_{ac(pk),\max} + \frac{n_1}{n_3} V_o - V_b \right) + V_b \right]^2}{\left(i_{s1,M2}(t_3) \right)^2} \right). \tag{3.42}$$

3.3 Analysis of the Line Current Waveform

As shown in Fig. 3.3, the low pass filter L_f–C_f will filter out the switching frequency components and harmonics of i_{Lb}. Thus, the rectified line current $|i_{ac}(t)|$ is the average value of $i_{Lb}(t)$ within a switching period, namely, $|i_{ac}| = i_{Lb,ch(ave)} + i_{Lb,dis(ave)}$. Moreover, the expression of $i_{Lb,dis(ave)}$ in (3.27) can be rearranged as follows by substituting (3.35) into (3.27):

$$i_{Lb,dis(ave)}(t) = \frac{(1 - D_{M2}(t))^2 T_s}{2} \cdot \frac{n_2}{n_1 + n_2} \cdot \frac{L_r + L_m}{L_r L_m} \cdot \left[\left(\frac{n_2}{n_1 + n_2} \right)^2 \cdot \frac{L_r + L_m}{L_r L_m} L_b + 1 \right] \cdot \frac{\left\{ \frac{L_m}{L_r + L_m} \cdot \left[\frac{L_r}{L_r + L_b} \cdot \left(|v_{ac}(t)| + \frac{n_1}{n_3} V_o - V_b \right) + \frac{n_2}{n_3} V_o \right] - \frac{n_2}{n_3} V_o \right\}^2}{\left(\frac{L_m}{L_r + L_m} V_b - \frac{n_2}{n_1 + n_2} v_{ac}(t) \right)}. \tag{3.43}$$

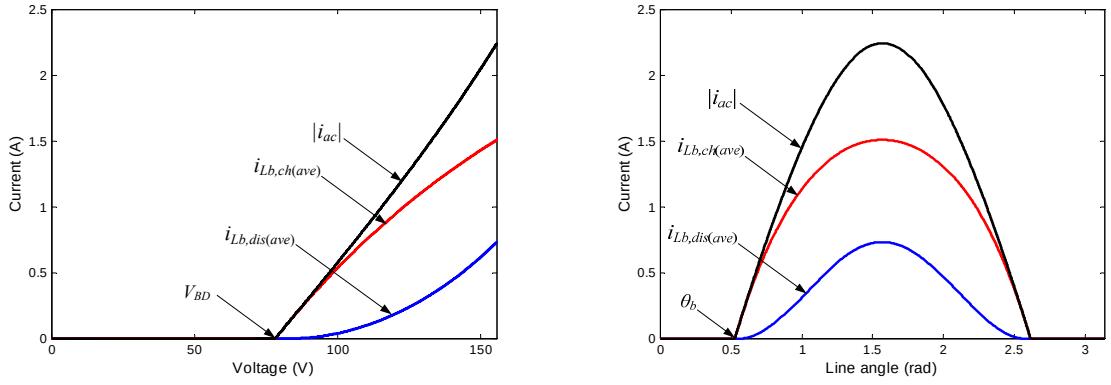
According to (3.16), (3.34), and (3.43), $i_{Lb,ch(ave)}$, $i_{Lb,dis(ave)}$, and $|i_{ac}|$ in a half line cycle are plotted in Fig. 3.8, in which only mode M_2 is considered. Moreover, based on (3.34) and (3.35), the curves of $(1 - D)$ and D_{s5} for mode M_2 can be drawn in Fig. 3.9. These curves are sketched by using the following parameters: L_r = 27.5 μH, L_b = 10 μH, L_m = 318.4 μH, n_1: n_2: n_3 = 2.3: 2.3: 1, V_{ac} = 110 Vrms, V_b = 1.15 · $V_{ac(pk)}$, T_s = 10 μs, V_o = 48 V, and P_o = 100 W. Although the determination of turns ratio n_1/n_3 is somewhat arbitrary at present, the detailed selection criterion of n_1/n_3 will be discussed in the next section for satisfying the harmonic requirements.

As shown in Fig. 3.8(a), the i-v curve of $i_{Lb,ch(ave)}$ can be designed to bend convexly while that of $i_{Lb,dis(ave)}$ still bends concavely. Since these two bent curves have remarkable compensa-

tion to each other, the i-v curve of $|i_{ac}|$ has very good linear characteristics. The special charging mechanism of $i_{Lb,ch(ave)}$ is explained as follows. When $|v_{ac}(t)|$ increases, D_{s5} also increases correspondingly. Moreover, the charging voltage of L_m in the $D_{s5}T_s$ duration is smaller than that in the $(D-D_{s5})T_s$ duration, as illustrated in Fig. 3.6(b). Smaller charging voltage produces less magnetizing energy injected in L_m and consequently lower output voltage is formed. To maintain the constant output voltage, the controller will increase the duty ratio D under output voltage feedback control. Thus, $(1-D)$, or named the effective duty ratio of the ICS cell, will be inversely proportional to the instantaneous rectified line voltage with DC offset, as shown in Fig. 3.9. The AC modulation effect on $(1-D)$ makes $i_{Lb,ch(ave)}(t)$ convexly vary with $|v_{ac}(t)|$. The compensation produces a result in which the second derivative $\partial i_{ac}^2/\partial^2 v_{ac}$ is very small and ranges between -1.1×10^{-4} and 2.2×10^{-4}. This result shows that the relationship between $|i_{ac}|$ and $|v_{ac}|$ is nearly linear and can be expressed as

$$|i_{ac}| = \frac{(|v_{ac}| - V_{BD})}{R_{eq}} + \text{negligible nonlinear terms} \tag{3.44}$$

where R_{eq} is the equivalent input resistance. The linear result can be seen clearly from Fig. 3.8.



(a) (b)

Fig. 3.8 Comparison of $i_{Lb,ch(ave)}$, $i_{Lb,dis(ave)}$, and $|i_{ac}|$ drawn by the proposed converter in a half line cycle at 110 Vrms: (a) the currents as a function of instantaneous line voltage and (b) the current waveforms as a function of line angle.

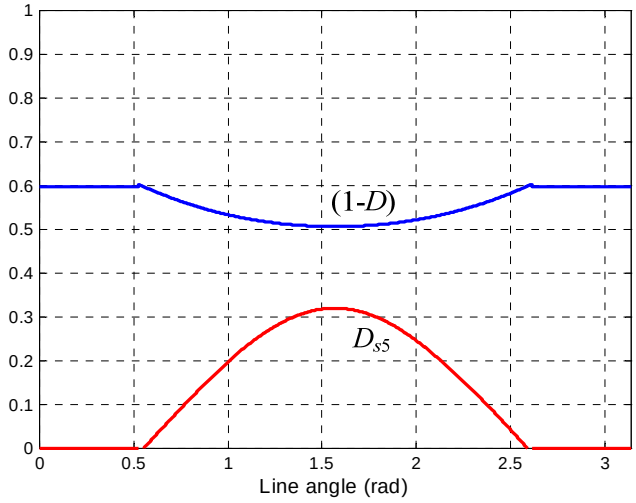


Fig. 3.9 $(1-D)$ and D_{s5} versus line angle for 110 Vrms in a half line cycle.

3.4 Designing the ICS Cell to Meet IEC 61000-3-2 Requirements

Equation (3.37) shows that a larger n_1/n_3 will cause a smaller boundary angle and lower current harmonics. However, a larger n_1/n_3 also causes more energy of L_m to redundantly circulate to C_b through winding N_1. Thus, the design objective of determining n_1/n_3 is to find its minimum value with which the input current harmonics can meet the IEC 61000-3-2 Class D requirements. Note that since n_2/n_3 has been determined in Section 3.2, the selection of n_1/n_3 is equivalent to the selection of the boundary angle. Thus, the design objective becomes finding the maximum acceptable boundary angle.

Since IEC 61000-3-2 Class D gives the requirements of the acceptable harmonics, to find the maximum acceptable boundary angle, each input current harmonic should be computed. According to the conclusion of (3.44) and Fig. 3.8(b), the mathematical expression of the line current during $[\theta_b, \pi-\theta_b]$ can be expressed as

$$i_{ac}(\omega t) = i_{ac}\left(\frac{\pi}{2}\right)\cdot\sin\left((\omega t-\theta_b)\cdot\frac{\pi}{\pi-2\theta_b}\right) \tag{3.45}$$

where ω is the angular frequency of the line voltage. Thus, the nth harmonic component I_n can

be calculated by Fourier analysis:

$$I_n = \frac{\pi - 2\theta_b}{\pi} \cdot i_{ac}\left(\frac{\pi}{2}\right) \cdot \left\{ \left[\sin\left((n-1)\pi - n\theta_b\right) - \sin\left(n\theta_b\right)\right] \cdot \frac{1}{(n-1)\pi - 2n\theta_b} - \left[\sin\left((n+1)\pi - n\theta_b\right) - \sin\left(n\theta_b\right)\right] \cdot \frac{1}{(n+1)\pi - 2n\theta_b} \right\} \tag{3.46}$$

where n = 1, 3, 5...39. Since the Class D limits are defined as the ratio of current harmonic to fundamental-frequency component, I_n/I_1. From (3.46), we can obtain the normalized value of each harmonic as a function of the boundary angle as drawn in Fig. 3. 10. Fig. 3.10 shows that the most critical harmonic is the fifth for complying with the Class D requirements since its acceptable boundary angle is smaller than all the others. Therefore, the maximum allowable boundary angle is 1.005 rad (= 57.58°). It should be noted that since (3.45) is derived in neglecting the small current components presenting in mode M_1, the practical allowable boundary angle will be a little larger than that obtained from (3.45).

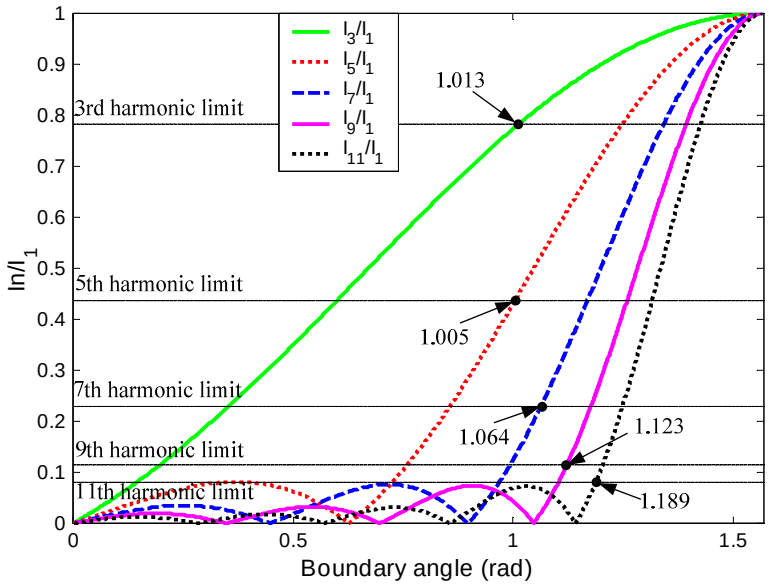


Fig. 3.10 The maximum boundary angles of 3rd–11th harmonics complying with IEC 61000-3-2 Class D specifications.

Next, by solving the set of (3.30), (3.31), and (3.37), we obtain the value of n_1/n_3 as

$$\frac{n_1}{n_3} = V_{ac(pk)} \cdot \left(\frac{V_b}{V_{ac(pk)}} \cdot \frac{1}{V_o} + \frac{n_2}{n_3} \cdot \frac{L_r}{L_m} \cdot \frac{1}{V_{ac(pk)}} - \frac{\sin\theta_b}{V_o} \right). \tag{3.47}$$

In the proposed converter, a higher line input voltage causes a larger boundary angle. Thus, we must make sure that the design satisfies the requirements of the Class D especially at the nominal high line input, that is 230 Vrms. Using the same values of L_m, L_r, n_2/n_3, V_o, and $V_b/V_{ac(\mathrm{pk})}$ as in the previous section, we obtain n_1/n_3 = 2.27 when V_{ac} = 230 Vrms and θ_b =1.005 rad. In other words, n_1/n_3 = 2.27 is the boundary of compliance with Class D limits.

3.5 Experimental Results

To verify the feasibility of the proposed topology, experimental tests were performed under the specifications described in Section 3.2. The circuit components used for the experiment are listed in Table 3.1 The capacitance C_r consists of only the output capacitances of S_1 and S_2. In the experimental circuit, the low-cost current-mode integrated controller UC3843 was used to generate the PWM control signal. Also, the combination of simple logic IC's, R–C circuits, and a high-side switch driver IR2110 was used to generate the complementary control signals for switches S_1 and S_2. Note that the inductance ratio L_b/L_m employed in the prototype circuit is only 0.03, which is about 1/30–1/8 times as large as the L_b/L_m ratio employed in the previous converters with similar line current waveforms [34], [39].

Fig. 3.11 shows the measured switching waveforms of the prototype circuit operating at 110 Vrms. Figs. 3.11(a) and 3.11(b) illustrate the gate-drive voltage of S_1, the resonant inductor current, the current of S_1, and the drain-to-source voltage of S_1. Experiments have verified the soft-switching characteristics as well as the active clamping of the voltage drop across switch S_1. In Figs. 3.11(c) and 3.11(d), the waveform of the boost inductor current i_{Lb} reveals that the ICS cell operates in DCM. It also can be seen from the waveform of the output rectifier current i_{N3} that the rectifier reverse recovery effect has been suppressed. From Figs. 3.11(b)

and 3.11(d) with respect to mode M_2, it can be seen that i_{S1} and i_{Lb} are operated with interleaved fashion since the two figures use the same time base.

Fig. 3.12 shows the measured line voltage and line current waveforms at V_{ac} = 110 Vrms. It can be seen that the current waveform has a near-sinusoidal shape in mode M_2. Fig. 3.13 shows that the detailed current harmonics measured from the experimental prototype operating in the high and low line inputs can satisfy the requirements of IEC 61000-3-2 Class D. Fig. 3.14 shows that the conversion efficiency at full load is 88.3–91.3%. The experimental results of Figs. 3.13 and 3.14 indicate that with the selected turns ratio n_1/n_3 = 2.3 the harmonic contents can be guaranteed to comply with the Class D specifications, and meanwhile, the conversion efficiency can achieve around 90%. Fig. 3.15 shows that the bulk capacitor voltages are maintained within a desirable range (1.1–1.2 times as high as the peak line voltage) even though the converter operates in a wide range of input voltage (90–260 Vrms). The maximum bulk capacitor voltage is 425 V, which occurs at 260 Vrms input voltage. Thus, the commercially available 450V-rated electrolytic capacitors can be used. Fig. 3.15 also demonstrated that the proposed converter can obtain a well shaped line current waveform while M (ratio of $V_b/V_{ac(pk)}$) is only in the range of 1.1 to 1.2.

Table 3.1 Component values for the prototype circuit

Component	Device Description
S_1, S_2	SPA11N60C3
D_1	U08A100
D_2	U08A30C
L_b	10 μH
L_r	27.5 μH
L_m	318.4 μH
n_1: n_2: n_3	23: 23: 10
C_b	300 μF/450 V
C_r	780 pF
C_c	0.22 μF/400 V
C_o	100 μF/100 V

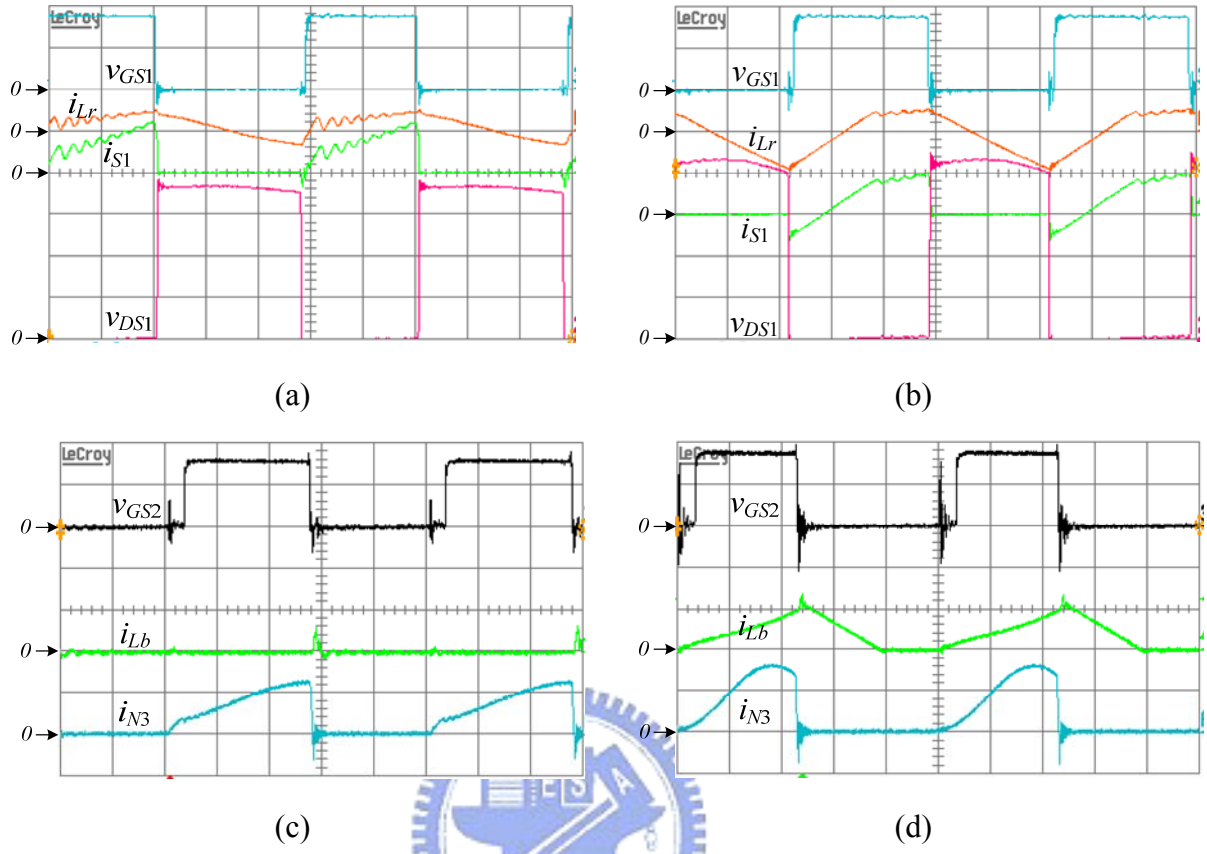


Fig. 3.11 Measured waveforms during a switching period:

(a) waveforms in mode M_1: v_{GS1} (10 V/div); i_{Lr} (5 A/div); i_{S1} (3.2 A/div); v_{DS1} (100 V/div),

(b) waveforms in mode M_2: v_{GS1} (10 V/div); i_{Lr} (10 A/div); i_{S1} (3.2 A/div); v_{DS1} (100 V/div),

(c) waveforms in mode M_1: v_{GS2} (10 V/div); i_{Lb} (2 A/div); i_{N3} (100 V/div), and

(d) waveforms in mode M_2: v_{GS2} (10 V/div); i_{Lb} (5 A/div); i_{N3} (100 V/div).

Time scale: 2 μ s/div.

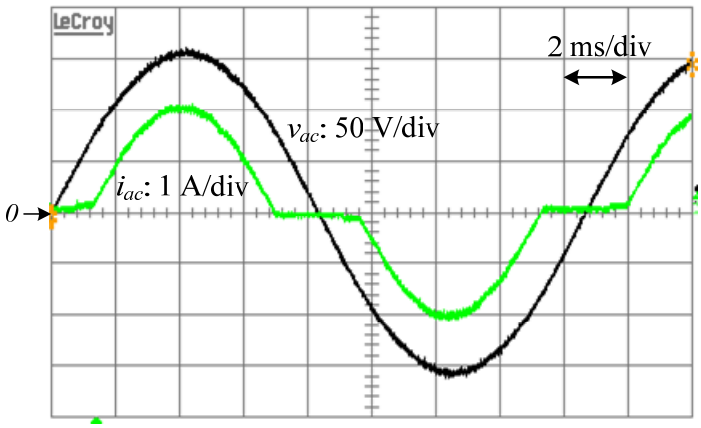


Fig. 3.12 Measured line voltage and current waveforms at V_{ac} = 110 Vrms and full load.

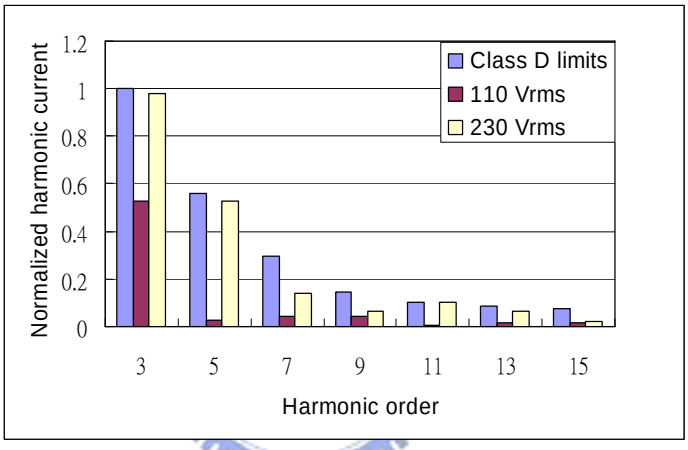


Fig. 3.13 Measured line current harmonics comparison at full load.

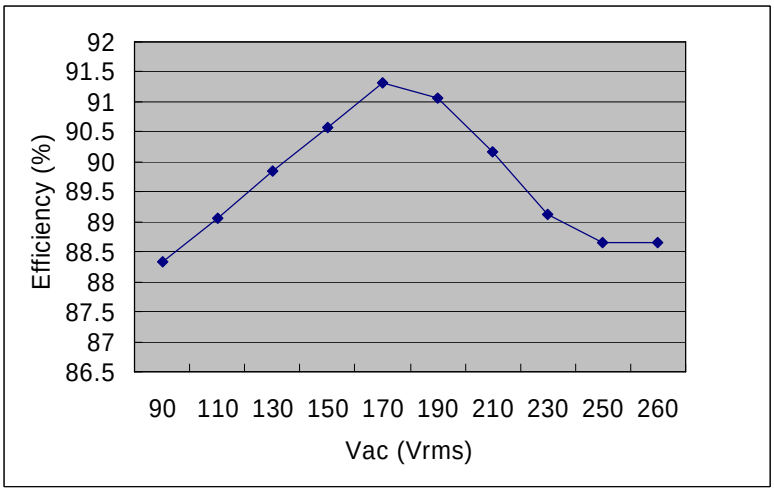


Fig. 3.14 Conversion efficiency versus input voltage.

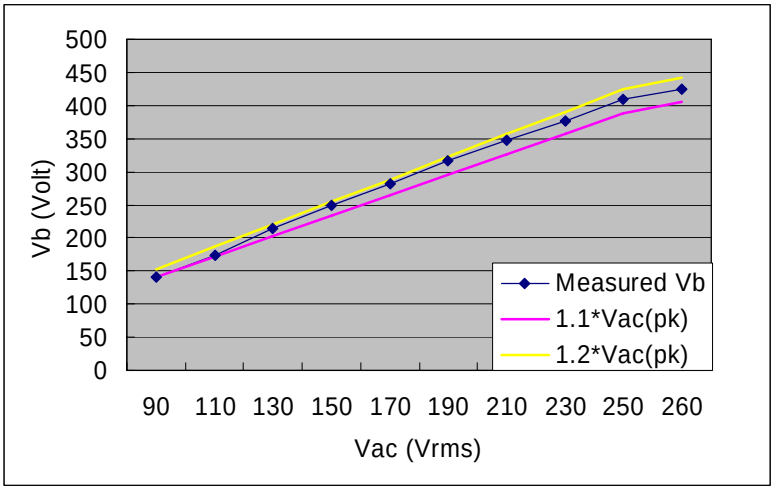


Fig. 3.15 Bulk capacitor voltage versus input voltage.

3.6 Topology Refinement

3.6.1 Proposed Circuit and Operating Principles

As can be seen in Fig. 3.3, since winding N_1 is in the charging path of L_r, the inductor L_r can be used to provide both the boost ICS function operating in DCM and the soft-switching function for the DC-DC cell. Thus, the boost inductor can be saved and the volume and weight of magnetic components are reduced. Based on the above concept, a new single-stage soft-switching AC-DC flyback converter, shown in Fig. 3.16, is proposed. Like the fly-back-type implementation of the topology shown in Fig. 3.3, the new flyback converter can also provide the two following key functions. First, the ICS cell of the converter is charged in the duty-off time; therefore, the current stress on the main switch S_1 is alleviated. Second, the charging time of the ICS cell is designed to be inversely modulated by the line voltage, so that the i-v curve of the average charging current presents a opposite deformation characteristic to that of the average discharging current. Therefore, the average charging current of the ICS cell can effectively compensate the line current distortion caused by the modulation of the ICS inductor discharging time. To sum up briefly, this converter combines the advantages of sim-ple topology, line current waveform correction, and switch current stress reduction.

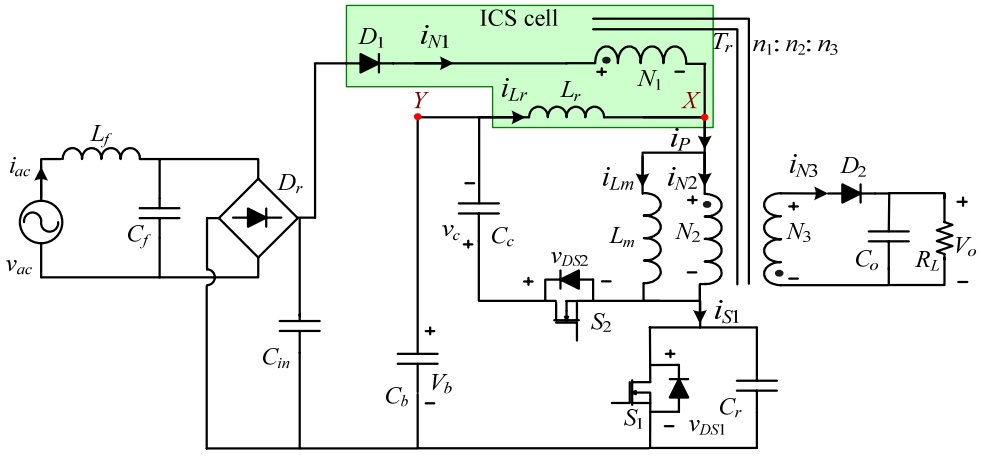


Fig. 3.16 Proposed single-stage soft-switching AC-DC converter.

The basic operating principles of this converter can be referred to subsection 3.1.2. But the expressions of the average charging current and the average discharging current of the ICS cell are different from (3.16) and (3.27), respectively. To evaluate the line current shaping performance, we derive the related equations as follows.

Using the operating principle obtained in State 3, the average charging current of the ICS cell in one switching period can be calculated. First, by employing Ampere's law, the current i_{N1} in this state is given by

$$i_{N1} = -\frac{n_2}{n_1} \cdot i_{N2} - \frac{n_3}{n_1} \cdot i_{N3} . \tag{3.48}$$

From Fig. 3.16 and KCL, the following equation is given:

$$i_{N1} + i_{Lr} = i_P = i_{Lm} + i_{N2} . \tag{3.49}$$

Substitute (3.49) into (3.48) to replace i_{N2}, the integration of (3.48) through the duty-off time can be obtained as:

$$\int_0^{(1-D)T_s} i_{N1}(t)dt = -\frac{n_2}{n_1} \cdot \int_0^{(1-D)T_s} \left(i_{N1}(t) + i_{Lr}(t) - i_{Lm}(t)\right)dt - \frac{n_3}{n_1} \cdot \int_0^{(1-D)T_s} i_{N3}(t)dt . \tag{3.50}$$

Replacing the time functions of i_{Lr}, i_{Lm}, and i_{N3} with their corresponding voltage expressions yields

$$\left(\frac{n_1+n_2}{n_1}\right)\cdot\int_0^{(1-D)T_s} i_{N1}(t)dt$$
$$=\frac{n_2}{n_1}\cdot\frac{1}{L_r}\left(\left|v_{ac}(t)\right|+\frac{n_1}{n_3}\cdot V_o-V_b\right)\cdot\frac{t^2}{2}\Bigg|_0^{(1-D)T_s}-\frac{V_o}{L_m}\cdot\frac{{n_2}^2}{n_1n_3}\cdot\frac{t^2}{2}\Bigg|_0^{(1-D)T_s}-\frac{n_3}{n_1}\cdot\frac{P_o}{V_o}\cdot T_s. \tag{3.51}$$

Averaging (3.51) over a switching period, the average charging current of the ICS cell can be obtained as follows:

$$i_{N1,ch(ave)}(t)=\frac{(1-D)^2T_s}{2}\cdot\frac{n_2}{n_1+n_2}\cdot\left[\frac{1}{L_r}\cdot\left(\left|v_{ac}(t)\right|+\frac{n_1}{n_3}\cdot V_o-V_b\right)-\frac{V_o}{L_m}\cdot\frac{n_2}{n_3}\right]-\frac{P_o}{V_o}\cdot\frac{n_3}{n_1+n_2}. \tag{3.52}$$

Moreover, the discharging current of the ICS cell in one switching period can be calculated as follows. By employing Ampere's law and KCL, the expression of i_{N1} in State 5 can be given by

$$i_{N1}=-\frac{n_2}{n_1}\cdot i_{N2}=-\frac{n_2}{n_1}\cdot\left(i_{N1}+i_{Lr}-i_{Lm}\right) \tag{3.53}$$

where i_{Lr} and i_{Lm} can be expressed as follows:

$$i_{Lr}(t)=i_{Lr}(t_4)+\frac{V_b-\frac{|v_{ac}|}{1+n_1/n_2}}{L_r}\cdot t \tag{3.54}$$

$$i_{Lm}(t)=i_{Lm}(t_4)+\frac{|v_{ac}|}{L_m(1+n_1/n_2)}\cdot t. \tag{3.55}$$

The substitution of (3.54) and (3.55) into (3.53) to replace i_{Lr} and i_{Lm} yields

$$i_{N1}(t)=i_{N1}(t_4)+\frac{n_2}{n_1+n_2}\cdot\left(-\frac{V_b}{L_r}+\frac{|v_{ac}|}{1+n_1/n_2}\cdot\frac{L_r+L_m}{L_rL_m}\right)\cdot t. \tag{3.56}$$

By integrating (3.56) through the $D_{s5}T_s$ interval, the average discharging current of the ICS cell can be given as

$$i_{N1,dis(ave)}(t)=\left(\frac{n_2}{n_1+n_2}\right)\cdot\left(V_b-\frac{|v_{ac}(t)|}{1+n_1/n_2}\cdot\frac{L_r+L_m}{L_m}\right)\cdot\frac{t^2}{2L_rT_s}\Bigg|_0^{D_{s5}T_s}$$
$$=\frac{{D_{s5}}^2\cdot T_s}{2L_r}\cdot\left(\frac{n_2}{n_1+n_2}\right)\cdot\left(V_b-\frac{|v_{ac}(t)|}{1+n_1/n_2}\cdot\frac{L_r+L_m}{L_m}\right)\cdot \tag{3.57}$$

3.6.2 Steady-State Analysis

The steady-state analysis of this converter is similar to the analysis introduced in subsection 3.1.3 and performed as follows. By employing the voltage-second balance across L_m, one can obtain the following equation:

$$V_b \cdot \left(\frac{L_m}{L_m + L_r} \right) \cdot (D - D_{s5}) - \frac{n_2}{n_3} V_o \cdot (1 - D) + \frac{|v_{ac}|}{1 + n_1/n_2} \cdot D_{s5} = 0 . \tag{3.58}$$

Similarly, the voltage-second balance across L_r gives

$$V_b \cdot \left(\frac{L_r}{L_m + L_r} \right) \cdot (D - D_{s5}) - \left(V_c - \frac{n_2}{n_3} V_o \right) \cdot (1 - D) + \left(V_b - \frac{|v_{ac}|}{1 + n_1/n_2} \right) \cdot D_{s5} = 0 . \tag{3.59}$$

Since the D_{s5} in mode M_1 is very small and can be neglected in the circuit analysis, from (3.58), the duty ratio in mode M_1 can be approximated as:

$$D_{M1} \approx \frac{V_o}{V_b \cdot \left(\frac{L_m}{L_m + L_r} \right) \cdot \frac{n_3}{n_2} + V_o} . \tag{3.60}$$

Moreover, we assume that the transformer almost has ideal coupling, thus the clamp capacitor voltage in mode M_2 can be obtained from KVL along C_{in}-D_1-N_1-N_2-S_2-C_c-C_b.

$$v_{c,M2}(t_2) = |v_{ac}| + \frac{n_1 + n_2}{n_3} \cdot V_o - V_b . \tag{3.61}$$

Substitute (3.61) into (3.59) to replace V_c; thus, the addition of (3.58) and (3.59) yields

$$V_b \cdot (D - D_{s5}) - \left(|v_{ac}| + \frac{n_1 + n_2}{n_3} V_o - V_b \right) \cdot (1 - D) + V_b \cdot D_{s5} = 0 . \tag{3.62}$$

From (3.62), the time function of the duty ratio in mode M_2 can be obtained as

$$D_{M2}(t) = 1 - \frac{V_b}{|v_{ac}(t)| + \frac{n_1 + n_2}{n_3} \cdot V_o} . \tag{3.63}$$

By substituting (3.63) into (3.58), the time function of D_{s5} in mode M_2 can be obtained as

$$D_{s5,M2}(t) = (1 - D_{M2}(t)) \cdot \frac{\frac{L_m}{L_m + L_r} \cdot \left(|v_{ac}(t)| + \frac{n_1 + n_2}{n_3} \cdot V_o - V_b \right) - \frac{n_2}{n_3} \cdot V_o}{\left(V_b \cdot \frac{L_m}{L_m + L_r} - \frac{|v_{ac}(t)|}{1 + n_1 / n_2} \right)}. \quad (3.64)$$

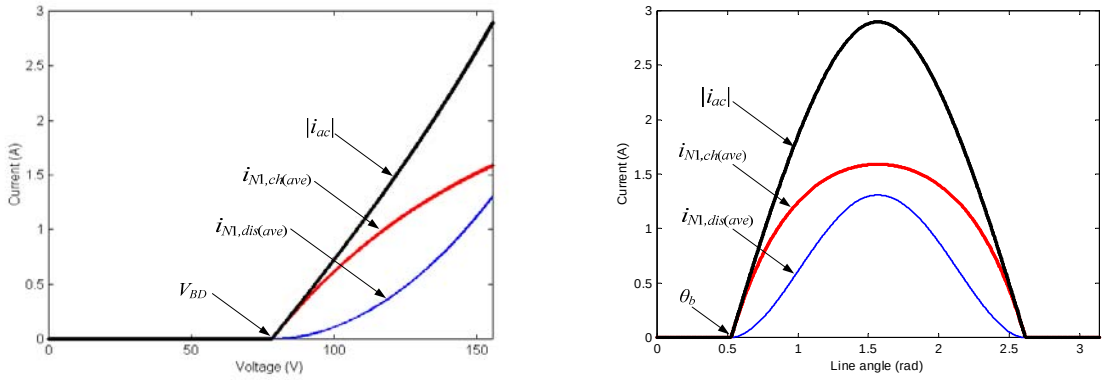
It is worth mentioning that the expressions of D_{M1}, $v_{c,M2}$, D_{M2}, and $D_{s5,M2}$ are equal to (3.30), (3.32), (3.34), and (3.35), respectively, in which if L_b is neglected. Additionally, for this converter, the clamp capacitor voltage V_c and the boundary angle θ_b have the same expressions as those of the flyback-type implementation of the converter shown in Fig. 3.3.

3.6.3 Analysis of the Line Current Waveform

For a quantitative evaluation of the ICS function of the proposed converter, the characteristic curves of $i_{N1,ch(ave)}$, $i_{N1,dis(ave)}$, and $|i_{ac}|$ should be sketched. First, by substituting (3.64) into (3.57), the expression of $i_{N1,dis(ave)}$ can be rearranged as follows:

$$i_{N1,dis(ave)}(t) = \frac{(1 - D_{M2}(t))^2 \cdot T_s}{2L_r} \cdot \frac{n_2}{n_1 + n_2} \cdot \frac{L_r + L_m}{L_m} \cdot \frac{\left[\frac{L_m}{L_r + L_m} \cdot \left(|v_{ac}(t)| + \frac{n_1 + n_2}{n_3} \cdot V_o - V_{Cb} \right) - \frac{n_2}{n_3} \cdot V_o \right]^2}{\left(V_b \cdot \frac{L_m}{L_r + L_m} - \frac{|v_{ac}(t)|}{1 + n_1 / n_2} \right)}. \quad (3.65)$$

According to (3.52), (3.63), and (3.65), $i_{N1,ch(ave)}$, $i_{N1,dis(ave)}$, and $|i_{ac}|$ in a half line cycle are plotted in Fig. 3.17, in which only mode M_2 is considered. These curves are sketched by using the same parameters as those in Section 3.3 for V_{ac} = 110 Vrms and $V_b = 1.15 \cdot V_{ac(pk)}$.



(a) (b)

Fig. 3.17 Comparison of $i_{N1,ch(ave)}$, $i_{N1,dis(ave)}$, and $|i_{ac}|$ drawn by the proposed converter in a half line cycle at 110 Vrms: (a) the currents as a function of instantaneous line voltage and (b) the current waveforms as a function of line angle.

As shown in Fig. 3.17(a), the i-v curve of $i_{N1,ch(ave)}$ can be designed to vary convexly while that of $i_{N1,dis(ave)}$ still varies concavely. It is apparent that $i_{N1,ch(ave)}$ and $i_{N1,dis(ave)}$ have remarkable distortion cancellation result. The special operation mechanism of $i_{N1,ch(ave)}$ is the same as that of $i_{Lb,ch(ave)}$ introduced in Section 3.3. In this design example, the second partial derivative $\partial i_{ac}^2/\partial^2 v_{ac}$ ranges between -2.4×10^{-5} and 2.9×10^{-4}. Therefore, the relationship between $|i_{ac}|$ and $|v_{ac}|$ has been verified to be nearly linear and can be concluded as (3.44). Meanwhile, the converter also can draw almost sinusoidal line current from the AC line in mode M_2, as shown in Fig. 3.17(b).

3.6.4 Experimental Results

To verify the discussed features of the proposed topology, a hardware prototype has been built and tested under the same specifications described in Section 3.2 and the input voltage range is 90–135 Vrms. The circuit components for the experimental prototype are the same as listed in Table 3.1 Fig. 3.18 shows the measured waveforms of the line voltage and line current. It can be seen that the current waveform has a near-sinusoidal shape in mode M_2. Fig.

3.19 shows that the detailed harmonic contents of the line current well satisfy the requirements of IEC 61000-3-2 Class D. It is worth mentioning that the harmonic components are extremely low except for the third harmonic caused by the limited boundary angle. Fig. 3.20 shows the maximum efficiency at full load is 91.7%. Fig. 3.21 shows that the bulk capacitor voltages for different input voltages range between 1.1–1.2 times as high as the peak line voltage. It also demonstrated that the proposed converter can obtain a well shaped line current waveform while M (ratio of $V_b/V_{ac(pk)}$) is only from 1.1 to 1.2.

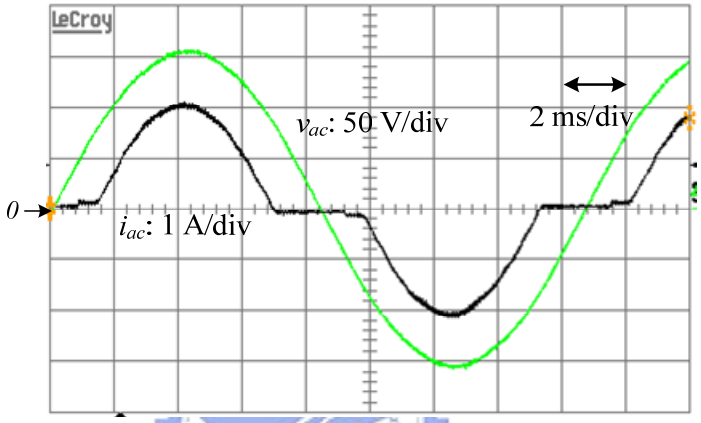


Fig. 3.18 Measured line voltage and current waveforms at V_{ac} = 110 Vrms and 48 V/100 W output.

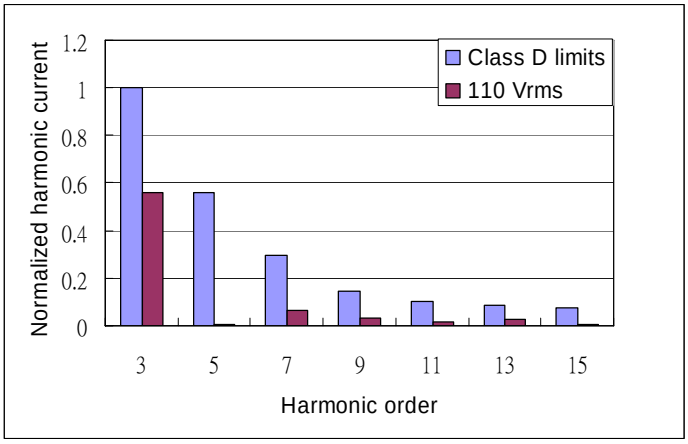


Fig. 3.19 Measured line current harmonics distribution at full load.

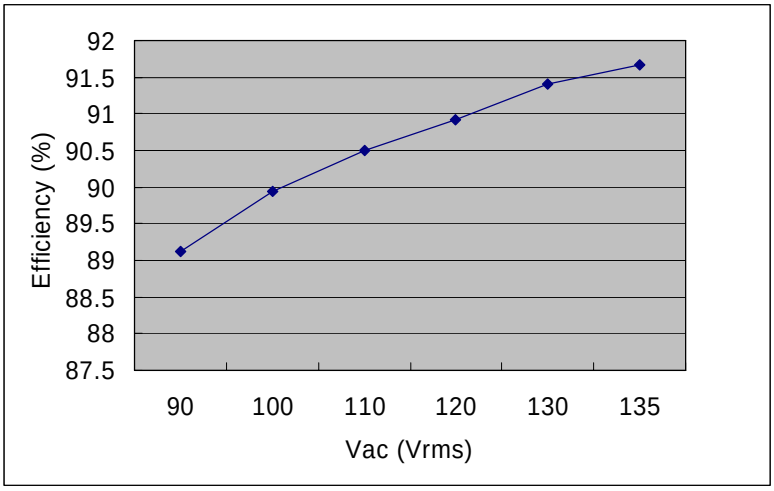


Fig. 3.20 Conversion efficiency versus input voltage.

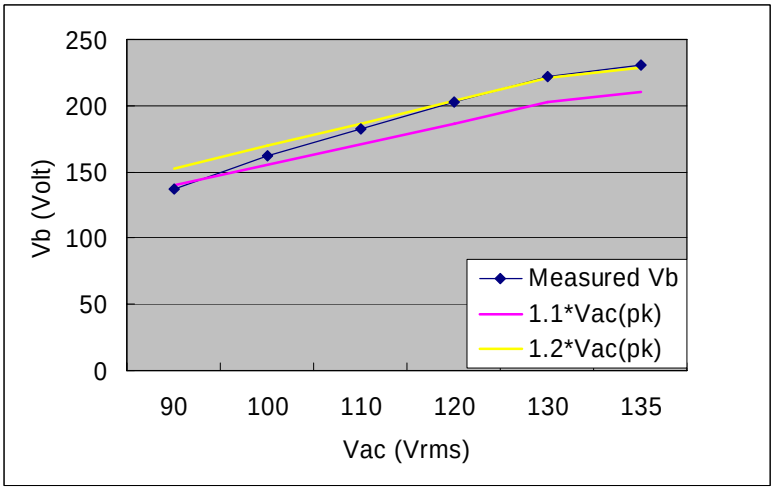
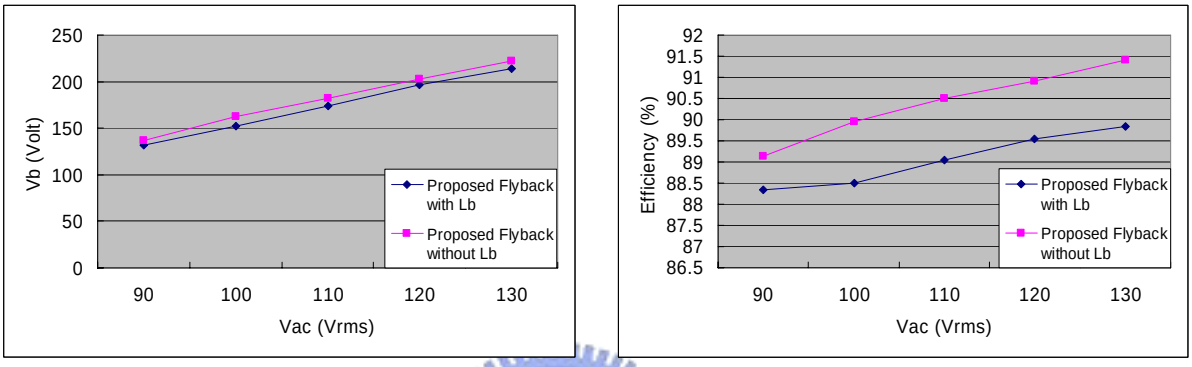


Fig. 3.21 Bulk capacitor voltage versus input voltage.

3.7 Comparison of the Two Proposed AC-DC Flyback Converters

To evaluate the impact of L_b, we compare the performance of the two proposed flyback converters shown in Figs. 3.3 and 3.16, respectively, in the same input voltage range (90–130 Vrms). The measured data including the bulk capacitor voltage and conversion efficiency are shown in Fig. 3.22. From Fig. 3.22(a), it can be found that the use of L_b is favorable to suppress the voltage stress across C_b. This is because L_b can resist i_{Lb} to charge C_b and thus achieving lower V_b. However, from Fig. 3.22(b), it can be seen that using L_b is detrimental to

the conversion efficiency. The reason is explained as follows. When L_b is used, the bulk capacitor voltage becomes lower so that the duty ratio must increase to maintain constant output voltage and thus the power loss on main switch increases too. Even though using L_b can lower the current flowing through N_1 and thus decrease the recycling power. Experimental results shown in Fig. 3.22(b) reveal that the power consumption on active components has more significant effect on conversion efficiency.



(a) (b)

Fig. 3.22 Comparison of the performance of two proposed flyback converters: (a) bulk capacitor voltage and (b) conversion efficiency.

Moreover, since the design without L_b is characterized by the rapidly rising V_b, it is suggested being operated in the applications with narrow input voltage range. The converter can be designed to be operated in low line input (90–135 Vrms) or high line input (180–260 Vrms) by properly adjusting the turns ratio n_1/n_3. Furthermore, since the boost inductor used in the conventional ICS cell is saved, it is possible to achieve higher power density in this converter.

3.8 Concluding Remarks

In this chapter, a novel ICS technique for single-stage AC-DC converters has been introduced. The detailed steady-state behavior of flyback-type implementation with the special ICS function has been studied and analyzed with performance characteristics. It has been

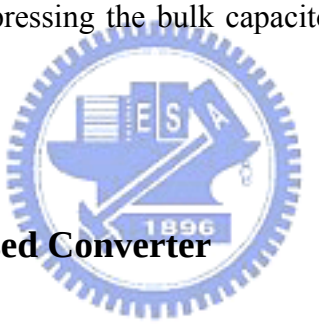
shown that by employing the proposed ICS technique, two key advantages are obtained. First, the ICS cell of the proposed converter is charged in the duty-off time so that the current stress across the main switch is alleviated. Second, the effective duty ratio of the ICS cell is modulated by the instantaneous line voltage. This yields the result that the average charging current of the boost inductor can effectively compensate the modulation effect of the boost inductor discharging time. Consequently, a nearly linear relationship between the line current and voltage through the conduction interval is achieved.

Owing to the ability to draw a near-sinusoidal line current waveform while keeping V_b below a desirable value (V_b < 450 V), the proposed ICS technique is suitable for the universal line voltage applications (90–260 Vrms). Moreover, the design procedure for selecting the minimum n_1/n_3 has been presented to comply with the IEC 61000-3-2 Class D requirements. Using the selected n_1/n_3 ratio, the maximum conversion efficiency of 91.3% can be obtained at full load. Experimental results have demonstrated the proposed line current correction function by a well shaped current waveform and the low current harmonics complying with requirements of IEC 61000-3-2 Class D. Furthermore, the high conversion efficiency has verified the effectiveness of the switch current stress alleviation and soft-switching function.

CHAPTER 4

ANALYSIS AND PERFORMANCE OF THE PROPOSED AC-DC FLYBACK-FORWARD CONVERTER

In general, for a conventional two-stage PFC converter, the input current waveform and the bulk capacitor voltage are well regulated. However, in the S^2ICS converters, the compromise between the input current harmonics, bulk capacitor voltage stress and overall conversion efficiency becomes a very critical issue. A good design of the S^2ICS converter must find a careful trade-off among them. This chapter is going to provide an advanced S^2ICS design with the consideration for suppressing the bulk capacitor voltage stress and improving converter efficiency.



4.1 Analysis of the Proposed Converter

4.1.1 Circuit Derivation

Based on the literature review described in Section 2.3, it can be found that the approach of operating the DC-DC cell in DCM is the most effective and simplest since the addition of extra coupled winding or external circuits is not needed. However, the resulting high RMS current requires a high current-rating switch and reduces the efficiency, as compared with the CCM DC-DC design. This feature is particularly unfavorable for low-voltage high-current applications. To remedy the above drawback, a special combination of the flyback and forward topologies shown in Fig. 4.1 is adopted here [52]. This flyback-forward converter is used as the DC-DC cell in the proposed single-stage design. Moreover, the flyback and forward sub-converters are designed to operate in CCM and DCM, respectively. The design objective is to deactivate the flyback sub-converter and keep the forward sub-converter provid-

ing the output power when the converter operates in the light load condition. Thus, it is possible to achieve high conversion efficiency in the heavy load condition and suppress the bulk capacitor voltage stress in the light load condition.

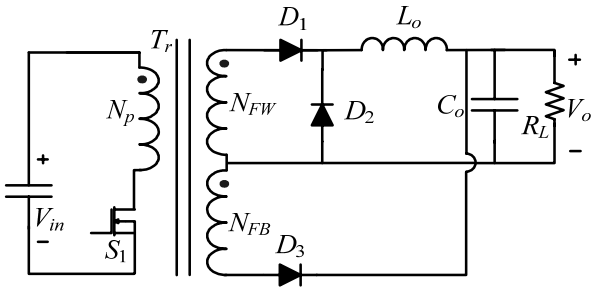


Fig. 4.1 Basic flyback-forward converter [52].

4.1.2 Circuit Configuration

Fig. 4.2 shows the circuit configuration of the proposed single-stage AC-DC converter. This converter is derived from a center-tapped flyback-forward converter with the addition of the auxiliary circuit. The auxiliary circuit forms the ICS cell and the center-tapped flyback-forward converter forms the DC-DC cell. In the proposed converter, a multi-winding transformer T_r is employed. It includes four windings N_1, N_2, N_3, and N_4 with turns number n_1, n_2, n_3, and n_4, respectively, and the primary magnetizing inductance L_m. As marked by the shaded area in Fig. 4.2, the ICS circuit, consisting of the rectifier diode D_1, boost inductor L_b, and auxiliary winding N_1, is inserted between the full-bridge rectifier D_r and the bulk capacitor C_b. The purpose of this circuit is to force the boost inductor current to be discontinuous and AC modulated to achieve inherent PFC. The diode D_1 is used to provide fast rectification and prevent the filter capacitor C_{in} from being charged by the reverse current of i_{Lb}. Different from the conventional ICS schemes, bulk capacitor C_b is intentionally connected to the undotted end of winding N_1. Through the winding N_1 with enough large turns, the coupled voltage $-V_o \cdot n_1/n_4$ across winding N_1 can force to charge L_b during the duty-off time. Therefore, the current stress of the main switch S_1 in the duty-on time can be reduced.

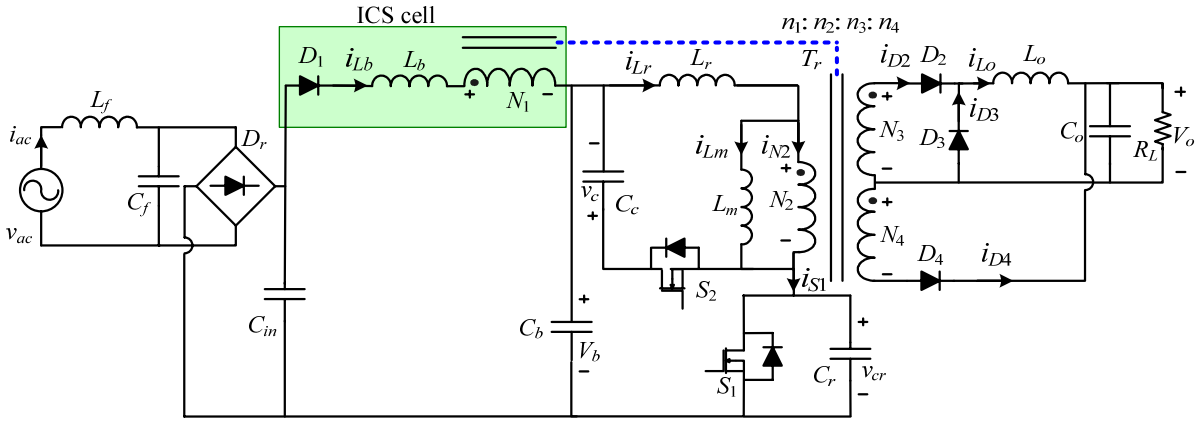


Fig. 4.2 Proposed single-stage soft-switching AC-DC converter.

The ICS cell is then followed by an active-clamp flyback-forward circuit which provides isolation and post-regulation function. C_r represents the sum of the parasitic capacitances contributed by main switch S_1 and auxiliary switch S_2. L_r represents the sum of the transformer leakage inductance and an external inductor, which forms a series resonant circuit with C_r to enable soft-switching function. The resonant inductor L_r, the clamping capacitor C_c, and the auxiliary switch S_2 form the main part of the active-clamp circuit for limiting the turn-off voltage spike of S_1. The combination of forward (primary and upper secondary of T_r) and flyback (primary and lower secondary of T_r) circuits in a single unit by using a center-tapped transformer ensures that the energy is always transferred to the load even when the main switch S_1 is turned off. Moreover, with the use of transformer T_r, the magnetization energy stored in L_m is split into two portions in duty-off time. One portion is directly delivered to the output load by the flyback sub-converter; the rest is delivered to the auxiliary winding N_1 for generating i_{Lb} and charging the bulk capacitor C_b. In addition, the flyback sub-converter is designed to operate in CCM for providing a reflected voltage v_{N1} from the output voltage during the duty-off time. The forward sub-converter is designed to operate in DCM all the time even in light load condition while the flyback sub-converter is deactivated. Furthermore, the control circuit can be implemented by a simple control loop, a common PWM controller, and a driver circuit.

4.1.3 Principle of Operation

To simplify the analysis, the following assumptions are made:

(i) The switching and conduction losses of the components are neglected;

(ii) The rectified line voltage $|v_{ac}|$ is considered constant during a switching period;

(iii) The bulk capacitor voltage V_b and the output capacitor voltage V_o are ripple-free DC in each half of a line cycle;

(iv) The leakage inductances of the transformer are neglected.

In each half line cycle, the converter has two operation modes, M_1 and M_2, as shown in Fig. 4.3. In mode M_1, the rectified line voltage $|v_{ac}|$ is lower than $V_b - V_o \cdot n_1/n_4$; thus, diode D_1 is reverse biased and no line current I_{ac} is formed. In this circumstance, the converter simply operates as an active-clamp flyback-forward DC-DC converter. While $|v_{ac}|$ is higher than $V_b - V_o \cdot n_1/n_4$, the converter operates in mode M_2, in which L_b can provide the voltage-boost function and thus the line current is established. From the definition of operation modes, the boundary angle θ_b between modes M_1 and M_2 can be obtained as

$$\theta_b = \sin^{-1}\left(\frac{V_b - V_o \cdot n_1/n_4}{\left|V_{ac(pk)}\right|}\right) \tag{4.1}$$

Furthermore, Fig. 4.4 illustrates that the topological states of the converter during one switching period. Referring to the symbol definitions, topological states, and key waveforms shown in Figs. 4.2, 4.4, and 4.5, respectively, the detailed operation is explained as follows.

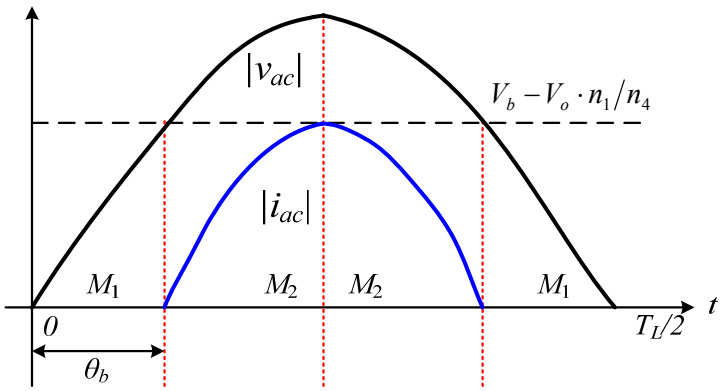


Fig. 4.3 Operation modes in a half line cycle.

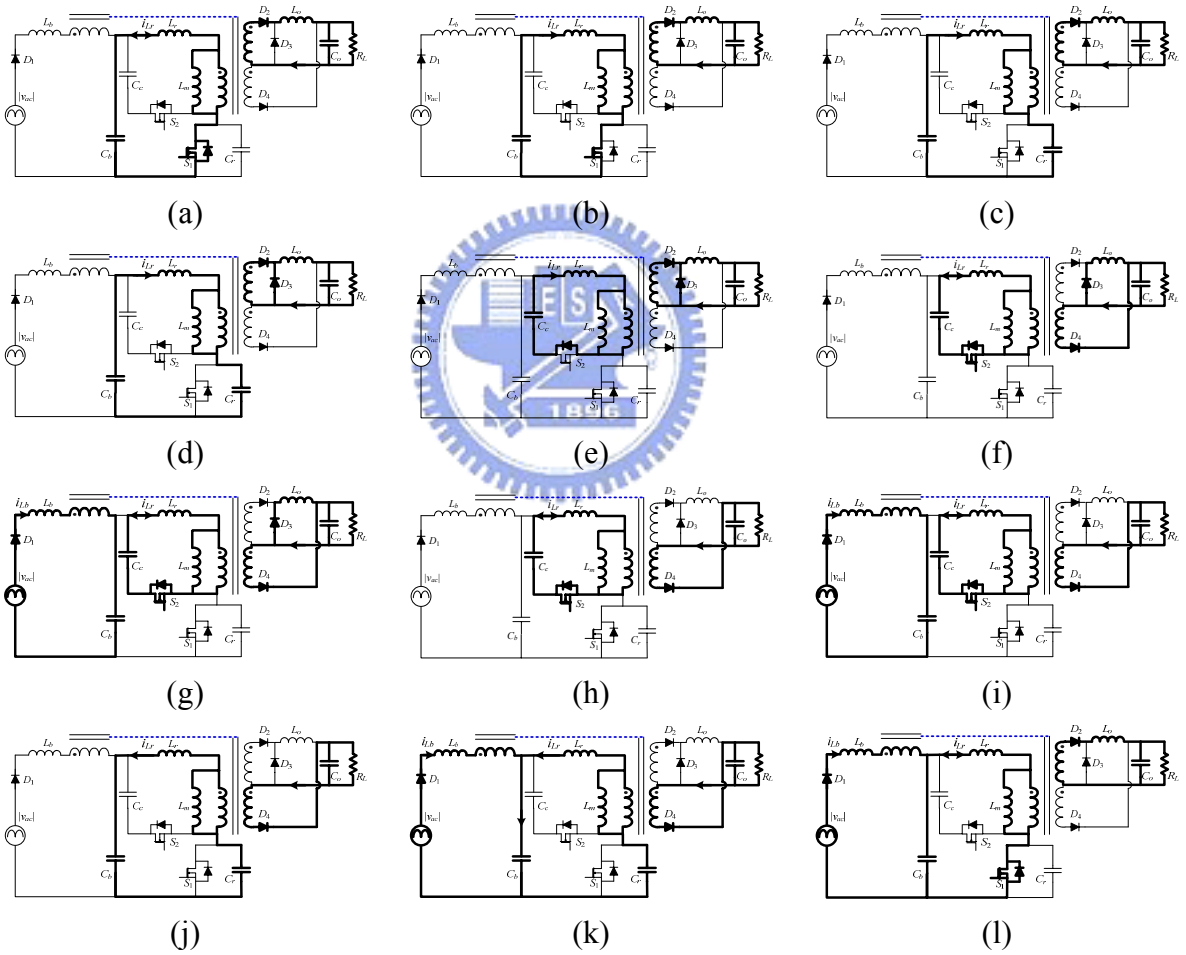


Fig. 4.4 Topological states of the proposed converter: (a) State 1 for mode M_1, (b) State 1 for mode M_2, (c) State 2, (d) State 3, (e) State 4, (f) State 5 for mode M_1, (g) State 5 for mode M_2, (h) State 6 for mode M_1, (i) State 6 for mode M_2, (j) State 7 for mode M_1, (k) State 7 for mode M_2, and (l) State 8.

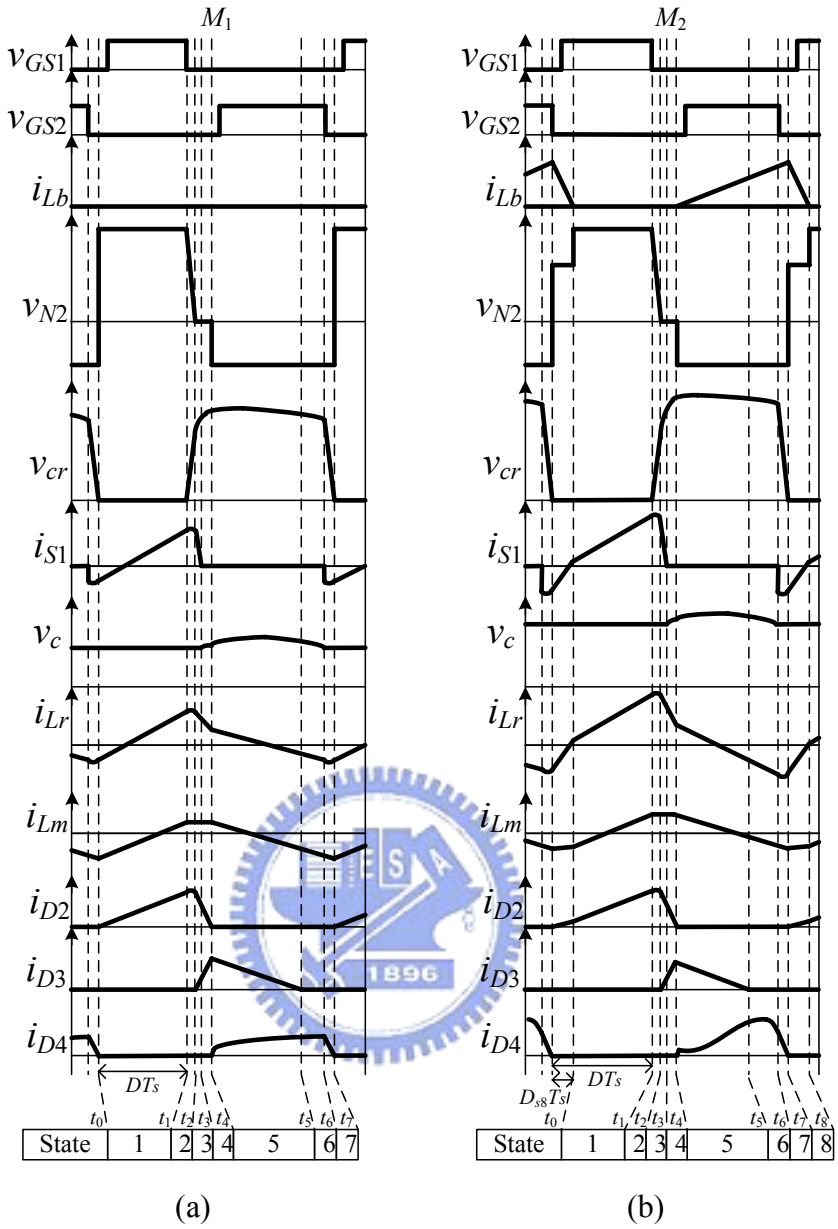


Fig. 4.5 Steady-state waveforms of the proposed converter in (a) mode M_1 and (b) mode M_2.

State 1 [Fig. 4.4(a) or 4.4(b), $t_0 \le t < t_1$]:

In this state, switch S_1 is on and switch S_2 is off. From KVL, the bulk capacitor voltage V_b equals the sum of the voltage across resonant inductor L_r and the voltage across the primary winding N_2. The positive voltage across winding N_2 induces a positive voltage across the secondary winding N_3. Thus, the output inductor current flows through the diode D_2 and diodes D_3 and D_4 are reverse biased. Since V_b is approximately constant, both the magnetizing

inductance L_m and resonant inductor L_r are linearly magnetized. The voltage and current at the transformer primary side can be obtained as

$$v_{N2,t0} = \frac{\frac{V_b}{L_r} + \frac{n_3}{n_2}\frac{V_o}{L_o}}{\frac{1}{L_r} + \frac{1}{L_m} + \left(\frac{n_3}{n_2}\right)^2 \frac{1}{L_o}} \tag{4.2}$$

$$i_{Lr}(t) = i_{Lm}(t_0) + \frac{v_{N2,t0}}{L_m}\cdot(t-t_0) + \frac{n_3}{n_2}\cdot\left(i_{Lo}(t_0) + \frac{v_{N2,t0}\cdot n_3/n_2 - V_o}{L_o}\cdot(t-t_0)\right) \tag{4.3}$$

where

$$i_{Lo,M1}(t_0) = 0 \tag{4.4}$$

$$i_{Lo,M2}(t_0) = \frac{v_{N2,t7}\cdot n_3/n_2 - V_o}{L_o}\cdot D_{s8}T_s\,. \tag{4.5}$$

where $D_{s8}T_s$,equal to (t_8–t_7), is the duration occupied by State 8. The derivation of (4.2) is shown in Appendix E. In this state, since the large positive voltage presents across winding N_1, no current flows through L_b.

State 2 [Fig. 4.4(c), $t_1 \le t < t_2$]:

At t_1, S_1 is turned off. The resonant capacitance C_r is charged by the primary current i_{Lr}. Since C_r is very small, v_{Cr} rises almost linearly from 0 to V_b in a short time.

State 3 [Fig. 4.4(d), $t_2 \le t < t_3$]:

At t_2, v_{Cr} rises to a high value that makes the primary side voltage v_{N2} equal zero. Thus, the secondary side diodes D_2 and D_3 conduct and the output inductor current is decreasing linearly. The resonant tank in this state consists of L_r and C_r. Solving the resonant network gives the current and voltage as

$$i_{Lr}(t) = i_{Lr}(t_2)\cdot\cos(\omega_1(t-t_2)) - \frac{v_{cr}(t_2)}{Z_1}\cdot\sin(\omega_1(t-t_2)) \tag{4.6}$$

$$v_{cr}(t) = V_b - (V_b - v_c(t_2))\cdot\cos(\omega_1(t-t_2)) + i_{Lr}(t_2)Z_1\cdot\sin(\omega_1(t-t_2)) \tag{4.7}$$

where $\omega_1 = 1/\sqrt{L_rC_r}$, $Z_1 = \sqrt{L_r/C_r}$.

State 4 [Fig. 4.4(e), $t_3 \le t < t_4$]:

At t_3, v_{Cr} rises to a value that makes the body diode of S_2 conduct. Since the clamp capacitor C_c is much greater than the resonant capacitor C_r, the resonant tank primarily consists of L_r and C_c. Solving the resonant network yields

$$i_{Lr}(t) = i_{Lr}(t_3)\cdot\cos(\omega_2(t-t_3)) - \frac{v_c(t_3)}{Z_2}\cdot\sin(\omega_2(t-t_3)) \tag{4.8}$$

$$v_c(t) = v_c(t_3)\cdot\cos(\omega_2(t-t_3)) + i_{Lr}(t_3)Z_2\cdot\sin(\omega_2(t-t_3)) \tag{4.9}$$

where $\omega_2 = 1/\sqrt{L_r C_c}$, $Z_2 = \sqrt{L_r/C_c}$. Furthermore, the increase of v_{Cr} causes i_{Lr} to decrease. Consequently, the diode current i_{D2} keeps decreasing till $i_{D2} = 0$ and contrarily the diode current i_{D3} increases until $i_{D3} = i_{Lo}$. Before i_{D2} decreases to zero, the primary side voltage v_{N2} is still kept zero value.

State 5 [Fig. 4.4(f) or 4.4(g), $t_4 \le t < t_5$]:

At t_4, $i_{D2} = 0$ and $i_{D3} = i_{Lo}$. After time t_4, the fast varying current i_{Lr} decreases to a value that is smaller than i_{Lm}; thus, the winding current i_{N2} turns to negative. According to Ampere's law, the winding current i_{N4} will be induced correspondingly. The fact that diode D_4 conducts results in the voltage v_{N2} being clamped at $-V_o\cdot n_2/n_4$. Shortly, S_2 is turned on before i_{Lr} resonates to the negative direction; thus, ZVS of S_2 is achieved. The resonant tank is formed by L_r and C_c. The resonant inductor current and clamp capacitor voltage can be found as

$$i_{Lr}(t) = i_{Lr}(t_4)\cdot\cos(\omega_2(t-t_4)) + \frac{\frac{n_2}{n_4}V_o - v_c(t_4)}{Z_2}\cdot\sin(\omega_2(t-t_4)) \tag{4.10}$$

$$v_c(t) = \frac{n_2}{n_4}V_o - \left(\frac{n_2}{n_4}V_o - v_c(t_4)\right)\cdot\cos(\omega_2(t-t_4)) + i_{Lr}(t_3)Z_2\cdot\sin(\omega_2(t-t_4)). \tag{4.11}$$

Within this state, v_{N1} turns to negative. If the line voltage is greater than $V_b - V_o\cdot n_1/n_4$, i.e. in mode M_2 operation, the current i_{Lb} will be generated and is given by

$$i_{Lb}(t) = \frac{1}{L_b}\left(|v_{ac}(t)| + \frac{n_1}{n_4}V_o - V_b\right)\cdot(t-t_4). \tag{4.12}$$

In such a design, the winding N_1 also resets a partial energy stored in L_m to C_b. When i_{Lo} re-

duces to zero, this state is ended. Meanwhile, the DCM operation of L_o is achieved and D_2 and D_3 are reverse biased.

State 6 [Fig. 4.4(h) or 4.4(i), $t_5 \le t < t_6$]:

This circuit analysis in this state is the same as that in State 5 except the output inductor current is zero.

State 7 [Fig. 4.4(j) or 4.4(k), $t_6 \le t < t_7$]:

At t_6, S_2 is turned off. C_c is disconnected and L_r and C_r form a new high frequency resonant circuit. The transformer primary side current i_{Lr} resonates in the negative direction to discharge C_r; therefore, v_{Cr} decreases from $v_c(t_6)+V_b$ to zero and then v_{N2} turns to positive. At t_7, i_{D4} decreases to zero and after then D_4 becomes reverse biased. Since the down-slope of di_{D4}/dt is determined by the resonant speed, D_4 can be designed to switch softly to reduce the rectifier switching loss. The resonant inductor current and resonant capacitor voltage can be expressed as

$$i_{Lr}(t) = i_{Lr}(t_5)\cdot\cos(\omega_1(t-t_5)) + \frac{V_b + \frac{n_2}{n_4}V_o - v_{cr}(t_5)}{Z_1}\cdot\sin(\omega_1(t-t_5)) \tag{4.13}$$

$$v_{cr}(t) = V_b + \frac{n_2}{n_4}V_o - \left(V_b + \frac{n_2}{n_4}V_o - v_{cr}(t_5)\right)\cdot\cos(\omega_1(t-t_5)) + i_{Lr}(t_5)Z_1\cdot\sin(\omega_1(t-t_5)). \tag{4.14}$$

For the mode M_2 case, the current i_{Lb} is increasing linearly with the same slope as expressed in (4.12).

State 8 [Fig. 4.4(l), $t_7 \le t < t_8$]:

At t_7, the body diode of S_1 begins to conduct. Shortly after time t_7, while the body diode of S_1 is conducting, S_1 is turned on to achieve ZVS operation. Since $|v_{ac}|$ is smaller than $v_{N1}+V_b$, the boost inductor current i_{Lb} linearly decreases and becomes zero at time t_8 (= t_0). The above operation gives

$$i_{Lb}(t) = i_{Lb}(t_7) + \frac{|v_{ac}| - v_{N1,t7} - V_b}{L_b}\cdot(t-t_7) \tag{4.15}$$

where

$$v_{N1,t7}(t)=\frac{\frac{n_1\left(\left|v_{ac}(t)\right|-V_b\right)}{n_2L_b}+\frac{V_b}{L_r}+\frac{n_3V_o}{n_2L_o}}{\frac{L_r+L_m}{L_rL_m}+\left(\frac{n_1}{n_2}\right)^2\frac{1}{L_b}+\left(\frac{n_3}{n_2}\right)^2\frac{1}{L_o}}\cdot\frac{n_1}{n_2} \tag{4.16}$$

The derivation of (4.16) is shown in Appendix F. It is worth mentioning that the output power is fed directly from the line input by the utilization of winding N_1 in this state. In addition, when the converter operates in mode M_1, this state does not exist.

4.1.4 Steady-State Analysis

Based on the circuit analysis of the proposed converter introduced in the previous sub-section, States 2-4 and 7 can be neglected in the steady-state analysis because these four intervals are very short as compared with the total switching period. By employing the voltage-second balance across L_m, one can obtain the following equation.

$$v_{N2,t0}\cdot(D-D_{s8})-\frac{n_2}{n_4}V_o\cdot(1-D)+v_{N2,t7}\cdot D_{s8}=0. \tag{4.17}$$

Similarly, by employing the voltage-second balance across L_r and neglecting the small oscillation term of V_c, one can obtain

$$(V_b-v_{N2,t0})\cdot(D-D_{s8})-\left(V_c-\frac{n_2}{n_4}V_o\right)\cdot(1-D)+(V_b-v_{N2,t7})\cdot D_{s8}=0. \tag{4.18}$$

Also, the voltage-second balance across L_b gives

$$\left(\left|v_{ac}\right|+\frac{n_1}{n_4}V_o-V_b\right)\cdot(1-D)+\left(\left|v_{ac}\right|-\frac{n_1}{n_2}v_{N2,t7}-V_b\right)\cdot D_{s8}=0. \tag{4.19}$$

In mode M_1, since the D_{s8} does not exist, the duty ratio in mode M_1 can be obtained from (4.17):

$$D_{M1}=\frac{V_o}{v_{N2,t0}\cdot n_4/n_2+V_o}. \tag{4.20}$$

According to (4.19), the time function of D_{s8} in mode M_2 is obtained as

$$D_{s8}(t)=\frac{|v_{ac}(t)|+\frac{n_1}{n_4}V_o-V_b}{\frac{n_1}{n_2}v_{N2,t7}(t)+V_b-|v_{ac}(t)|}\cdot(1-D_{M2}(t)). \tag{4.21}$$

Adding (4.17) to (4.18), the clamp capacitor voltage can be expressed as

$$V_c=\frac{D}{1-D}V_b. \tag{4.22}$$

According to (4.18) and (4.21), the clamp capacitor voltage in mode M_2 can be further expressed as

$$v_{c,M2}(t)=\left[\frac{n_2}{n_4}V_o+\frac{|v_{ac}(t)|+\frac{n_1}{n_4}V_o-V_b}{\frac{n_1}{n_2}v_{N2,t7}(t)+V_b-|v_{ac}(t)|}\cdot(v_{N2,t0}(t)-v_{N2,t7}(t))\right]\cdot\frac{V_b}{v_{N2,t0}}. \tag{4.23}$$

Thus, from (4.22) and (4.23), the time function of the duty ratio in mode M_2 is given by

$$D_{M2}(t)=\frac{v_{c,M2}(t)}{V_b+v_{c,M2}(t)}. \tag{4.24}$$

So far, the steady-state analysis for the full load condition has been carried out. The steady-state analysis for the light load condition is then derived as follows.

When the output load decreases, the DC-DC cell of the proposed converter degenerates to an active-clamp forward circuit. Due to the DCM operation of L_o, one can obtain

$$\left(\frac{n_3}{n_2}v_{N2,t7}-V_o\right)\cdot D_{s8}+\left(\frac{n_3}{n_2}v_{N2,t0}-V_o\right)\cdot(D-D_{s8})=\frac{L_o i_{Lo(pk)}}{T_s}=\sqrt{\frac{2P_oL_o}{T_s}}. \tag{4.25}$$

where $i_{Lo(pk)}$ is the peak current of output inductor. By employing the voltage-second balance across L_m and neglecting the small oscillation term of v_{N2} in State 5, one can obtain the following equation.

$$v_{N2,t0}\cdot(D-D_{s8})+v_{N2,t4}\cdot(1-D)+v_{N2,t7}\cdot D_{s8}=0. \tag{4.26}$$

Similarly, the voltage-second balance across L_r gives

$$\left(V_b - v_{N2,t0}\right)\cdot\left(D - D_{s8}\right) - \left(V_c + v_{N2,t4}\right)\cdot\left(1 - D\right) + \left(V_b - v_{N2,t7}\right)\cdot D_{s8} = 0\,. \tag{4.27}$$

And the voltage-second balance across L_b gives

$$\left(\left|v_{ac}\right| - \frac{n_1}{n_2}v_{N2,t4} - V_b\right)\cdot\left(1 - D\right) + \left(\left|v_{ac}\right| - \frac{n_1}{n_2}v_{N2,t7} - V_b\right)\cdot D_{s8} = 0\,. \tag{4.28}$$

Adding (4.26) to (4.27), the clamp capacitor voltage can be found as (4.22). From (4.26), one can obtain

$$v_{N2,t4} = -\frac{v_{N2,t0}\cdot\left(D - D_{s8}\right) + v_{N2,t7}\cdot D_{s8}}{1 - D}\,. \tag{4.29}$$

According to (4.25), the duty ratio in mode M_2 is given by

$$D_{M2} = \frac{\sqrt{\frac{2P_oL_o}{T_s}} - \frac{n_3}{n_2}\cdot\left(v_{N2,t7} - v_{N2,t0}\right)\cdot D_{s8}}{\frac{n_3}{n_2}v_{N2,t0} - V_o}\,. \tag{4.30}$$

Substituting (4.29) and (4.30) into (4.28), D_{s8} can be obtained as

$$D_{s8} = \frac{\sqrt{\frac{2P_oL_o}{T_s}}\cdot\frac{\left|v_{ac}\right| - \frac{n_1}{n_2}v_{N2,t0} - V_b}{\frac{n_3}{n_2}v_{N2,t0} - V_o} - \left(\left|v_{ac}\right| - V_b\right)}{\left(v_{N2,t7} - v_{N2,t0}\right)\cdot\left[\frac{\frac{n_3}{n_2}\cdot\left(\left|v_{ac}\right| - \frac{n_1}{n_2}v_{N2,t0} - V_b\right)}{\frac{n_3}{n_2}v_{N2,t0} - V_o} + \frac{n_1}{n_2}\right] + \left(\left|v_{ac}\right| - \frac{n_1}{n_2}v_{N2,t7} - V_b\right)}\,. \tag{4.31}$$

4.2 Design Considerations

The design specifications of the proposed converter are given as follows: the input voltage range V_{ac} = 90–260 Vrms (60 Hz), output voltage V_o = 20 V, rated output power P_o = 100 W, and switching frequency f_s = 100 kHz. To maximize the conversion efficiency, the duty ratio range is designed to from 0.15 to 0.4. The conversion efficiency η is assumed to be 0.85.

With the consideration of the voltage limitation of a commercially available electrolytic capacitor, the maximum bulk capacitor voltage is needed to be kept below 450 V. Moreover,

according to the empirical rule, the moderate value of V_b usually ranges between 1.1 and 1.2 times as high as $V_{ac(pk)}$. However, when V_{ac} = 260 Vrms, the possible maximum value of V_b equals $260 \times \sqrt{2} \times 1.2 = 441$ and the value extremely approaches 450 V. Therefore, in the following design, the target maximum value of V_b, $V_{b,max}$, is chosen to be 1.15 time as high as $V_{ac(pk)}$ at 260 Vrms line input. To ensure the proposed converter operating properly, the converter parameters including n_2/n_3, n_2/n_4, n_1/n_4, L_r, L_m, L_o, and L_b are determined as follows.

(1) Determining the Turns Ratio n_2/n_3

Let $L_m >> L_r$, thus the voltage $v_{N2,t0}$ is approximated to be V_b. By using the voltage conversion ratio theory of the simple forward circuit operating in CCM, the primary to secondary turns ratio n_2/n_3 can be approximately expressed as

$$\frac{n_2}{n_3} = \frac{V_{b,\min} D_{\max}}{V_o}. \tag{4.32}$$

(2) Determining the Turns Ratio n_2/n_4

The proposed converter is designed to operate the forward sub-converter in DCM and flyback sub-converter in CCM. With this design, the bulk voltage can be easily suppressed in the worse case, i.e. the high line input with light load condition, by deactivating the flyback sub-converter. The above function can be achieved by manipulating the voltage of V_c. In the high line with light load case, since D becomes smaller, lower V_c and $-v_{N2}$ will be formed. Thus, the induced voltage across N_4, $-v_{N4}$, can be designed to be insufficient to forward bias D_4 so that the flyback sub-converter is deactivated. Based on the above concept, the following condition must be satisfied.

$$V_{c,\min} \cdot n_4 / n_2 < V_o . \tag{4.33}$$

By substituting (4.22) into (4.33), the ratio of n_2/n_4 can be found:

$$\frac{n_2}{n_4} = \frac{V_{b,\max}}{V_o} \cdot \frac{D_{\min}}{1 - D_{\min}}. \tag{4.34}$$

(3) Determining the Turns Ratio n_1/n_4

The design objective of determining n_1/n_4 is to find its minimum value with which the input current harmonics can meet the IEC 61000-3-2 Class D requirements. According to (4.1), the selection of n_1/n_4 is equivalent to the selection of the boundary angle. Thus, the design objective becomes finding the maximum acceptable boundary angle. Since IEC 61000-3-2 Class D gives the requirements of the acceptable harmonics, to find the maximum acceptable boundary angle, each input current harmonic should be computed. Since the line current is an analogous sinusoid waveform, the line current during $[\theta_b, \pi-\theta_b]$ can be expressed as

$$i_{ac}(\omega t) = i_{ac}\left(\frac{\pi}{2}\right) \cdot \sin\left((\omega t - \theta_b) \cdot \frac{\pi}{\pi - 2\theta_b}\right) \tag{4.35}$$

where ω is the angular frequency of the line voltage. Thus, the nth harmonic component I_n can be calculated by Fourier analysis:

$$\begin{aligned} I_n = \frac{\pi - 2\theta_b}{\pi} \cdot i_{ac}\left(\frac{\pi}{2}\right) \cdot \Bigg\{ & \left[\sin\left((n-1)\pi - n\theta_b\right) - \sin\left(n\theta_b\right)\right] \cdot \frac{1}{(n-1)\pi - 2n\theta_b} \\ & - \left[\sin\left((n+1)\pi - n\theta_b\right) - \sin\left(n\theta_b\right)\right] \cdot \frac{1}{(n+1)\pi - 2n\theta_b} \Bigg\} \end{aligned} \tag{4.36}$$

where n = 1, 3, 5...39. Since the Class D limits are defined as the ratio of the current harmonic to fundamental-frequency component, I_n/I_1. From (4.36), we can obtain the normalized value of each harmonic as a function of the boundary angle as drawn in Fig. 3.10. Fig. 3.10 shows that the most critical harmonic is the fifth for complying with the Class D requirements since its acceptable boundary angle is smaller than all the others. Therefore, the maximum allowable boundary angle is 1.005 rad (= 57.58°). Next, the turns ratio n_1/n_4 can be obtained by rearranging (4.1):

$$\frac{n_1}{n_4} = \frac{V_b - V_{ac(pk)} \sin\theta_b}{V_o}. \tag{4.37}$$

In the proposed converter, a higher line input voltage causes a larger boundary angle. Thus, we must make sure that the design satisfies the requirements of the Class D especially at the nominal high line input, that is 230 Vrms. Substituting $V_b = 1.15 \cdot V_{ac(\mathrm{pk})}$ in (4.37), we obtain $n_1/n_4 = 4.97$ when $V_{ac} = 230$ Vrms and $\theta_b = 1.005$ rad. In other words, $n_1/n_3 = 4.97$ is the boundary of compliance with Class D limits.

(4) Determining the Resonant Inductor L_r

According to the operating principle of State 7, to ensure the ZVS turn-on for S_1, the energy stored in the resonant inductor L_r must be greater than the energy stored in the resonant capacitor C_r. Thus, for the given C_r contributed by the parasitic capacitances of S_1 and S_2, the following relationship should be guaranteed.

$$L_r > \frac{C_r \cdot \left(V_{b,\max} + \frac{n_2}{n_4} V_o \right)^2}{\left(i_{s1,M1}(t_6) \right)^2}. \tag{4.38}$$

(5) Determining the Transformer Primary Magnetizing Inductance L_m

With the design consideration that the flyback sub-converter is deactivated at high line and light load condition, the output power provided by the sub-converter at 260 Vrms and full load situation is designed to be lower than $P_o/2$. Meanwhile, this sub-converter is designed to always operate in CCM at full load. Thus, the inductance L_m must satisfy the following condition:

$$L_m > \frac{\left((1 - D_{\min}) \cdot V_o\right)^2 \cdot \eta}{f_s P_o} \cdot \left(\frac{n_2}{n_4} \right)^2. \tag{4.39}$$

(6) Determining the Output Inductor L_o

According to the design criterion mentioned above, the output power provided by the forward sub-converter at 260 Vrms should be greater than $P_o/2$. To fulfill this design and ensure that L_o always operates in DCM, the following relationship should be guaranteed.

$$L_o < \min\left(\frac{D_{\min}^2 T_s \eta}{P_o} \cdot \left(V_{b,\max} \frac{L_m}{L_m + L_r} \cdot \frac{n_3}{n_2} - V_o \right)^2, \frac{\frac{n_3}{n_2} V_o \cdot \left(\frac{1 - D_{\max}}{D_{\max}} \right)}{\frac{V_{b,\min}}{L_r} - \frac{n_2 V_o}{n_3 D_{\max}} \left(\frac{1}{L_m} + \frac{1}{L_r} \right)} \right). \tag{4.40}$$

(7) Determining the Boost Inductor L_b

To achieve the self-PFC property, the boost inductor must operate in DCM over the entire line cycle. Thus, the design must satisfy the condition of $D_{s8} < D$ in the whole line cycle. Since the critical boundary condition of CCM and DCM occurs at the lowest peak input voltage, the maximum boost inductance can be determined from (4.21):

$$L_{b,\max} = \frac{\frac{n_1}{n_2} \cdot \left(\frac{1 - D_{\max}}{D_{\max}} \right) \cdot \left(V_{ac(pk),\min} - V_{b,\min} + \frac{n_1}{n_4} V_o \right)}{\frac{V_{b,\min}}{L_r} + \frac{n_3 V_o}{n_2 L_o} - \frac{n_2}{n_1 D_{\max}} \left[V_{ac(pk),\min} - V_{b,\min} + \frac{n_1}{n_4} V_o (1 - D_{\max}) \left(\frac{L_r + L_m}{L_r L_m} + \left(\frac{n_3}{n_2} \right)^2 \frac{1}{L_o} \right) \right]}. \tag{4.41}$$

(8) Determining the clamp capacitor C_c

The determination of C_c is the same as that of the conventional active-clamp flyback converter. That is to say, the resonant frequency determined by C_c and L_r should be sufficiently low so that the half resonant period $\pi\sqrt{L_r C_c}$ is greater than the duty-off time. Thus, the minimum value of C_c can be obtained as:

$$C_c > \frac{\left((1 - D_{\min}) \cdot T_s \right)^2}{\pi^2 L_r}. \tag{4.42}$$

Based on equations (4.32) to (4.42), we choose the desired circuit parameters as follows:

the turns of $n_1/n_2/n_3/n_4$ = 35/24/9/7, L_r = 15 μH, L_m = 329 μH, L_o = 20 μH, L_b = 105 μH, and C_c = 0.6 μF.

4.3 Mechanism for Suppressing Bulk Capacitor Voltage Stress

To clarify the mechanism for suppressing bulk capacitor voltage stress in the proposed converter, the analysis of the boost inductor currents at heavy load and light load is performed as follows. Fig. 4.6 shows the relation of both the duty-on time change of S_1 and the boost inductor current change in a switching period under the load variation. At the rated condition, both the forward and flyback sub-converters work normally. Therefore, the boost inductor is charged by the voltage $|v_{ac}| + V_o \cdot n_1/n_4 - V_b$ since the voltage v_{N1} is reflected from the output side during the duty-off time, as shown by the dashed lines of Fig. 4.6. When the load decreases, the bulk capacitor voltage increases due to the power imbalance between the input and output. Meanwhile, the duty ratio decreases correspondingly to keep the constant output voltage in CCM operation. When the load decreases further, the reduced clamp capacitor voltage V_c caused by the decreased duty ratio can not induce the voltage $-v_{N4}$ higher enough to forward bias D_4. Thus, the flyback sub-converter is deactivated and only the forward sub-converter keeps supplying the output power. In this condition, the voltage v_{N1} is reflected from the clamp capacitor voltage instead of the output voltage. Therefore, the boost inductor L_b is charged by the approximate voltage of $|v_{ac}| + V_c \cdot n_1/n_2 - V_b$, as shown by the solid lines of Fig. 4.6, where V_c is determined by the duty ratio as shown in (4.22). Since the value of $V_c \cdot n_1/n_2$ is smaller than that of $V_o \cdot n_1/n_4$, the solid triangle will have a small area and a reduced boost inductor current is produced. With the proper arrangement of turns ratios between N_1, N_2, and N_4, the reduced quantity of input current can yield the result that V_b is suppressed at light load.

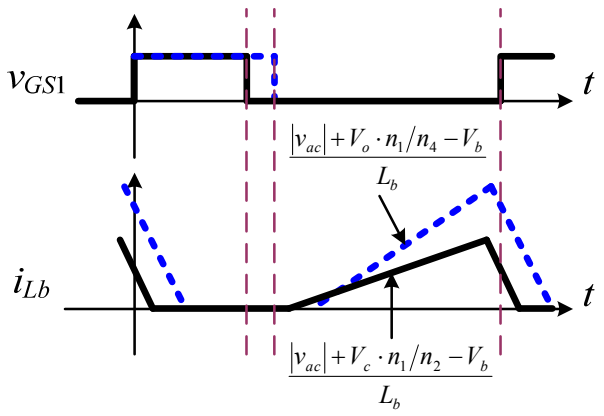


Fig. 4.6 The gate voltage of S_1 and the boost inductor current for different loads.

To examine the effect of suppressing the voltage stress on the bulk capacitor, it is intuitional to calculate the value of V_b. In steady state, the energy absorbed by the converter should be equal to the output energy, the bulk capacitor voltages at full and light loads can be expressed as shown in (4.43) and (4.44), respectively.

$$2\int_{\theta_b}^{\frac{\pi}{2}}|v_{ac}(t)|\cdot\frac{|v_{ac}(t)|+\frac{n_1}{n_4}V_o-V_b}{2L_b}\cdot(1-D_{M2})T_s\cdot(1-D_{M2}+D')dt=\frac{P_oT_L}{2} \tag{4.43}$$

$$2\int_{\theta_b}^{\frac{\pi}{2}}|v_{ac}(t)|\cdot\frac{|v_{ac}(t)|+V_b\frac{n_1}{n_2}\cdot\frac{D_{M2}}{1-D_{M2}}-V_b}{2L_b}\cdot(1-D_{M2})T_s\cdot(1-D_{M2}+D')dt=\frac{P_oT_L}{2} \tag{4.44}$$

where T_L is the line period. However, the values of V_b in (4.43) and (4.44) cannot be solved analytically. Thus, instead of directly calculating the value of V_b, we examine the change of input power under load variation. Fig. 4.7 shows the variations of instantaneous input power for different load conditions under the assumption of constant bulk capacitor voltage. These curves are sketched by using the parameters obtained in Section 4.2 for V_{ac} = 260 Vrms and $V_b = 1.15 \cdot V_{ac(pk)}$. From Fig. 4.7, it can be seen that the input power always decreases as the load is reduced. After the calculation, the change rate of $\Delta P_{in(ave)}/\Delta P_{o(ave)}$ can be obtained as 1.06 when the load is changed from I_o to (3/4)I_o, and the value of $\Delta P_{in(ave)}/\Delta P_{o(ave)}$ is 2.55

when the load is changed from (3/4)I_o to (1/2)I_o. Since the reduction amount of $P_{in(ave)}$ is greater than that of $P_{o(ave)}$, the actual bulk capacitor voltage must decrease to maintain the input and output average power balance. Meanwhile, the actual bulk capacitor voltage has a gradual decrease with the reduction of load current.

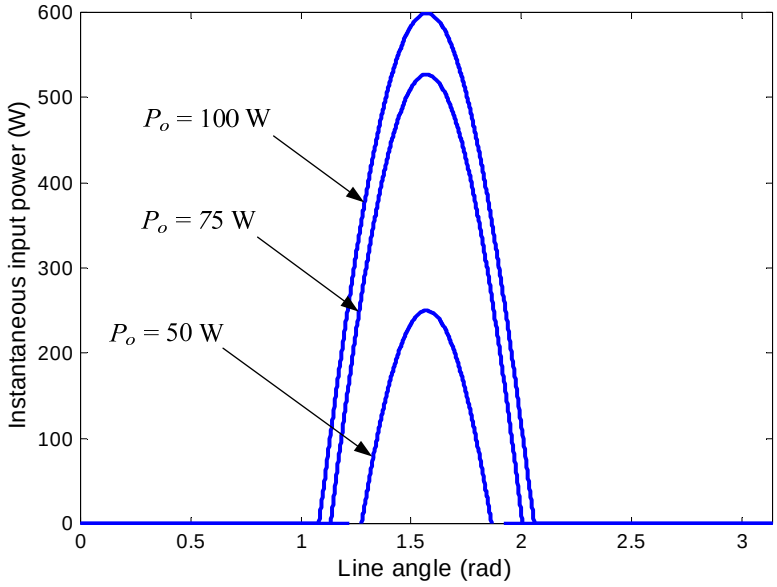


Fig. 4.7 The variations of instantaneous input power for different loads.

4.4 Analysis of the Line Current Waveform

To investigate the line current waveform drawn by the proposed converter, the input i-v characteristic curves should be examined. As shown in Fig. 4.2, since the low pass filter L_f–C_f will filter out the switching frequency components and harmonics of i_{Lb}, the rectified line current $|i_{ac}(t)|$ mathematically approximates to the average value of $i_{Lb}(t)$ within a switching period, namely, $|i_{ac}| = i_{Lb,ch(ave)} + i_{Lb,dis(ave)}$. By using (4.12), (4.15), (4.21), (4.23), and (4.24), the expressions of $i_{Lb,ch(ave)}$ and $i_{Lb,dis(ave)}$ can be calculated as follows:

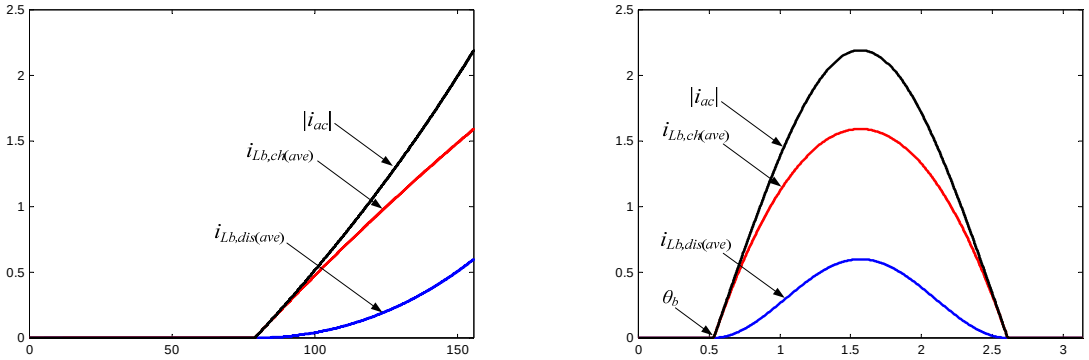
$$i_{Lb,ch(ave)}(t) = \frac{(1-D_{M2}(t))^2 T_s}{2L_b} \cdot \left(|v_{ac}(t)| + \frac{n_1}{n_4} V_o - V_b \right) \tag{4.45}$$

$$i_{Lb,dis(ave)}(t)=\frac{(1-D_{M2}(t))^2 T_s}{2L_b}\cdot\frac{\left(|v_{ac}(t)|+\frac{n_1}{n_4}V_o-V_b\right)^2\cdot\left[\frac{L_r+L_m}{L_rL_m}+\left(\frac{n_1}{n_2}\right)^2\cdot\frac{1}{L_b}+\left(\frac{n_3}{n_2}\right)^2\cdot\frac{1}{L_o}\right]}{\frac{n_1V_b}{n_2L_r}+\frac{n_1n_3V_o}{n_2^2L_o}+\left[\frac{L_r+L_m}{L_rL_m}+\left(\frac{n_3}{n_2}\right)^2\cdot\frac{1}{L_o}\right]\cdot\left(V_b-|v_{ac}(t)|\right)}. \quad (4.46)$$

With the computation of (4.45) and (4.46), $i_{Lb,ch(ave)}$, $i_{Lb,dis(ave)}$, and $|i_{ac}|$ in a half line cycle can be obtained as plotted in Fig. 4.8. Moreover, based on (4.20), (4.21) and (4.24), the curves of $(1-D)$ and D_{s5} can be drawn in Fig. 4.9. These curves are sketched by using the parameters obtained in Section 4.2 for V_{ac} = 110 Vrms and V_b = 1.15 · $V_{ac(pk)}$. According to (4.15), when $|v_{ac}(t)|$ increases, the discharging voltage across L_b decreases. Thus, D_{s8} increases correspondingly as shown in Fig. 4.9. Moreover, the charging voltage of energy-storage inductor, i.e. L_m or L_o, in the $D_{s8}T_s$ duration is smaller than that in the $(D-D_{s8})T_s$ duration, as illustrated in Fig. 4.5. Smaller charging voltage produces less magnetizing energy injected in energy-storage inductors and consequently lower output voltage is formed. To maintain the constant output voltage, the controller will increase the duty ratio D under output voltage feedback control. Thus, (1–D) will decreases with the increase of instantaneous rectified line voltage, as shown in Fig. 4.9. From the above result and (4.45), it can be found that the AC modulation effect on (1–D) makes $i_{Lb,ch(ave)}(t)$ convexly vary with $|v_{ac}(t)|$, as shown in Fig. 4.8(a). Thus, the waveform of $i_{Lb,ch(ave)}$ can compensate the line current distortion caused by $i_{Lb,dis(ave)}$. Although the slope of i_{ac}-v_{ac} curve is not definitely constant and still consists of small high order terms, the second derivative $\partial i_{ac}^2/\partial^2 v_{ac}$ is small and ranges between -2.2×10^{-4} and 5.5×10^{-4}. This result shows that the relationship between $|i_{ac}|$ and $|v_{ac}|$ is nearly linear and can be expressed as

$$|i_{ac}|=\frac{\left(|v_{ac}|-V_b+V_o\cdot n_1/n_4\right)}{R_{eq}}+\text{negligible nonlinear terms} \quad (4.47)$$

where R_{eq} is the equivalent input resistance. The linear result can be seen clearly from Fig. 4.8.



(a) (b)

Fig. 4.8 Comparison of $i_{Lb,ch(ave)}$, $i_{Lb,dis(ave)}$, and $|i_{ac}|$ drawn by the proposed converter in a half line cycle at 110 Vrms: (a) the currents as a function of instantaneous line voltage and (b) the current waveforms as a function of line angle.

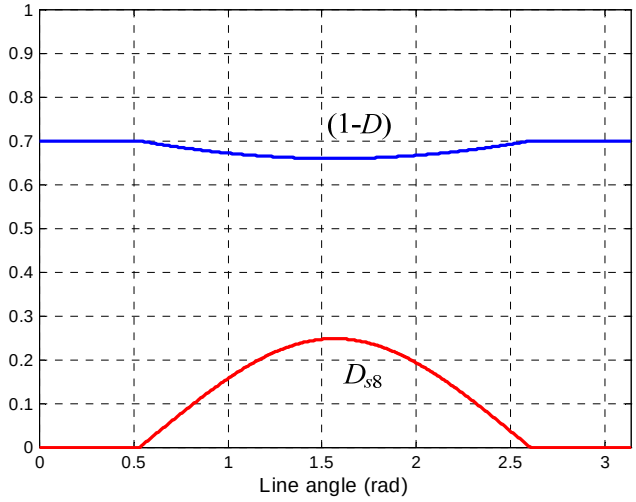


Fig. 4.9 $(1-D)$ and D_{s8} versus line angle for 110 Vrms in a half line cycle.

4.5 Experimental Results

To verify the feasibility and performance of the proposed topology, experimental tests were performed under the specifications described in Section 4.2. The circuit components used for the experiment are listed in Table 4.1.

Fig. 4.10 shows the measured line voltage and line current waveforms at V_{ac} = 110 Vrms.

It can be seen that the current waveform has a near-sinusoidal shape in mode M_2. Fig. 4.11 shows that the detailed current harmonics measured from the experimental prototype operating in the nominal high and low line inputs both can satisfy the requirements of IEC 61000-3-2 Class D. Fig. 4.12 shows that the conversion efficiency at full load is 87–91.3%. Fig. 4.13 shows that the bulk capacitor voltages are maintained within a desirable range (1.1–1.2 times as high as the peak line voltage) for the universal line voltage range (90–260 Vrms). Fig. 4.14 shows the bulk capacitor voltages with load variation at 260 Vrms line input. The measured data indicate that the maximum bulk capacitor voltage is 418 V, so the commercially available 450V-rated capacitor can be used safely.

Table 4.1 Component values for the prototype circuit

Component	Device Description
S_1, S_2	SPA11N60C3
D_1	U08A100
D_2, D_3, D_4	U08A20C
L_b	105 μH
L_r	15 μH
L_m	329 μH
L_o	20 μH
n_1: n_2: n_3: n_4	35: 24: 9: 7
C_b	300 μF/450 V
C_r	780 pF
C_c	0.6 μF/400 V
C_o	2000 μF/50 V
PWM controller	UC3843
High-side switch driver	IR2110

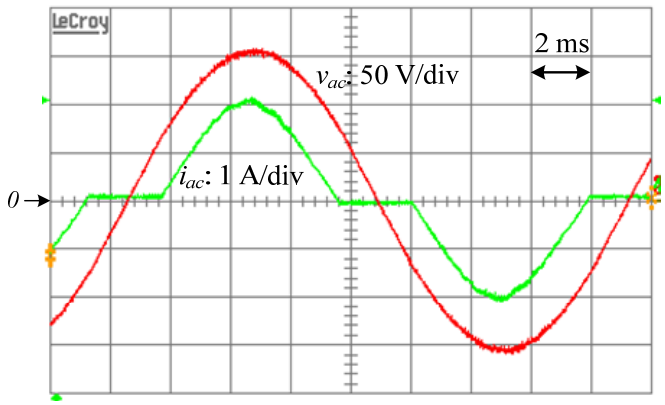


Fig. 4.10 Measured line voltage and current waveforms at V_{ac} = 110 Vrms and full load.

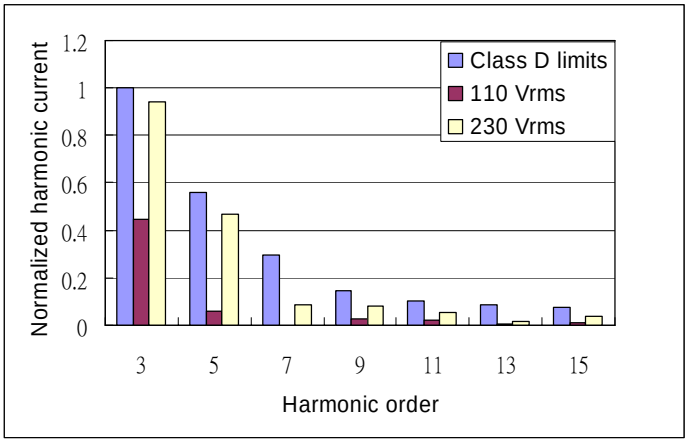


Fig. 4.11 Measured line current harmonics comparison at full load.

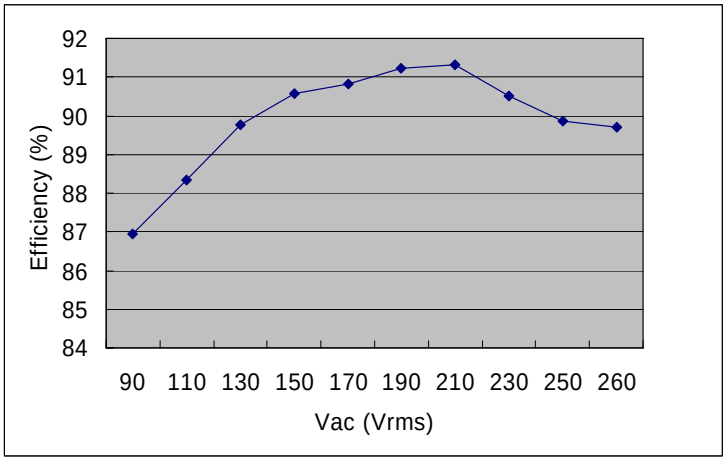


Fig. 4.12 Conversion efficiency versus input voltage.

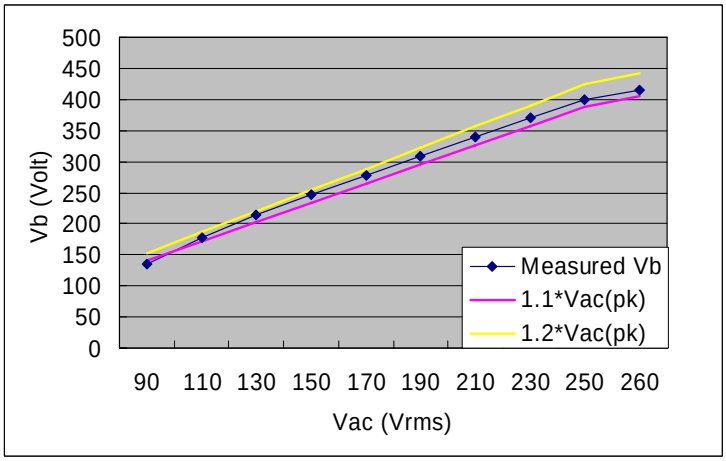


Fig. 4.13 Bulk capacitor voltage versus input voltage.

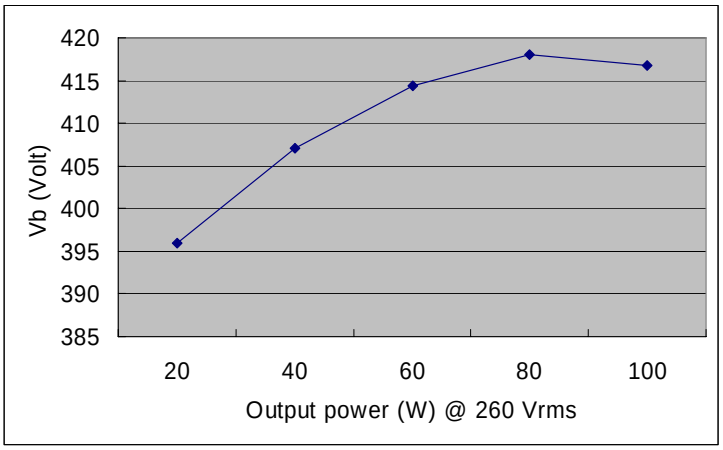


Fig. 4.14 Bulk capacitor voltage versus output power at 260 Vrms line input.

4.6 Concluding Remarks

In this chapter, a novel S^2ICS AC-DC converter for universal line and wide load range applications has been proposed based on an active-clamp flyback-forward topology. The ICS scheme is the two-terminal implementation of that proposed in Chapter 3. By employing the proposed ICS technique, two key advantages are obtained. First, during the duty-on time, the current stress across the main switch is alleviated. Second, the fact that the effective duty ratio of the ICS cell, $(1-D)$, is modulated by the instantaneous line voltage results in a better linear relationship between the line current and voltage through the conduction interval. Moreover, by the intentional arrangement of deactivating the flyback sub-converter of the DC-DC cell at light load, the voltage stress across C_b is suppressed effectively because only the DCM forward sub-converter is operated and the slope of the boost inductor charging current is adjusted by the duty ratio.

Experimental results show that the maximum bulk capacitor voltage is 418 V in a wide range of output load at 260 Vrms line input. Owing to the ability to keep V_b below a desirable value (V_b < 450 V) under wide line and load variations, the proposed converter is very suitable for the universal line voltage applications.

CHAPTER 5

CONCLUSIONS AND SUGGESTIONS FOR FURTHUR WORK

5.1 Conclusions

The original S^2ICS concept comes from the integration of the DCM boost rectifier and PWM DC-DC converter by using one common switch. Thus, conventional S^2ICS converters usually suffer from the relatively high switch current stress and line current waveform distortion caused by the voltage-follower control. To obtain better performance and achieve the cost-effective objective simultaneously, this dissertation explores advanced techniques for S^2ICS AC-DC converters.

First, a novel ICS technique for single-stage AC-DC converters is introduced. Unlike the conventional single-stage designs, the proposed ICS scheme is intentionally arranged to be charged in the duty-off time. With this design, the switch current stress in the duty-on time is significantly reduced and accordingly the power loss is reduced. Moreover, this design produces AC modulation effect on the charging time of the ICS cell so that the waveforms of the average charging current and average discharging current of the boost inductor can compensate each other automatically. Consequently, the input i-v curve has nearly linear relationship.

The proposed ICS scheme is then employed in an active-clamp DC-DC converter. In the flyback-type implementation, the resonant inductor L_r is arranged in the charging path of the boost inductor L_b so that L_r and L_b can provide the voltage-boost function together. Therefore, a small inductance for L_b is sufficient to achieve the DCM operation and the size reduction of magnetic material is allowable. Moreover, by programming the turns ratio between the additional and secondary windings, the proposed converter can be guaranteed to comply with the IEC 61000-3-2 Class D specifications at as high efficiency as possible. Meanwhile, the bulk

capacitor voltages can be maintained within a desirable range, 1.1–1.2 times of the peak line voltage, even though the converter operates in a wide range of input voltage, 90–260 Vrms. Experimental results have demonstrated the proposed line current correction function by a well shaped current waveform and the low current harmonics complying with requirements of IEC 61000-3-2 Class D. Furthermore, the high conversion efficiency around 90% has verified the effectiveness of the switch current stress alleviation and soft-switching function. In addition, by saving the boost inductor, a refined topology can be obtained, which is suitable for narrow input voltage (90–135 Vrms or 180–260 Vrms) and higher power density applications.

Another key issue of S^2ICS technique is the high bulk capacitor voltage stress. The bulk capacitor voltage V_b is not regulated and varies with the line voltage and the output load. To limit the bulk capacitor voltage stress below the tolerance of commercially available electrolytic capacitors, this dissertation proposes a novel S^2ICS AC-DC converter for universal line and wide load range applications based on an active-clamp flyback-forward topology. In the proposed topology, the flyback and forward sub-converters are operated in CCM and DCM, respectively, to achieve the hybrid operation mode with DCM while light load and CCM while heavy load. Thus, by deactivating the flyback sub-converter and keeping the forward sub-converter supplying the output power, the bulk capacitor voltage at light load condition can be suppressed effectively. Experimental results show that the maximum bulk capacitor voltage is 418 V in a wide range of output load at 260 Vrms line input. Moreover, owing to the center-tapped flyback-forward configuration, the energy is continuously transferred from the DC-DC cell to load irrespective of the state of main switch S_1. Hence, this converter can be adopted in the applications with high output current and/or high output power.

In conclusion, the dissertation provides a practical solution to implement simple, reliable, efficient and cost-effective AC-DC converters.

5.2 Suggestions for Further Work

The dissertation employs the technique of using a multi-winding transformer to integrate a boost PFC rectifier and an active-clamp DC-DC circuit. Based on the proposed converters, the suggested further work is to realize magnetic integration circuits by integrating the external inductors and the power transformer with single magnetic core. This implementation will result in smaller size, lighter weight and lower cost as well as more attraction for low power applications.

To further promote the conversion efficiency of the proposed converters, several topics could be the potential further work for this objective. Since the active-clamp circuit can only provide turn-on ZVS for the main switch, the suggested further work is to replace the active-clamp circuit with advanced soft-switching technique, such as zero-voltage-transition (ZVT) circuit or zero-current-transition (ZCT) circuit, etc. These techniques can effectively achieve soft-switching and voltage spike suppression at turn-off of the power switch. Moreover, although this dissertation employs the flyback-forward converter to facilitate the power delivery, there still exists a part of input power is processed two times before reaching final output. The part of input power is first transferred to bulk capacitor via the additional winding N_1 and then transferred to output port via the DC-DC cell. Thus, another suggested further work is to achieve the power transfer process in one time delivery from input terminal to output port.

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APPENDIX A

Derivation of Equations (3.12) and (3.13)

According to Fig. 3.5(d), KVL and KCL, the circuit equations are given by

$$i_P(t) = i_{Lr}(t) + i_{Lb}(t) \tag{A.1}$$

$$|v_{ac}(t)| - v_{N1}(t) - v_{N2}(t) - v_c(t) - V_b = L_b \frac{di_{Lb}(t)}{dt} \tag{A.2}$$

$$-v_c(t) - v_{N2}(t) = L_r \frac{di_{Lr}(t)}{dt} \tag{A.3}$$

$$C_c \frac{dv_c(t)}{dt} = i_P(t) \tag{A.4}$$

where

$$v_{N1}(t) = -\frac{n_1}{n_3} \cdot V_o \quad \text{and} \quad v_{N2}(t) = -\frac{n_2}{n_3} \cdot V_o . \tag{A.5}$$

Differentiating (A.1), (A.2) and (A.3) with respect to t yields

$$\frac{d^2 i_P(t)}{dt^2} = \frac{d^2 i_{Lr}(t)}{dt^2} + \frac{d^2 i_{Lb}(t)}{dt^2} \tag{A.6}$$

$$-\frac{dv_c(t)}{dt} = L_b \frac{d^2 i_{Lb}(t)}{dt^2} \tag{A.7}$$

$$-\frac{dv_c(t)}{dt} = L_r \frac{d^2 i_{Lr}(t)}{dt^2} . \tag{A.8}$$

And rearranging (A.4) yields

$$\frac{dv_c(t)}{dt} = \frac{i_P(t)}{C_c} . \tag{A.9}$$

Substituting (A.7), (A.8) and (A.9) into (A.6) yields

$$\frac{d^2 i_P(t)}{dt^2} = -\frac{1}{L_r}\frac{dv_c(t)}{dt} - \frac{1}{L_b}\frac{dv_c(t)}{dt} = -\frac{i_P(t)}{L_r C_c} - \frac{i_P(t)}{L_b C_c} . \tag{A.10}$$

Applying Laplace transform to (A.10), we can obtain (3.12).

Moreover, $v_c(t)$ can be derived by using the following equation:

$$\frac{di_{Lr}(t)}{dt} = \frac{di_P(t)}{dt} - \frac{di_{Lb}(t)}{dt} . \tag{A.11}$$

The substitution of (A.2) and (A.3) as well as the derivation of (3.12) into (A.11) yields

$$\frac{\frac{n_2}{n_3}\cdot V_o - v_c(t)}{L_r} = \left(-A_2\omega_2\cdot\sin(\omega_2 t) + B_2\omega_2\cdot\cos(\omega_2 t)\right) - \frac{|v_{ac}| + \frac{n_1}{n_3}\cdot V_o + \frac{n_2}{n_3}\cdot V_o - v_c(t) - V_b}{L_b}. \quad \text{(A.12)}$$

Rearranging (A.12), one can obtain the expression of v_c as shown in (3.13). Based on the initial condition

$$\begin{cases} i_P(0) = i_P(t_1) \\ v_c(0) = v_c(t_2) \end{cases} \quad \text{(A.13)}$$

A_2 and B_2 can be found.

APPENDIX B

Derivation of Equation (3.15)

According to Fig. 3.5(d) and Ampere's law, the current i_{Lb} in State 3 is given by

$$i_{Lb} = -\frac{n_2}{n_1} \cdot i_{N2} - \frac{n_3}{n_1} \cdot i_{N3}. \tag{B.1}$$

From Fig. 3. 5(d) and KCL, the following equation is given

$$i_{Lb} + i_{Lr} = i_{Lm} + i_{N2}. \tag{B.2}$$

Substituting (B.2) into (B.1) to replace i_{N2}, the integration of (B.1) through the duty-off time $(1-D)T_s$ can be obtained as

$$\int_0^{(1-D)T_s} i_{Lb}(t)dt = -\frac{n_2}{n_1} \cdot \int_0^{(1-D)T_s} \left(i_{Lb}(t) + i_{Lr}(t) - i_{Lm}(t)\right)dt - \frac{n_3}{n_1} \cdot \int_0^{(1-D)T_s} i_{N3}(t)dt. \tag{B.3}$$

Replacing the time functions of i_{Lr}, i_{Lm}, and i_{N3} with their corresponding voltage expressions yields

$$\begin{aligned}
&\left(\frac{n_1+n_2}{n_1}\right) \cdot \int_0^{(1-D)T_s} i_{Lb}(t)dt \\
&= \frac{n_2}{n_1} \cdot \frac{1}{L_r + L_b} \cdot \left(|v_{ac}(t)| + \frac{n_1}{n_3} \cdot V_o - V_b\right) \cdot \frac{t^2}{2}\Bigg|_0^{(1-D)T_s} - \frac{n_2}{n_1} \cdot \frac{L_b}{L_r + L_b} \int_0^{(1-D)T_s} i_p(t)dt + \frac{n_2}{n_1} \cdot \frac{L_b}{L_r + L_b} A_2 t\Big|_0^{(1-D)T_s} \\
&- \frac{n_2^2}{n_1 n_3} \cdot \frac{V_o}{L_m} \cdot \frac{t^2}{2}\Bigg|_0^{(1-D)T_s} - \frac{n_3}{n_1} \cdot \frac{P_o}{V_o} \cdot T_s.
\end{aligned} \tag{B.4}$$

Notice that the integration of i_p through the duty-off time $(1-D)T_s$ equals zero according to the charge balance across C_c. Rearranging (B.4), one can obtain the integration of i_{Lb} through $(1-D)T_s$ as

$$\int_0^{(1-D)T_s} i_{Lb}(t)dt = \frac{n_2}{n_1+n_2}\cdot\frac{1}{L_r+L_b}\cdot\left(|v_{ac}(t)|+\frac{n_1}{n_3}\cdot V_o - V_b\right)\cdot\frac{t^2}{2}\Bigg|_0^{(1-D)T_s} + \frac{n_2}{n_1+n_2}\cdot\frac{L_b}{L_r+L_b}A_2 t\Big|_0^{(1-D)T_s}$$
$$-\frac{V_o}{L_m}\cdot\frac{n_2^2}{(n_1+n_2)n_3}\cdot\frac{t^2}{2}\Bigg|_0^{(1-D)T_s} - \frac{n_3}{n_1+n_2}\cdot\frac{P_o}{V_o}\cdot T_s. \tag{B.5}$$

Moreover, i_{Lb} can also be expressed as (3.14). The integration of (3.14) through the duty-off time $(1-D)T_s$ is given by

$$\int_0^{(1-D)T_s} i_{Lb}(t)dt = \frac{1}{L_r+L_b}\left[\left(|v_{ac}(t)|+\frac{n_1}{n_3}V_o - V_b\right)\cdot\frac{t^2}{2}\Bigg|_0^{(1-D)T_s} - L_r A_2 t\Big|_0^{(1-D)T_s}\right]. \tag{B.6}$$

Equating (B.5) with (B.6), one can obtain A_2 as expressed in (3.15).

APPENDIX C

Derivation of Equations (3.19) and (3.20)

The derivation of Equations (3.19) and (3.20) is similar to that described in Appendix A. The most obvious difference lies in that the resonant capacitance is C_r instead of C_c. Thus, according to Fig. 3.5(e), the circuit equations are given by

$$i_P(t) = i_{Lr}(t) + i_{Lb}(t) \tag{C.1}$$

$$|v_{ac}(t)| - v_{N1}(t) - v_{N2}(t) - v_c(t) - V_b = L_b \frac{di_{Lb}(t)}{dt} \tag{C.2}$$

$$V_b - v_{N2}(t) - v_{Cr}(t) = L_r \frac{di_{Lr}(t)}{dt} \tag{C.3}$$

$$C_r \frac{dv_{Cr}(t)}{dt} = i_P(t) \tag{C.4}$$

where $v_{N1}(t)$ and $v_{N2}(t)$ are the same as (A.5). With the use of the differentiation and substitution, the equations of resonant current $i_P(t)$ and voltage $v_c(t)$ can be obtained as

$$\frac{d^2 i_P(t)}{dt^2} = -\frac{i_P(t)}{L_r C_r} - \frac{i_P(t)}{L_b C_r} \tag{C.5}$$

and

$$\frac{V_b + \frac{n_2}{n_3} \cdot V_o - v_{Cr}(t)}{L_r} = \left(-A_3\omega_3 \cdot \sin(\omega_3 t) + B_3\omega_3 \cdot \cos(\omega_3 t)\right) - \frac{|v_{ac}(t)| + \frac{n_1}{n_3} \cdot V_o + \frac{n_2}{n_3} \cdot V_o - v_{Cr}(t)}{L_b} \tag{C.6}$$

respectively. Applying Laplace transform to (C.5), one can obtain $i_P(t)$ as expressed in (3.19). Rearranging (C.6), $v_{Cr}(t)$ can be found as shown in (3.20).

APPENDIX D

Derivation of Equation (3.25)

Referring to Fig. 3.5(f), the circuit equations are given by

$$i_P(t) = i_{Lr}(t) + i_{Lb}(t) \tag{D.1}$$

$$i_{N2}(t) = i_P(t) - i_{Lm}(t) \tag{D.2}$$

$$n_1 i_{Lb}(t) = -n_2 i_{N2}(t) \tag{D.3}$$

$$|v_{ac}(t)| - v_{N1}(t) - v_{N2}(t) = L_b \frac{di_{Lb}(t)}{dt} \tag{D.4}$$

$$V_b - v_{N2}(t) = L_r \frac{di_{Lr}(t)}{dt} \tag{D.5}$$

$$v_{N2}(t) = L_m \frac{di_{Lm}(t)}{dt}. \tag{D.6}$$

Substituting (D.2) and (D.3) into (D.1), and then differentiating (D.1) with respect to t, one can obtain

$$\frac{di_{Lr}(t)}{dt} = \frac{di_{Lm}(t)}{dt} - \left(\frac{n_1 + n_2}{n_2}\right) \cdot \frac{di_{Lb}(t)}{dt}. \tag{D.7}$$

By substituting (D.4), (D.5), and (D.6) into (D.7), one can obtain

$$\frac{V_b - v_{N2}(t)}{L_r} = \frac{v_{N2}(t)}{L_m} - \left(\frac{n_1 + n_2}{n_2}\right) \cdot \frac{|v_{ac}(t)| - \left(\frac{n_1 + n_2}{n_2}\right) \cdot v_{N2}(t)}{L_b}. \tag{D.8}$$

Rearranging (D.8), v_{N2} can be obtained as shown in (3.25).

APPENDIX E

Derivation of Equation (4.2)

According to Figs. 4.4(a) and 4.4(b), the circuit equations are given by

$$n_2 i_{N2}(t) = n_3 i_{Lo}(t) \tag{E.1}$$

$$i_{Lr}(t) = i_{Lm}(t) + i_{N2}(t) \tag{E.2}$$

$$V_b - v_{N2,t0} = L_r \frac{di_{Lr}(t)}{dt} \tag{E.3}$$

$$v_{N2,t0} = L_m \frac{di_{Lm}(t)}{dt} \tag{E.4}$$

$$\frac{n_3}{n_2} v_{N2,t0} - V_o = L_o \frac{di_{Lo}(t)}{dt}. \tag{E.5}$$

Substituting (E.1) into (E.2) to replace i_{N2} and then differentiating (E.2) with respect to t, one can obtain

$$\frac{di_{Lr}(t)}{dt} = \frac{di_{Lm}(t)}{dt} + \frac{n_3}{n_2} \cdot \frac{di_{Lo}(t)}{dt}. \tag{E.6}$$

Substituting (E.3), (E.4), and (E.5) into (E.6) yields

$$\frac{V_b - v_{N2,t0}}{L_r} = \frac{v_{N2,t0}}{L_m} + \frac{n_3}{n_2} \cdot \frac{\frac{n_3}{n_2} v_{N2,t0} - V_o}{L_o}. \tag{E.7}$$

Rearranging (E.7), $v_{N2,t0}$ can be obtained as shown in (4.2).

APPENDIX F

Derivation of Equation (4.16)

According to Fig. 4.4(l), the circuit equations are given by

$$i_{Lr}(t) = i_{Lm}(t) + i_{N2}(t) \tag{F.1}$$

$$n_1 i_{Lb}(t) + n_2 i_{N2}(t) = n_3 i_{Lo}(t) \tag{F.2}$$

$$|v_{ac}(t)| - v_{N1,t7}(t) - V_b = L_b \frac{di_{Lb}(t)}{dt} \tag{F.3}$$

$$V_b - v_{N2,t7}(t) = L_r \frac{di_{Lr}(t)}{dt} \tag{F.4}$$

$$v_{N2,t7}(t) = L_m \frac{di_{Lm}(t)}{dt} \tag{F.5}$$

$$\frac{n_3}{n_2} v_{N2,t7}(t) - V_o = L_o \frac{di_{Lo}(t)}{dt}. \tag{F.6}$$

Substituting (F.1) into (F.2) to replace i_{N2} and then differentiating (F.2) with respect to t, one can obtain

$$n_1 \frac{di_{Lb}(t)}{dt} + n_2 \left(\frac{di_{Lr}(t)}{dt} - \frac{di_{Lm}(t)}{dt} \right) = n_3 \frac{di_{Lo}(t)}{dt}. \tag{F.7}$$

Substituting (F.3), (F.4), (F.5), and (F.6) into (F.7) yields

$$n_1 \cdot \frac{|v_{ac}(t)| - v_{N1,t7}(t) - V_b}{L_b} + n_2 \cdot \left(\frac{V_b - v_{N2,t7}(t)}{L_r} - \frac{v_{N2,t7}(t)}{L_m} \right) = n_3 \cdot \frac{\frac{n_3}{n_2} v_{N2,t7}(t) - V_o}{L_o}. \tag{F.8}$$

Replacing $v_{N2,t7}(t)$ with $(n_2 / n_1) \cdot v_{N1t7}(t)$ and rearranging (F.8), $v_{N2,t7}$ can be obtained as shown in (4.16).