國　立　交　通　大　學

機械工程學系

碩士論文

利用鎖相迴路鑑別結構共振

Identifying Resonant Structure with Phase Locked Loops

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中華民國九十六年十二月

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摘　　要

本論文目的在探討利用一個簡單的方法去估計一個共振二階系統的自然頻率以及阻尼比。在陀螺儀和加速度計中結構的瑕疵以及黏滯阻尼會降低微機電系統的性能。利用鎖相迴路當作微機電系統裝置的驅動電路，我們可以利用追蹤頻率去估計一個共振二階系統的自然頻率以及阻尼比。接下來我們利用一個電路去完成我們所提議的方法，以及利用此電路去估計一個二階系統的自然頻率以及阻尼比。

Identifying Resonant Structure with Phase Locked Loops

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Abstract

This study presents a simple method to evaluate the natural frequency and the damping ratio of a second order system considering resonant excitation. Structural imperfection and the viscous damping can dramatically reduce the performance of micro-electromechanical systems (MEMS) in gyro or accelerometer applications. Using the phase locked loops (PLL) as the electrical driving circuit of the MEMS devices, the tracking frequency can be used to calculate the natural frequency and the damping ratio. The proposed method is implemented using a simple circuit.

誌謝

在研究所的日子裡，我得到了許多人的協助，使論文得以順利完成，首先得感謝指導老師成維華教授在各方面給予我辛勤的教誨與指引我學習方向，幫助我解決了許多問題，相信這些學習與成長會對自己往後人生會有莫大的幫助。

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謹以此篇論文獻給每一個關心我、陪伴我以及愛我的人，並祝平安健康。

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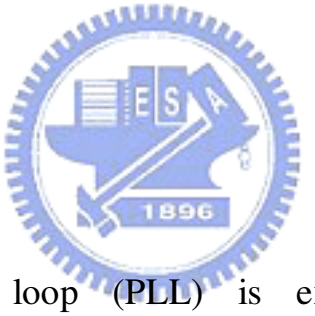
Chapter 1 Introduction

1.1 History

The system damping ratio is an important index of the performance of a micro electromechanical system (MEMS) or any system that exhibits resonance. The Q factor is the reciprocal of the damping ratio. With a high Q, the measurement signal of the system response can be effectively magnified. However, the damping ratio can never be easily determined in practice, especially when the excitation frequency from the driving circuit is as high as 20K Hz.



1.2 Motive

The phase locked loop (PLL) is extensively used in the modulation/demodulation circuits [1,2]. It provides a fixed phase error between output and input signals, locking the frequency and phase. Typically, the phase difference between the output and input of a PLL is $\pi/2$. The phase difference of a second order system without damping is $-\pi/2$ when the system is driven at its natural frequency. The natural frequency can be obtained when a PLL is the driving circuit of a second order system. In practice, the system always contains the damping component, which shifts the tracking frequency from the natural frequency. Thus, measuring the tracking frequency reveals the damping ratio.

The phase difference between output and input signals depends on the system's parameters [3]. Those of a mechanical system are effective mass, effective stiffness, and system damping; for an electronic circuit, they are equivalent inductance, capacitance, and resistance. Evaluating the input/output relationship, including phase difference, identifies the system's parameters.

1.3 Research Orientation

Phase locked loops (PLL) are used in so many different application. Examples of applications that use PLL include clock and data recovery, clock synthesis or synchronization, frequency synthesis, and PLL modulator or de-modulator application. In clock and data recovery applications the PLL is used to generate a synchronized sampling signal, where none exited before, from transitions in the data stream. Clock synchronizations systems use a PLL to clock a local signal, generated by VCO, to an incoming clock signal that already exists. In the way, skew between the data and clock signals can be eliminated, even when there are delay differences between the two paths due to clock buffering and other factors. In some designs, such as high frequency microprocessor implementations, an internal clock is needed at a higher frequency than the external reference. In this case the PLL clock generator is actually a frequency synthesizer. Other frequency synthesizer applications include RF transceiver applications where a number of closely spaced RF local oscillator frequencies need to be created to select the desired incoming channel.

The PLL is mostly used as an oscillator to lock or track input signals in both phase and frequency. When phase errors between input signal and output signal are zero or very small, it is often called “lock”. Hence, the purpose of PLL is to reduce phase errors as small as possible. The traditional analog PLL satisfies the purpose.

Chapter 2 PLL Overview

This chapter starts with the basic concepts of phase-locked loop (PLL). The basic concept includes the linear model and the operation of the PLL. The types of phase-locked loop are introduced next. Finally, the applications of phase-locked loop are introduced. It consists of skew suppression, jitter reduction, frequency synthesizer, and clock-data recovery.

2.1 Phase-Locked Loop Background

A phase-locked loop (PLL) is simply a servo system controlling the phase of its output in such a way that the phase error between output and input reduces to a minimum. A block diagram of a phase-locked loop (PLL) is shown in Fig.2.1. The PLL consists of three basic functional blocks:

1. A phase detector (PD)
2. A loop filter (LF)
3. A voltage controlled oscillator (VCO)

In some PLL circuits a current-controlled oscillator (CCO) is used instead of a VCO. In this case the output signal of the phase detector is a controlled current source rather than a voltage source. However, the operating principle remains the same.

The phase detector (PD) compares the phase of the output signal with the phase of the input signal and produces an output signal, which is approximately proportional to the phase error between each other.

The output signal of the PD consists of DC and AC components. The latter is undesired: hence the loop filter decays it. The output of the loop filter is applied to the VCO. The control voltage changes the VCO frequency in a direction that reduces the phase difference between the input and the VCO output.

Under the lock condition, the negative feedback adjusts the dc value of the VCO control voltage that VCO output oscillates at the same frequency as the input. However, there is a fixed phase error between the input and output signal when in lock. On the other hand, the phase domain analysis of PLL is commonly used to illustrate the operation principle of the PLL. Next, the linear model in phase domain will be presented.

In Figure 2.2, the linear model of the PLL in phase domain is illustrated. Assuming H(s) is the transfer function of a first-order RC low-pass filter. According to the function of the phase detector, generating a dc voltage proportional to the phase differences of the input and the output signals which is sent to the VCO via a loop filter. Thus, the phase detector can be modeled as a multiplier with a gain K_p. Since the phase is the integral of the frequency and the VCO acts as an ideal integrator for the input voltage when output variable is the phase. The frequency response of the VCO is equal to $\frac{Kvco}{s}$ where K_{VCO} is the gain of the VCO.

After some manipulation, the phase transfer function of the close loop is represented as follows:

$$\frac{\Phi_{out}(s)}{\Phi_{in}(s)} = \frac{K_P K_{VCO} H(s)}{s + K_P K_{VCO} H(s)} \quad (2\text{-}1)$$

The transfer function of H(s) is given by the equation (2-2).

$$H(s) = \frac{1}{1 + RCs} \quad (2\text{-}2)$$

Then the close loop transfer function can be determined by combining the equation (2-1) and (2-2) as

$$\frac{\Phi_{out}(s)}{\Phi_{in}(s)} = \frac{K\omega}{s^2 + \omega s + K\omega} \quad (2\text{-}3)$$

Where $K = K_P K_{VCO}$ is the loop gain of PLL and $\omega = \frac{1}{RC}$.

Because the equation (2-3) is the second-order, it can be converted into the standard form of the second-order transfer function as

$$\frac{\Phi_{out}(s)}{\Phi_{in}(s)} = \frac{\omega_n^2}{s^2 + 2\omega_n \zeta s + \omega_n^2} \quad (2\text{-}4)$$

Where $\omega_n = \sqrt{K\omega}$ and $\zeta = \sqrt{\frac{\omega}{K}}$.

Let the phase difference of input and output signals be Φ_e, i.e,

$$\Phi_e(s) = \Phi_{in}(s) - \Phi_{out}(s) \quad (2\text{-}5)$$

Combing Equation (2-4) and (2-5), we have

$$\frac{\Phi_e(s)}{\Phi_{in}(s)} = \frac{s^2 + 2\zeta\omega_n s}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2-6}$$

Where $\Phi_{in}(s)$ represents the phase error at the input as shown in the Figure 2.2.

If ω_{in} is the input in angular frequency and the phase grows linearly thus the input signal is adapted as $\frac{\omega_{in}}{s^2}$. Finally, via final value theorem represented as,

$$\lim_{s\to\infty} \theta(t) = \lim_{s\to 0} s \bullet \theta(s) \tag{2-7}$$

then the static phase error Φ_{se} is determined as

$$\Phi_{se} = \lim_{s\to 0} s\Phi_e(s) = \lim_{s\to 0} \frac{\omega_{in}}{s} \bullet \frac{s^2 + 2\zeta\omega_n s}{s^2 + 2\zeta\omega_n s + \omega_n^2} = \frac{2\zeta}{\omega_n} \bullet \omega_{in} = \frac{2\omega_{in}}{K} \tag{2-8}$$

where $K = K_P K_{VCO}$ is the loop gain of PLL.

The equation (2-8) shows there will be an unwanted phase error which is proportional to the input frequency. This effect can be eliminated by introducing of a pole at the origin.

A linear model is suitable to explain the tracking performance of the PLL, if the PLL was initially locked. If the PLL are initially unlocked, however, the phase error can take on arbitrarily large valves, and the linear model is no longer valid.

2.1.1 PLL Design Concepts

■ **Phase detector:**

An ideal phase detector produces an output signal whose average dc value is linearly proportional to the phase of two periodic inputs (Figure 2.3).

$$\overline{V_{OUT}} = K_d \times \Delta\Phi \tag{2-9}$$

K_d is the gain of the phase detector and its unit is V/rad, and $\Delta\Phi$ is the input phase difference. However, a circuit that can detect both phase and frequency difference proves extremely useful because it significantly increases the acquisition range and lock speed of PLLs.

■ **Loop Filter:**

The loop filter determines most of the PLL's specifications. Intuitively, it is utilized to extract the DC component of the signals from PD for the following VCO. It can be realized in either active or passive forms and the overall system performance of PLLs is greatly affected by the loop filter design. Fig 2.4 depicts several passive filters commonly adopted in most PLLs. High order filters are advantageous to rejecting noise within the PLL. However, the stability issue is of great concern. Contrarily, low order filters result in more stable operations yet moderate noise rejection capability. The choice between high order and low order filters depends on the applications and careful attention must be paid to prevent PLLs from unstable operations.

■ **Voltage Control Oscillator:**

If a voltage can vary the output frequency of an oscillator, then the circuit is called a "voltage-controlled oscillator" (VCO), and the characteristic of VCO is shown in Fig 2.5.

Some important considerations of VCO design are

(1) Phase stability: the frequency spectrum of the VCO output should look like an ideal Dirac-impulse. In other words, the phase noise of a VCO must be as low as possible.

(2) Electrical tuning range: the tunable frequency range of a VCO must be able to cover the entire required frequency range of the interested application.

(3) Tuning linearity: An ideal VCO has a constant VCO gain, K_{VCO} at the entire frequency range. A constant VCO gain can simplifies the design procedure of a PLL.

(4) Frequency pushing: the dependency of the center frequency on the power supply voltage (in [MHz/V]).

(5) Frequency pulling: the dependency of the center frequency on the output load impendence.

(6) Low cost.

We define an ideal VCO as a circuit that generates a periodic output whose frequency is a linear function of a control voltage, V_{ctrl}, as shown in Figure 2.5. It is given by

$$f_0 = f_{free} + K_{VCO} V_{ctrl} \qquad (2\text{-}10)$$

where f_{free} is the free-running frequency and K_{VCO} is the gain of the VCO, expressed in rad/S/V. The existence of f_0 in the above equation simply indicates that, for the practical range of V_{ctrl}, f_0 may not approach zero. In other words, V_{ctrl} creates a change around f_0.

Once the VCO starts to change frequency, the loop is in the capture state. PLL will stay in this state until the VCO and the input frequencies are exactly the same, which is called “phase-locked”. During phase-locked state, the VCO frequency is identical to the input of the loop, except for a fixed phase difference.

The range that the system will follow changes in the input frequency is called the locking range. The frequency range in which the loop acquires phase-locked is called the capture range, and will never greater than the locking range.

The dynamic characteristic of the phase-locked loop is controlled primarily by the loop filter. Once the loop is phase-locked, the filter limits the respond speed when the loop tracks changes in the input frequency. In addition, the loop filter provides some kinds of short-term memory and recapture rapidly if the system is out of lock by a noise transient.

In most PLLs, the low-pass filter is first or second order. The simplest structure is an RC low-pass filter, which has been the most commonly used filter. There are many different structure of the phase detector, including an analog multiplier, a simple exclusive-OR gate, a combination of digital circuits such as D flip-flops (three-state), or even extended range (N-state) phase detector. The voltage-controlled oscillator

mainly has three forms, which are LC-tuned oscillators in discrete circuits or MMICs, ring oscillators, or double-crossed multivibrators in CMOS integrated circuit.

Different PLL types are built from different building blocks. Following sections give brief conception to analyze and design the categories of PLL.

2.2 Types of Phase-Locked Loop

Recently, the technique of integration circuit is growing substantially. Due to speed of each system circuit is increasing by a wide margin, it is more important to synchronize operation frequency among chips. Furthermore, communication system is developed rapidly, such as data transmission and personal communication system, etc, that to economize the use of hardware in communication is more significant. For instance, in data transmission only data signal is delivered but clock signal doesn't, receiver must find out and adjust the data modulated with clock signal therefore and that is called clock recovery or timing recovery [6]. Phase-locked loop is applicable to these circuit systems for convenient integration and extensive functionality. Not only operation amplifier but phase-locked loop is functional integrated circuit.

Generally, based on the development of phase-locked loop, phase-locked loop is divided into four types:

1. Linear Phase-Locked Loop
2. Digital Phase-Locked Loop
3. All-Digital Phase-Locked Loop

4. Software Phase-Locked Loop

A simple introduction to these four architectures of phase-locked loop is proposed as follow.

2.2.1 Linear Phase-Locked Loop

From 1930s, certain relevant theories of phase-locked loop have been published and the aspect of linear phase-locked loop was started to notice. Fig. 2.6 shows the basic structure of linear phase-locked loop that consists of phase detector, loop filter, and voltage controlled oscillator [5].

Phase detector is a four quadrant analog multiplier or mixer that is used to detect input signal, U_i and U_o, and compare U_i with U_o as well as generate voltage depended on the phase error. Loop filter, used to filter high frequency signal and noise through phase detector, stabilize system and transform the signal into DC voltage for adjusting the output oscillation frequency and phase of voltage controlled oscillator, contains resistor and capacitor. Voltage controlled oscillators is an analog voltage controlled oscillation circuit which generates relative oscillation frequency in a fixed range by varied controlled voltage.

The input of phase detector includes input signal and output signal of voltage-controlled oscillator, as shown in Fig. 2.6. Because the phase detector of linear phase-locked loop is a four-quadrant analog multiplied or mixer [7], only phase error is detected. The output signal of phase detector is the product of two input signal, U_i and U_o. The product is provided with two signal which contains high frequency signal and low

frequency signal, $U_d(\theta_1+\theta_2)$ and $U_d(\theta_1-\theta_2)$ respectively, filtered by low pass filter in order to remove the high frequency component and use the low frequency signal to control the oscillator frequency of voltage controlled oscillator. To operate repeatedly will make $\theta_1=\theta_2$ to finish locking.

Linear phase-locked loop is the initial structure of phase-locked loop. However, the output frequency range, lock time, and phase error of linear phase-locked loop are worse than digital and all digital phase-locked loops. Therefore linear phase-locked loop is rarely used in all digitization design.

2.2.2 Digital Phase-Locked Loop

Digital phase-locked loop is a structure of phase-locked loop combined analog signal with digital signal. The difference to linear phase-locked loop is that the phase detector of digital phase-locked loop is a digital circuit called digital phase detector [6]. The detected signal of digital phase detector, which consists of digital logic circuit such as exclusive gate or flip-flops etc, is not sine wave but square wave.

Fig. 2.7 shows the basic structure diagram of digital phase-locked loop which includes digital phase-frequency detector (PFD), analog charge pump (CP), loop filter, voltage controlled oscillator (VCO), and divider. The functionality of phase-frequency detector is that comparing the frequency and phase of input signal with feedback signal generates UP and DOWN signal depended on the frequency and phase to charge and discharge charge pump. Loop filter is used to filter high frequency

signal generated by charge pump in order to transform digital signal to analog signal for adjusting the output frequency of voltage-controlled oscillator. Then using the analog signal to control varied output frequency of voltage controlled oscillator generates output signal which is N times input signal through divider.

Charge pump is divided into two types, voltage control and current control. These types have the same operating theory. Using the open and close, charge and discharge, to increase and decrease output voltage respectively alters the frequency range of voltage-controlled oscillator. Divider is not necessarily required in the design of phase-locked loop. Divider makes the phase-locked loop to generate multiple frequencies, raises input frequency range and increases the purity of output frequency of voltage-controlled oscillator. But the disadvantage is enhancing the difficulty in designing system and increasing power dissipation.

Due to the growth of the technique of integrated circuit, phase-locked loop already achieves Giga-Hz operation frequency. When operating in such high frequency, the interference of signals affects system performance significantly. Due to digital phase-locked loop produces analog and digital signals simultaneously, digital signal interferes with analog signal easily. That is an emphasis on designing digital phase-locked loop.

Now the technique of CMOS has undergone an incredible development, digitalizing circuit becomes most important part. Traditional phase-locked loop taking analog approach makes difficult design. Form a system viewpoint, the integration of phase-locked loop poses big design challenges such as noise interference, signal barrier, and

stable voltage source, etc [7]. Digital design can reduce these problems. Digital phase-locked loop is applicable to the design of communication circuit and on-chip clock generation circuit.

2.2.3 ALL-Digital Phase-Locked Loop

As implied by the name, all-digital phase-locked loop operates in an all-digital signal environment [8]. The analog signal of voltage-controlled oscillator must be replaced by the digital signal of digital controlled oscillator (DCO). With digital filter all system of phase-locked loop without passive devices becomes all-digital phase-locked loop. Due to free from passive devices, system has lowered noise interference and increased the stabilization [7].

Fig. 2.8 presents the basic structure of all-digital phase-locked loop. Phase-frequency detector, consists of various digital logic circuits, produces the discrepancy of two input signal phase. After receiving the generated result of phase-frequency detector, control unit processes the signal and then controls digital control oscillator to generate required frequency.

2.2.4 Software Phase-Locked Loop

Software phase-locked loop uses programming operation to control oscillation frequency until the output signal of oscillator is identical with the external input signal [9]. As the operation rate of microprocessor is improved, digital filter can be achieved by coding operation. Thus, software phase-locked loop can be implemented practicably. Compared to

other phase-locked loop, software phase-locked loop is more flexible. However, due to the limitation in the operation speed and analog-to-digital converter, the performance of software phase-locked loop is inferior to other hardware phase-locked loop. Fig. 2.9 shows the structure of software phase-locked loop simulated linear phase-locked loop [1]. Fig. 2.10 presents the structure of software phase-lock loop simulated digital phase-locked loop [1].

2.2.5 The Compare of PLL

In the analog PLL, the digital PLL and the all-digital PLL, they have many advantages and disadvantages respectively. We compare and illustrate them in Table 2-1.

These advantages and disadvantages are principally separated by design methodology. The PLL designed with analog circuits has characteristics of analog circuits. In opposition, the ADPLL designed with digital circuits has characteristics of digital circuits. Therefore, the analog PLL and the DPLL have characteristics of analog circuits but the ADPLL has characteristics of digital circuits.

The analog circuits take much tine to design, so they take long turnaround time. The digital circuits have higher noise immunity than the analog circuits. The VCO of an analog PLL or a DPLL produces a continuous frequency band but the DCO of an ADPLL produces a discrete frequency band. The VCO has higher resolution than the DCO. The digital circuits generally have lower power consumption than the analog circuits. An ADPLL may have small area because the loop filter of

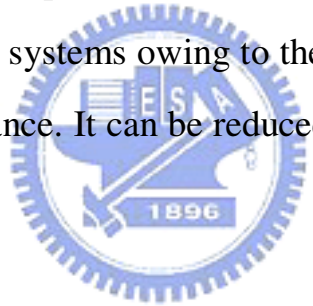
an analog PLL or a DPLL always has one or more large capacitors, whose area cannot be efficiently reduced as the process technology improving. An ADPLL shorten lock time by dealing with digital signals.

2.3 PLL Applications

PLL is useful building block in many applications which are described as follows:

2.3.1 Skew Suppression

Figure 2.11(a) is the expression of clock skew. Clock skew usually happens in the high speed systems owing to the delay of wire in the chips or interconnected capacitance. It can be reduced by using a PLL as shown in Figure 2.11(b).



2.3.2 Jitter Reduction

Jitter is the deviation from the precise clock transition as shown in Figure 2.12. The dotted line means the correct clock transition and the solid line means the clock suffered from with a deviation of Δ occur. In general, the phenomenon of the jitter can be reduced efficiently by the PLL.

2.3.3 Frequency Synthesizer

Many applications need frequency multiplication. A high frequency with a good quality is not easy to realize but PLL has a function of

frequency synthesizing and can achieve frequency multiplication efficiently.

2.3.4 Clock/Data Recovery

In a data transmission system, the data may be interfered by the noise, or the clock information may not be transferred so it needs to be extracted from the data. The PLL is useful to achieve this purpose. Figure 2.13 illustrates an example, the noisy data enters clock recovery circuit and cooperates with DFF to extract the precise data.

Chapter 3 Second Order System with PLL

Consider a second order system, the governing equation is shown as follows.

$$a_2\ddot{X} + a_1\dot{X} + a_0 X = F\sin\omega t \tag{3-1}$$

Where a_2 is effective mass, a_0 is effective stiffness, F is applied signal, ω is driving frequency, and a_1 is system damping. The particular solution is expressed as follows.

$$X = A\sin(\omega t - \theta) \tag{3-2}$$

Where A is the amplitude, and θ is the phase lag. The phase lag is expressed as follows.

$$\theta = \tan^{-1}\left(\frac{2\varsigma\omega/\omega_n}{1-\omega^2/{\omega_n}^2}\right) \tag{3-3}$$

Where ς is the damping ratio, and ω_n is the natural frequency.

There are two kinds of phase locked loops that we use. One is the PLL output is square waves, the other is the PLL output is sine waves. We discuss separately as follows.

3.1 Phase-Locked Loop (Square wave)

First of all, we discuss the PLL output is square waves. With the function block diagram for a second order system with phase-locked loops as shown in Fig. 3.1(a). The input and output signals are shown as follows.

$$f_1(t) = \sum_{n=1}^{\infty} \frac{4A_1}{(2n-1)\pi} \sin((2n-1)\omega_0 t) \tag{3-4}$$

$$f_2(t) = \sum_{n=1}^{\infty} \frac{4A_2}{(2n-1)\pi} \sin((2n-1)(\omega_0 t - \theta)) \tag{3-5}$$

Where A_1 and A_2 are the signal amplitude. The input signal and output signal through the Phase detector (a multiplier) are modulated as follows.

$$f_1(t) \times f_2(t) = (\frac{4}{\pi})^2 \sum_{\substack{n=1,3,5... \\ m=1,3,5...}}^{\infty} \frac{A_1 A_2}{2nm} \left[\cos((n-m)\omega_0 t + m\theta) - \cos((n+m)\omega_0 t - m\theta)\right] \tag{3-6}$$

Using the loop filter, simply as low pass filter yields a modulated signal is shown as follows.

$$f_1(t) \times f_2(t) = \sum_{n=1}^{\infty} (\frac{4}{(2n-1)\pi})^2 \frac{A_1 A_2}{2} \cos(-(2n-1)\theta) \tag{3-7}$$

The multiplier was used as AD633. The output of the multiplier is the product that divided by 10 of the input and output signal. The input and output signal amplitude is assumed as 10. Thus the LF output signal is expressed as follows.

$$f = \sum_{n=1}^{\infty} \left(\frac{4}{(2n-1)\pi}\right)^2 \frac{A_1 A_2}{2} \cos(-(2n-1)\theta) \\ = \sum_{n=1}^{\infty} \left(\frac{40}{(2n-1)\pi}\right)^2 \frac{1}{20} \cos(-(2n-1)\theta) \tag{3-8}$$

Using equation (3-8) to plot a figure as shown in Fig. 3.2 that contains the phase lag and the LF output signal. We can find relations between the phase lag and the LF output signal. The relation is shown as follows.

$$V = (90-\theta) * \frac{1}{9} \tag{3-9}$$

In the steady state, the filtered signal is fed into the voltage-controlled oscillator (VCO) and the output frequency of VCO is shown as follows.

$$\omega = \omega_0 + K_{VCO} \cdot V \tag{3-10}$$

where ω_0 is the initial frequency of VCO, K_{VCO} is the VCO gain, and V is the LF output signal.

The output signal of VCO is fed back to the phase detector and is fed into the plant. Fig. 3.1(a) depicts the loop. From equation (3-9) and equation (3-10) we can find relations as follows.

$$\theta = 9(10 - \frac{\omega - \omega_0}{K_{VCO}}) \tag{3-11}$$

Moreover, ω_n may be unknown or should be checked. We could set different initial frequency as ω_{01} and ω_{02}; therefore, different tracking frequency, ω_1 and ω_2 could be obtained. The resonant frequency and damping ratio can be estimated as follows.

$$\omega_n = \sqrt{\frac{\omega_1\omega_2(\omega_1 \tan\theta_1 - \omega_2 \tan\theta_2)}{\omega_2 \tan\theta_1 - \omega_1 \tan\theta_2}} \tag{3-12}$$

$$\varsigma = -\frac{(\omega_1{}^2 - \omega_n{}^2)\tan\theta_1}{2\omega_1\omega_n} \tag{3-13}$$

3.2 Phase-Locked Loop (Sine wave)

Now we discuss the PLL output is sine waves. With fixed input and output signals as shown in Fig. 3.1(b), the input signal and output signal are modulated as follows.

$$\sin(\omega t-\theta)\cdot\sin(\omega t)=\frac{1}{2}\cos(-\theta)-\frac{1}{2}\cos(2\omega t-\theta) \qquad (3\text{-}14)$$

Using the loop filter, simply as low pass filter yields a modulated signal is shown as follows.

$$\sin(\omega t-\theta)\cdot\sin(\omega t)\cong\frac{1}{2}\cos(-\theta). \qquad (3\text{-}15)$$

Consider a driving frequency ω, close to the natural frequency ω_n. Replace ω/ω_n with α in the first few terms of the Taylor expansion in equation (3-15) as follows.

$$\frac{1}{2}\cos(-\theta)=\frac{1}{2}\{-\frac{1}{\varsigma}(\alpha-1)+\frac{1}{2\varsigma}(\alpha-1)^2+\frac{1-\varsigma^2}{2\varsigma^3}(\alpha-1)^3+\ldots\} \qquad (3\text{-}16)$$

When α is around one, Equation (3-16) could be approximated as follows.

$$\frac{1}{2}\cos(-\theta)=-\frac{1}{2}\cdot\frac{1}{\varsigma}(\alpha-1). \qquad (3\text{-}17)$$

In the steady state, the filtered signal is fed into the voltage-controlled oscillator (VCO) and the output frequency of VCO is shown as follows.

$$\omega = \omega_0 + K_{VCO} \cdot \omega_0 \cdot \frac{1}{2}\cos(-\theta) \tag{3-18}$$

where ω_0 is the initial frequency of VCO, and K_{VCO} is the VCO gain. The output signal of VCO is fed back to the modulator and is fed into the plant. Figure 3.1(b) depicts the loop. Equation (3-18) yields the steady state of frequency as follows.

$$\frac{\omega}{\omega_n} = \frac{\omega_0 + K_{VCO} \cdot \omega_0 / 2\varsigma}{\omega_n + K_{VCO} \cdot \omega_0 / 2\varsigma}. \tag{3-19}$$

Measuring the tracking frequency yields an estimate of the damping ratio as follows.

$$\varsigma = \frac{1}{2} \cdot \frac{K_{VCO} \cdot \omega_0}{\omega_n} \left(\frac{\omega - \omega_n}{\omega_0 - \omega}\right) \tag{3-20}$$

Moreover, ω_n may be unknown or should be checked. We could set different initial frequency as ω_{01} and ω_{02}; therefore, different tracking frequency, ω_1 and ω_2 could be obtained. The resonant frequency and damping ratio can be estimated as follows.

$$\omega_n = \frac{\omega_{01}\omega_1(\omega_2 - \omega_{02}) - \omega_{02}\omega_2(\omega_1 - \omega_{01})}{\omega_{01}\omega_2 - \omega_{02}\omega_1} \tag{3-21}$$

$$\varsigma = \frac{K_{VCO}}{2} \cdot \omega_{01}\omega_{02} \cdot \frac{(\omega_1 - \omega_2)}{\omega_{01}\omega_1(\omega_2 - \omega_{02}) - \omega_{02}\omega_2(\omega_1 - \omega_{01})}. \qquad (3\text{-}22)$$

In the next chapter, we can use a resistance(R), inductance(L) and capacitance(C) to simulate a second order system to do this experiment. We can use equation (3-12~3-13) and equation (3-21~3-22) to estimate the resonant frequency and the damping ratio of a second order system. Finally we actually utilize one device to substitute for RLC. Using phase locked loops to evaluate the natural frequency and the damping ratio of this device.

Chapter 4 Experiment

We can use a resistance(R), inductance(L) and capacitance(C) to simulate a second order system as shown in Fig.4.1. We can estimate the resonant frequency and the damping ratio of a second order system considering resonant excitation according to equation (3-12~3-13) and equation (3-21~3-22).

4.1 Phase-Locked Loop (Square wave)

The Bode diagram of a second order system is shown as Fig. 4.2. We change the scale of x-axis from log to linear. The diagram is shown as Fig. 4.3.

According to equation (3-10) we set two different VCO gain to plot a figure as shown in Fig. 4.4 that contains the output frequency of VCO and the input voltage of VCO. We can find relations between the output frequency of VCO and the input voltage of VCO.

We change y-axis of the phase plot of Fig. 4.3 from phase to voltage according to equation (3-9). The diagram is shown as Fig. 4.5.

We combine with Fig. 4.4 and Fig. 4.5. The diagram is shown as Fig. 4.6. Intersection points of Fig. 4.6 are the tracking frequency. So we can set different VCO parameters to obtain different tracking frequencies. Equation (3-11~3-13) yield estimates of the natural frequency and the damping ratio of a second order system with different VCO parameters, when VCO parameters are decided.

The experiment involves an electric circuit. An inductor, resister and

capacitor are used to emulate a second-order plant. The transfer function can be expression as follows.

$$G(S)=\frac{1}{CLs^2+CRs+1} \tag{3-23}$$

We assume

$$R = 250\Omega$$

$$L = 100mH$$

$$C = 100\text{n}\,f$$

Fig. 4.7 shows the schematic diagram of the circuit. The voltage signal, fed into the VCO module, stands for the driving frequency. The equipment is shown as Fig. 4.8.

For practical components with quantitative errors, the system damping ratio is determined by measuring relationship between the input and output using a dynamic signal analyzer (HP 35607A), as shown in Fig. 4.9(a) and Fig 4.9(b).

Equation (3-12) and (3-13) yield estimates of the natural frequency and the damping ratio with different phases, when θ_1 and θ_2 are obtained from equation (3-11).

The theoretical natural frequency, ω_n of the plant is a function of both the inductance and the capacitance. Though the parameters of the passive components are not accurate, they still provide information to indicate the nature frequency of the plant. Various resistances were set to yield different damping ratios.

4.1.1 Experimental Result

The experimental result is shown as Table 4-1(a). The natural frequency is (1.55±0.05)KHz. The damping ratio is 0.32±0.03. Figure 4.10 plots the tracked profile. The yellow line is the output of the PLL. The green line is the output passing RLC. We set different resistances to yield different damping ratios. The experimental result is shown as Table 4-1(b) and Table 4-1(c). The resonant frequency and the damping ratio are different between an experiment and the theory. There are several reasons for these results. One of that is the low pass filter is not an ideal filter. Thus, the output of the low pass filter includes parts of high frequency. The accuracy of equation (3-9) becomes imprecision. The resonant frequency and the damping ratio are also inaccuracy, but they and the result of HP35670A identification are very close.

4.2 Phase-Locked Loop (Sine wave)

An inductor, resister and capacitor are used to emulate a second-order plant. The transfer function can be expression as follows.

$$G(S)=\frac{1}{CLs^2+CRs+1}$$

$$R = 250\Omega$$

$$L=100mH$$

$$C = 100\text{n}\,f$$

Fig. 4.11 shows the schematic diagram of the circuit. The voltage signal, fed into the VCO module, stands for the driving frequency. For practical components with quantitative errors, the system damping ratio is

determined by measuring relationship between the input and output using a dynamic signal analyzer (HP 35607A), as shown in Fig. 4.12(a) and Fig 4.12(b).

Equation (3-21) and (3-22) yield estimates of the natural frequency and the damping ratio. We set different resistances to yield different damping ratios.

4.2.1 Experimental Result

The experimental result is shown as Table 4-2(a). The natural frequency is (1.53±0.02)KHz. The damping ratio is 0.31±0.02. Figure 4.13 plots the tracked profile. The yellow line is the output of the PLL. The green line is the output passing RLC. We set different resistances to yield different damping ratios. The experimental result is shown as Table 4-2(b). The resonant frequency and the damping ratio have a little different between an experiment and the theory. There are several reasons for these results. One of that is the low pass filter is not an ideal filter. Thus, the output of the low pass filter includes parts of high frequency. The accuracy of equation (3-15) becomes imprecision. The resonant frequency and the damping ratio are also inaccuracy, but they and the result of HP35670A identification are very close.

4.3 The ultrasonic cleaning tank

Before we use a resistance(R), inductance(L) and capacitance(C) to simulate a second order system, we actually utilize one device to substitute for RLC. Using phase locked loops to evaluate the natural

frequency and the damping ratio of this device considering resonant excitation. We select the ultrasonic cleaning tank to do this experiment. The ultrasonic cleaning tank is shown as Fig. 4.14. Based on electronic vibration principle, the ultrasonic cleaning tank makes use of piezoelectric oscillator to produce high frequency shock waves (ultrasonic waves) to shake the liquid to reach the result of washing. The ultrasonic cleaning tank that we select produces 42K-Hz frequency ultrasonic waves to shake the liquid. The specifications of the ultrasonic cleaning tank are shown as Table 4-3.

The schematic diagram is shown as Fig. 4.15. We put different liquids in the ultrasonic cleaning tank. We can evaluate the natural frequency and the damping ratio of the liquid in the ultrasonic cleaning tank. The equipment is shown as Fig. 4.16.

4.3.1 Experimental Result

We separately put 100ml water, oil and ink in the ultrasonic cleaning tank. The experimental result is shown as Table (4-4~4-6). The natural frequency is about 42KHz. The damping ratio is about 0.257, 0.276 and 0.260 separately. The result is not so accurate, because the output of the ultrasonic cleaning tank is not continuous waves. Sometimes we can not distinguish water and the ink. Figure 4.17 plots the tracked profile. The yellow line is the output of the PLL. The green line is the output of the ultrasonic cleaning tank. We put 500ml water in the ultrasonic cleaning tank in addition. The experimental result is shown as Table 4-7.

Chapter 5 Conclusion

This work presented a method to measure the second order system damping ratio and natural frequency using PLL. The system works by taking advantage of resonance, at which the PLL provides information on the system parameters. Electrical circuit experimentation is also performed. We also utilize this circuit to measure one device's damping ratio and natural frequency. The estimated damping ratio and natural frequency are close to the actual damping ratio and natural frequency when we use a resistance, inductance and capacitance to simulate a second order system. The proposed scheme measures the net effect of the total system.

Practically, a real system is usually not a simple second order system. Continuous bodies have several natural frequencies in different modes. Furthermore, the junction between the structure and the circuits may results in extra modes. Dividing the frequency bandwidth into many sub-bands of the system that each behaves as a second order system for every division. Multi-band testing can be performed to estimate the system parameters with the proposed method. Moreover, this scheme can determine the net effect of the system.

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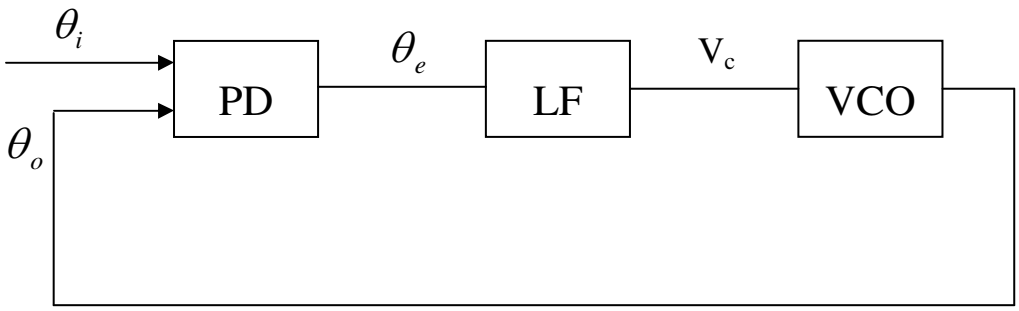

Fig. 2.1 A simplified PLL block diagram

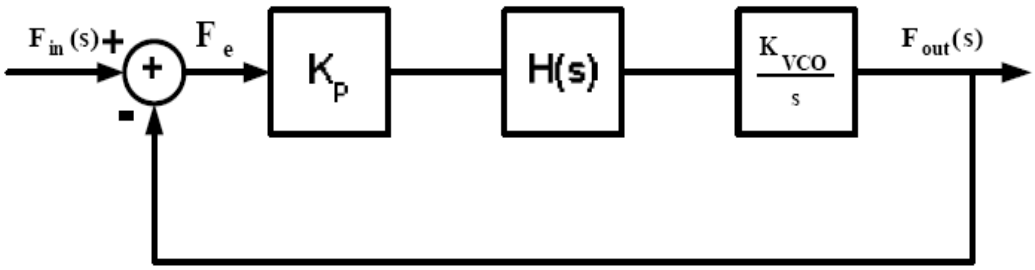

Fig. 2.2 A classical linear model of PLLs

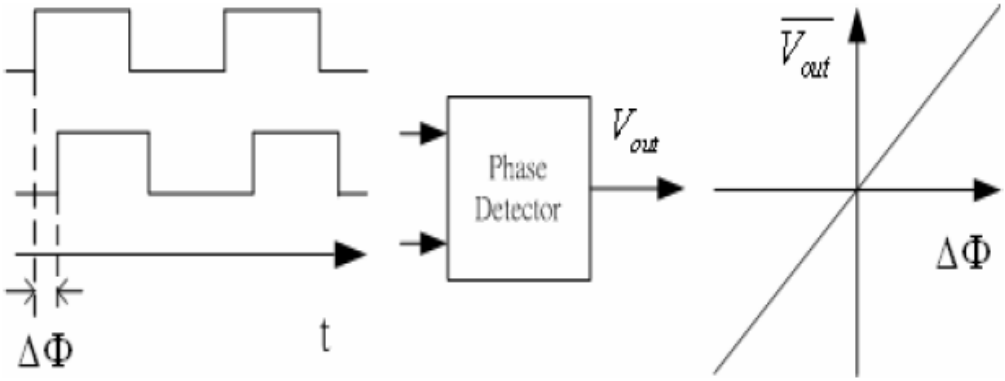

Fig 2.3 Characteristic of an ideal phase detector

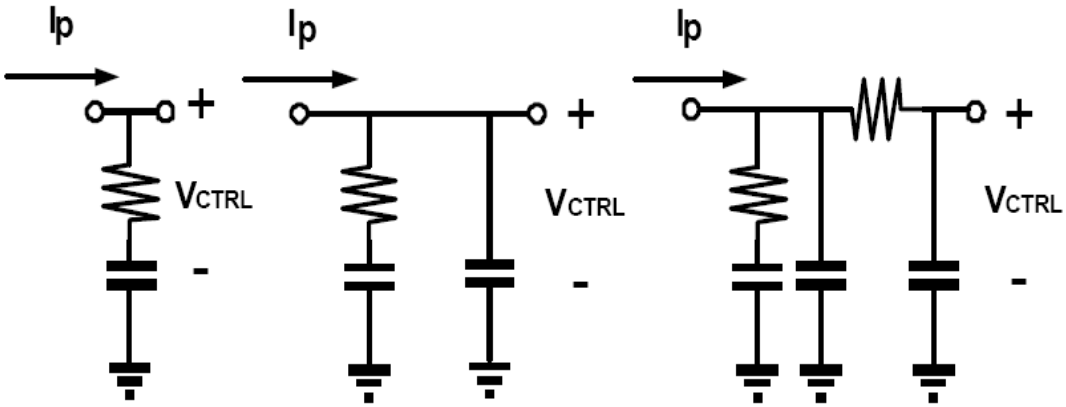

Fig 2.4 The loop filter schematics

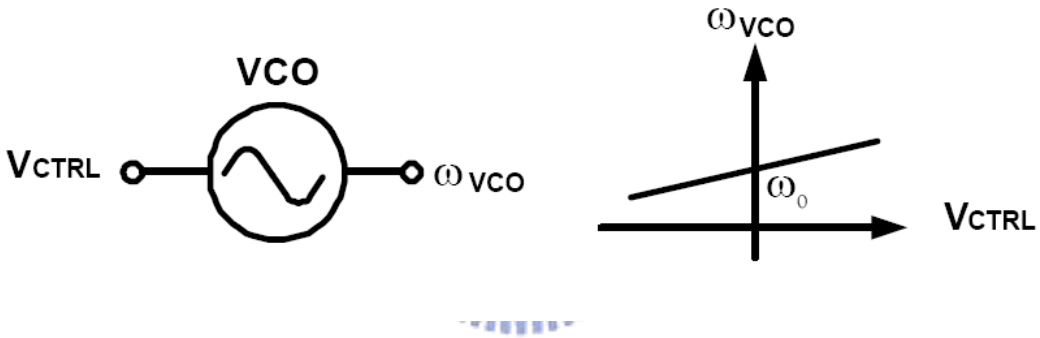

Fig 2.5 The characteristic of VCO

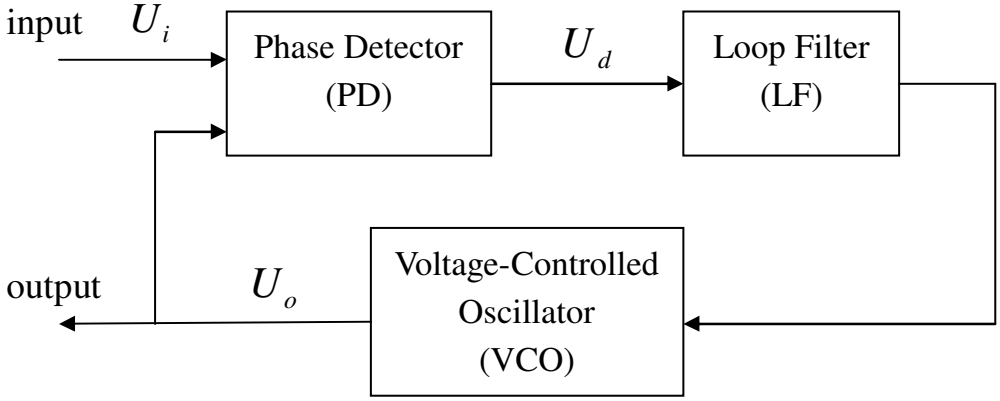

Fig. 2.6 Structure of linear phase-locked loop

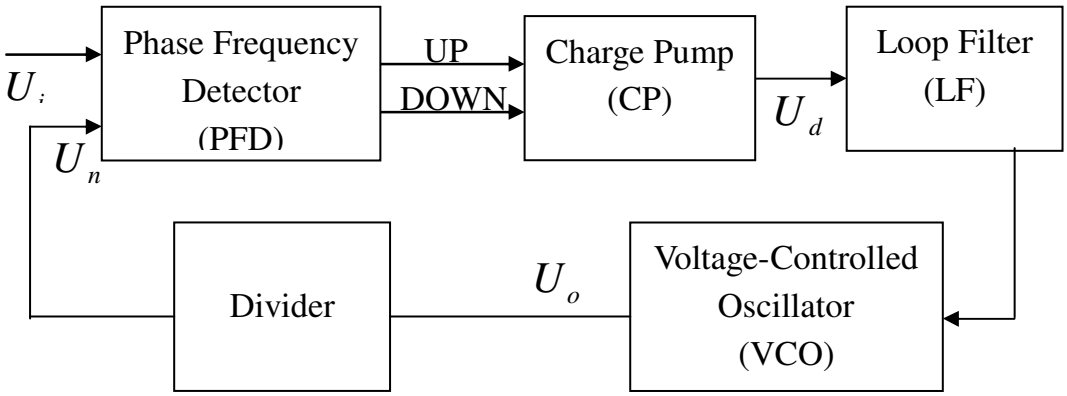

Fig. 2.7 Structure of digital phase-locked loop

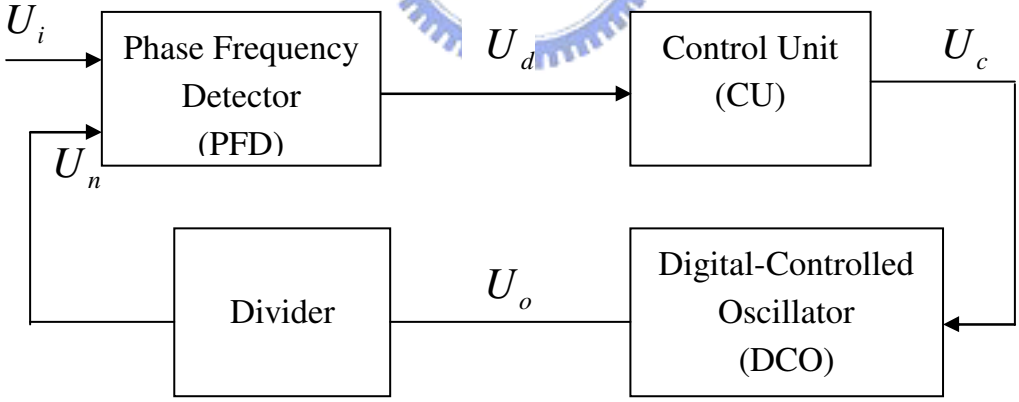

Fig. 2.8 Structure of all-digital phase-locked loop

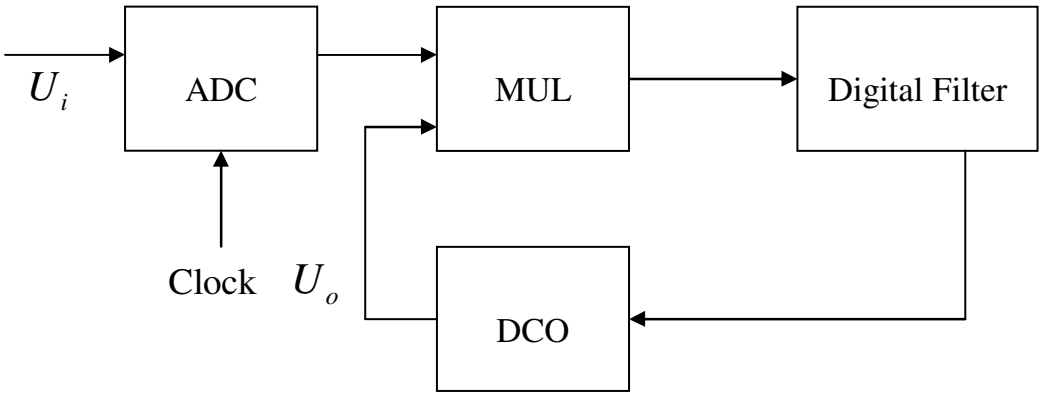

Fig. 2.9 Structure of software simulated linear phase-locked loop

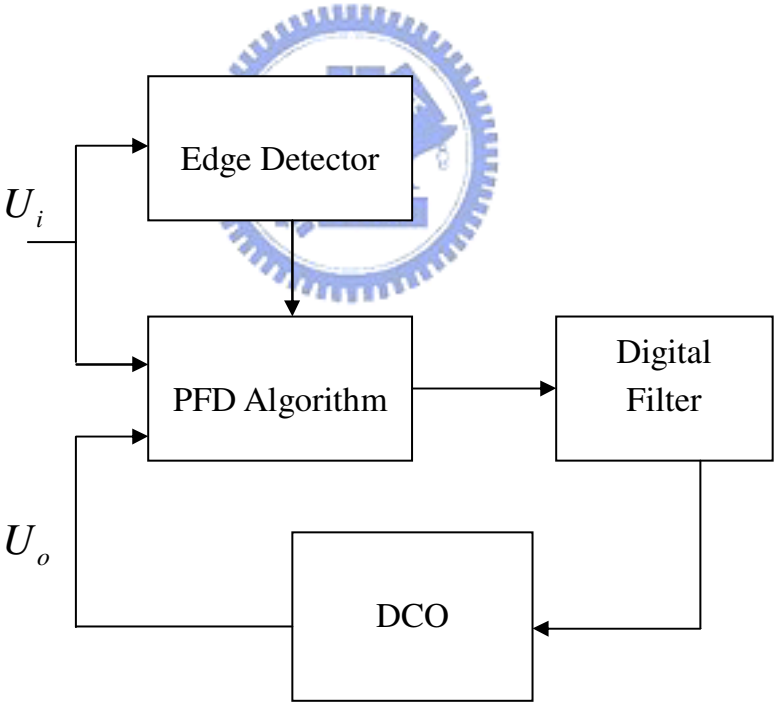

Fig. 2.10 Structure of software simulated digital phase-locked loop

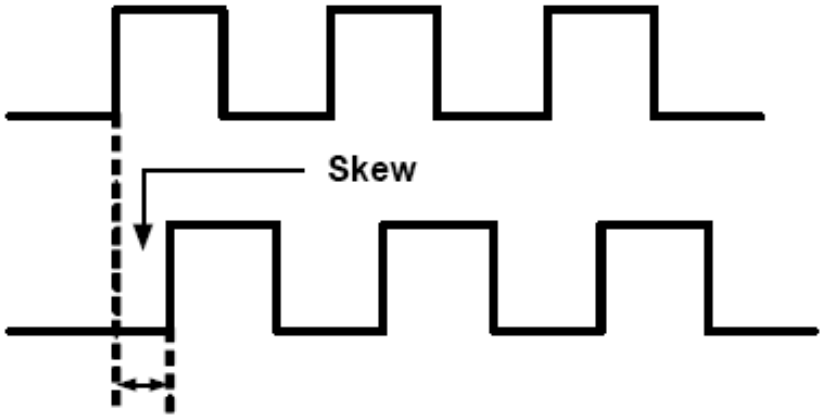

Fig. 2.11(a) Clock skew

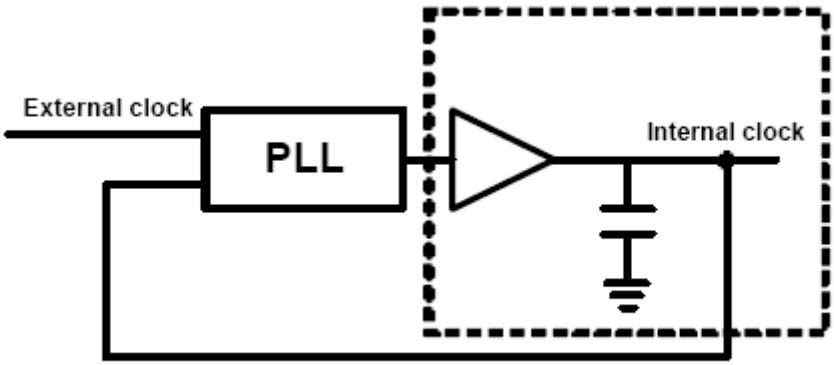

Fig. 2.11(b) Skew reduction

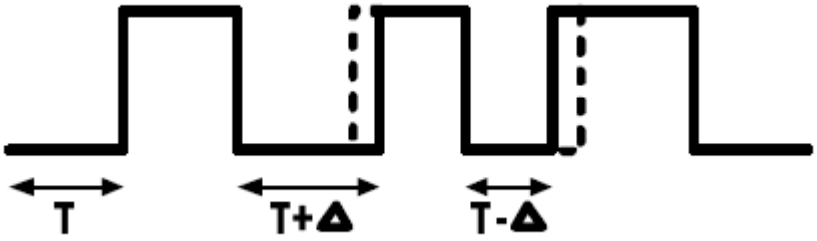

Fig. 2.12 Clock Jitter

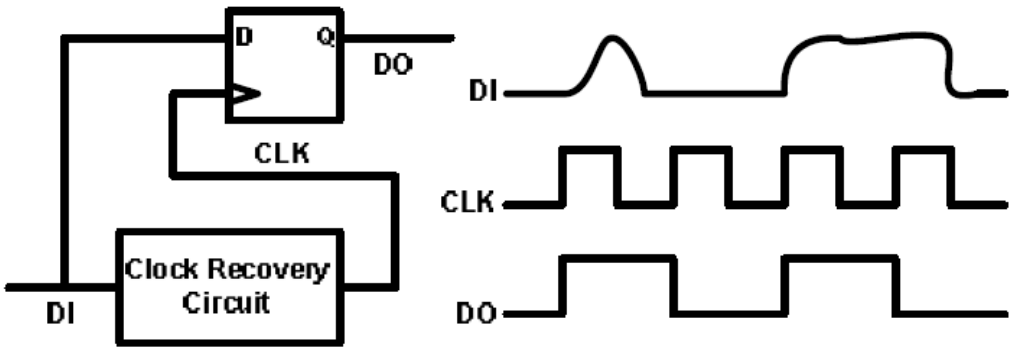

Fig. 2.13 An example of clock and data recovery circuit

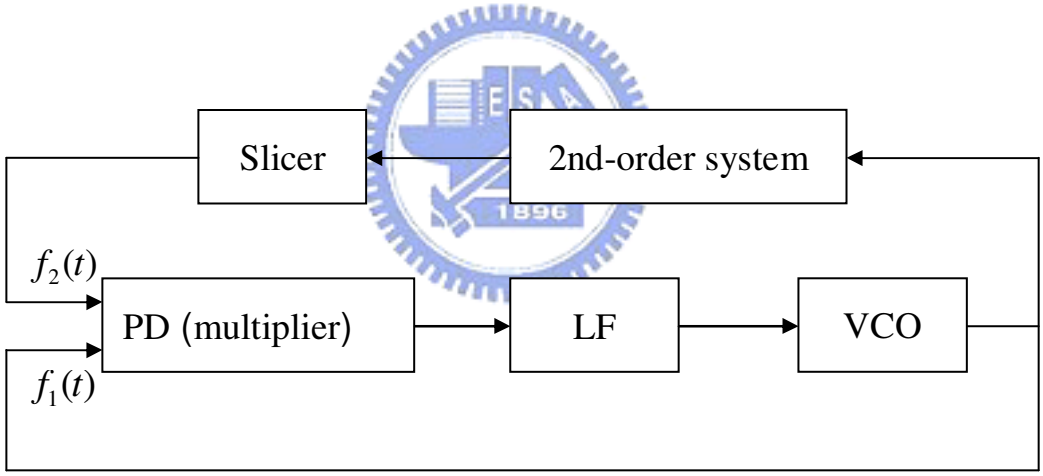

Fig. 3.1 (a) Function block diagram for second order system with PLL (Square wave)

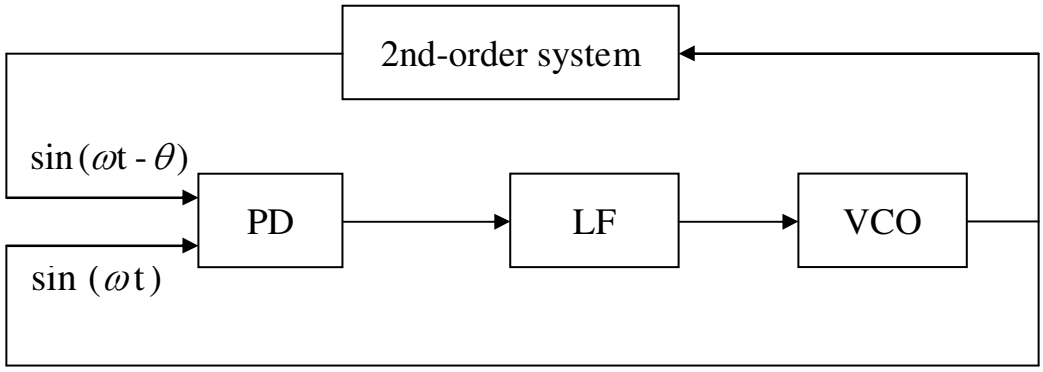

Fig. 3.1 (b) Function block diagram for second order system with PLL (Sine wave)

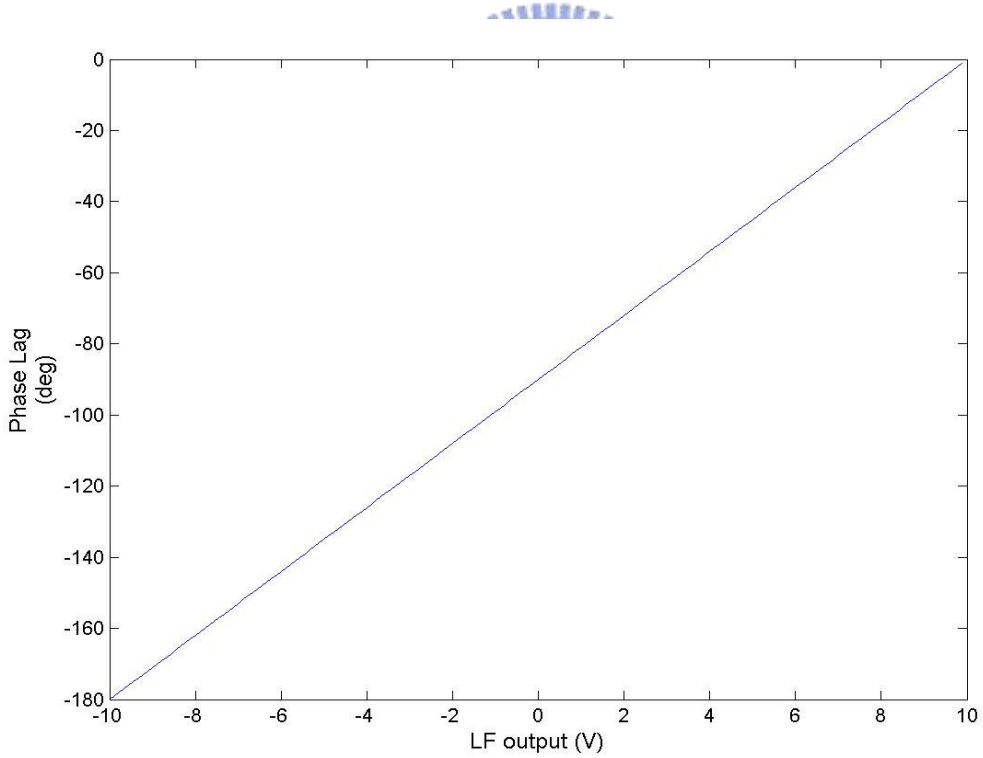

Fig. 3.2 The LF output vs the phase lag

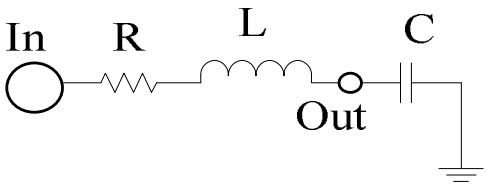

Fig. 4.1 The RLC simulated the second order system

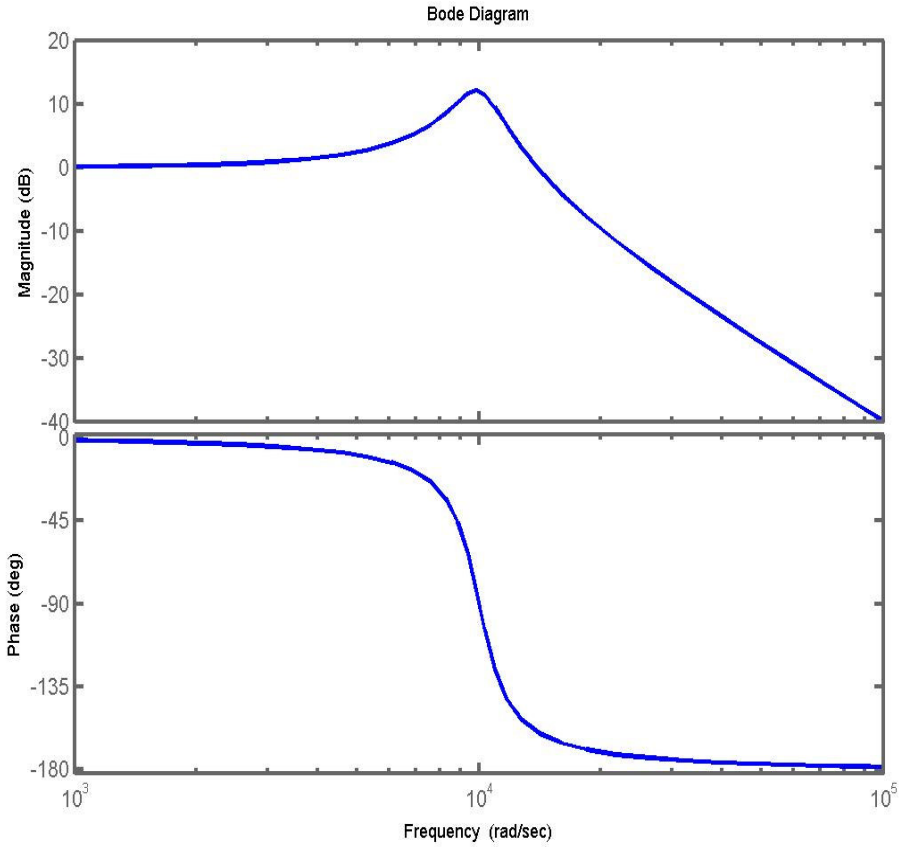

Fig. 4.2 The bode diagram of second order system

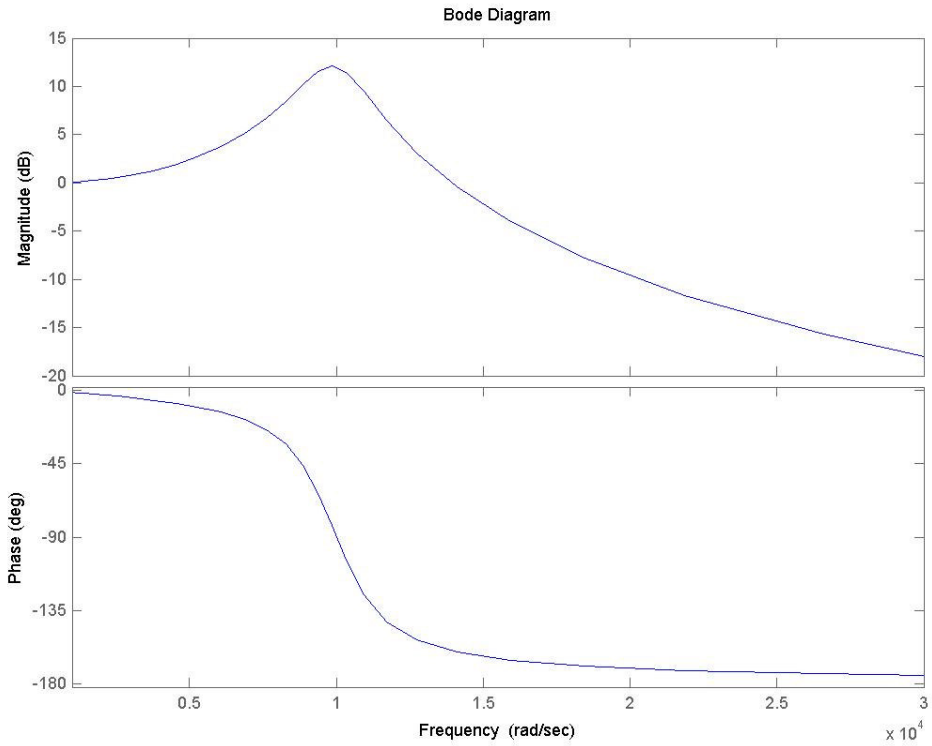

Fig. 4.3 The bode diagram of second order system (linear scale)

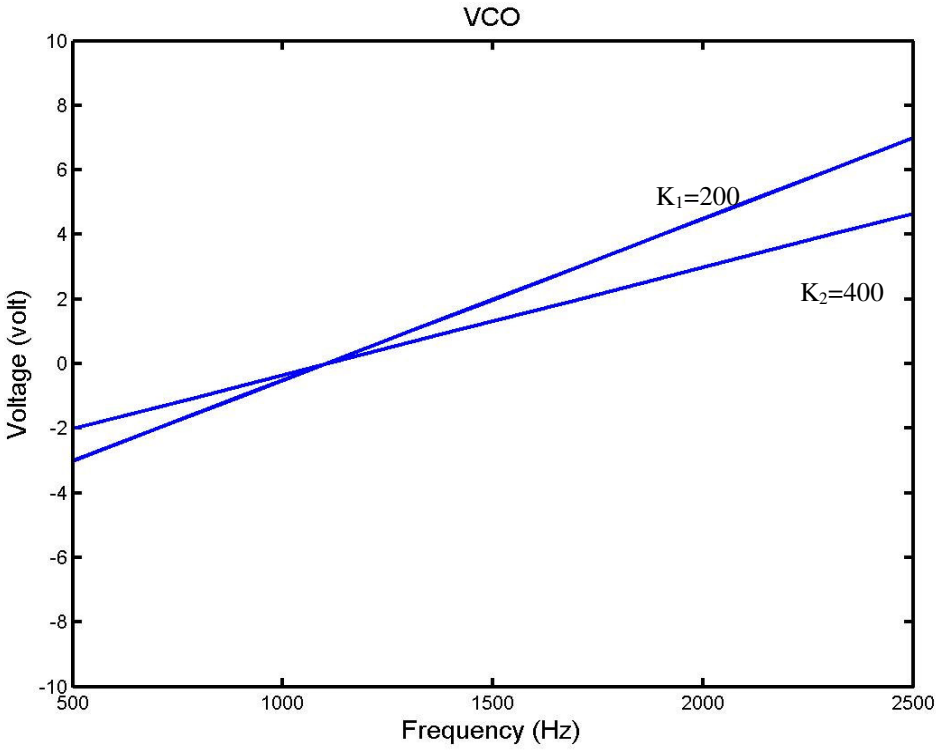

Fig. 4.4 The output frequency of VCO vs the input voltage of VCO

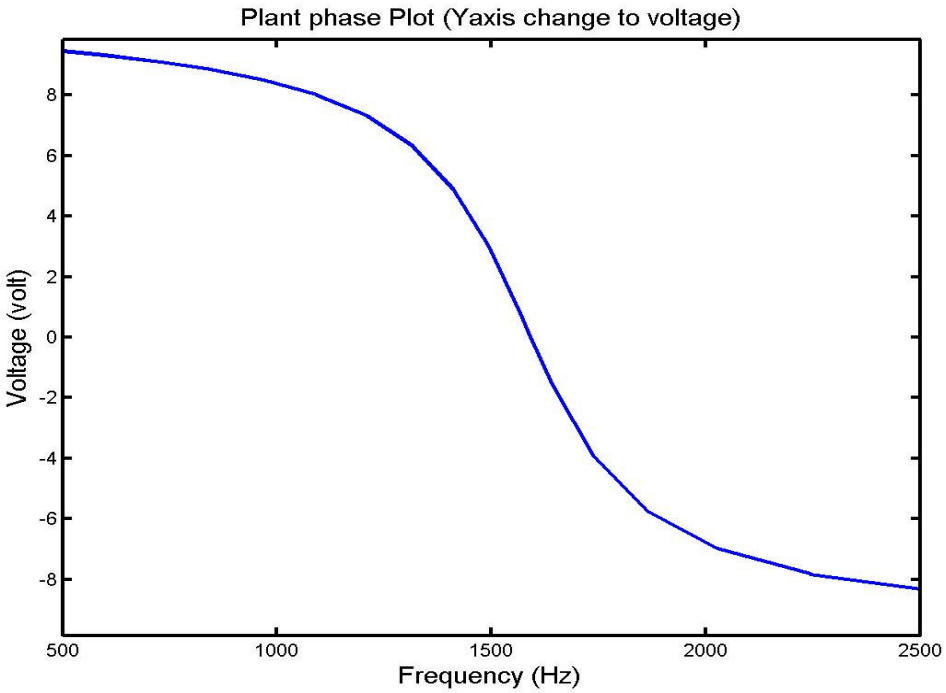

Fig. 4.5 The phase plot (Y-axis change to voltage)

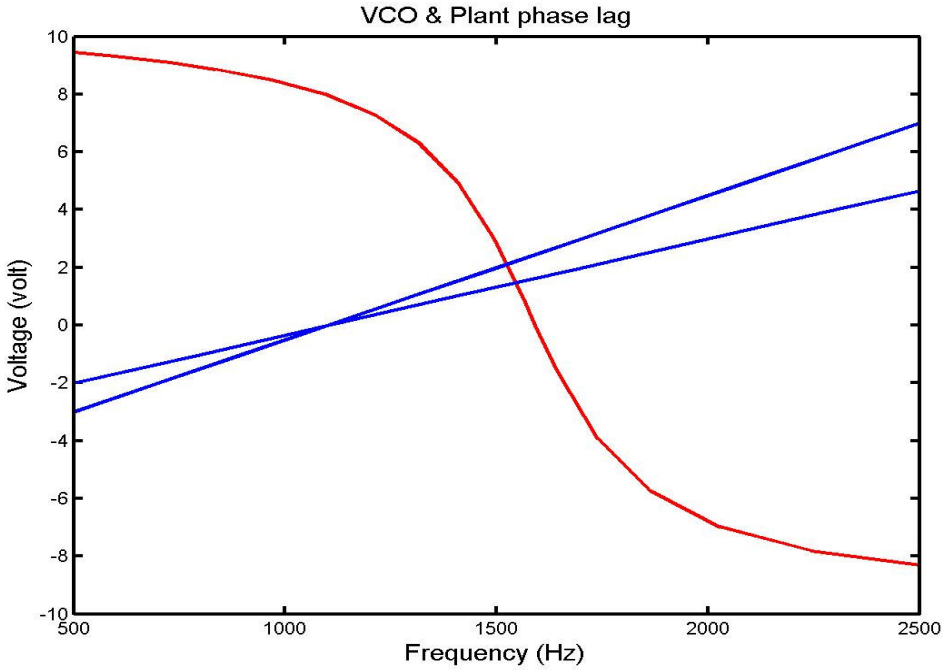

Fig. 4.6 The VCO and the phase plot

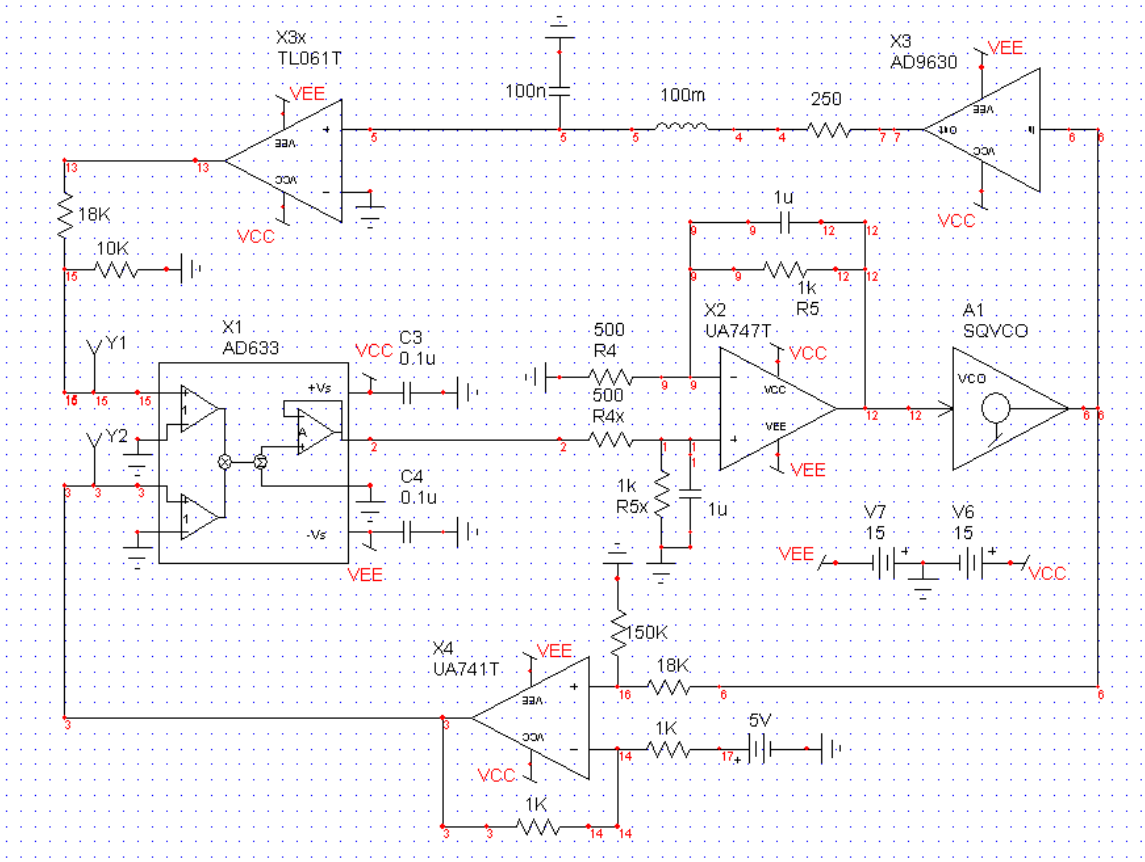

Fig. 4.7 The schematic diagram of testing circuit (Square wave)

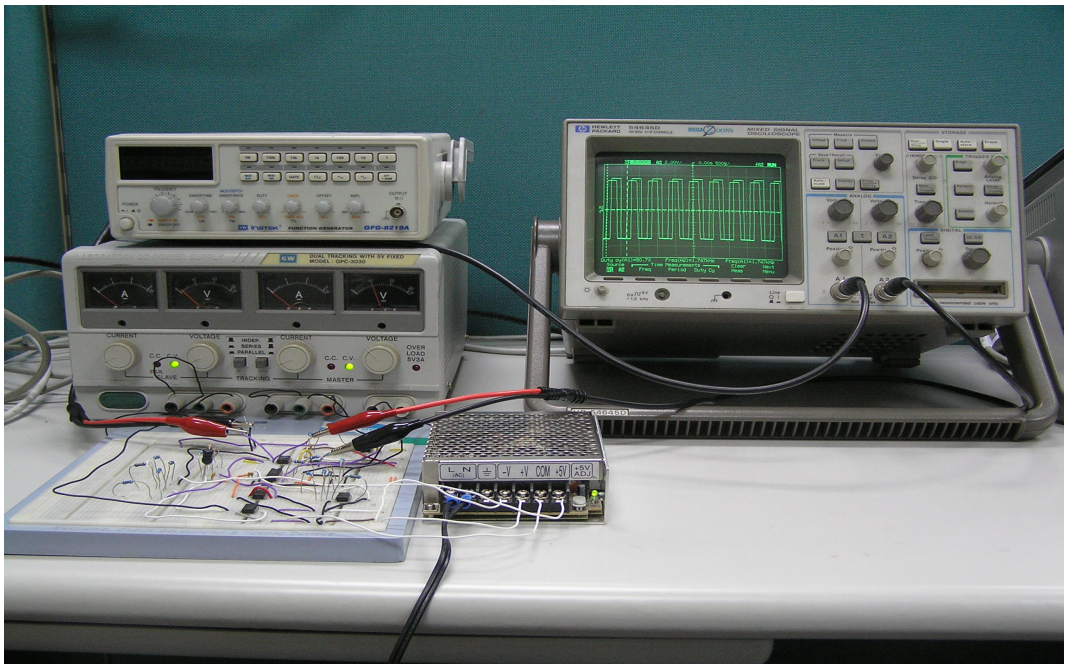

Fig. 4.8 The experimental equipment

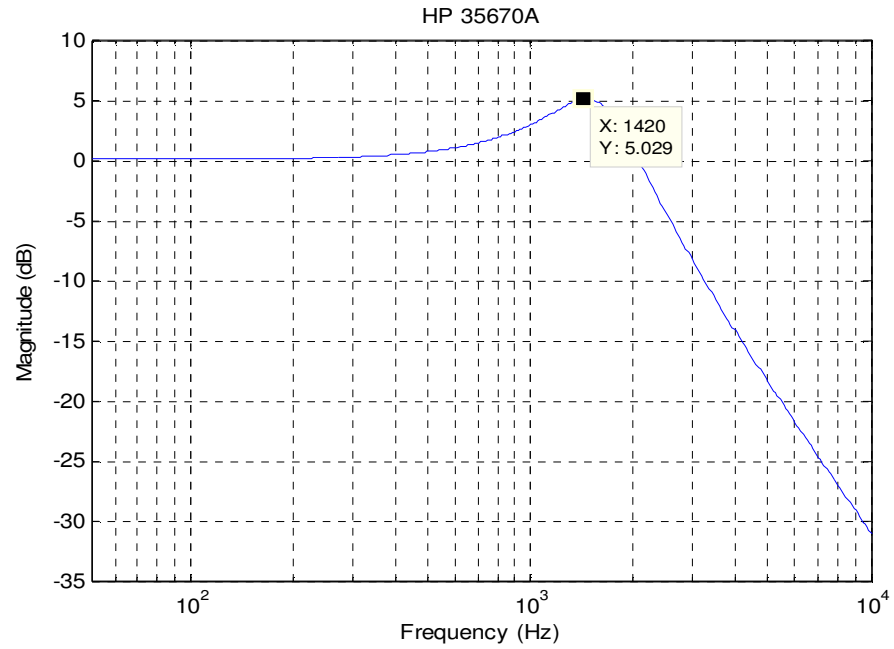

Fig. 4.9 (a) The bode diagram of the emulation plant (Square wave)

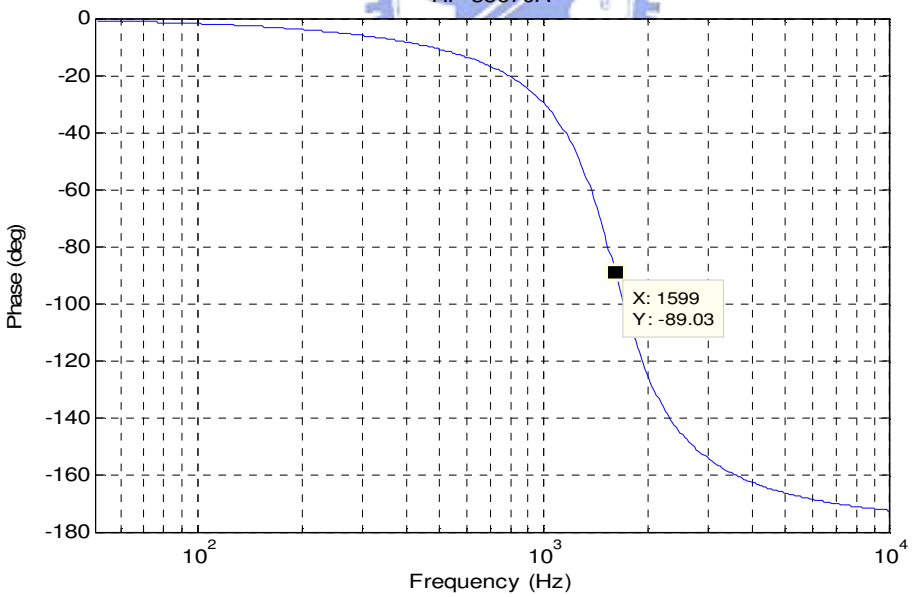

Fig. 4.9 (b) The bode diagram of the emulation plant (Square wave)

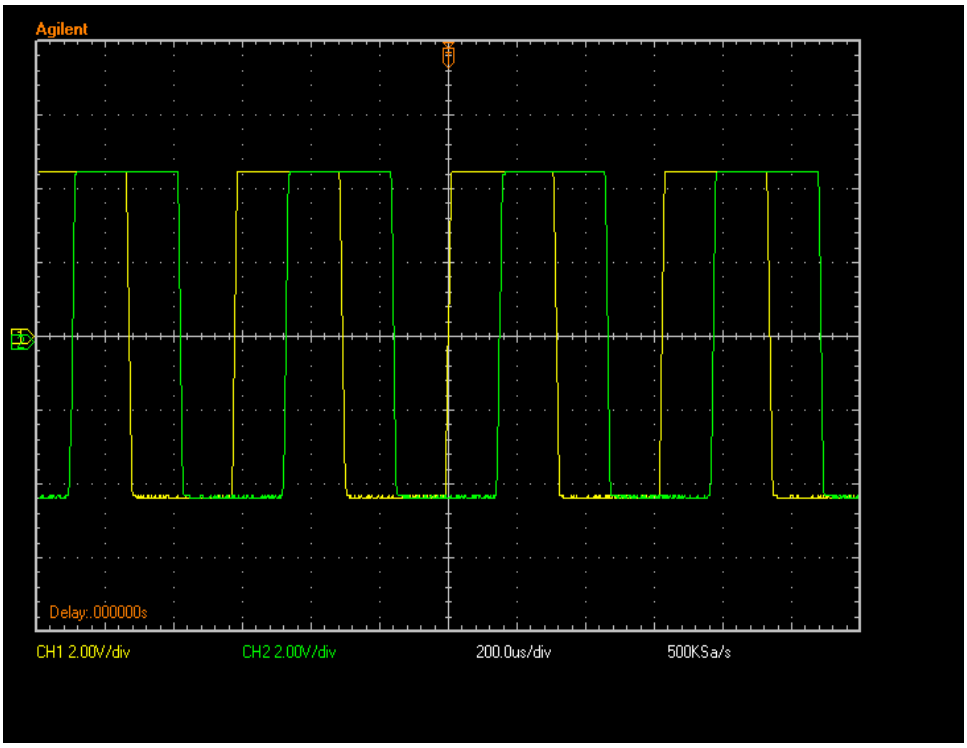

Fig. 4.10 The tracking profile (ω_t=1.516KHz)

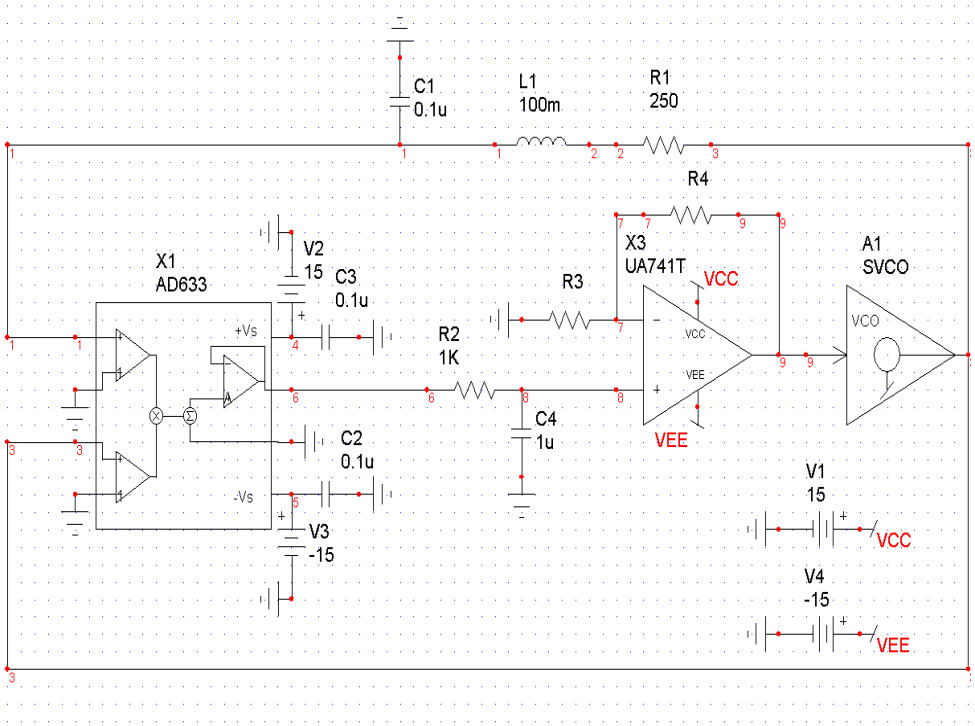

Fig. 4.11 The schematic diagram of testing circuit (Sine wave)

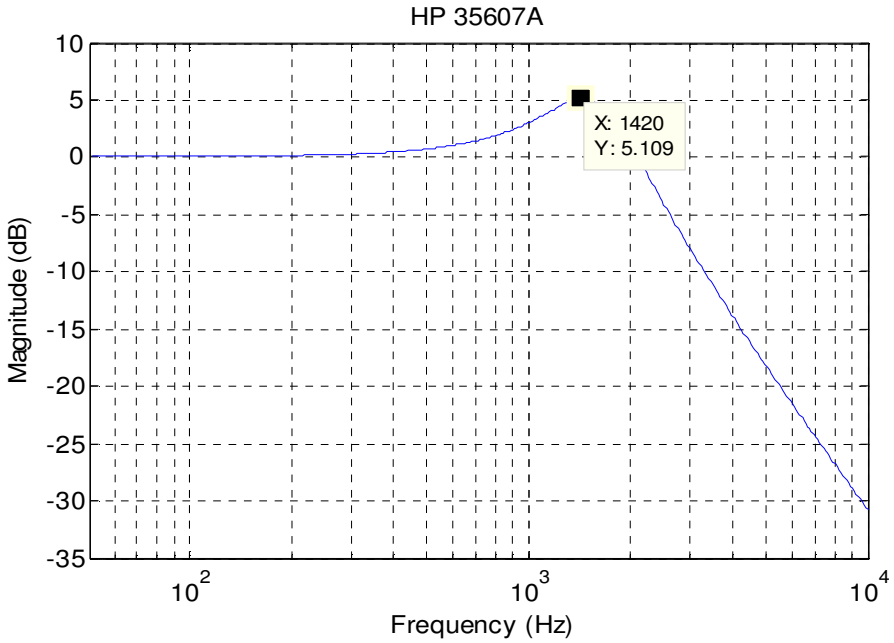

Fig. 4.12 (a) The bode diagram of the emulation plant (Sine wave)

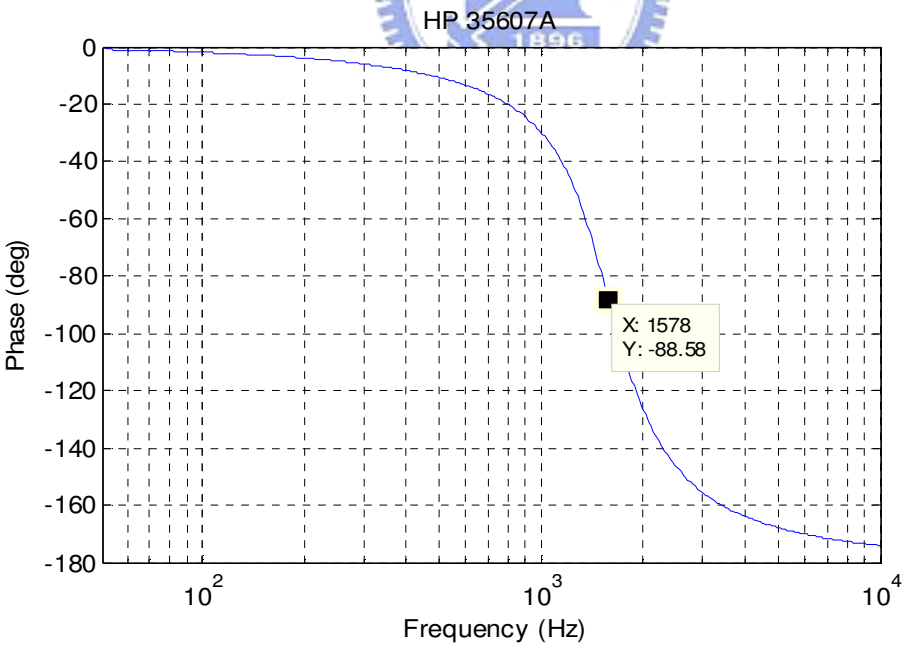

Fig. 4.12 (b) The bode diagram of the emulation plant (Sine wave)

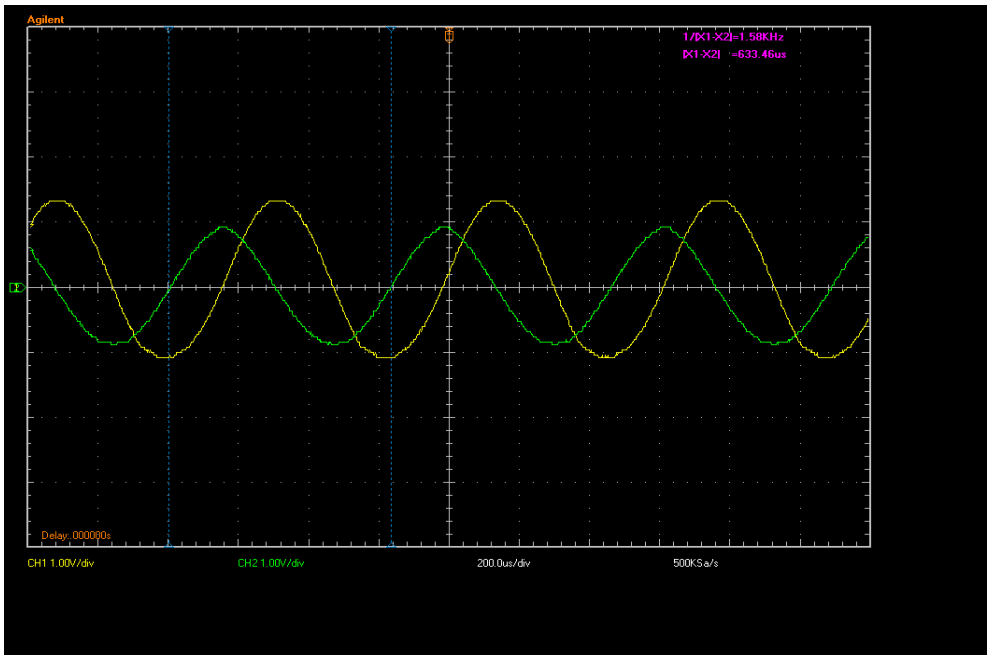

Fig. 4.13 The tracking profile (ω_t=1.580KHz)

Fig. 4.14 The ultrasonic cleaning tank

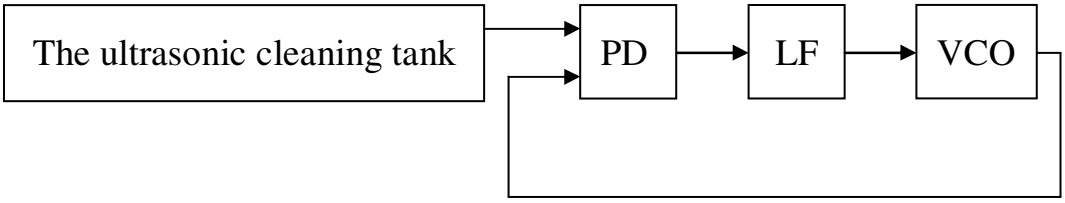

Fig. 4.15 The function block diagram for PLL

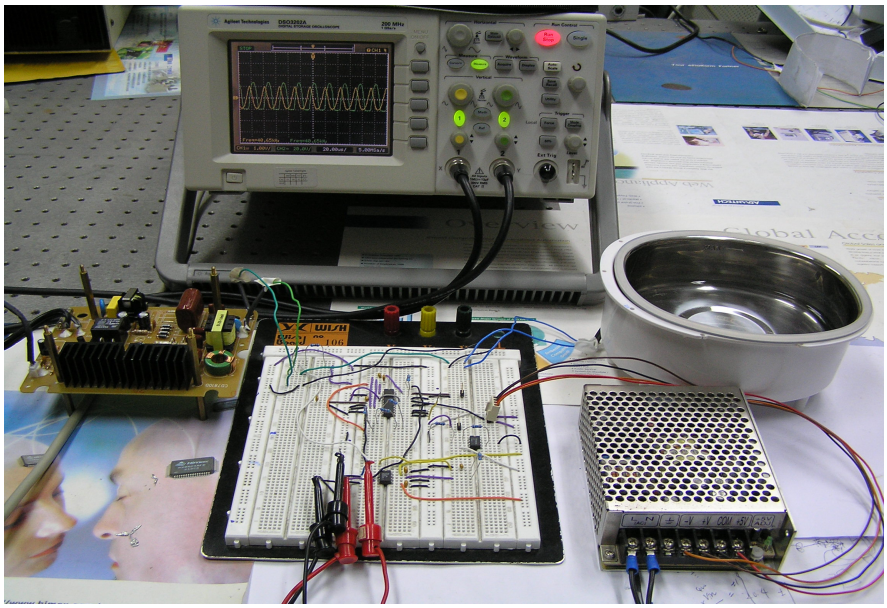

Fig. 4.16 The experimental equipment

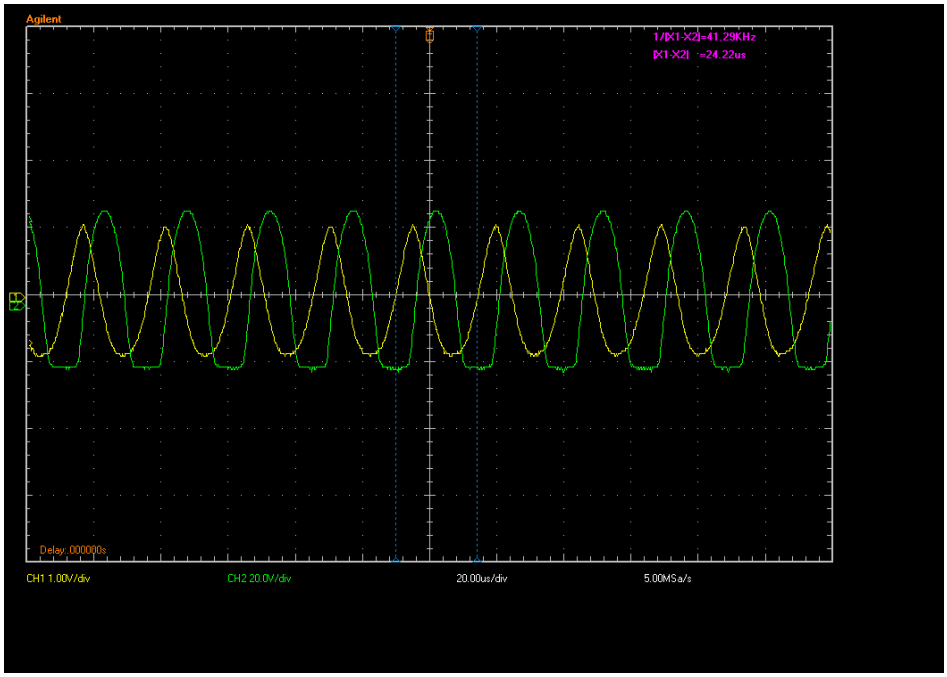

Fig. 4.17 The tracking profile (ω_t=41.29KHz)

Table 2-1 The compare of PLL

	Analog PLL	DPLL	ADPLL
Design methodology	Analog	Analog and digital mixed mode	Digital
Turnaround time	Long	Long	**Short**
Noise immunity	Low	Low	**High**
Oscillator frequency	**High**	**High**	Low
Oscillator resolution	**High**	**High**	Low
Lock time	Long	Long	**Short**
Power consumption	Large	Large	**Small**
Area	Large	Large	**Small**

(The boldface words represent advantages.)

Table 4-1 (a) The compare of identification data and experimental results

Plant Parameters		R=250Ω L = 100mH C = 0.1uF			
Emulation plant identification data					
Theoretical Calculation	ω_n	1.592KHz			
	ς	0.125			
HP35670A Identification	ω_n	1.5995KHz			
	ς	0.325			
Experiment data of estimation & tracking frequency					
Estimation	ω_n	1.533KHz	1.554KHz	1.550KHz	1.585KHz
	ς	0.312	0.308	0.345	0.326
Tracking Frequency	ω_{t1}	1.496KHz	1.516KHz	1.507KHz	1.545KHz
Phase	θ_1	85.494°	85.431°	85.343°	85.576°
Tracking Frequency	ω_{t2}	1.460KHz	1.486KHz	1.473KHz	1.502KHz
Phase	θ_2	81.085°	81.757°	81.603°	80.693°

(PLL output is square waves)

Table 4-1 (b) The compare of identification data and experimental results

Plant Parameters		R=100Ω, L = 100mH, C = 0.1uF			R=500Ω, L = 100mH, C = 0.1uF		
Emulation plant identification data							
Theoretical Calculation	ω_n	1.592KHz			1.592KHz		
	ς	0.05			0.25		
HP35670A Identification	ω_n	1.600KHz			1.599KHz		
	ς	0.249			0.425		
Experiment data of estimation & tracking frequency							
Estimation	ω_n	1.529KHz	1.541KHz	1.578KHz	1.565KHz	1.581KHz	1.595KHz
	ς	0.269	0.263	0.251	0.439	0.449	0.405
Tracking Frequency	ω_{t1}	1.490KHz	1.504KHz	1.545KHz	1.513KHz	1.527KHz	1.545KHz
Phase	θ_1	84.564°	84.771°	85.226°	85.608°	85.574°	85.524°
Tracking Frequency	ω_{t2}	1.464KHz	1.477KHz	1.518KHz	1.460KHz	1.473KHz	1.500KHz
Phase	θ_2	80.868	80.882°	81.263°	81.017°	81.033°	81.397°

(PLL output is square waves)

Table 4-1 (c) The compare of identification data and experimental results

Plant Parameters		R=100**Ω,** L = 50mH, C = 0.1uF			R=500**Ω,** L = 50mH, C = 0.1uF		
Emulation plant identification data							
Theoretical Calculation	ω_n	2.251KHz			2.251KHz		
	ς	0.071			0.354		
HP35670A Identification	ω_n	2.534KHz			2.314KHz		
	ς	0.224			0.425		
Experiment data of estimation & tracking frequency							
Estimation	ω_n	2.453KHz	2.498KHz	2.534KHz	2.210KHz	2.246KHz	2.280KHz
	ς	0.198	0.23	0.217	0.400	0.411	0.416
Tracking Frequency	ω_{t1}	2.417KHz	2.454KHz	2.494KHz	2.085KHz	2.166KHz	2.144KHz
Phase	θ_1	85.685°	85.565°	85.822°	81.744°	81.743°	81.585°
Tracking Frequency	ω_{t2}	2.378KHz	2.413KHz	2.452KHz	2.143KHz	2.176KHz	2.205KHz
Phase	θ_2	81.033°	81.414°	81.402°	85.628°	85.595°	85.402°

(PLL output is square waves)

Table 4-2 (a) The compare of identification data and experimental results

Plant Parameters		R=250Ω, L = 100mH, C = 0.1uF			R=500Ω, L = 100mH, C = 0.1uF		
Emulation plant identification data							
Theoretical Calculation	ω_n	1.592KHz			1.592KHz		
	ς	0.125			0.25		
HP35670A Identification	ω_n	1.5785KHz			1.5785KHz		
	ς	0.308			0.415		
Experiment data of estimation & tracking frequency							
Estimation	ω_n	1.522KHz	1.534KHz	1.539KHz	1.541KHz	1.524KHz	1.505KHz
	ς	0.313	0.33	0.301	0.385	0.403	0.425
Tracking Frequency	ω_{t1}	1.563KHz	1.577KHz	1.618KHz	1.630KHz	1.616KHz	1.600KHz
VCO Initial Frequency	ω_{01}	1.202KHz	1.212KHz	1.004KHz	1.253KHz	1.242KHz	1.233KHz
Tracking Frequency	ω_{t2}	1.608KHz	1.623KHz	1.577KHz	1.695KHz	1.684KHz	1.673KHz
VCO Initial Frequency	ω_{02}	0.986KHz	1.002KHz	1.212KHz	1.115KHz	1.106KHz	1.097KHz

(PLL output is sine waves)

Table 4-2 (b) The compare of identification data and experimental results

Plant Parameters		R=250Ω, L = 50mH, C = 0.1uF			R=500Ω, L = 50mH, C = 0.1uF		
Emulation plant identification data							
Theoretical Calculation	ω_n	2.251KHz			2.251KHz		
	ς	0.177			0.354		
HP35670A Identification	ω_n	2.195KHz			2.314KHz		
	ς	0.248			0.425		
Experiment data of estimation & tracking frequency							
Estimation	ω_n	2.071KHz	2.098KHz	2.136KHz	2.297KHz	2.272KHz	2.246KHz
	ς	0.246	0.237	0.214	0.427	0.419	0.419
Tracking Frequency	ω_{t1}	2.176KHz	2.201KHz	2.230KHz	2.339KHz	2.312KHz	2.286KHz
VCO Initial Frequency	ω_{01}	1.664KHz	1.681KHz	1.704KHz	1.805KHz	1.786KHz	1.761KHz
Tracking Frequency	ω_{t2}	2.255KHz	2.275KHz	2.300KHz	2.370KHz	2.342KHz	2.315KHz
VCO Initial Frequency	ω_{02}	1.464KHz	1.482KHz	1.495KHz	1.563KHz	1.546KHz	1.529KHz

(PLL output is sine waves)

Table 4-3 The specifications of the ultrasonic cleaning tank

ITEM NUMBER	SS-802A
NAME	DIGITAL ULTRASONIC CLEANER
POWER SUPLY	AC 100~120V 50/60Hz
POWER	35W
WEIGHT	1.00kg
Ultrasonic frequency	42000Hz

Table 4-4 The experimental results (Water)

Estimation	ω_n	42.176KHz	42.252KHz	42.358KHz	42.449KHz	42.586KHz
	ς	0.2578	0.2569	0.2566	0.2570	0.2596
Tracking Frequency	ω_{t1}	41.54KHz	41.62KHz	41.72KHz	41.81KHz	41.93KHz
VCO Initial Frequency	ω_{01}	45.41KHz	45.51KHz	45.62KHz	45.71KHz	45.90KHz
Tracking Frequency	ω_{t2}	40.40KHz	40.43KHz	40.48KHz	40.53KHz	40.60KHz
VCO Initial Frequency	ω_{02}	53.02KHz	53.53KHz	54.10KHz	54.50KHz	55.00KHz

	ω_n	ς
Average	42.364KHz	0.25759
Standard deviation	161.580Hz	0.00121

Table 4-5 The experimental results (Oil)

Estimation	ω_n	42.371KHz	42.286KHz	42.473KHz	42.206KHz	42.554KHz
	ς	0.2760	0.2747	0.2767	0.2771	0.2764
Tracking Frequency	ω_{t1}	41.62KHz	41.54KHz	41.72KHz	41.46KHz	41.80KHz
VCO Initial Frequency	ω_{01}	45.94KHz	45.83KHz	46.02KHz	45.71KHz	46.11KHz
Tracking Frequency	ω_{t2}	40.44KHz	40.41KHz	40.49KHz	40.36KHz	40.53KHz
VCO Initial Frequency	ω_{02}	53.25KHz	52.85KHz	53.70KHz	52.42KHz	54.10KHz

	ω_n	ς
Average	42.378KHz	0.27618
Standard deviation	139.730Hz	0.00092

Table 4-6 The experimental results (Ink)

Estimation	ω_n	42.125KHz	42.057KHz	41.956KHz	42.296KHz	42.212KHz
	ς	0.2579	0.2619	0.2592	0.2623	0.2594
Tracking Frequency	ω_{t1}	41.46KHz	41.38KHz	41.29KHz	41.61KHz	41.54KHz
VCO Initial Frequency	ω_{01}	45.52KHz	45.45KHz	45.34KHz	45.73KHz	45.62KHz
Tracking Frequency	ω_{t2}	40.37KHz	40.35KHz	40.30KHz	40.45KHz	40.43KHz
VCO Initial Frequency	ω_{02}	52.80KHz	52.12KHz	51.80KHz	53.40KHz	53.00KHz

	ω_n	ς
Average	42.129KHz	0.26014
Standard deviation	132.199Hz	0.00189

Table 4-7 The experimental results (500ml Water)

Estimation	ω_n	41.848KHz	41.743KHz	41.697KHz	41.651KHz	41.626KHz
	ς	0.2564	0.2522	0.2541	0.2566	0.2595
Tracking Frequency	ω_{t1}	40.60KHz	40.53KHz	40.48KHz	40.43KHz	40.400KHz
VCO Initial Frequency	ω_{01}	48.89KHz	48.71KHz	48.62KHz	48.51KHz	48.41KHz
Tracking Frequency	ω_{t2}	39.50KHz	39.45KHz	39.41KHz	39.36KHz	39.30KHz
VCO Initial Frequency	ω_{02}	58.00KHz	57.80KHz	57.50KHz	57.30KHz	57.28KHz

	ω_n	ς
Average	41.713KHz	0.25576
Standard deviation	87.657Hz	0.00276