Chapter 1

Introduction

1.1 Supercritical Fluid Technology

Supercritical fluids are compounds above their critical temperatures and pressure, as shown in Fig 1-1 [1, 2]. The attractiveness of supercritical fluids for commercial applications is their unique combination of liquid-like and gas-like properties. The Table 1-1 shows critical temperature and pressure for some common fluids. CO_2-based supercritical fluids are particularly attractive because CO_2 is non-toxic, non-flammable, and inexpensive. Besides, its critical conditions are easily achievable with existing process equipment (31 °C, 1072 psi =72.8 atm).

Figure 1-2 shows the density-pressure-temperature surface for pure CO_2. It can be discovered that relatively small changes in temperature or pressure near the critical point, resulting in large changes in density. Table 1-2 shows the comparison of several physical properties of typical liquid, vapor, and supercritical fluid state for CO_2. It could be seen that supercritical CO_2 ($SCCO_2$) fluids possesses liquid-like density, so that $SCCO_2$ fluids are analogous with light hydrocarbon to dissolve most solutes and own exceptional transport capability [3, 4]. On the other hand, $SCCO_2$ fluids hold gas-like characteristic due to their viscosity and surface tension are extremely low, it allows $SCCO_2$ fluids to keep fine diffusion capability and enter the nano-scale pores or spaces without damage. These properties are the reasons for $SCCO_2$ fluids to employ in many commercial applications, including the extraction of caffeine from coffee, fats from foods, and essential oils from plants for using in perfumes. Furthermore, in last years, many records are investigated with $SCCO_2$ fluids to apply in semiconductor fabrication, such as cleaning wafer and stripping photoresist, by means of its high mass transfer rates and infiltration capabilities [4-6].

1.2　General Background

1.2.1 Metal Oxide dielectric films (High dielectric constant material, High-k)

The Majority of metal oxide dielectric films, such as Al_2O_3, Ta_2O_5 and HfO_2, hold higher dielectric constant than oxide, and studied to replace the gate dielectric layer for future generation CMOS devices because of the lower leakage current and thicker physics thickness than thermal oxide (SiO_2) under identical equivalent oxide thicknesses (EOT) [7, 8]. Additionally, due to the property of high dielectric constant, the oxide metal materials are taken as replacement for blocking oxide of SONOS memory device [7]. The better voltage coupling on tunneling oxide of memory device could be achieved by the utilization of metal oxide material, and leading to superior carrier program/erase speed. For thin film transistors, in pervious records, the use of low-temperature-deposited metal oxide films as gate dielectrics not only reduces the threshold voltage to near zero for pentacene and zinc oxide (ZnO_2) TFTs but also the thickness of the gate insulator to nanometer scale [9, 10]. For extending the application, the novel method to improve the quality of metal oxide films is necessary.

1.2.2 Amorphous silicon thin film transistor

In recent years, the liquid crystal displays (LCDs) are widely used in digital products, such as notebook computer, television, cell phone and personal digital assistant (PDA). Amorphous silicon thin film transistors (a-Si:H TFTs) were reported by LeComber et al. for the first time in 1979 [11], and have been commonly employed as the switch elements of pixel in LCDs due to lower cost (compare with poly-silicon transistors) and agreeing with glass substrates (i.e. low-temperature fabrication). The on-off ratio of a-Si:H TFTs, defined as the ratio of transistor current in on-state and off-state, is larger than six orders (10^6), and it satisfies the requirement for application of switching elements. Excluding pixel switch, the a-Si:H TFTs is also proposed to fabricate the driver circuit in displays. Therefore, the investigation on a-Si:H TFTs for enhancing the performance of electric characteristic is very important.

1.2.3 Nanocrystal nonvolatile memories

Nanocrystal nonvolatile memories are one particular implementation of storing charges by dielectric-surrounded nanodots, and were first introduced in the early 1990s by IBM researchers who proposed flash memory with a granular floating gate made from silicon nanocrystals, In a nanocrystal nonvolatile semiconductor memory device, charge is not stored on a continuous floating-gate poly-Si layer, but instead on a layer of discrete, mutually isolated, crystalline nanocrystals or dots. Each dot will typically store only a handful of electrons; collectively the charges stored in these dots control the channel conductivity of the memory transistor.

As compared to conventional stacked gate nanocrystal nonvolatile semiconductor memory devices, nanocrystal charge storage offers several advantages, the main one being the potential to use thinner tunnel oxide without sacrificing nonvolatility. This is a quite attractive proposition since reducing the tunnel oxide thickness is a key to lowering operating voltages and/or increasing operating speeds. This claim of improved scalability results not only from the distributed nature of the charge storage, which makes the storage more robust and fault-tolerant, but also from the beneficial effects of Coulomb blockade. Quantum confinement effects (bandgap widening; energy quantization) can be exploited in sufficiently small nanocrystal geometries to further enhance the memory's performance.

Due to the less drain to floating-gate coupling, nanocrystal memories suffer less from drain induced barrier lowering. One way to exploit this advantage is to use a higher drain bias during the read operation, thus improving memory access time. Of particular importance is the low capacitive coupling between the external control gate and the nanocrystal charge storage layer. This does not only results in higher operating voltages, thus offsetting the benefits of the thinner tunnel oxide, but also removes an important design parameter typically used to optimize the performance and reliability tradeoff.

Unlike volume distributed charge traps, nanocrystals be deposited in a

two-dimensional layer at a fixed distance from the channel separated by a thin tunnel oxide. By limiting nanocrystals deposition to just one layer and adjusting the thickness of the top blocking dielectric, charge leakages to the control gate from the storage nodes can be effectively prevented.

1.3   Motivation

Metal oxide dielectrics, such as Al_2O_3, Ta_2O_5 and HfO_2, have attracted much attention for memory cell capacitors and gate dielectric applications in the ultra large scale integration (ULSI) technology [7, 8]. Among several metal oxide film formation methods [7, 8, 12], in general, low-temperature technology is welcome due to a low thermal budget process. Also, it is suitable for thin film transistor liquid crystal displays (TFT-LCDs) technology on the base of glass substrates or plastics. However, the low-temperature-deposited dielectric films perform inferior properties and larger current leakage due to numerous traps inside the metal oxide film [13, 14]. It is thereby required for the low-temperature-deposited metal oxide film to reduce electrical traps by implementing a post-treatment process. High-temperature (>600 °C) annealing is typically used to diminish the traps in metal-oxide films [14-16]. Nevertheless, there are several considerable issues present for high-temperature annealing process. For example, crystallizing phenomenon would occur possibly during the process duration, and leads to unexpected leakage current through grain boundaries [16-18]. Additionally, the high-temperature process is not applicable to the substrates with low glass transition temperature (T_g), such as glasses and plastics [19]. The supercritical fluids technology has been applied to remove photoresist and impurity in integrated circuit (IC) fabrications [20]. It is also operative method to extract moisture from nano-scale structures, such as porous dielectric-material and carbon nano-tube [21, 22]. By the liquid-like property, it is allowed for supercritical fluids to own fine transport capability [26]. Supercritical fluids, in addition, hold gas-like and high-pressure properties to efficiently diffuse into thin films with no

damage. Here, these advantages would be adequately employed to passivate the defects in low- temperature-deposited metal oxide dielectric film at 150 °C.

Besides, amorphous silicon thin film transistor (a-Si:H TFTs) are widely used in the active matrix liquid crystal displays (AMLCDs) as switch device [27, 28]. The excellent transfer characteristics are thereby demanded, such as high mobility and lower threshold voltage. Especially, in recent years, the fabrication of a-Si:H TFTs tends to being implemented at low temperature processes for cost down and comparable with plastic substrates (120~250 °C) [19]. The performance of low-temperature-fabricated a-Si:H TFTs, however, is unsuitable for application to display technology, due to the poor a-Si film dielectrics with plenty of defects. For improving electrical characteristics of a-Si TFTs, it is necessary to passivate the defect-states in mobility gap of a-Si:H film. The $O_2/H_2/NH_3$ plasma treatments were traditionally applied to reduce these defects [29, 30]. Moreover, in other records, high-pressure H_2O vapor was used to reduce the dangling bond at the SiO_2/Si interface and grain boundaries for poly-Si TFTs [31-32]. Nevertheless, these processes always require a high temperature ambient (>200 °C). For example, high-pressure H_2O vapor method needs high temperature (>25O °C) to achieve enough pressure for H_2O molecule diffusing into poly-silicon film and repairing silicon dangling bonds. Therefore, it is critical to develop a traps passivation technology at low temperature for extending the application of a-Si:H TFTs. In this work, therefore, the supercritical fluids treatment is also proposed to effectively decrease the defects in a-Si:H TFTs at low temperature.