國　立　交　通　大　學

光電工程學系暨顯示科技研究所

碩 士 論 文

具輕摻雜汲極結構之多晶矽薄膜電晶體之溫度效應研究

Study on Temperature Response of Poly-Si TFT's with LDD Structure

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摘　要

多晶矽薄膜電晶體在面板技術的應用上，由於具有高遷移率，有機會整合面板周邊電路，實現系統面板（System on Panel）的目標。而在實際的應用上，多晶矽薄膜電晶體通常會使用輕摻雜汲極結構。在本論文中，我們將分別針對多晶矽薄膜電晶體的載子遷移率，以及輕摻雜汲極區域所造成的寄生電阻效應，做相關的實驗分析與研究，尤其著重於遷移率與寄生電阻的溫度效應。

首先，我們提出一個遷移率模型，此模型是以熱電子發射效應以及聲子散射效應交互作用後所產生之溫度效應作為理論基礎來建構。我們利用該遷移率模型，針對無輕摻雜汲極結構的元件進行載子遷移率的模擬。而不論是在遷移率的模擬或是在元件電流特性的模擬中，都可以在不同的閘極偏壓與不同的環境溫度之下，分別得到與遷移率萃取值以及元件電流測量值相當吻合的結果。

接下來，我們討論了輕摻雜汲極結構所造成的寄生電阻效應。針對具輕摻雜汲極結構的元件，我們先由其電流特性計算出元件電阻，再以無輕摻雜汲極結構元件的電阻作為參考電阻，將其電阻相減，即可得到輕摻雜汲極區域所造成的寄生電阻。而根據由此萃取出的寄生電阻結果，我們發現寄生電阻會受到閘極偏壓的調變，而且對越短的輕摻雜汲極長度而言，其寄生電阻受到閘極偏壓調變的情形會越嚴重。

接著，我們利用 Silvaco 元件模擬軟體，針對具輕摻雜汲極的元件結構進行元件模擬的工作。根據元件模擬的結果，可以推論出在閘極電極的周圍，存在一個寄生電晶體，並且在溫度效應上，同樣受到熱電子發射效應的影響。此外，在距離閘極電極較遠的輕摻雜汲極區域，並不受到閘極偏壓的調變，因此在同一溫度下可視為定電阻，而在合理的推論下，我們認為此段未受閘極偏壓調變之輕摻雜汲極區域電阻，其溫度效應是由雜質散射效應所主導。

最後，我們根據上述的假設與分析，針對具輕摻雜汲極結構的元件，提出了一個包含溫度效應的寄生電阻模型，並且利用此寄生電阻模型，針對具輕摻雜汲極結構的元件進行寄生電阻的模擬。而不論是在寄生電阻的模擬或是在元件電流特性的模擬中，都可以在不同的閘極偏壓與不同的環境溫度之下，分別得到與寄生電阻萃取值以及元件電流測量值相當吻合的結果。

Study on Temperature Response of Poly-Si TFT's with LDD Structure

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Abstract

Polycrystalline silicon thin film transistors (Poly-Si TFT's) have been studied extensively for their application on system-on-panel (SOP) technology due to the high mobility. For actual applications, lightly-doped drain (LDD) structure is usually applied to Poly-Si TFT's. In this thesis, we will study on the effect of field effect mobility and parasitic resistance caused by LDD structure in Poly-Si TFT's, especially on the temperature response of field effect mobility and parasitic resistance.

First, the mobility modeling of the Poly-Si TFT without LDD structure is performed by using the proposed mobility model. The proposed mobility model has taken thermionic emission effect and phonon scattering effect into account to explain the temperature response of field effect mobility. Excellent agreement between experimental and modeling results over the wide range of gate voltage and temperature is both obtained in the field effect mobility modeling and the transfer characteristics modeling by using the proposed mobility model for the Poly-Si TFT without LDD structure.

Next, the parasitic resistance effect due to LDD structure is discussed. The parasitic resistance caused by LDD structure is calculated by subtracting the device resistance of the Poly-Si TFT without LDD structure from the device resistance of the Poly-Si TFT's with

LDD structure. According to the extracted parasitic resistance data, it is found that the parasitic resistance is modulated by gate bias and the modulation is more serious for the Poly-Si TFT's with shorter LDD lengths.

After that, the device simulation results which are performed by Silvaco TCAD for the device with LDD structure show that parasitic transistor effect exists alongside the gate electrode. The parasitic transistor is also dominated by thermionic emission effect in temperature response. Besides, the resistance is treated as a pure resistor with a constant resistance at some temperature for the LDD region without gate bias modulation, and the mechanism of the temperature response in this series resistance region is preferred to conceive as impurity scattering effect.

Finally, the proposed parasitic resistance model is established basing on the analysis and the assumptions mentioned above. Good agreement between experimental and modeling results over the wide range of gate voltage and temperature is both obtained in the parasitic resistance modeling and the transfer characteristics modeling by using the proposed parasitic resistance model for the Poly-Si TFT's with LDD structure.

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光明 2007 初秋 于新竹交通大學

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Chapter 1

Introduction

1.1 An Overview of the Poly-Si TFT Technology

Polycrystalline silicon thin film transistors (Poly-Si TFT's) have attracted more attention because of their wide applications on active matrix liquid crystal displays (AMLCD's) [1-3], memory devices such as dynamic random access memories (DRAM's) [4] and static random access memories (SRAM's) [5], electrical programming read only memories (EPROM's) [6] and electrical erasable programming read only memories (EEPROM's) [7].

Unlike amorphous silicon (a-Si) TFT's, Poly-Si TFT's have much larger carrier mobility which usually exceeds 100 cm^2 / *V-sec* by present mature technology. The superior carrier mobility is essential to successfully integrate Poly-Si TFT's and peripheral driving circuits [5] on the same panel to reduce the assembly complexity and cost. Therefore, the low temperature process of Poly-Si TFT's with high mobility makes it possible to realize the ultimate goal, system on panel (SOP) [8]. Furthermore, due to the higher mobility, the device dimension of Poly-Si TFT's can be made smaller than that of a-Si TFT's to get higher aperture ratio in each pixel and achieve high density and high resolution AMLCD's.

However, there are still some problems existed in Poly-Si TFT's. Comparing to single crystalline silicon (c-Si), Poly-Si has a lot of defects at grain boundaries. These defects, regarded as trap states, are located in the disordered grain boundary regions and degrade device performance severely. In other words, the performance of Poly-Si TFT's is strongly affected by the grain structure inside the channel region. Thus, the larger grain with less grain boundary defects is desirable and currently many researches attempting to achieve this goal have been studied, such as solid phase crystallization (SPC) [9], metal induced lateral crystallization (MILC) [10] and laser crystallization [11]. Because the recrystallization

process will influence the quality of Poly-Si film, it will influence the device performance of Poly-Si TFT's spontaneously. Thus, the device models should have the ability to be effectively applied to Poly-Si TFT's fabricated from Poly-Si films of different film qualities. For example, the proposed mobility model which will be presented later in this thesis can be applied to Poly-Si TFT's with different grain sizes by adjusting the model parameters, and the interactive influence between thermionic emission effect and phonon scattering effect is performed to express the temperature response.

1.2 Mobility Models for Poly-Si TFT's

For Poly-Si TFT's, unlike c-Si transistors, not all charges induced by gate voltage can become free carriers to contribute to drain current. Instead, one significant part of the gate-bias-induced charges will be captured by the trap states associated with grain boundaries. Therefore, field effect mobility will increase gradually with gate voltage because the ratio of free carrier density to induced charge density increases. This is so-called pseudo-subthreshold region which is caused by the decrease of energy barrier height at grain boundaries in Poly-Si TFT's. M. Jacunski *et al.* had proposed an appropriate mobility model to take this effect into account empirically and the equation was expressed as: [12]

$$\frac{1}{\mu_{FET}} = \frac{1}{\mu_0} + \frac{1}{\mu_1 \left| \frac{2(V_{GS} - V_t)}{\eta_i V_{th}} \right|^m} \tag{1-1}$$

where m, μ_0 and μ_1 are extractable mobility parameters. But it is a pity that this model is not valid under various temperatures because the temperature effects such as phonon scattering effect at high gate biases are not under consideration. Thus, the above formula fails to precisely describe the behaviors of carrier mobility in Poly-Si TFT's.

To improve this problem, an empirical assumption with power law is applied to describe phonon scattering effect and to modify this mobility model, and the modified model equation

can be written as:

$$\frac{1}{\mu_{FET}} = \frac{1}{\mu_0 \left(\frac{T}{T_0}\right)^{-\beta}} + \frac{1}{\mu_1 \left|\frac{2(V_{GS} - V_t)}{\eta_i V_{th}}\right|^m} \tag{1-2}$$

where β stands for the temperature dependence due to phonon scattering effect.

Besides, Apostolos T. Voutsas proposed another mobility model which was given as: [13]

$$\frac{1}{\mu_{app}} = \frac{1}{\mu_{SIMOX}} + \frac{1}{\mu_{Defect}} + \frac{1}{\mu_{GB}} \tag{1-3}$$

where μ_{app} is the measured mobility, μ_{SIMOX} is the equivalent SIMOX mobility accounting for phonon scattering effect, μ_{Defect} is the mobility term attributed to intra-grain-defect scattering and μ_{GB} is the mobility term attributed to grain-boundary scattering, i.e. thermionic emission effect. However, this model is complicated to use because the fitting parameters are too many, or in other words, the parameter extraction procedure is too inextricable.

In fact, we have proposed the mobility model basing on physical theories, and the proposed model is verified in different devices including N-type devices and P-type devices. The details and verification results of the proposed mobility model are described particularly in Appendix.

1.3 Motivation

The proposed mobility model (as shown in Appendix) is used to describe the electrical properties in device channel region. But for actual applications, lightly-doped drain (LDD) structure is usually applied to devices with total LDD length approaching 2μm or above. Therefore, LDD structure will influence the device performance more seriously with shorter channel length. The effect of LDD structure will be investigated in this thesis in detail, especially the temperature response of LDD structure.

LDD structure is usually used to suppress leakage currents and Kink effect in Poly-Si

TFT's because LDD structure can effectively lower down drain electric field. The LDD region will produce an extra parasitic resistance and that will influence the performance of Poly-Si TFT's considerably, but the modeling of parasitic resistance effect is not well-established so far.

When long channel devices are checked, parasitic resistance effect seems not so important because channel resistance is much larger and the difference caused by parasitic resistance can be eliminated by a global fitting in field effect mobility models. But for short channel devices, parasitic resistance effect becomes significant and the modeling of field effect mobility can not be achieved very well only by existing mobility models. The modeling of parasitic resistance effect due to LDD region should be taken into account in Poly-Si TFT device models and then the accurate modeling results of device electrical characteristics can be obtained. Therefore, the modeling of parasitic resistance effect is important to precisely predict the device performance of Poly-Si TFT's with LDD structure, especially for the tendency toward short channel devices.

1.4 Thesis Outline

In Chapter 1, the various kinds of applications, the advantages and the disadvantages of Poly-Si TFT's are introduced in a brief overview of the Poly-Si TFT technology. Then, several mobility models for Poly-Si TFT's are discussed, and these models mainly emphasize on the effect of energy barrier height caused by grain boundary defects in Poly-Si TFT's. Finally, the motivation of this work to study the parasitic resistance modeling of Poly-Si TFT's with LDD structure is expressed.

In Chapter 2, the fabrication process and the measurement experimental conditions of the Poly-Si TFT's used in this work are firstly described in brief. Following that, the proposed mobility model is presented and the physical basis of the proposed mobility model is also interpreted. The mobility extraction method from the measured data used in this work is

introduced and the extracted field effect mobility of the Ploy-Si TFT without LDD structure is then modeled over the wide range of gate voltage and temperature by the proposed mobility model. Besides, the measured transfer characteristics of the Poly-Si TFT without LDD structure are also simulated over the wide range of gate voltage and temperature basing on the field effect mobility fitting results of the proposed mobility model.

In Chapter 3, the parasitic resistance extraction method used in this work is introduced to extract the values of the parasitic resistance under different gate biases and several temperatures for the Poly-Si TFT's with various LDD lengths. The dependence between the extracted parasitic resistance and the gate voltage is checked to discuss the possible mechanism. Next, the device simulation results including the current density distribution results and the vertical electric field distribution results performed by Silvaco TCAD are presented. Afterwards, the parasitic resistance model basing on the experimental results and the simulation results is proposed. The extracted parasitic resistance of the Poly-Si TFT's with various LDD lengths is then modeled over the wide range of gate voltage and temperature by the proposed parasitic resistance model. Finally, the measured transfer characteristics of the Poly-Si TFT's with various LDD lengths are also simulated over the wide range of gate voltage and temperature basing on the field effect mobility fitting results of the proposed mobility model from the Poly-Si TFT without LDD structure and the parasitic resistance fitting results of the proposed parasitic resistance model from the Poly-Si TFT's with various LDD lengths.

In Chapter 4, the conclusions of the works done in this thesis are given.

In Appendix, the proposed mobility model is derived in detail and the physical basis is also interpreted particularly. In addition, the proposed model is verified in different devices including N-type devices and P-type devices and the analysis of the verification results are given.

Chapter 2

Modeling of the Poly-Si TFT's without LDD Structure

2.1 Device Fabrication Process and Measurement Conditions

The typical top-gate, coplanar self-aligned Poly-Si TFT's which were fabricated on the glass substrates and crystallized by excimer laser annealing (ELA) recrystallization technology are used in this study. The Poly-Si TFT's with and without LDD structure were also fabricated, respectively. The schematic cross-sectional view of the devices with LDD structure is shown in Fig.2-1, and that of the devices without LDD structure is shown in Fig.2-2. The device fabrication process is described below.

First, the oxide buffer layer was deposited on the glass substrate to prevent the diffusion of the impurities existing in the glass substrate from the silicon layer. Then, the undoped 50-*nm*-thick a-Si layer was deposited on the buffer layer. After that, the a-Si films were recrystallized by ELA method with 420 mJ / cm^2 laser energy, and the recrystallized Poly-Si films were patterned into the active islands. Afterward, the gate insulator layer was deposited. Here the gate insulator layer was combined with the 50-*nm*-thick oxide layer and the 20-*nm*-thick nitride layer. Next, phosphorus ions were implanted to form the n^+ source/drain regions and the n^- LDD regions. These dopants were activated by thermal process. Finally, metal layer was deposited and then patterned for the source/drain and gate regions as the metal pads.

The electrical characteristics of the 6μm channel width and 6μm channel length N-type Poly-Si TFT without LDD structure were measured under various temperatures which varies form 233K to 373K to check the accuracy of the proposed mobility model, and those of the 6μm channel width and 6μm channel length N-type Poly-Si TFT's with different LDD lengths which varies from 0.5μm to 3.5μm were also measured over the wide temperature range to

check the influence of the LDD structure. Therefore, the further study of the parasitic resistance effect can be achieved basing on these measured data.

2.2 Modeling of Field Effect Mobility

2.2.1 The Proposed Mobility Model for Poly-Si TFT's

In Poly-Si TFT's, the gate-bias-induced charges will be captured by the trap states associated with the grain boundaries. At small gate biases, the energy barrier height at grain boundaries is still large and influences field effect mobility very seriously. Free carriers transport through grain boundaries by thermionic emission to overcome the energy barrier height at small gate biases. Therefore, field effect mobility will increase as temperature increases.

On the contrary, at large gate biases, the energy barrier height at grain boundaries is almost suppressed by gate-bias-induced charges. Thus, the dominated mechanism of field effect mobility is changed to phonon scattering and mobility will decrease with increasing temperature. Both thermionic emission effect and phonon scattering effect were considered in the proposed mobility model and the equation is given as: [14]

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{TE}} + \frac{1}{\mu_{PS}} = \frac{1}{\frac{L_G}{L_{GB}} \cdot \mu_G \cdot \exp\left(\frac{-E_A}{kT}\right)} + \frac{1}{\mu_{T0} \cdot \left(\frac{T}{T_0}\right)^{-\beta}} \tag{2-1}$$

where

L_G is the grain size of the Poly-Si film;

L_{GB} is the grain boundary size of the Poly-Si film;

μ_G is the carrier mobility at the intra-grain regions;

E_A is the activation energy, or the energy barrier height at grain boundaries;

k is Boltzmann constant;

μ_{T0} is the constant mobility at high gate biases at 298K;

T is the environment temperature with the unit of Kelvin;

T_0 is the reference temperature which defined as the room temperature, 298K;

β is the temperature dependence coefficient to describe phonon scattering effect.

Besides, oxide-silicon interface scattering effect also has to be considered. A common empirical form to describe interface scattering effect is used in the proposed mobility model. Then, the final field effect mobility can be given as:

$$\mu_{FET} = \frac{\mu_{eff}}{1 + \theta \cdot (V_{GS} - V_T)} \tag{2-2}$$

where θ is the gate bias dependence coefficient to describe oxide-silicon interface scattering effect and V_T is the threshold voltage of device.

2.2.2 Mobility Extraction Method

The field effect mobility of the Poly-Si TFT without LDD structure is extracted from the measured data according to the general drain current equation in linear region as shown below:

$$I_{DS} = \frac{W}{L} \cdot \mu \cdot C_{OX} \cdot \left(V_{GS} - V_T - \frac{1}{2} V_{DS} \right) \cdot V_{DS} \tag{2-3}$$

The drain current versus gate voltage (i.e. I_{DS}-V_{GS}, the transfer characteristic) data were all measured at drain voltage V_{DS}=0.1V under different environment temperatures, then the mobility can be calculated individually to get the complete mobility versus gate voltage results (μ-V_{GS}) at V_{DS}=0.1V for each environment temperature. The calculation method is described as:

$$\mu = \frac{I_{DS}}{\frac{W}{L} \cdot C_{OX} \cdot \left(V_{GS} - V_T - \frac{1}{2} V_{DS} \right) \cdot V_{DS}} \tag{2-4}$$

where the threshold voltage V_T is extracted by constant current method and the normalized

threshold current is set as $W / L \times 10^{-9}$ A.

2.2.3 Mobility Modeling Results

The measured transfer characteristic data of the 6μm channel width and 6μm channel length N-type Poly-Si TFT without LDD structure at drain bias V_{DS}=0.1V over the temperature range from 233K to 373K are used to extract the field effect mobility values. After that, the proposed mobility model is then applied to model the extracted field effect mobility.

First, the average grain size (i.e. L_G) value of the Poly-Si film has to be determined. Hence, the sample of the Poly-Si film after ELA recrystallization process with 420 mJ / cm^2 laser energy was analyzed by the scanning electron microscopy (SEM). The top view SEM image of the Poly-Si film is shown in Fig.2-3 and the value of the average grain size is taken as 0.8μm.

In addition, the activation energy (i.e. E_A) is also extracted at each gate voltage from the measured transfer characteristic data. The activation energy is extracted from the slope of the Ln(I_{DS}) (the natural logarithm of the drain current) versus 1/kT (the reciprocal of the thermal energy) curve at each gate voltage, and the curves for several gate voltages are shown in Fig.2-4. In fact, the value of the activation energy is equal to the negative number of the slope and then the activation energy is extracted. The activation energy of the Poly-Si TFT without LDD structure is shown in Fig.2-5.

After the global fitting step according to the proposed mobility model, the comparison between the extracted field effect mobility and the modeling field effect mobility for the Poly-Si TFT without LDD structure is shown in Fig.2-6 and excellent agreement over the wide range of gate voltage and temperature is obtained. The values of the all model parameters of the proposed mobility model for the Poly-Si TFT without LDD structure are summarized in Table I.

2.3 Modeling of Transfer Characteristics

Furthermore, the transfer characteristics are simulated from Eq.(2-3) by adopting the mobility fitting results of the proposed mobility model. The comparison of the measured transfer characteristics and the modeling transfer characteristics for the Poly-Si TFT without LDD structure is shown in Fig.2-7. Good agreement over the wide range of gate voltage and temperature between the raw measured transfer characteristic data and the modeling transfer characteristic results is achieved spontaneously.

Chapter 3

Modeling of the Poly-Si TFT's with LDD Structure

3.1 The Parasitic Resistance Effect of LDD Structure

3.1.1 Parasitic Resistance under Various LDD Lengths

According to the measured transfer characteristic data from the Poly-Si TFT without LDD structure, the device resistance is calculated at each gate voltage and the relation between the device resistance and the gate voltage is obtained. These device resistance values are taken as the reference values of the channel resistance. Because the Poly-Si TFT's with and without LDD structure were all fabricated in the same run, the channel resistance of these devices is regarded as identity. Therefore, the additional resistance caused by LDD structure can be obtained by subtracting the reference channel resistance from the device resistance calculated from the Poly-Si TFT's with LDD structure at each gate voltage, and this additional resistance can be regarded as the parasitic resistance.

The parasitic resistance caused by LDD structure is calculated for the 6μm channel width and 6μm channel length Poly-Si TFT with 0.5μm, 1μm, 1.5μm, 2μm, 3μm and 3.5μm LDD length. The relation between the parasitic resistance and the gate voltage is checked for various LDD lengths over the whole gate bias range, and the phenomenon of the decreasing parasitic resistance with increasing gate voltage is observed in the all Poly-Si TFT's with LDD structure. Thus, the decided dependence between the parasitic resistance caused by LDD structure and the gate voltage is now confirmed.

In order to further study the influence of the gate bias on the parasitic resistance of the Poly-Si TFT's with different LDD lengths, a percentage analyzing method is used under well-above threshold region. The parasitic resistance value at V_{GS}=3V is taken as the reference resistance and the ratio of the parasitic resistance to the reference resistance is

calculated at each gate voltage from V_{GS}=3V to V_{GS}=15V for the all Poly-Si TFT's with LDD structure. The decreasing percentage comparison between the Poly-Si TFT's with different LDD lengths is shown in Fig.3-1. It is obvious that the percentage decreases more rapidly for the Poly-Si TFT's with shorter LDD lengths.

Besides, the comparison between the parasitic resistance and the LDD length under several well-above threshold gate biases is also checked in Fig.3-2. The linear relation is observed in the long LDD length region. The parasitic resistance of the short LDD length region, such as 0.5μm and 1μm, seems larger than the resistance value predicted from the linear relation observed in the long LDD length region. It is clear that gate voltage plays an important role in parasitic resistance from the above, especially for short LDD region. Hence, the influence of the gate voltage can be deduced that the gate bias may only control a limited region around the gate electrode.

3.1.2 Device Simulation Results

The device simulation tool, Silvaco TCAD including the process simulator ATHENA and the device simulator ATLAS, is applied to perform the device simulation and to further study the influence of the gate voltage and the LDD length on the parasitic resistance. The device structure used in this device simulation work is shown in Fig.3-3.

The current density distribution of the device with and without LDD structure is firstly simulated and compared in Fig.3-4 and Fig.3-5. It is very obvious that the current density distribution shows a very different performance around the gate electrode between the two structures. The current path seems to extend from the channel region into the LDD region in the device with LDD structure. In other words, this current extending effect seems to cause the extended channel length, ΔL. On the contrary, the current path of the device without LDD structure is regular, the current extending effect does not occur.

In addition, the vertical electric field distribution of the two device structures is also

simulated, and the simulation results are shown in Fig.3-6. Both the device structures show the respectable vertical electric field distribution alongside the gate electrode. This electric field may be the reason that the current path of the device with LDD structure extends into the LDD region. Because of the existence of the vertical electric field around the gate electrode, the current path is induced and bounded unceasingly even the carriers have flowed out the gate-electrode-directly-controlled region, i.e. the channel region. But for the device without LDD structure, the current extending situation is not noticeable. That may be due to that the extended vertical electric field distributes just above the highly-doped source/drain region and the current extending effect is concealed.

According to the simulation results for the device with LDD structure given above, it seems that there is a parasitic transistor with the channel length which is equal to the extended channel length, ΔL. The channel resistance and the resistance caused by the parasitic transistor can be combined in series.

Finally, the dependence between the extended channel length and the gate voltage is checked by simulating the current density distribution for the device with LDD structure at different gate voltages. The same simulation work is also done for the device without LDD structure. The simulation results are shown in Fig.3-7. From the simulation result of the device with LDD structure, the extended channel length ΔL increases with increasing gate bias, but the variation is not very huge. The variation of the ΔL values is less than 0.2μm from low gate bias (V_{GS}=3V) to high gate bias (V_{GS}=15V). Besides, the extended channel length is not notable for the device without LDD structure at every gate bias.

3.2 Modeling of Parasitic Resistance

3.2.1 The Parasitic Resistance Model for Poly-Si TFT's with LDD Structure

From the parasitic transistor assumption, the first part of the proposed parasitic resistance model can be set up. Similar to a simple Poly-Si TFT structure, the equation includes the

activation energy term to describe the temperature response due to thermionic emission effect. In addition, it is expectable that the power dependence on gate voltage will be less than unity because the gate bias does not control the extended channel region directly. Thus, the parasitic resistance model equation basing on the parasitic transistor effect can be written as:

$$R_{PT} = \frac{\Delta L}{W \cdot K_N \cdot (V_{GS} - V_{TN})^{\alpha}} \tag{3-1}$$

$$K_N = K_{N0} \cdot \exp\left(-\frac{E_{AN}}{kT}\right) \tag{3-2}$$

$$K_{N0} = C_{eff} \cdot \mu_N \tag{3-3}$$

where

ΔL is the channel length of the parasitic transistor, i.e. the extended channel length;

W is the channel width of the parasitic transistor, the same as the width of the device;

V_{TN} is the effective threshold voltage of the parasitic transistor;

α is the gate voltage dependence coefficient;

E_{AN} is the activation energy of the parasitic transistor;

k is Boltzmann constant;

T is the environment temperature with the unit of Kelvin;

K_{N0} is a fitting parameter and means the product of C_{eff} and μ_N. The C_{eff} term is the effective gate insulator capacitance of the parasitic transistor, and μ_N is the carrier mobility at the intra-grain region of the parasitic transistor.

Following the parasitic transistor, the resistance caused by the remaining LDD region in the device with larger LDD length is considered. Without modulating by gate voltage, this region can be treated as a pure resistor with a constant resistance at some temperature. In order to study the temperature response of the Poly-Si TFT's with LDD structure particularly, the temperature response of this series resistance has to be checked. Due to the higher doping

concentration in LDD region than in channel region, plenty of the ionized space charges exist in LDD region. Therefore, the mechanism of the temperature response in the series resistance region is preferred to be considered as impurity scattering effect. Then the parasitic resistance model equation basing on the series resistance can be written as:

$$R_{SR} = R_{T0} \cdot \left(\frac{T}{T_0} \right)^{-\gamma} \tag{3-4}$$

where

R_{T0} is the constant resistance of the series resistor at 298K;

T is the environment temperature with the unit of Kelvin;

T_0 is the reference temperature which defined as the room temperature, 298K;

γ is the temperature dependence coefficient to describe impurity scattering effect.

After giving the proposed parasitic resistance model equations basing on parasitic transistor effect and impurity scattering effect, the completed parasitic resistance model can be finally written as:

$$R_P = R_{PT} + R_{SR} = \frac{\Delta L}{W \cdot K_{N0} \cdot \exp\left(-\frac{E_{AN}}{kT} \right) \cdot (V_{GS} - V_{TN})^{\alpha}} + R_{T0} \cdot \left(\frac{T}{T_0} \right)^{-\gamma} \tag{3-5}$$

3.2.2 Parasitic Resistance Modeling Results

The measured transfer characteristic data of the 6μm channel width and 6μm channel length N-type Poly-Si TFT's with LDD structure at V_{DS}=0.1V over the temperature range from 233K to 373K are used to calculate parasitic resistance values. The proposed parasitic resistance model is then applied to model the extracted parasitic resistance.

First, the value of the extended channel length ΔL (i.e. the channel length of the parasitic transistor) is checked. From the simulation results and the experimental data analysis such as Fig.3-2, ΔL is estimated at about 0.6μm to 0.7μm. In order to simplify the parameter

extraction procedure, the value of ΔL is chosen as the constant value, 0.65μm. But for the Poly-Si TFT with 0.5μm LDD length, the value of ΔL will be set as 0.5μm, that is, it is considered as that the parasitic resistance of the Poly-Si TFT with 0.5μm LDD length is only contributed by the parasitic transistor effect. Besides, it is hard to extract the effective threshold voltage of the parasitic transistor (i.e. V_{TN}), so this parameter is treated as a fitting parameter for the time being.

The activation energy of the parasitic transistor (i.e. E_{AN}) is also extracted at each gate voltage from the extracted parasitic resistance of the Poly-Si TFT with 0.5μm LDD length. The activation energy is extracted from the slope of the $Ln(R_P)$ (the natural logarithm of the parasitic resistance) versus 1/kT (the reciprocal of the thermal energy) curve at each gate voltage, and the curves for several gate voltages are shown in Fig.3-8. Then, the extracted activation energy of the parasitic transistor is shown in Fig.3-9. In addition, the activation energy of the parasitic transistor is shown and compared with the activation energy of the Poly-Si TFT without LDD structure in Fig.3-10. From the figure, it can be found that the dependence between the gate voltage and the activation energy of the parasitic transistor is a little slighter than the dependence between the gate voltage and the activation energy of the Poly-Si TFT without LDD structure because the gate bias does not modulate the parasitic transistor directly.

Moreover, the value of the temperature dependence coefficient to describe impurity scattering effect γ is also checked. The γ coefficient can be extracted from the slope of the $Ln(R_P)$ (the natural logarithm of the parasitic resistance) versus Ln(T) (the natural logarithm of the temperature) curve under larger gate voltages to avoid the parasitic transistor effect. The extraction curves at several gate voltages for the Poly-Si TFT's with 3.5μm LDD length are shown in Fig.3-11. The value of γ does not vary seriously for different gate voltages, so it can regarded as a constant for some device.

After the global fitting step according to the proposed parasitic resistance model, the

parasitic resistance modeling results of the Poly-Si TFT's with LDD structure are obtained. In order to get the clearer comparison results, both the extracted resistance and the modeling resistance are taken for the reciprocal to get the value of the conductance. The comparison between the extracted conductance values and the modeling conductance values is depicted in Fig.3-12 to Fig.3-17, respectively. From these figures, excellent agreement over the wide range of gate voltage and temperature between the extracted parasitic resistance and the modeling parasitic resistance is obtained. The all model parameter values of the proposed parasitic resistance model for the Poly-Si TFT's with various LDD lengths are summarized in Table II to Table VII.

3.3 Modeling of Transfer Characteristics

Once again, the transfer characteristics are re-simulated by adopting the field effect mobility modeling results of the proposed mobility model for the Poly-Si TFT without LDD structure and the parasitic resistance modeling results of the proposed parasitic resistance model for the Poly-Si TFT's with LDD structure. The calculation method to get the simulated drain current of the device with LDD structure is shown as:

$$I_{DS} = \frac{V_{DS}}{\frac{L}{W \cdot \mu_{FET} \cdot C_{OX} \cdot \left(V_{GS} - V_T - \frac{1}{2} V_{DS} \right)} + R_P} \tag{3-6}$$

where μ_{FET} is the mobility modeling results for the device without LDD structure and R_P is the parasitic resistance modeling results for the device with LDD structure.

The transfer characteristics simulation results for the Poly-Si TFT's with LDD structure are shown in Fig.3-18 to Fig.3-23, respectively. Good agreement over the wide range of gate voltage and temperature between the raw measured transfer characteristic data and the modeling transfer characteristic results is also achieved.

Chapter 4

Conclusion

In this thesis, the Poly-Si TFT's were fabricated by excimer laser annealing (ELA) recrystallization technology and the measurement work was done for the Poly-Si TFT's of the same channel width and channel length with different LDD lengths at small drain bias under various environment temperatures.

For the Poly-Si TFT without LDD structure, the field effect mobility is extracted from the measured transfer characteristics and modeled by the proposed mobility model. The proposed mobility model has taken thermionic emission effect and phonon scattering effect into account, so it can provide reliable predictions for mobility variation under various temperatures. Good agreement over the wide range of gate voltage and temperature between the extracted mobility and the modeling mobility for the Poly-Si TFT without LDD structure is obtained. In addition, the transfer characteristics are also modeled by adopting the mobility modeling results of the proposed mobility model and good agreement over the wide range of gate voltage and temperature between the measured transfer characteristics and the modeling transfer characteristics for the Poly-Si TFT without LDD structure is also obtained.

Next, the parasitic resistance effect due to LDD structure is discussed. The parasitic resistance caused by LDD structure is calculated by subtracting the device resistance of the Poly-Si TFT without LDD structure from the device resistance of the Poly-Si TFT's with LDD structure. According to the extracted parasitic resistance data, it is found that the parasitic resistance is modulated by gate bias and the modulation is more serious for the Poly-Si TFT's with shorter LDD lengths.

After that, the device simulation results which are performed by Silvaco TCAD for the device with LDD structure show that parasitic transistor effect exists alongside the gate

electrode. The current path extends from the channel region into the LDD region due to the extended vertical electric field from the side of the gate electrode and then causing the extended channel length. The extended channel length is regarded as the channel length of the parasitic transistor and the parasitic transistor is also dominated by thermionic emission effect in temperature response. Besides, the resistance is treated as a pure resistor with a constant resistance at some temperature for the LDD region without gate bias modulation. Due to the higher doping concentration in LDD region than in channel region, plenty of the ionized space charges exist in LDD region. Therefore, the mechanism of the temperature response in this series resistance region is preferred to be considered as impurity scattering effect.

Finally, the proposed parasitic resistance model is established basing on the analysis and the assumptions mentioned above. The parasitic resistance modeling of the Poly-Si TFT's with LDD structure is performed by using the proposed parasitic resistance model. Good agreement over the wide range of gate voltage and temperature between the extracted parasitic resistance and the modeling parasitic resistance is obtained. In addition, the transfer characteristics are re-simulated by adopting the mobility modeling results of the proposed mobility model for the Poly-Si TFT without LDD structure and the parasitic resistance modeling results of the proposed parasitic resistance model for the Poly-Si TFT's with LDD structure. Good agreement over the wide range of gate voltage and temperature between the measured and the modeling transfer characteristics is also achieved for the all devices with LDD structure.

Appendix

The Proposed Mobility Model for Poly-Si TFT's

There are two main mechanisms to affect the mobility of Poly-Si TFT's. The first one is thermionic emission effect, and that introduces the effect of the activation energy (E_A) which stands for the energy barrier height (E_B) at grain boundaries. The other one is phonon scattering effect due to lattice thermal vibration. At small gate biases, the grain barrier height is still large and influences the mobility very seriously. The free carriers transport through the grain boundaries by thermionic emission, so the mobility increases as the temperature increases at small gate biases. On the contrary, at large gate biases, the energy barrier height at grain boundaries is almost suppressed by gate-induced charges. Thus, the dominated mechanism of mobility is changed to phonon scattering and mobility will decrease with increasing temperature. In fact, phonon scattering effect is also observed in single crystalline silicon.

As discussed above, the mobility of Poly-Si TFT's is dominated by the grain barrier height at small gate biases, and the main conduction mechanism through the grain boundaries is thermionic emission over the grain-boundary energy barrier height. The equation can be generally written as:

$$\mu_{GB} = \mu_G \cdot \exp\left(\frac{-E_A}{kT}\right) \qquad \text{(A-1)}$$

where

μ_{GB} is the carrier mobility at the grain boundary regions;

μ_G is the carrier mobility at the intra-grain regions;

E_A is the activation energy, or the energy barrier height at grain boundaries;

k is Boltzmann constant.

However, the above formula can be refined to introduce the significance of the grain size and the grain boundary size. A linear relation between the field effect mobility and the grain size was observed. Therefore, the model equation can be improved by including a new term L_G / L_{GB} to describe the effect of the grain size and the grain boundary size on the field effect mobility.

Fig.A-1 is the illustration diagram for the derivation of the mobility model equation. It is assumed that the whole Poly-Si film is composed of the identical grain regions and the identical grain boundary regions in periodical structure. Furthermore, the assumption that each of them has an equivalent resistance and the all grain regions and the all grain boundary regions can be combined by Ohm's Law is also presented. The derivation of the model equation is provided below:

$$R_{ch} = \frac{L}{L_G} R_G + \frac{L}{L_G} R_{GB}$$

$$= \frac{L}{L_G} \frac{L_G}{\mu_G nqt_{ch} W} + \frac{L}{L_G} \frac{L_{GB}}{\mu_{GB} nqt_{ch} W}$$

$$= \frac{L}{Wnqt_{ch}} \left(\frac{1}{\mu_G} + \frac{1}{\frac{L_G}{L_{GB}} \mu_{GB}} \right)$$

$$I_D = \frac{V_{DS}}{R_{ch}} = V_{DS} \frac{W}{L} qnt_{ch} \left(\frac{\mu_G \mu_{GB} \frac{L_G}{L_{GB}}}{\mu_{GB} \frac{L_G}{L_{GB}} + \mu_G} \right) = JWt_{ch} = \sigma \frac{V_{DS}}{L} Wt_{ch}$$

$$J = \frac{V_{DS}}{L} \times qn \left(\frac{\mu_{GB} \frac{L_G}{L_{GB}}}{1 + \frac{\mu_{GB}}{\mu_G} \frac{L_G}{L_{GB}}} \right)$$

If the dominated mechanism of the mobility is regarded as thermionic emission effect, then the Eq.(A-1) can be used in substitution for the term μ_G. Therefore, the effective mobility to describe thermionic emission can be written as:

$$\mu_{TE} = \frac{\mu_{GB}\frac{L_G}{L_{GB}}}{1+\frac{\mu_{GB}}{\mu_G}\frac{L_G}{L_{GB}}} = \frac{\mu_{GB}\frac{L_G}{L_{GB}}}{1+\frac{L_G}{L_{GB}}\exp\left(\frac{-E_A}{kT}\right)} \approx \mu_{GB}\frac{L_G}{L_{GB}} = \frac{L_G}{L_{GB}}\cdot\mu_G\cdot\exp\left(\frac{-E_A}{kT}\right) \quad \text{(A-2)}$$

where

L_G is the grain size of the Poly-Si film;

L_{GB} is the grain boundary size of the Poly-Si film;

μ_G is the carrier mobility at the intra-grain regions;

E_A is the activation energy, or the energy barrier height at grain boundaries;

k is Boltzmann constant;

T is the environment temperature with the unit of Kelvin;

Besides, if the mobility is dominated by phonon scattering effect, the equation is generally given as:

$$\mu_{PS} = \mu_{T0}\cdot\left(\frac{T}{T_0}\right)^{-\beta} \quad \text{(A-3)}$$

where

μ_{T0} is the constant mobility at high gate biases at 298K;

T is the environment temperature with the unit of Kelvin;

T_0 is the reference temperature which defined as the room temperature, 298K;

β is the temperature dependence coefficient to describe phonon scattering effect.

The value of β for single crystalline silicon is 3/2. While approaching to this value more, the crystal quality of the intra-grain region in Poly-Si film is closer to single crystalline silicon. After deriving the mobility equations for thermionic emission effect and phonon scattering effect, the completed mobility model can be finally written as:

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{TE}} + \frac{1}{\mu_{PS}} = \frac{1}{\frac{L_G}{L_{GB}}\cdot\mu_G\cdot\exp\left(\frac{-E_A}{kT}\right)} + \frac{1}{\mu_{T0}\cdot\left(\frac{T}{T_0}\right)^{-\beta}} \quad \text{(A-4)}$$

Besides, oxide-silicon interface scattering effect also has to be considered. A common empirical form to describe interface scattering effect is used in the proposed mobility model. Then, the final field effect mobility can be given as:

$$\mu_{FET} = \frac{\mu_{eff}}{1 + \theta \cdot (V_{GS} - V_T)} \tag{A-5}$$

where θ is the gate bias dependence coefficient to describe oxide-silicon interface scattering effect and V_T is the threshold voltage of device.

Afterward, the extracted mobility values of the N-type and P-type long channel devices are modeled by the proposed mobility model, respectively. Although the devices used in this section were recrystallized by ELA method with 420 mJ / cm^2 laser energy, the same as the devices used in chapter 2 and chapter 3, but they were fabricated in different runs, so the device performance of these devices is very different.

First, the 6μm channel width and 30μm channel N-type Poly-Si TFT with 0.5μm LDD length and the 6μm channel width and 30μm channel P-type Poly-Si TFT without LDD structure are checked, respectively. The mobility modeling results for both is shown in Fig.A-2 and Fig.A-3, and good agreement is obtained. It is obvious that the field effect mobility of the P-type Poly-Si TFT is dominated by phonon scattering effect more strongly than the N-type Poly-Si TFT. The model parameters of the proposed mobility model for the N-type TFT and the P-type TFT are summarized in Table VIII and Table IX, respectively.

The temperature dependence of the model parameters V_T and μ_G / L_{GB} is also checked. The relation between the threshold voltage V_T and the temperature and the relation between the parameter μ_G / L_{GB} and the temperature for the N-type TFT and the P-type TFT are shown in Fig.A-4 and Fig.A-5, respectively. The near-linear relation is observed for the both parameters in the N-type TFT and the P-type TFT. Thus, the linear equation can be both used to describe the temperature dependence of the two parameters, and the inconvenience of the model parameter adjusting is alleviated.

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Table I

The model parameter values of the proposed mobility model

for the $W/L = 6\mu m / 6\mu m$ N-type Poly-Si TFT ***without LDD structure***

Temperature (K)	V_T ***(Volt)***	μ_G / L_{GB}	L_G ***(μm)***	μ_{T0}	β	θ
233	-1.725	400	0.8	152	0.12	0.012
253	-1.866	420				
273	-1.970	440				
298	-2.126	460				
323	-2.231	480				
348	-2.384	500				
373	-2.481	520				

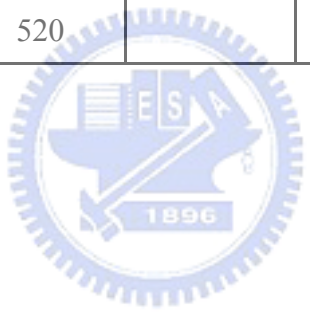


Table II

The model parameter values of the proposed parasitic resistance model for the *W/L = 6μm / 6μm* N-type Poly-Si TFT with ***0.5μm LDD length***

Temperature (K)	V_{TN} ***(Volt)***	K_{N0}	***W (μm)***	***ΔL (μm)***	***α***	R_{T0}	***γ***
233	-3.0	2.12×10^{-5}	6	0.5	0.5	0	0
253	-3.0	2.12×10^{-5}					
273	-3.0	2.12×10^{-5}					
298	-3.0	2.12×10^{-5}					
323	-3.0	2.12×10^{-5}					
348	-3.0	2.12×10^{-5}					
373	-3.0	2.12×10^{-5}					

Table III

The model parameter values of the proposed parasitic resistance model for the *W/L = 6μm / 6μm* N-type Poly-Si TFT with ***1.0μm LDD length***

Temperature (K)	V_{TN} ***(Volt)***	K_{N0}	***W (μm)***	***ΔL (μm)***	***α***	R_{T0}	***γ***
233	-3.0	1.80×10^{-5}	6	0.65	0.5	3850	1.63
253	-3.0	1.80×10^{-5}					
273	-3.0	1.80×10^{-5}					
298	-3.0	1.80×10^{-5}					
323	-3.0	1.80×10^{-5}					
348	-3.0	1.76×10^{-5}					
373	-5.0	1.60×10^{-5}					

Table IV

The model parameter values of the proposed parasitic resistance model for the *W/L = 6μm / 6μm* N-type Poly-Si TFT with ***1.5μm LDD length***

Temperature (K)	V_{TN} *(Volt)*	K_{N0}	*W (μm)*	*ΔL (μm)*	*α*	R_{T0}	*γ*
233	-3.0	1.80×10^{-5}	6	0.65	0.5	9150	1.63
253	-3.0	1.80×10^{-5}					
273	-3.0	1.80×10^{-5}					
298	-3.0	1.80×10^{-5}					
323	-3.0	1.80×10^{-5}					
348	-3.0	1.76×10^{-5}					
373	-5.0	1.60×10^{-5}					

Table V

The model parameter values of the proposed parasitic resistance model for the *W/L = 6μm / 6μm* N-type Poly-Si TFT with ***2.0μm LDD length***

Temperature (K)	V_{TN} *(Volt)*	K_{N0}	*W (μm)*	*ΔL (μm)*	*α*	R_{T0}	*γ*
233	-3.0	1.25×10^{-5}	6	0.65	0.5	14600	1.63
253	-3.0	1.30×10^{-5}					
273	-3.0	1.35×10^{-5}					
298	-3.0	1.35×10^{-5}					
323	-3.0	1.35×10^{-5}					
348	-3.0	1.35×10^{-5}					
373	-5.0	1.20×10^{-5}					

Table VI

The model parameter values of the proposed parasitic resistance model

for the *W/L = 6μm / 6μm* N-type Poly-Si TFT with ***3.0μm LDD length***

Temperature (K)	V_{TN} ***(Volt)***	K_{N0}	***W (μm)***	***ΔL (μm)***	***α***	R_{T0}	***γ***
233	-3.0	9.00×10^{-6}	6	0.65	0.5	27000	1.63
253	-3.0	9.50×10^{-6}					
273	-3.0	1.05×10^{-5}					
298	-3.0	1.05×10^{-5}					
323	-3.0	1.05×10^{-5}					
348	-3.0	1.05×10^{-5}					
373	-3.0	1.00×10^{-5}					

Table VII

The model parameter values of the proposed parasitic resistance model

for the *W/L = 6μm / 6μm* N-type Poly-Si TFT with ***3.5μm LDD length***

Temperature (K)	V_{TN} ***(Volt)***	K_{N0}	***W (μm)***	***ΔL (μm)***	***α***	R_{T0}	***γ***
233	-3.0	1.00×10^{-5}	6	0.65	0.5	36000	1.63
253	-3.0	1.10×10^{-5}					
273	-3.0	1.20×10^{-5}					
298	-3.0	1.30×10^{-5}					
323	-3.0	1.30×10^{-5}					
348	-3.0	1.30×10^{-5}					
373	-3.0	1.30×10^{-5}					

Table VIII

The model parameter values of the proposed parasitic resistance model

for the *W/L = 6μm / 30μm* ***N-type*** Poly-Si TFT with ***0.5μm LDD length***

Temperature (K)	***V_T (Volt)***	***μ_G / L_{GB}***	***L_G (μm)***	***μ_{T0}***	***β***	***θ***
233	0.001	610	0.8	405	1.05	0.025
253	-0.165	660				
273	-0.231	750				
298	-0.418	880				
323	-0.472	950				
348	-0.499	1000				
373	-0.649	1050				

Table IX

The model parameter values of the proposed parasitic resistance model

for the *W/L = 6μm / 30μm* ***P-type*** Poly-Si TFT ***without LDD structure***

Temperature (K)	***V_T (Volt)***	***μ_G / L_{GB}***	***L_G (μm)***	***μ_{T0}***	***β***	***θ***
233	-1.776	122	0.8	210	1.55	0.02
253	-1.757	128				
273	-1.667	135				
298	-1.538	142				
323	-1.506	150				
348	-1.360	152				
373	-1.285	156				

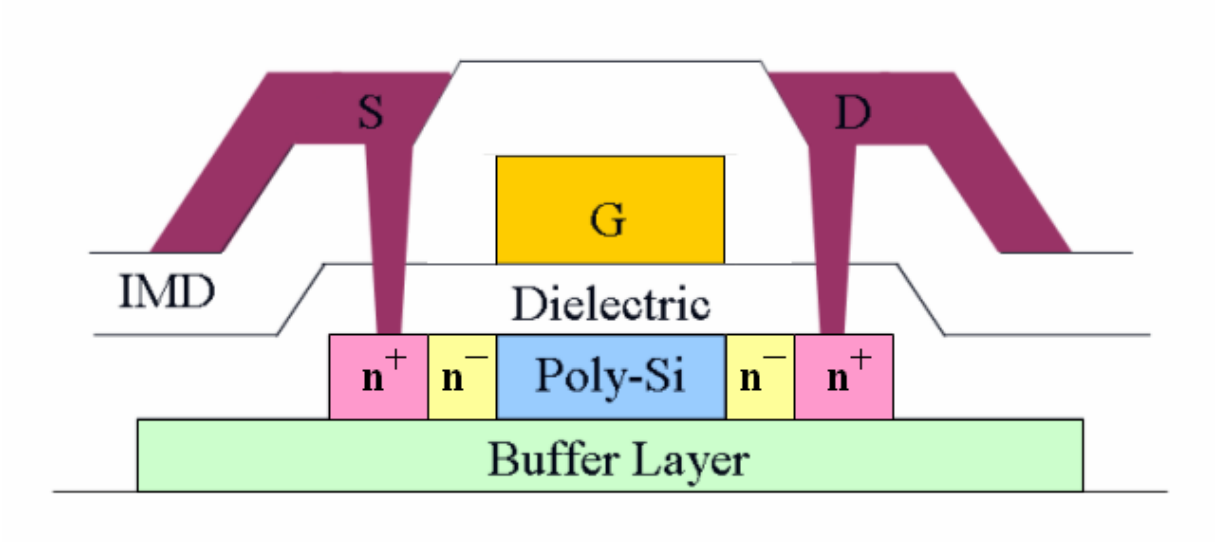


Fig.2-1 The schematic cross-sectional view of the *W/L = 6μm / 6μm* N-type Poly-Si TFT with LDD structure

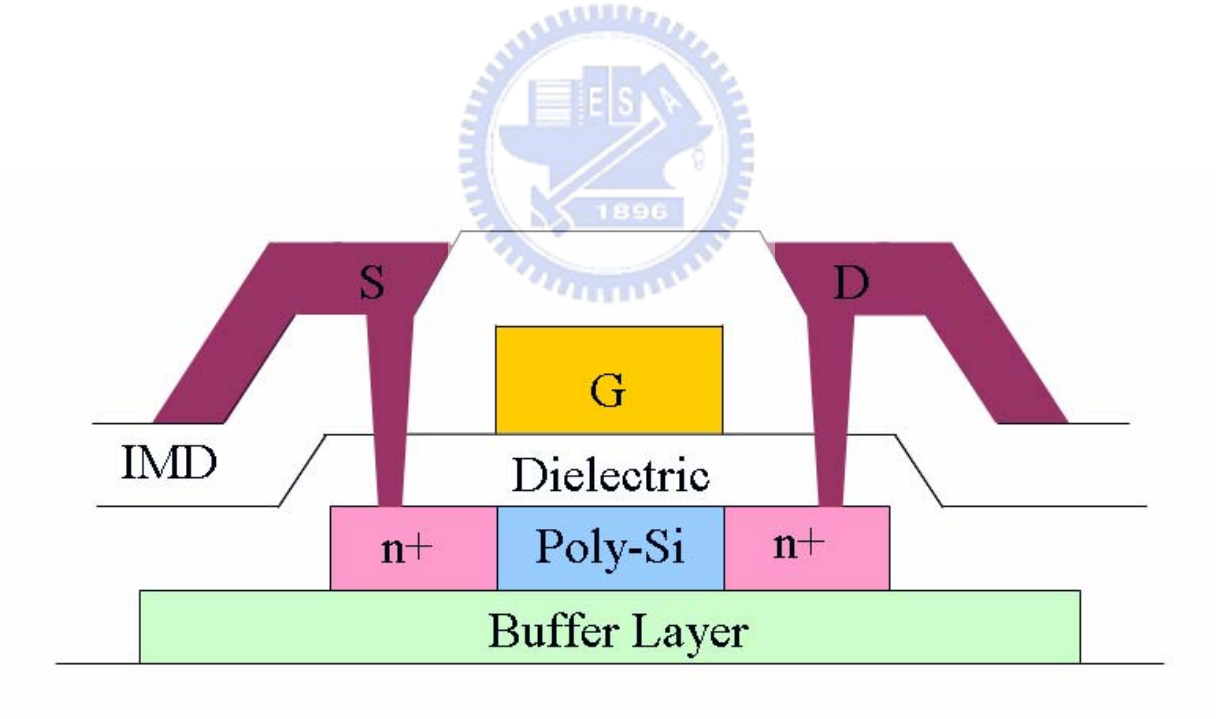


Fig.2-2 The schematic cross-sectional view of the *W/L = 6μm / 6μm* N-type Poly-Si TFT's without LDD structure

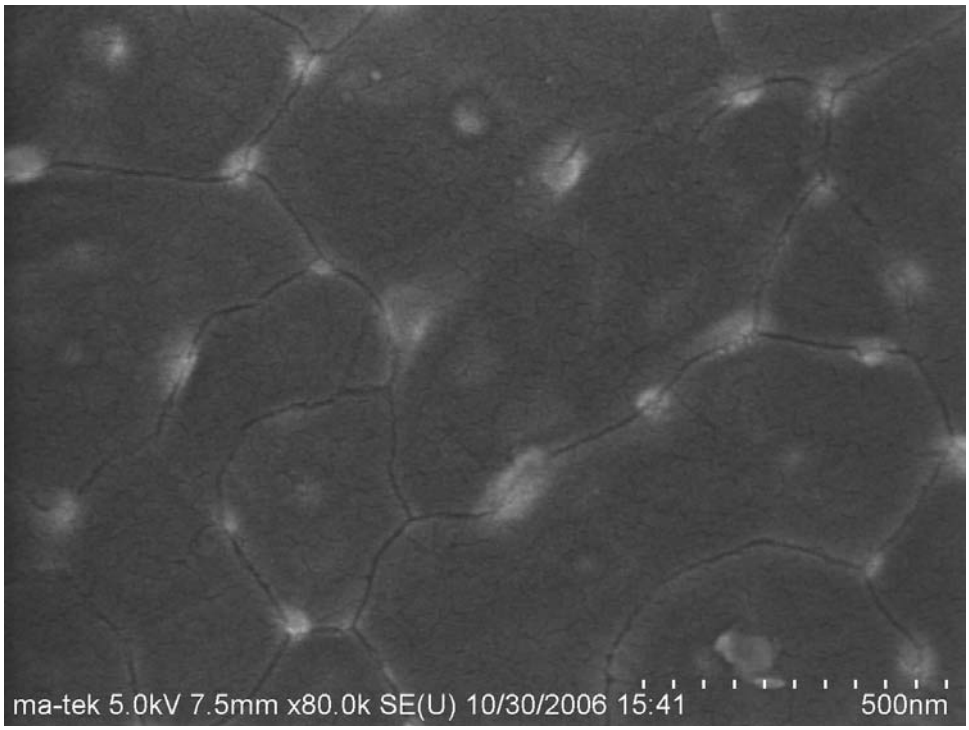


Fig.2-3 The SEM image of the Poly-Si film annealed by ELA method under 420 mJ / cm^2 laser energy

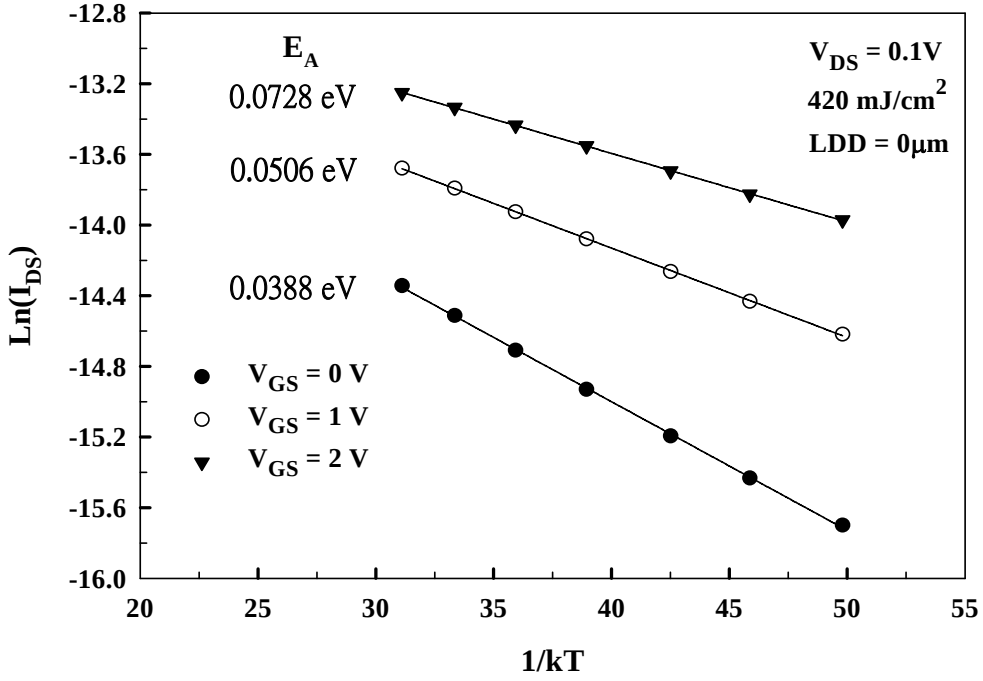


Fig.2-4 The extraction method for the activation energy E_A of the *W/L = 6μm / 6μm* N-type Poly-Si TFT ***without LDD structure*** due to thermionic emission effect

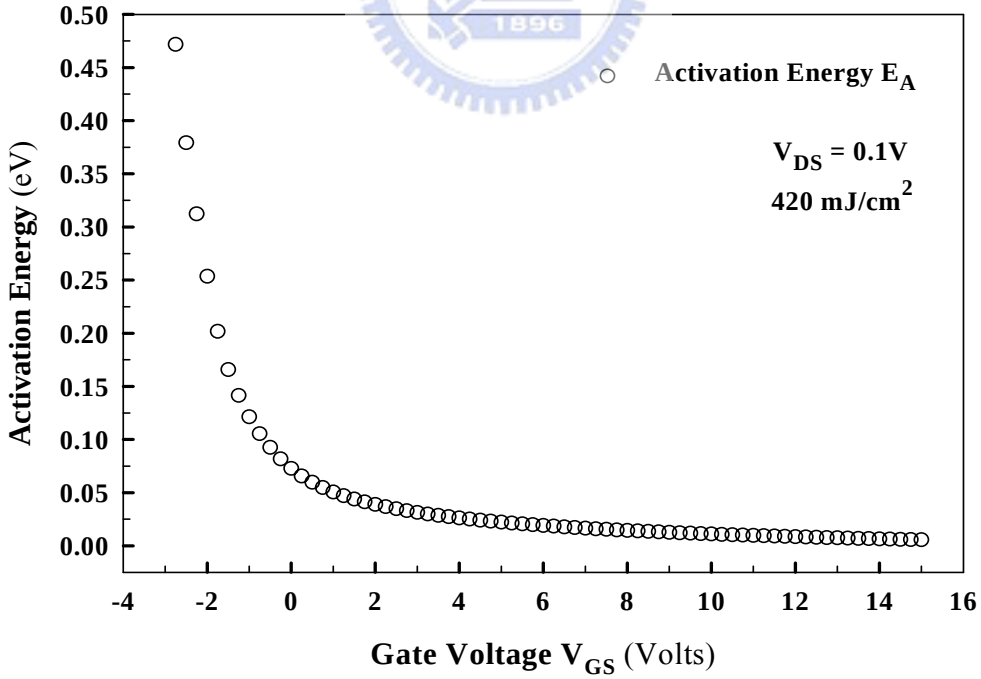
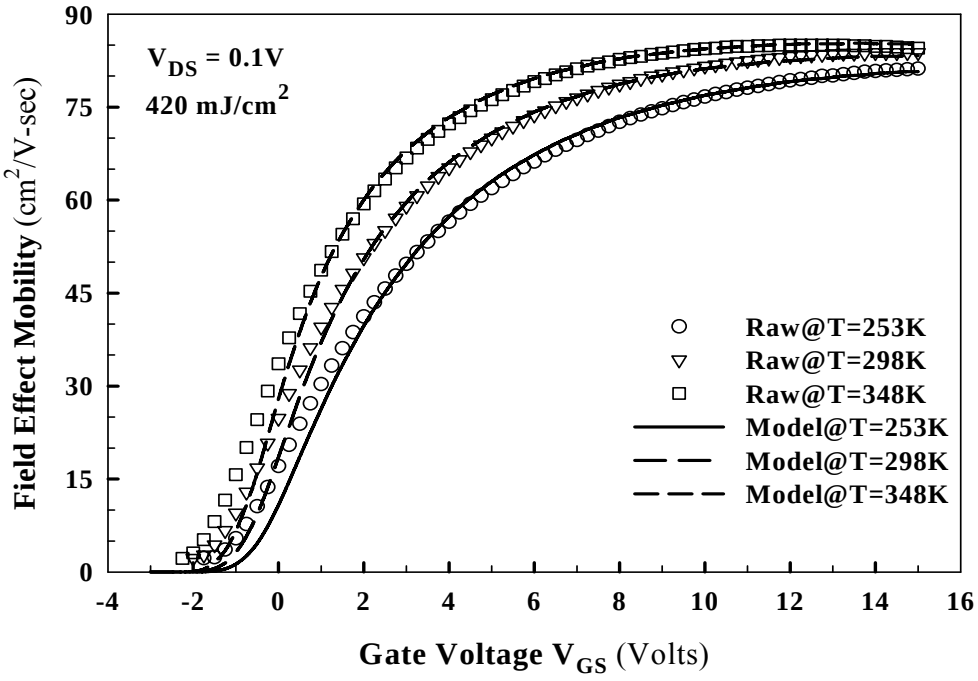
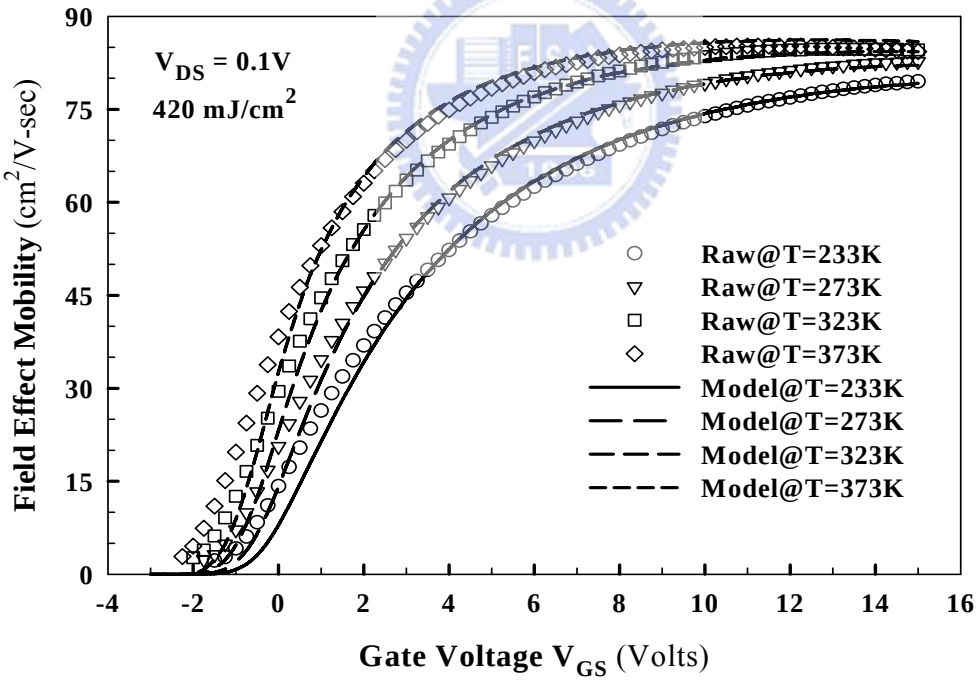


Fig.2-5 The activation energy E_A extracted from the *W/L = 6μm / 6μm* N-type Poly-Si TFT ***without LDD structure***

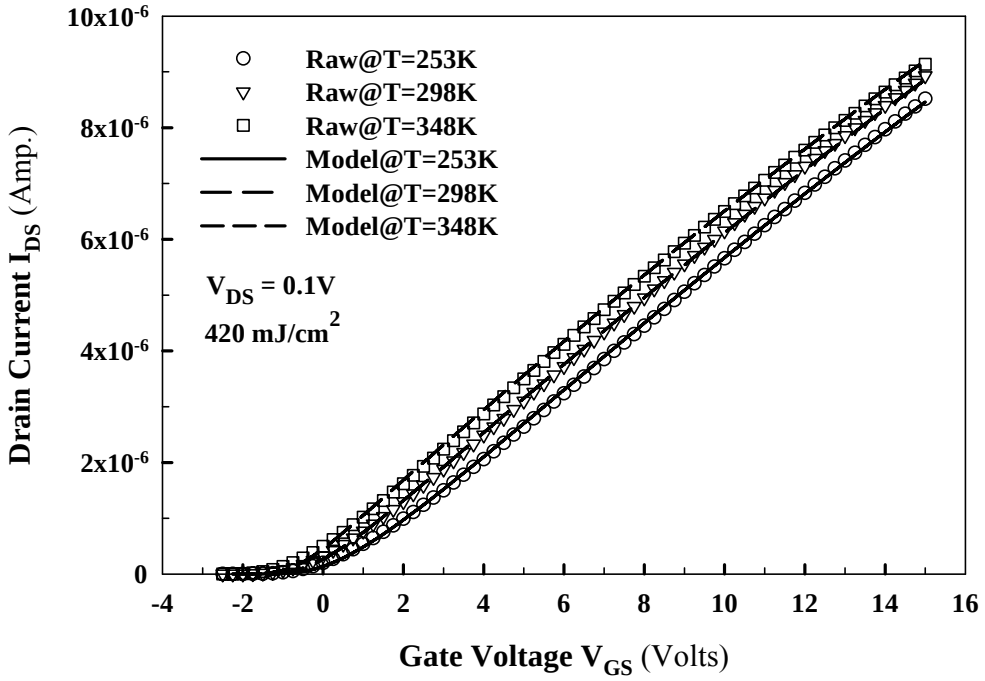


(a)

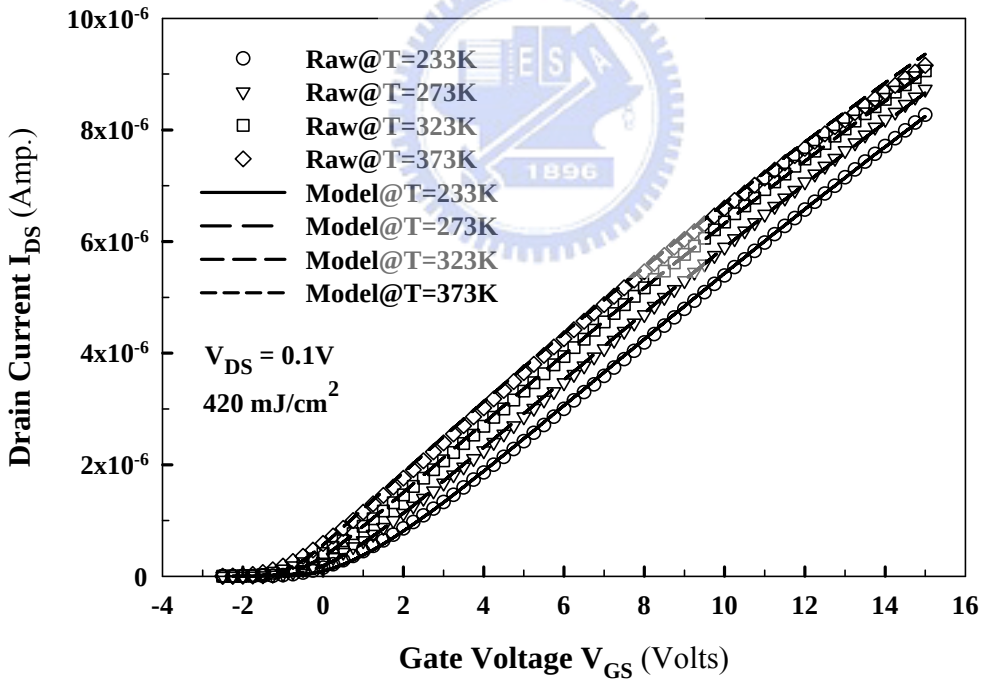


(b)

Fig.2-6 The comparison between the raw extracted mobility values and the modeling mobility values for the *W/L = 6μm / 6μm* N-type Poly-Si TFT ***without LDD structure*** at various temperatures: (a) T = 253K, 298K and 348K; (b) T = 233K, 273K, 323K and 373K



(a)



(b)

Fig.2-7 The comparison between the measured transfer characteristics and the modeling transfer characteristics for the *W/L = 6μm / 6μm* N-type Poly-Si TFT ***without LDD structure*** at various temperatures: (a) T = 253K, 298K and 348K; (b) T = 233K, 273K, 323K and 373K

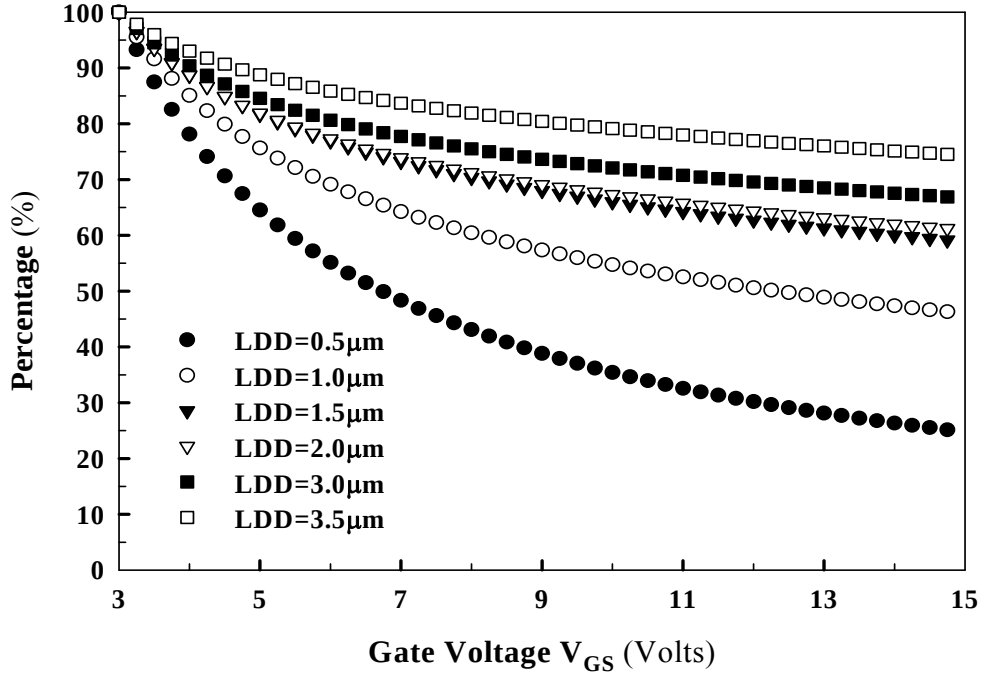


Fig.3-1 The parasitic resistance percentage comparison between the *W/L = 6μm / 6μm* N-type Poly-Si TFT's with different LDD lengths from V_{GS}=3V to V_{GS}=15V

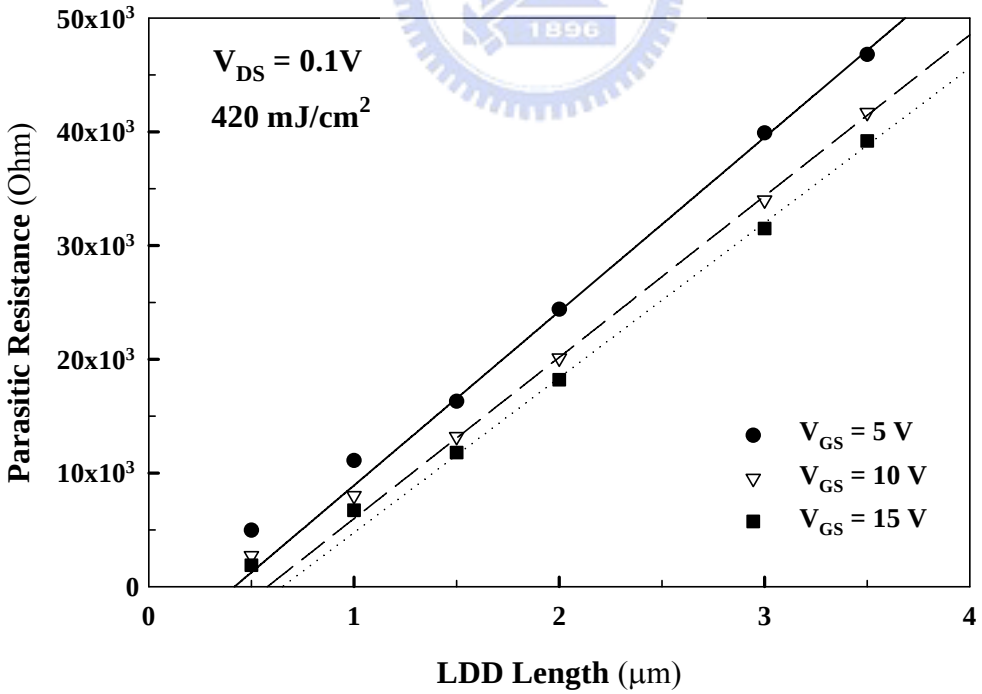


Fig.3-2 The relation between the parasitic resistance and the LDD length including the linear fits for the extracted data of the *W/L = 6μm / 6μm* N-type Poly-Si TFT's with larger LDD lengths

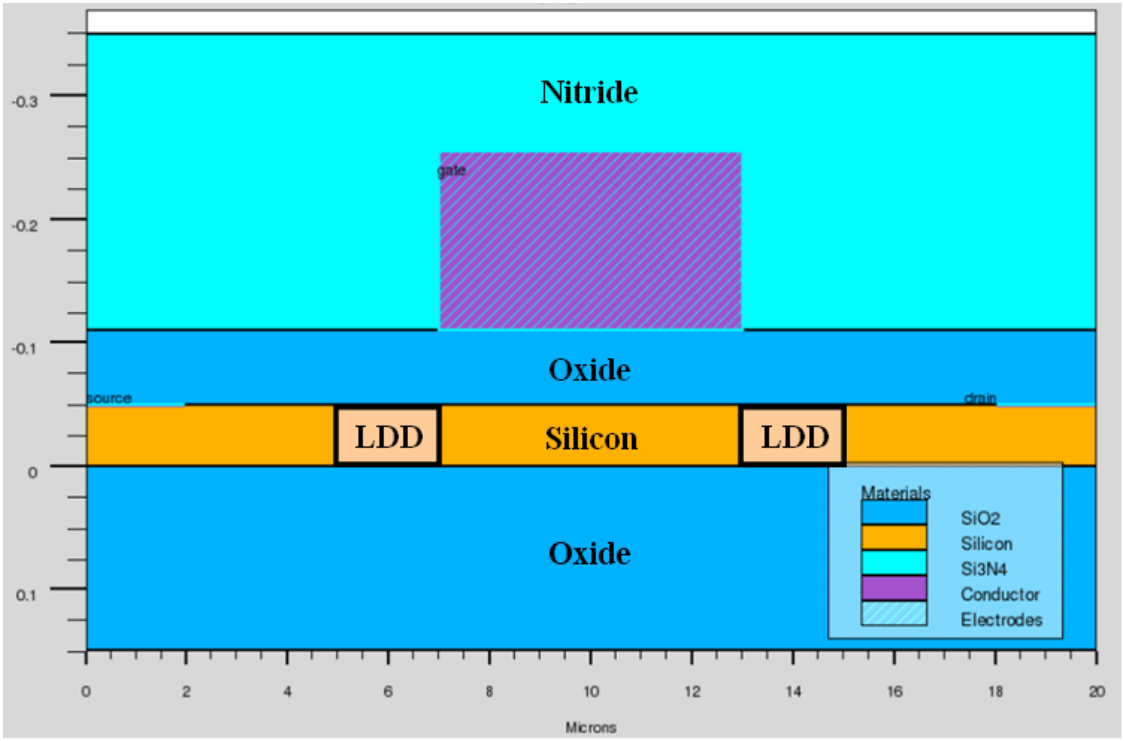
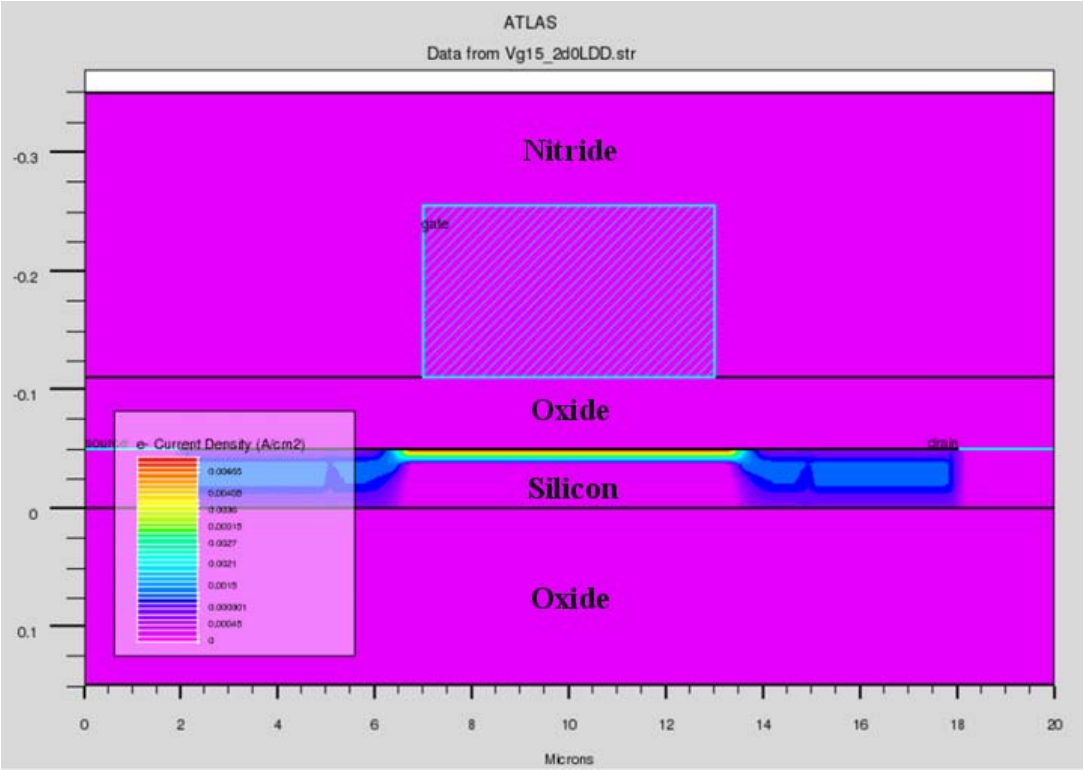
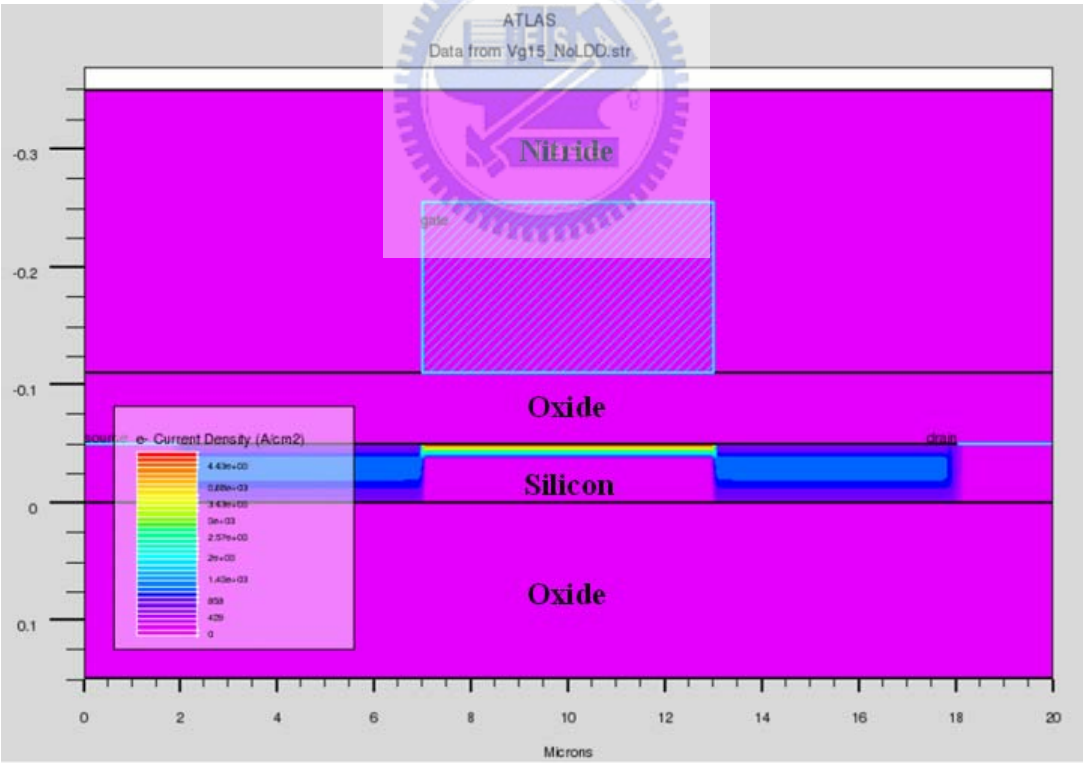


Fig.3-3 The device structure which is used in device simulation performed by Silvaco TCAD

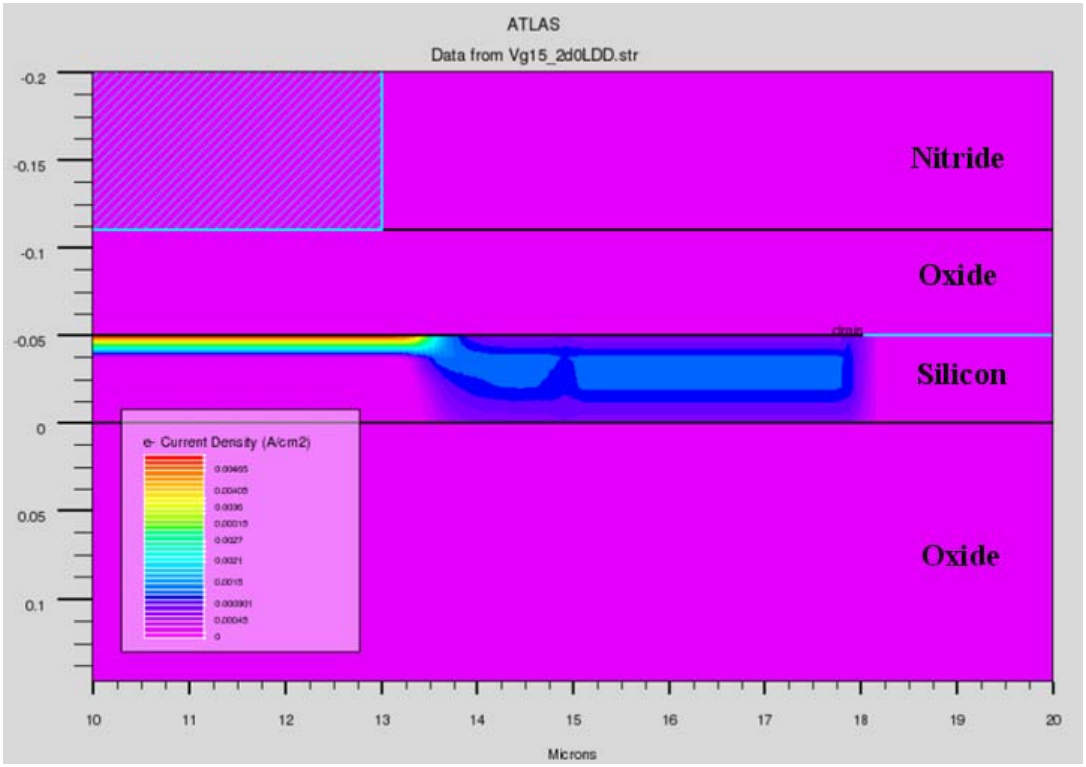


(a)

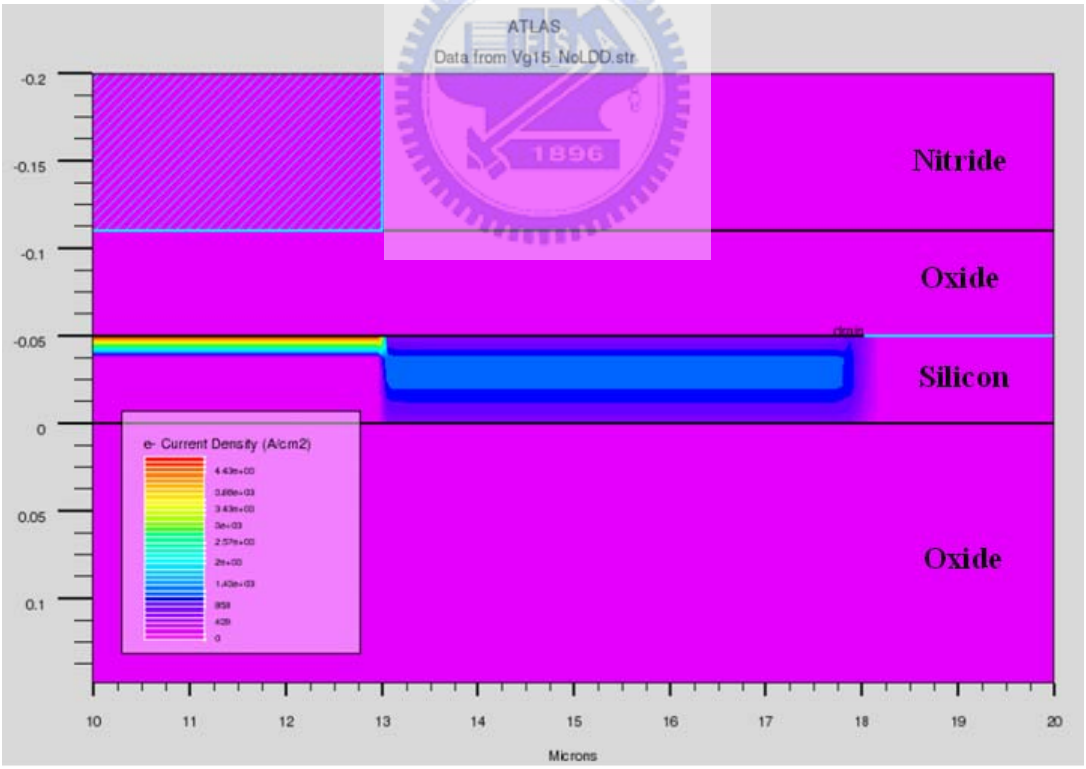


(b)

Fig.3-4 The comparison of the current density distribution simulation results between the devices (a) with and (b) without LDD structure

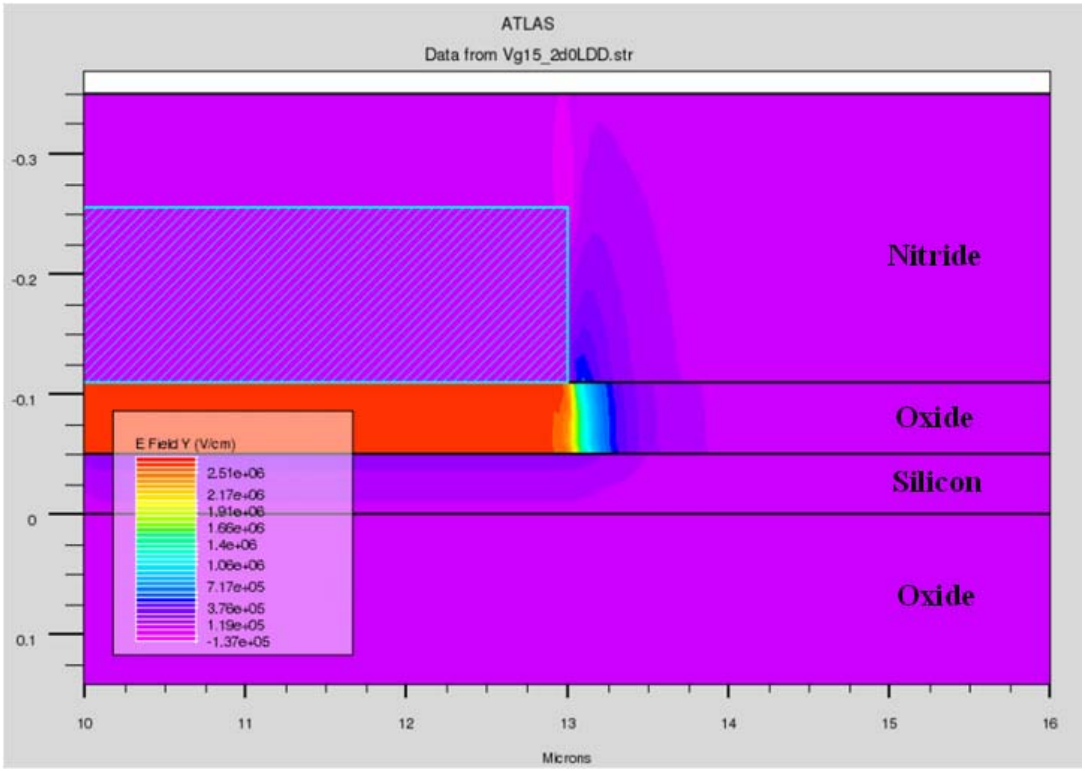


(a)

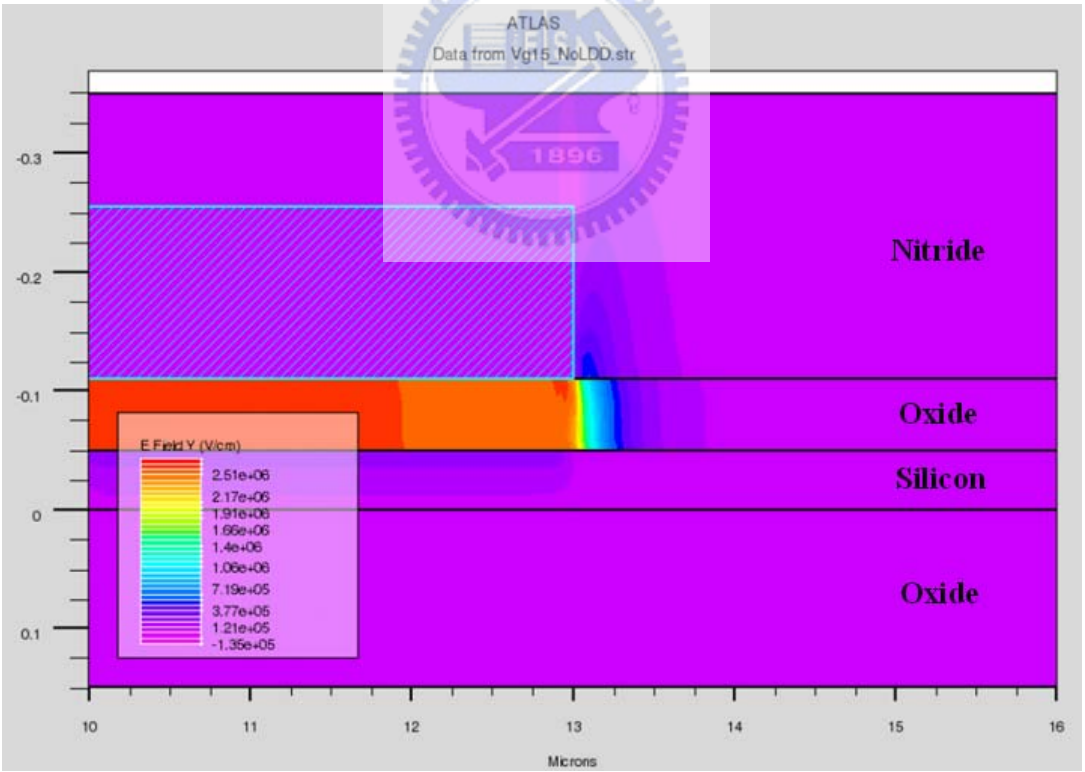


(b)

Fig.3-5 The comparison of the zoom-in on current density distribution simulation results between the devices (a) with and (b) without LDD structure

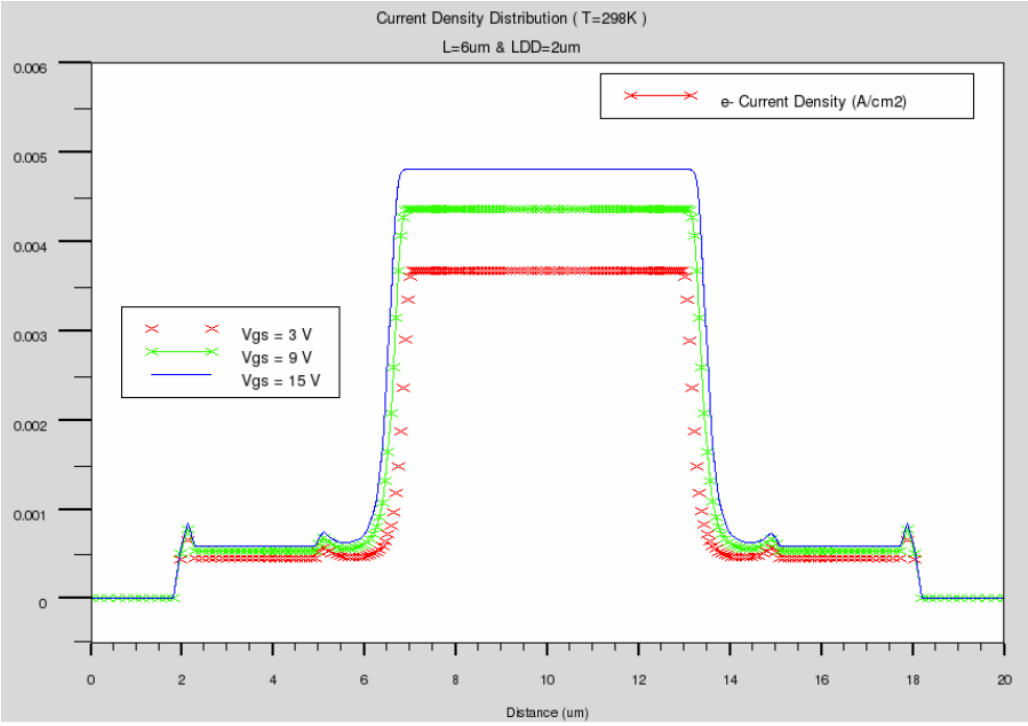


(a)

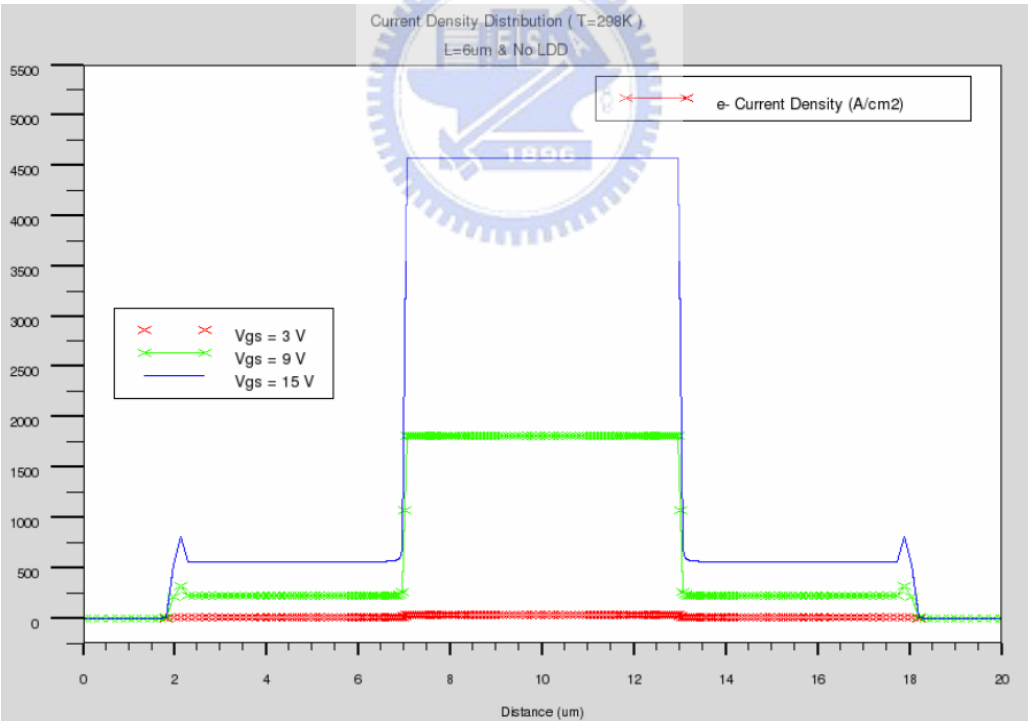


(b)

Fig.3-6 The comparison of the zoom-in on vertical electric field distribution simulation results between the devices (a) with and (b) without LDD structure



(a)



(b)

Fig.3-7 The comparison of the current density distribution simulation results from source side (Distance = 0μm) to drain side (Distance = 20μm) between the devices (a) with and (b) without LDD structure

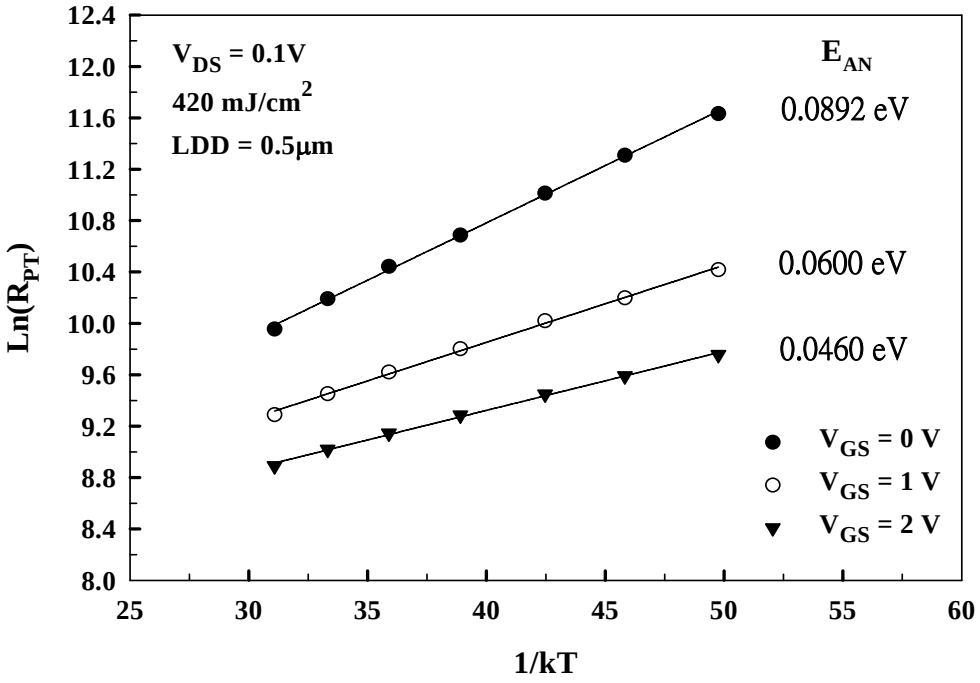


Fig.3-8 The extraction method for the activation energy of the parasitic transistor E_{AN} due to thermionic emission effect from the *W/L = 6μm / 6μm* N-type Poly-Si TFT with ***0.5μm LDD length***

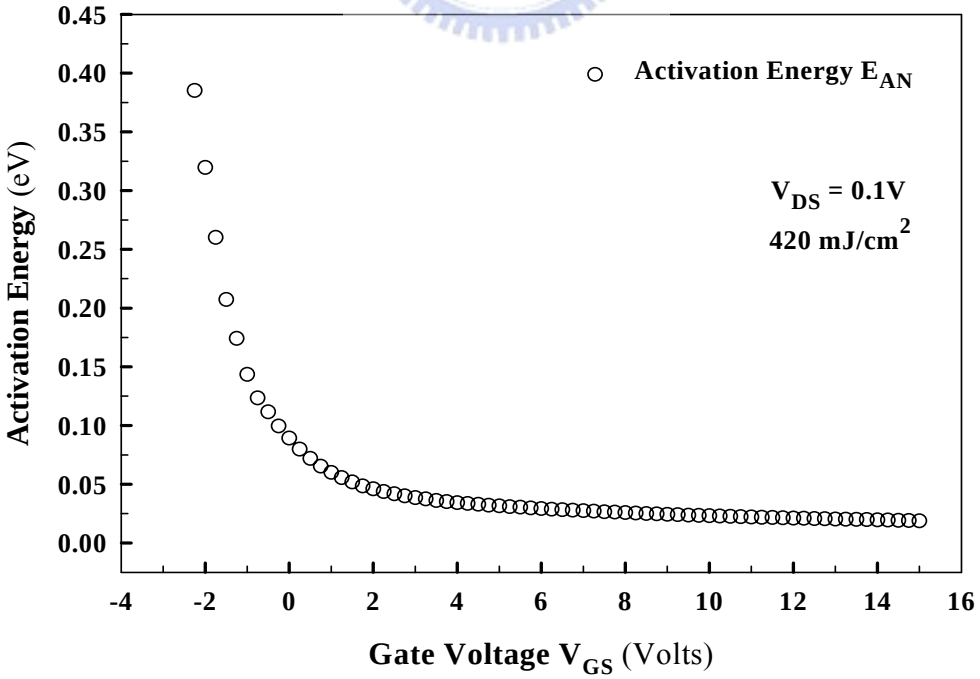


Fig.3-9 The activation energy of the parasitic transistor E_{AN} extracted from the *W/L = 6μm / 6μm* N-type Poly-Si TFT with ***0.5μm LDD length***

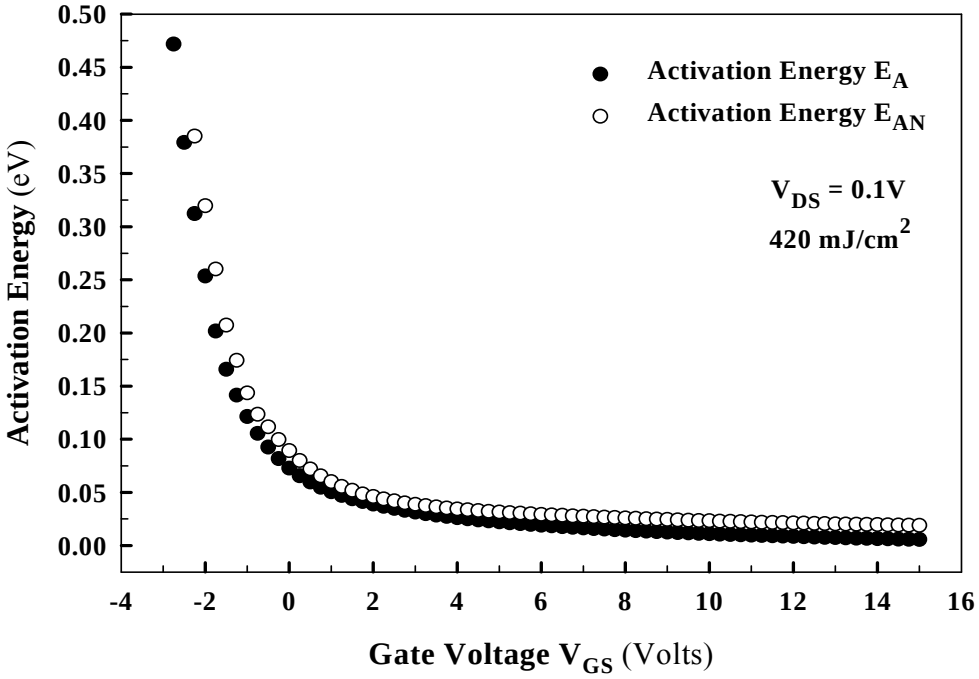


Fig.3-10 The comparison between the activation energy E_A extracted from the measured transfer characteristics of the *W/L = 6μm / 6μm* N-type Poly-Si TFT ***without LDD structure*** and the activation energy of the parasitic transistor E_{AN} extracted from the extracted parasitic resistance of the *W/L = 6μm / 6μm* N-type Poly-Si TFT ***with 0.5μm LDD length***

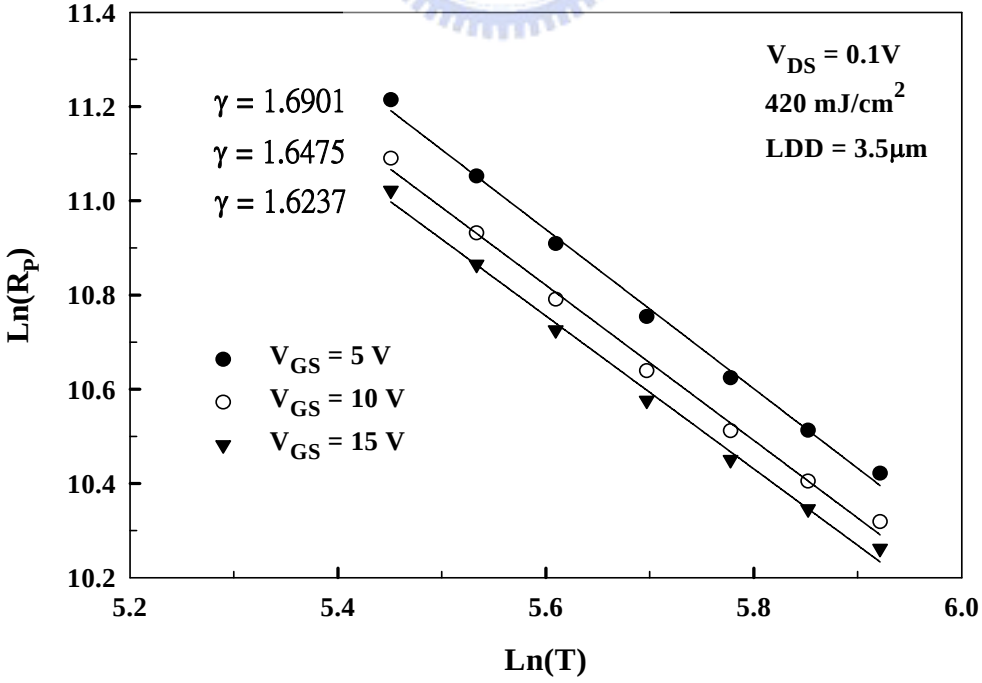
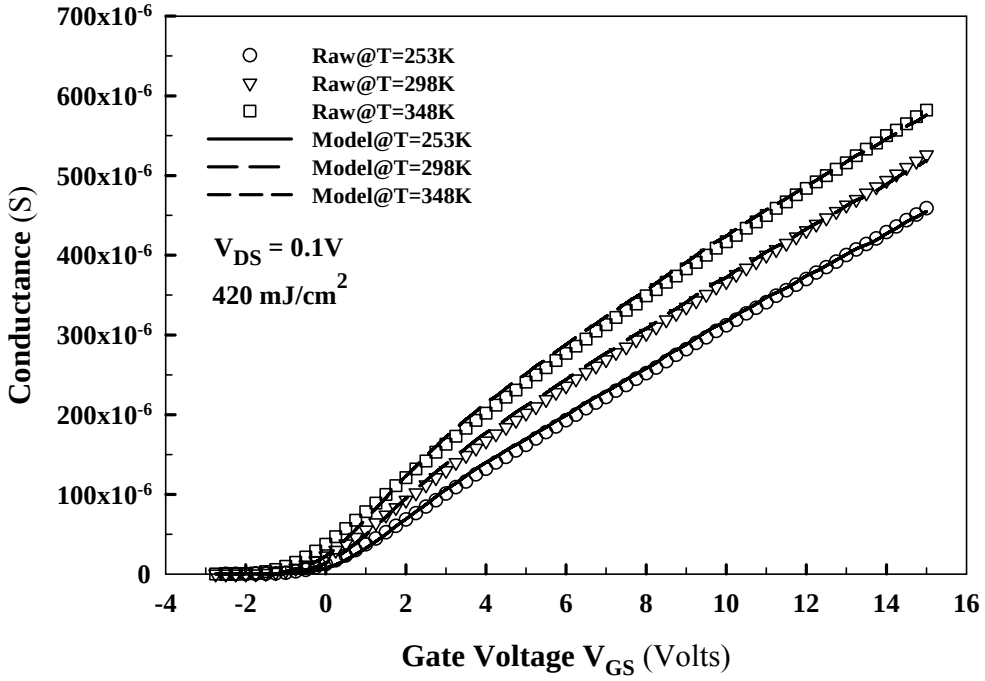
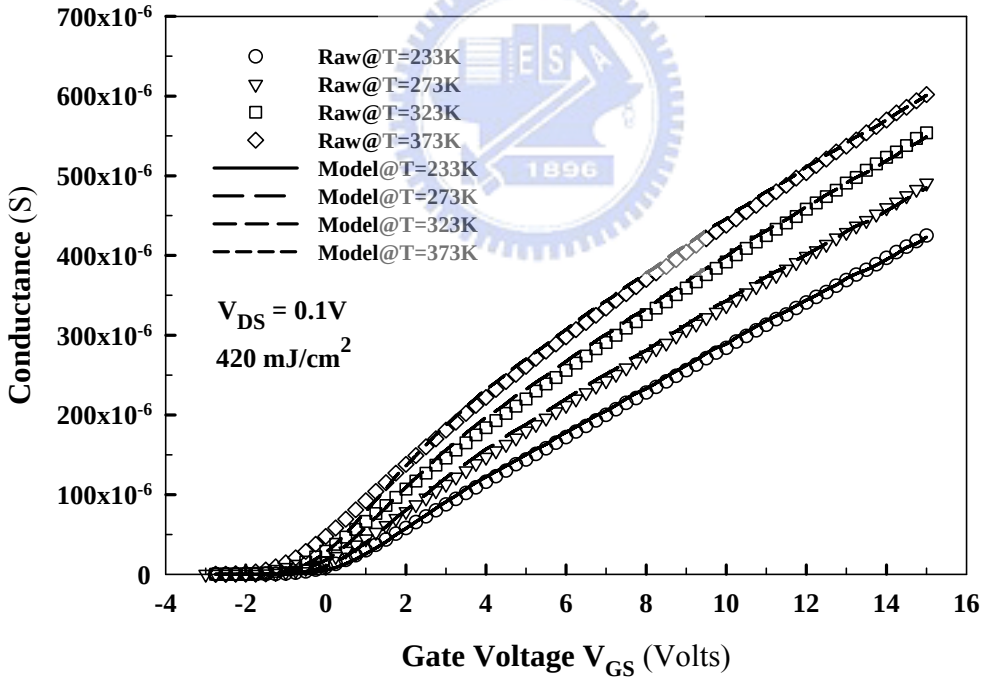


Fig.3-11 The extraction method of the temperature dependence coefficient γ due to impurity scattering effect for the *W/L = 6μm / 6μm* N-type Poly-Si TFT ***with 3.5μm LDD length***

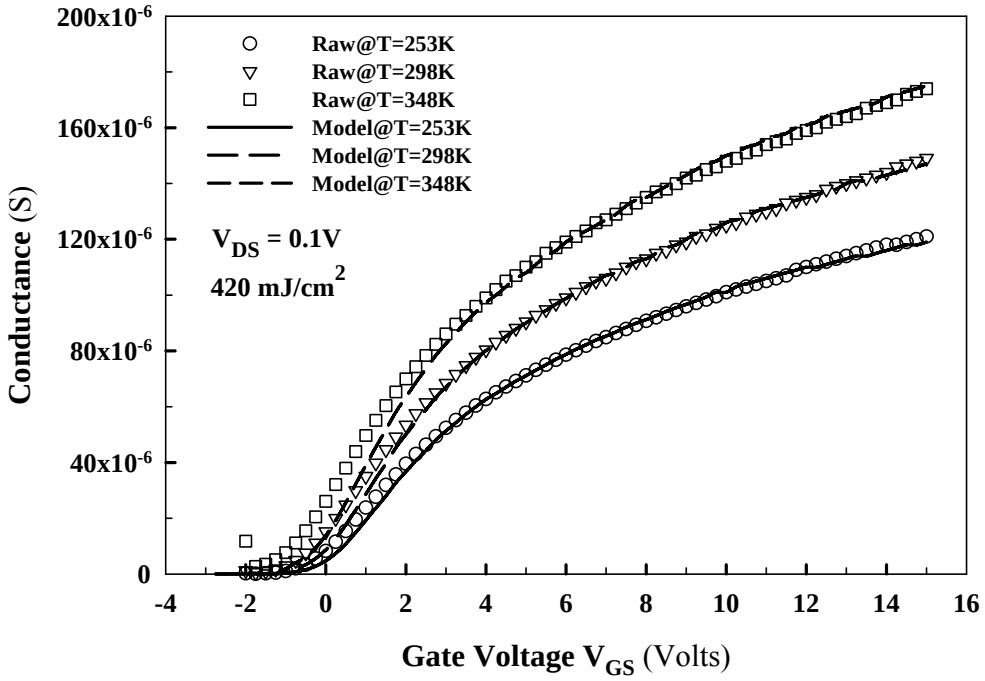


(a)

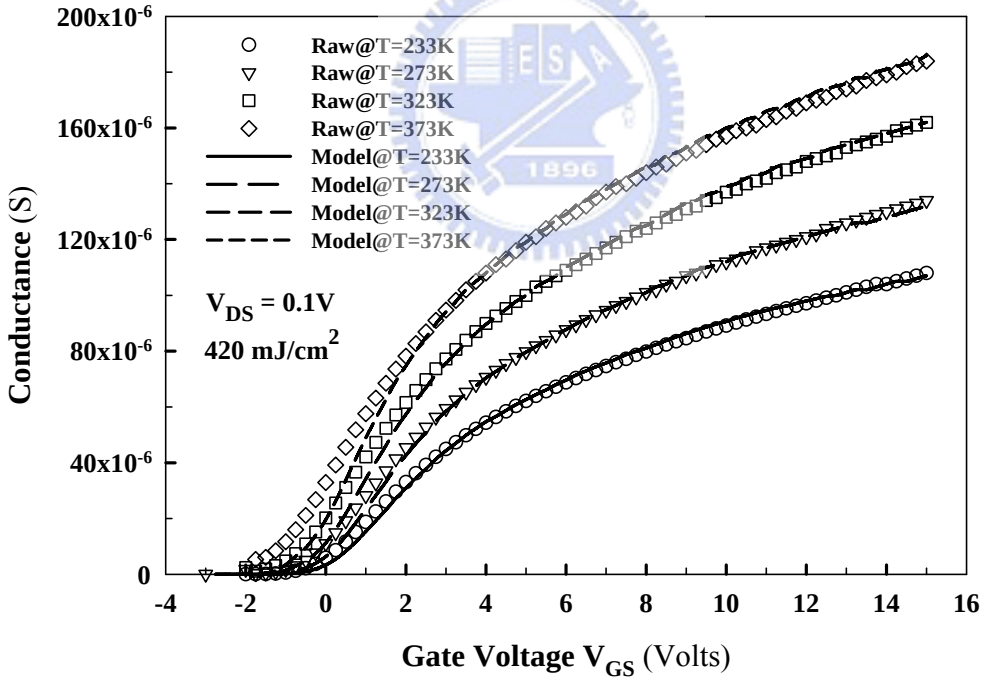


(b)

Fig.3-12 The comparison between the extracted conductance and the modeling conductance for the *W/L = 6μm / 6μm* N-type Poly-Si TFT with ***0.5μm LDD length*** at various temperatures: (a) T = 253K, 298K and 348K; (b) T = 233K, 273K, 323K and 373K

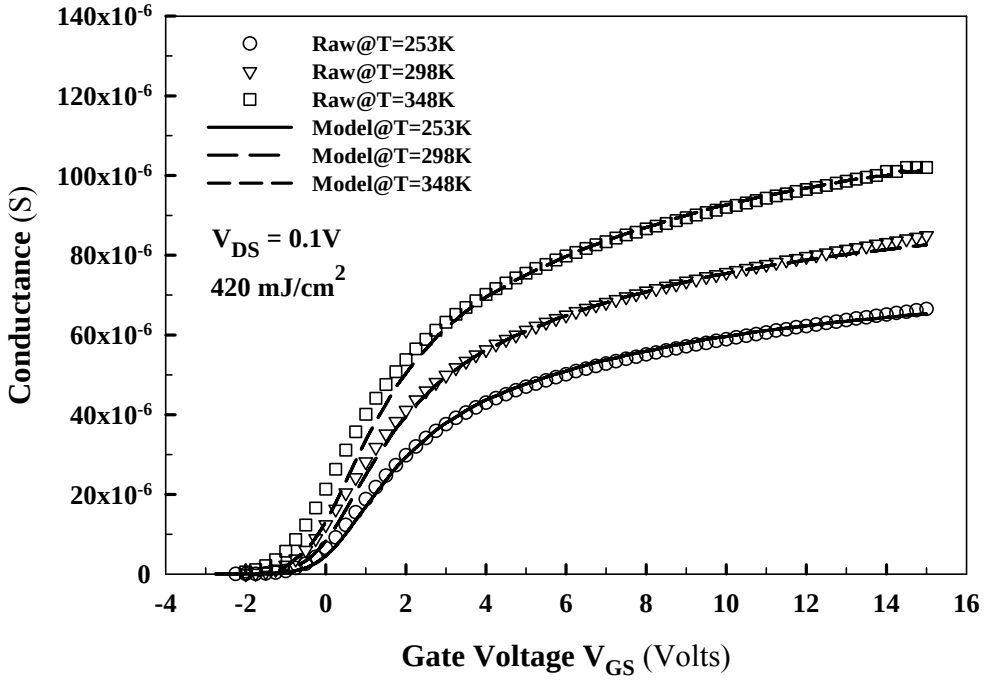


(a)

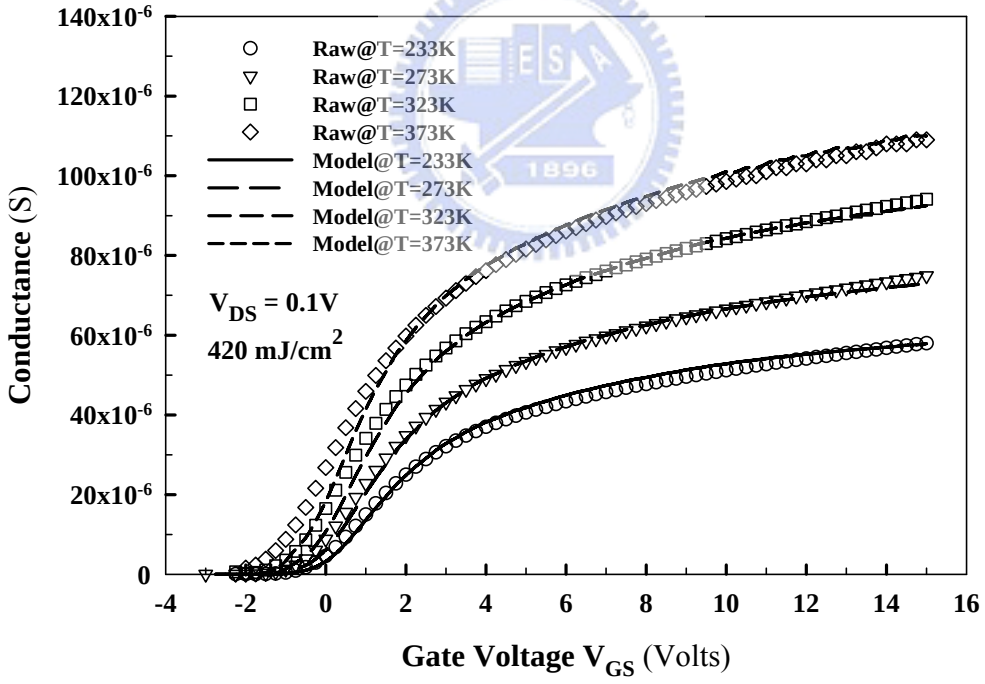


(b)

Fig.3-13 The comparison between the extracted conductance and the modeling conductance for the *W/L = 6μm / 6μm* N-type Poly-Si TFT with ***1.0μm LDD length*** at various temperatures: (a) T = 253K, 298K and 348K; (b) T = 233K, 273K, 323K and 373K

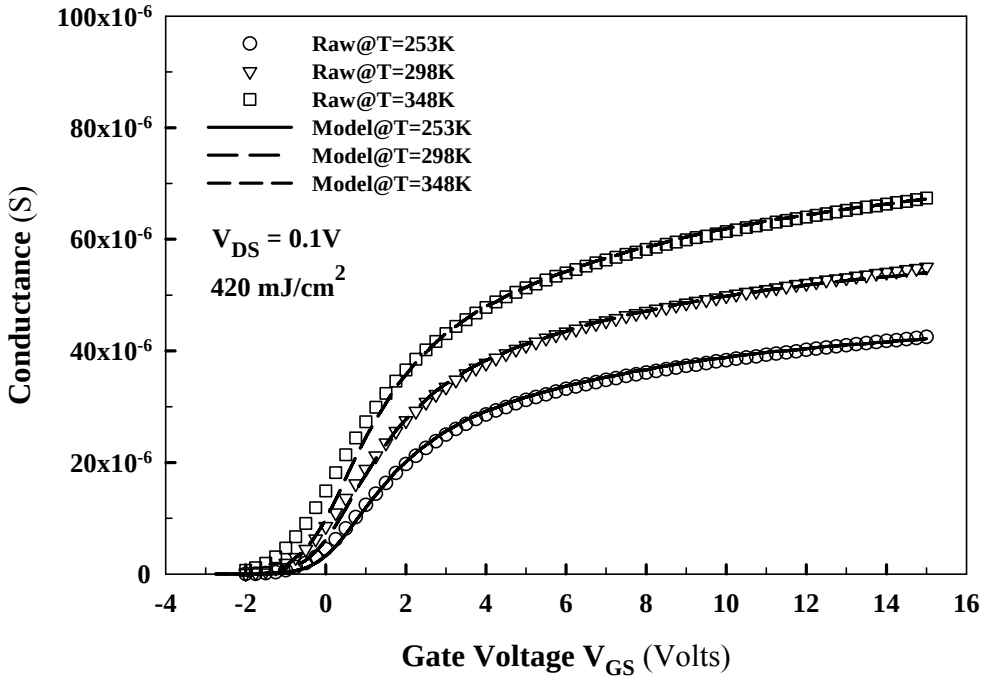


(a)

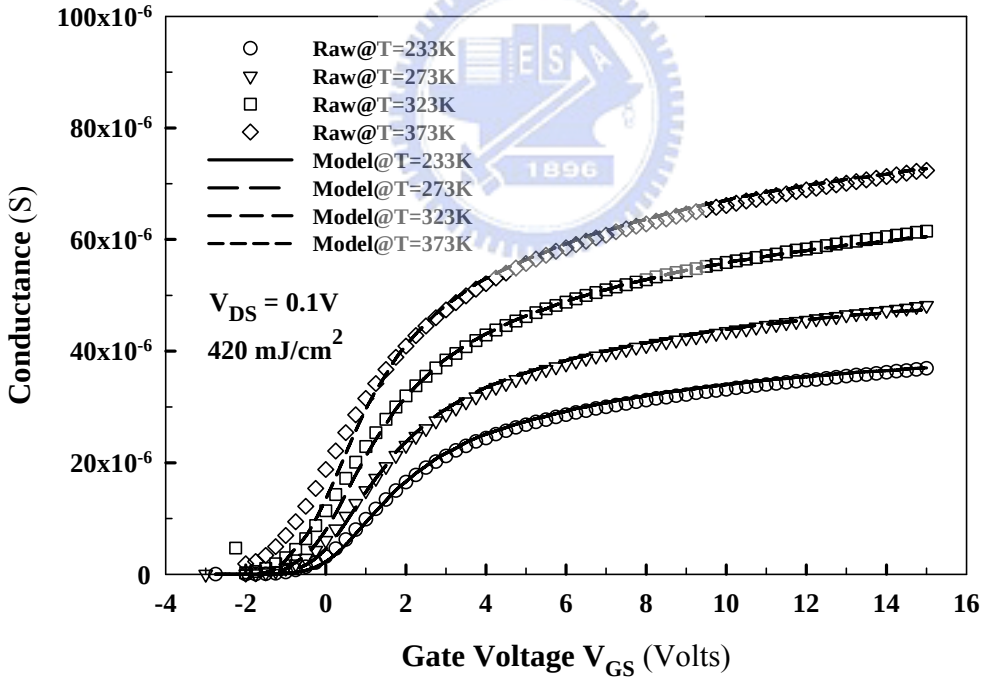


(b)

Fig.3-14 The comparison between the extracted conductance and the modeling conductance for the *W/L = 6μm / 6μm* N-type Poly-Si TFT with ***1.5μm LDD length*** at various temperatures: (a) T = 253K, 298K and 348K; (b) T = 233K, 273K, 323K and 373K

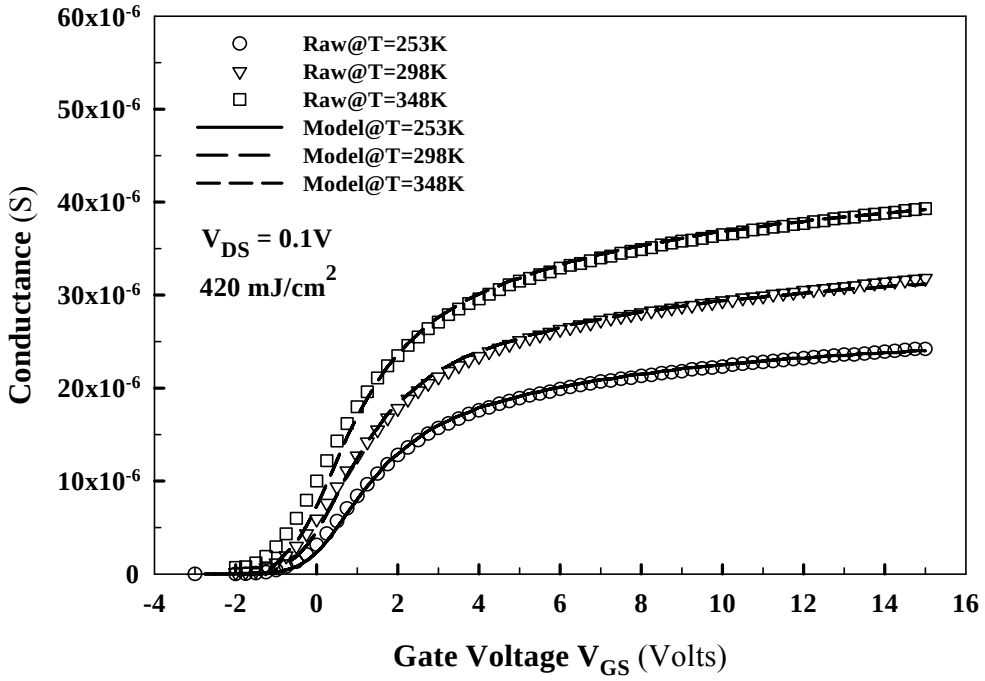


(a)

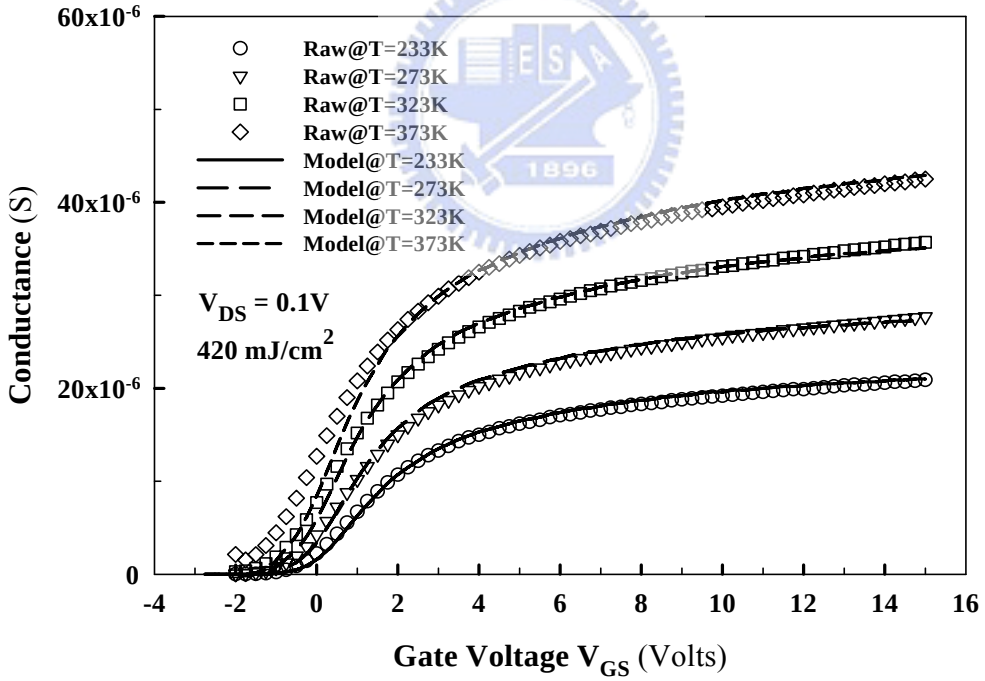


(b)

Fig.3-15 The comparison between the extracted conductance and the modeling conductance for the *W/L = 6μm / 6μm* N-type Poly-Si TFT with ***2.0μm LDD length*** at various temperatures: (a) T = 253K, 298K and 348K; (b) T = 233K, 273K, 323K and 373K

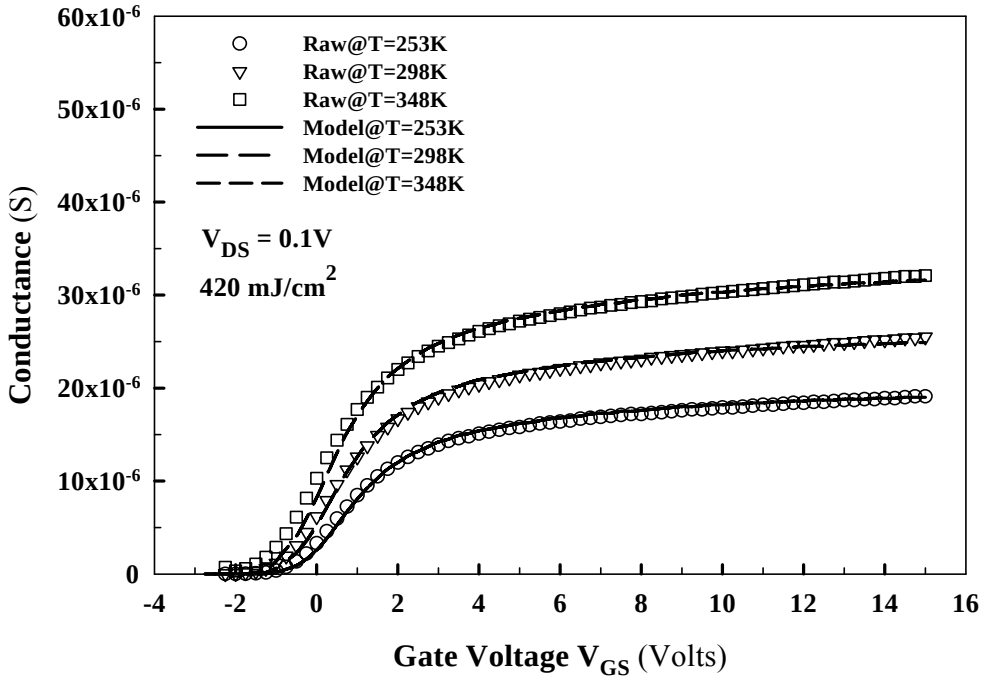


(a)

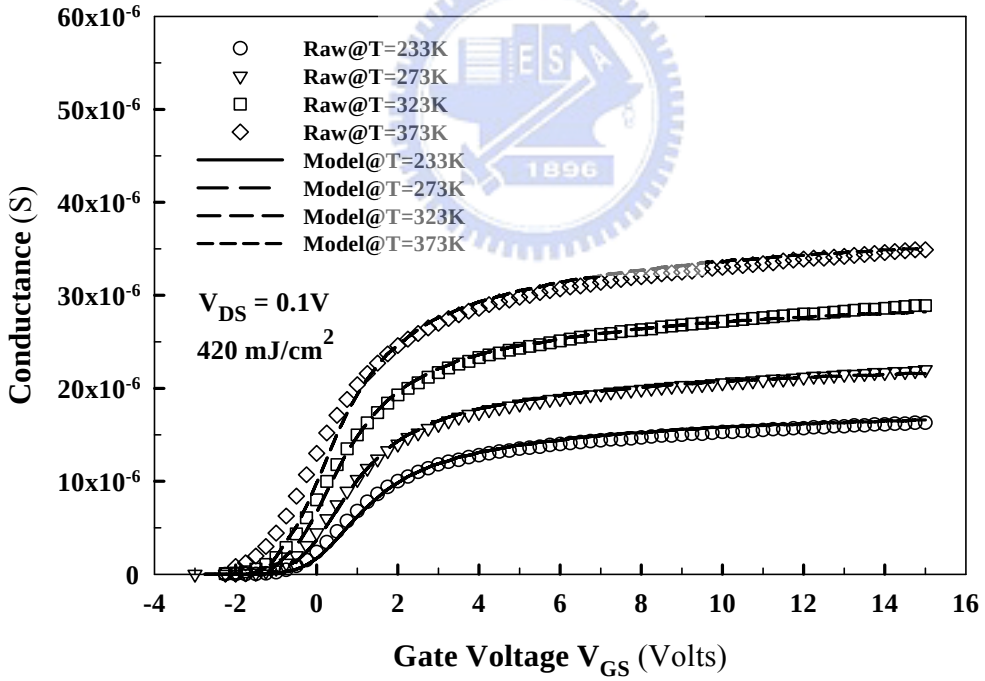


(b)

Fig.3-16 The comparison between the extracted conductance and the modeling conductance for the *W/L = 6μm / 6μm* N-type Poly-Si TFT with ***3.0μm LDD length*** at various temperatures: (a) T = 253K, 298K and 348K; (b) T = 233K, 273K, 323K and 373K

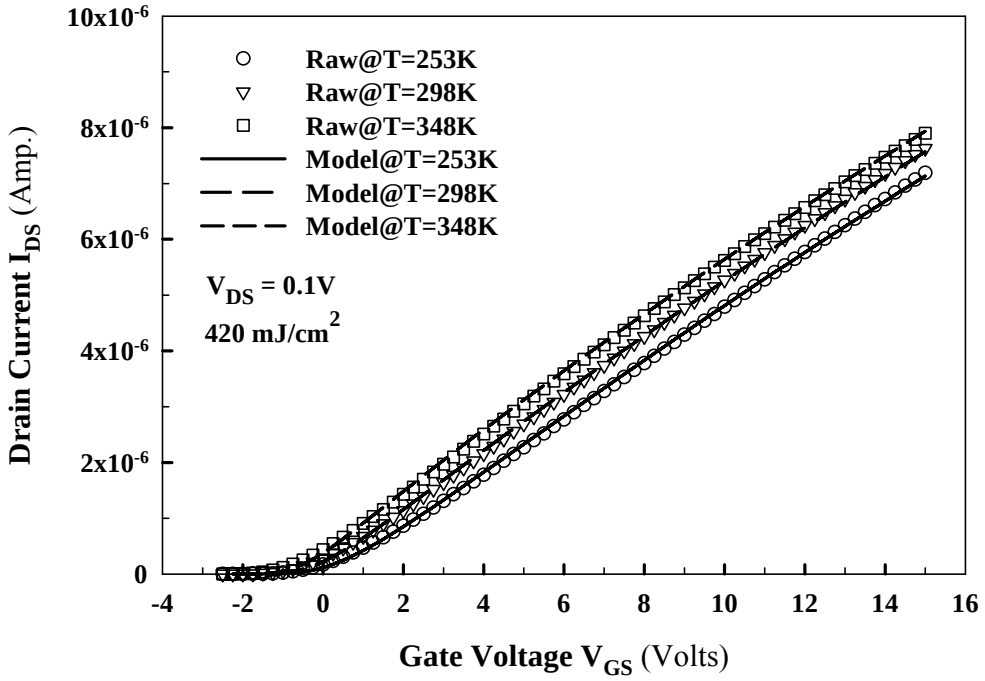


(a)

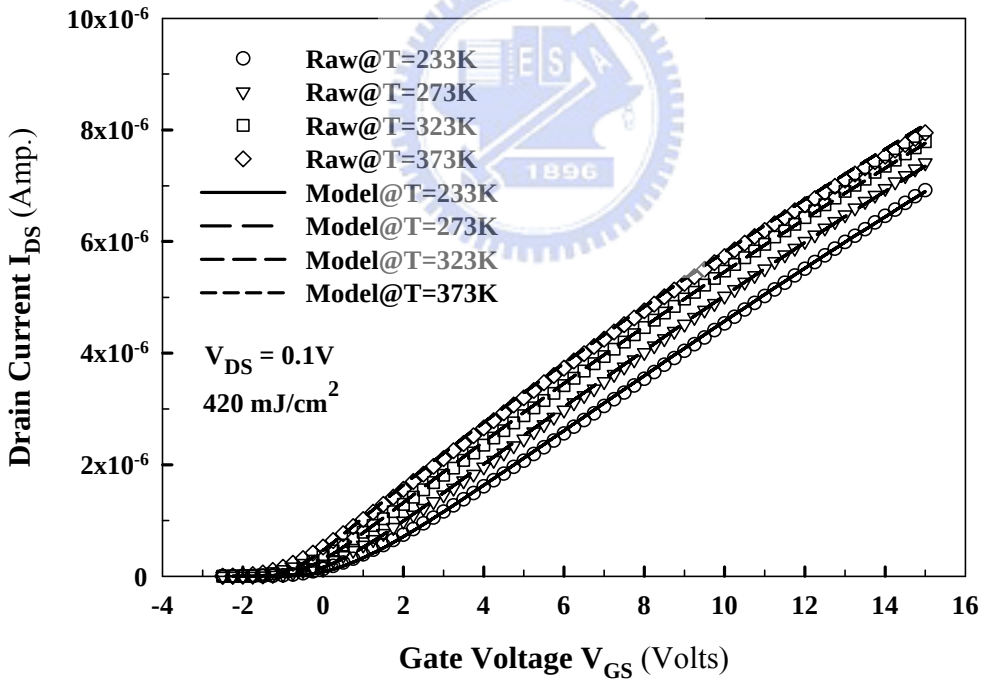


(b)

Fig.3-17 The comparison between the extracted conductance and the modeling conductance for the *W/L = 6μm / 6μm* N-type Poly-Si TFT with ***3.5μm LDD length*** at various temperatures: (a) T = 253K, 298K and 348K; (b) T = 233K, 273K, 323K and 373K

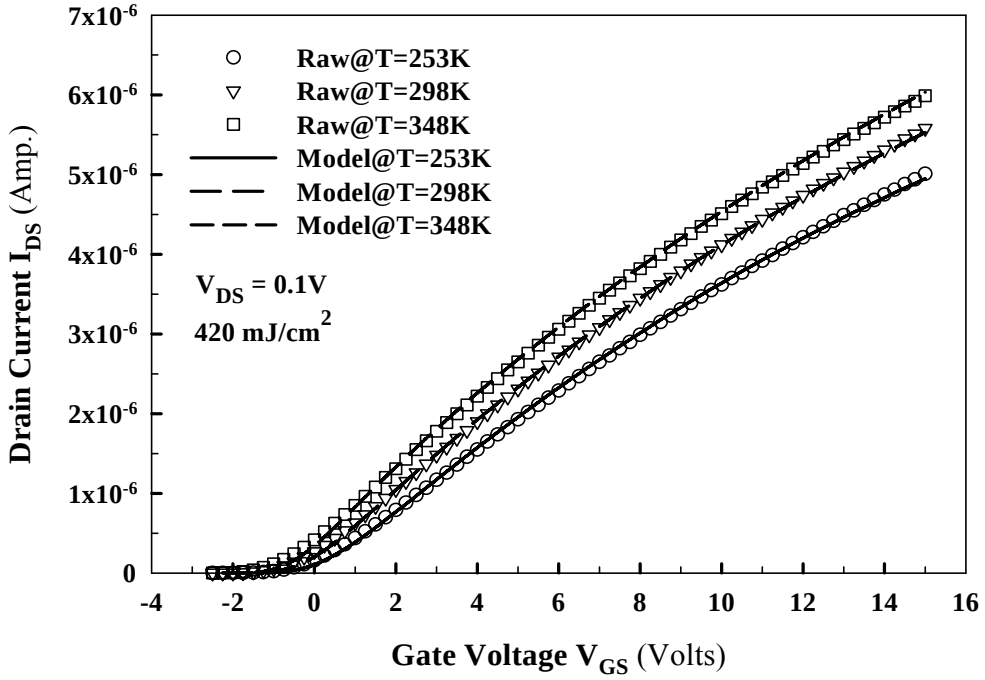


(a)

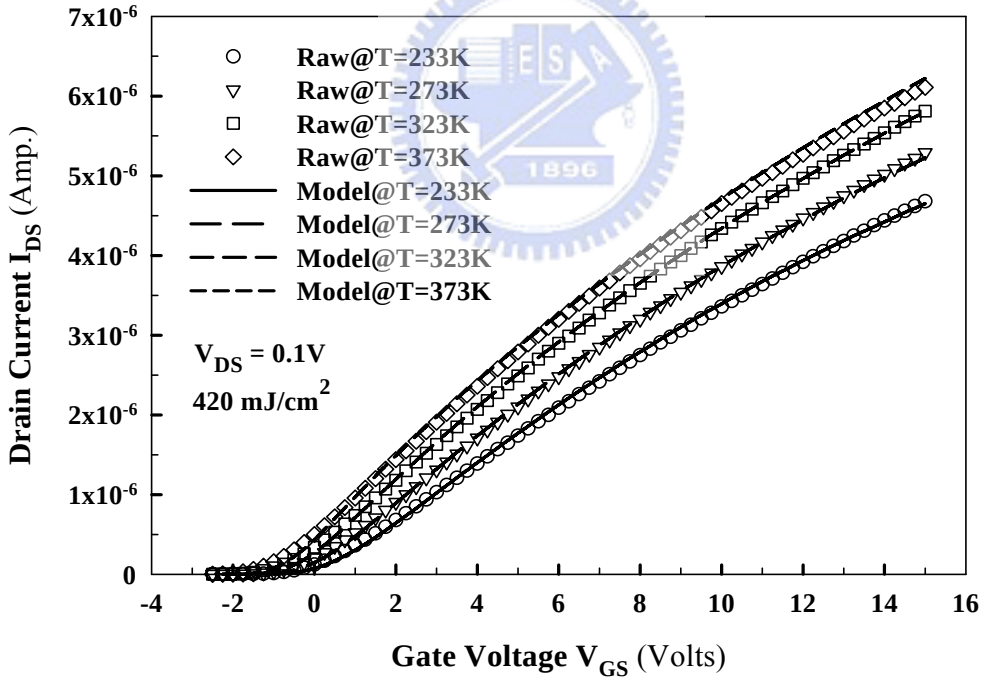


(b)

Fig.3-18 The comparison between the measured transfer characteristics and the modeling transfer characteristics for the *W/L = 6μm / 6μm* N-type Poly-Si TFT with ***0.5μm LDD length*** at various temperatures: (a) T = 253K, 298K and 348K; (b) T = 233K, 273K, 323K and 373K

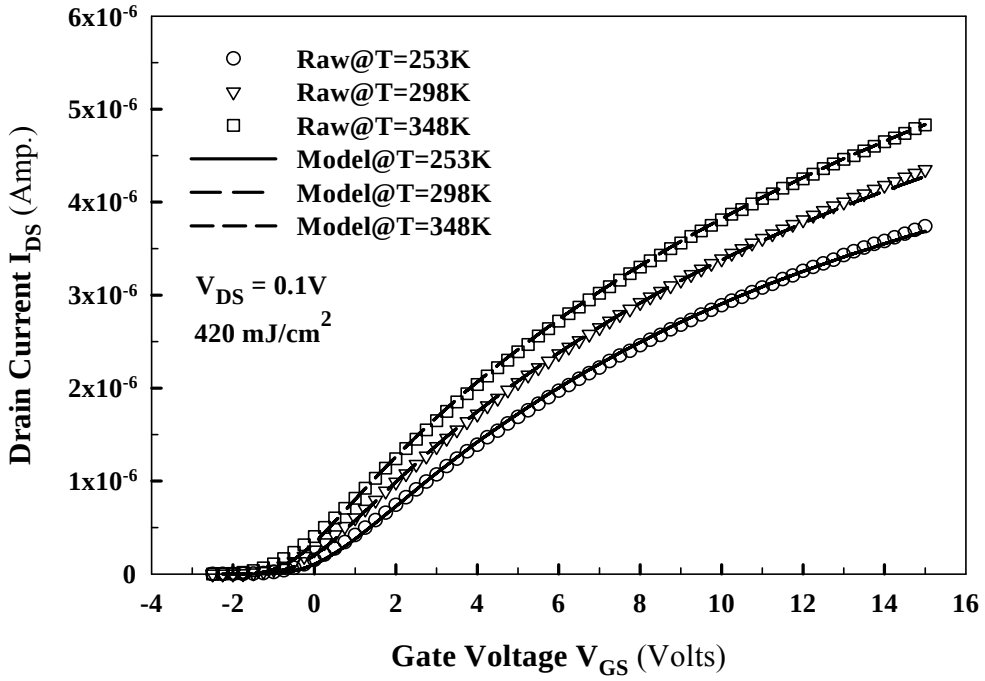


(a)

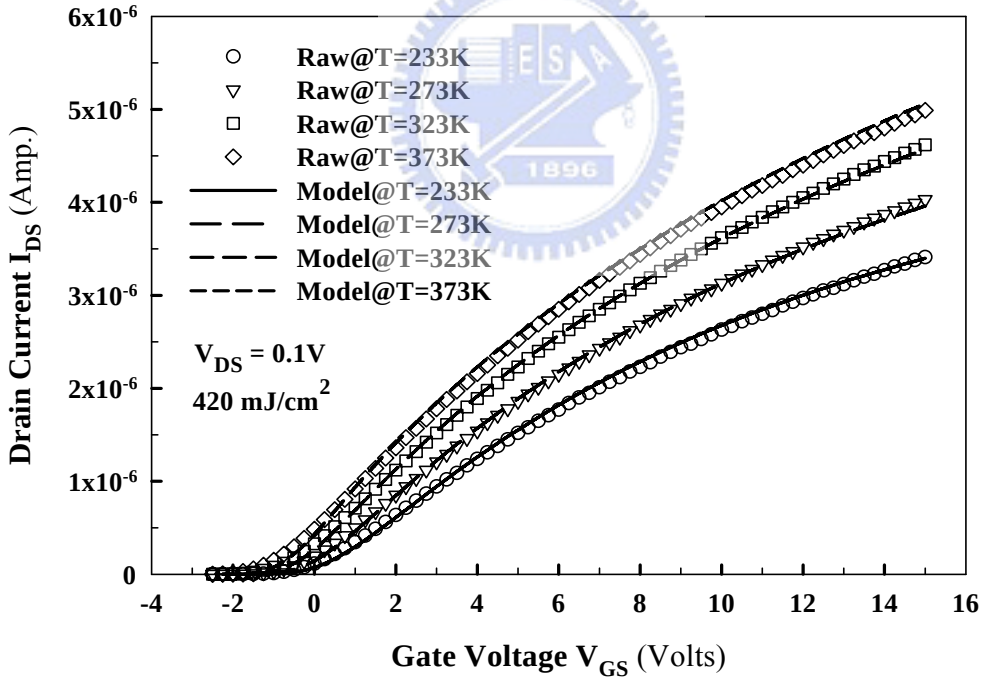


(b)

Fig.3-19 The comparison between the measured transfer characteristics and the modeling transfer characteristics for the *W/L = 6μm / 6μm* N-type Poly-Si TFT with ***1.0μm LDD length*** at various temperatures: (a) T = 253K, 298K and 348K; (b) T = 233K, 273K, 323K and 373K

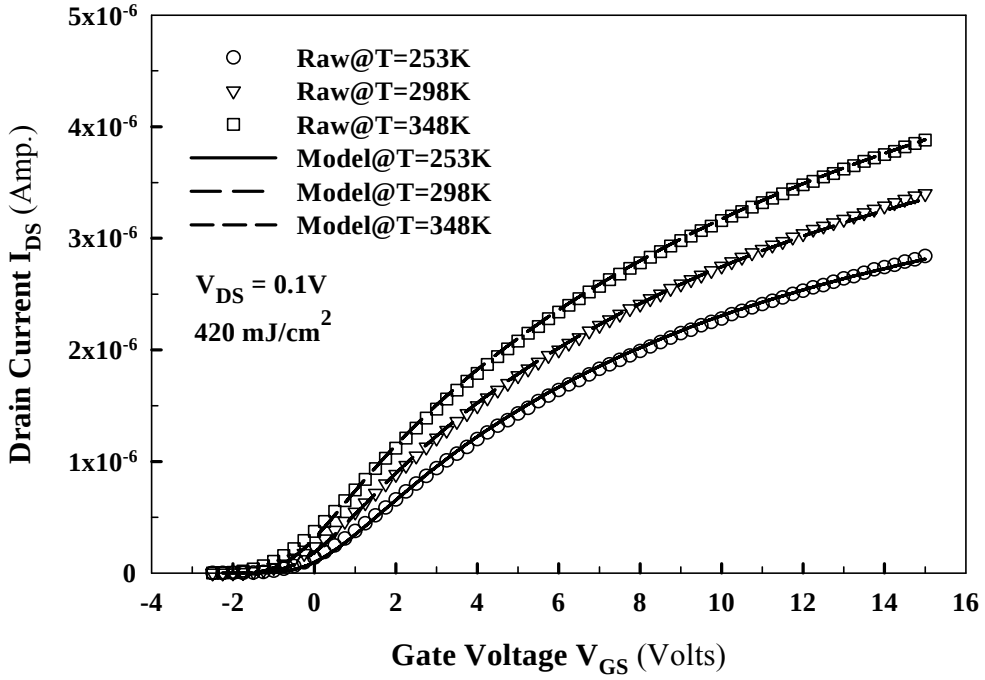


(a)

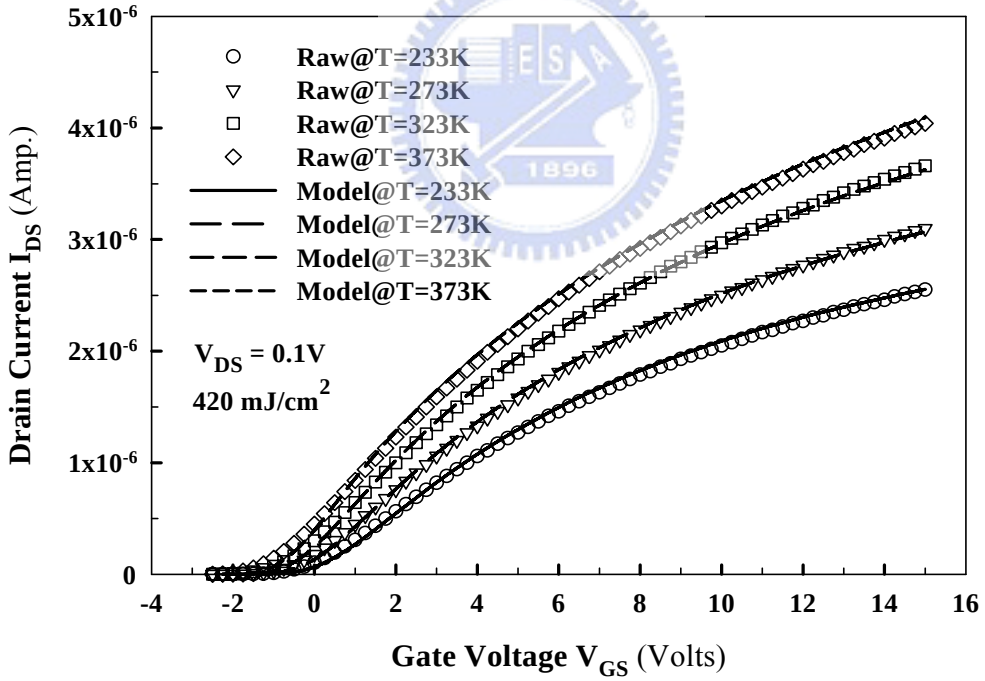


(b)

Fig.3-20 The comparison between the measured transfer characteristics and the modeling transfer characteristics for the *W/L = 6μm / 6μm* N-type Poly-Si TFT with ***1.5μm LDD length*** at various temperatures: (a) T = 253K, 298K and 348K; (b) T = 233K, 273K, 323K and 373K

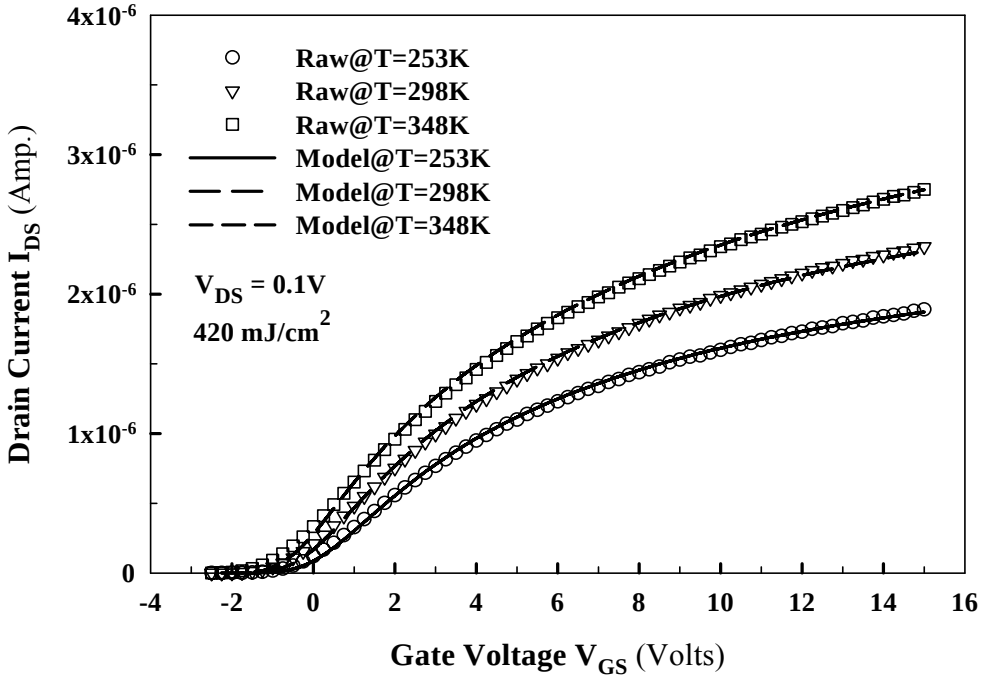


(a)

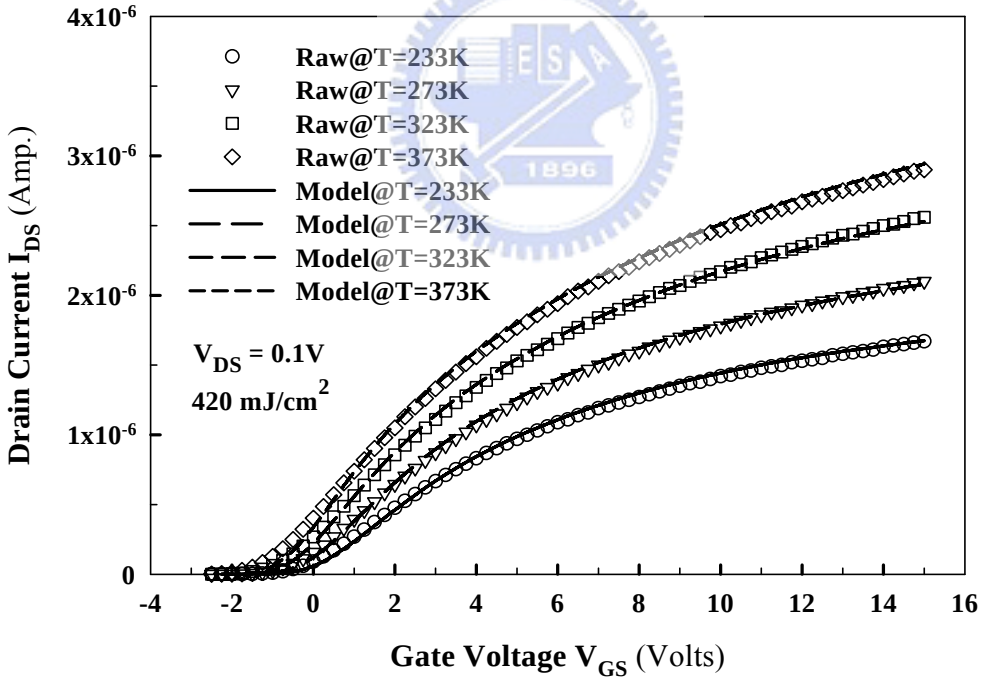


(b)

Fig.3-21 The comparison between the measured transfer characteristics and the modeling transfer characteristics for the *W/L = 6μm / 6μm* N-type Poly-Si TFT with ***2.0μm LDD length*** at various temperatures: (a) T = 253K, 298K and 348K; (b) T = 233K, 273K, 323K and 373K

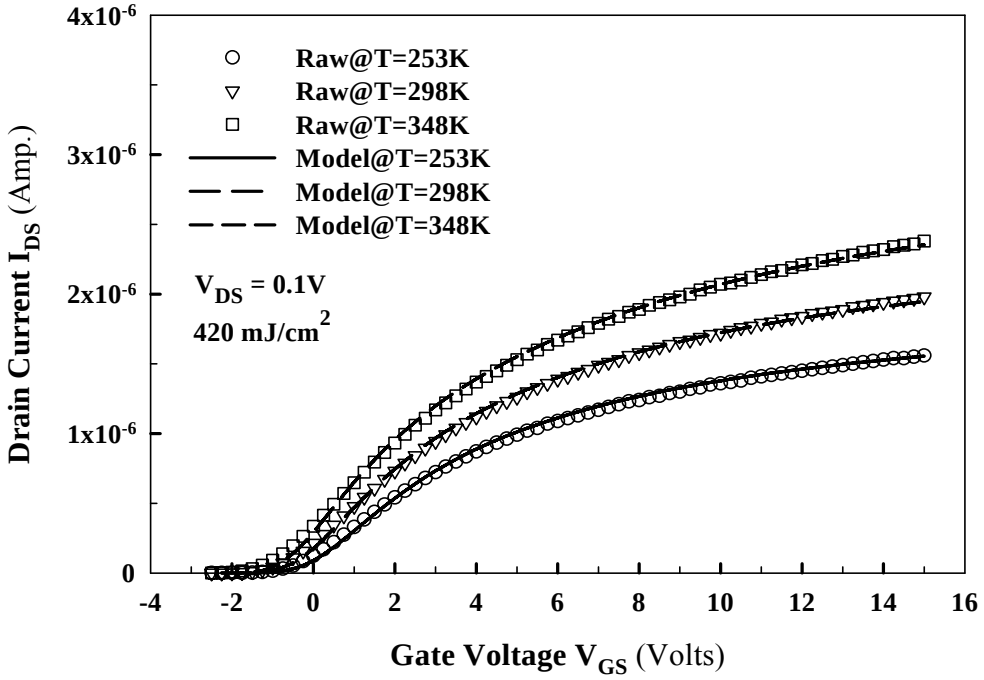


(a)

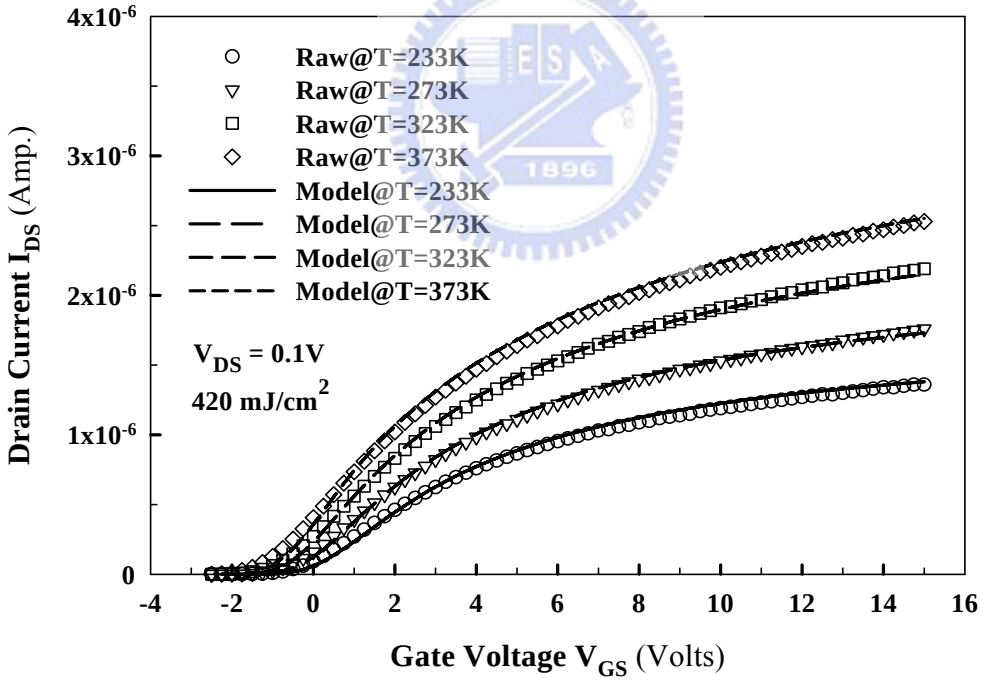


(b)

Fig.3-22 The comparison between the measured transfer characteristics and the modeling transfer characteristics for the *W/L = 6μm / 6μm* N-type Poly-Si TFT with ***3.0μm LDD length*** at various temperatures: (a) T = 253K, 298K and 348K; (b) T = 233K, 273K, 323K and 373K



(a)



(b)

Fig.3-23 The comparison between the measured transfer characteristics and the modeling transfer characteristics for the *W/L = 6μm / 6μm* N-type Poly-Si TFT with ***3.5μm LDD length*** at various temperatures: (a) T = 253K, 298K and 348K; (b) T = 233K, 273K, 323K and 373K

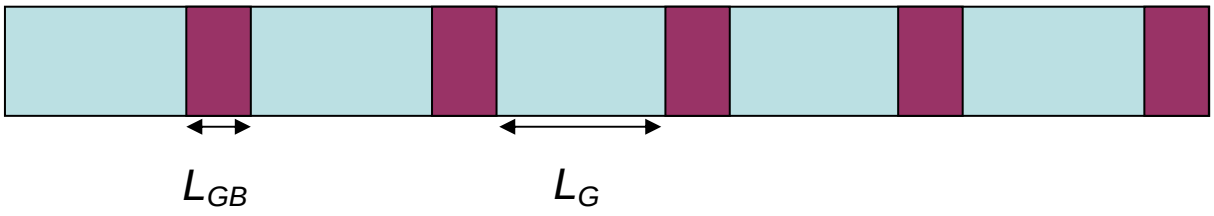
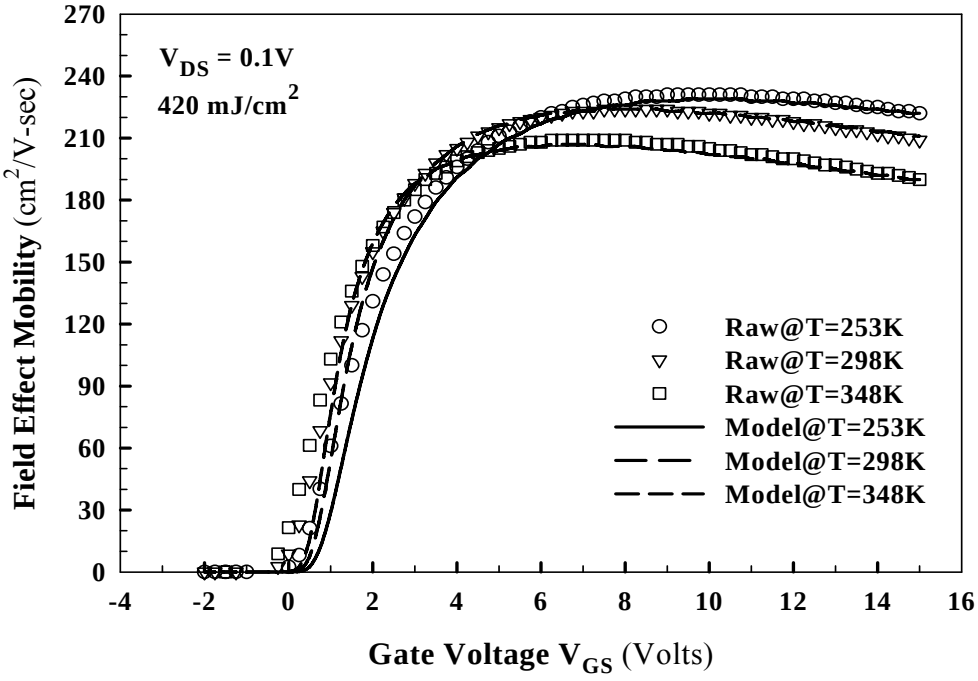
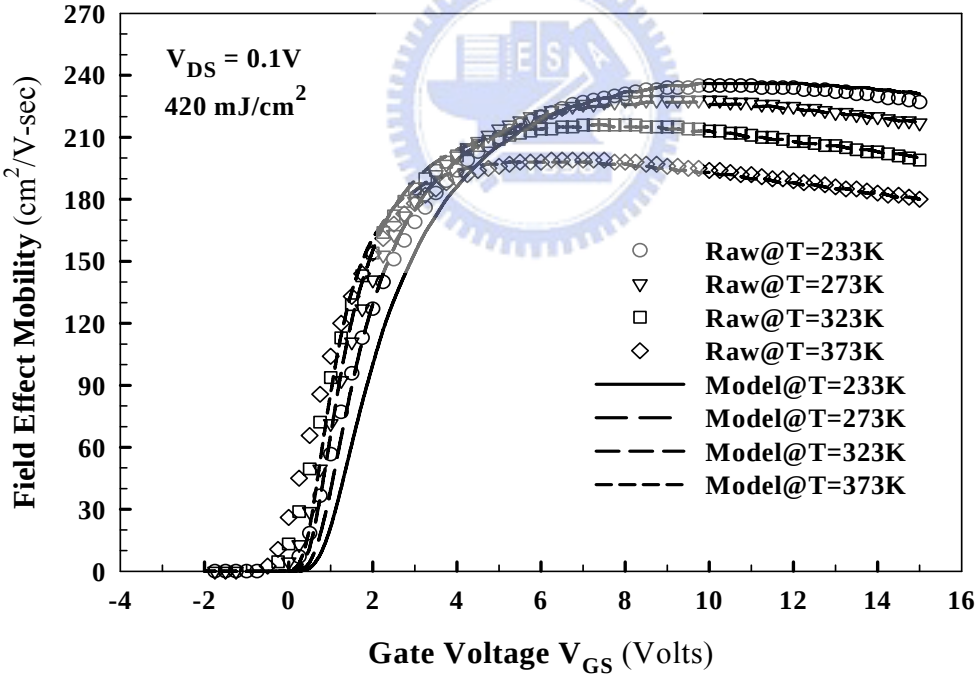


Fig.A-1 The illustration diagram of grain and grain boundary for the proposed mobility model

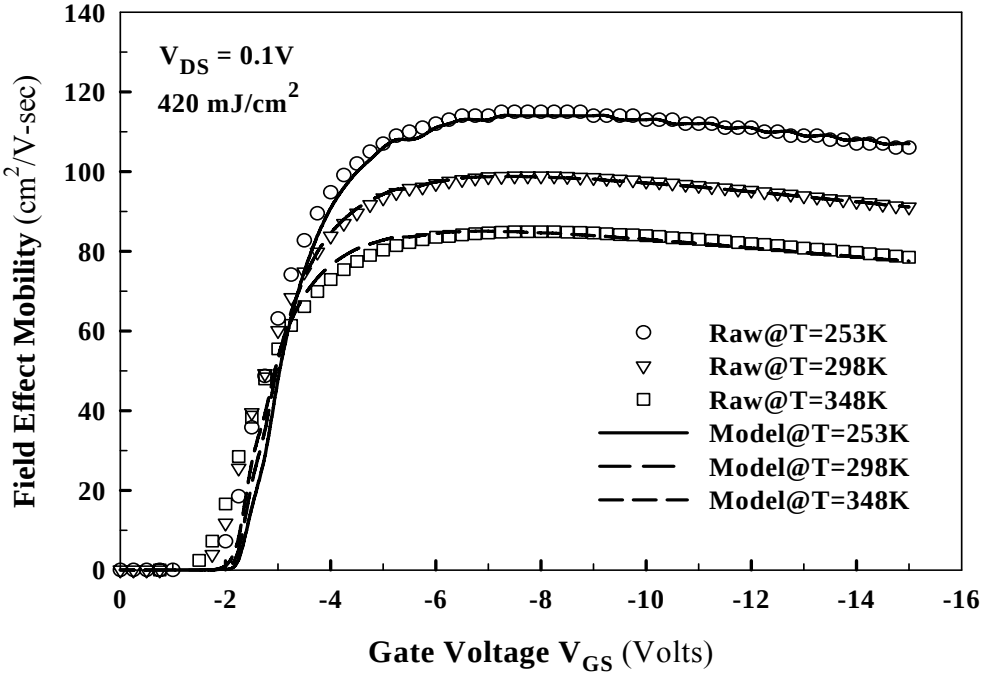


(a)

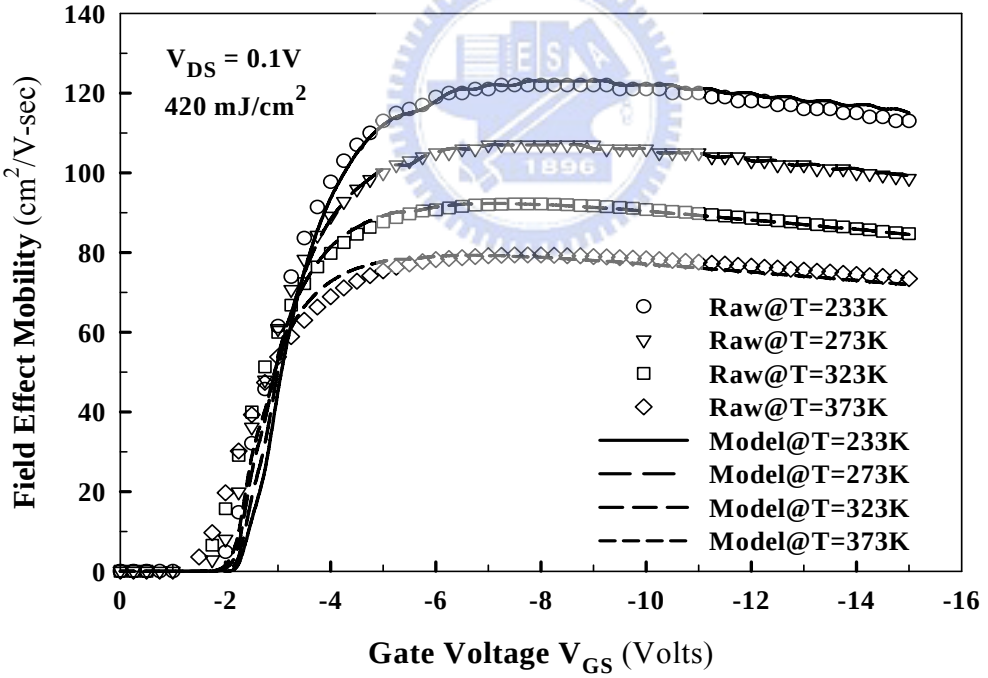


(b)

Fig.A-2 The comparison between the raw extracted mobility values and the modeling mobility values for the *W/L = 6μm / 30μm* N-type Poly-Si TFT with ***0.5μm LDD length*** at various temperatures: (a) T = 253K, 298K and 348K; (b) T = 233K, 273K, 323K and 373K

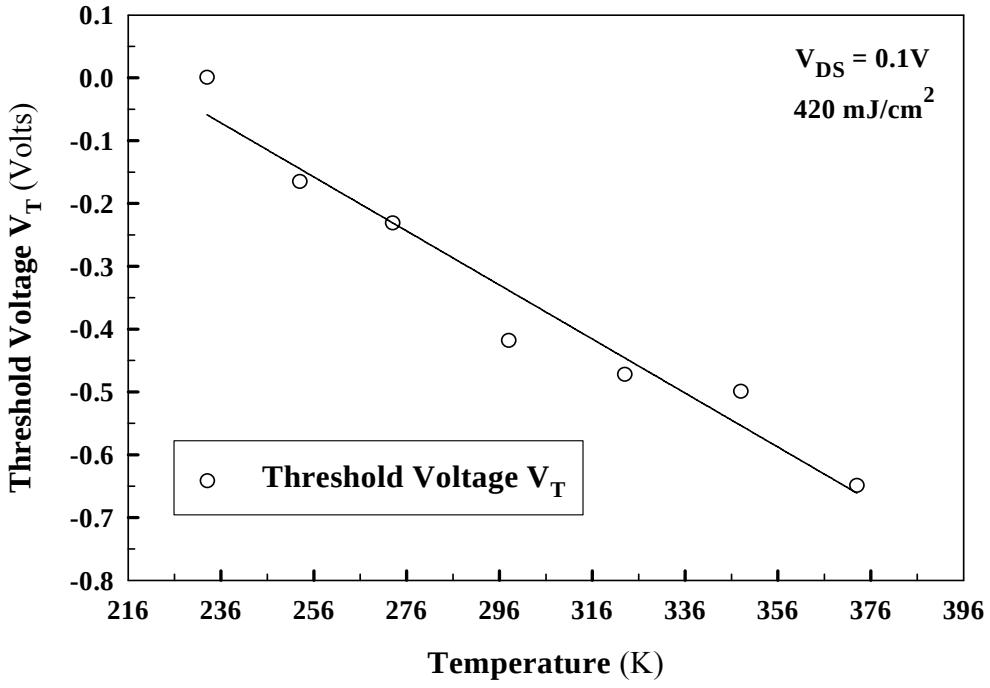


(a)

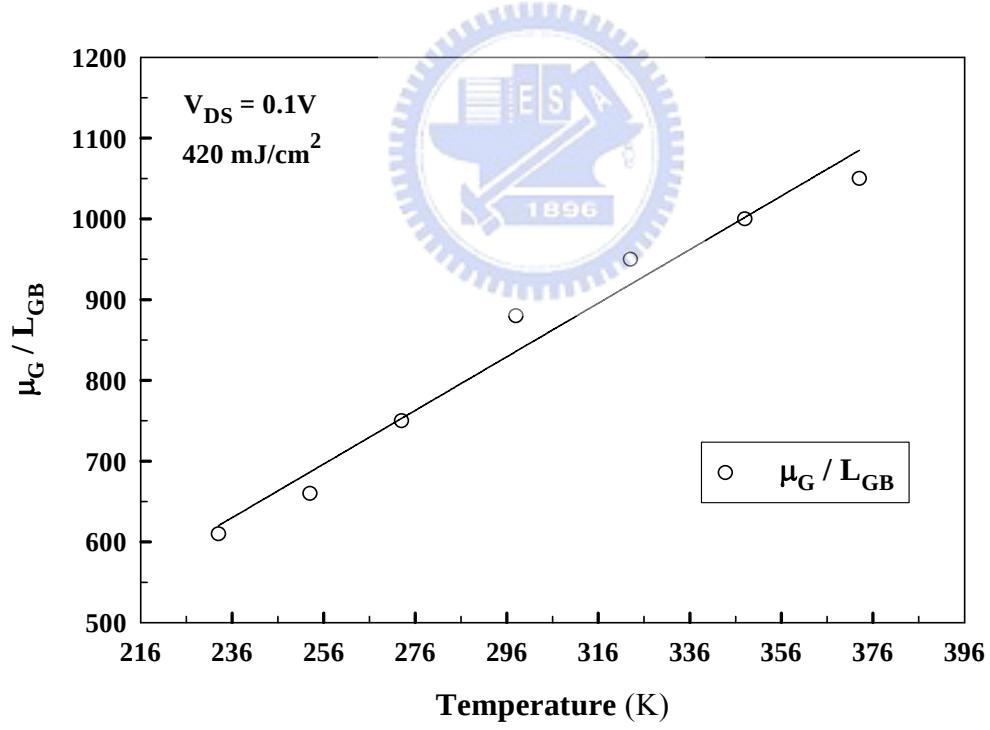


(b)

Fig.A-3 The comparison between the raw extracted mobility values and the modeling mobility values for the *W/L = 6μm / 30μm* P-type Poly-Si TFT ***without LDD structure*** at various temperatures: (a) T = 253K, 298K and 348K; (b) T = 233K, 273K, 323K and 373K

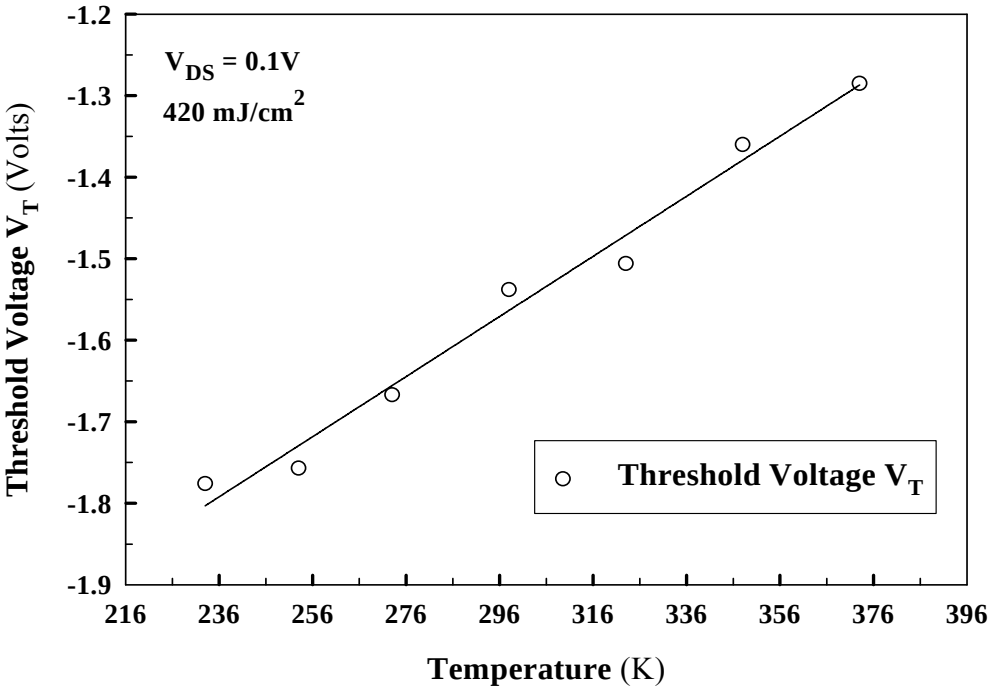


(a)

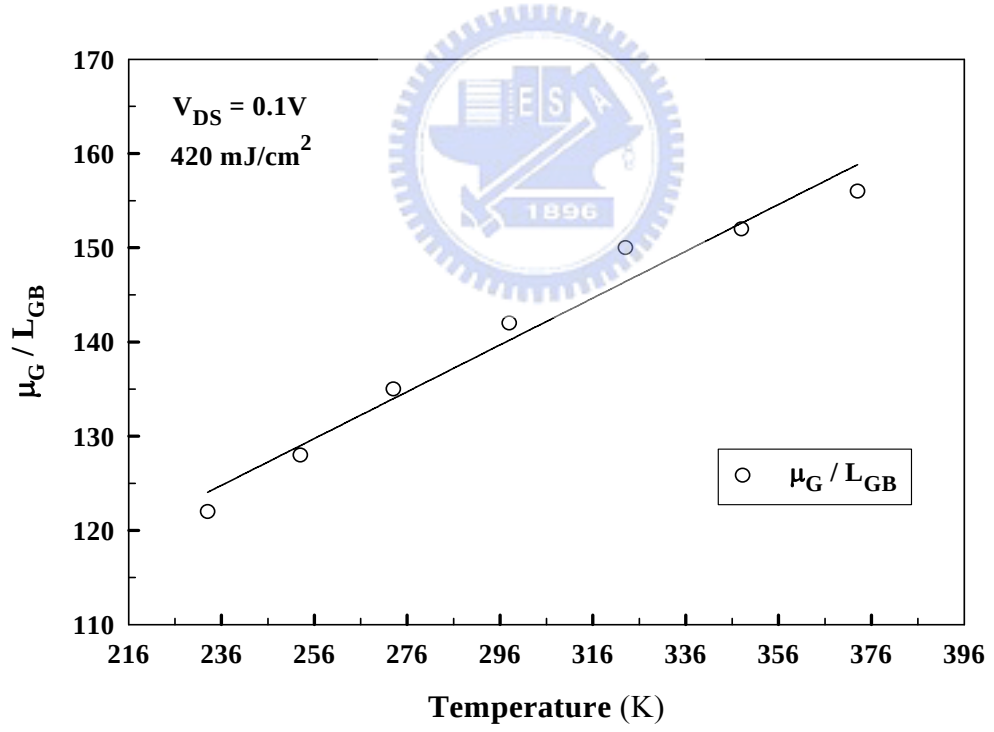


(b)

Fig.A-4 The temperature dependence of the model parameters including of the proposed mobility model (a) V_T and (b) μ_G / L_{GB} for the *W/L = 6μm / 30μm* N-type Poly-Si TFT with ***0.5μm LDD length***



(a)



(b)

Fig.A-5 The temperature dependence of the model parameters including of the proposed mobility model (a) V_T and (b) μ_G / L_{GB} for the *W/L = 6μm / 30μm* P-type Poly-Si TFT ***without LDD structure***

簡　　歷

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碩士論文題目：

具輕摻雜汲極結構之多晶矽薄膜電晶體之溫度效應研究

Study on Temperature Response of Poly-Si TFT’s with LDD Structure