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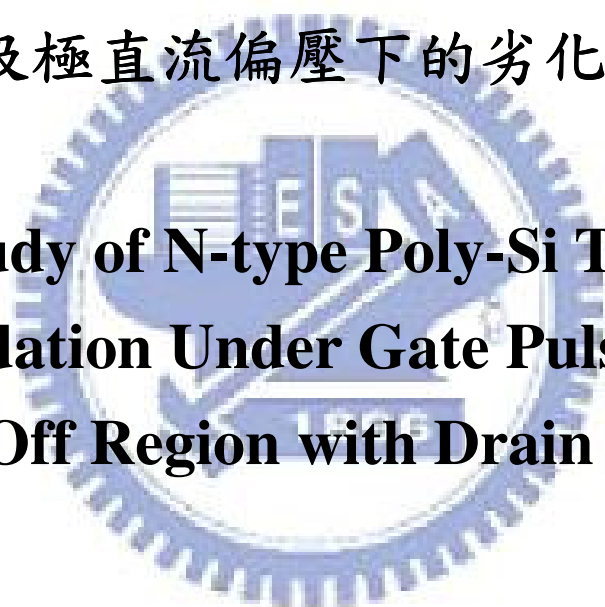## 顯示科技研究所

碩士論文

N 型複晶矽薄膜電晶體在閘極負電壓脈波汲極直流偏壓下的劣化研究

Study of N-type Poly-Si TFTs Degradation Under Gate Pulse Stress in Off Region with Drain Bias

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指導教授:戴亞翔 博士   Dr. Ya-Hsiang Tai

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顯示科技研究所碩士班

碩 士 論 文

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N型複晶矽薄膜電晶體在閘極負電壓脈波

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摘要

　　複晶矽薄膜電晶體(poly-Si TFT)因為其優異的元件特性，最近幾年在液晶顯示器(AMLCD)及有機發光二極體(AMOLED)顯示器應用中之所以會是眾所注目的焦點。相較非晶矽薄膜電晶體，複晶矽薄膜電晶體有較高電流趨動能力及較好的可靠度，因此在複晶矽薄膜電晶體顯示器裡，它可以被用來整合畫素電路及周邊驅動電路於同一片玻璃基板上，如此使面板結構簡單化且可以減少週邊半導體零組件的使用數量以及後段模組在組裝時的接點數目，進而提高工程可靠度，除此之外更可降低驅動 IC 成本，維持低耗電特性，提供高精細的畫質表現。所以，複晶矽薄膜電晶體被視為實現系統化面板(System on Panel)的關鍵技術。

　　然而不同於畫素的薄膜電晶體，在驅動電路上的薄膜電晶體會受到高頻的閘極脈波電壓所驅動。因此，薄膜晶體在交流訊號操作下的劣化機制必須要仔細的探討。

　　在這篇論文中，我們研究了低溫複晶矽薄膜電晶體在閘極負偏壓脈波且汲極直流偏壓的劣化，我們觀察到在汲極端會有一個嚴重的劣化，當閘極操作在負偏壓交流訊號且汲極直流偏壓下會量測到一個電流（在此我們稱為 pump

current）。汲極和源極有不同的電場效應，因此，在此電流經過時，也在這兩端產生不一樣的劣化行為。我們也觀察到元件的劣化和汲極端的電壓、閘極電壓上升時間、閘極電壓下降時間、閘極電壓的範圍很有關係。我們可以用量到的 pump current 來解釋不同操作情況下對元件的劣化行為。這個發現幫助我們在研究 LTPS 元件的可靠度上，了解並估計元件的劣化機制並在設計元件上面提供了一個參考。

Study of N-type Poly-Si TFTs Degradation Under Gate Pulse Stress in Off Region with Drain Bias

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Abstract

Polycrystalline silicon (poly-Si) thin film transistors (TFTs) have recently attracted much attention in the application on the integrated peripheral circuits of active matrix liquid crystal displays (AMLCDs) and active matrix organic light emitting diode (AMOLED) displays. The significant advantages over amorphous silicon (a-Si) TFTs are in the higher current driving capability and the better reliability. In poly-Si TFT-controlled displays, poly-Si TFTs are used to implement pixel circuits and driving circuits on a single glass substrate to reduce system cost and posses compact module. Therefore, the poly-Si TFT is the best candidate to realize system–on–panel (SOP).

However, unlike pixel TFTs, TFTs in driver circuits are subjected to high-frequency voltage pulses. Therefore, the degradation mechanism under dynamic operation should be understood in detail.

In this thesis, the device degradation of low-temperature polycrystalline thin film transistor under gate AC stress in off region with drain bias has been investigated. The effective drain current, pumped by the AC gate voltages in the off region, undergoes different electric field effects near the source and drain junction and therefore results

in different degradation behavior near these two regions. It is noticed that the degradation depends profoundly on the DC drain bias. It is also affected by the rising time Tr, falling time Tf, and the Vg range. This finding would be helpful in the understanding and evaluation of the device degradation mechanism and provide a guideline to design for reliability of poly-Si TFT circuit.

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