CHAPTER 1

Introduction

1.1 Overview of Low-Temperature Polycrystalline Silicon Thin Film Transistors (LTPS TFTs)

In recent years, low temperature polycrystalline silicon (LTPS) thin film transistors (TFTs) have attracted much attention because they have been used very successfully for active matrix displays, such as active matrix liquid crystal displays (AMLCDs) and active matrix organic light emitting displays (AMOLEDs). Expect large area displays, poly-Si TFTs have been applied into some memory device such dynamics random access memories (DRAMs), static random access memories (SRAMs), and have great potential for 3-dimention ICs' applications.

Compared to conventional a-Si TFTs, the field-effect-mobility of poly-Si TFTs is much higher. Higher field-effect-mobility means transistor can provide higher driving current. The higher driving currents can allow the pixel-switching element TFT's dimension shrinkage, resulting higher aperture ratio and lower parasitic gate-line capacitance for improved display performance. Besides, the superior mobility performance allows the integration of both the active matrix pixel switching elements and the peripheral driving circuitry on the same glass substrate, which brings the era of system-on-glass (SOG) that will include a memory, central processing unit (CPU), and display.

The process complexity can be greatly simplified and manufacturing cost can be substantially reduced. The ability of fabricating high-performance LTPS TFTs enables their use in a wide range of new applications. Therefore, there is great interest in improving the performance of LTPS TFTs.

In comparison with signal-crystalline silicon, poly-Si suffers from many grain boundary defects and intra-grain defects. The order of poly-Si grain size is about 0.1um. At present, when poly-Si TFTs are used in LCD applications, the minimum feature size is typically much larger than 10μm, and therefore a large number of grain boundaries are present in the channel. Electrons are scattered at the grain boundaries or trapped by the interface states, leading to lower mobility than in single crystal silicon. Much effort has been made to improve the performance of LTPS TFTs. Crystallization of a-Si thin films has been considered the most critical process for fabricating high-performance LTPS TFTs. Among various crystallization technologies, excimer laser crystallization has become the mainstream technology for mass production of flat panel displays (FPDs) because of high throughput, low temperature process compatible with glass substrate, and formation of high-quality poly-Si.

From the viewpoint of device technologies, various structural improvements, such as offset gate, lightly doped drain (LDD), multi-gate structure, and gate-overlapped LDD have been proposed. Most of these structures effectively reduce the electric field near the drain junction. Consequently, the anomalous leakage current and kink current of poly-Si TFTs can be effectively reduced accompanying with a promotion of reliability in poly-Si TFTs.

In summary, it is expected that the poly-Si TFTs will becomes increasingly important in future technology, especially when the 3-D circuit integration and SOP era is coming. There are lots of interesting and important topics that are worthy to be investigated.

1.2 Review of Studies on TFT under DC and AC Stress

In order to make LTPS TFTs suitable for advanced circuits, besides the improvement of performance of LTPS TFTs, the improvement of reliability is also significant. Therefore, reliability testing and understanding of reliability mechanisms become more and more necessary.

1.2.1 DC stress

In LTPS TFTs, several DC stress degradation mechanisms have been reported. In 2002 Satoshi Inoue paper brought up the stress voltage dependence of the V_{th} shift in poly-Si TFTs, as shown in figure 1-1 . Thus, in 2003 Satoshi Inoue's paper classified the degenerated phenomena. Figure 1-2 shows the effect of stress voltage on the I_{on} variation in TFTs. This result indicates two main degradation regions, the stress voltage of region A and region B. At first, hot carrier degradation is considered to originate from the damage of the metal-oxide-semiconductor (MOS) interface and of the channel poly-Si layer near the drain of TFTs. On the other hand, self-heating degradation is thought to originate in breaking of Si-H bonds and regeneration of dangling bonds in the MOS interface and channel poly-Si layers.

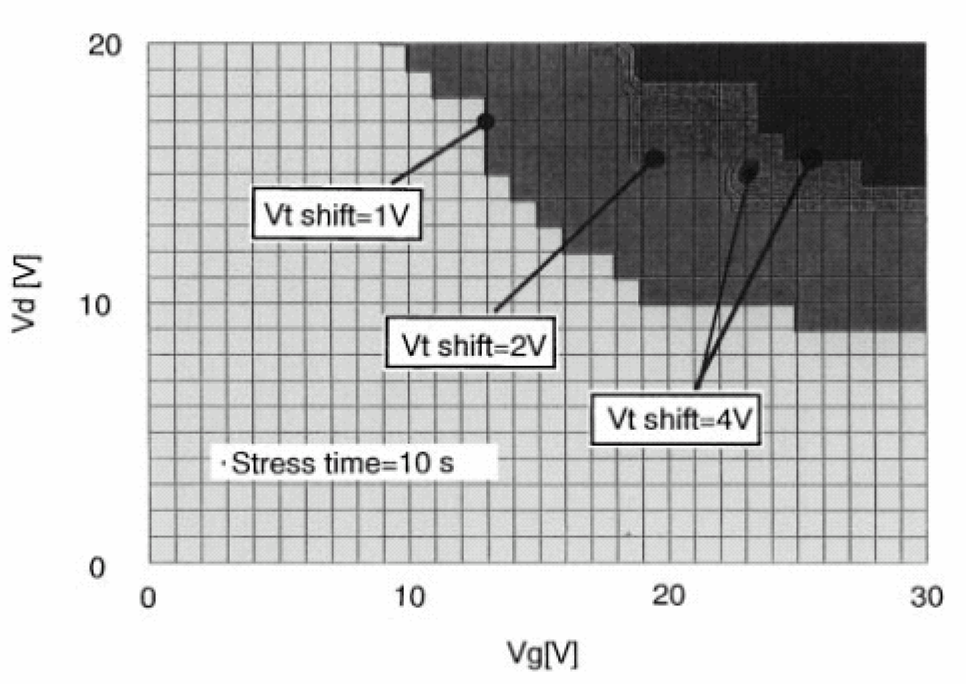

Figure 1-1 Stress voltage dependence of the V_T shift of the TFTs

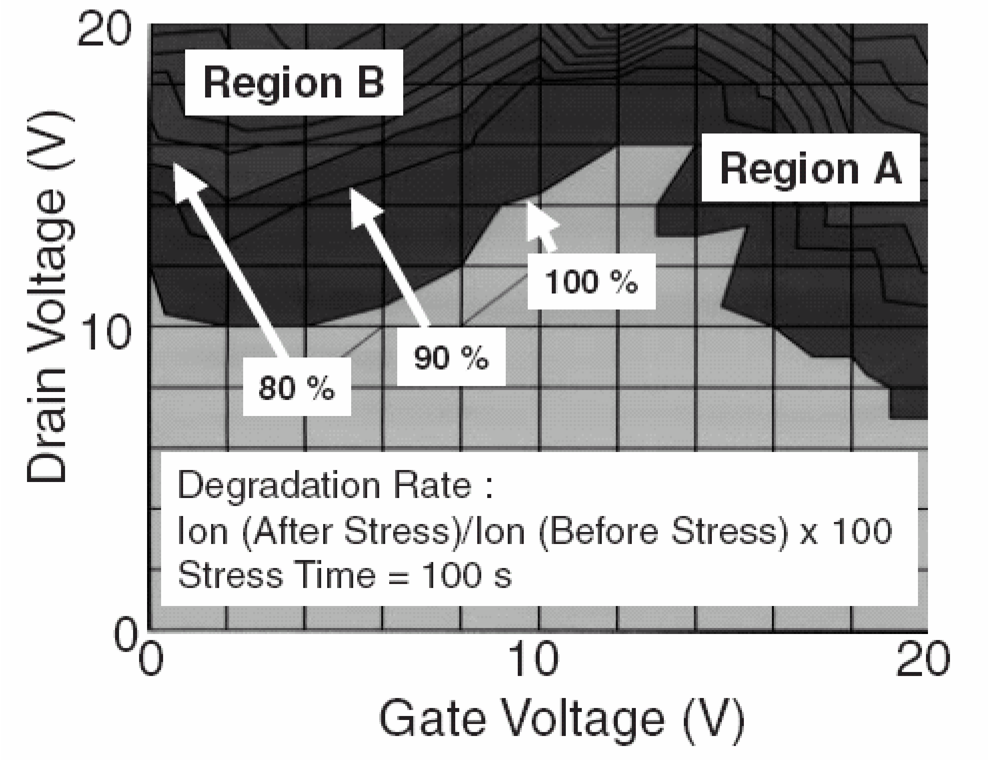

Figure 1-2 Dependence of stress voltage on the I_{on} variation in the TFTs

In region A, the dominant degradation mechanism is self-heating, both the drain and gate voltages are high, typically over 10V. In region B, the dominant degradation mechanism is hot carrier, only the stress drain voltage is high, typically over 10V, and gate voltage is low, typically from 2V to 5V.

1.2.2 AC stress

In previous reports, Toyota et al. proposed that mobile carriers are able to follow the transient variation of gate voltage while the electrons trapped in the midgap state aren’t. In addition, Uraoka et al. attributed the dominant AC degradation mechanism to hot electrons generated by trapped electrons exposed to the high electric field and gain energy from the electric field during ac stress. The mechanism was analyzed by using a picosecond emission microscope and a device simulation to examine the transient current experimentally and theoretically, respectively.

The earlier degradation model under ac stress is described as follow. When the gate voltage is high, the electrons gather to form a channel shown in Figure 1-3(a). When the gate voltage drops, the electrons in the channel move rapidly to the source and drain shown in Figure 1-3(b). Some of the trapped electrons are exposed to the high electric field and gain energy from the field. Hot electrons are generated at this moment and form electron traps shown in Figure 1-3(c), and a density of state (DOS) in tail edge of poly-Si is increased by the hot electrons.

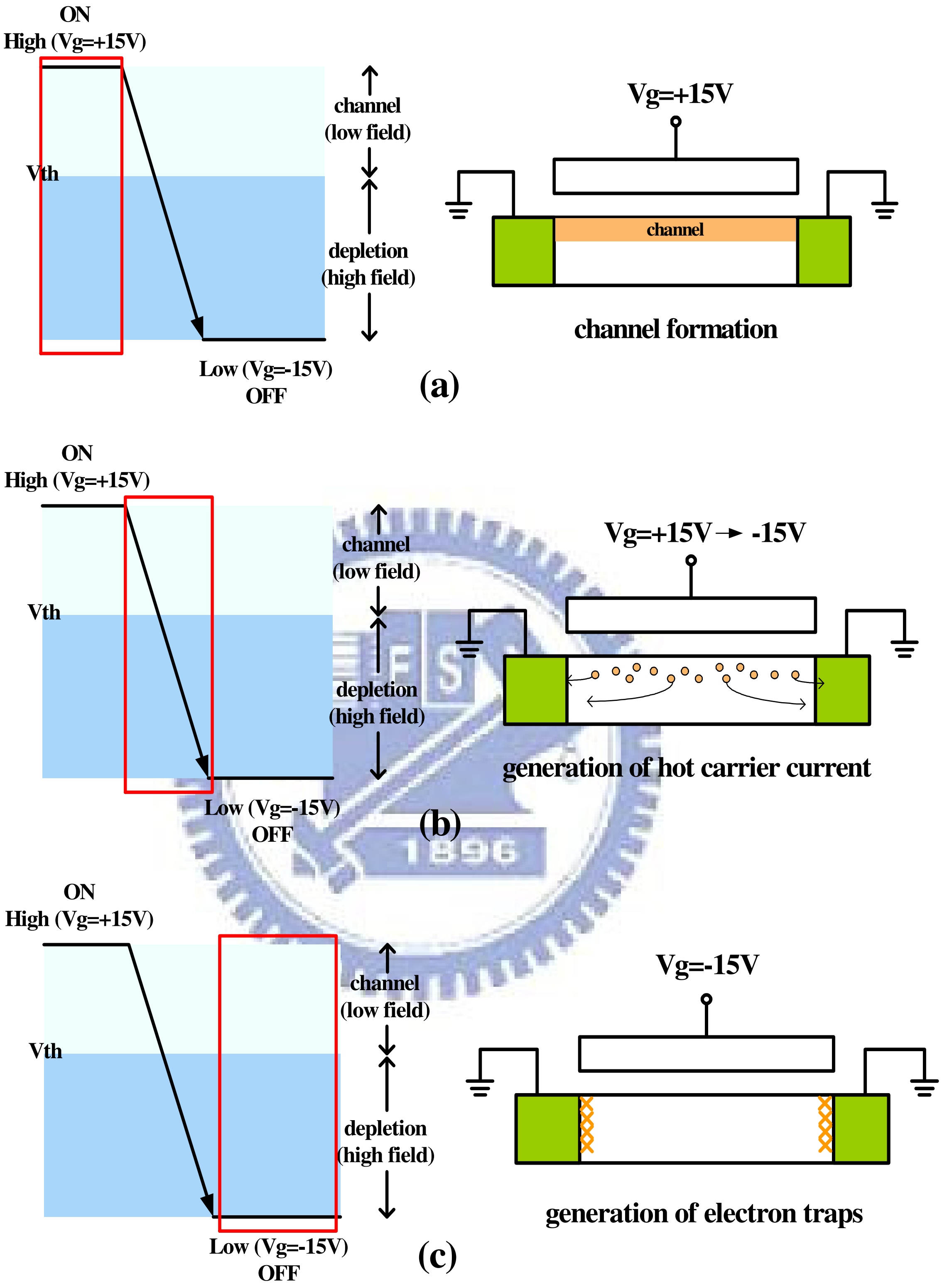

Figure 1-3 A schematic diagram for degradation model of the poly-Si TFT.

1.2.2(a) Repetition Number Dependence

The frequency dependence of the degradation of n-channel TFT is re-plotted as the repetition number dependence as shown in Figure 1-4. Disregarding the frequency, all lines follow the universal curve. The figure clearly indicates the relationship between the degradation and the repetition number and the independence of the frequency. In other words, the degradation arisen by the unchanging voltage can be ignored.

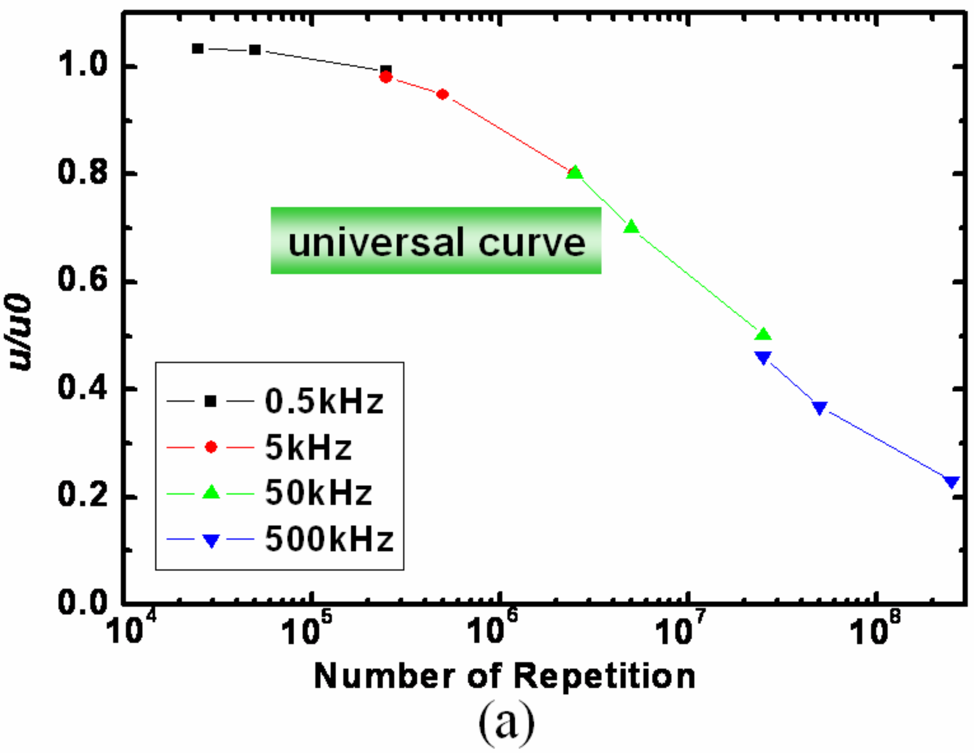

Figure 1-4 Dependence on the number of pulse repetitions of n-channel TFT

1.2.2(b) Gate Voltage Leveling Effect

The range of the gate pulse swing is separated into two parts according to the threshold voltage, as shown in Fig 1-5(a). In the ON region, the channel is formed, while in the OFF region, the channel was fully depleted. Figure 1-5(b) clearly indicate that the degradation of mobility strongly depends on the levels of the gate voltage. For the gate pulse swing in the ON region, the degradation is very small, however, that for the gate pulse swing fully in the OFF region become large. It is because the transient electrical field is high in the OFF region, but that is very low in the ON region. Carriers can gain energy from high electrical field and become hot carriers, and the traps are generated.

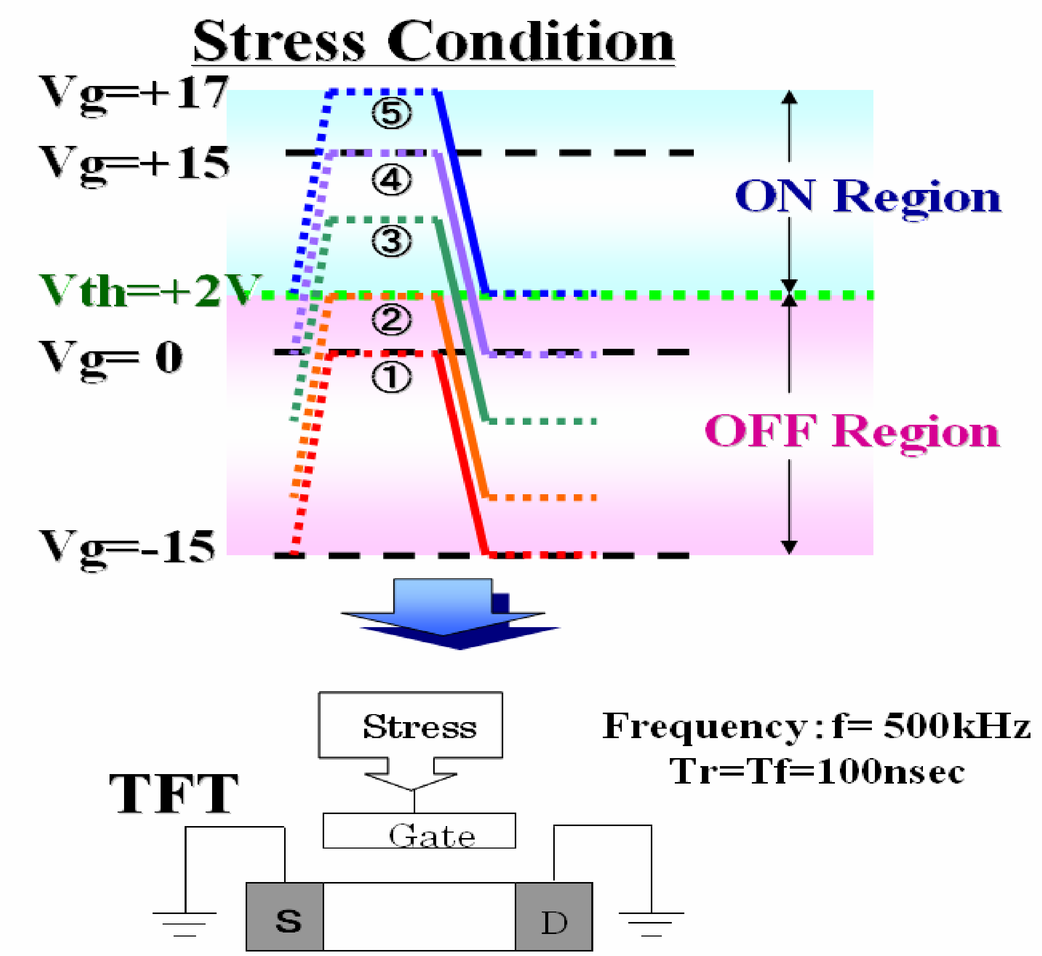

Figure 1-5(a) Swing region

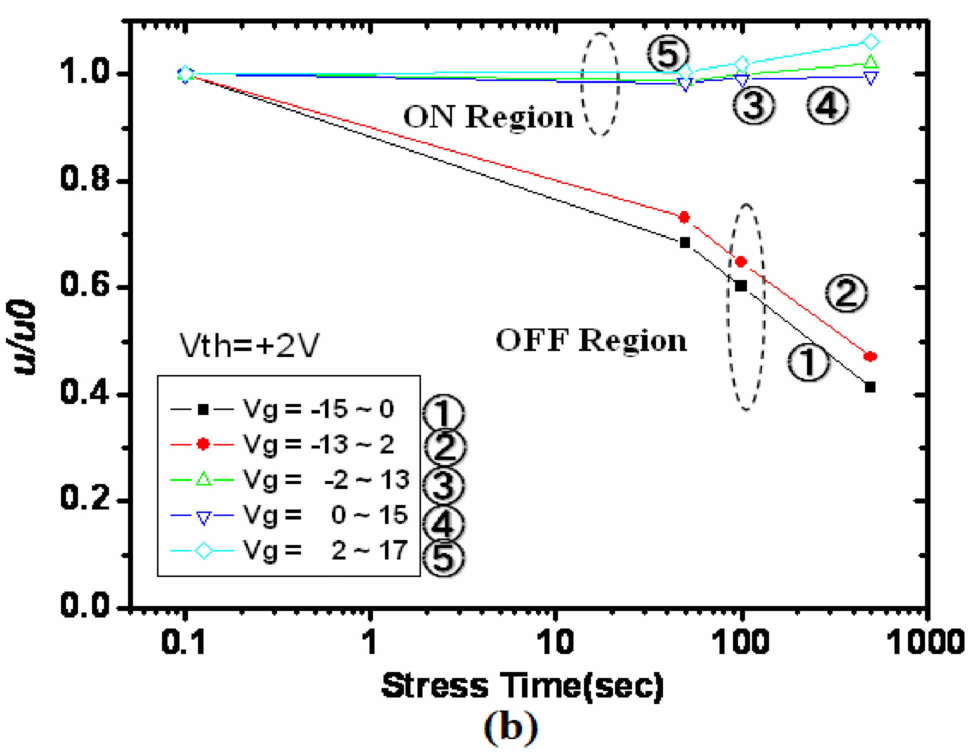

Figure 1-5(b) Dependence of degradation on swing region for n-channel TFT

1.2.2(c) Transient Time for Vg ON/OFF switch Dependence Effect (Vg=15V~-15V)

The transient time dependence for the degradation for Vg of ON/OFF switch was examined as shown in Figure 1-6. During the variation of rising time Tr from 100 ns to 700 ns with a fixed Tf of 100 ns, no significant change in μ/μ_0 was observed as shown in Figure 1-6(a). On the contrary, the degradation depended strongly on the falling time Tf as shown in Figure 1-6(b). The degradation is remarkably accelerated with the decrease of the falling time from 700 ns for 100 ns for a fixed Tr of 100 ns. In the case of changing rising time, the gate voltage varies from OFF region to ON region, and the mobile carriers are sited at so low electrical field that no device degradation is formed. But in the case of changing falling time, the gate voltage varies from ON region to OFF region, some carries remain in the channel and are subjected to the high electrical field becoming hot carries.

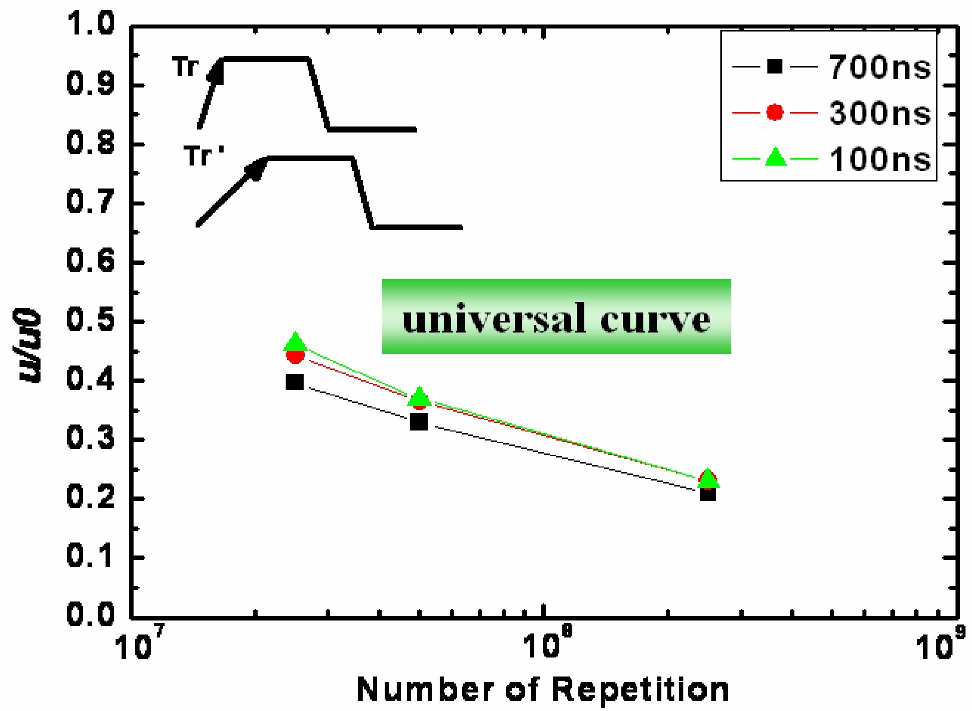

Figure 1-6(a) Rising time dependence of the degradation

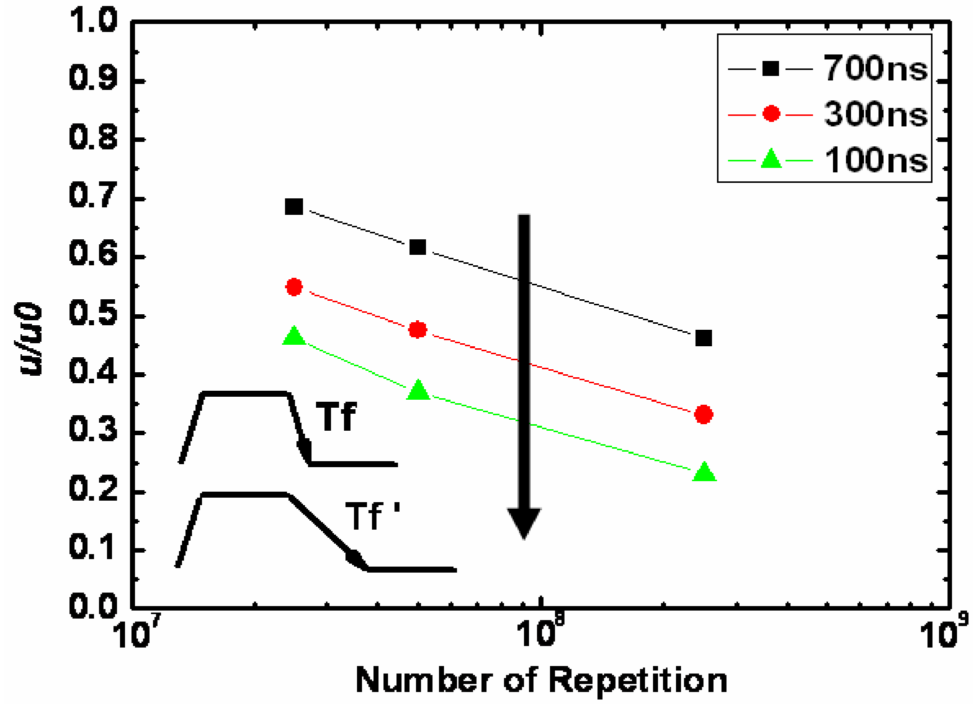

Figure 1-6(b) Falling time dependence of the degradation

1.2.2(d) Transient Time for Vg OFF region Dependence Effect (Vg=0V~-15V)

Reviewing section 1.2.2(c), we have known that degradation by pulse swing for the ON region was very small, however, that by pulse swing for the OFF region was large. In section 1.2.2(d), we already observe the transient time dependence for the degradation of n-channel TFTs under AC stress with Vg = -15 V to 15V. For this gate swing, it can be taken as steps of Vg = -15 V to 0V and Vg =0 V to 15V. For n-channel TFT, Vg = -15 V to 0V is OFF region, and Vg =0 V to 15V is ON region. Because no device degradation is formed for n-channel TFT under AC stress with Vg = 0 V to 15 V, we are only interested in the transient time dependence for the degradation of n-channel TFT at Vg = -15 V to 0V. For the gate voltage swings from -15 V to 0 V, it is firstly observed that the degradation is obviously dependent on both the rising time and falling time, as shown in Figure 1-7(a) and Figure 1-7(b).

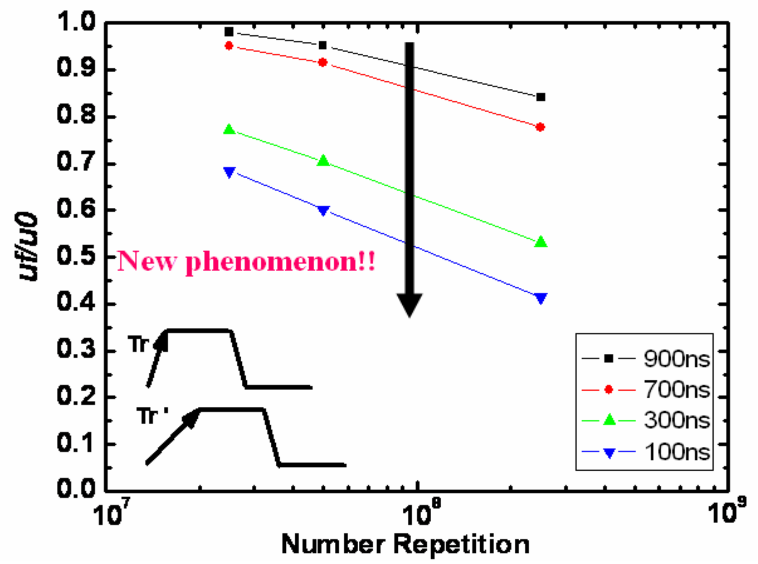

Figure 1-7(a) Degradation of μ/μ_0 in n-channel TFT under AC stress with Vg = -15 V to 0 V measured for various rising times Tr and for Tf = 100 ns

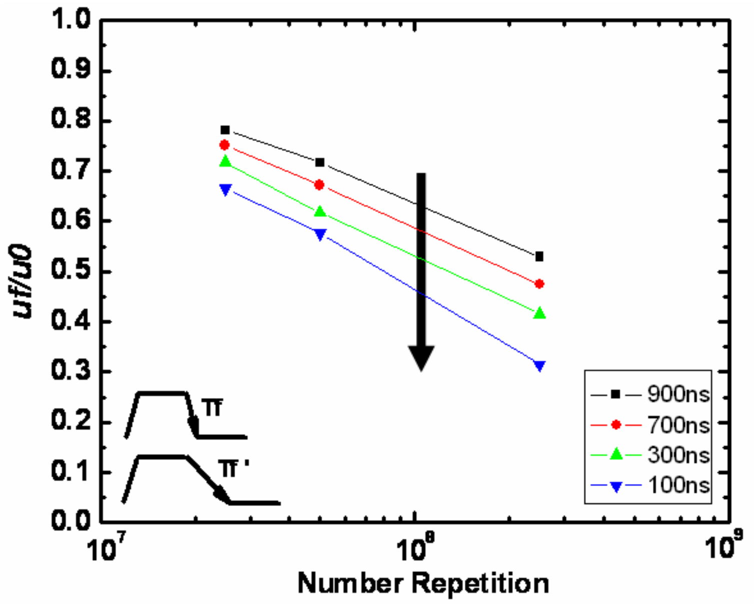

Figure 1-7(b) Degradation of μ/μ_0 in n-channel TFT under AC stress with Vg = -15 V to 0 V measured for various rising times Tf and for Tr = 100 ns

1.3 Motivation

The reliability mechanisms of LTPS TFTs under DC (direct current) bias stress and AC stress which source drain were ground have been widely discussed, as mentioned in section1.2. However, up to now, the reliability of LTPS TFTs under gate AC (alternating current) stress with drain bias has been paid much less attention, shown in Figure 1-8. In previous study regarding AC stress, the source and drain were ground to avoid the DC effect during dynamic stress. However, when the gate of the TFT is under dynamic operation, the drain-source voltage is usually present. For instance, the pixel TFTs driven by multi level gate scanning waveforms can be subject to the off-region AC stress at gate with DC drain bias, shown in Figure 1-9.

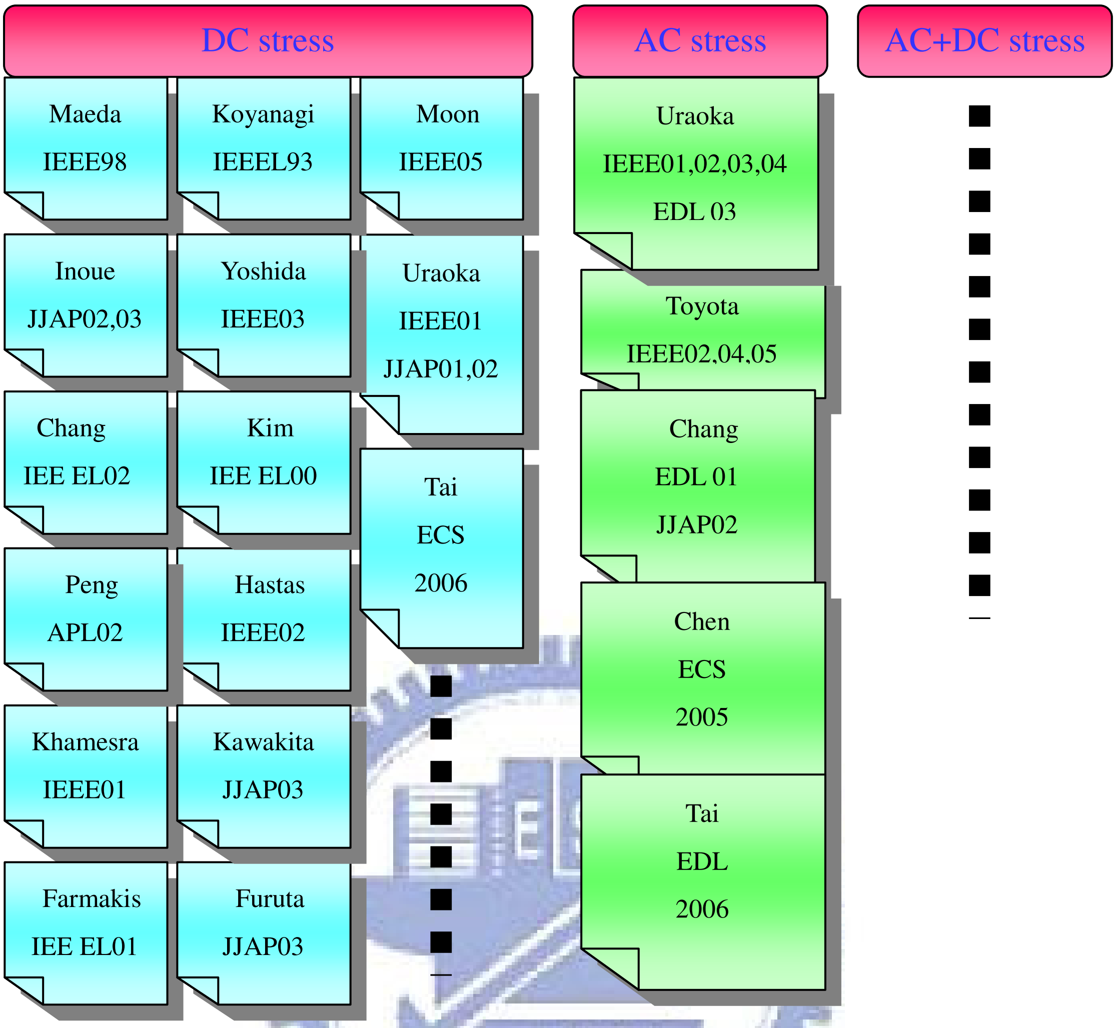

Figure 1-8 Previous researches of LTPS TFT reliability

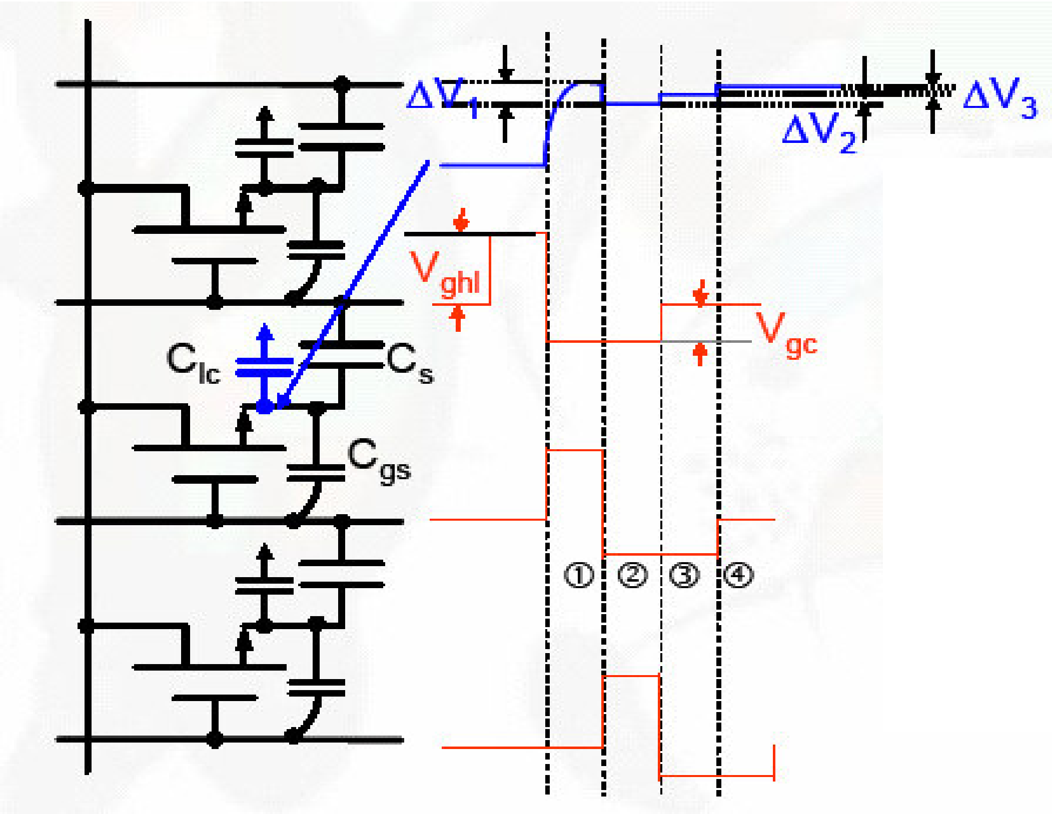

Figure 1-9 Three Level Gate Drive (gate off region AC stress with drain bias)

In this study, the degradation of n-channel LTPS TFTs under off-region AC stress with various drain bias , including swing range, and falling/rising times, was discussed to verify the degradation mechanism under gate AC stress with drain bias.

1.4 Thesis Organization

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Chapter2

Experiments

2.1 Procedures of Fabrication of LTPS TFTs

LTPS TFTs used in the experiment were the conventional top-gate structure and fabricated on the glass substrates. The cross-section views of n-channel LTPS TFTs are shown in Fig 2-1. The basic process flow is described as follows. Firstly, the buffer oxide and a-Si:H films were deposited on glass substrates by the PECVD system. Then, XeCl excimer laser was used to crystallize a-Si:H film followed with poly-Si active area definition. Subsequently, gate insulator was deposited by PECVD. The thickness of gate oxide is 650Å. Next, the metal gate formation and source/drain doping were performed. Dopant activation and hydrogenation was carried out after interlayer dielectric deposition. Finally, contact holes formation and metallization were performed to complete fabrication work. The lightly doped drain (LDD) structure was used in the n-channel TFTs to enhance hot carrier endurance. The width/length of the TFT was 20 μm/5 μm.

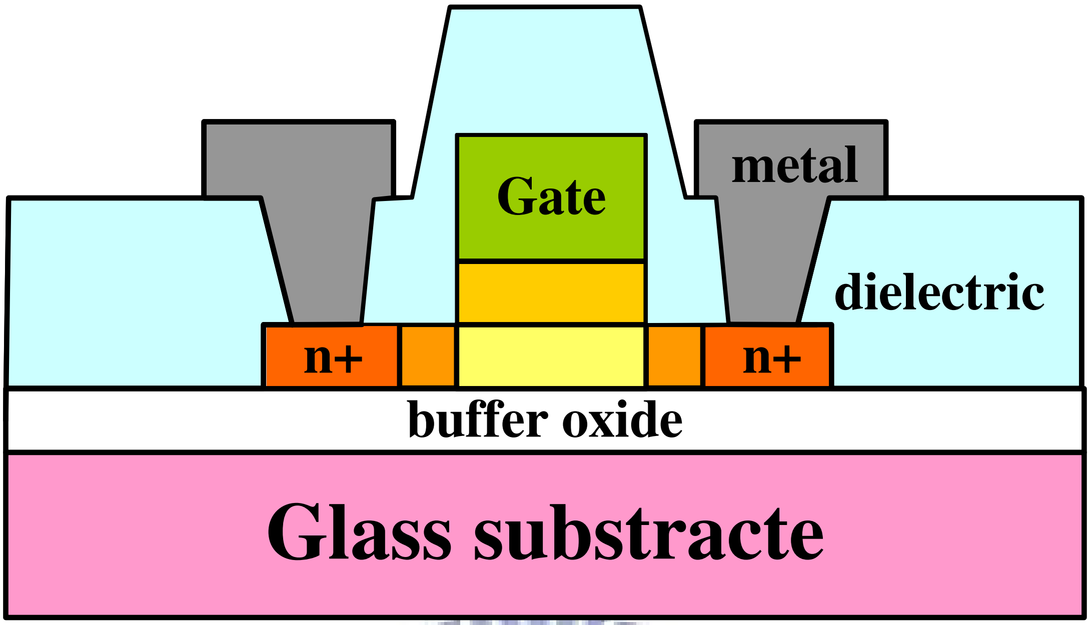


Figure 2-1 The cross-section views of n-channel LTPS TFTs with LDD structure

2.2 AC Stress Conditions

The basic parameters of AC signal consists of frequency (F), signal high level (Vgh), signal low level (Vgl), high-level time (T_vgh), low-level time (T_vgl), rising time (Tr), and falling time (Tf). Fig 2-2 shows the waveform of the AC signal. In AC signal, the definition of individual parameter is given as follow:

$$T = Tr + T\_vgh + Tf + T\_vgl \quad (2.1)$$

$$F = 1/T \quad (2.2)$$

$$\text{Duty ratio} = (Tr + T\_vgh)/T \quad (2.3)$$

where T is the signal period.

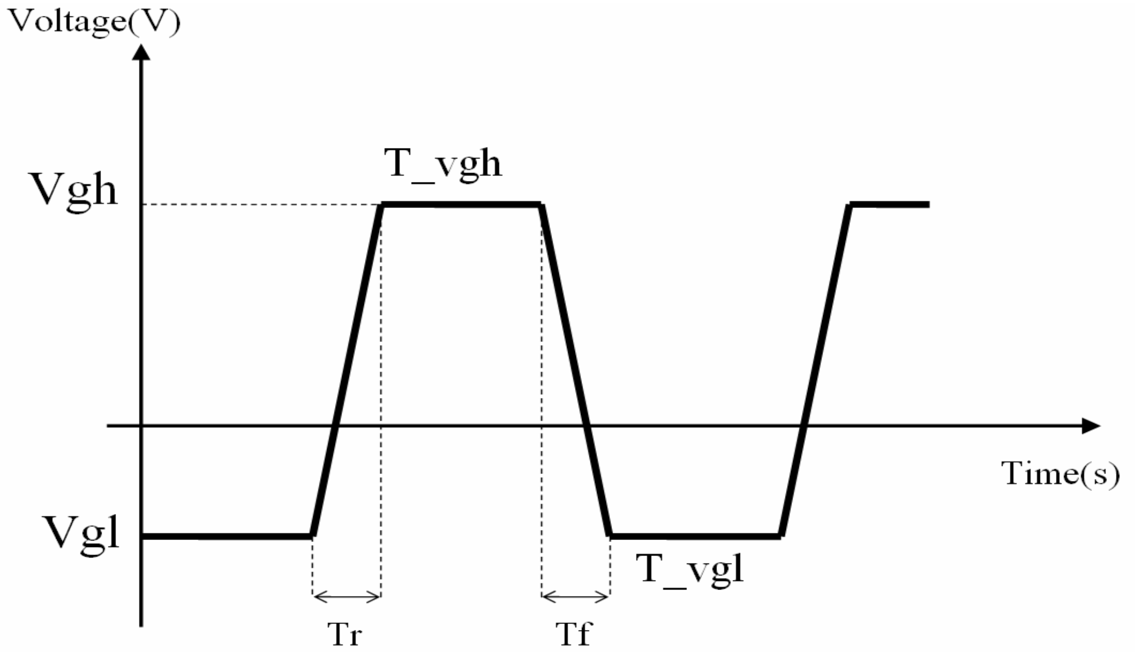


Figure 2-2 Waveform and definition of the AC signal

Under AC stress, pulse voltage is applied to the gate electrode with drain DC bias while source is grounded, as shown in Fig 2-3. The standard stress condition in the experiment includes the gate voltage swing of -15 V to 0 V, V_D of 20V, F of 500k Hz, Tr and Tf of both 100ns, and duty ratio of 50%. These parameters are adjusted to perform then various stress conditions.

Firstly, V_D is changed from 0V to 20V, to study the effect of drain voltage under gate AC stress, as shown in Figure2-3. Secondly, we change Tr and Tf from 100ns to 700ns to understand the transient time dependence, as shown in Figure2-4 and Figure2-5. Thirdly, we change Vgl from -5V to -20V to investigate the effect of gate voltage range, as shown in Figure2-6. The stress conditions in this thesis are summarized in Table 2-1.

Experiment	Drain voltage	Vg pulse	Rising time (ns)	Falling time (ns)	Figure
VD effect	0V,5V,10V,15V,20	Vg=-15V~0V	100	100	Fig.2-3
Rising time	20V	Vg=-5,-10V,-15V, -20V~0V	100300700	100	Fig. 2-4
Falling time	20V	Vg=-15V~0V	700	100,300,700	Fig. 2-5
Vg range effect	20V	Vg=-5,-10V,-15V, -20V~0V	100	100	Fig. 2-6

Table 2-1 four stress conditions summary (Frequency=500k Hz, stress 60s)

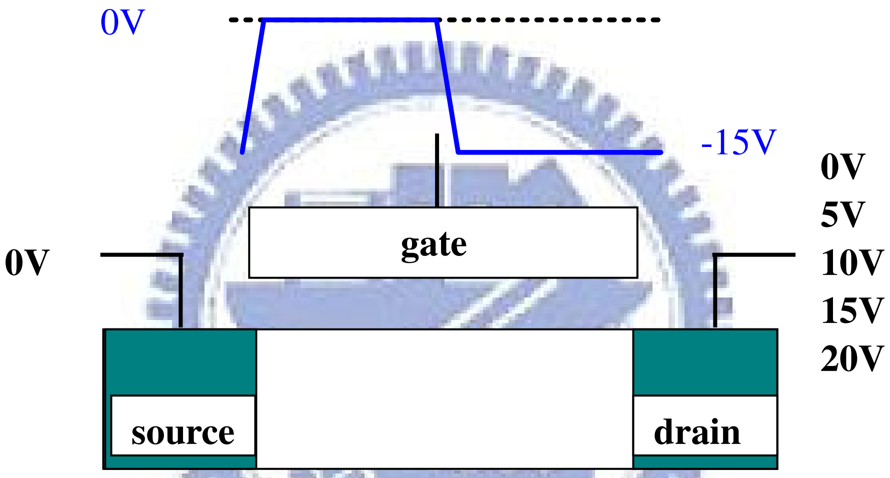


Figure 2-3 Illustration of the TFT under AC stress with various drain bias while source is grounded

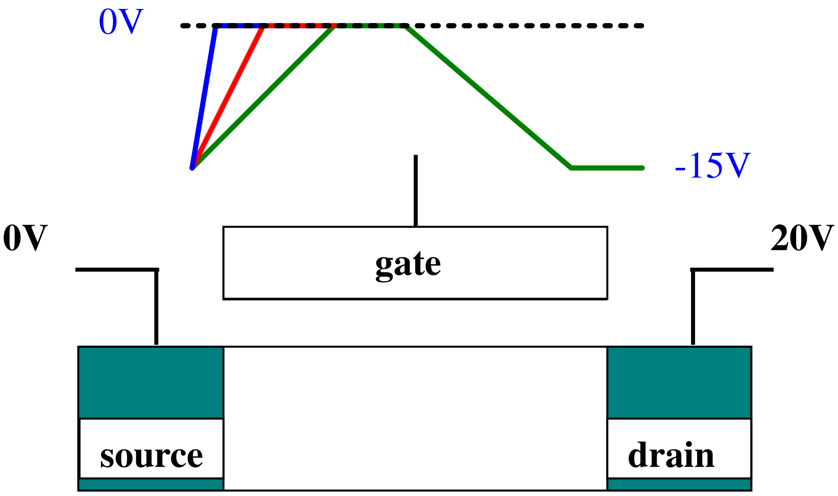


Figure 2-4 TFT under gate AC stress with various rising time with drain bias 20V

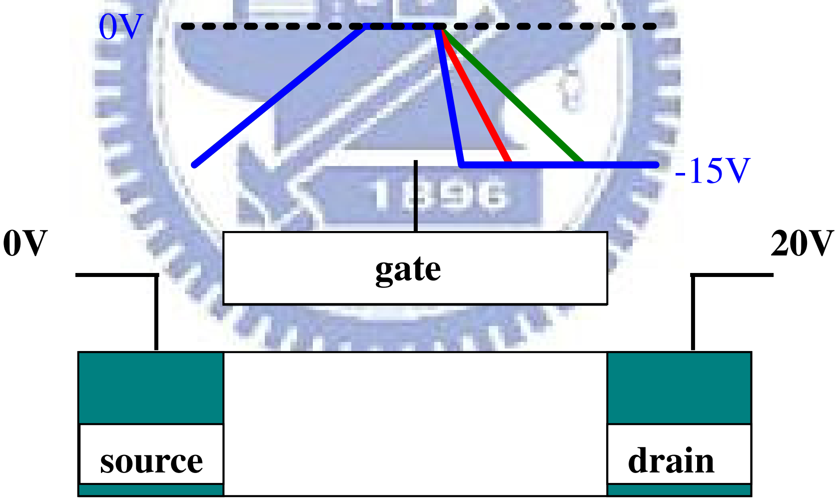


Figure 2-5 TFT under gate AC stress with various falling time with drain bias 20V

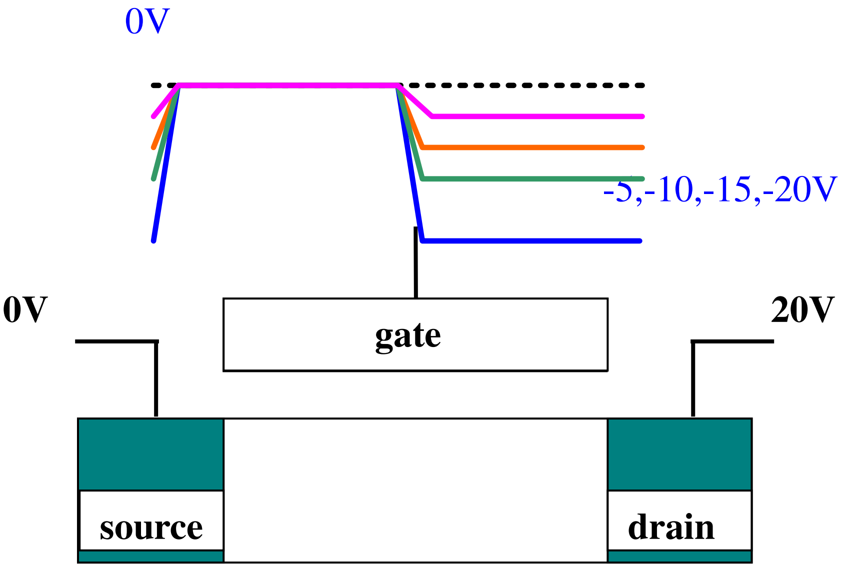


Figure 2-6 TFT under various Vg range stress with drain bias

2.3 Extraction of Device Electrical Parameters

The methods of the typical electrical parameter extraction will be introduced in the following, including threshold voltage, field-effect mobility, subthreshold swing, on-current, and leakage current.

2.3.1 Determination of the Threshold Voltage (V_{th})

The method to determine the threshold voltage in this thesis is the constant drain current method, which is adopted in most studies of TFTs. The threshold voltage is defined as the gate voltage which yields a normalized drain current (i.e. the threshold current). Typically, the threshold current is specified as 10nA at $|V_{ds}|=0.1V$ in most papers to extract the threshold voltage.

2.3.2 Determination of the Field Effect Mobility (μFE)

The field effect mobility (μ_{EF}) is determined from the transconductance gm at low drain bias. The transfer characteristics of poly-Si TFTs can be derived by a gradual channel approximation. The relation can be expressed as

$$I_d = \mu_{FE} C_{ox} \frac{W}{L}[(V_{gs} - V_{th})V_d - \frac{1}{2}V_d{}^2] \qquad (2.4)$$

Where

C*ox* is the gate oxide capacitance per unit area,

W is channel width,

L is channel length, and

V*th* is the threshold voltage.

The transconductance is defined as

$$g_m = \left.\frac{\partial Id}{\partial Vg}\right|_{Vd=const.} = \mu_{FE}\frac{W}{L}C_{ox}V_d \qquad (2.5)$$

Therefore, the field effect mobility can be obtained by

$$\mu_{FE} = \frac{L}{C_{ox}WV_d}g_m \qquad (2.6)$$

2.3.3 Determination of the Subthreshold Swing (SS)

Subthreshold swing is a measure of the efficacy of the gate potential to modulate drain current. It is defined as the amount of gate voltage to increase and/or decrease drain current by one order of magnitude. It can be shown that the expression for *SS* is given by

$$SS = \frac{\partial V_g}{\partial(\log I_d)} \qquad (2.7)$$

Clearly, the smaller value of *SS*, the better transistor is as a switch. A small value of *SS* means that a small change in the input bias can modulate the output current considerably.

2.3.4 Determination of the On-Current (Ion) and

Off-Current (Ioff)

Ion is an indicator of driving ability. A high Ion enable TFTs to provide sufficiently high drive current, which results in shorter pixel capacitance charging time and high aperture ratio. A low Ioff enable TFTs to hold the current during off-stage, which results in high aperture ratio. In this thesis, the on current is specified by the maximum drain current at $|V_{ds}|=10V$ and $|V_{gs}|=20V$, while the off current is specified by the minimum drain current at $|V_{ds}|=10V$.

Chapter3

AC Stress with Drain Bias Effect

3.1 Degradation of I-V Behavior

3.1.1 Effect of drain bias

Figure 3-1(a) shows the I_D-V_G transfer curves of the n-type poly-Si TFT before and after 60s of dynamic gate stresses with different drain voltage $V_{D.}$ The higher threshold voltage, lower mobility and higher sub-threshold swing are observed after stress. They seriously depend on the supplied drain bias. Comparing to the initial mobility of 70 cm^2/V-sec, after AC stress with drain bias of 20 V, the mobility decreases to only 5 cm^2/V-sec, as shown in Figure 3-1(b). The initial sub-threshold swing is 0.25 V/dec. After the AC stress it degrades to 1.0 V/dec, as shown in Figure 3-1(c).

In previous studies, poly-Si TFTs degradation under gate AC stress with source and drain grounded are usually characterized by a decrease of on current. It is attributed to the generation of traps at tail states in poly-Si grains. The sub-threshold swing (S.S) and threshold voltage are almost not changed. On the other hand, the degradation under DC stress usually exhibits a decrease of the sub-threshold slope mainly due to the generation of traps at deep states in poly-Si grains, as well as a threshold voltage shift caused by charge trapping in the gate oxide and at the interface states.

For the case of AC stress with drain bias, the mobility, sub-threshold swing and threshold voltage are all degraded. For other words, gate AC stress with drain bias can possibly generate both deep state and tail state in associations with degradation in sub-threshold swing and on current respectively.

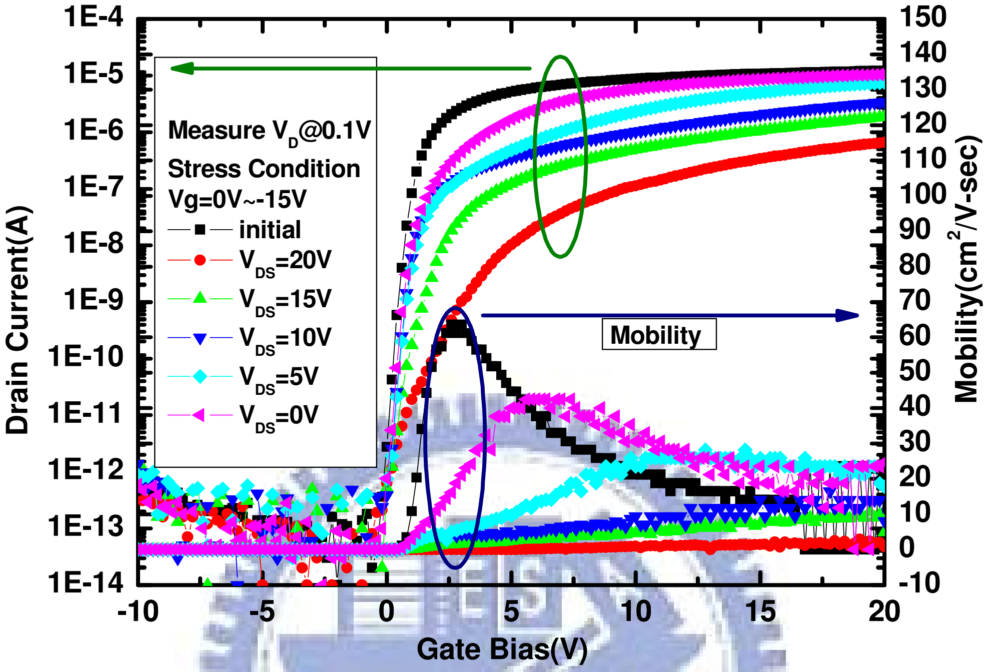


Figure 3-1(a) Id-Vg curves before and after dynamic gate stress (Frequency=500 kHz, stress 60 s) with different drain bias voltages

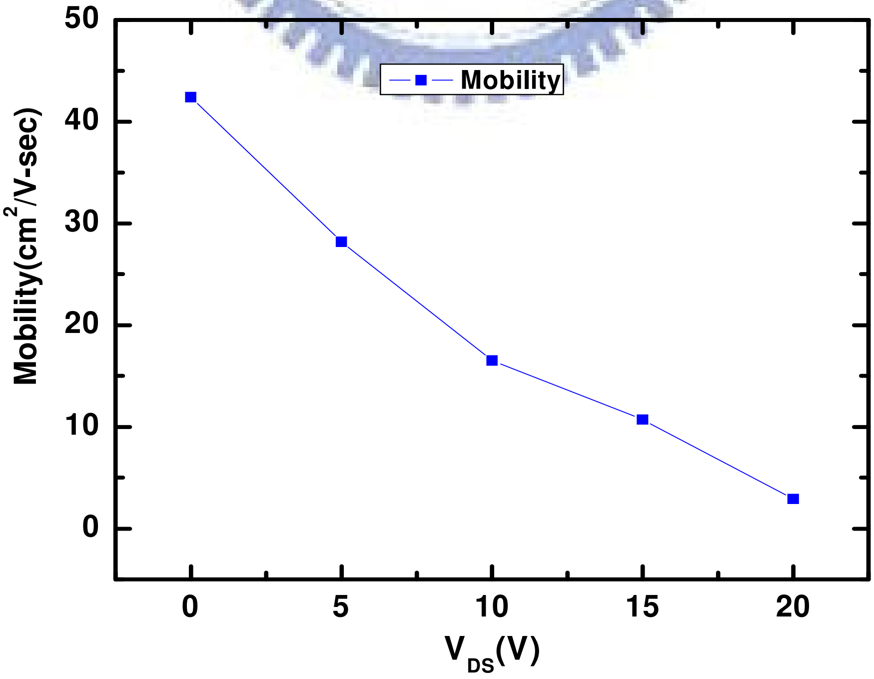


Figure 3-1(b) Dependence of the mobility on V_{DS} with gate AC stress in off region

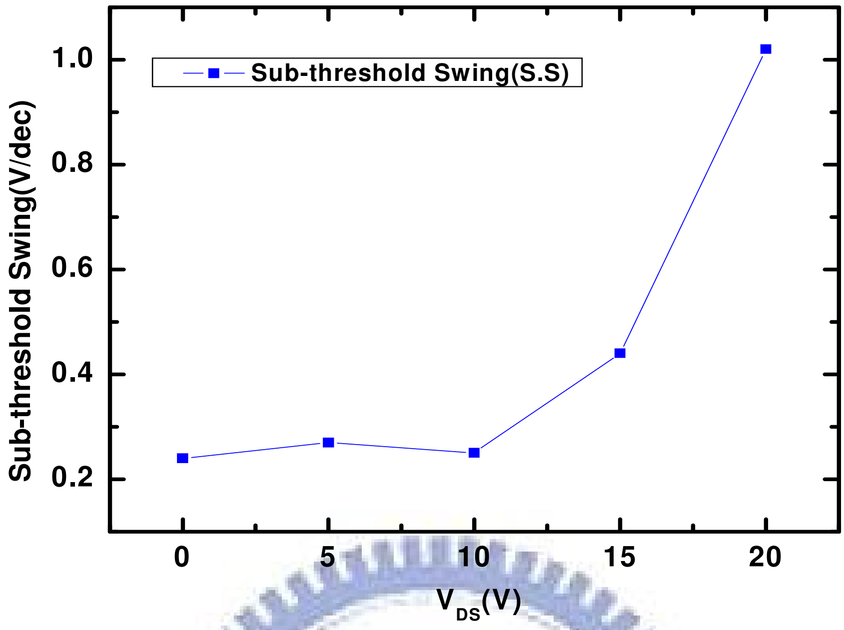


Figure 3-1(c) Dependence of the S.S on V_{DS} with gate AC stress in off region

3.1.2 Damaged region

To clarify the location of damaged regions in the TFT after gate AC stress with drain bias, electrical analysis using higher drain voltage was performed.

Figure 3-2(a) and (b) respectively show the forward and reverse I_D-V_G relations with the drain bias of 10 V after 60 seconds stress along with their corresponding measurement configurations. The forward ON-current saturation region (V_D = 10V) is much better than that measured with source/drain reverse.

For the forward measurement in the saturation region ($V_{DS} > V_{GS}$-V_T), the pinch off region appears near the drain and the depletion region increasingly expands toward to the source with increasing drain voltage. Carriers are swept into the drain by the electrical field when they enter the pinch off region. Note that the carriers moving into pinch-off region are no longer confined to the inversion layer near the surface, but begin to move away the surface into the bulk. Carriers tend to repel the high-resistivity region at the oxide/poly-Si interface near the drain, even if the region is damaged.

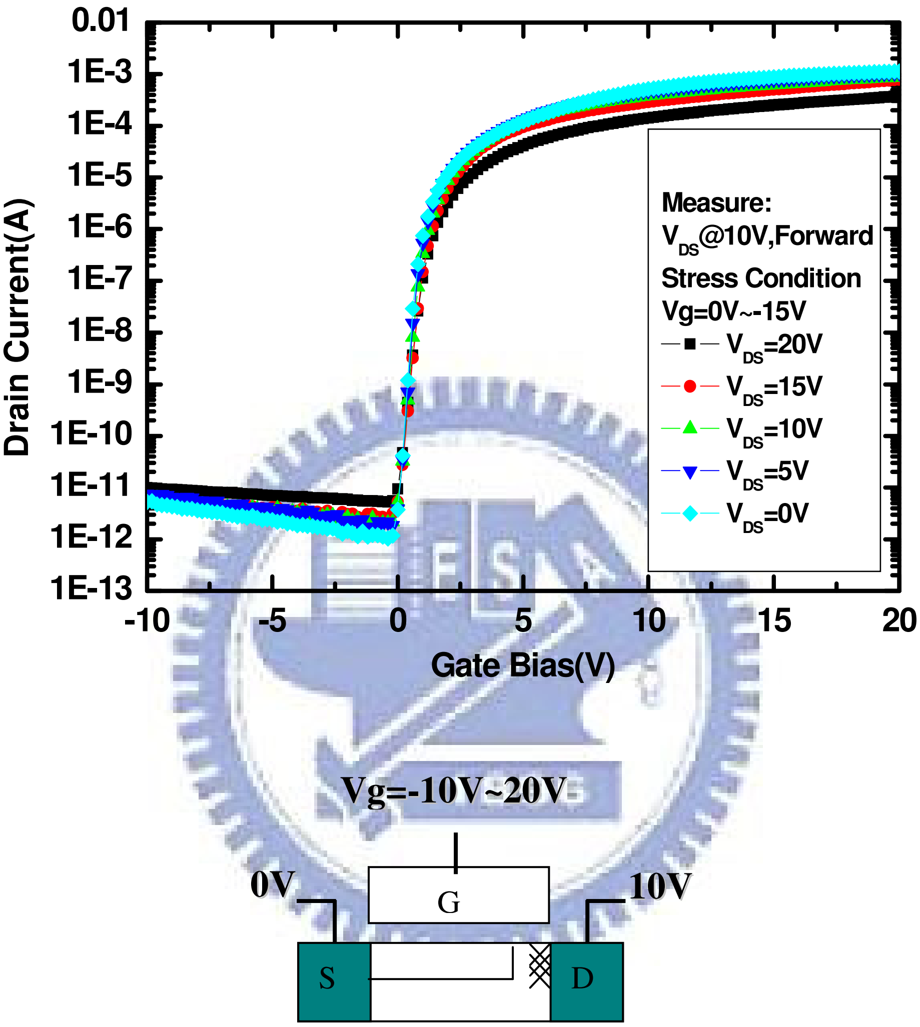


Figure 3-2 (a) Forward saturation current (measure V_{DS} =10V)

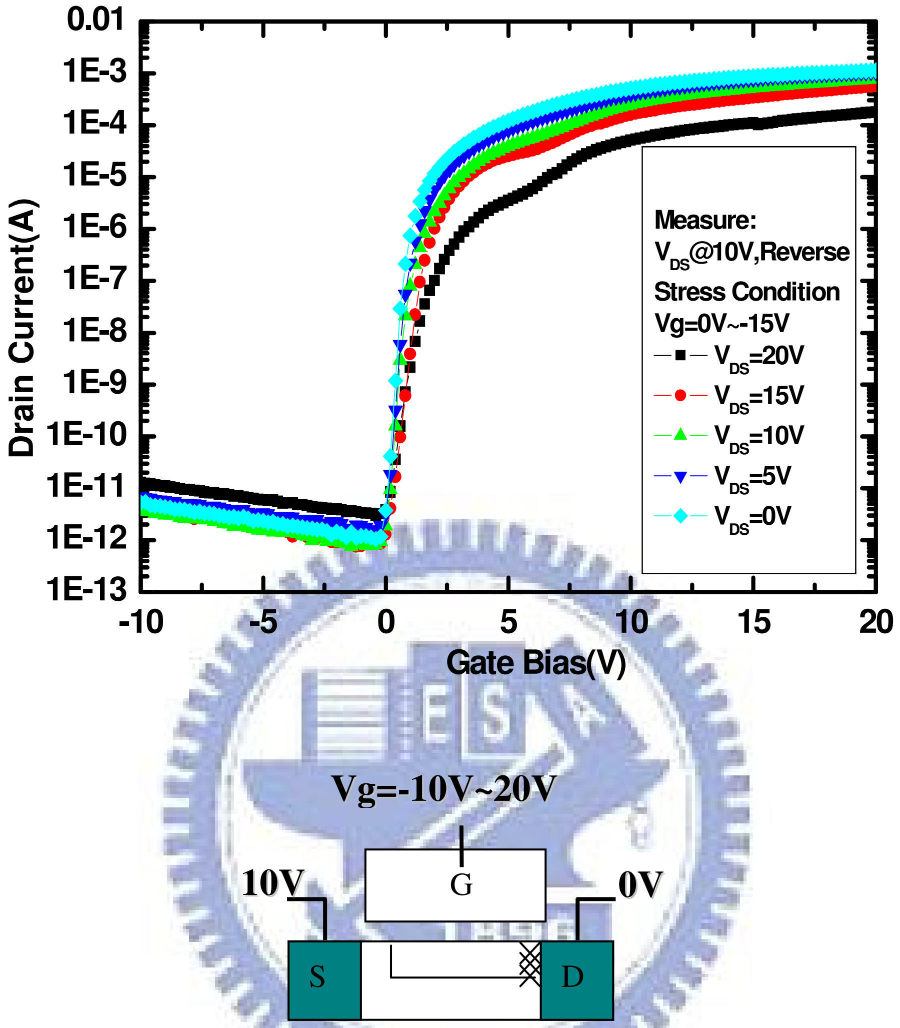


Figure 3-2 (b) Reverse saturation current (measure V_{DS} =10V)

On the other hand, when device measured reversely the carriers must flow through the damaged region with high resistivity near the drain. It is observe that the forward current is much better than the reverse current. Thus,we can verify the damage region is near the drain.

3.2 Degradation of C-V Behaviors

3.2.1 Slicing circuit model

The C-V measurements were further employed to investigate the degradation near the source and drain regions of TFTs. Gate-source capacitance (C_{GS}) and gate-drain capacitance (C_{GD}) are both measured. Before the measurement results are discussed, the slicing circuit model is introduced to analysis the degradation of C-V behaviors. Figure 3.3 shows the circuit model considering the channel resistances and gate insulator capacitances to be the distributing insulator capacitance (C_{in}), channel resistance (R_{ch}), junction capacitance (C_j), and contact resistance (R_C). In this model, the C-V behavior can be correlated to the I-V behavior by the gate-voltage dependent Rch.

As the gate voltage is much higher than the V_{th}, the channel is turned on and the channel resistance will become very small, as illustrated in Figure 3-4(a). The total impedance would be dominated by the insulator capacitance. Hence the major part of the signal current to be measured will flow through the channel resistance and thus the measured capacitance would be the summation of C_{in}. On the other hand, as the gate voltage is far below the V_{th}, the channel resistances R_{ch} is so high that they will block out the signal deep in the channel, as shown in Figure 3-4(b). Therefore, the measured C-V behavior in this region may actually represents the capacitance near the edges of the channel. However, for the transient region, neither the resistance nor the capacitance would dominate the impedance. Hence both the capacitance and the resistance will make effect.

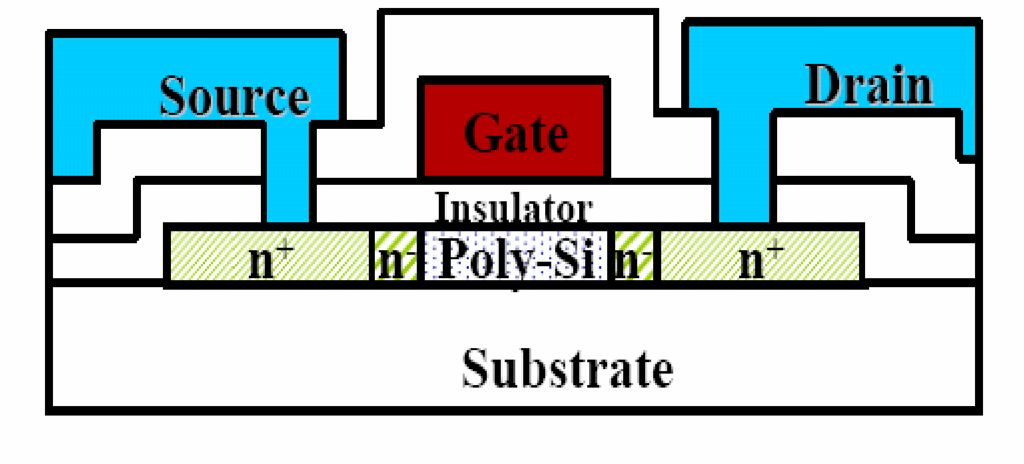


Figure 3-3(a). The n-type devices cross sectional.

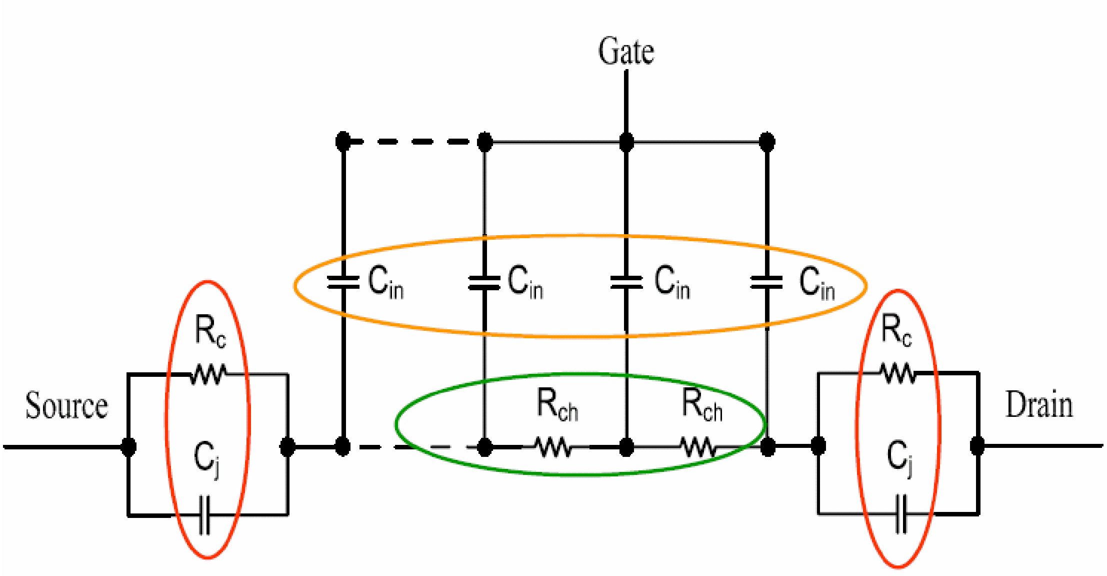


Figure 3-3(b)The n-type slicing circuits

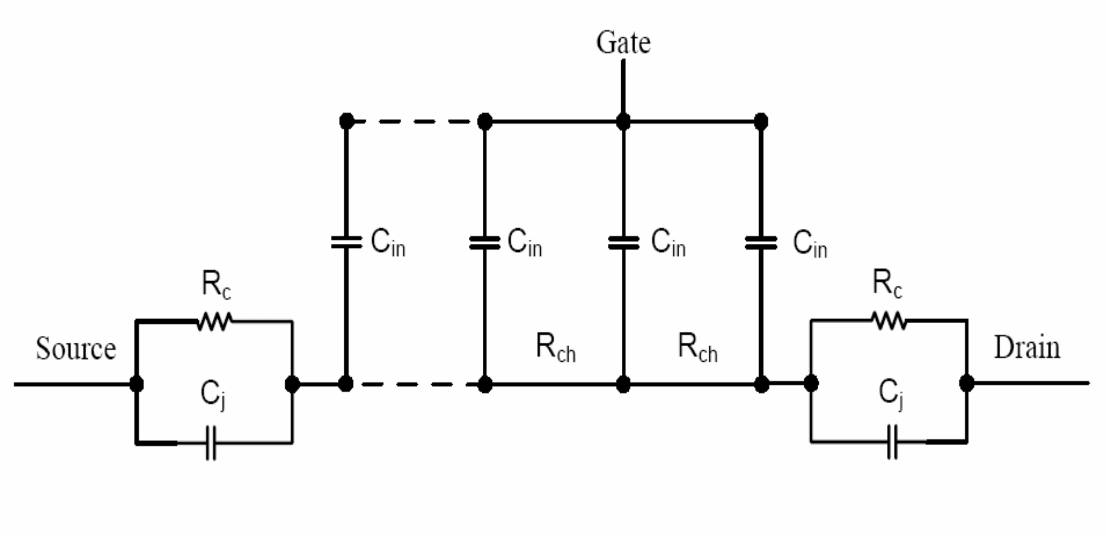


Figure 3-4(a) The slicing circuit that the R_{ch} is short when gate voltage is much higher than the V_{th}.

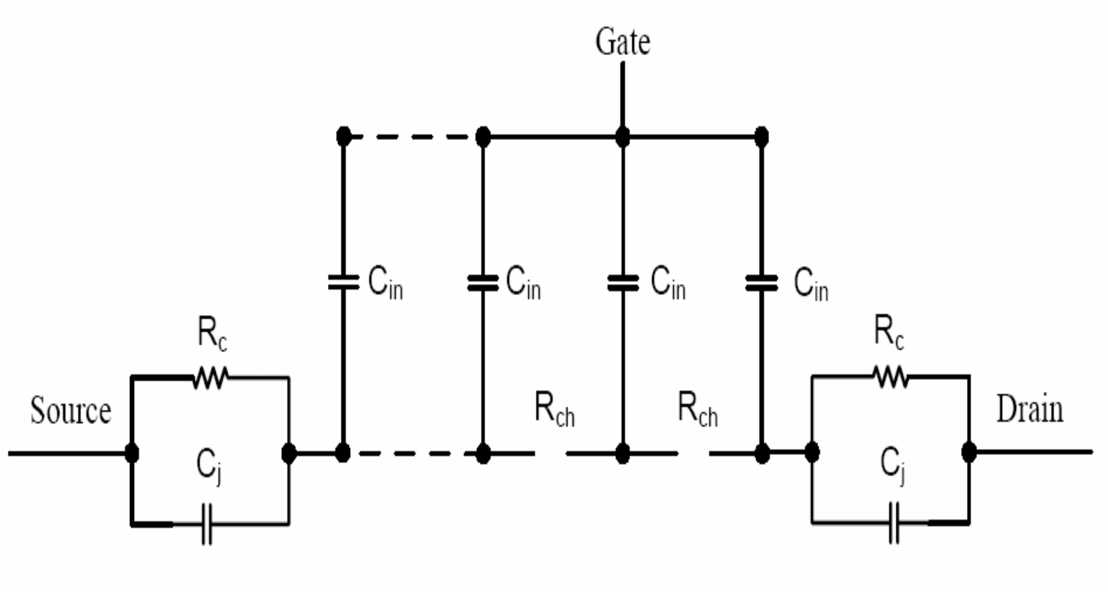


Figure 3-4(b) The slicing circuit that the R_{ch} is open when gate voltage is far below the $V_{th.}$

3.2.2 Gate-source capacitance and gate-drain capacitance

The gate voltage dependences of the normalized gate-source capacitance (C_{GS})

and gate-drain capacitance (C_{GD}) are shown in figure 3-5 and 3-6, respectively. The C_{GS} is measured with a floating drain and C_{GD} is measured with a floating source. The normalized capacitance is the ratio of the measured capacitance to a constant of 61.5 fF, which is the gate oxide capacitance of the TFT under test.

For the gate dynamic stress with V_D smaller than 10 V, the C_{GS} curves show almost no change, while C_{GD} curves slightly shift. For those with V_D higher than 10 V, both C_{GS} and C_{GD} curves exhibit serious distortion.

As Vg sweep from off region to on region, the channel resistance will become small and the measured C_{GS} would induce more and more distributed Cin from source region to drain region,as shown in Figure 3-7. For the TFT after stress the modified slicing model is shown in Figure 3-7, In the model, a large Rch' channel resistance near drain is introduced to represent the degradation due to many traps generated near drain region. In this case, we need higher Vg to turn on channel near drain. For the stress drain voltage of 20V, the capacitance deficiency of the C_{GS} curves appear in the range of gate voltage from 3 V to 15 V, indicating that the degradation region is near the drain.

On the other hand, for the measured C_{GD} the degraded Rch' prevents the charges flowing to the channel. Therefore, summation of Cin from drain region to source region can not be measured until the gate voltage increases highly enough, as illustrated in Figure 3-7. For the stress drain voltage of 20V, the C_{GD} approaches to maximum when gate voltage higher than 10 V as shown in 3-6(b).

It is noticeable that the degradation accelerated drastically by the drain bias are observed in both the I-V and C-V characteristics. It requires more analyses to be explained. In next section, we use simulation tool ISE to provide the information about the electric field distribution in the TFT.

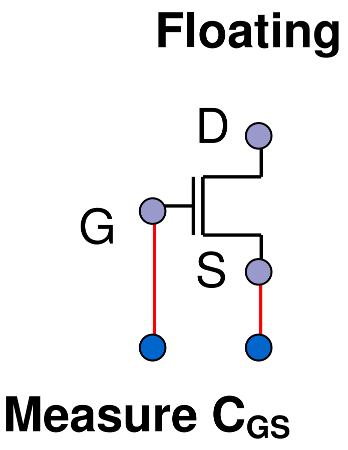


Figure 3-5 (a) C_{GS} measurement configuration

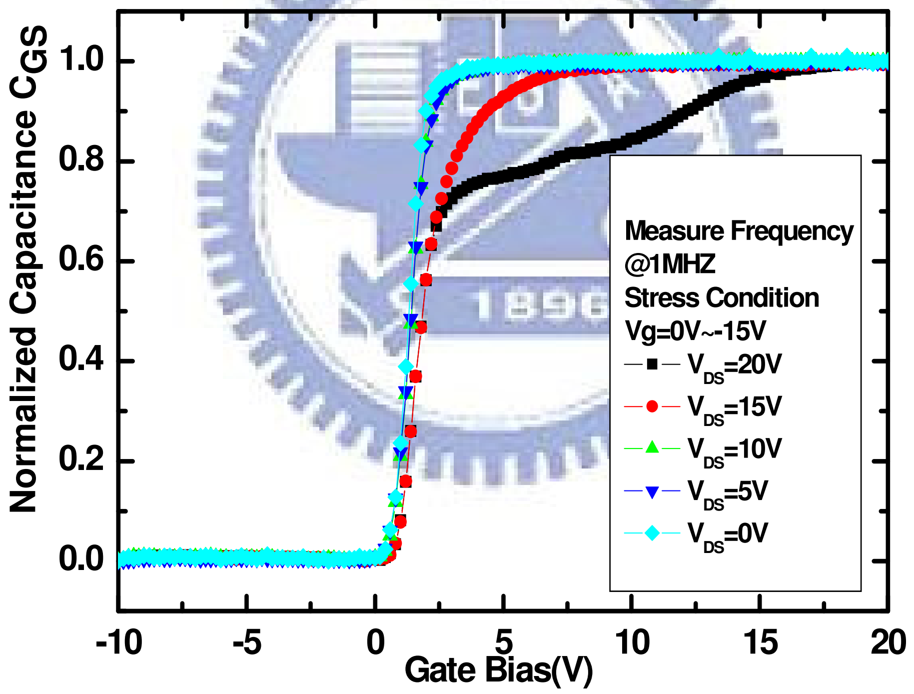


Figure 3-5 (b) Normalized C_{GS} curves versus gate voltage after AC stress with drain bias measured at frequency of 1M Hz

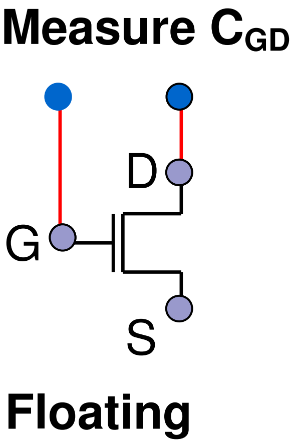


Figure 3-6 (a) C_{GD} measurement configuration

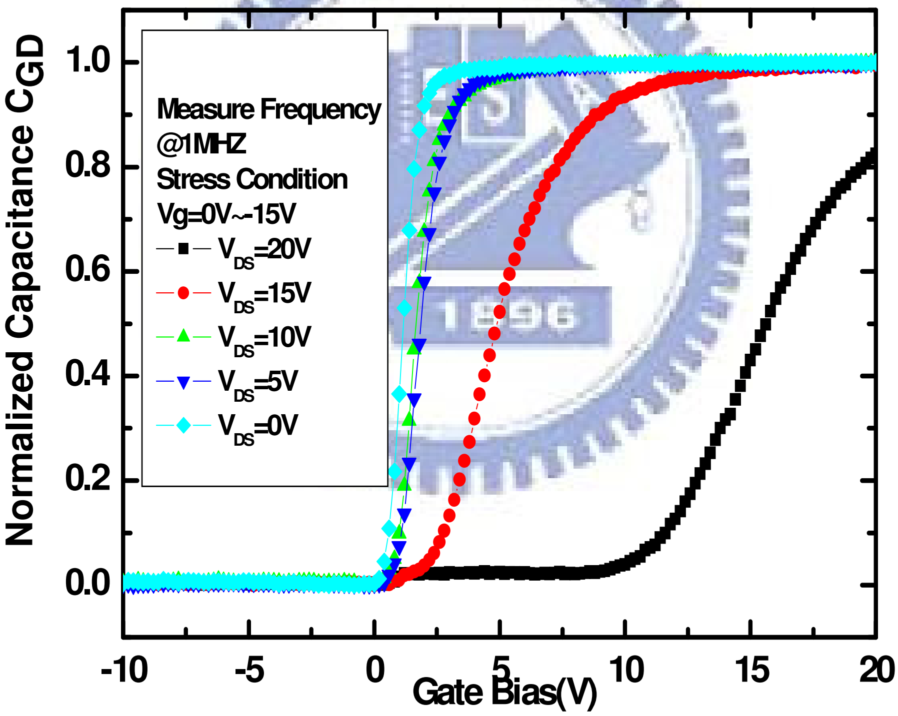


Figure 3-6 (b) Normalized C_{GD} curves versus gate voltage after AC stress with drain bias measured at frequency of 1M Hz.

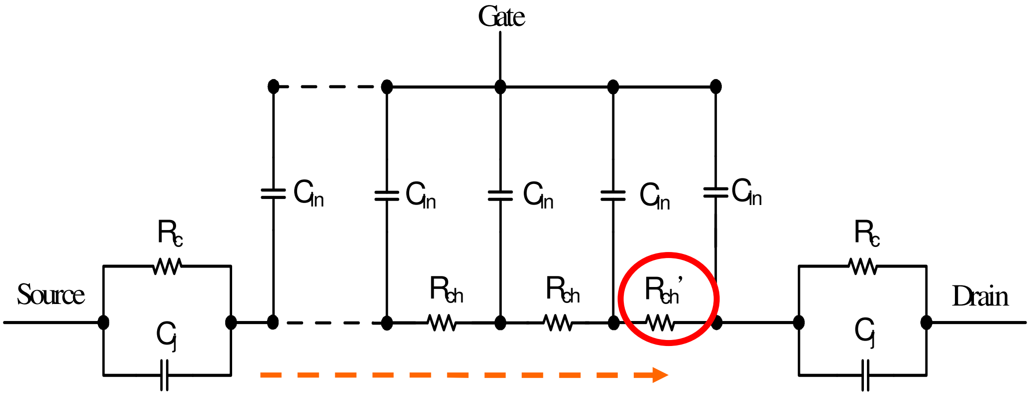


Figure 3-7 The modified slicing circuit with large resistance Rch' near drain region after stress

3.3 Electric field simulation

In order to profile the electric field distribution in the device, ISE_TCAD was used to simulate the device. Owing to the limit of this application software, only the DC cases can be simulated. For gate voltage of -15V and source and drain grounded (V_S=0V, Vg=-15V ,V_D=0V) , the simulated electric field magnitudes distribution is shown in Figure 3-8. It is observed that the high electric field occurs near the source and drain symmetrically. The field along the channel is plotted in Figure3-10 and the maximal value is about $4x10^4$ V/m . For gate voltage of -15V, source grounded, and drain bias of 20V (V_S=0V, Vg=-15V ,V_D=20V), it is observed that the maximal electric field is as high as $5.8x10^5$ V/m near drain region as shown in Figure 3-9. The electric field magnitude distribution along the channel is plotted in Figure 3-10. With the drain voltage increase, the electric field increases only near drain region. As shown in Figure 3-11, that the relation between the V_{DS} and the maximal electric field value is almost linear. Figure 3-12 and Figure 3-13 respectively show the vertical component (Ey)and lateral component (Ex) of the electric field. The negative value means the field directions are from bulk to gate and from drain to source correspondingly. The device lateral electric field (Ex) is about five times of vertical electric field (Ey) in the amplitude. Electrons flowing through the high electric field near the drain region can gain energy to become hot electrons. The existence of the drain field makes the degradation of the AC stress with drain bias very different from that with source/drain grounded.

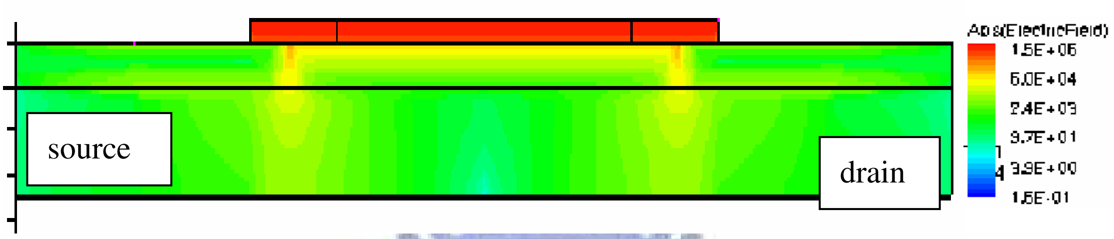


Figure3-8 The electric field distribution for gate voltage of -15V and source/drain grounded (V_S=0V,Vg=-15V,V_D=0V)

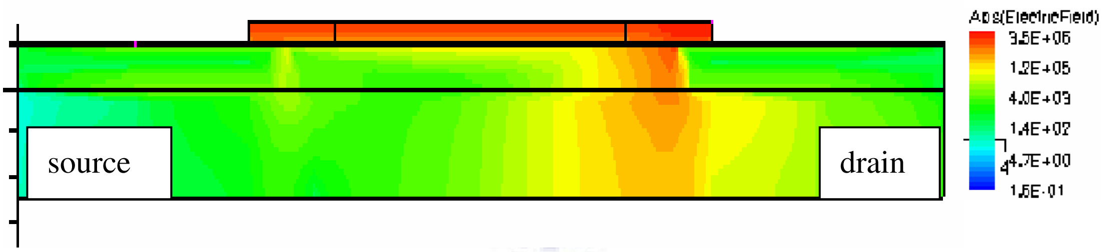


Figure 3-9 The electric field distribution for gate voltage of -15V, source grounded, and drain bias of 20V (V_S=0V,Vg=-15V,V_D=20V)

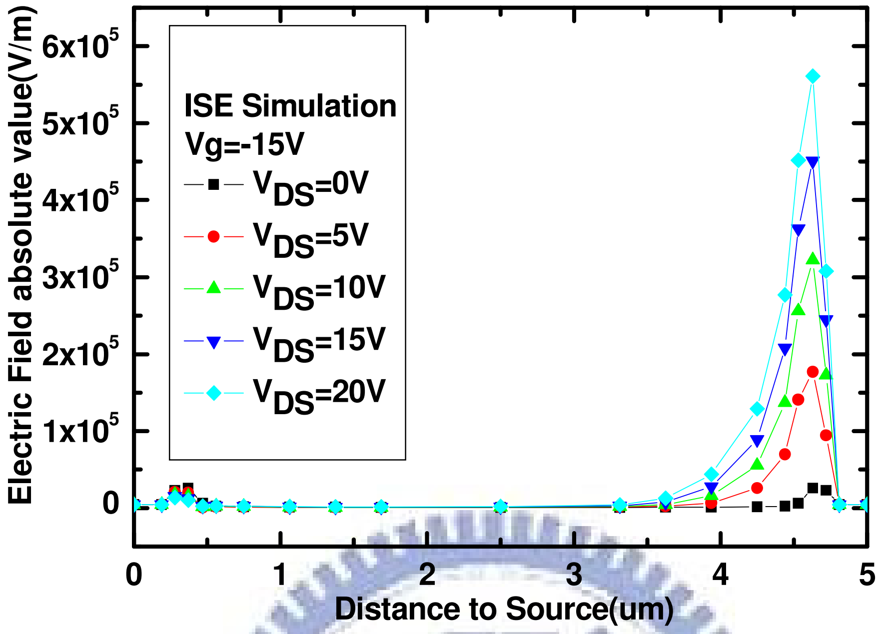


Figure 3-10 The electric field absolute value under gate voltage of -15V and source grounded with various drain bias

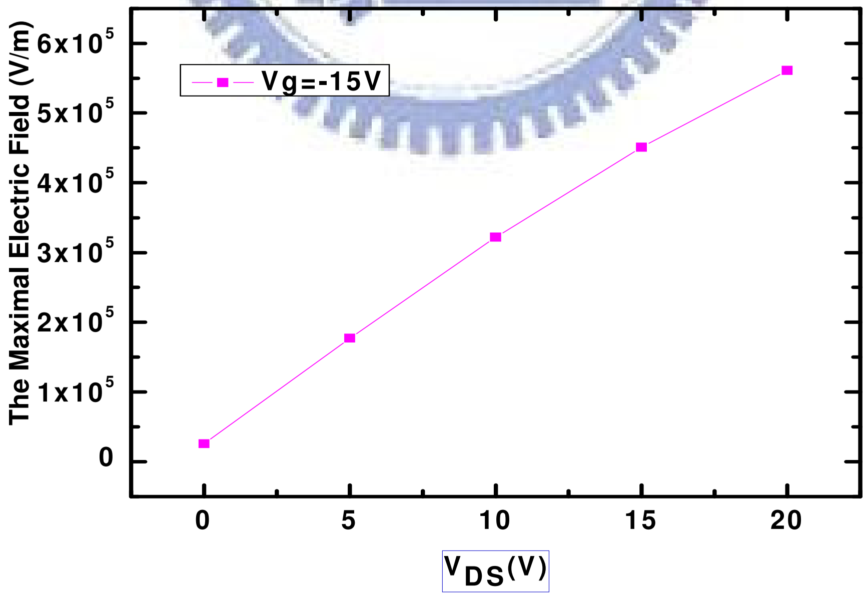


Figure 3-11 The maximal electric field under gate voltage of -15V and source grounded with various drain bias

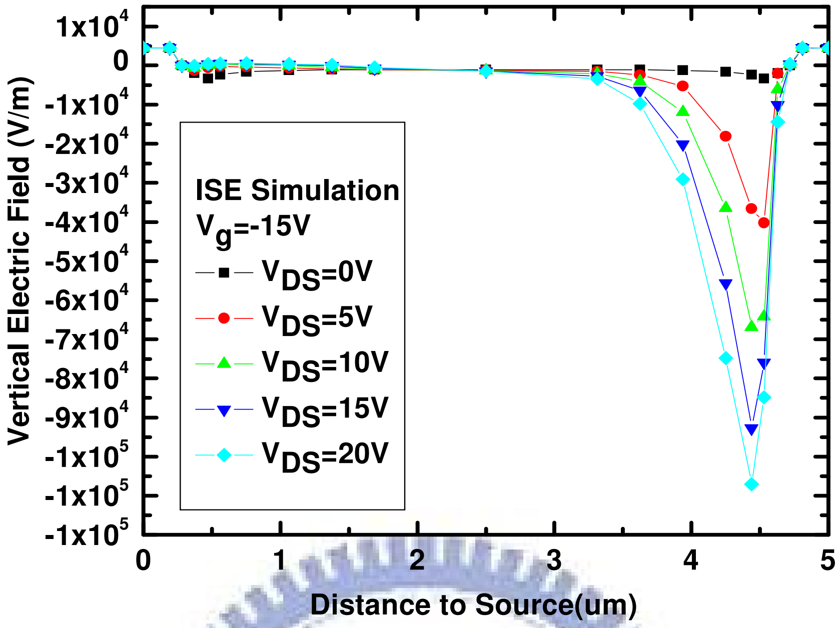


Figure 3-12 The vertical electric field distribution along the channel

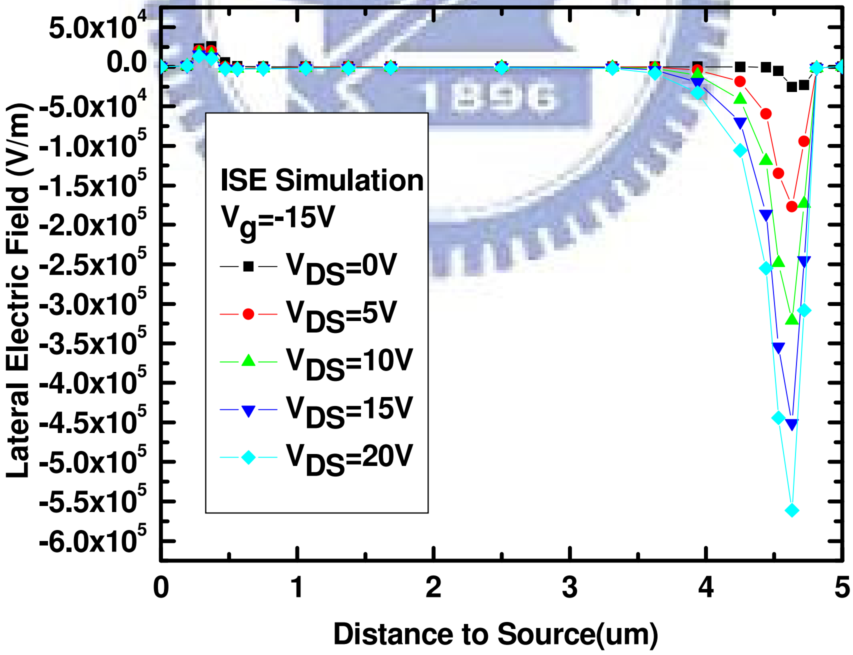


Figure 3-13 The lateral electric field distribution along the channel

3.4 Off Region AC stress with Drain and Source Bias

For this section, we further investigate the effect of drain bias by comparing the degradation degree to those without source/drain voltage difference. Another gate AC stress with source and drain both 20V as shown in Figure 3-14 is considered.

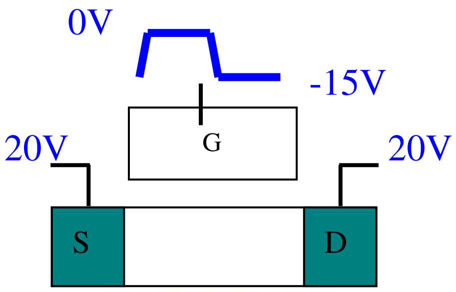


Figure 3-14 TFT under gate AC stress in off region with drain and source 20V

We simulate the electric field distribution when V_S=20V,Vg=-15V,and V_D=20V by ISE_TCAD. The result is shown in Figure 3-15. The electric field is plotted in Figure 3-16 with the other two cases of V_S=V_D=0V,Vg=-15V and V_S=0V,V_D=20V,Vg=15V. It is observed the electric field almost the same as source and drain grounded. For the cases without voltage difference between source and drain the maximal electric field is 1.79x10^5 V/m. On the contrary, with drain bias of 20V, the maximal electric field is near drain and its value is increased to 5.61x10^6 V/m.

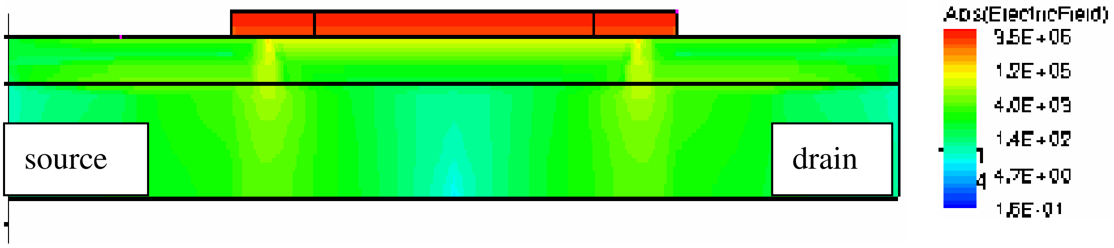


Figure 3-15 electric field distribution when V_S=20V Vg=-15V, and V_D=20V.

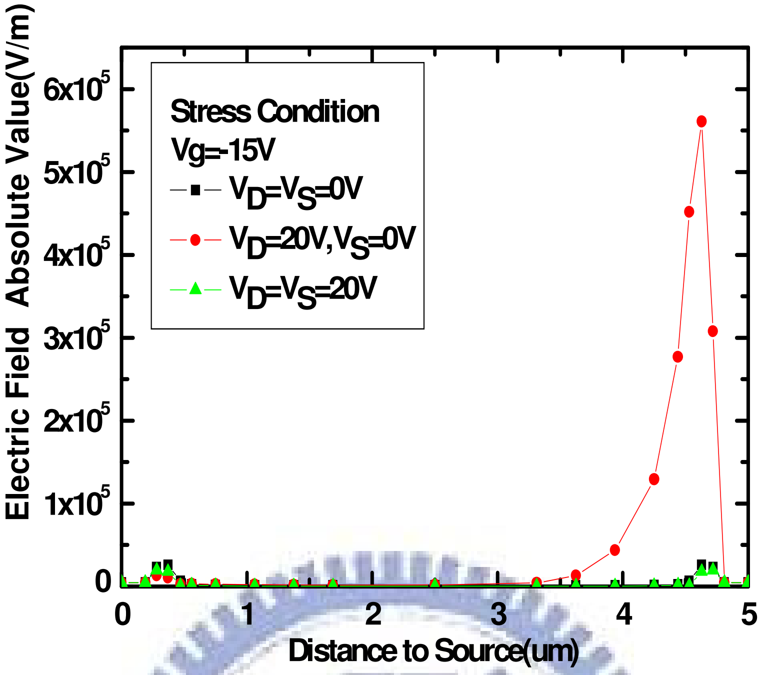


Figure 3-16 The electric field absolute value under gate AC stress with various source and drain bias

Figure 3-17 compares the Id-Vg transfer curves of the n-type poly-Si TFT before and after 60 s of dynamic gate stresses of the three cases., After the gate AC stress with both drain and source voltage at 20 V, the curves of Id-Vg and the gate-dependent mobility are very similar to those stressed with source and drain grounded. In Figure 3-18 and Figure 3-19 ,we also can see that the C_{GS} and C_{GD} almost no change.

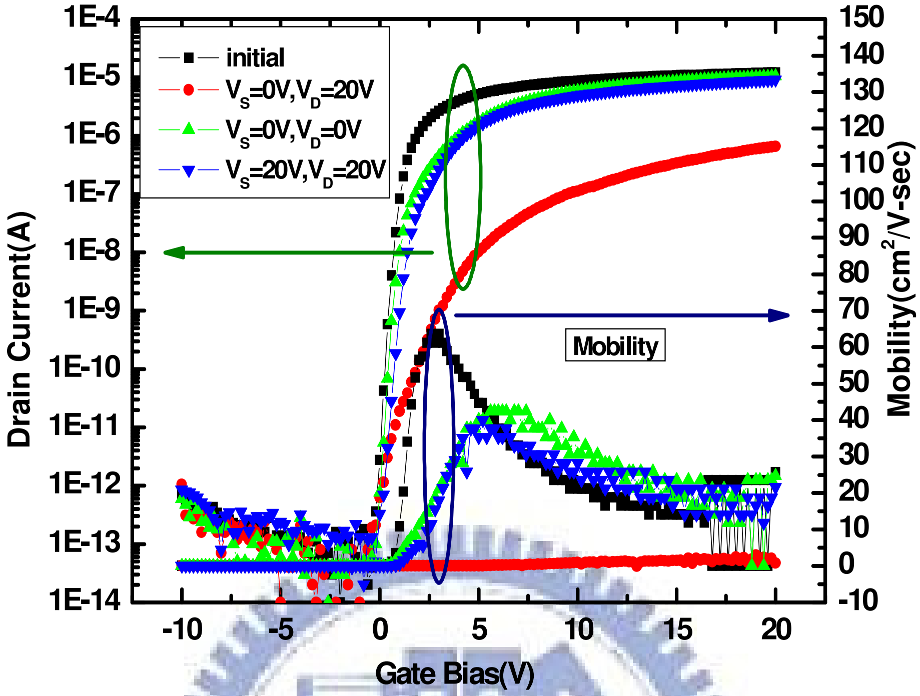


Figure 3-17 I_D-V_G and mobility extract under various stress condition

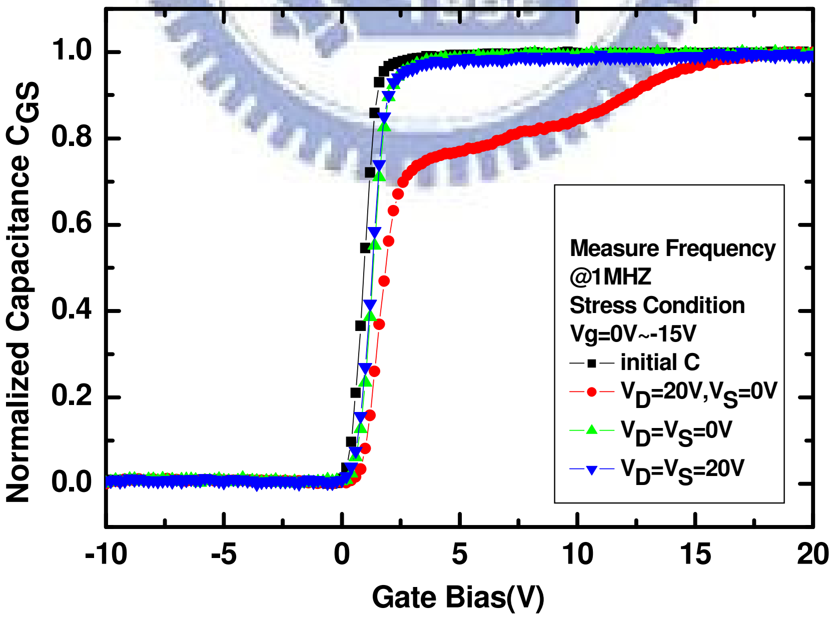


Figure 3-18 Normalized C_{GS} curves under gate AC stress with various source and drain bias measured at frequency of 1M Hz

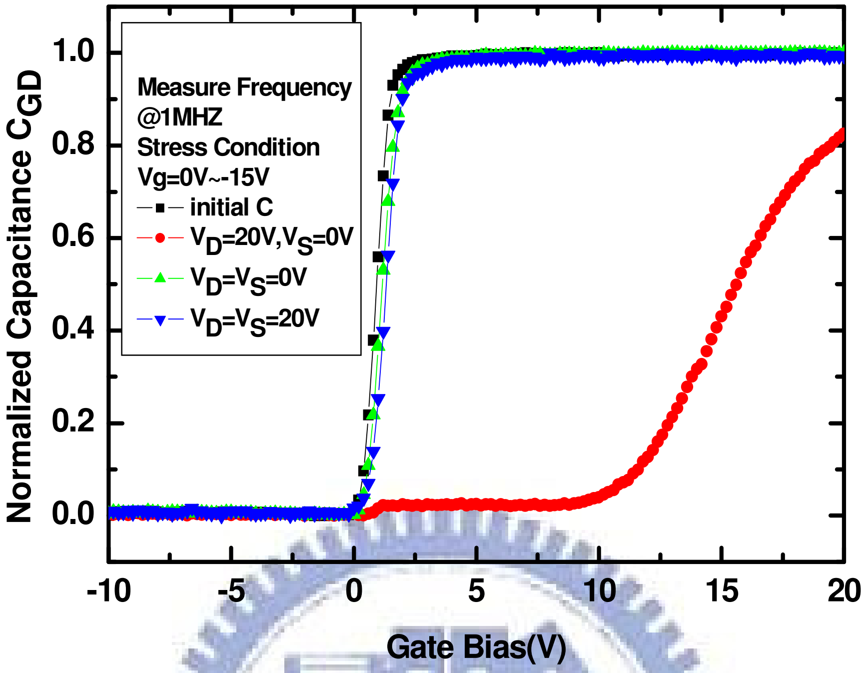
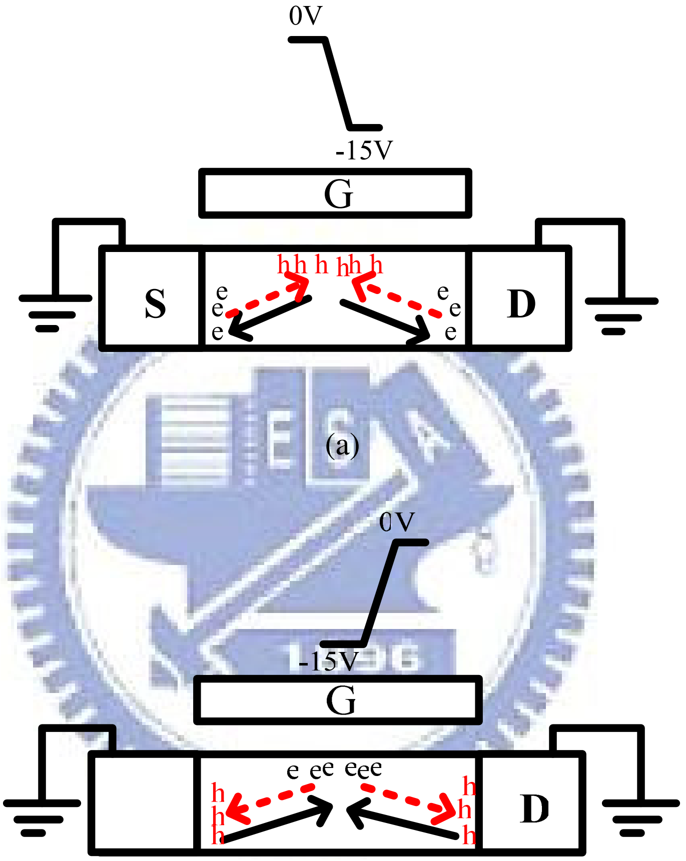


Figure 3-19 Normalized C_{GD} curves under gate AC stress with various source and drain bias measured at frequency of 1M Hz

3.5 Degradation Model and Pump Current

For the case with source and drain grounded, as the gate voltage swings between the ON and OFF region, carriers are gathered to the oxide/poly-Si interface. When the gate voltage swings from high to low, the induced electrons in the channel would rush to the source and drain regions. These carriers exposed to the high electric field move rapidly to the source and drain symmetrically and become hot carriers, causing the device degradation. The flow of the carriers reflects the displacement current induced by the AC gate pulses. In MOSFETs, under similar stress condition, the induced current may come from and goes to the bulk electrode besides the source and drain electrode. However, in poly-Si TFTs, since there is no bulk electrode, the carriers could only come from and go to source and drain. When the gate voltage swings from 0V to -15V, gate voltage of -15V would induce holes in the channel and can only be discharged the electrons to source and drain symmetrically, as shown in figure 3-20(a).On the contrary, when the gate voltage swings from -15V to 0V, the holes discharged to source and drain that means the electrons flow to channel surface region , as shown in figure 3-20(b).



(b)

Figure 3-20 The proposed AC stress degradation model in TFT structure with source and drain grounded when Vg swings (a) from 0V to -15V and (b) from -15V to 0V

On the other hand, during AC gate stress when drain bias is applied, the current flow to source and drain asymmetrically and the electrons tend to rush toward the drain electrode, as illustrated by the bold arrow in figure 3-21(c). Therefore, an effective DC current from source to drain could be measured. Intuitively, since the TFT operates in the off region, this current should be very small. Nevertheless, since there is no bulk electrode for poly-Si TFTs, the potential of the silicon surface would be directly coupled by gate voltages. When the gate voltage swings from 0V to -15V, the gate voltage induce the holes make the devices stay in deep accumulation and discharge mass electrons to drain because the drain bias of 20V ,as illustrated in figure 3-21(a). On the contrary, when the gate voltage swings from -15V to 0V in the transient region, the induced holes discharge to source region and the electrons near source flow to channel region. In this condition, the drain bias is so large that almost all the channel electrons will flow to drain, as illustrated in figure 3-21(b) At this time, a channel could be formed temporarily. In such case, the offset currents under gate voltage toggling process may then be observed even in the range of the off voltage.

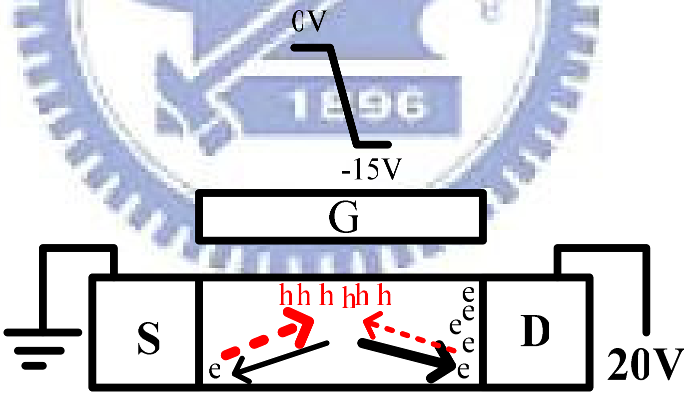


Figure 3-21(a) The proposed AC stress degradation model in TFT structure with drain bias voltage when Vg swings from 0V to -15V

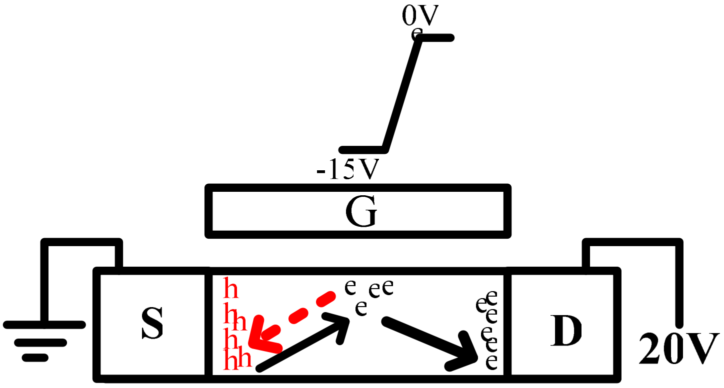


Figure 3-21(b) The proposed AC stress degradation model in TFT structure with drain bias voltage when Vg swings from -15V to 0V

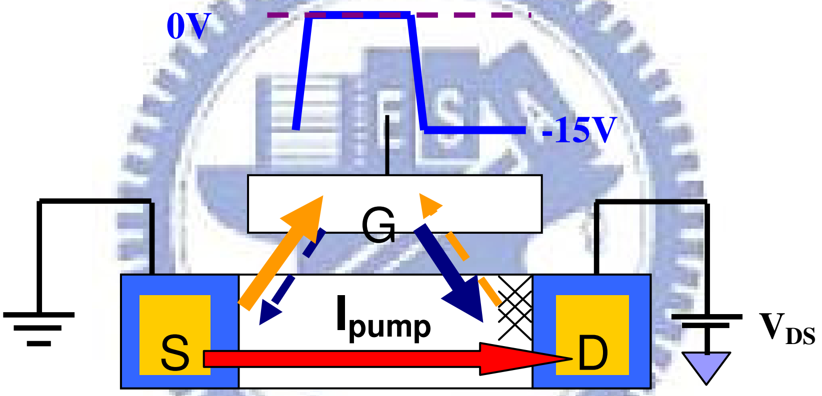


Figure 3-21(c) The proposed AC stress degradation model in TFT structure with drain bias voltage

For the case with source and drain grounded, the current induced by the gate AC stress flows symmetrically and thus the average drain current is zero. However, for the gate AC stress with drain bias, the electron current flowing to drain is larger than that flowing to source, as illustrated in figure 3-21(c). Consequently, the overall drain current is no more zero. This current may in turn obtain energy from the electric field near the drain region, resulting in the severe degradation. According to the inference, an offset drain current induced by the gate pulses should occur during the AC stress. Hence, the sampling measurement using Agilent 4156A semiconductor parameter analyzer was conducted to monitor the current be during the gate dynamic stress. As shown in figure 3-22, the drain current as large as 10^{-6} A during stress is observed. The stress and sampling setup is shown in the inset of figure 3-22. The measured current can be taken as the drain current pumped by the gate pulses. In the source region of the TFT, the electric field prevent the carriers flow into the source. Hence the degradation near the source region is less and restricts the creation of hot carriers. On the contrary, in the drain region, the pumped current flows through the high electric field, making the carriers accelerated and becoming the high energy carriers. This current would be larger for the higher drain voltage, which eventually leads to the worse device degradation. It is further observed that the initial values of the measured pump currents with the stressed drain voltages of 15V and 20V are much higher than those for the other three stress conditions, revealing that the corresponding degradation behavior would be much worse. For higher drain bias, the pump current decrease with sampling time reflects the degrading process of the device under stress.

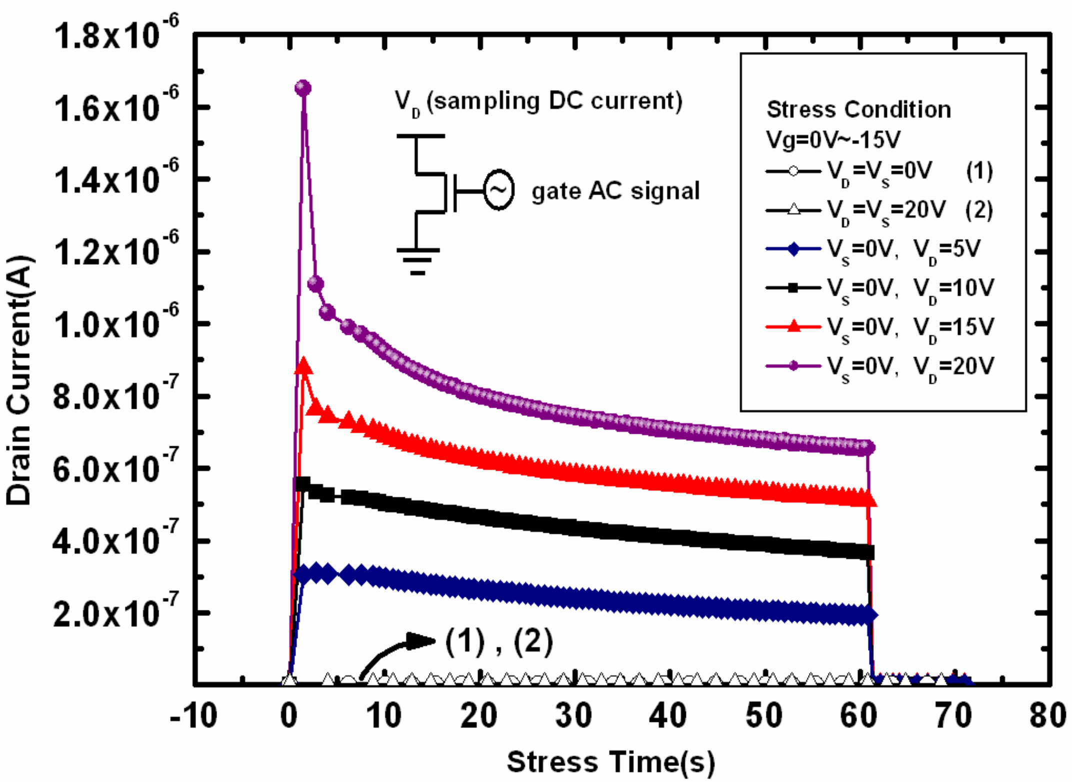


Figure 3-22 The measured DC drain currents under AC gate stress in the off region with various drain voltages.

Chapter4

Other Effects

In chapter 3, we investigate the effect under gate AC stress in off region with various drain bias. In this chapter, other effects of the stress conditions are studied. Firstly, in section 4.1 we examine the duty ratio dependence for the pump current. Secondly, we change rising time (Tr) and falling time (Tf) from 100ns to 700ns to understand their effects in sections 4-2 and 4-3. Finally, the gate voltage range is discussed dependence in section 4.4. The stress conditions are summarized in Table 4-1.

For all the results, they seem to be understandable based on the mechanisms proposed in section 3.5. Therefore, for conciseness, we only report the measurement results without explain in detail.

Experiment	Drain voltage	Vg pulse	Rising time (ns)	Falling time (ns)	Duty Ratio	Section
Duty ratio	20V	Vg=-15V~0V	100	100	25%,50 %,75%	4.1
Rising time	20V	Vg=-15V~0V	100300700	100	50%	4.2
Falling time	20V	Vg=-15V~0V	700	100,300,700	50%	4.3
Vg range effect	20V	Vg=-5,-10V,-15V, -20V~0V	100	100	50%	4.4

Table 4-1 Four stress conditions summary (Frequency=500 kHz, Stress time=60s)

4.1 Duty Ratio Dependence

In order to know the duty ratio dependence of the pump current, drain current induced by the gate pulses were measured during the gate AC stress of various duty ratio with drain bias of 20V. The experiment is illustrated in Figure 4-1. The measured currents versus stress time are shown in Figure 4-2. It is observed that the pumped current is almost the same when stressed with various gate pulse duty ratios. It tells us the duty ratio is not critical and the pulse repetition numbers maybe the dominate factor when the current is pumped. In other words, the high-level time (T_vgh) and low-level time (T_vgl) will not affect the pumped current. This result would help us to design the other experiments following.

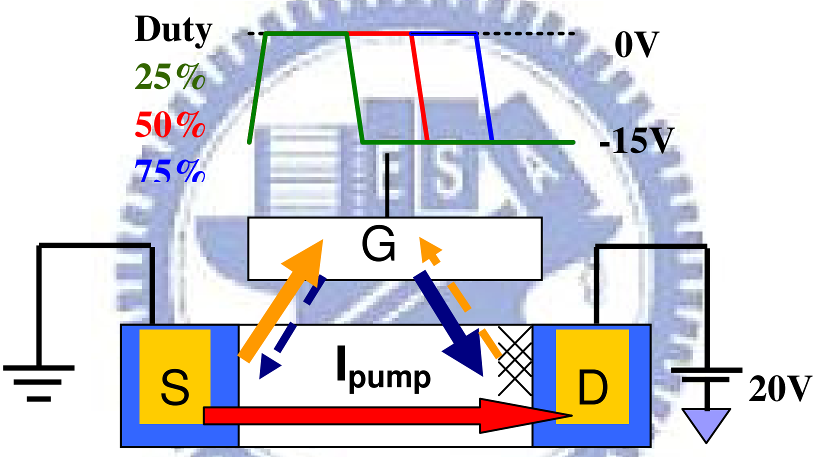


Figure 4-1 The pumped current measure under various gate pulse duty ratio

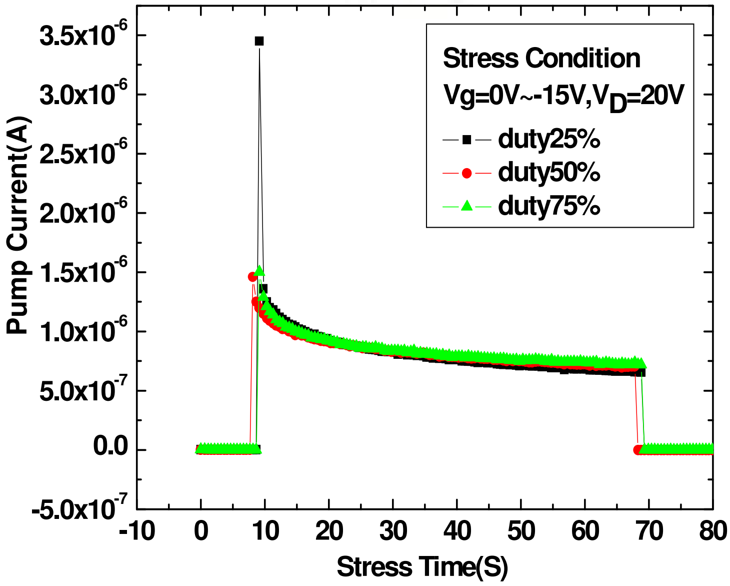


Figure 4-2 The measured DC drain currents under various gate pulse duty ratio

4.2 Rising Time Effect

In this section, we design the experiments of the gate pulse with rising time Tr 700ns, 300ns and 100ns. The falling time Tf is fixed at 700ns and the time Vg at low voltage T_vgl is 300ns. And the the time at high voltage T_vgh is changed to be according to Tr correspondingly, 300ns, 700ns and 900ns, as listed in Table 4-2. In last section, we know the T_vgh and T_vgl would not affect the pumped current and it is not the dominate factor for the device degradation. The concept of the experiment is illustrated in Figure 4-3. As the rising time getting shorter, the lower mobility and higher sub-threshold swing are observed after stress, as shown in Figure 4-4(a) and Figure 4-4(b). They seriously depend on the rising time. These results suggest that the degradation occurred during the rising transition of the gate voltage.

We also measured the pumped current under the stress with various Tr. The experimental setup is shown in Figure 4-5. In Figure 4-6, we could see the pumped current dependence on the rising time. When the rising time is shorter, the pumped current increases. When Tr is as short as 100ns, the drain current is as large as 10^{-6} A. When Tr is 300ns, the drain current decreases to 10^{-8} A. As Tr increases to 700ns, the drain current is only 10^{-10} A.

Figure 4-7(a) illustrates the carrier flow under the stress of gate swing from -15V to 0V with short rising time. More electrons are induced from source to channel. When the drain bias is very large, all the induced channel electrons may flow to drain. Figure 4-7(b) illustrates the other case withlong rising time. In this case the gate induces less carriers from source to channel, since the dVg/dt is smaller than that.with short rising time In this experiment, we can know the rising time is one of the dominated factors for the device degradation as well as the pumped current. When the pump current increases, the electrons flow to high electric field near drain would result in more hot carriers. Thus the degradation behavior would be worse.

Exp	Tr (ns)	T_vgh (ns)	Tf (ns)	T_vgl (ns)	Period (ns)
1.	700	300	700	300	2000
2.	300	700	700	300	2000
3.	100	900	700	300	2000

Table 4-2 Setting of time for the experiment of Tr from 100ns to 700ns.

(Frequency=500 kHz, Stress time 60s)

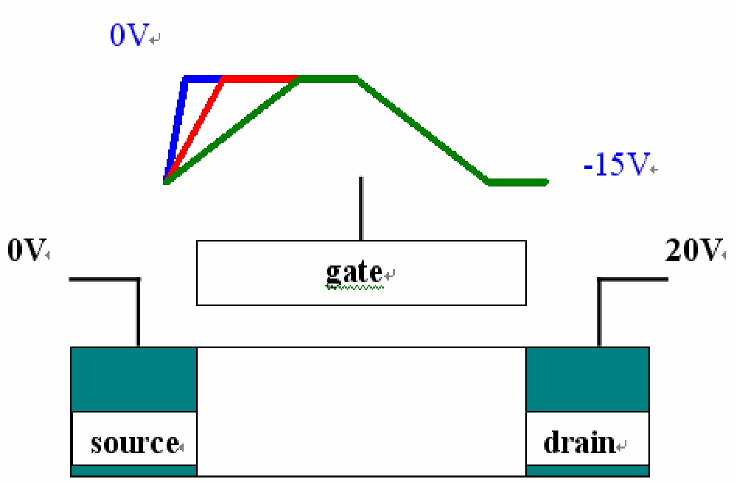


Figure 4-3 The three stressed condition with Tr from 100ns to 700ns

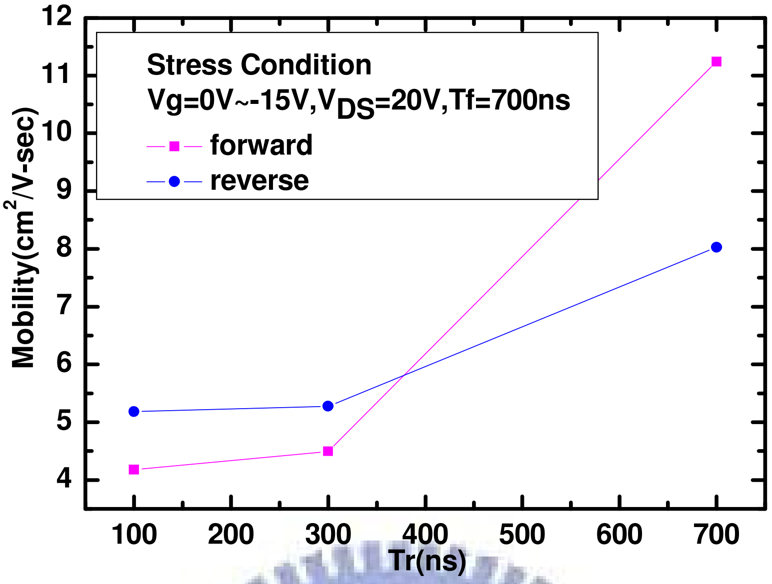


Figure 4-4(a) Dependence of the mobility after gate AC stress in the off region on rising time

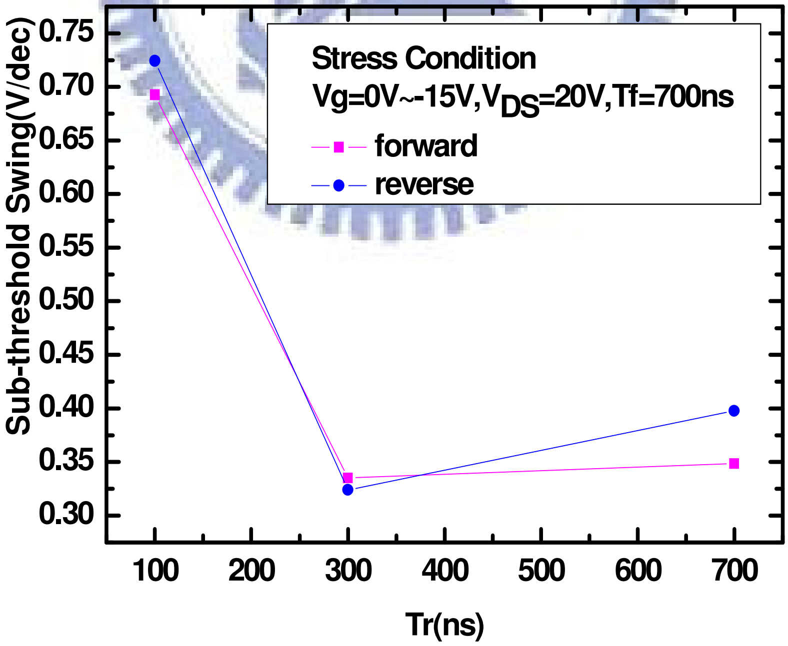


Figure 4-4(b) Dependence of the S.S. after gate AC stress in the off region on rising time

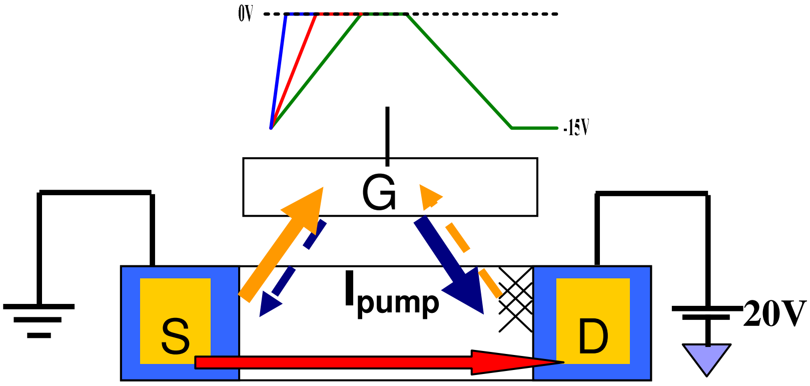


Figure 4-5 The pump current under various gate pulse rising time.

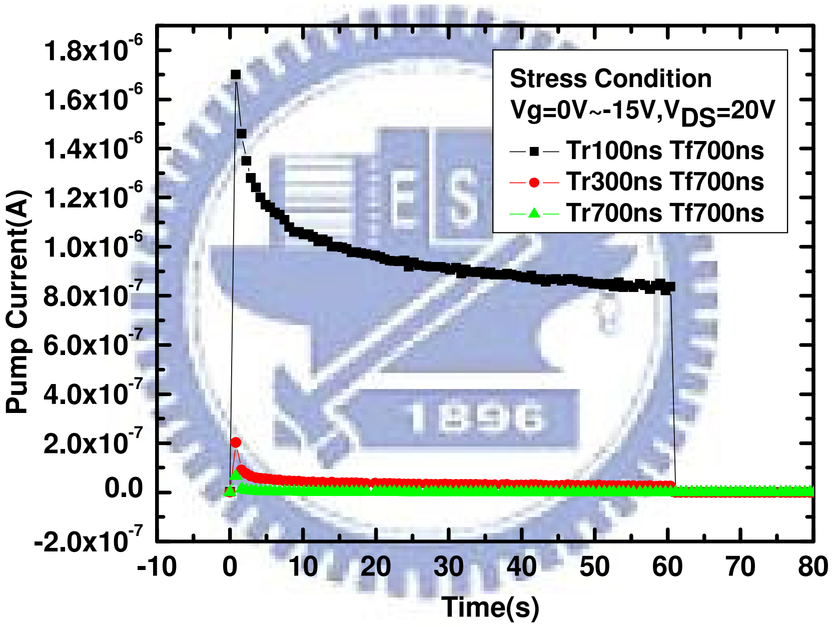


Figure 4-6 The measured DC drain current versus stress time under gate pulses with various rising time

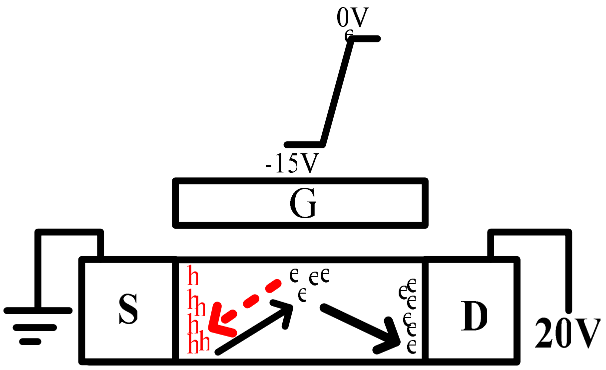


Figure 4-7(a) The proposed AC stress degradation model in TFT structure with drain bias voltage when Vg swings from -15V to 0V with short rising time

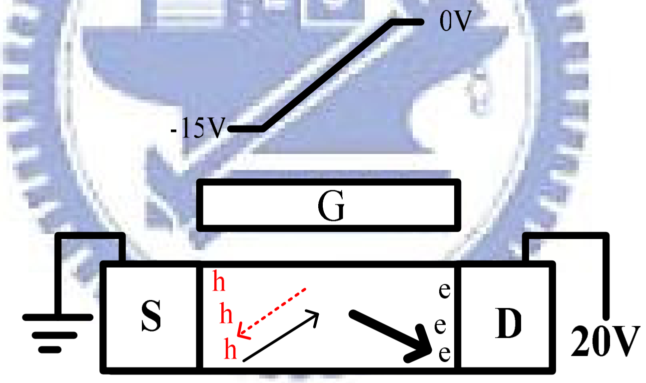


Figure 4-7(b) The proposed AC stress degradation model in TFT structure with drain bias voltage when Vg swings from -15V to 0V with long rising time

4.3 Falling Time Effect

In this section, we design the experiments of the gate pulse with falling time Tf 700ns, 300ns and 100ns. The rising time Tr is fixed at 700ns and the time at high voltage T_vgh is 300ns. And the Vg at low voltage T_vgl is changed to be according to Tf correspondingly, 300ns, 700ns and 900ns, as listed in Table 4-3. In last section, we know the T_vgh and T_vgl would not affect the pumped current and it is not the dominate factor for the device degradation. The concept of the experiment is illustrated in Figure 4-8. As the falling time getting shorter, the lower mobility and higher sub-threshold swing are observed after stress, as shown in Figure 4-9(a) and Figure 4-9(b). They seriously depend on the falling time. These results suggest that the degradation occurred during the falling transition of the gate voltage.

We also measured the pumped current under the stress with various Tf. The experimental setup is shown in Figure 4-10. Figure 4-11(a) illustrated the pumped current when rising time Tr is fixed at 700ns, we could see the pumped current only 10^{-8} A at first. After three seconds, the pumped current decreases to zero quickly. Thus we measure the pumped current when Tr is fixed at 100ns with various Tf, as illustrated in Figure 4-11(b). It is observed the pumped current is as large as 10^{-6} A. When the falling time is shorter, the pumped current decreases quickly.

Figure 4-12(a) illustrates the carrier flow under the stress of gate swing from 0V to -15V with short falling time. More electrons are discharged to drain. When the drain bias is very large, all the induced channel electrons may flow to drain. Figure 4-12(b) illustrates the other case with long falling time. In this case the gate discharges less carriers from channel to drain, since the dVg/dt is smaller than that with short falling time.

In this experiment, we can know the falling time is one of the dominated factors for the device degradation as well as the pumped current. In other word, the short falling time provides the electrons more energy to become hot electrons. Thus the pumped current decreases quickly and the degradation behavior would be worse.

Exp	Tr (ns)	T_vgh (ns)	Tf (ns)	T_vgl (ns)	Period (ns)
1.	700	300	700	300	2000
2.	700	300	300	700	2000
3.	700	300	100	900	2000

Table 4-3 Setting of time for the experiment of Tf from 100ns to 700ns

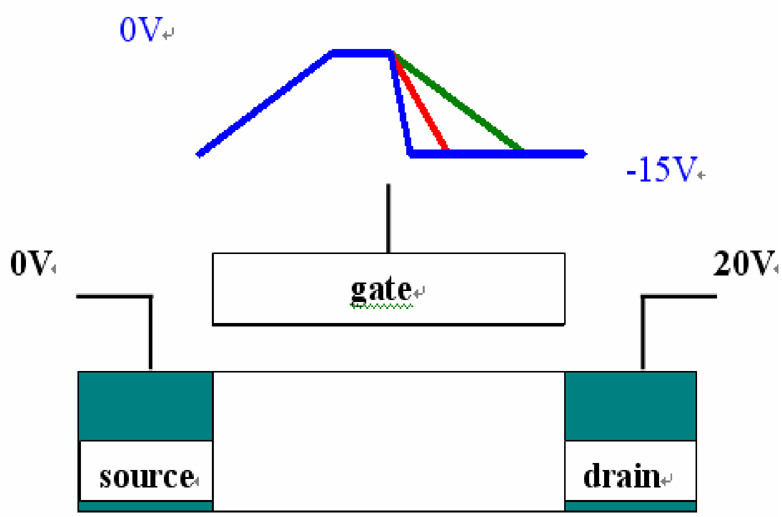


Figure 4-8 The three stressed condition with Tf from 100ns to 700ns

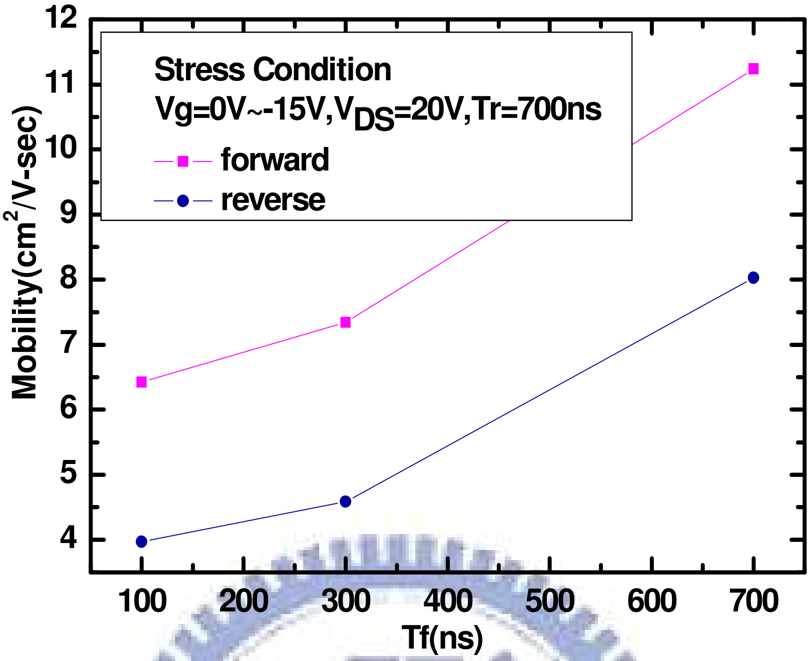


Figure 4-9(a) Dependence of the mobility after gate AC stress in the off region on falling time

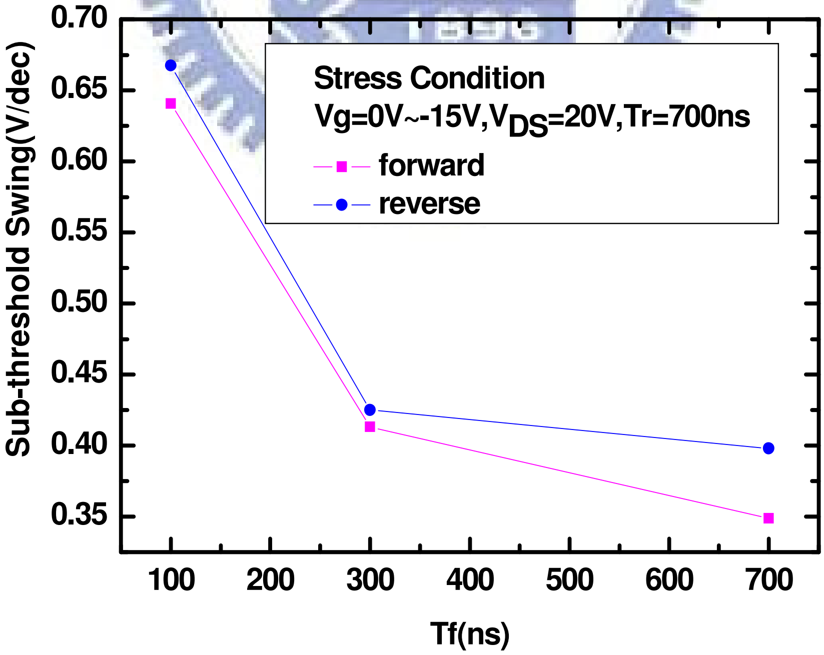


Figure 4-9(b) Dependence of the S.S. after gate AC stress in the off region on falling time

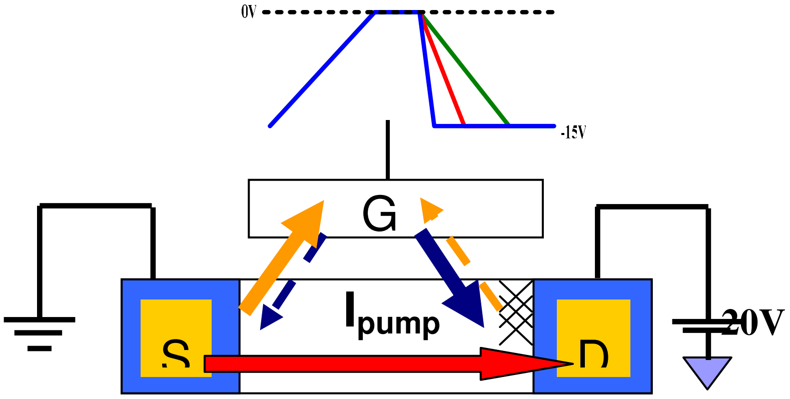


Figure 4-10 The pump current under various gate pulse falling time

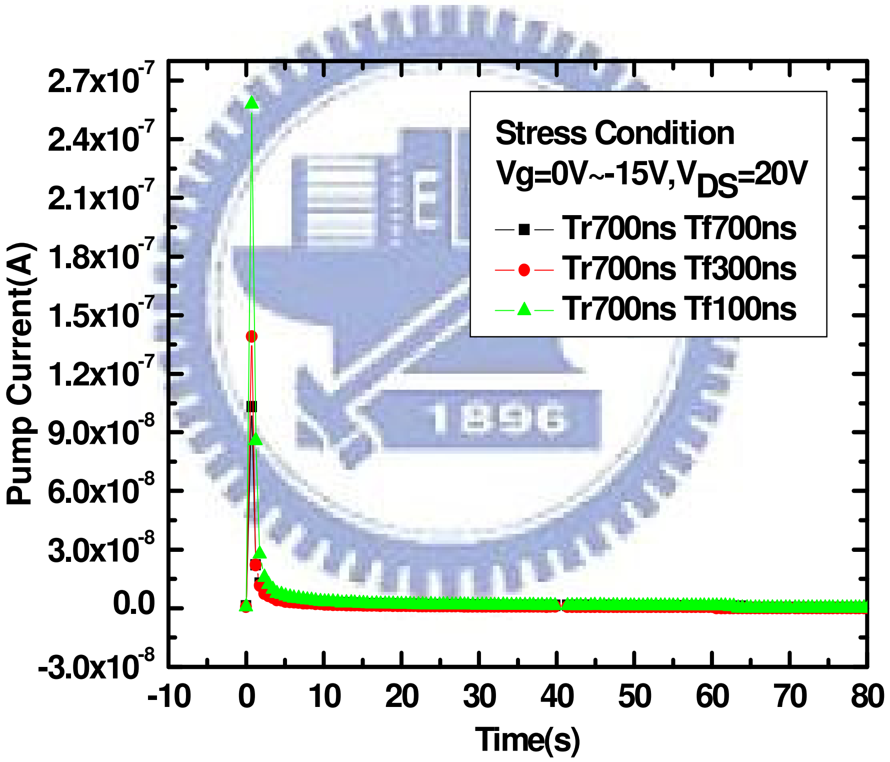


Figure 4-11(a) The measured DC drain current versus stress time under gate pulses with various falling time

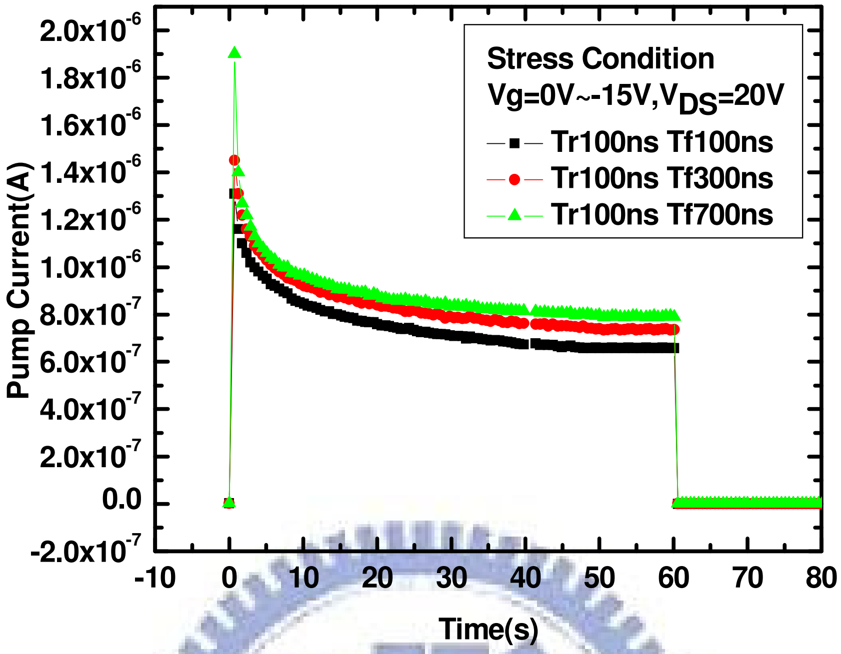


Figure 4-11(b) The measured DC drain current versus stress time under gate pulses with various falling time

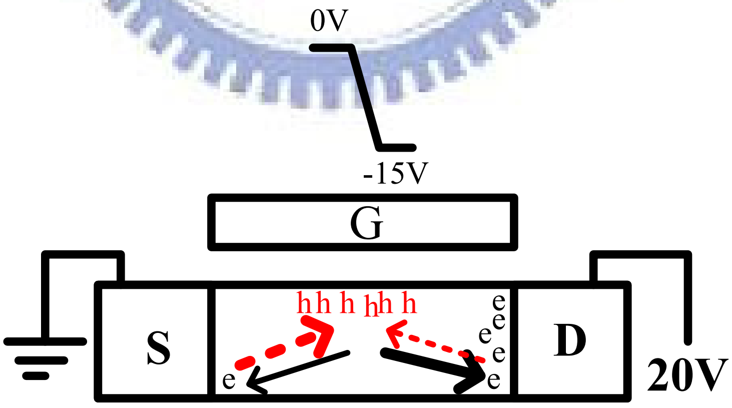


Figure 4-12(a) The proposed AC stress degradation model in TFT structure with drain bias voltage when Vg swings from 0V to -15V with short falling time

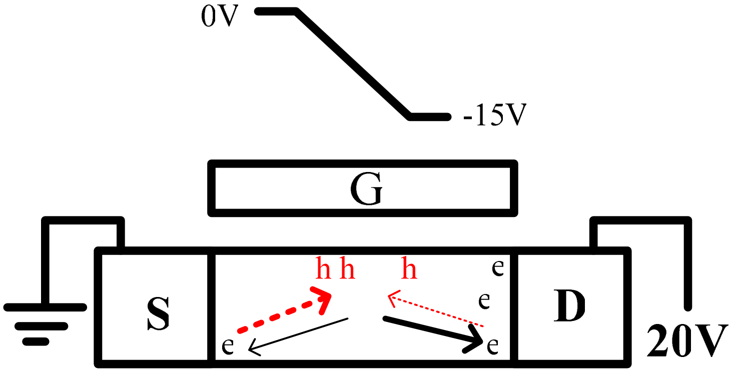


Figure 4-12(b) The proposed AC stress degradation model in TFT structure with drain bias voltage when Vg swings from 0V to -15V with long falling time

4.4 Vg Range Effect

The pulse signals with Vgh of 0 V and Vgl from -5V to -20V was applied to the gate electrode of TFTs. The AC stress experiment is illustrated in Figure 4-13.

Figure 4-14(a) shows the degraded mobility of the n-type poly-Si TFT after 60s of dynamic gate stress with different drain voltage V_D for different Vg ranges. The larger Vg range, the more degradation of the mobility is observed. Figure 4-14(b) shows the degraded sub-threshold swing of the n-type poly-Si TFT after 60s of dynamic gate stress with different drain voltage V_D for different Vg ranges. It is observed when V_{DS} is smaller than 10 V and Vg range is smaller than 15 V, the sub-threshold swing exhibits almost no degradation. But when V_{DS} higher than 10V, the sub-threshold swing seriously degrades.

Figure 4-15(a)~(h) shows the C_{GS} and C_{GD} curves of the devices stressed by various gate voltage ranges and various drain bias voltages. It is observed the CV curve show serious distortion when V_{DS} higher than 10 V and Vg range higher than 15 V. Both the Vg range effect and drain bias dependence are dominately responsible for the degradation. The electric field distributions in the device under various Vg ranges with drain 20V are simulated and shown in Figure 4-16. The highest electric field locates near the drain region and increases with the magnitude of Vg shown in Figure 4-17.

The pumped drain current during AC stress with various gate ranges and fixed drain bias of 20V is measure, as shown in Figure 4-18. Figure 4-19 plots the pumped current under various gate AC range. It is observe that higher Vg range would pump more current to flow. For the case of Vg range from 0V to -20V, the pump current decreases much faster than the other cases. It may be attributed to the self heating effect gets more important, resulting the severe degradation.

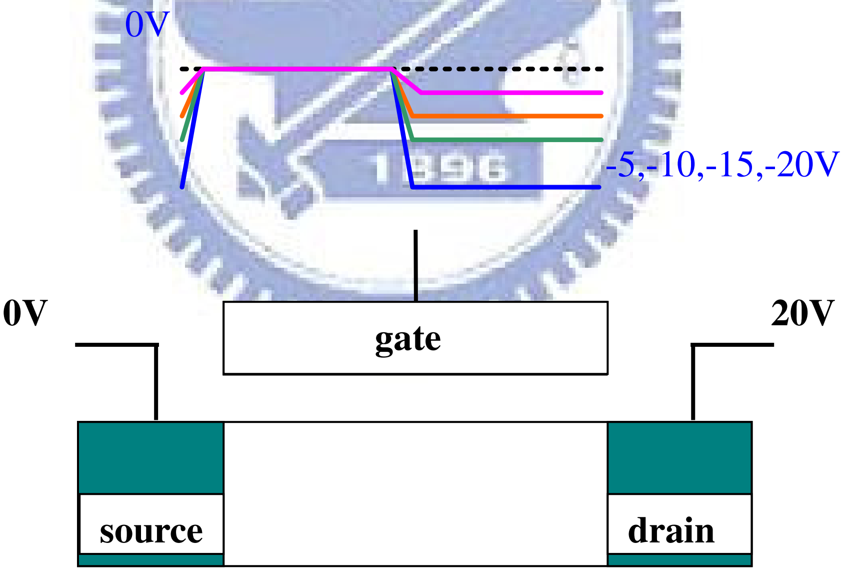


Figure 4-13 TFT under various Vg range stress with drain bias

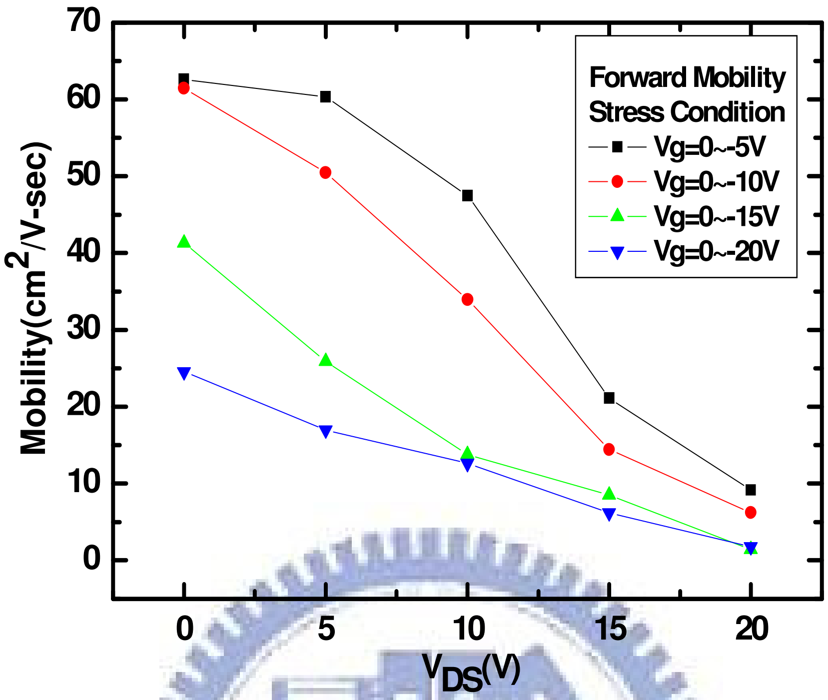


Figure 4-14(a) The mobility extract under various V_{DS} and Vg range

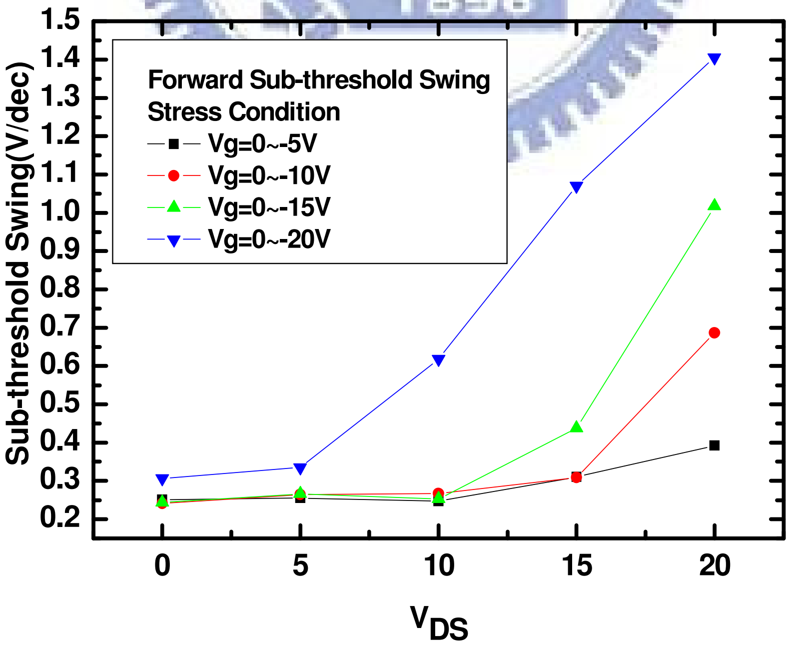


Figure 4-14(b) The sub-threshold swing extract under various V_{DS} and Vg range

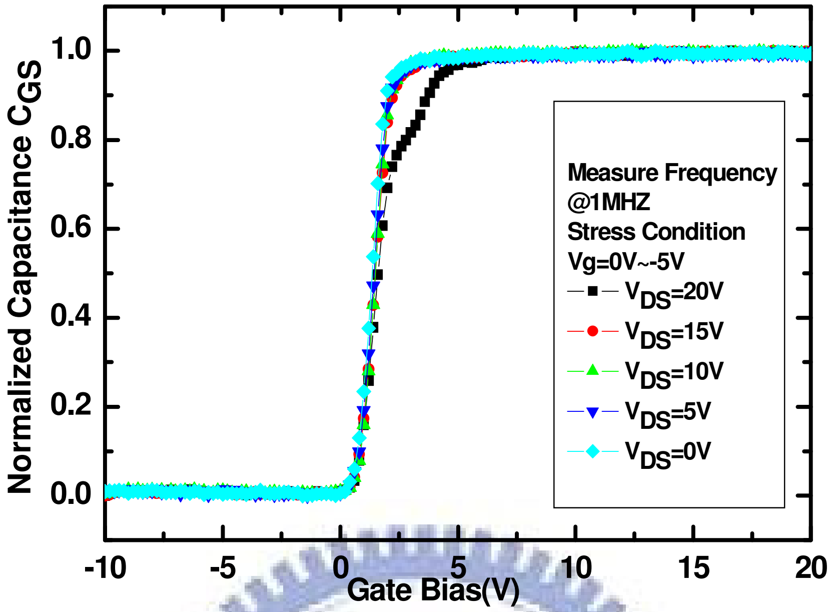


Figure 4-15(a) Normalized C_{GS} curve (after AC stress with drain bias) versus drain voltage at frequencies 1M Hz

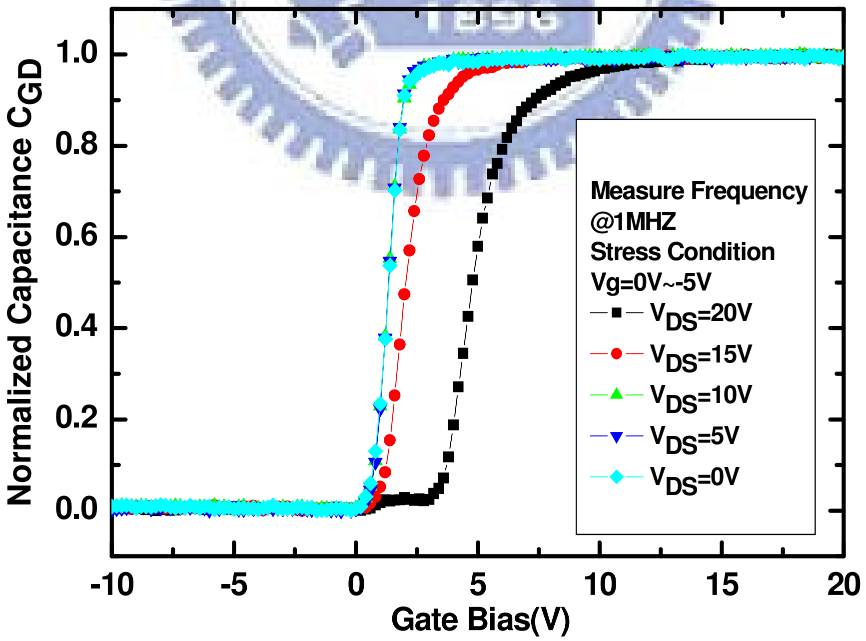


Figure 4-15(b) Normalized C_{GD} curve (after AC stress with drain bias) versus drain voltage at frequencies 1M Hz

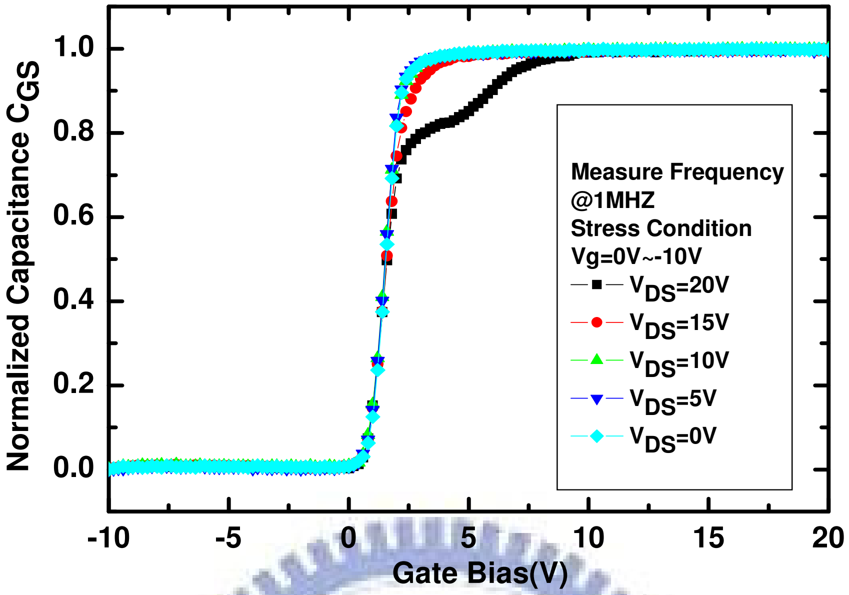


Figure 4-15(c) Normalized C_{GS} curve (after AC stress with drain bias) versus drain voltage at frequencies 1M Hz

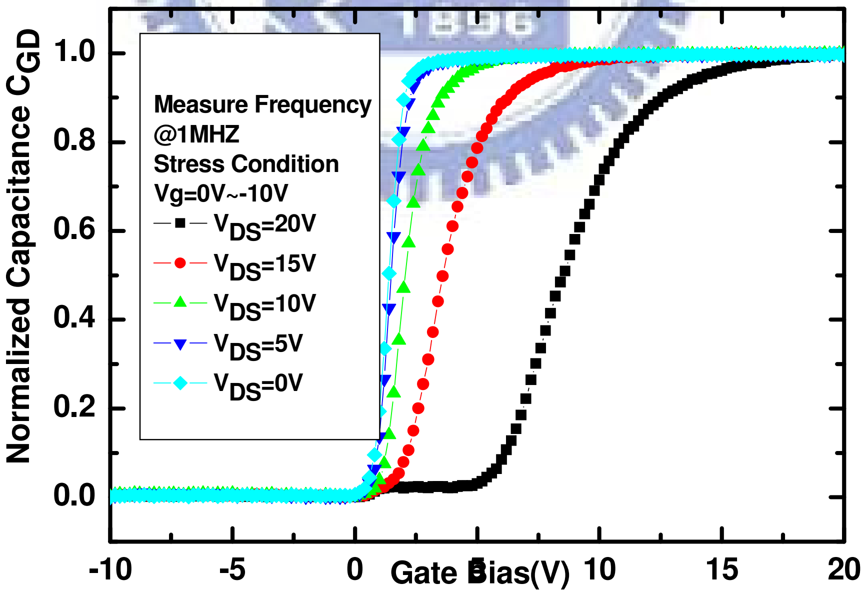


Figure 4-15(d) Normalized C_{GD} curve (after AC stress with drain bias) versus drain voltage at frequencies 1M Hz

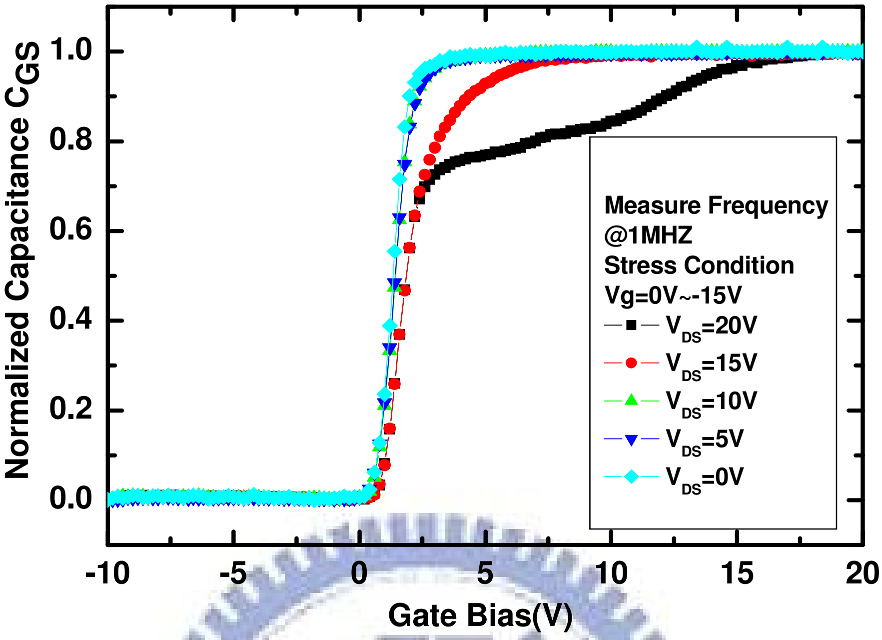


Figure 4-15(e) Normalized C_{GS} curve (after AC stress with drain bias) versus drain voltage at frequencies 1M Hz

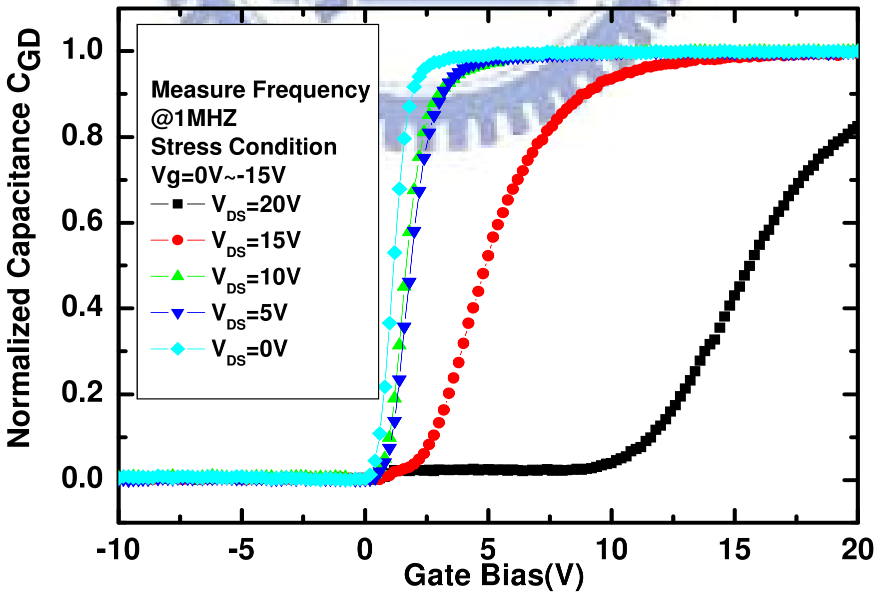


Figure 4-15(f) Normalized C_{GD} curve (after AC stress with drain bias) versus drain voltage at frequencies 1M Hz

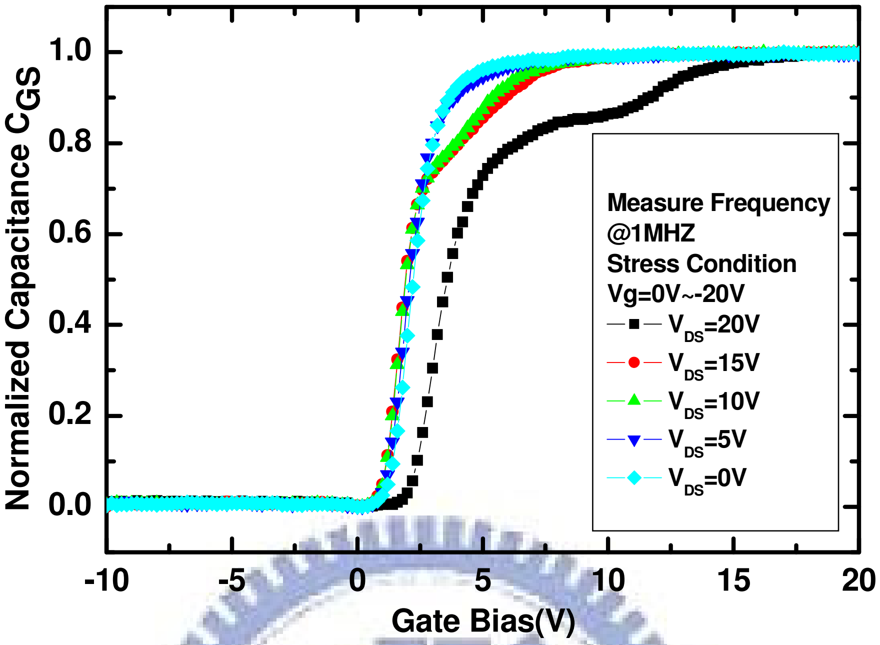


Figure 4-15(g) Normalized C_{GS} curve (after AC stress with drain bias) versus drain voltage at frequencies 1M Hz

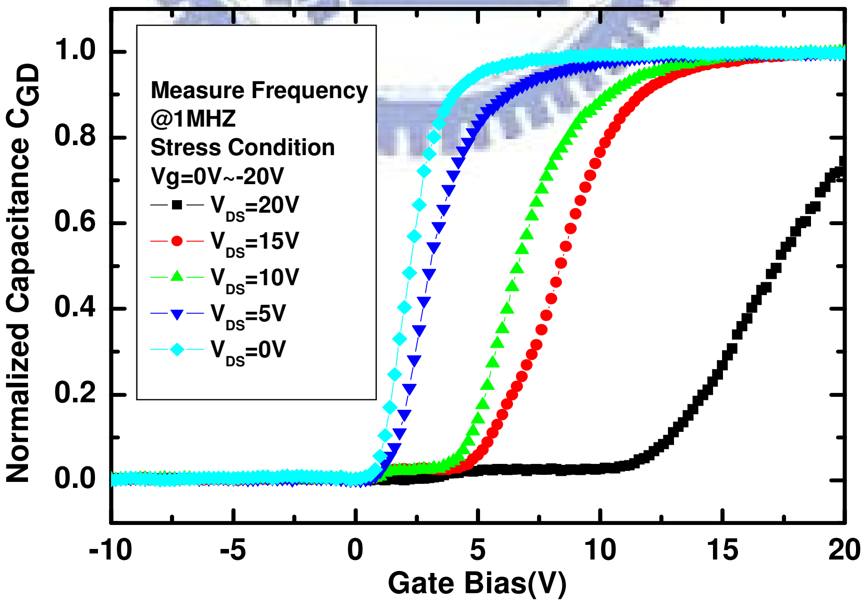


Figure 4-15(h) Normalized C_{GD} curve (after AC stress with drain bias) versus drain voltage at frequencies 1M Hz

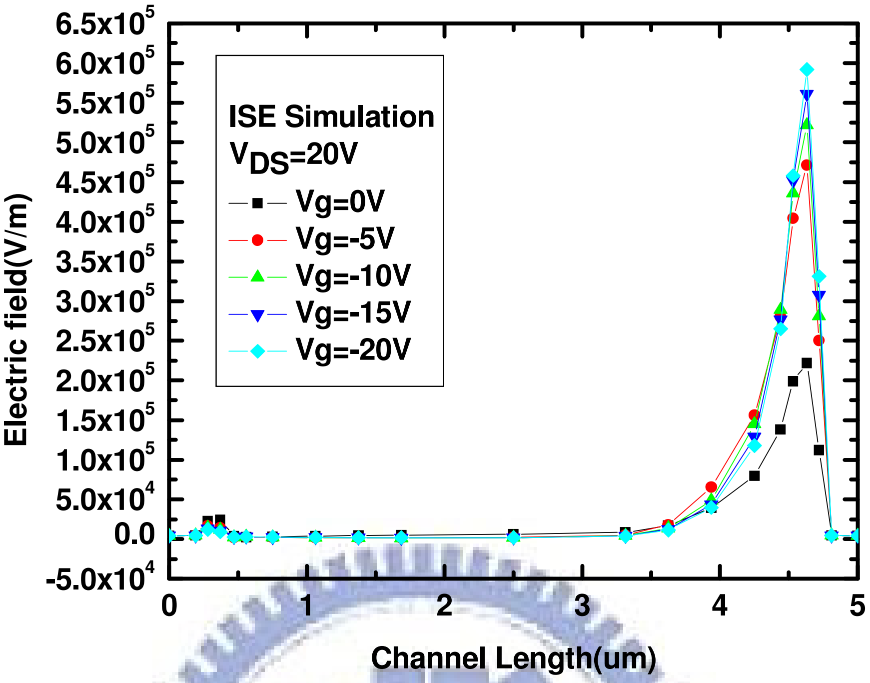


Figure 4-16 The electric field under various gate range AC stress with drain 20 V

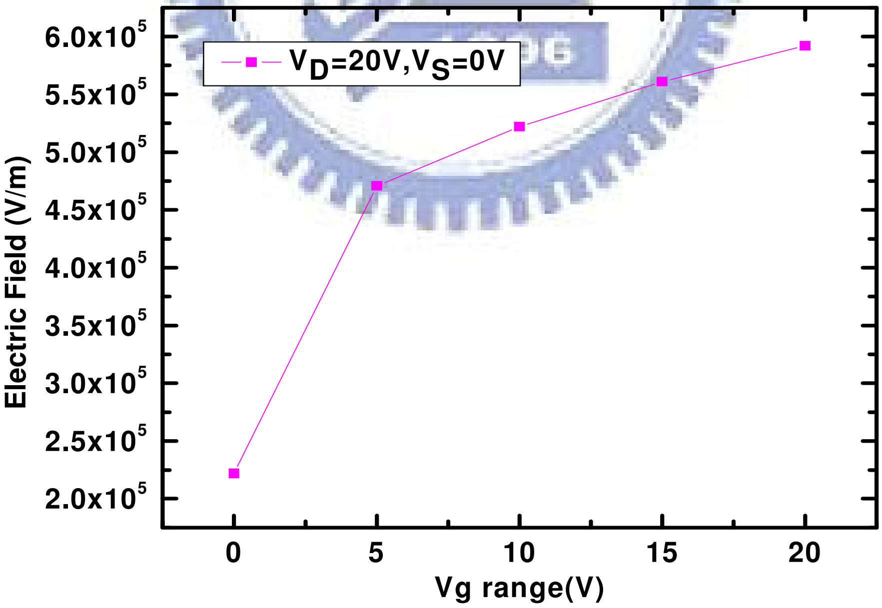


Figure 4-17 The highest electric field under various Vg voltage

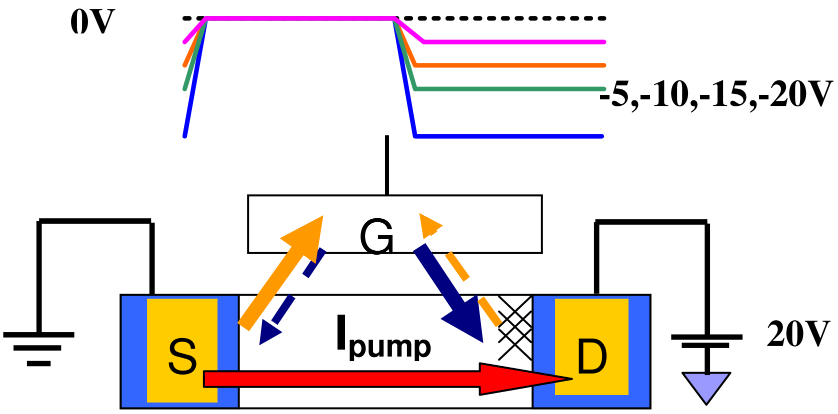


Figure 4-18 The pumped current measure under various gate pulse range

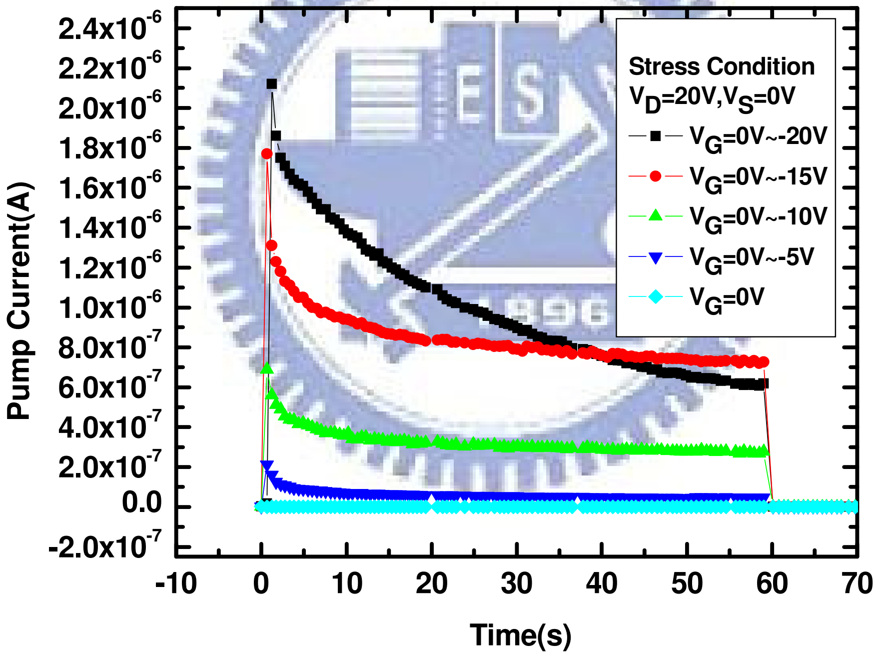


Figure 4-19 The measured DC drain current under various Vg range AC

gate stress with drain 20 V

CHAPTER5

Conclusions

For the gate AC stress in off region with DC drain bias, a serious degradation is observed. The effective drain current, pumped by the AC gate voltages in the off region, undergoes different electric field effects near the source and drain junctions and therefore results in different degradation behaviors near these two junctions. It is noticed that the degradation depends profoundly on the DC drain bias. It is also affected by the rising time Tr, falling time Tf, and the Vg range. This finding would be helpful in the understanding and evaluation of the device degradation mechanism and provide a guideline to design for reliability of poly-Si TFT circuit.

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碩士班論文題目：

N型複晶矽薄膜電晶體在閘極負電壓脈波汲極直流偏壓下的劣化研究

(Study of N-type Poly-Si TFTs Degradation Under Gate Pulse Stress in Off Region with Drain Bias)