國立交通大學
光電工程學系　　顯示科技研究所
碩士論文

五環素有機薄膜電晶體之可靠度分析

The DC/AC Reliability of Pentacene-based OTFT

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摘要

有機薄膜電晶體，因其具有低溫製程、低成本和製程簡單的優勢，所以有很好的潛力應用在如可撓曲式面板、感測器和RFID及其他的電子元件。近來的文獻及研究著重在DC gate bias stress without drain bias，而對於電子元件實際操作上， drain bias 及操作AC signal的研究比較缺乏。因此此論文將對於DC gate bias with drain bias stress 及AC bias stress做深入的研究。

首先，在DC gate bias stress without drain bias部分，ΔV_{th} 隨著時間的關係，符合Stretched-exponential equation，與現有的文獻一樣的結果。而當Drain bias施加後，ΔV_{th} 會隨V_D增加而減小，我們分析得到當V_D增加時，通道內載子濃度的減少，由於載子濃度與ΔV_{th} 成正比的關係，造成ΔV_{th} 的變小。因此我們對載子濃度歸一化後可得DC gate bias stress with drain bias中ΔV_{th} 隨時間的關係亦符合Stretched-exponential equation。

在AC stress部分，在同樣的duty ratio下ΔV_{th} 會隨著頻率越高ΔV_{th} 越小，我們分析發現pentacene本身的電容與電阻以及與金屬間的接觸電阻所等效的RC電路，造成通道內載子濃度因RC delay time隨著pulse width的變小而減少，使得ΔV_{th} 變小。同DC bias stress的部份，亦可對載子濃度歸一化後可得在AC bias stress中ΔV_{th} 隨時間的關係亦符合Stretched-exponential equation。

The DC/AC Reliability of pentacene-based OTFT structure

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Institute of Dispaly

National Chiao Tung University

Abstract

As organic thin film transistor has lots of advantage of low temperature fabrication、low cost and easy fabrication, it has good potential for application on flexible display、sensor、radio-frequency identification tags and other electronics. Although studies have been made on DC gate bias stress without drain bias, the drain bias and AC bias stress in actual operation of organic electronic device is unknown. So we focus on the study of DC gate bias with drain bias stress and AC bias stress in this thesis.

First, in the DC gate bias stress without drain bias, the dependence of the threshold voltage shift on the stressing time is found to follow a stretched-exponential function. It is the same as the many recent researchs. When the drain bias is applied, the threshold voltage shift will decrease and be suppressed as the drain bias becomes more negative. Since the threshold voltage shift is proportional to the carrier density, as the drain bias becomes more negative, the carrier concentration in channel is decrease such that the threshold voltage shift is reduced. Therefore, a channel charge normalization factor was used to describe the influence of drain bias and to modify the conventional stretched-exponential function.

The threshold voltage shift has strong frequency dependence-the higher frequency same duty ratio, the smaller the magnitude of threshold voltage shift. We used an simple RC equivalent circuit to simulate the device under negative pulsed bias stress. The RC circuit consists of the insulator capacitance C_i, pentacene capacitance C_s, and a effective pentacene resistance R_s for hole conduction and injection. Th effective channel carrier concentration considering the RC delay can successfully explain the dependence of threshold voltage shift on the pulse width of the stressing signal. The channel charge normalization also can be used as the DC bias effect modeto describe the influence of AC bias stress and to modify the conventional stretched-exponential function.

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Contents

Figure Captions

Chapter 1

Introduction

1-1. Introduction of Organic Thin Film Transistors (OTFTs)

Recently, organic thin-film transistors (OTFTs) have drawn lots of attentions due to their applications on the organic electronics, the radio-frequency identification tags, the electronic papers, and other electronics integrated with organic circuits have been proposed flexible displays [1] [2]. Within a few years, the performances of OTFTs had been improved to be comparable to or better than those of amorphous Si (a-Si) TFTs [3] [4]. Many reports have successfully demonstrated low temperature processes to fabricate low-voltage high-mobility OTFTs. A number of organic materials such as polythiophene, α- sexithiophene (α-6T) have been investigated for use in field effect transistors (FETs) . Polycrystalline molecular solids such as α-sexithiophene (α-6T) or amorphous/semi-crystalline polymers such as polythiophene or acenes such as pentacene, teracene show the highest mobilities[5]. Fig 1.1 shows the evolution of organic materials and the improvement in their mobilities over the years[6]. Pentacene based FETs show the high mobilities and have been extensively studied. Pentacene is made up of five benzene rings as shown in Fig. 1.2 Pentacene has a sublimation

temperature of 300℃. Well ordered pentacene films can be deposited at low temperatures making it suitable for deposition on plastic substrates. However, the reliability issues were still not comprehensively studied. When passivation layers were used to alleviate the device degradation due to the invasion of water vapor or oxygen in the air, the reliability issues under the gate and the drain biases require further investigations[7].

1-2. The reliability of organic thin film transistors

I t was observed in many reports that the performance of OTFTs degraded under gate bias stress[7] [8]. While the field-effect mobility and the subthreshold swing kept unchanged, threshold voltage shifted severely after the bias stress. The threshold voltage shift is found to be reversible, and is almost not dependent on the dielectric materials[9]. Therefore, the charge trapped in the dielectric layer should not be the reason. On the other hand, the creation of charged defect states in the organic semiconductor layer is proposed to be the underlying mechanism. Moreover, the dependence of the threshold voltage shift on the stressing time is found to follow a stretched-exponential function. It is the same as the bias stress effect in a-Si TFTs. In a-Si TFTs, the generation rate of charged defect is proportional to the

number of carriers, this is known as the defect-pool model[10]. In organic TFTs, J. E. Northrup et al. used density functional calculation to propose that the defect state generation is caused by hydrogen- and oxygen-related defects perturb a carbon atom so as to remove its p_z orbital from the π system and give rise to a state in the gap[11]. They proposed chemical equations to describe these reactions, in which the reaction rate was proportional to the carrier density. They also concluded that the reaction was relative to the bias stress effect.

1-3. Physical mechanism of bias stress effect

In twenty years ago, the reliability model of amorphous silicon thin film transistors had been studied. Researchers found that the reliability issue came from the threshold voltage (V_{th}) shift of devices. The characteristic of threshold voltage shift is the power-law time decay. Therefore the stretched exponential equation is used to describe this phenomenon[12]. The relaxation and dispersive transport of disorder system were often explained by the stretched exponential decay before it was used for describing the threshold voltage shift of amorphous silicon thin film transistors, and the proposed model is valid for any disorder material with a distribution of diffusion-site energy. In resent

experiment, organic material was adopted as the active layer of thin film transistors. Organic thin film transistors (OTFTs) are very potential to fabricate the radio-frequency identification tags, the electronic papers, and the flexible displays. The organic film often was deposited by evaporating or spinning. Therefore it is not prefect single crystal structure; it can be treated as a disorder system. In practice, bias stress effects also restrict the commercial application of OTFTs due to threshold voltage shift. It is interesting that the characteristic of threshold voltage shift is similar to amorphous silicon thin film transistors. Up to now, some studies pointed out that the threshold voltage shift is caused by the state creation and the state creation is governed by a dispersion process. Therefore, they thought that the stretched exponential equation is able to quantify OTFTs stability.

These proposed models described the threshold voltage shift very well, but there are only a few explanations on the micro process of defect generation. Recently the bipolaron mechanism is mentioned. The deep states slowly trap holes to form a bipolaron and the formation of bipolaron would cause the threshold voltage shift due to mobile hole decreasing. The reaction of bipolaron formation can represent.[13] [14].

$$h + h \rightarrow (hh)_{BP}$$

On the other hand,

$$2h^{+} + C_{22}H_{16} + C_{22}H_{14} \rightarrow 2(C_{22}H_{15})^{+}$$

and

$$2h^{+} + C_{22}H_{16}O + C_{22}H_{14} \rightarrow (C_{22}H_{15}O)^{+} + (C_{22}H_{15})^{+}$$

which is mentioned and the mechanism is based on density functional calculation. It is proposed that there are C-H_2, O_H, and C-HOH defects in organic semiconductors. These defects may be rise to the bias stress effect. We can find that their mechanisms proposed the defect creation be proportional to carrier concentration. On the defect generation phenomenon studies, the generation and quenching of defect in pentacene is obviously relative to hydrogen diffusion. They thought the relation may be suitable to other organic material[15].

As above mentions, the critical arguments proposed the defect creation rate is proportional to carrier concentration. Therefore, the stretched exponential equation may be verified by applying various drain bias during the gate bias stress. When the carrier concentration in channel was adjusted by various drain bias, the threshold voltage shift was obviously dependent on drain bias. If the data can be fitted very well by considering the channel charge normalization factor, it shows that the state creation rate is proportional to the carrier concentration. The phenomenon is only observed while state creation dominates the threshold voltage shift. Therefore, the main degradation

mechanism of pentacene-based TFTs is state creation which is demonstrated by the modified model.

1-4. Stretched-exponential Equation

The difference between charge trapping and state creation were explained clearly[10]. When charge trapping dominates, the threshold voltage shift is logarithmic, $\Delta V_{th} \sim r_d \, log\left(1+\frac{t}{t_0}\right)$. When state creation dominates, the threshold voltage shift is given by a power law, $\Delta V_{th} \sim a\left(\frac{t}{t_0}\right)^{\beta}$. And Powell also introduced the stretched-exponential equation $\left[V_G - V_{th}(t)\right] / \left[V_G - V_{th}(0)\right] = exp\left[\left(\frac{t}{t_0}\right)^{\beta}\right]$ from $\frac{dN_{DB}}{dt} \sim N_{WB}\frac{n_{BT}}{N_{BT}} D_0 t^{\beta}$. When the state creation is small, the stretched-exponential equation approximates to $\Delta V_{th} = (V_G - V_{th})\left(\frac{t}{t_0}\right)^{\beta}$. The state creation is small which means t_0 >> t. Charge trapping generally needs larger electrical field than state creation. Even t_0 >> t, state creation is still dominated at low electrical field. The stretched-exponential equation is valid to describe the characteristic of threshold voltage on pentacene based TFTs, and equation $\Delta V_{th} = (V_G - V_{th})\left(\frac{t}{t_0}\right)^{\beta}$ is used fitting the threshold voltage shift[16], when t_0 is much larger. In fact, the amorphous Silicon film is more stable than pentacene film. Therefore $\Delta V_{th} = (V_G - V_{th})\left(\frac{t}{t_0}\right)^{\beta}$ is suitable to fitting their data.

1-5. Motivation

Organic thin film transistor have many advantages, but only a few studies were published in reliability of bias stress. In order to understand, we will discuss under the following topics: DC bias effect and AC bias effect.

It will begin our discussion by considering the DC bias effect inevitably related to the AC bias effect. Thus, we analyze dividedly the gate bias effect with and without drain bias. Because lots of applications of electronic device are operated on different frequency, reliability of organic thin film transistors under AC bias stress is needed to study. So we design experimental condition about frequency and base voltage of pulse.

1-6. Thesis Organization

In Chapter 1, we describe the introduction of OTFTs, Physical mechanism of bias stress effect, and motivation of the thesis. In Chapter 2, we introduce the transportation mechanisms of organic semiconductor, operation of OTFTs, and parameter extraction. In Chapter 3, the fabrication and the structure of OTFTs are presented. In Chapter 4, gate bias stress effect without drain bias effect, and gate bias stress effect with drain bias effect. In Chapter 5,

frequency effect, AC reliability model, and pulse design. Finally, we describe the conclusion in Chapter 6.

Chapter 2

DEVICES FABRICATION

2-1. Transportation Mechanisms of Organic Semiconductor

Over the past few years, Carrier transportation in the organic semiconductors have been investigated on the theory and modeling[17]. In the conventional silicon-based semiconductors, carrier transport occurs in delocalized states. However, in the organic materials, carrier transport occurs by hopping of charges between localized states. Organic semiconductors are conjugated materials, where the π-electrons are conducted intra the molecular. Its crystalline is formed by relatively weak Van der Waals interaction between molecules, where the molecular-stacking determines the carrier behavior. There are two major model : “The band-transport model” and “The hopping models” to describe the hopping transport. Band transport should not be suitable for some disordered organic semiconductors, in which carrier transport is govern by the hopping between localized states. Hopping is assisted by phonons and the mobility increases with temperature. Typically, the mobility is very low, usually much lower than 1cm^2/V-sec. The boundary between the localized and delocalized processes is taken at a mobility

between 0.1 and 1 cm^2/V-sec[18]. Lots of polycrystalline organic semiconductors, including pentacene, rubrene, have room temperature mobility over the boundary[19]. But, temperature-independent mobility was found in some polycrystalline pentacene devices[20]. Therefore, this research indicate that the the whole carrier transport behaviors in high performance polycrystalline pentacene film for such thermal activated hopping process remains a matter to be discussed further. The coherent band-like transport of delocalized carriers becomes the prevalent transport-mechanism in the single crystals of organic semiconductors under the low-temperature environments. The very high hole mobility values have been measured by time-of-flight experiments[21]. Thus, the temperature dependence mobility was found below 100K and following with a power law of $\mu \propto T^{-n}$, n~1, in single crystals of organic semiconductors, consistent with the band-transport model[22]. However, between 100K and 300K, the carrier mobility show a constant value, that has been described as the superposition of two independent carrier transport mechanisms. The first carrier transport mechanism is small molecular polaron. It is formed as a result of interaction of a charge carrier with the intramolecular vibrations of the molecule, on which it is localized during the residence time, with the intramolecular vibrational modes of nearest-neighbour molecules, and move coherently via tunneling. In this small molecular polaron

mechanism, the mobility follows the power law $u = aT^{-n}$. The other mechanism is a small lattice polaron, which transport by thermally activated hopping and follow a typical exponential dependence of mobility on temperature law: $u = b\exp(-E_a / kT)$. The superposition of these two mechanisms has a good results with experimenta of temperature-dependence mobility from room temperature[23]. However, the charge carrier transport in organic molecular crystals is still not well-understood. There is still room for analyzing[24].

2-2. Operation of Organic thin film transistor

There are four basic elements: (i) semiconductor film; (ii) insulating layer; and (iii) source and drain electrode (iv) gate electrode; to be composed a thin film transistor. Actually, the general operation concepts are originated from MOSFET theory. In conventional inorganic thin film transistor, most devices are operated in inversion mode. However, the operation of organic thin film transistor is generally in accumulation mode . The Fermi level of gold and HOMO-LUMO levels of pentacene are shown in Fig. 2-1. When a positive voltage is applied to the gate, the Fermi level of gold is far away from the LUMO level, so that electron injection is very unlikely. therefore, no current

passes through the pentacene layer, and the small measured current essentially comes from leaks through the insulating layer. When the negative voltage is applied to the gate, positive charges are induced in the channel, holes can be injected easily from the source to the semiconductor, because the Fermi level of gold is close to the HOMO level of pentacene. Accordingly, pentacene is said to be a p-type organic semiconductor. However, it need to indicate that this concept differs from conventional semiconductors, which can be made either n-type or p-type by doping mechanism. Symmetrically, an organic semiconductor will be said either n-type or p-type by work function of source is close to HOMO level or LUMO level. The insulator serves as a capacitance per unit area which stores charges and can be represented as C_{OX}, then the accumulated charge per unit area is about $V_G C_i$. Additionally, assuming that a negligibly small voltage, V_{th}, is dropped across the semiconductor. In this situation, the applied drain bias can drive the current from source to drain. The conduction is determined by the mobility which represents the driving ability of the electrical field on the accumulated charges.

In general, It is divide the operation of organic into two regions, linear and saturation regions. The drain current in the linear region is determined from the following equation:

$$I_D = \frac{W}{L} C_{OX} \mu (V_G - V_{TH} - \frac{V_D}{2}) V_D$$

where W and L corresponds to the channel width and length,respectively.

Since the drain voltage is quite small, sometimes equation can be simplified as

$$I_D = \frac{W}{L} C_{OX} \mu (V_G - V_{TH}) V_D$$

For $-V_D > -(V_G - V_{TH})$, I_D tends to saturate due to the pinch-off of the accumulation layer. The current equation is modified as:

$$I_D = \frac{W}{2L} C_{OX} \mu (V_G - V_{TH})^2$$

2-3. Parameter Extraction

2-3-1. Mobility

In the linear region, mobility can be extracted from the transconductance maximu m g_m:

$$g_m = \left[\frac{\partial I_D}{\partial V_G} \right]_{V_D = constant} = \frac{WC_{OX}}{L} \mu V_D$$

In the saturation region, Mobility can also be extracted from the slope of the curve of the square-root of drain current versus the gate voltage:

$$\sqrt{I_D} = \sqrt{\frac{W}{2L} \mu C_{OX}} (V_G - V_{TH})$$

2-3-2. Threshold voltage

In the linear region, threshold voltage can be extracted from the current equation of linear region: The intersection point of the drain current versus gate voltage minus 1/2 drain voltage when the device is in the linear mode operation.

In the linear region, threshold voltage can be extracted from the current equation of saturation region:

The intersection point of the square-root of drain current versus gate voltage when the device is in the saturation mode operation.

2-3-3. Subthreshod swing

Subthreshold can also be extracted from

$$S = \frac{\partial V_G}{\partial(\log I_D)}\bigg|_{V_D=\text{constant}}$$, when $V_G < V_{th}$ for p-type.

Chapter 3

Fabrication of OTFTs

The devices used in this series of experiments are the top contact (TC) structure, which means the organic semiconductor layer is deposited on the bottom of the contact electrodes. Below the following sections, we would detail introduce the process of different structures:

Step1. Substrate and gate electrode

4-inch P-type heavily-doped single crystal silicon wafer (100) was used as the substrate and the gate electrode.

Step2. Gate dielectric formation

After the initial RCA cleaning, the 1000Å thermally grown SiO_2 layer was deposited in furnace.

Step3. Pentacene film deposition through the shadow mask[25,26]

The pentacene material obtained from Aldrich without any purification was directly placed in the thermal coater for the deposition. It is well known that

the deposition pressure, deposition rate, and deposition temperature are the three critical parameters to the quality of the organic film. The deposition is started at the pressure around 3×10^{-6}torr. The deposition rate is controlled at ~0.5Å/sec and the thickness of pentacene film was about 1000Å, monitored by the quartz crystal oscillator. Stable deposition rate is expected to result in smoother and better ordering of the organic molecules. The deposition temperature is also a factor influencing the pentacene film formation. The temperature we use in depositing pentacene films is 70 ^{o}C. We use shadow mask to define the active region of each device.

Step4. Source/Drain deposition through the shadow mask[26]

The injection barrier of the OTFT device is determined by the materials of the source and drain electrodes. Materials with large work function are preferred to form Ohmic contact. The Au with work function ~5.1eV does help to provide a better injection. We used shadow mask to define top contact of each device. The top electrodes were Au. Au was deposited on the active layer by ULVAC thermal coater at deposition pressure 3×10^{-6} torr. The thicknesses of the metal layer were 1000Å.

In this study, all the measured data were obtained from the semiconductor parameter analyzer (HP 4156A) in the darks at room temperature. And we measure the OTFTs immediately when the samples were unloaded from the evaporation chamber.

Chapter 4

DC BIAS EFFECT

Fig. 4-1 shows the cross-section of the conventional top-contact pentacene-based OTFTs used in this study Firstly, 100-nm-thick thermal oxide was grown on heavily doped Si wafers to serve as the gate dielectric. Then, pentacene obtained from Aldrich without any purification was evaporated through shadow mask onto the thermal oxide to form the active layer. The deposition rate was controlled at 0.5Å/s while the substrate temperature was kept as 70°C. After the formation of 100-nm-thick pentacene, 100-nm-thick gold was deposited through the shadow mask to form the source/drain contacts. The device channel width and length were defined as 1000 μm and 600 μm, respectively. Two series of bias-stress measurements were performed: one with zero drain bias and various gate biases and the other with a fixed gate bias and different drain biases.

4-1. Only VG bias, no VD bias

4-1-1. Bias-stress effect

Firstly, we analyze the Bias stress effect with zero drain bias. The linear-region transfer characteristics of the devices before stress and after 2000-sec stress are depicted in Fig. 4-2. With source and drain connected to ground, negative gate biase were used as the stress conditions (V_{DS} = 0 V, $V_G - V_{th}^{ini}$ = -15V), where V_{th}^{ini} is the initial threshold voltage). The negative gate-bias stress causes a shift of the transfer characteristics while the subthreshold swing stays almost unchanged. The threshold voltage V_{th} , subthreshold swing and the field-effect mobility μ_{FE} as a function of stress time are shown in Fig. 4-3 and Fig. 4-4, respectively. Apparently μ_{FE} is not affected by the stress, while V_{th} is drastically changed[27] [28]. Such a phenomenon is often believed to be caused by the generation of deep states with long discharge time that degrade V_{th}. The shallow traps that would affect μ_{FE} may not be changed by the gate bias stress . The power-law dependence between the threshold voltage shift and the stress time is also found in Fig. 4-5. This can be explained by the approximation of the OTFT BSE model, in which the stretched exponential function reduces to the simple power-law function when the stress time is much less than the effective trapping time τ. when the stretched exponential function is used, the dispersion parameter β can be

obtained by plotting $\log\left\{-\ln\left[1-\Delta V_T/(V_{GS}-V_T^{ini})\right]\right\}$ as a function of log(t) shown in Fig. 4-6. After extracting β = 0.283 and defining the attempt to escape frequency ν = 10^5 Hz, the effective trapping time τ and the mean activation energy for the defect generation E_A can be determined by fitting ΔV_T with the stretched exponential function shown in Fig. 4-7 . The resulting E_A is 0.57 eV and τ is 36127 sec at room temperature.

4-1-2. Recovery

Devices subjected to bias stress recover to their original state within a few hours when left in the dark shown in Fig. 4-8 and at the end of the recovery process, the transfer characteristic is essentially identical to that of the unstressed state. The cycle of stress and recovery was repeated with no any change in behavior. Even though the recovery mechanism is still not clearly understood, recombination of the trapped holes with free electrons is proposed to be a plausible reason[29].

4-1-3. Influence of positive VG bias on stress and recovery

Under the same condition as negative gate stress, The stress gate voltage changes to +6V. Because of the presence of pentacene layer at the

source/drain contacts, only the hole conduction characteristics are observed. The characteristics have positive shifts under +6V Bias stress. The evolution of the threshold voltage shift extracted from the curve is shown in Fig. 4-9.As shown in Fig. 4-10, the recovery curves of two identical OTFTs after stress are compared. When the positive gate bias (V_{GS} = +4V) is added to induce electrons, the recovery of the device is faster than that of the device without positive gate bias. At the 1000s, the threshold voltage shift over the original value become positive under the +4V gate bias and with the discussion in the early part of this section, these results lead us to the conclusion that the positive gate bias not just increase the recovery also include the positive bias effect. This means that electrons can be used to remove defect states or more negative defect states are generated to compensate the threshold voltage shift[29].

4-2. Fix VG bias stress, various VD bias stress

4-2-1. stress under different VD

Then, different drain biases (V_{DS} = 0 V, -5 V, -10 V, and -15 V) were added to the bias-stress measurement while the gate bias was fixed as $V_G - V_{th}^{ini}$ = -15 V. The μ_{FE} and the subthreshold swing extracted from devices with different stress conditions are plotted as a function of stress time in Fig. 4-11.

Unchanged μ_{FE} and subthreshold are observed, and consequently the influence of drain-bias stress on the shallow traps can be excluded. The influence of drain-bias stress on the V_{th}, however, is significant. As shown in Fig. 4-12, the threshold voltage shift ΔV_{th} is suppressed when the drain bias becomes more negative. All the relationships depicted in Fig. 4-13 follow the power-law dependence with identical slope. According to the BSE model, the slope represents the dispersion parameter β that influences the relaxation and the dispersive transport of disorder system. Identical β value implies that the microscopic processes of the state creation such as the impurity diffusion or the defect creation kinetics should be independent of the drain bias. The influence of drain bias on the carrier concentration is believed, as in a-Si TFTs, to be the dominant reason that causes the ΔV_{th} to be dependent on V_{DS}.

To quantitatively discuss this relationship, for a given V_{GS}, we define the relative threshold voltage shift ΔV_T^{rel} as the ratio between the ΔV_{th} with various V_{DS} stress and the ΔV_{th} with zero drain-bias stress. Since the defect generation rate is proportional to the carrier density, the influence of drain bias on the carrier density in the accumulation channel should be considered. For simplicity, the channel charge normalization factor (Q_{G0}/Q_G) proposed is used[16]. As a result, Stretched-exponential equation is modified as:

$$\Delta V_T \times \frac{Q_{G0}}{Q_G} = (V_G - V_T^{ini})\left\{1 - \exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]\right\}$$

where Q_{G0} and Q_G are expressed as:

$$Q_{G0} = C_G \times W \times L\left(V_G - V_T\right)$$

$$Q_G = \frac{2}{3} C_G \times W \times L \frac{\left(V_{GS} - V_T\right)^3 - \left(V_{GD} - V_T\right)^3}{\left(V_{GS} - V_T\right)^2 - \left(V_{GD} - V_T\right)^2}$$

The calculated normalized channel charge is defined Q_G/Q_{G0} , where Q_G is the channel charge when V_D is varied and Q_{G0} is the channel charge when V_{DS} = 0V. Good agreement can be observed between ΔV_T^{rel} and the calculated Q_G/Q_{G0} curve. The result verifies the proportionate relationship between the defect creation rate and the carrier concentration. Also, the result suggests that convergent data can be obtained by plotting the restored threshold voltage shift $\Delta V_T^{res} = (Q_{G0}/Q_G)\Delta V_{th}$ as a function of stress time as shown in Fig. 4-14. The restored threshold voltage shift ΔV_T^{res} excludes the drain bias effect and can be used to extract the parameters associated with the defect creation kinetics. For example, when the stretched exponential function is used, the dispersion parameter β can be obtained by plotting $\log\left\{-\ln\left[1 - \Delta V_T^{res}/(V_{GS} - V_T^{ini})\right]\right\}$ as a function of log(t) in the inset of Fig. 4-14. After extracting β = 0.283 and defining the attempt to escape frequency $\nu = 10^5$ Hz, the effective trapping time τ and the mean activation energy for the defect generation E_A can be determined by fitting ΔV_T^{res} with the stretched

exponential function. The resulting E_A is 0.57 eV and τ is 36127 sec at room temperature.

4-2-2. Recovery with VD

Finally, the drain bias effect on the threshold voltage recovery is addressed. It is expected that the positive drain bias reduces the electron amount and suppresses the recovery rate. As shown in Fig. 4-15, the recovery curves of two identical OTFTs after stress are compared. When the same positive gate bias (V_{GS} = 4V) is added to induce electrons, the recovery of the device without the drain bias is faster than that of the device with a positive drain bias (V_{DS} = 4V). This result gives an insight of the recovery mechanism; though a comprehensive understanding should be carefully studied in future work.

Chapter 5

AC BIAS STRESS EFFECT

The AC signal used in this study consists of signal amplitudes, frequencies, and duty ratios. We can adjust these parameters and then perform various stress conditions on the gate electrode to realize the instability of Pentacene-based TFTs under different swing regions. Fig. 5-1 shows the waveform of the AC signal. In AC signal, the definition of individual parameter is give as follow:

$t_c = t_p + t_b$ (1)

$f = 1/t_c$ (2)

$D.R. = t_p/t_c$ (3)

Where t_c is the signal period, f is the signal frequency and D.R. is the duty ratio.

In the waveform of AC signal, V_P is the defined as the peak voltage, while V_b is defined as the base voltage. The frequency (f) is equal to $1/t_c$, where the t_c is the signal period and the duty ratio is defined a eq. (3). The t_p is the time of peak voltage and the t_b is the time of base voltage. Effective stress time is the sum of tp. Falling time and rising time are not considered in here because they are very smaller than signal period.

5-1. Frequency effect

Fig. 5-2 show the evolution of I_D-V_G characteristics during negative pulsed bias stress with a duty-cycle of 50% and gate bias pulse width of 2.5ms after effective stress time 2000s at room temperature. The negative pulsed gate bias stress causes a shift of the transfer characteristics while the subthreshold swing and field-effect mobility μ_{FE} stays almost unchanged similar with DC bias stress effect. The threshold voltage V_{th} , subthreshold swing and the field-effect mobility μ_{FE} as a function of stress time are shown in Fig. 5-3 and Fig. 5-4, respectively. Fig. 5-5 shows the threshold voltage shift versus effective stress time under negative pulse bias stress for different pulse conditions. The effective stress time is the accumulated time when the gate voltage is high(ON). Threshold voltage shift has strong frequency dependence-the higher frequency, the smaller the magnitude of threshold voltage shift. There are two possible reasons to explain the phenomenon. (1) OFF region: The state creation defects were recovered during OFF cycle region. (2) ON region: The effective concentration dominates the pulsed bias stress dependence of threshold voltage shift.

5-2. AC reliability model

5-2-1. off-cycle effect

Because the recovery rate of defects in pentacene is faster than defects in amorphous silicon, the effect of OFF cycle region must be considered. In section 4-1-2 shows the threshold voltage shift decreases fast after removing the bias stress. In order to demonstrate recovery effect, the fixed ON region combine various OFF region to form various duty cycle. Fig. 5-6 shows the threshold voltage shift do not dependent on the OFF region.

5-2-2. Equivalent circuit

In order to analyze the apparent pulse width dependent threshold voltage shift for negative pulsed bias stress effect, we used an simple RC equivalent circuit to simulate the device under negative pulsed bias stress. The RC circuit consists of the insulator capacitance C_i, pentacene capacitance C_s, and a effective pentacene resistance R_s for hole conduction and injection, as shown in Fig. 5-7. After applying a gate pulse with amplitude V_{ST} is expressed as[30] [31]

$$V_i(t^*) = V_{ST}[1 - \frac{C_i}{C_i + C_s}\exp(-\frac{t^*}{\tau_{RC}})]$$

where $\tau_{RC} = R_s C_s$ represents the effective time constant of hole

accumulation along the pentacene/oxide interface. The accumulated hole concentration along the pentacene/oxide interface can be expressed as $N_{accum} = -N_i + N_s$ where $N_i=C_iV_i/q$, $N_s=C_sV_s/q$ .And by $V_{ST}=V_i+V_s$ we can derive

$$N = -Ni + Ns = \frac{1}{q}(-C_i V_i + C_s V_s) = \frac{1}{q}[-C_i V_i + C_s (V_{ST} - V_i)]$$

$$\Rightarrow N = \frac{1}{q}\{C_s V_{ST} + (C_s + C_i)(-V_{ST})[1 - \frac{C_i}{C_i + C_s}\exp(-\frac{t^*}{\tau_{RC}})]\}$$

$$= \frac{1}{q}[C_s V_{ST} - V_{ST}(C_s + C_i) + C_i \exp(-\frac{t^*}{\tau_{RC}})]$$

$$= \frac{C_i V_{ST}}{q}[\exp(-\frac{t^*}{\tau_{RC}}) - 1]$$

The average accumulated hole concentration, N_{AC} during a pulse width time can be expressed as

$$N_{AC} = \frac{1}{PW}\int_0^{PW} N(t^*)dt^* = N_{DC}[1 - \frac{\tau_{RC}}{PW} + \frac{\tau_{RC}}{PW}\exp(-\frac{PW}{\tau_{RC}})]$$

Where N_{DC} is the accumulated hole concentration under DC gate bias stress. According to the section 4-2-1, the threshold voltage shift under the negative bias stress is proportional the carrier concentration, the relationship between DC stress and AC stress induced the threshold voltage shift with the same effective stress time can be expressed as

$$\frac{\Delta V_T^{AC}}{\Delta V_T^{DC}} = 1 - \frac{\tau_{RC}}{PW} + \frac{\tau_{RC}}{PW}\exp(-\frac{PW}{\tau_{RC}})$$

where ΔV_{th}^{AC} and ΔV_{th}^{DC} are threshold voltage shift by AC stress and DC stress, respectively.

5-2-3. pulse width effect

The degree of threshold voltage shift is decided by ON region. If off region do not affect the dependent, the on region decide the direct. Section 5-2-2 used effective carrier model to explain the threshold voltage shift decreasing with pulse width increasing. Fig. 5-8 shows the experiment threshold voltage and theoretical curve as a function of pulse width at effective stress time of 2000s , $\tau_{RC} \fallingdotseq$ 15us per unit area for 100nm thick pentacene. This result discussed the threshold voltage shift under various pulse width along with the pulsed gate bias stress when the defect creation was the dominant mechanism. Similar to the DC bias stress model, the defect generation rate in AC bias stress was proportional to the carrier density. Therefore, a effective channel carrier normalization factor was used to describe the pulse width effect and to modify the conventional stretched-exponential function. Good agreement was achieved between the theoretical equation and the experimental results.

5-3. Pulse design

5-3-1. Off-state bias stress effect

In order to examine the Vb adjustment effect of the bipolar bias stress,it will be useful to analyze the positive pulsed bias stress. The Fig. 5-9 shows

that the time dependence of the threshold voltage shift which caused by the positive AC stress compared with positive DC bias stress. For positive pulse bias stress, the threshold voltage shifts are significant smaller in comparison with threshold voltage shift induced by positive DC gate bias stress. This result can be explained by considering the characteristic of pentacene-based TFTs. Au was used as drain and source on pentacene layer. The Fig. 2-1 shows the work function of Au is near the LOMO band of pentacene. When the positive bias was applied, the interface of Au/pentacene would induce a large barrier to impede electron injection. During positive AC bias stress, the on region time of period is effective time to accumulate electrons. The interface barrier makes a huge barrier to induce huge RC delay time generation. Although electrons are easily to cause defects, there is not enough time to accumulate electrons.

5-3-2. Vb adjustment

F ig. 3-10 shows the threshold voltage shift induced by negative ($V_G - V_{th}^{ini}$ = -20V) pulsed bias stress and bipolar pulsed bias stress by various base voltage of negative ($V_G - V_{th}^{ini}$ = -20V) and positive (V_b = +6V, +8V, +10V) with the same 50% duty cycle and 2.5ms pulse width. The threshold voltage shift of bipolar pulse bias stress with V_b=+6V is slightly small than that for negative pulsed bias stress but depend apparently on magnitude of base voltage. In

section 5-3-1, it was pointed out that the threshold voltage shifts of positive pulsed bias stress are significant smaller in comparison with threshold voltage shift induced by positive DC gate bias stress, but actually have small shift. Therefore, it seems reasonable to conclude that the threshold voltage shift of bipolar pulsed bias stress is combined the effect of negative and positive pulsed bias stress together.

5-3-3. frequency adjustment

With various pulse width (2.5ms, 100us, 50us), the threshold voltage shift induced by negative ($V_G - V_{th}^{ini}$ = -20V) pulsed bias stress and bipolar pulsed bias stress of negative ($V_G - V_{th}^{ini}$ = -20V) and positive (V_b = +8V) are shown in Fig. 5-11, Fig. 5-12 and Fig. 5-13, respectively. The threshold voltage shift of bipolar pulse bias stress with V_b=+8V is small than that for negative pulsed bias stress with different pulse width. This result provided one more evidence for that the threshold voltage shift of bipolar pulsed bias stress is combined the effect of negative and positive pulsed bias stress together.

Chapter 6

CONCLUTION

6-1. DC bias effect

This chapter discussed the threshold voltage shift under various drain biases along with the gate bias stress when the defect creation was the dominant mechanism. Similar to the defect pool model in a-Si TFTs, the defect generation rate in OTFTs was proportional to the carrier density. Therefore, a channel charge normalization factor was used to describe the influence of drain bias and to modify the conventional stretched-exponential function. Good agreement was achieved between the modified equation and the experimental results.

6-2. AC bias effect

The instability of OTFTs under various AC biases was investigated. Firstly, the state creation governed by the defect pool model is found to be dominant under the bias stress. Calculating the effective channel carrier concentration considering the RC delay can successfully explain the dependence of threshold voltage shift on the frequency or on the pulse width of the stressing signal. It was also found that in AC stress, only holes contribute

to defect creation, electrons may not exist due to their large charging time through the high injection barrier. Finally, by changing the base voltage in the AC stressing signal, the threshold voltage shift can be modified since the effect of negative and positive pulsed bias stress together.

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Figures

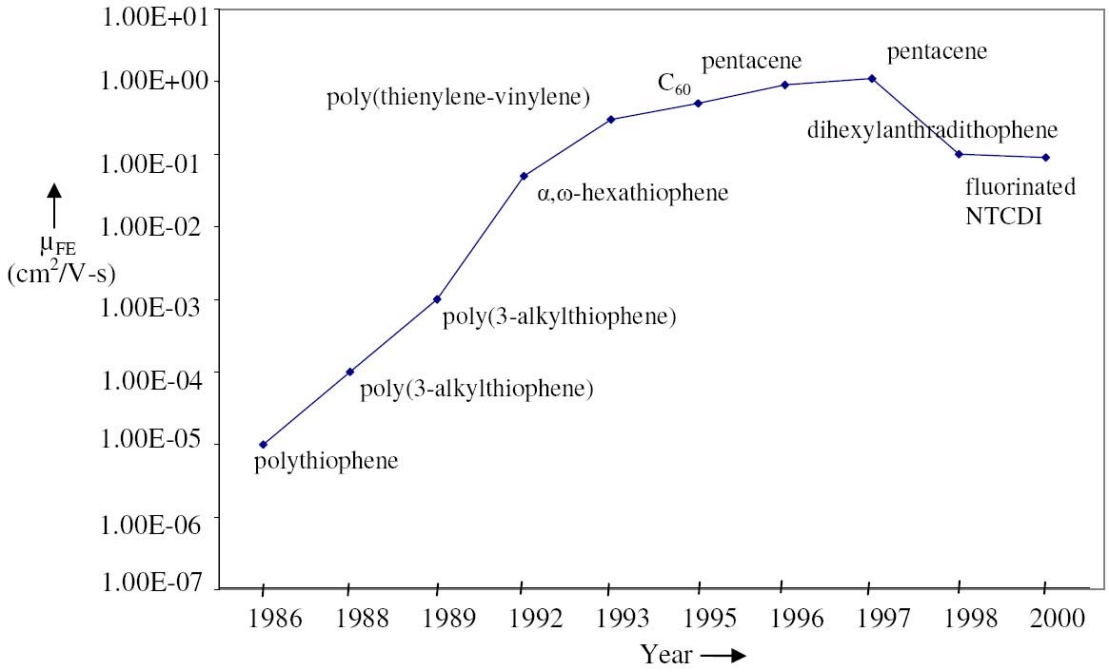

Fig. 1.1. Semilogarithmic plot of mobility vs.year.

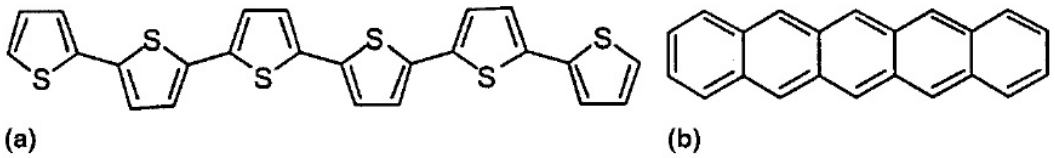

Fig. 1.2 Molecular structure of (a) sexithiophene and (b) pentacene.

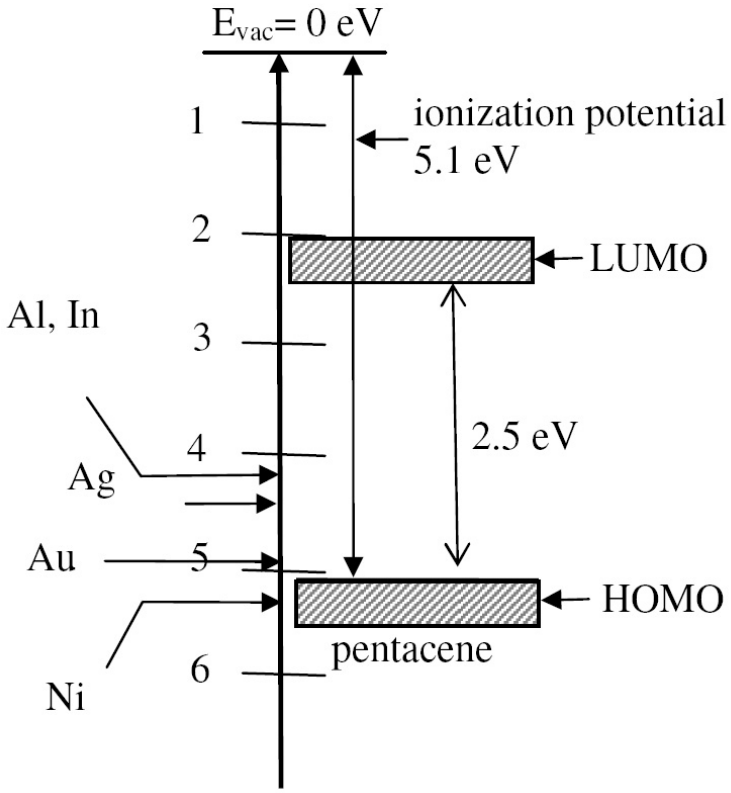

Fig. 2-1 Work function of various metals and ionization potential of pentacene.

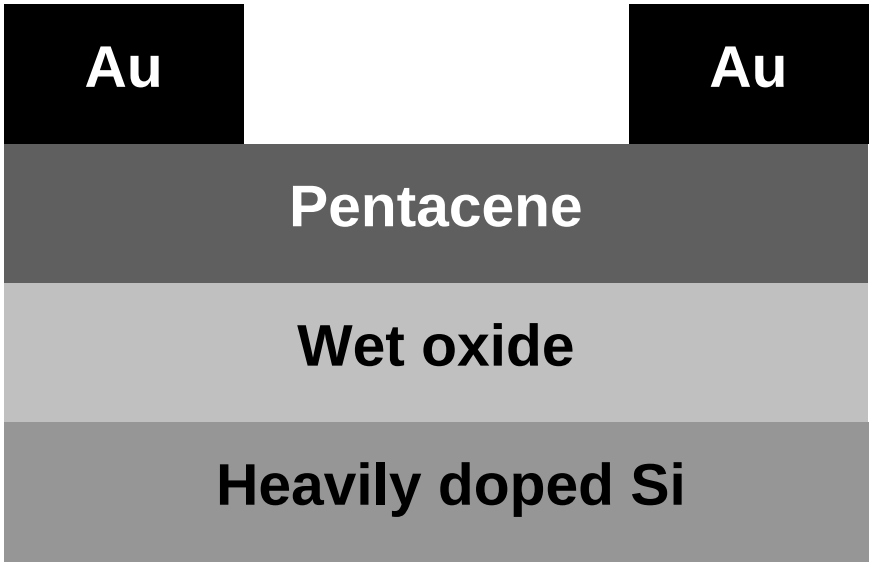

Fig. 4-1 Conventional top-contact pentacene-based OTFTs

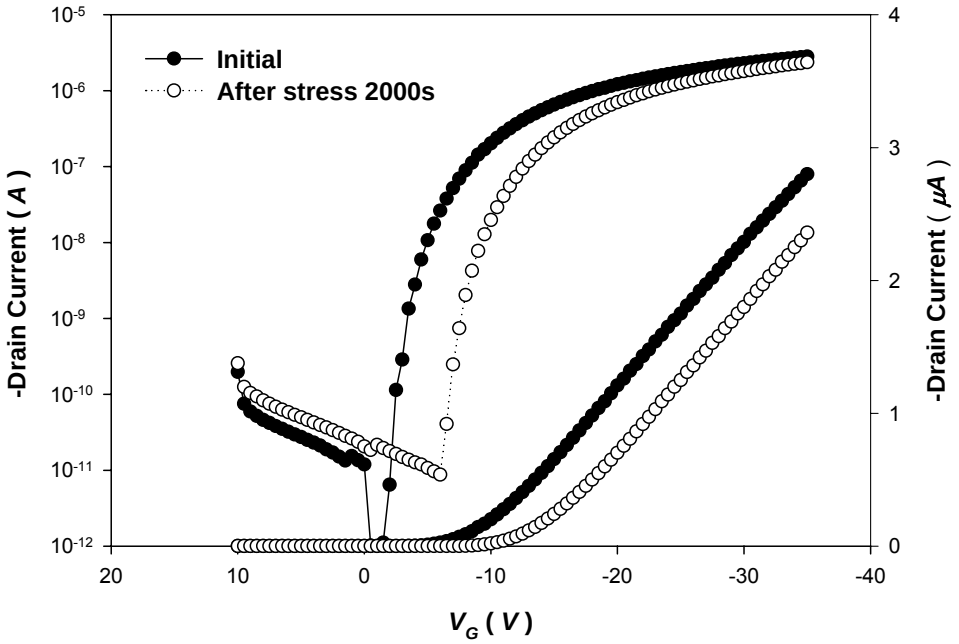

Fig. 4-2 The linear-region transfer characteristics of the devices before stress and after 2000-sec stress

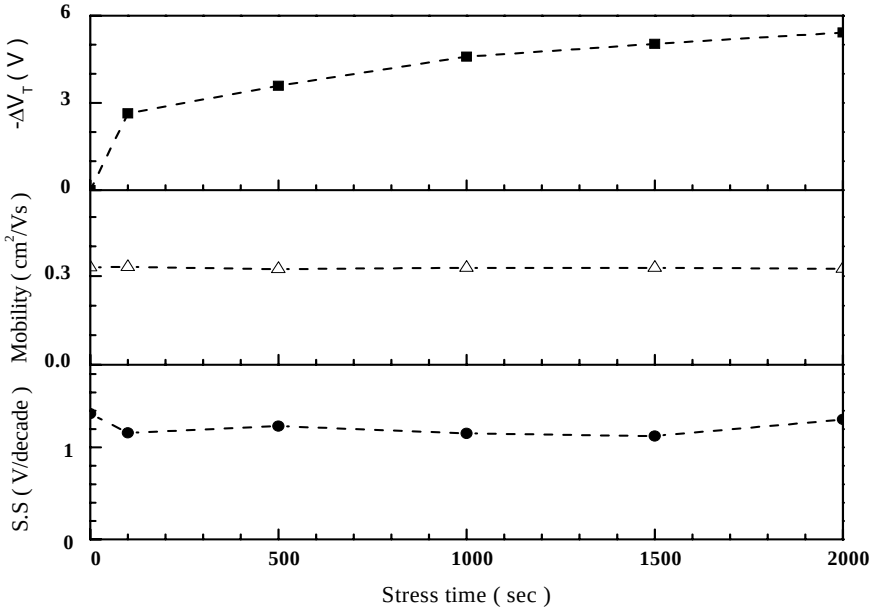

Fig. 4-3 The threshold voltage shift, subthreshold swing and the field-effect mobility

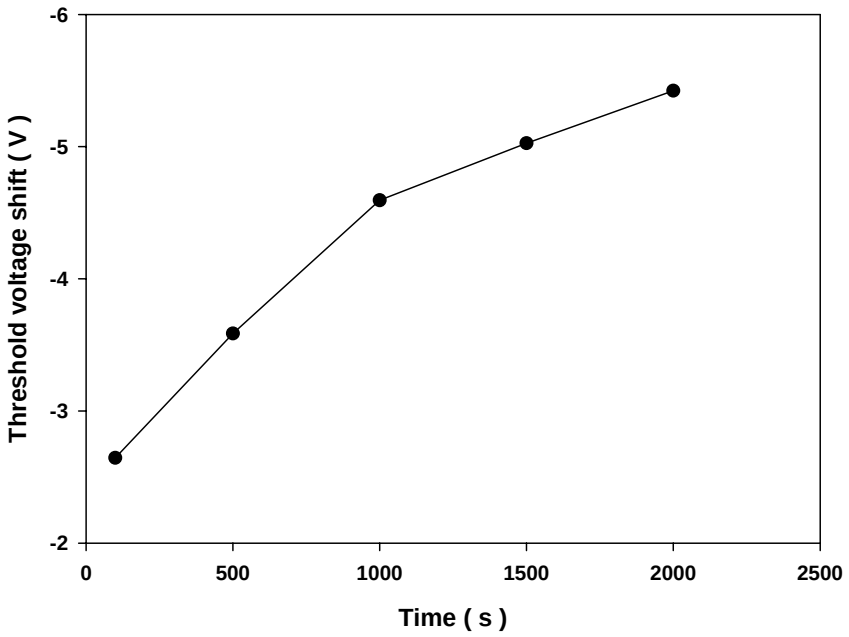

Fig. 4-4 The threshold voltage shift as a function of stress time on a linear scale

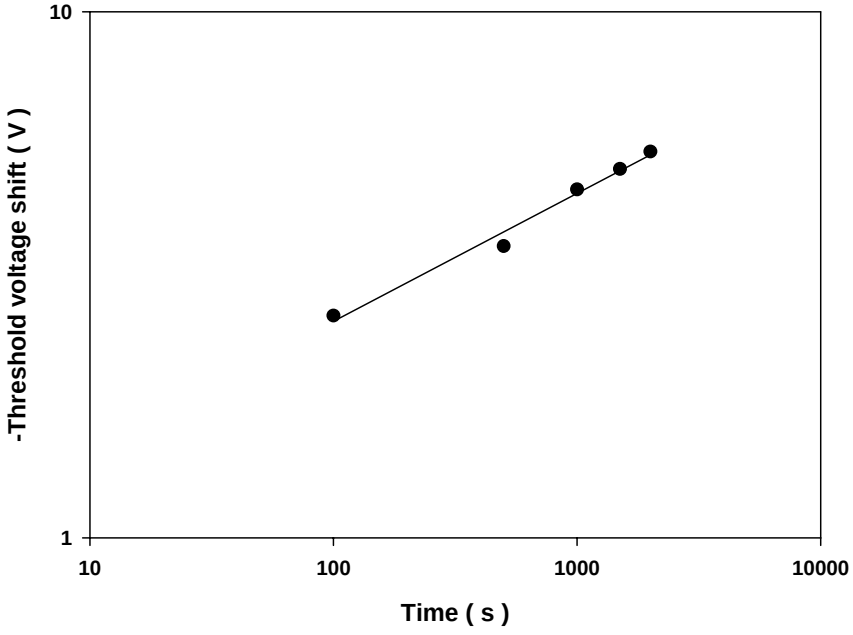

Fig. 4-5 The threshold voltage shift as a function of stress time on a logarithmic scale

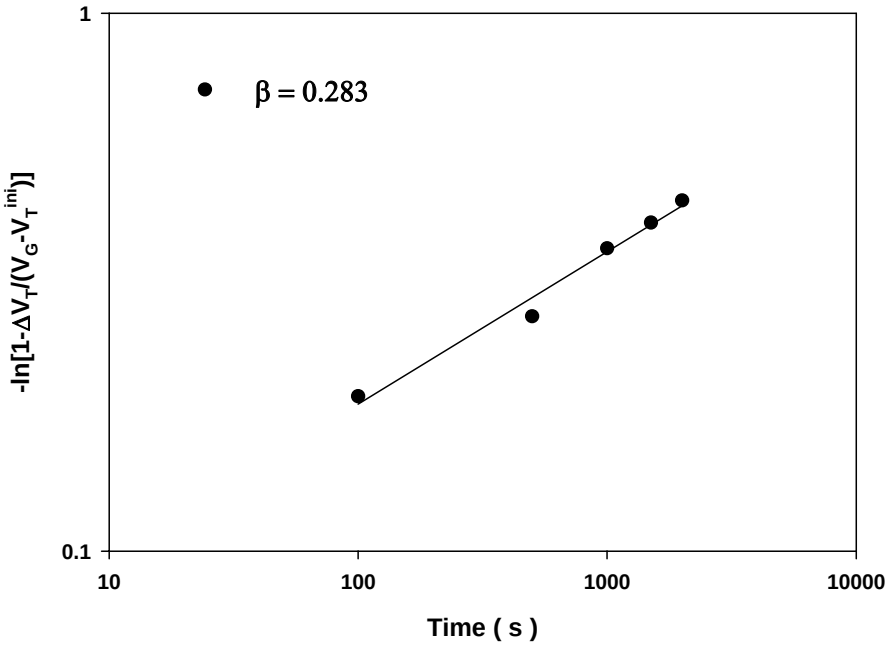

Fig. 4-6 The dispersion parameter β obtained by plotting $\log\left\{-\ln\left[1-\Delta V_T/(V_{GS}-V_T^{ini})\right]\right\}$ as a function of log(t)

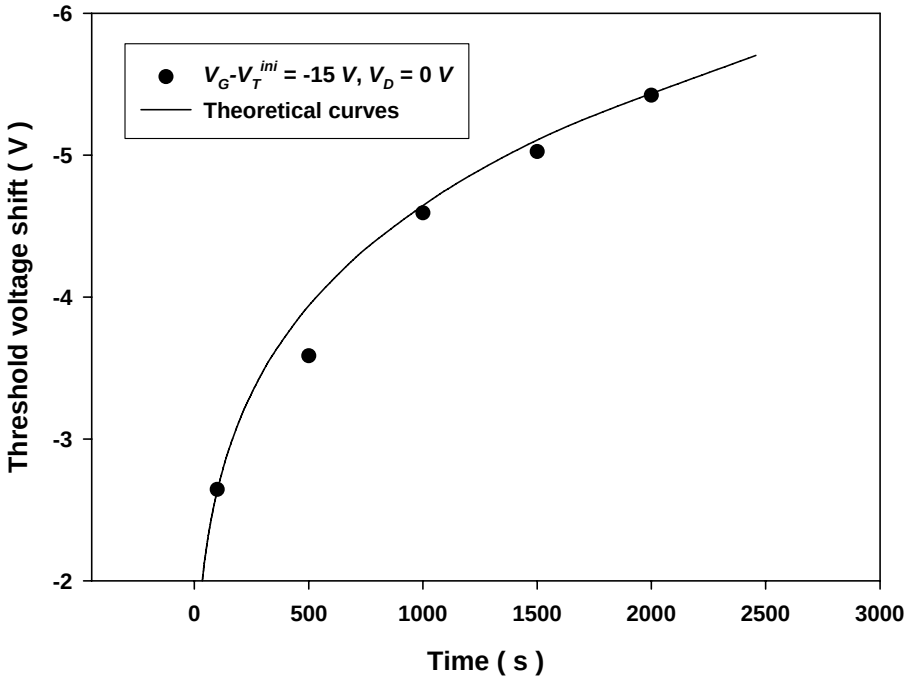

Fig. 4-7 The threshold voltage shift as a function of stress time. Circle denote experimental measurements and solid line denote theoretical curves.

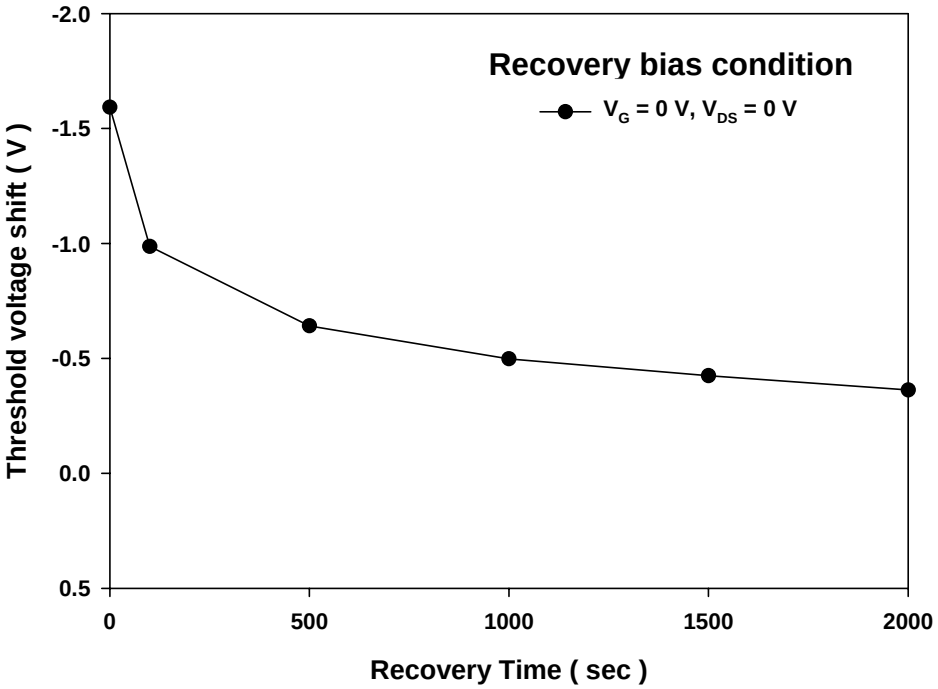

Fig. 4-8 The threshold voltage shift as a function of recovery time

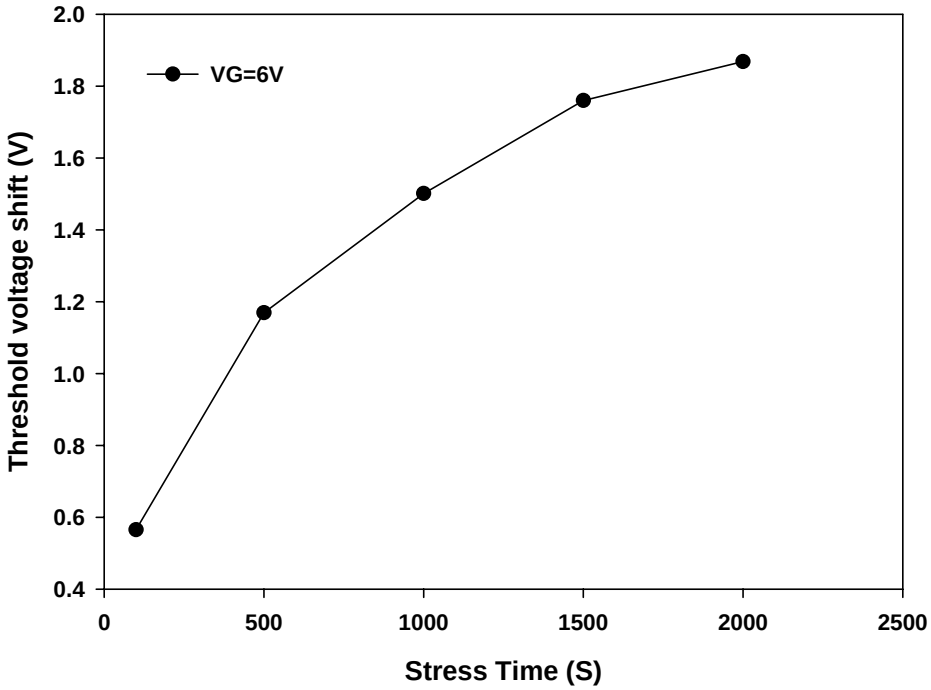

Fig. 4-9 The threshold voltage shift as a function of stress time

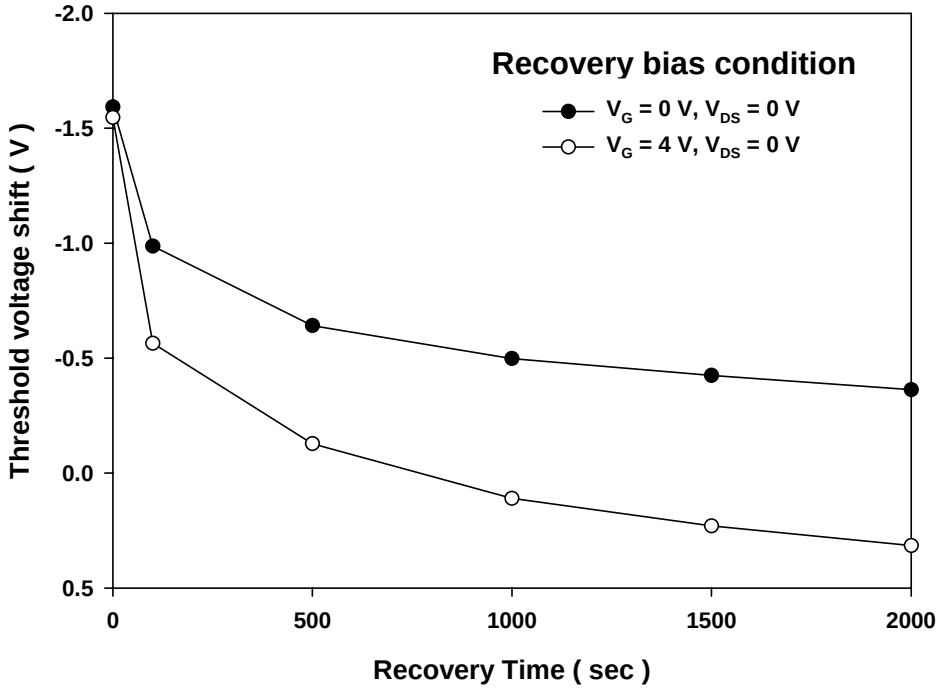

Fig. 4-10 The threshold voltage shift as a function of recovery time with different recovery bias condition

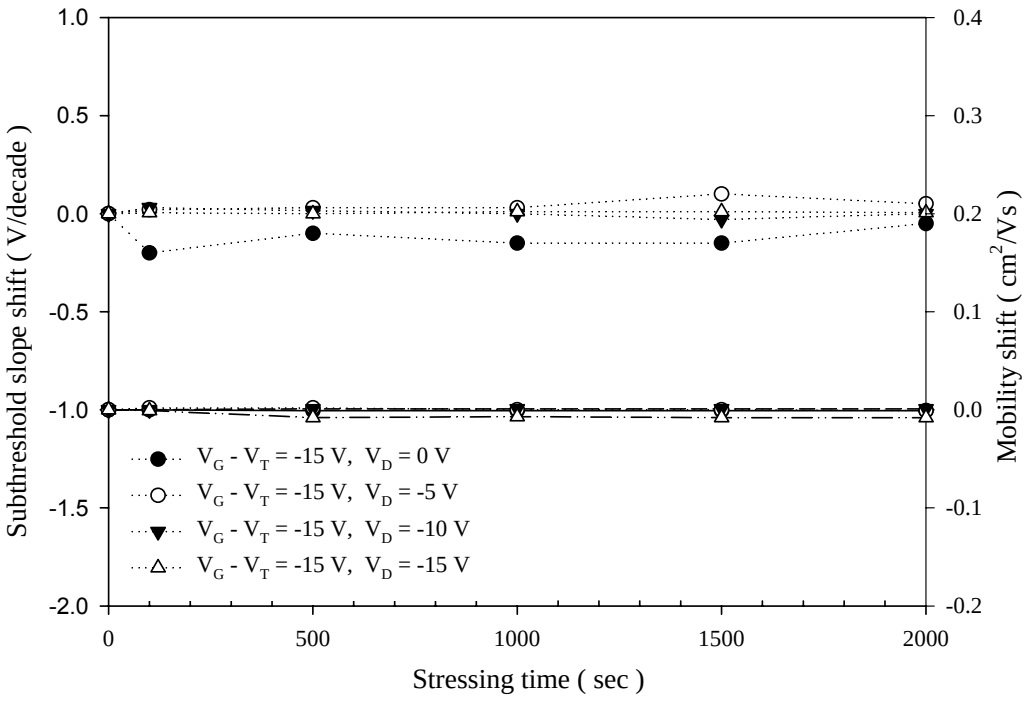

Fig. 4-11 The subthreshold swing and the field-effect mobility as a function of stress

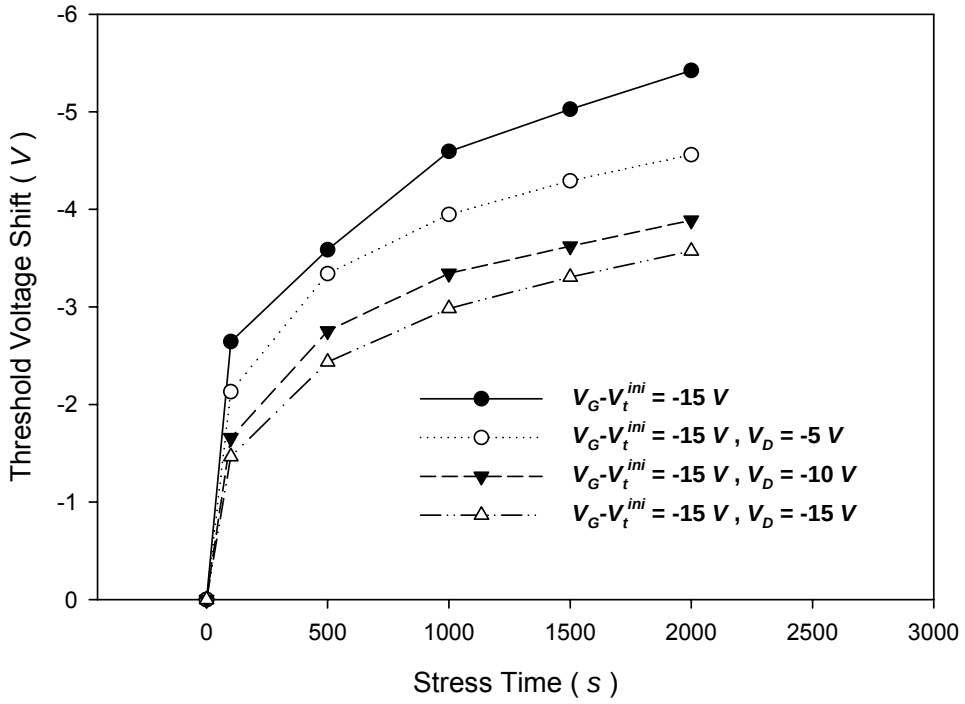

Fig. 4-12 The threshold voltage shift as a function of stress time with different stress condition

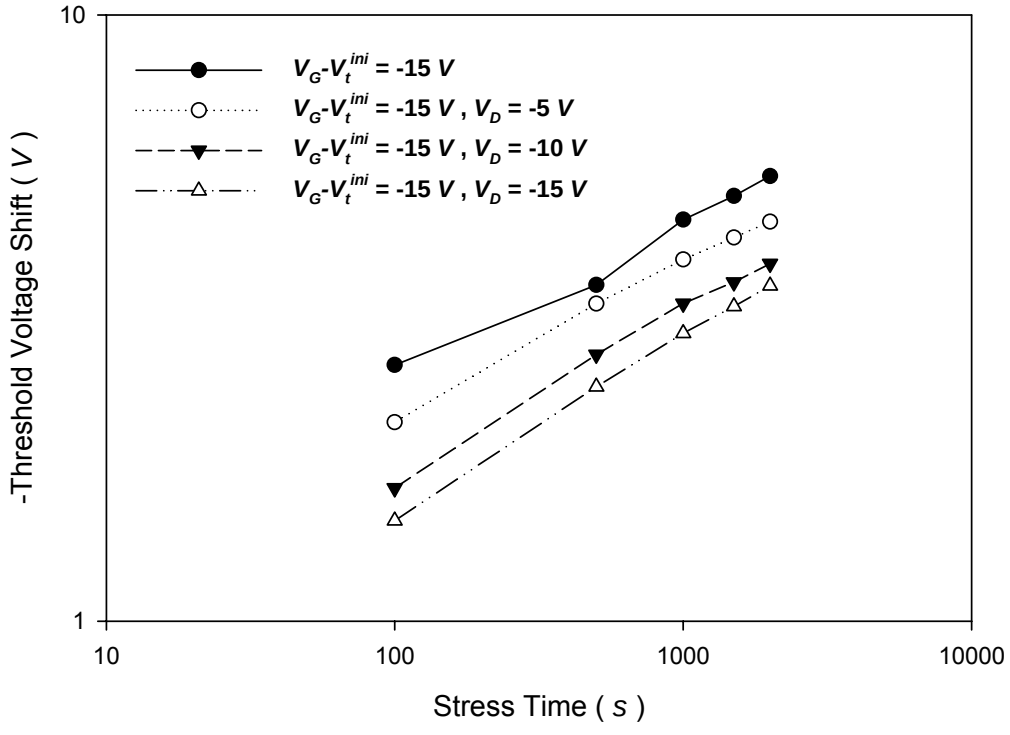

Fig. 4-13 The threshold voltage shift as a function of stress time with different stress

on a logarithmic scale condition

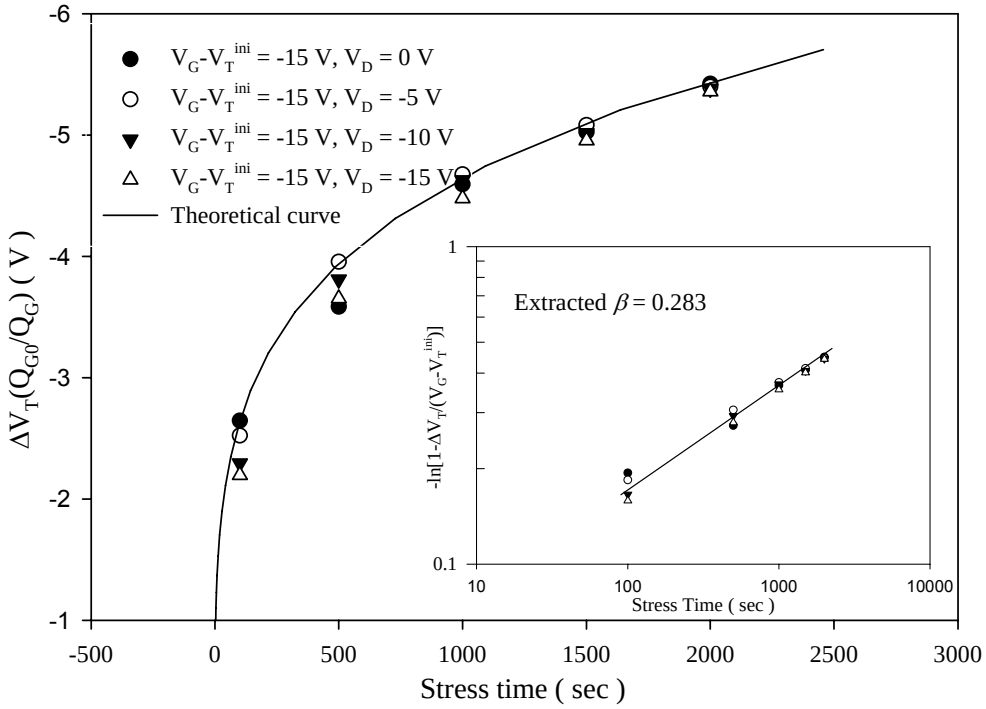

Fig. 4-14 The $\Delta V_T^{res} = (Q_{G0} / Q_G)\Delta V_{th}$ as a function of time. β is obtained by plotting $\log\left\{-\ln\left[1-\Delta V_T^{res}/(V_{GS}-V_T^{ini})\right]\right\}$ as a function of log(t) in the inset

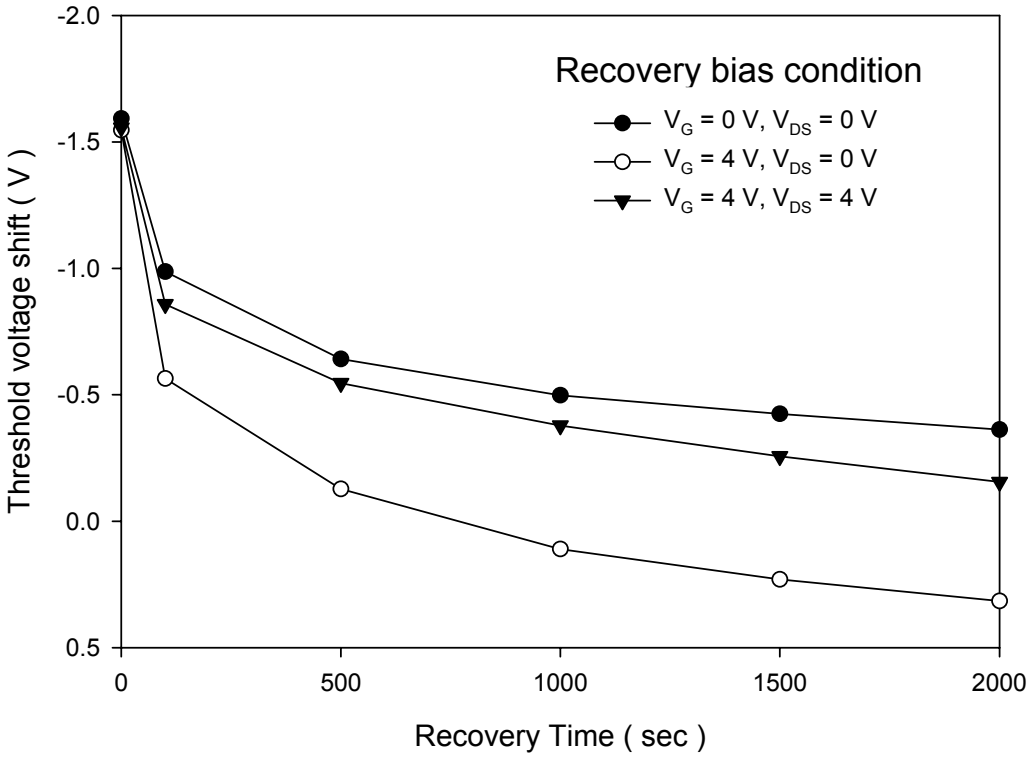

Fig. 4-15 The threshold voltage shift as a function of recovery time with different

recovery bias condition

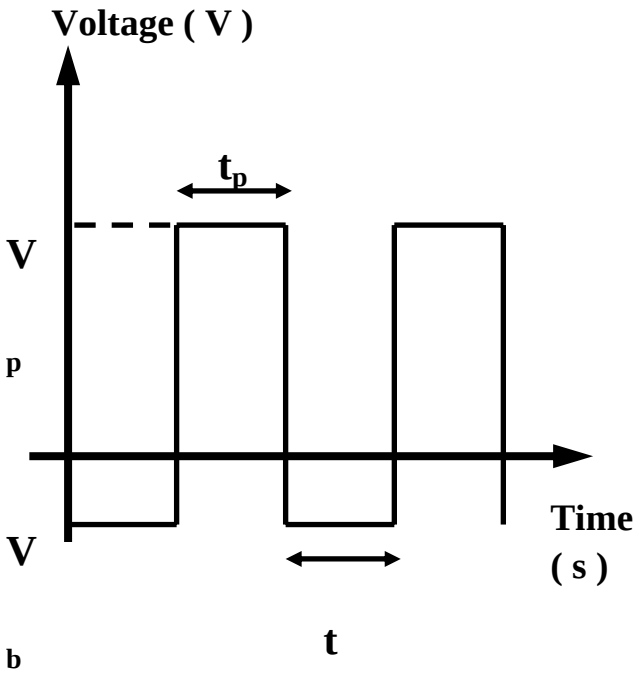

Fig. 5-1 The AC signal used in this study

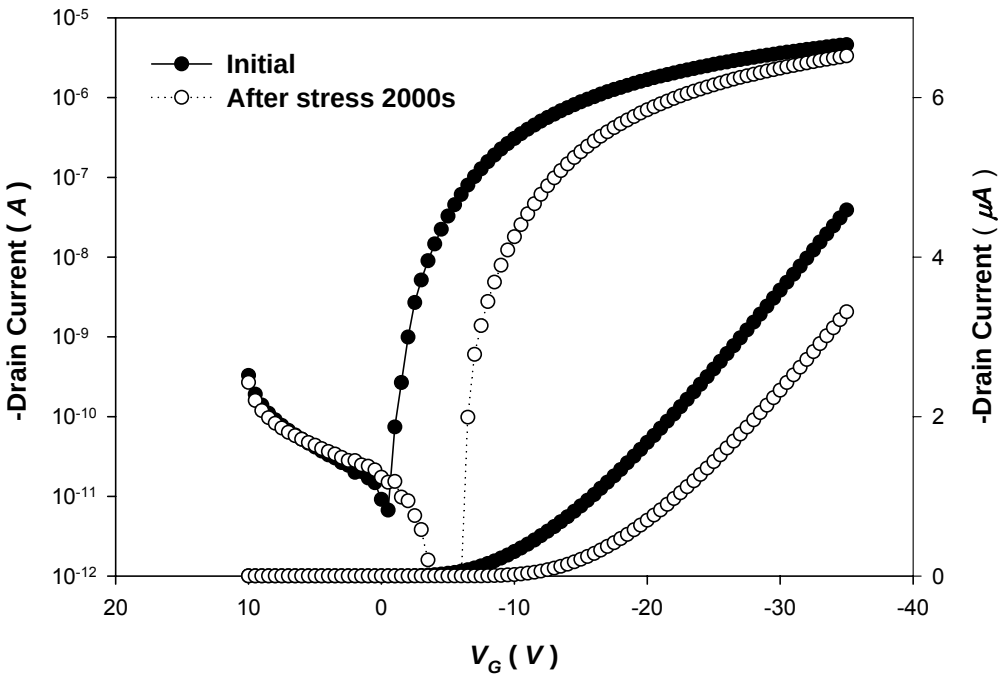

Fig. 5-2 The linear-region transfer characteristics of the devices before stress and after effective 2000-sec stress

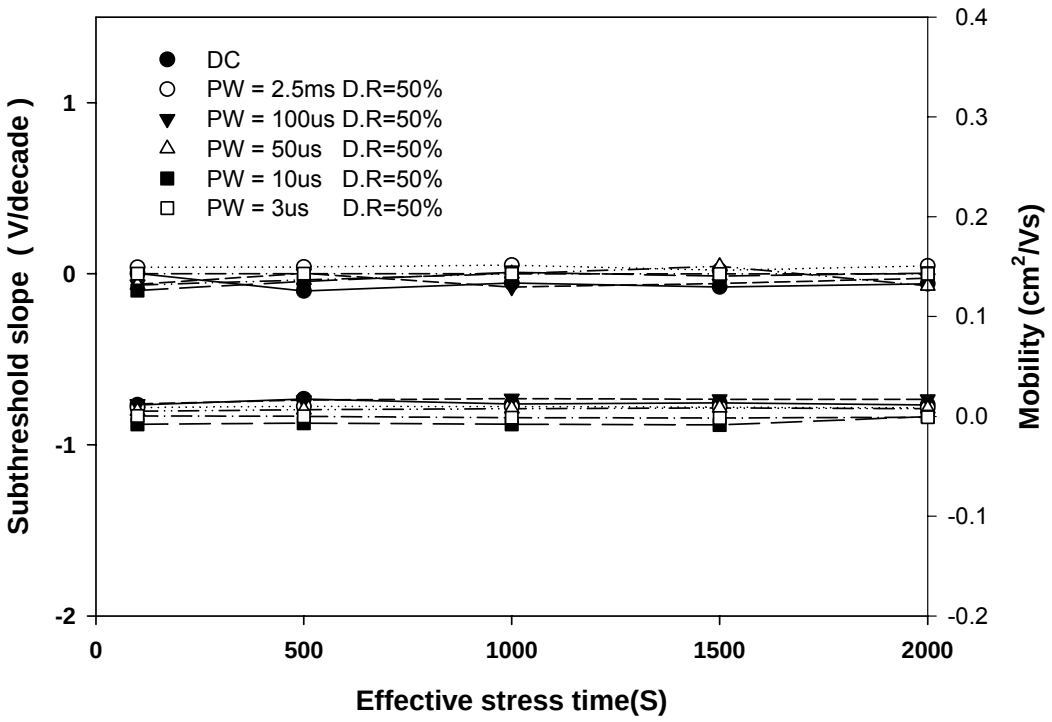

Fig. 5-3 The subthreshold swing and the field-effect mobility as a function of effective stress time with different stress condition

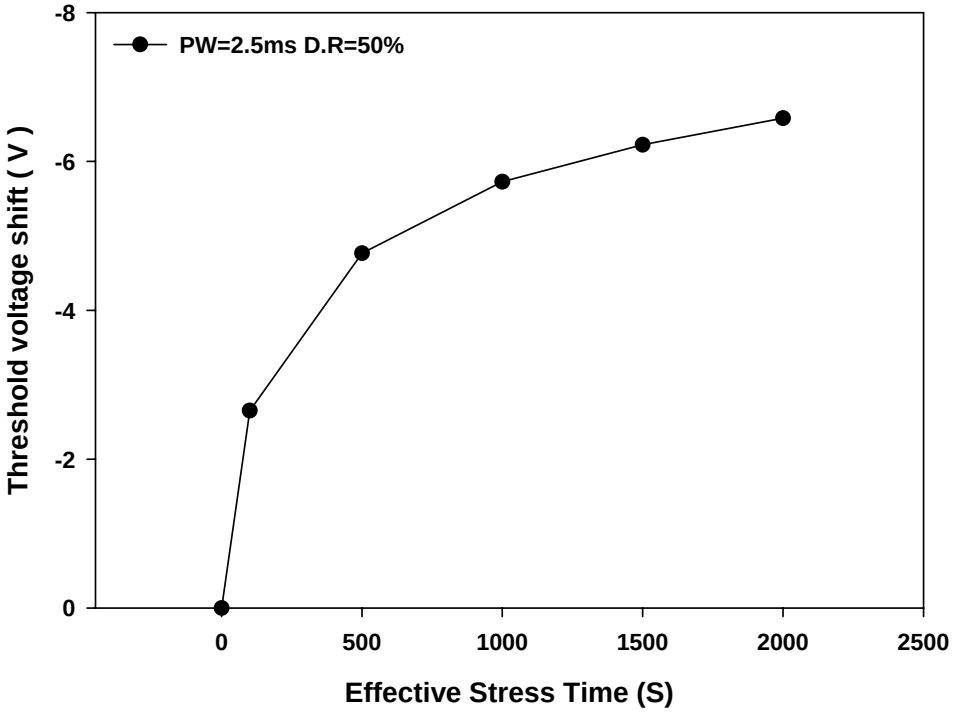

Fig. 5-4 The threshold voltage shift as a function of effective stress time

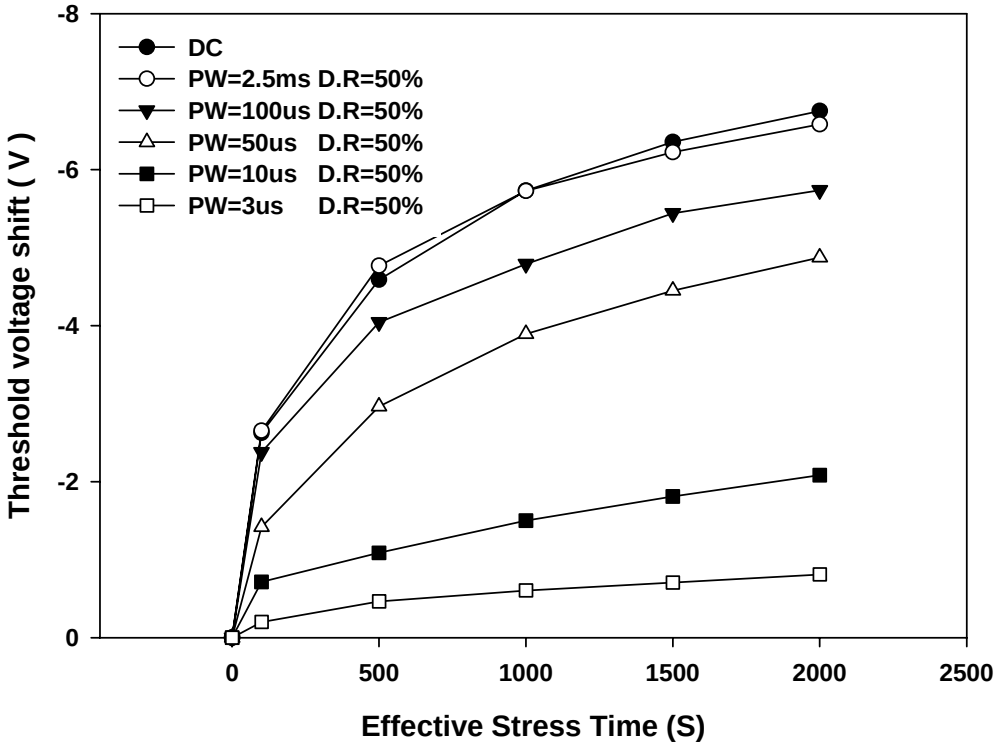

Fig. 5-5 The threshold voltage shift as a function of effective stress time with different stress condition

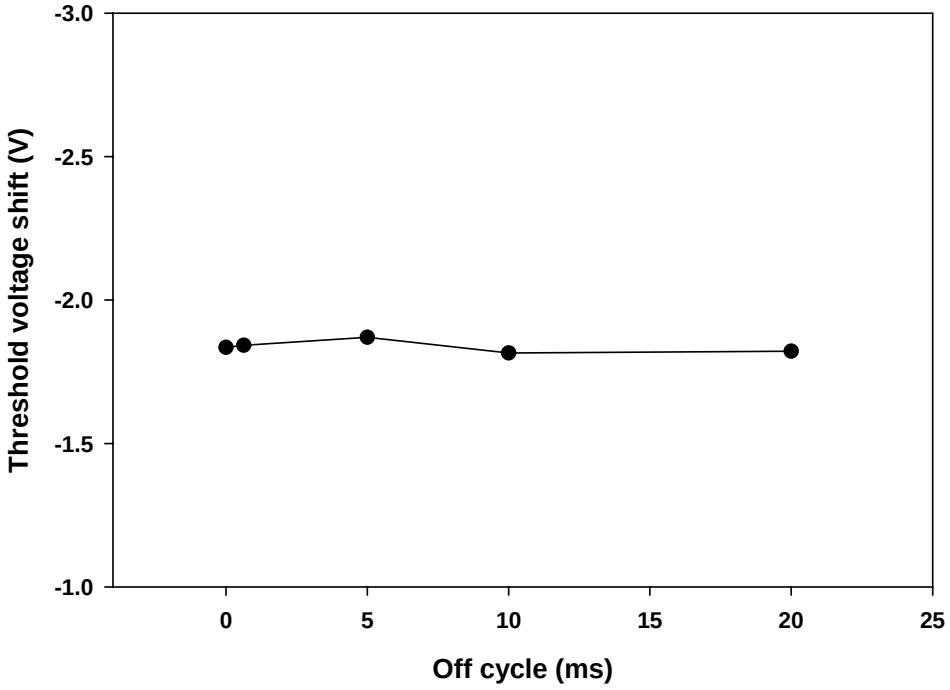

Fig. 5-6 The threshold voltage shift versus off cycle

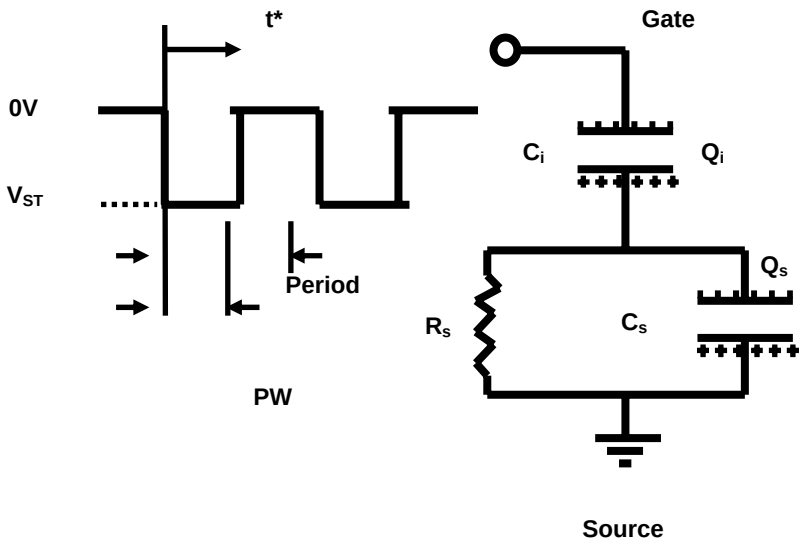

Fig. 5-7 The RC equivalent circuit to simulate the device under pulsed bias stress

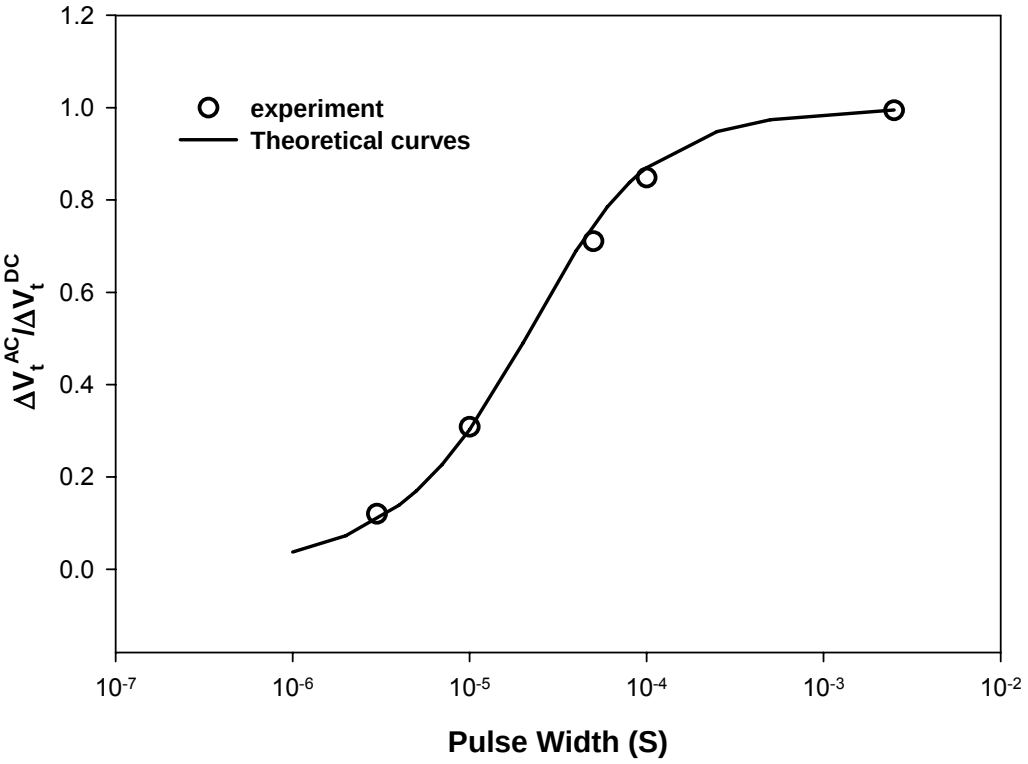

Fig. 5-8 Normalized threshold voltage shift versus gate bias stress pulse width

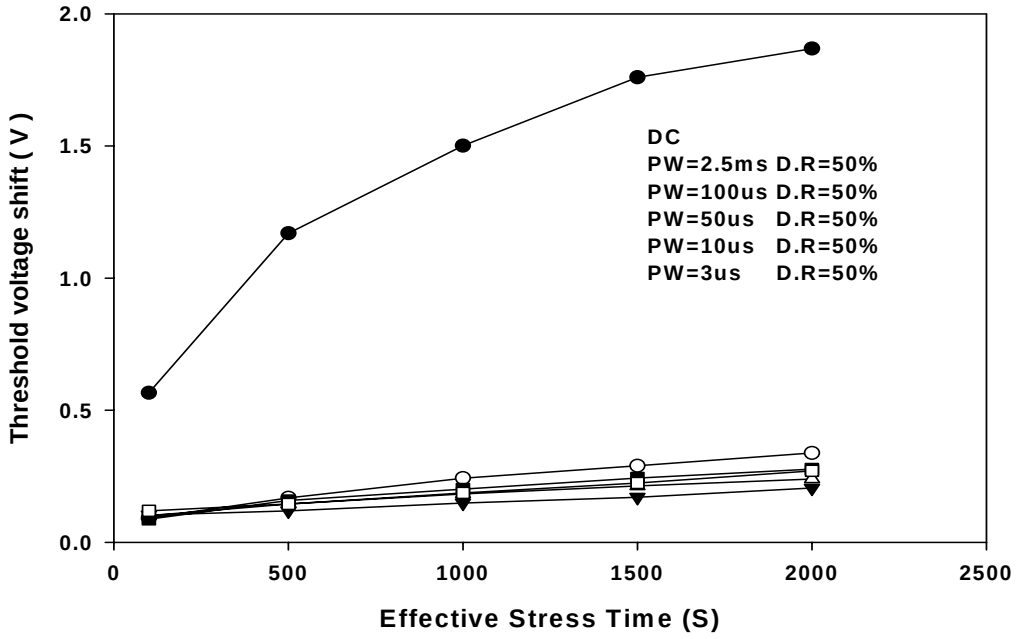

Fig. 5-9 The threshold voltage shift as a function of stress time with different stress condition

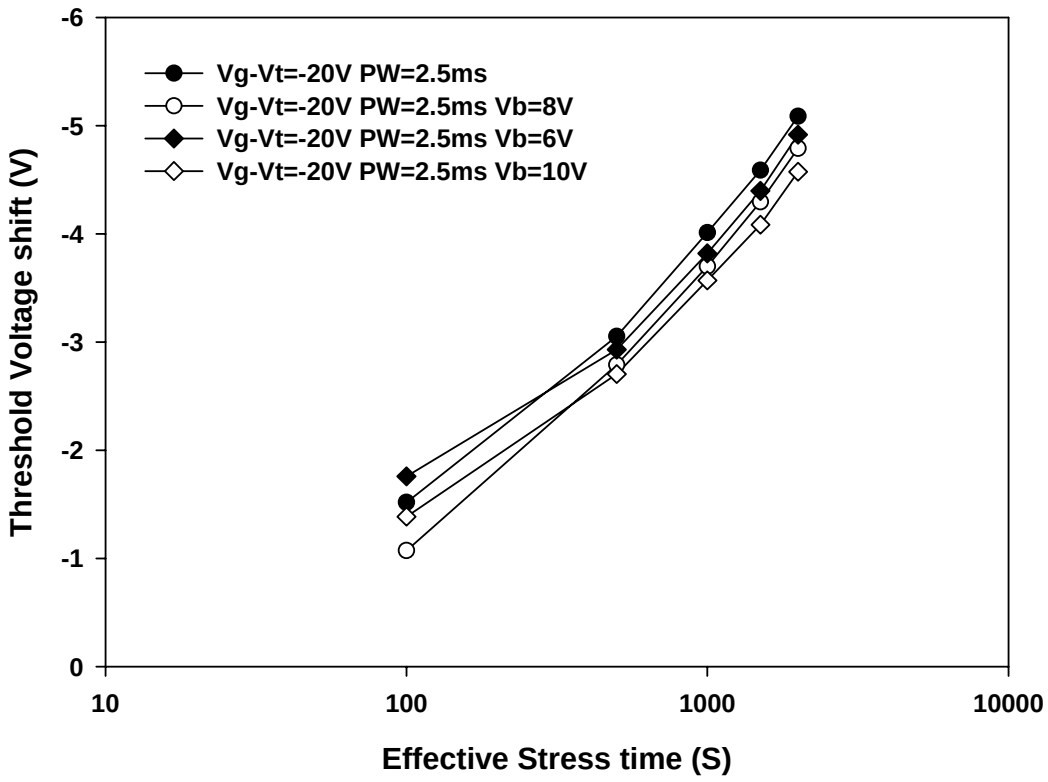

Fig. 5-10 The threshold voltage shift as a function of stress time with different stress condition

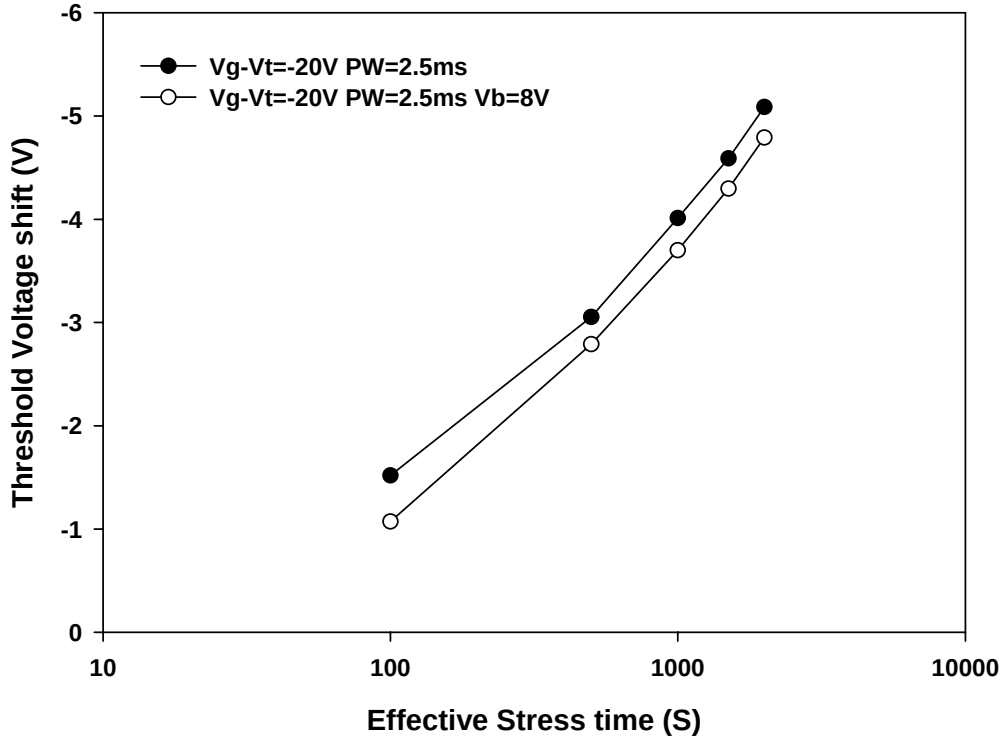

Fig. 5-11 The threshold voltage shift as a function of stress time with different stress condition

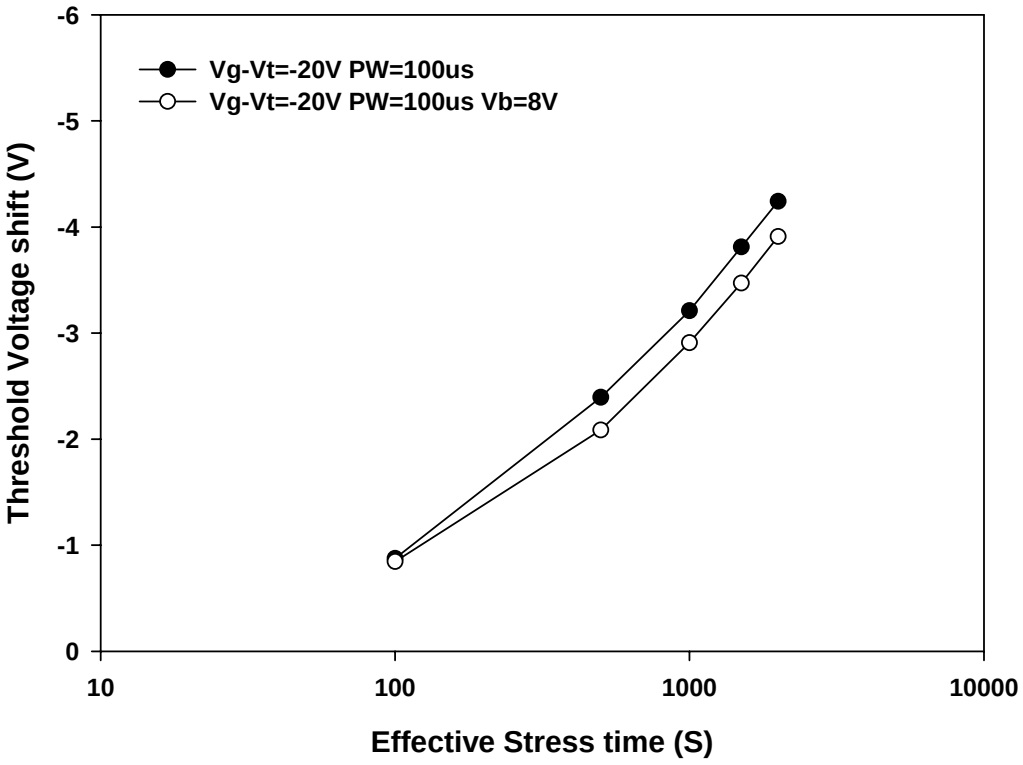

Fig. 5-12 The threshold voltage shift as a function of stress time with different stress condition

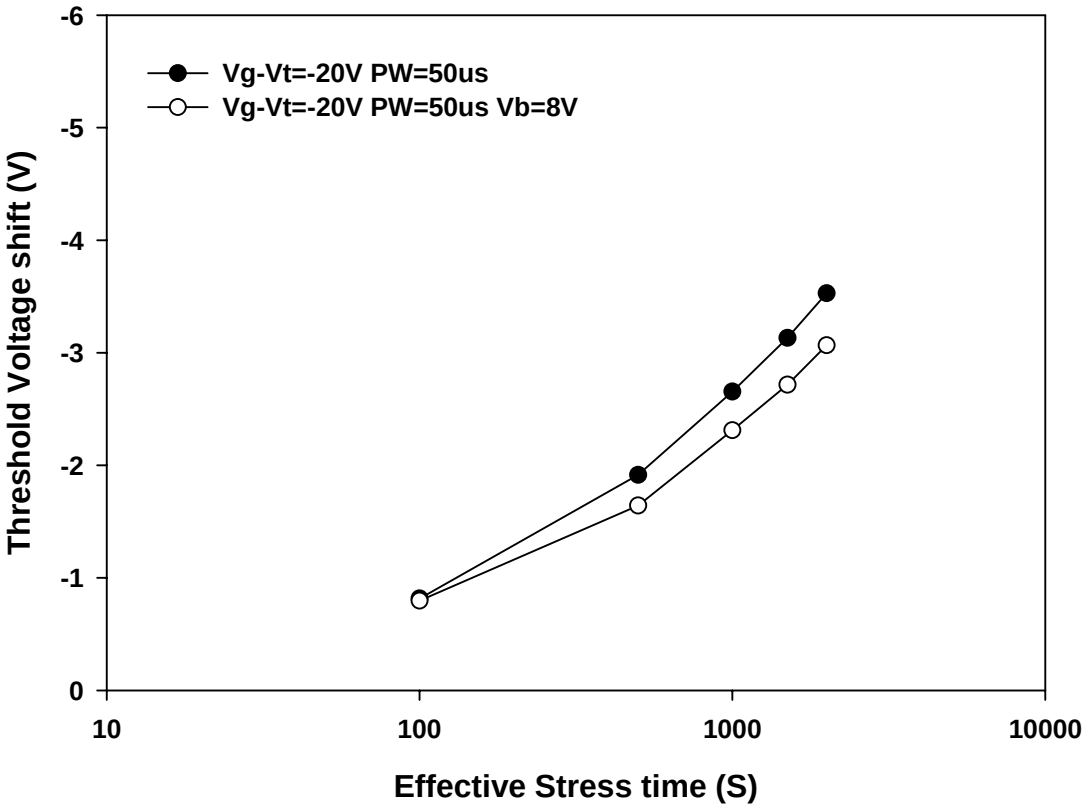

Fig. 5-13 The threshold voltage shift as a function of stress time with different stress condition

簡　　歷

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論文題目：

五環素有機薄膜電晶體之可靠度分析

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