國立交通大學

光電工程學系顯示科技研究所

碩士論文

有機薄膜電晶體後退火之影響研究

The Post-Annealing Effect on Organic Thin-Film Transistors

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摘　　要

在有機材料中，載子的傳遞主要是以載子躍遷的方式進行，遷移率受限於元件製程中有機薄膜品質的好壞。較差的成膜品質會使得有機薄膜電晶體之載子移動率無法有效提升，因此如何在元件製程中提升薄膜品質一直是非常重要的議題。本研究之主要目的在於探討元件熱退火處理對有機薄膜電晶體之元件特性的影響和元件效能改善的機制，並探討熱退火處理如何影響有機半導體層-pentacene-之成膜品質。

實驗結果顯示，有機薄膜電晶體經由元件熱退火處理後，元件的遷移率由原先的 0.42 $cm^2V^{-1}s^{-1}$ 提升至 0.8 $cm^2V^{-1}s^{-1}$，其中的原因部分來自於熱退火處理使得元件的通道電阻大幅下降。另外，透過原子力顯微鏡我們證明 pentacene 通道部分的晶界，在熱退火處理後有減少的趨勢，我們推測這是造成通道電阻下降的主因。然而，熱退火處理卻使得元件的接觸電阻和半導體層中垂直於通道部分的電阻上升了。其內部機制，我們也進一步由原子力顯微鏡和 X 光繞射儀的分析結果來探討。另外，我們也發現當我們結合 poly-α-methylstyrene 表面修飾及元件後退火效應，可以使得元件的 interface traps 大幅下降，而且 pentacene 和基板表面的附著變的更好，進而使得元件遷移率由 0.11 $cm^2V^{-1}s^{-1}$ 提升到 0.8 $cm^2V^{-1}s^{-1}$。

The Post-Annealing Effect on Organic Thin-Film Transistors

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ABSTRACT

Charge transport in organic semiconductor is typically described by hopping of charges between localized states. For this type of transport, the charge carriers are easily trapped at the grain boundary or by the disorder and impurities around the grains, resulting in the limitation of organic thin-film transistors (OTFTs) device mobility. Therefore, how to improve organic thin film quality becomes a very important issue. Based on the principle of controlling the growth of pentacene film, the effect of post-annealing treatment on pentacene-based TFTs is investigated in this study. Aims of our researches are to examine the effect of post-annealing treatment on device performance, pentacene crystal structures, and their correlations.

It is found that the device mobility is increased from 0.42 to 0.80 $cm^2V^{-1}s^{-1}$, which results from the reduced channel resistance. Images of atomic force microscopy (AFM) show that it is because the pentacene grain boundaries are reduced after thermal annealing. However, both contact and bulk resistances are slightly raised after post-annealing treatment. The mechanisms are further discussed by the investigation of the X-ray diffraction spectra and AFM patterns. In addition, the device mobility can be improved from 0.11 to 0.8 $cm^2V^{-1}s^{-1}$ by combining PαMS modification and the post-annealing treatment. It is because that traps in pentacene/insulator interface are significantly moved and the adhesion between pentacene and insulator are improved.

誌　　謝

本文能順利地完成全來自於顯示所的師長們、有機電子元件實驗室前輩們及伙伴們的傾囊相助，在此由衷地表達我的感激。

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最後，也要感謝我的家人在我求學過程中不斷地給我的鼓勵和生活上的支持。沒有他們的大力相助，我的求學過程不可能如此平順。

謹誌於

國立交通大學顯示科技研究所

中華民國九十六年七月

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Chapter 1

INTRODUCTION

1.1 General Statement of OTFT

In recent years, the research of organic materials grows rapidly because of their high potential for the applications on optoelectronic and electronic devices, such as photovoltaic cells [1-2], organic light-emitting diodes [3], organic thin-film transistors [4], nonlinear optical materials, etc. More and more optoelectronic devices tend to be fabricated based on organic materials due to many advantages, such as flexibility, low-cost and large-area devices.

Recently, organic thin-film transistors (OTFTs) have attracted intensive attention due to the significant improvement in mobility which reaches higher than 1 $cm^2V^{-1}sec^{-1}$ [5-8]. The state-of-art device mobility reported so far is even up to 35 $cm^2V^{-1}sec^{-1}$. [9] The development history of p-type OTFTs are shown in Figure 1.1 [4]. Apparently, pentacene is the most promising organic semiconductors applied in p-type OTFTs because pentacene exhibits high device performance comparable to that of hydrogenated amorphous silicon (α-Si:H). SONY Corp. even has developed the first full-color active-matrix organic light-emitting diode display on a flexible plastic substrate as shown in Figure 1.2. The semiconductor used in the transistors of this organic LED display is exactly pentacene.

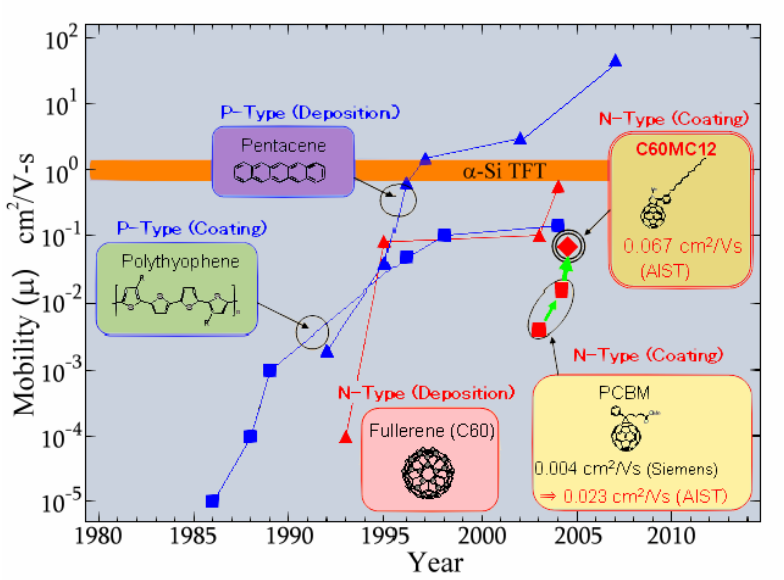


Figure 1.1 Evolution of hole-mobility for the most common p-type organic semiconductors. The mobility has been improved by more than five orders of magnitude during 15 years.

Figure 1.2 The first full-color active-matrix organic LED display on a flexible plastic substrate developed by SONY Corp.

(Picture source: http://www.eetimes.com/showArticle.jhtml?articleID=199703004)

Unlike the inorganic crystals which are formed by atoms with covalent bonds, the structure of organic materials is formed by molecules weakly bonded by van der Waals force. It is much weaker than the covalent force in inorganic materials, which is the reason for their low mobility. The conducting mechanism in organic semiconductors is quite different from that in metals or conventional semiconductors. Because organic semiconductors consist of chemically conjugated systems, charge transport is typically described by hopping of charges between localized states. In this type of transport, the charge carriers are localized due to the structure disorder, defects or self-localization (polarons). Furthermore, the mobile charges are easily trapped at the grain boundary or by the disorder and impurities around the grains, resulting in the limitation of the device mobility.

Pentacene is a well-known the organic semiconducting materials. The mobility of pentacene-based TFTs is relatively high since pentacene has a strong tendency to form an ordered film. However, the film quality is deeply affected by the growth conditions, such as deposition temperature, evaporation rate, base pressure, surface roughness, etc. Each condition mentioned above plays an important role in the property of film morphology; however, it is very difficult to control the deposition condition. [10-11] Therefore, an easier way to improve film quality is necessary.

1.2 Objective and Motivation

Although the device performance of OTFTs is still not good enough, the flexible property of organic materials creates the superiority of organic semiconductors over the inorganic semiconductors for applications. Therefore, how to enhance the device performance of OTFTs was always interested.

As mentioned in the preceding section, it has been shown that the formation of pentacene films is significantly sensitive to the growth conditions, and the film quality plays an important role on device performance. Consequently, to understand and, further, to control of molecular growth become crucial issues.

Post-annealing treatment is a simple method to improve the film quality. Several reports have investigated the post-annealing effect on the pentacene thin-film and device characteristics. [12-14] However, the detailed mechanism is still not well understood yet. In this work, the effect of the post-annealing treatment on pentacene-based TFTs is investigated systematically. We firstly controlled the growth of pentacene through the post-annealing treatment, followed by studying the correlation between the thin-film morphology of pentacene and TFT device performance. The details are as following issues:

(1) the effect of post-annealing treatment on device performance,

(2) the effect of post-annealing treatment on pentacene crystal structures, and

(3) their connections.

1.3 Organization of Thesis

The thesis consists of six chapters. In this chapter, our objective and motivation have been described.

In **chapter 2**, we have introduced the background knowledge of this thesis, including the operation and the parameters of OTFTs, the concept of charge conduction in organic semiconductor, and so on. Moreover, we also present an overview of related researches on thermal annealing effect and its device performance.

Chapter 3 gives a detailed description of our device fabrication process and measurement system.

In **chapter 4**, the analysis methods are introduced. It describes how we analyzed the grain boundary density and roughness from images recorded by atomic force microscopy, and how we examined pentacene phase and crystal structure from X-ray diffraction-spectra.

Chapter 5 shows our experimental results as well as the related details

Conclusions and future work are summarized in **chapter 6**.

Chapter 2

LITERATURE REVIEW

2.1 Organic Thin film Transistor [4]

2.1.1 The Geometry and Operation

Figure 2.1 (a) and 2.1 (b) show two structures of OTFTs that are most commonly used, top-contact and bottom-contact structures. In the top-contact device, the organic semiconductor is deposited before the deposition of metal electrodes. On the contrary, the deposition sequence of bottom-contact device is reversed. Pentacene-based TFTs exhibit p-type device behavior, which means that the holes serve as majority carriers. Therefore, a negative bias of gate voltage was applied to accumulate holes in the p-type active layer. The operation of a p-type OTFT can be simply described as following:

(1) When the gate bias V_{GS} is zero, there is no gate-induced charge near the semiconductor/insulator interface. At this moment, no charges can transport even if a small negative source-drain bias V_{DS} is applied, since there are no mobile charges in the organic semiconductor.

(2) When a negative V_{GS} is applied on gate electrode, accumulation of positive charges at the semiconductor/insulator interface takes place and an electric field

is induced. This is the *accumulation regime*. In this regime, the accumulation of charges will form a *channel* from source to drain electrodes, which allows hole current to flow inside.

(3) While the electric field is large enough and under an negative bias of V_{DS}, the hole current is induced in the *channel* and subsequently flows from the drain to the source electrode.

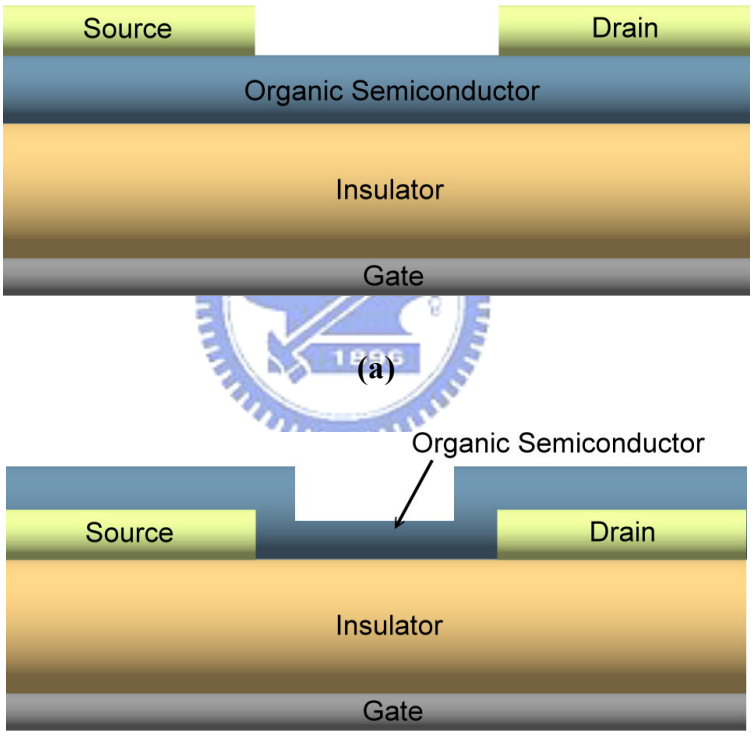


Figure 2.1 (a) top-contact structure of OTFT and (b) bottom-contact structure of OTFT. In the top-contact device, the organic semiconductor is deposited before the deposition of metal electrodes. On the contrary, the deposition sequence of bottom-contact device is reversed.

2.1.2 The Parameters

The current (I) –voltage (V) characteristics model of OTFTs are often expressed as that of convection inorganic semiconductors devices. Figure 2.2 shows a plot of drain current (I_D) versus drain voltage (V_{DS}) at various gate voltages (V_{GS}).

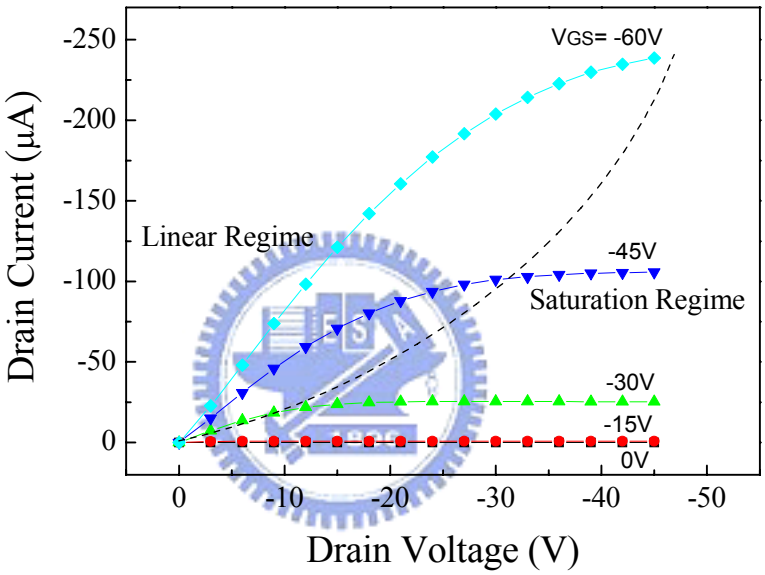


Figure 2.2 A typical plot of drain current (I_D) versus drain voltage (V_{DS}) at various gate voltages (V_{GS}). I_D linearly increases with V_{DS} in the linear regime; however, I_D tends to be independent of V_{DS} in the saturation regime.

At low V_{DS}, i.e., $-V_{DS} << -(V_{GS} - V_T)$, I_D increases linearly with V_{DS}, which is called *linear regime*. In this regime, I_D is approximately described as the following equation:

$$I_D = \frac{WC_i}{L}\mu(V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS} \quad (2.1)$$

where W is the channel width, L is the channel length, μ is the field-effect mobility, V_T is the threshold voltage, and C_i is the capacitance per unit area. At large V_{DS}, i.e., $-V_{DS} > -(V_{GS} - V_T)$, I_D tends to saturate due to the pinch off of accumulation layer, which is called *saturation regime*. The characteristics of the saturation current are expressed by the equation:

$$I_D = \frac{WC_i}{L}\mu(V_{GS} - V_T)^2 \quad (2.2)$$

Figure 2.3 shows Gate voltage dependence of Drain current.

The mobility (μ) discussed in this study is extracted from the slope of the plot of $|I_D|^{1/2}$ versus V_{GS} in the saturation regime, according to

$$\sqrt{I_D} = \sqrt{\frac{WC_i}{2L}\mu}(V_{GS} - V_T) \quad (2.3)$$

The threshold voltage (V_T) defines the onset voltage for the channel formation. V_T shown in Equation (2.3) represents the x-intercept of $|I_D|^{1/2}$-V_{GS} plot in the *saturation regime*. The on-off current ratio (I_{on}/I_{off}) which means the ratio of the current turned device on over the current turned device off is also exhibited in Figure 2.3. Further, the sub-threshold swing (*S.S.*) reveals how fast the device can be turned on and off, defined as

$$S.S. = \frac{\partial V_G}{\partial(\log I_D)} \quad (2.4)$$

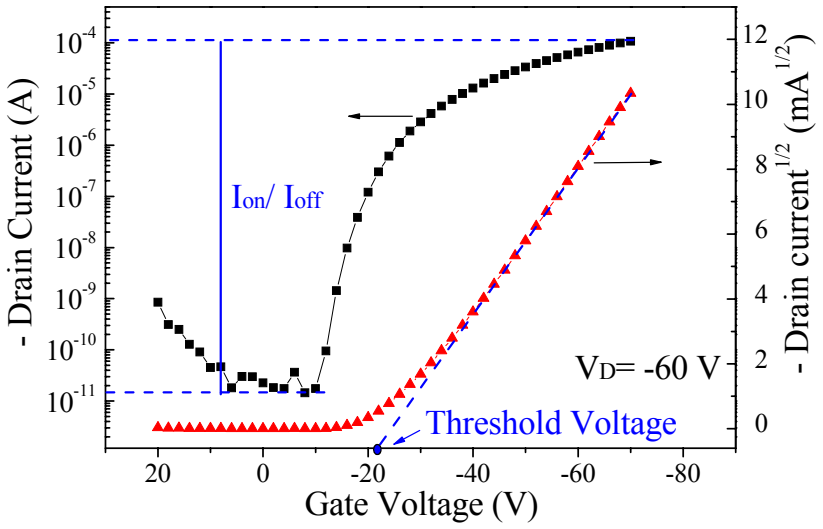


Figure 2.3 Semi-logarithmic plot of I_D versus V_{GS} (left y-axis) and plot of $|I_D|^{1/2}$ versus V_{GS} (right axis) at a constant drain voltage of –60 V (saturation regime).

2.1.3 Effective Resistance

The approach utilized to discuss resistance of OTFT is the transmission-line method (TLM). [15] The concept of TLM was described in Figure 2.4. Based on the TLM, we separate the whole device resistance (R_{on}) of OTFT into a total contact resistance (R_C, source/drain contacts) and channel resistance (R_{Ch}). At low V_{DS}, R_{Ch} is a function of L and V_{GS}. Therefore, the R_C is given by the intercept of R_{on} versus L plot at $L = 0$, where $R_{on} = R_{Ch} + R_C$.

But this assumption is not very critical. One of the reasons is that the R_C we obtained is the contact resistance at L=0 without taking the whole source/drain contact area into account. Besides, it is invalid to multiply R_C by source/drain contact area since

the distribution of the current is not uniform throughout the whole source/drain contact area. Another reason is that R_C is not the pristine contact resistance because the resistance comprises the resistance of contact surface and the resistance of bulk pentacene vertical to the channel, as shown in Figure 2.5.

Accordingly, the influence of contact resistance and bulk resistance should be discussed individually.

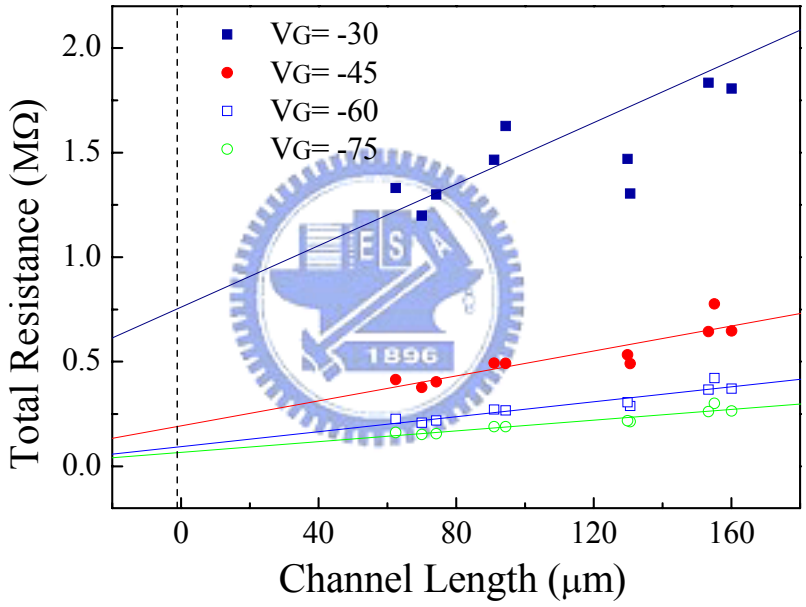


Figure 2.4 Total resistances as a function of L at different V_{GS}. By the TLM, R_C is given by the intercept of the total resistance R_{on} versus L plot at $L = 0$.

To obtain accurate contact resistance and bulk resistance, we followed the theorem which published by Michael Shur in 1990. [16-17] M. Shur's theory is based on TLM and followed by a second order differential equation to calculate effective resistance

and injection length.

According to his theorem, in the linear regime, the R_{on} can be expressed as the sum of the intrinsic channel resistance (r_{ch}) which is independent of L, and the parasitic resistance (R_p), as the following equation:

$$R_{on} = \frac{\partial V_{DS}}{\partial I_{DS}}\bigg|_{v_{ds}\to 0}^{v_g} = \frac{L}{W\mu_i C_i (V_G - V_T)} + R_P = r_{ch}L + R_p \tag{2.5}$$

where μ_i is the intrinsic mobility and V_T is the threshold voltage. In Figure 2.5, a simple schematic circuit diagram at the source contact of OTFT is illustrated.

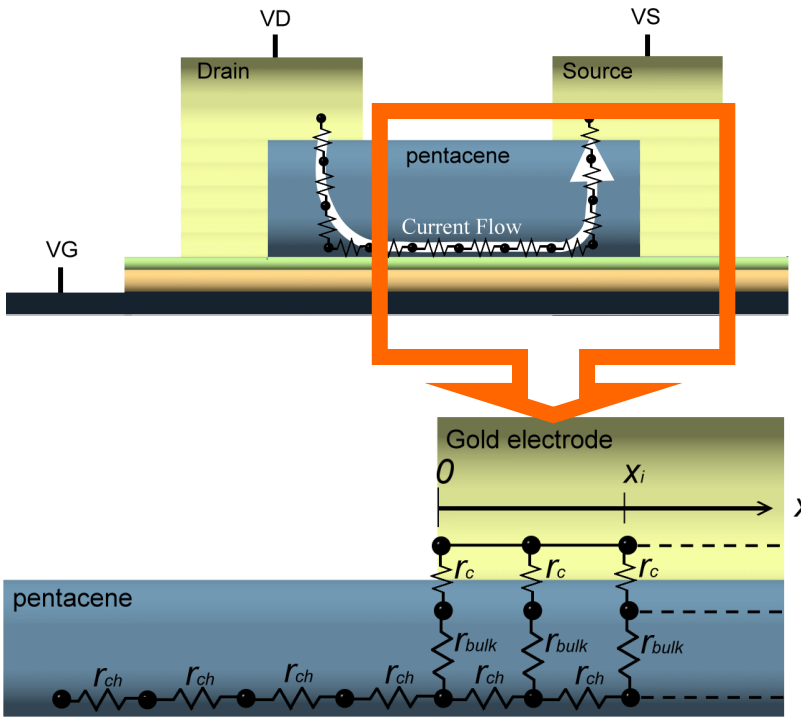


Figure 2.5 The equivalent circuit of top-contact OTFT near the pentacene and electrode interface. The r_{ch}, r_{bulk}, and r_C are calculated by the theorem which published by Michael Shur in 1990. [16-17]

The current distribution under a contact surface can be described from the following equation:

$$\frac{dI_{ch}(x)}{dx} = -WJ_c(x), \tag{2.6}$$

where $I_{ch}(x)$ specifies the current parallel to the channel, x represents the coordinate in the direction parallel to channel, and J_c is the vertical current density,

$$J_c(x) = V_{ch}(x)/r_P \tag{2.7}$$

Here $V_{ch}(x)$ is the electrical potential of channel at position x and r_P is the effective parasitic resistance consist of effective contact and bulk resistance.

$$r_P = r_{bulk} + r_C \tag{2.8}$$

The variation of $V_{ch}(x)$ along x can be expressed as

$$\frac{dV_{ch}(x)}{dx} = -I_{ch}(x)r_{ch} \tag{2.9}$$

where r_{ch} is the channel resistance of the pentacene film and W is the contact width. Combing Equations (2.6) and (2.9), we have a second order differential equation as:

$$\frac{d^2V_{ch}(x)}{dx^2} = \frac{V_{ch}(x)}{(L_T)^2} \tag{2.10}$$

where

$$L_T = \left(\frac{r_P}{Wr_{ch}}\right)^{1/2} \tag{2.11}$$

is the effective transfer length. The boundary conditions for Equation (2.10) are

$$\left.\frac{dV_{ch}(x)}{dx}\right|_{x=0} = -I_0 r_{ch} \tag{2.12}$$

and

$$\left.\frac{dV_{ch}(x)}{dx}\right|_{x=d} = 0 \tag{2.13}$$

where I_0 is the total channel current and d is the contact length. By solving the Equation (2.10) with boundary conditions of Equation (2.12) and (2.13), we get

$$L_T = R_P / r_{ch}, \tag{2.14}$$

From Equation (2.10), we can obtain the effective contact resistance,

$$r_{Ceff} = WL_T^2 r_{ch} = WR_P^2 / r_{ch} \tag{2.15}$$

2.2 Organic Semiconductor

2.2.1 The Basic Structure of Pentacene

Pentacene ($C_{14}H_{22}$) is a rod-like aromatic molecule composed of five benzene rings. (see Figure 2.6) [18] Benzene consists of a chemically conjugated system in its molecular structure, which is a system of carbon atoms covalently bonded with alternating single and double bonds. In a conjugated molecule the electrons in the π-bond can be excited while the electrons in the σ-bonds in the backbone maintain the structural integrity of the molecule, hence a conjugated polymer can be electronically excited without being destroyed. Moreover an electron (or hole) in a conjugated system will be delocalized within the conjugated segment. Therefore, the conduction mechanism in organic semiconductors is very different from that in metals or inorganic semiconductors. The carrier mobility is strongly dependent on the molecular structure and ordering. On the other hand, compared with other organic semiconductors, pentacene exhibits a strong tendency to form highly ordered films, which depend on the surface properties of substrates and the growth conditions. [10]

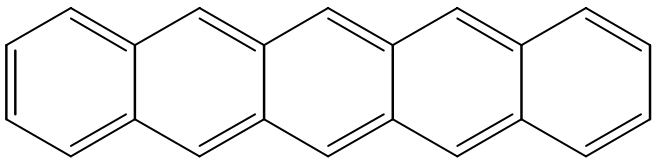


Figure 2.6 Chemical structure of pentacene ($C_{14}H_{22}$). It is a rod-like aromatic molecule composed of five benzene rings.

2.2.2 Charge Transport [19-21]

The conducting mechanism in inorganic semiconductors or metals is usually described by band transport. No matter how perfect the crystal is, the symmetry is always disrupted by phonons (lattice vibrations) that scatter the charge carriers. The diagram is shown in Figure 2.7 (a). Since less phonon are generated at lower temperature, the mobility of the charge carriers decreases with increasing temperature.

It is mentioned that organic semiconductor consist of a chemically conjugated system. This system results in a general delocalization of the electrons across all of the adjacent parallel aligned π-orbital of the atoms. Further, the structures of organic semiconductor are usually disordered, and the energy bands formed by extended conjugated chains are usually not very long and separated by defects. Those defects also create traps for charges; and hence the mobile charges are fairly localized. Because of defects and disorder, organic semiconductors have no extended band structures as inorganic semiconductors. Charge transport in organic semiconductors is typically described by hopping of charges between localized states, which is a phonon assisted mechanism from site to site as shown in Figure 2.7 (b). In this type of transport the carrier is localized due to disorder, defect or self-localization (polarons).

In summary, the charge transport mechanism in organic semiconductor is thermally activated hopping at high temperature. In some cases, it becomes band-like transport described by the band like a straight line at very low temperature. **[22]**

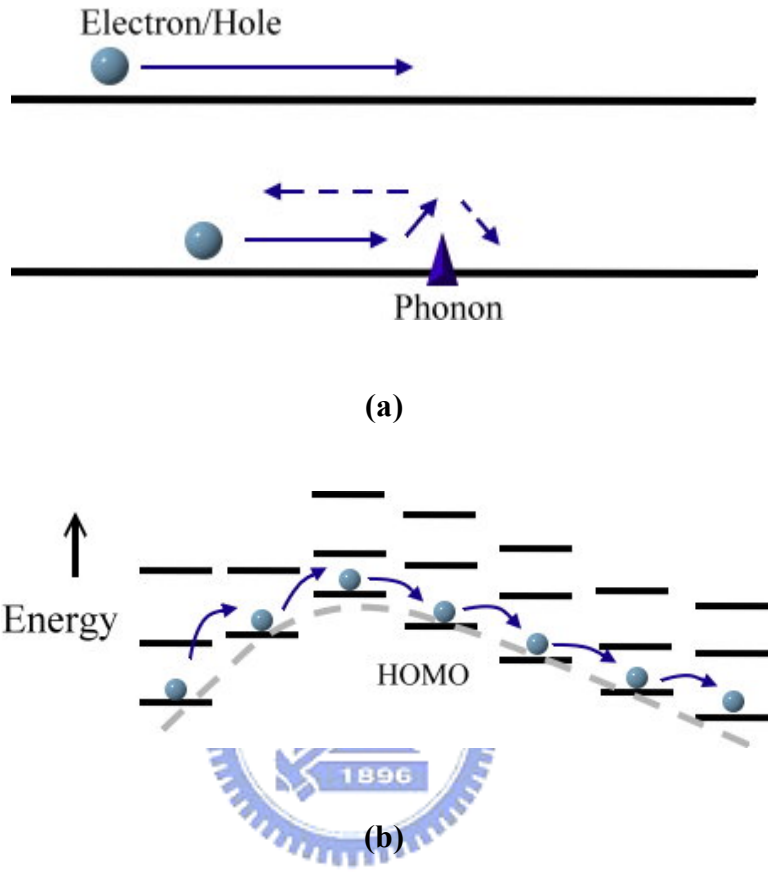


Figure 2.7 Charge transport in solids. (a)Band transport. The band of a perfect crystal is described as a straight line where the delocalized free carrier moves. (b) Hopping transport. In this type of transport the carrier is localized due to disorder, defects o self-localization (e.g. polarons) and hops from site to site with the essential help of lattice vibrations.

2.3 The Thermal Annealing Treatment

Thermal annealing is a heat treatment of material, usually changing its orderings or properties. The annealing process contains heating and maintaining at a suitable temperature, and then cooling. It is hoped to improve the molecular structure and the properties of devices. Therefore, the thermal annealing effect on film orderings and the relationship between molecular structure and device properties are concerned. The thermal annealing treatment has been widely used in the fabrication of poly-Si TFTs [23-24]. Since 2002, several researches about thermal annealing effect on OTFTs and organic films have been proposed. The related literatures are summarized in Table 2.1, including device structures, annealing conditions, and device mobility.

Researches on pentacene thin film and its device performance have been concerned. In Figure 2.8, the plot of ln(μ) versus 1000/T can be fitted by the Arrhenius formula:

$$\mu \propto \mu_0 \exp\left(-\frac{E_a}{kT}\right) \tag{2.16}$$

indicating that the charge transport in devices can be described by the hole-hopping model. [27, 30]

Table 2.1 The related researches about thermal annealing treatment.

Authors	Device Structure G\insulator\semiconductor\S.D	Best Annealing Condition	Mobility cm^2/Vs
T. Komoda *et al.* [25]	n^+-Si\SiO_2\pentacene\Gold	50 °C/1 hr (in vacuum)	0.2
S. J. Kang *et al.* [13]	n^+-Si\SiO_2\pentacene\ Gold	90 °C/1 hr (in vacuum)*	0.49
T. Seckitani *et al.* [26-28]	Au\Polyimide\pentacene\ Gold	140 °C/12 hr (in N_2)	0.56
R. Ye *et al.* [12]	n^+-Si\SiO_2\pentacene	40-120 °C/1 hr (in vacuum)	/
R. B. Chaabane *et al.* [29]	Si\SiO_2 + Si_3N_4\NiPc\Gold	100 °C/1 hr (in vacuum)	8.9×10^{-3}
D. Guo *et al.* [30]	n^+-Si\SiO_2\pentacene\ Gold	45 °C/2 hr (in vacuum)	≒0.22

* The annealing treatment is executed by "pre-annealing" in chamber after pentacene deposition.

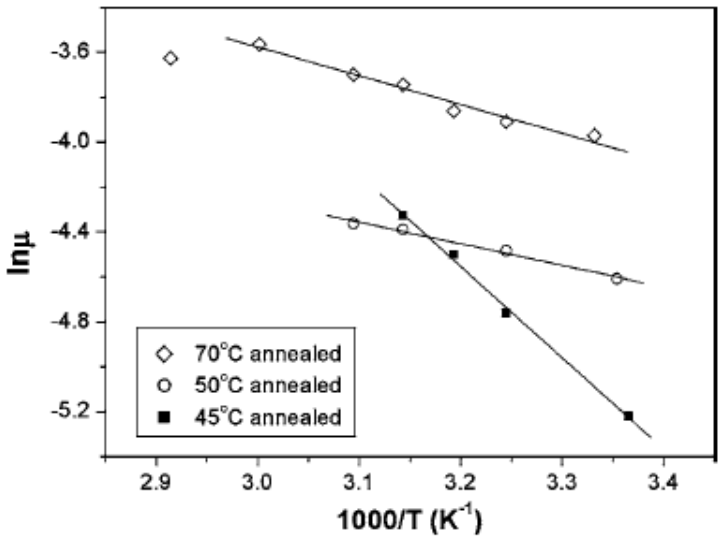


Figure 2.8 Arrhenius plot of the logarithm mobility versus the reciprocal temperature. [30]

In ref. [12, 13, 25], both AFM images and XRD analysis showed that pentacene ordering were improved by thermal annealing. Nevertheless, the mechanism has not been explained in details. How the device performance was influenced by the thermal annealing treatment was still not well understood yet. Therefore, to understand the mechanism of the post-annealing effect on OTFTs is the most important target in this study.

Chapter 3

EXPERIMENTAL PROCESS

3.1 Device Fabrication

3.1.1 Substrate Cleaning

The substrate used in this study consists of heavily n-doped silicon wafer with 200 nm-thick thermal oxides. To remove organic contaminants, the substrates were rinsed in de-ionized water for 5 minutes, dipped in H_2SO_4 + H_2O_2 (H_2SO_4:H_2O_2=3:1, 80 ^oC) solution for 20 minutes, and then rinsed in de-ionized water for another 10 minutes. Finally, the cleaned substrates were blew by dry N_2 gas and dried in an oven at 120 ^oC for 1 hour.

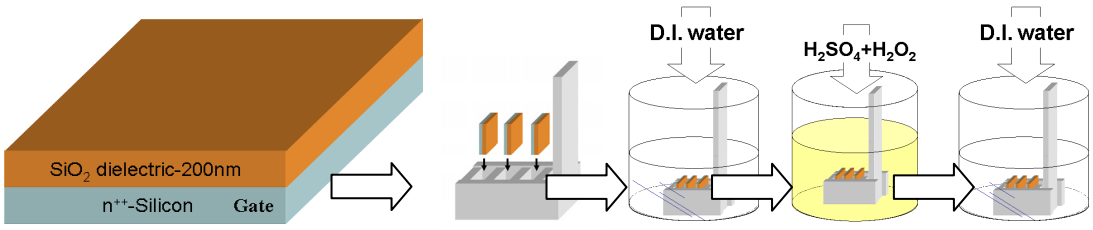


Figure 3.1 The procedure of substrate cleaning. The SiO_2 wafers were placed on the Teflon carrier during the cleaning process.

3.1.2 The Surface Treatment of Insulator Surface

Surface treatment on the gate insulator is one of the effective methods to control the condition of dielectric surface. The treatment has been proposed to have significant effects on the resulting thin film structure and electrical characteristics. [31] Therefore, surface treatment on the SiO_2 is carried out prior to the deposition of the pentacene layer. Our SiO_2 surface was modified with poly-α-methyl styrene (PαMS, Aldrich Co.) by spin-coating from toluene solutions, which can change the electronic state at the dielectric/channel interface, and improve the pentacene-based TFT performance. After spin-coating, the PαMS modified substrates were baked at 100 ^{o}C for 1 hour to remove residual solvent. The PαMS film was about 8-nm-thick, and the capacitance per unit area C_i of 200 nm-thick thermal oxides with PαMS-coating layer is 1.41×10^{-8} F/cm^2 in our study.

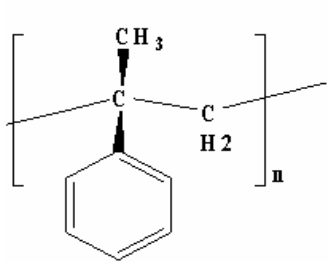


Figure 3.2 The chemical formula of poly-α-methyl styrene (PαMS). Our SiO_2 surface was modified with PαMS by spin-coating from toluene solutions.

3.1.3 Pentacene and Gold Electrode Deposition

The growth of pentacene thin film and deposition of gold electrodes were accomplished via vacuum sublimation by thermal evaporation. In the chamber, a quartz oscillator and a shutter were utilized to control the deposition rate avoiding deposition under unstable vapor flux. The deposition temperature was measured by an Al-Cr thermocouple. The pentacene source was placed in a BN-crucible and heated by a W-coil, and gold ingot was placed and heated in a W-boat.

The substrates were attached to shadow masks to define the deposited area. The 60 nm-thick pentacene (FLUKA Co., without further purification) thin-films were deposited under a working pressure below 1.6×10^{-6} Torr. During the thin film formation, the deposition rate was maintained at 0.05 nm/s, and the substrate temperature was kept at 17 ^{o}C.

Gold, as the source/drain electrode, was finally evaporated on top of the pentacene thin-film through a patterned shadow mask. The channel width (W) was 2 mm and the channel length (L) ranged from 75 to 160 μm. The device fabrication procedure is shown in Figure 3.3.

3.1.4 The Post-Annealing Treatment

To discuss the effect of post-annealing, a portion of our devices were treated by the thermal annealing process. The thermal annealing treatment was carried out at 90 ^{o}C for

80 min in a nitrogen-filled glove box. The concentrations of O_2 and H_2O in the glove box are both controlled bellow 1 ppm. After thermal annealing, the annealed samples are then cooled down naturally.

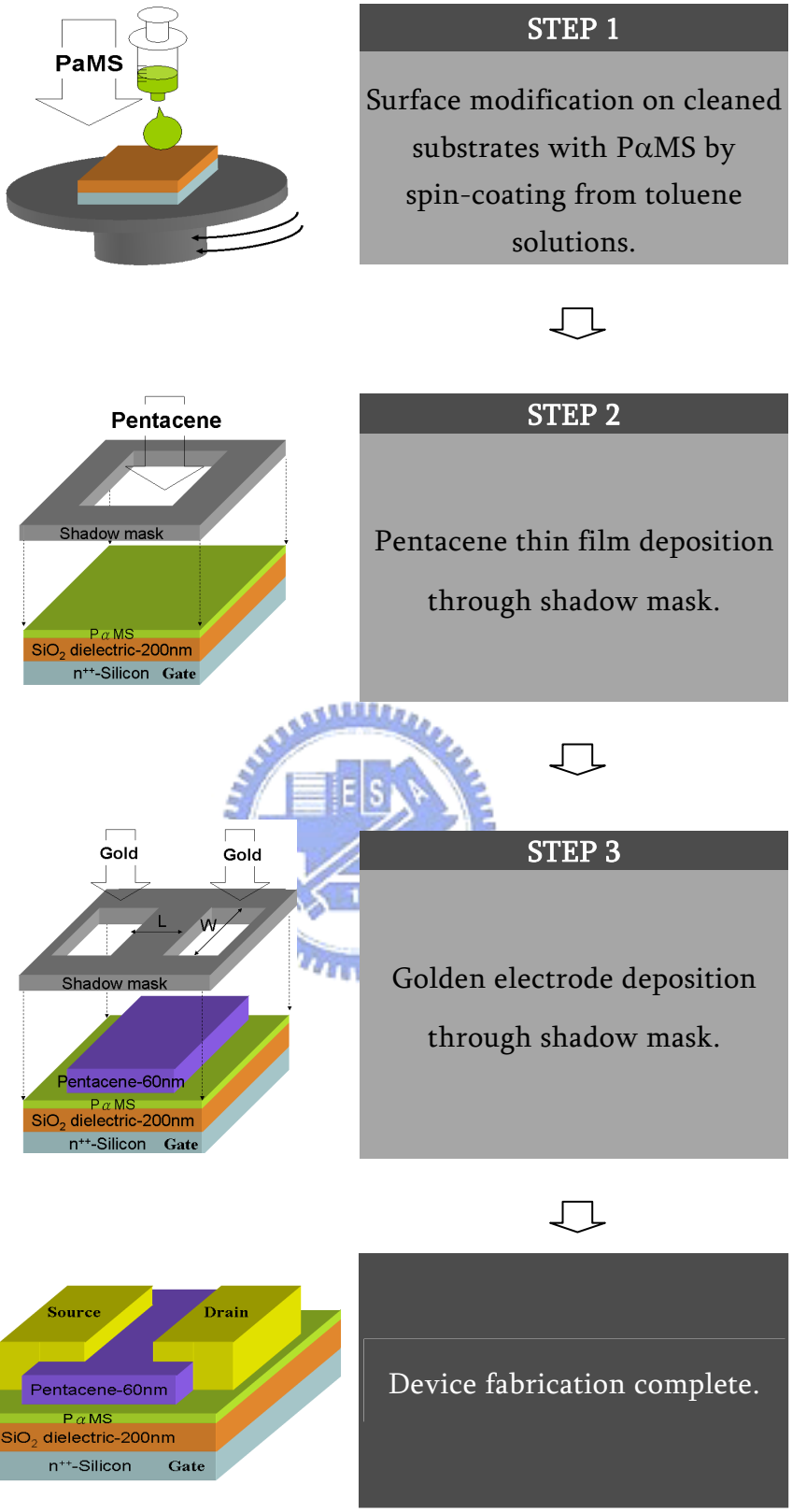


Figure 3.3 The flow chart of device fabrication. To discuss the effect of post-annealing, a portion of our devices were treated by thermal annealing process after device fabrication.

3.2 Device Measurement System

After completing the experimental process and before measuring the samples, all of our samples were conserved in the vacuum environment to avoid exposure to moisture and oxygen.

The current–voltage characteristics of this study were measured at room temperature under the atmosphere by a probe station connected with the Keithley 4200–SCS semiconductor parameter analyzer in a dark room. In the I_D-V_D measurement, the drain bias was swept from 0 to -45 Volts and the gate voltage step were 0, –15, –30, –45, and –60 Volts, respectively. In the I_D-V_G measurement, the gate bias ranged from +10 to –60 Volts, and the drain voltage step were 0, –15, –30, –45, and –60 Volts. To investigate into the effective contact resistance, the I_D–V_D curve was measured by small drain bias sweeping from 0 to –1 Volts and the step at each volt of gate voltage ranging from 0 to –90 Volts.

Chapter 4

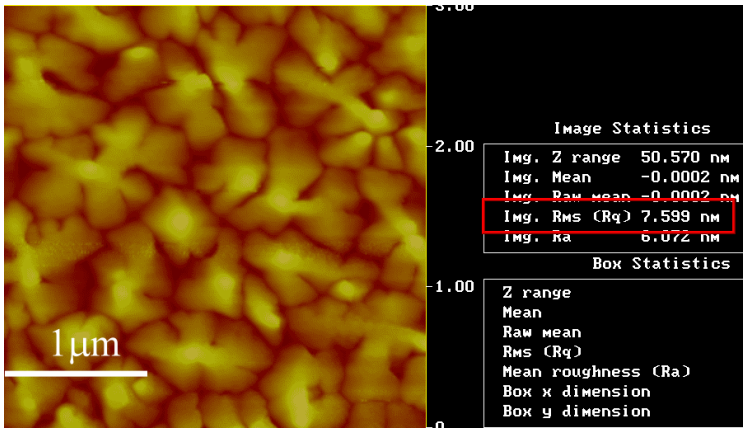
THEOREM & ANALYSIS METHOD

4.1 Morphology of Pentacene Thin Films

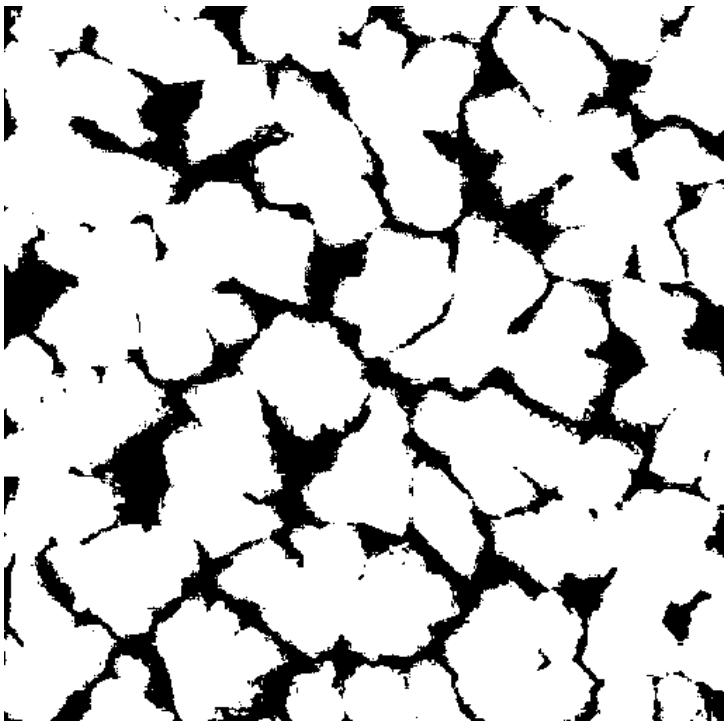
In our study, the crystal structure and morphology properties of pentacene thin film were investigated by using atomic force microscopy (AFM) and X-ray diffraction (XRD). In this chapter, the analysis methods of AFM images and the theorems of XRD-spectra analysis were investigated.

The characterization of the surface morphology of pentacene thin film was examined by AFM (Digital Instruments NanoScope Dimension D3100 probe microscope system). Each of our images was recorded in tapping mode in air with 1 Hz of scan rate and 256×256 dpi. To examine the post-annealing effect on pentacene grain in channel, in bulk, and in contact area, we prepared pentacene thin-film samples with different thickness: 5, 10, 20, 30, and 60 nm. The value of root-mean-square roughness (R_{rms}) of film was obtained by analyzing over 3×3 μm^2 area using the built-in software of the AFM instrument. Figure 4.1 displays one of the surface morphology from our samples, and a R_{rms} of 7.599 nm is obtained. Moreover, a program of MATLAB was used to calculate the density of grain boundary. The grain boundaries defined by the program were shown in the Figure 4.1 (b), and the density of grain boundary is 3.92

$(\mu m)^{-1}$.



(a)



(b)

Figure 4.1 (a) The R_{rms} of this AFM image is 7.599 nm , which was obtained by analyzing over 3×3 μm^2 area using the built-in software of the AFM. (b) The grain boundaries defined by a program of MATLAB. The detail of the program is shown in APPENDIX.

4.2 Pentacene Crystal Structure [5]

The characterization of our pentacene thin film structure was investigated by XRD, which is the direct evidence for the periodic atomic structure of crystals. The specification of XRD is M18 XHF, MacScience. The XRD measurements were performed to 60-nm thick pentacene thin films, and it was operated with Cu-Kα (λ = 1.5406 Å) radiation in a symmetric reflection, coupled θ–2θ mode. Phase identification using XRD relies mainly on the positions of the peaks in a diffraction profile and to some extent on the relative intensities of these peaks. The shapes of the peaks, however, contain additional and valuable information. The shape, particularly the width, of the peak is a measurement of the amplitude of thermal oscillations of the atoms at their regular lattice sites. It can also be a measurement of vacancy and impurity element concentrations and even plastic deformation, any factor which results in a distribution of *d*-spacings. In the following sections, we will discuss about how we analyze our XRD data.

4.2.1 Pentacene Phase - From Bragg's Law

The principle of diffraction is described by Bragg's law, which refers to the simple equation:

$$n\lambda = 2d_{hkl} \sin\theta_{hkl} \tag{4.1}$$

Intensity-peaks represent multiple lattice spacings (*d*), which can be labeled as (*hkl*) peaks. Each d_{hkl} corresponds to a specific angle (θ_{hkl}). λ is the wavelength of the

incident X-ray beam, and n is an integer. A XRD-spectrum consists of the position (2θ) and the intensity of (hkl) peaks. The former implies some information about crystal structures such as size and sharp, and the latter reveals what kind of atoms are included in a film and how these atoms arrange.

One of our pentacene X-ray diffraction (λ = 1.5406 Å) spectra is shown in Figure 4.2. Five intensity-peaks represent multiple d_{hkl}. According to the Bragg's law, (001) peak at 5.7° corresponds to d_{001} with value of 15.49 Å.

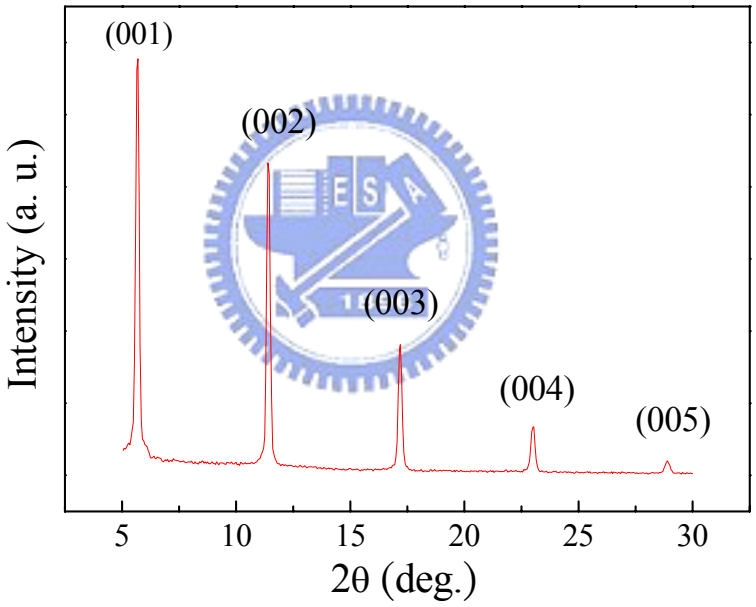


Figure 4.2 The XRD spectrum for 60-nm thick of pentacene thin films. There are five intensity-peaks, (00*l*), *l* = 1, 2, …, 5.

Similar result has been reported by C.D. Dimitrakopoulos *et al*. The value of d_{001} was found to be 15.4 Å. [4] However, the expected [32-33] single-crystal structure of pentacene in triclinic with a = 7.90 Å, b = 6.06 Å, c = 16.01 Å, α = 101.9 Å, β = 112.6

Å, and γ = 85.8 Å. In such a structure, the (*001*) plane spacing d_{001} is ~14.5 Å. Obviously, the result of d_{001} = 15.49 Å is attributed to a phase different with single crystalline phase, called "thin film phase." The other pentacene phase with (*001*) peak at 6.1° is called "bulk phase," which is closer to the (*001*) peak of single crystal phase at 6.25°. Only (*00l*) peaks are found in pentacene XRD-spectrum with the absence of any other (*hkl*) peaks, which indicates that all the pentacene crystals in the film are oriented along their (*00l*) planes parallel to the substrate.

4.2.2 Pentacene Crystal Size - From Scherrer Equation [34-35]

There are two ways to calculate pentacene grain size along *c*-axis, the Scherrer Equation and Paracrystal Theory. The crystallite size measured by the Scherrer method is given by

$$L_{hkl} = \frac{K\lambda}{\delta\theta_{hkl}\cos\theta_{\mathrm{hkl}}} \tag{4.2}$$

Here L_{hkl} is the volume-weighted size, θ_{hkl} is the Bragg angle, λ is the wavelength of the X-ray, and K is unit cell geometry dependent constant whose value is typically between 0.85 and 0.99. $\delta\theta_{hkl}$ is the full width of the peak at half maximum of Bragg's peak intensity (FWHM) in radians.

4.2.3 Pentacene Crystalline - From Paracrystal Theory [36-39]

Paracrystal theory is another way used to calculate pentacene crystal size along *c*-axis. To use both methods to verify our results becomes reliable. From the formula of paracrystal theory,

$$(\delta s)_0^2 = (\delta s)_c^2 + (\delta s)_{II}^2 = \frac{1}{\overline{L}_{hkl}^2} + \frac{\pi^4 g_{II}^4}{\overline{d}_{hkl}^2} m^4, \tag{4.3}$$

we can obtain two important parameters, $\overline{L}_{hkl}$ and g_{II}, from the intercept on the ordinate axis and the slope of the straight line determined by the least-squares fitting. Here $\overline{L}_{hkl}$ specifies the mean crystal size vertical to the plane (*hkl*), and g_{II} represents the distance fluctuation between successive planes of the family (*hkl*) or second kind of distortion of crystal structure.

Besides, $(\delta s)_c$ is the broadening associated with the size of the crystal domain, $(\delta s)_{II}$ stands for the broadening due to lattice distortions of the second kind, m is the order of the diffraction, and $\overline{d}_{hkl}^2$ is the mean spacing between (*hkl*) planes. $(\delta s)_0$ is the overall broadening excluding instrumental broadening and is further described by:

$$(\delta s)_0 = \frac{2\cos\theta_{hkl}\delta\theta_{hkl}}{\lambda} \tag{4.4}$$

where λ is the X-ray wavelength, θ_{hkl} is the diffraction angle and $\delta\theta_{hkl}$ represents the full width of the peak at half maximum of Bragg's peak intensity (FWHM) in radians.

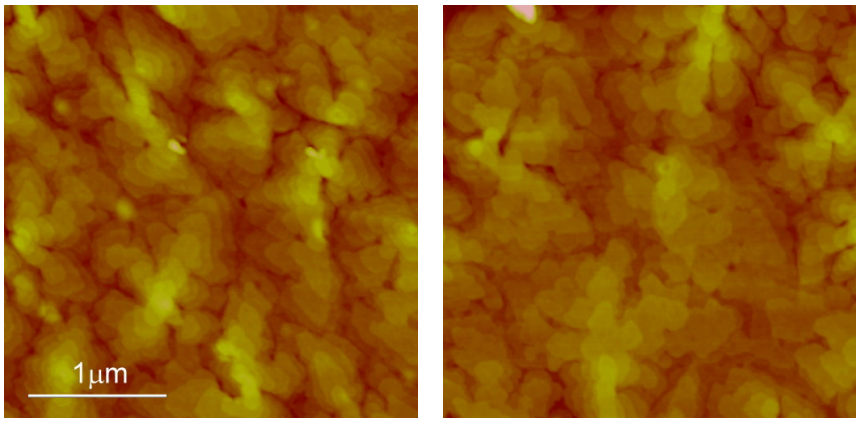
Chapter 5

RESULTS & DISCUSSION

5.1 The Effect on Pentacene Crystal

5.1.1 The Analysis of Film Morphology

Figure 5.1 (a) and 5.1 (b) show AFM images of pentacene thin films near the channel [40] for the as-prepared sample and the thermally annealed sample, respectively. From the AFM images, we can find that the layer-by-layer of pentacene growth and the grain boundary in channel became less apparent, especially after post-annealing. Pentacene grains seem to make better convection with each other and the grain size is slightly larger after thermal annealing. Further, the density of grain boundary reduces from 1.35 $(\mu m)^{-1}$ to 1.16 $(\mu m)^{-1}$ after thermal annealing, that is 14 % decrease. Since it has been reported that grain boundaries limit the charge transport in thin organic films, we can presume that the annealed device with less grain boundaries exhibits better electrical properties than the un-annealed one. [19]



(a) **(b)**

Figure 5.1 5-nm pentacene thin films for (a) as-prepared and (b) thermally annealed samples.

Figure 5.2 (a)-(f) are the images of pentacene thin films with different thicknesses and annealing condition. From the AFM images, it seems reasonable that the grain size only grows slightly, because the grain size of pentacene is dominated by the nucleation sites on substrate [41] and interaction/aggregation forces between pentacene/substrate molecules. [42] Thermal annealing treatment will not influence the number of nucleation sites.

From Figure 5.2 (e) and (f), the R_{rms} values calculated by the built-in software of AFM instrument showed that the film morphology are decreased after the thermal annealing treatment. It is well known that the rougher the surface is, the larger contact area becomes. Therefore, the contact area of pentacene/gold interface should be reduced after the thermal annealing treatment.

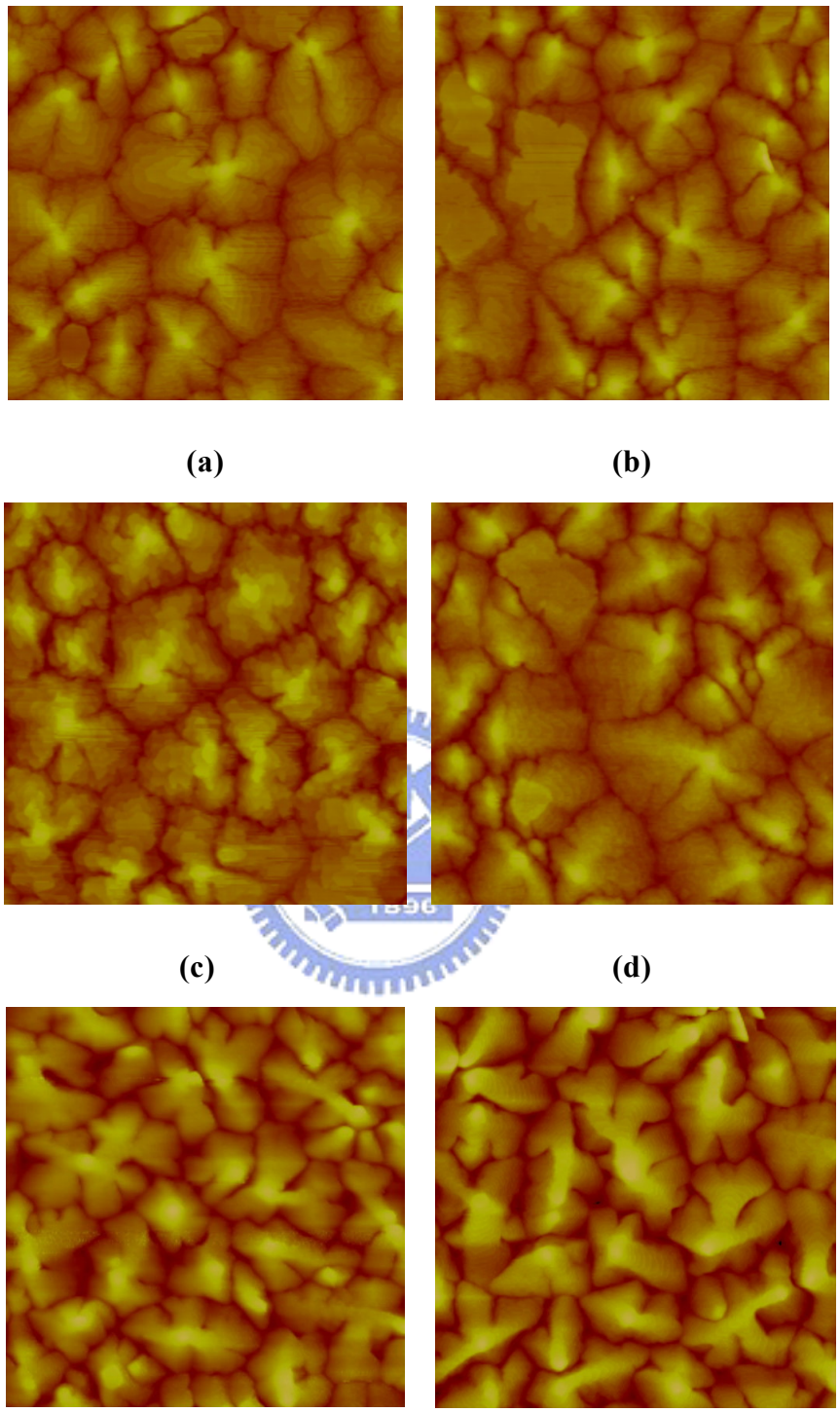


Figure 5.2 20-nm Pentacene thin films (a) as-prepared, (b) after thermal annealing. 30-nm thick samples (c) as-prepared, (d) after thermal annealing. 60-nm thick samples (e) as-prepared, and (f) after thermal annealing.

5.1.2 The Analysis of XRD spectra

XRD was carried out to study the crystal structure of the pentacene thin films, as shown in Figure 5.3. As discussed in **Chapter 4**, there are five intensity peaks and only (*00l*, *l* = 1,2,…5) peaks are found, indicating that all the pentacene crystals in the film are oriented along their (*00l*) planes parallel to the substrate. Whether the thermal annealing treatment was performed or not, only thin-film phase was observed in the spectra. This result reveals that the change of device performance is independent of the pentacene phase transition. After thermal annealing, the Bragg's peak intensity was significantly boosted, which implies the fact that thermal annealing treatment indeed improves the pentacene molecular ordering. The similar results have been proposed in reference [12].

Table 5.1 specifies the XRD parameters deduced from Equations (4.2), (4.3), and (4.4). Combined Equation (4.3) and (4.4), the following equation is obtained:

$$(\delta s)_0^2 = \left(\frac{2\cos\theta_{hkl}\delta\theta_{hkl}}{\lambda} \right)^2 = \frac{1}{\overline{L}_{hkl}^2} + \frac{\pi^4 g_{II}^4}{\overline{d}_{hkl}^2} m^4 \qquad (5.1)$$

By Substituting θ_{hkl} and FWHM of each Bragg's peak in Figure 5.3 into Equation (5.1), a plot of $(\delta s)_0^2$ versus the fourth power of the diffraction order m^4 (Figure 5.4) can be obtained. By linear fitting, $\overline{L}_{hkl}$ and g_{II} can be obtained from the intercept and slope of Equation (5.1), respectively. Both Scherrer Equation and Paracrystal Theory showed that the mean crystal size vertical to substrate is decreased after thermal annealing. The values of g_{II} below 2 % indicate that the structural perfection of pentacene crystalline is high [5]. After the thermal annealing treatment, the second kind of lattice distortion became more serious (increasing from 1.3 to 1.7 %).

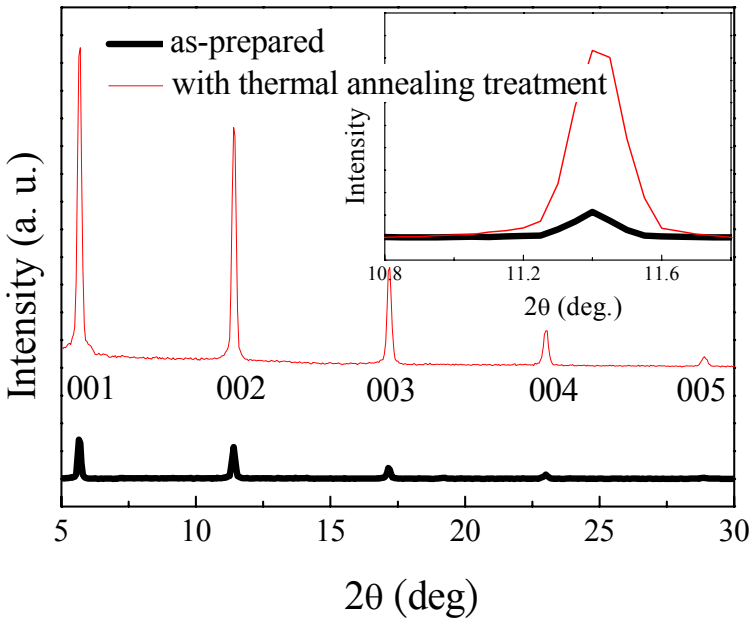


Figure 5.3 The XRD spectra obtained from 60 nm-thick pentacene films. The inset shows the XPS spectrum near (*002*) intensity peak.

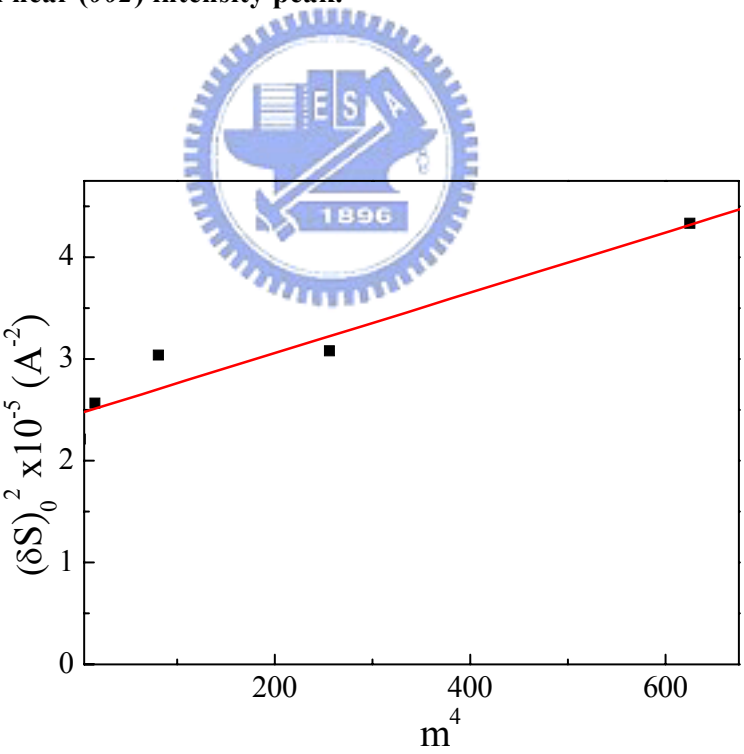


Figure 5.4 $(\delta s)_0^2$ as a function of the fourth power of the diffraction order m^4. From the intercept and slope of this plot, we can obtain the mean crystal size vertical to substrate and second kind of distortion of crystal structure.

Table 5.1 The analysis of XRD spectra.*

Condition	Intensity	FWHM (deg.)	L_{hkl} (nm)	$\overline{L}_{hkl}$ (nm)	g_{II} (%)
As prepared	575	0.136	58.0	33.0	1.3
With treatment	4333	0.229	34.5	20.5	1.7

* L_{hkl} is calculated from Scherrer Equation. $\overline{L}_{hkl}$ and g_{II} are evaluated from Paracrystal Theory.

5.2 The Effect on Device Property

5.2.1 Electrical Characteristics

In the beginning, we tried the annealing condition for different annealing temperature at 60, 90, and 120 ^{o}C for 80 min. The key results were listed in Table 5.2. We found that annealing at 90 ^{o}C gave to better device performance.

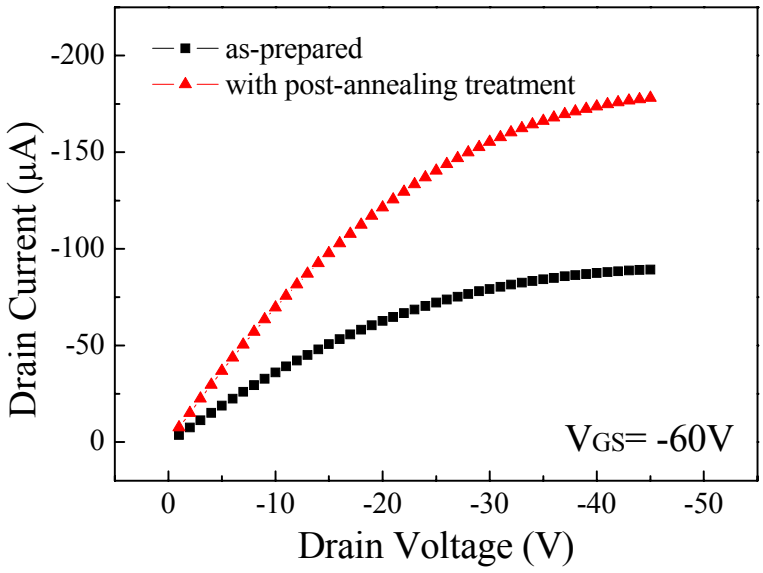
Table 5.2 The device performance*

Annealing Condition	μ_{sat} (cm^2/Vs)	V_T (V)	I_{on}/I_{off}
As prepared	0.42	-17.4	3×10^6
Annealing at 60 ^{o}C	0.54	-17.9	7×10^6
Annealing at 90 ^{o}C	0.80	-19.1	2×10^7
Annealing at 120 ^{o}C	0.49	-21.2	6×10^6

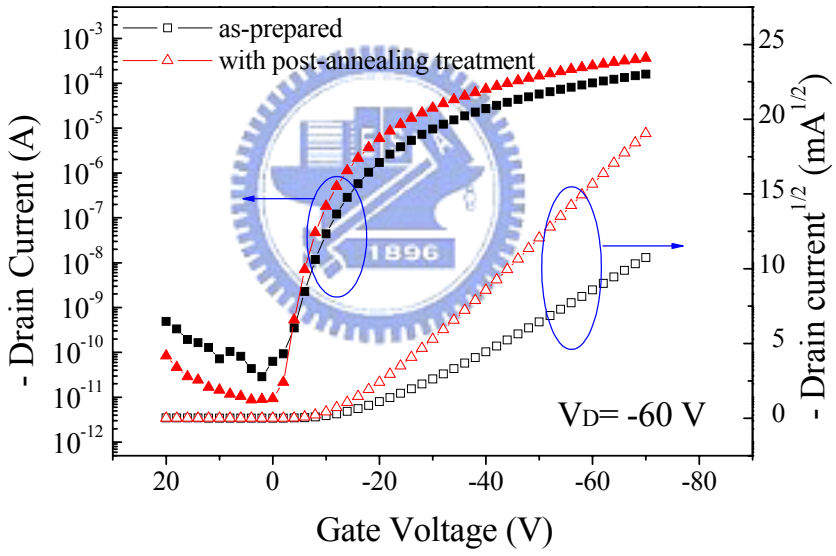
*** The device performance of pentacene-based TFT at different annealing temperature: room temperature (without annealing), 60, 90, and 120 ^{o}C, respectively.**

However, while the temperature is higher than 120 ^{o}C, the device performance degrades. Since, the best device performance was achieved at 90 ^{o}C in our experiment, so that the condition of annealing treatment was set to be at 90 ^{o}C for 80 min in the following discussions.

First, we focused on the post-annealing effect on the device performance. The resulting characteristics were presented in Figures 5.5, which exhibits the common TFT behavior as described in **Chapter 2**. The influence of the post-annealing treatment can be seen clearly. The drain current (I_D) was dramatically increased after the post-annealing treatment. The $log|I_D|-V_{GS}$ characteristics provide some information about the post-annealing effect. First, the I_{on}/I_{off} was increased by almost one order after post-annealing. The *S.S.* also decreased from 2.5 V/decade to 1.4 V/decade, and the V_T shifted from −17.4 to −19.1 V. From the $(I_D)^{1/2}$-V_{GS} characteristic, it was found that the device mobility increased from 0.42 to 0.80 $cm^2V^{-1}sec^{-1}$ in the saturation regime for V_{DS} = −60 V. Obviously, the device performance has been improved by the thermal annealing treatment.



(a)



(b)

Figure 5.5 The current-voltage characteristics of pentacene-based TFT with anneal/ un-annealed condition. (a) The drain current I_D versus the drain-source voltage V_{DS} at V_{GS} = –60 V and (b) the absolute value of the drain current and the logarithmic drain current versus the gate-source voltage V_{GS} at V_{DS} = –60 V. The post-annealing treatment was carried out at 90 ^{o}C for 80 min in a N_2-filled glove box.

5.2.2 Resistance Analysis

The device performance can be significantly improved, as mentioned above. In order to clarify the underlying mechanism, the device resistance was further investigated. Figure 5.6 shows a simplified equivalent OTFT circuit where the conducting path is divided into three parts of resistance, r_{ch}, r_C, and r_{bulk}.

As shown in Figure 5.7 (a), it is obviously observed that the channel resistance was significantly reduced after post-annealing. Accordingly, we can presume that a number of defects in the pentacene grain boundary in the channel were removed after the thermal annealing treatment. This improvement probably can be explained by the reduced number of defects existing in the grain boundary in the channel regime. The r_{bulk} and r_C were estimated by the method published by M. Shur in 1990. The concepts of M. Shur's theorem have been discussed in **Chapter 2**. According to this method, r_C and r_{bulk} can be discussed individually, and the equivalent circuit is shown in Figure 5.7(b).

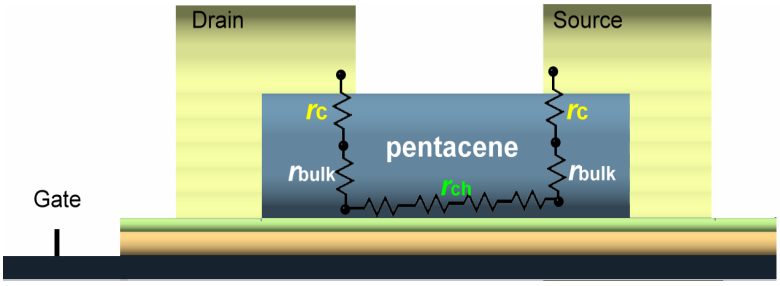
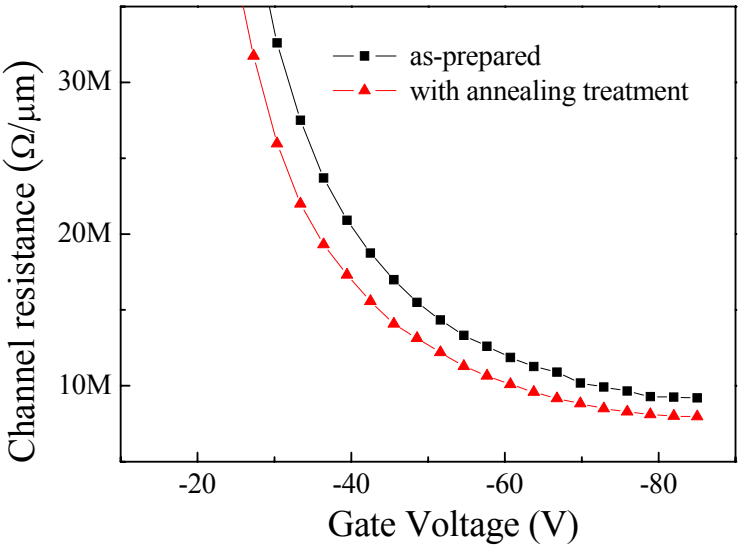
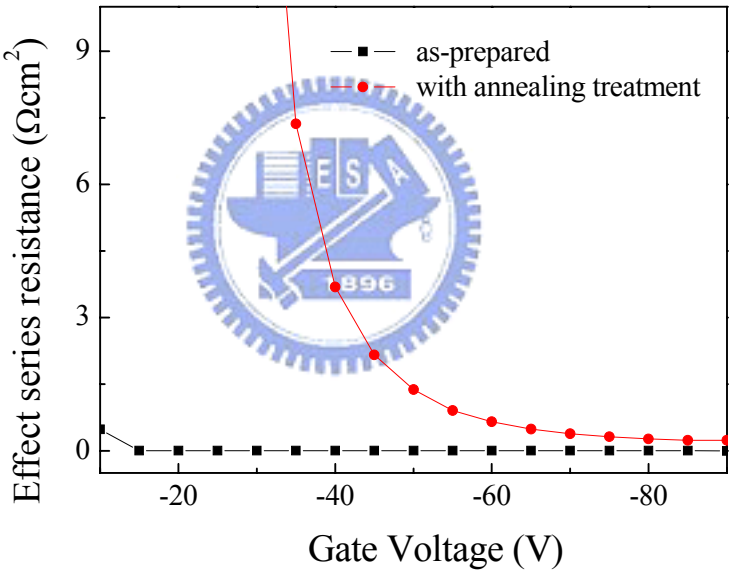


Figure 5.6 The simplified equivalent OTFT circuit, where the conducting path is divided into three parts of resistance, r_{ch}, r_C, and r_{bulk}.



(a)



(b)

Figure 5.7 Resistance characteristics of pentacene-based TFT with/without the annealing treatment. (a) the channel resistance versus gate voltage V_{GS} and (b) the effective series resistance versus V_{GS}. In our assumption, effective contact resistance r_C is V_{GS} independent and effective bulk resistance r_{bulk} is variable with V_{GS}. The effective series resistance is equal to the sum of r_C and r_{bulk}.

To simplify our problem, r_C was assumed to be independent of V_{GS}, and therefore r_{bulk} is a function of V_{GS}. Taking this assumption into consideration, r_{bulk} can be negligible as compared to r_C at high V_{GS}. The values of r_C for the untreated and the thermally annealed devices are 0.003 and 0.235 Ω-cm^2, respectively. In addition, the influence of r_{bulk} is extremely large than r_C at low V_{GS}. After post-annealing, both r_C and r_{bulk} increase, which are harmful to device performance. Combining the change of pentacene crystals and that of device performance, it is believed that the increased r_C is attributed to the reduced pentacene surface roughness. Since the contact area of pentacene/gold interface is reduced after post-annealing. Further, the increased r_{bulk} is due to the more serious lattice distortion which does not facilitate the carrier transport in pentacene.

As shown in Table 5.3, although both of r_C and r_{bulk} increased, r_{ch} decreased. For our devices, the channel lengths range form 75 to 160 μm. The decreased amount of r_{ch} is much more than the increased sum of r_C and r_{bulk}. Therefore, the total resistance of pentacene-based TFTs is decreased after post-annealing treatment. However, it must be noticed that the reduced degree of r_{ch} is much smaller than the increased degree of $\mu_{sat.}$ Accordingly, some other factors are expected to influence the device performance. The DC stress degradation on the OTFT devices was subsequently performed.

Table 5.3 The key parameters of devices*

Annealing Condition	μ_{sat} (cm^2/Vs)	r_C (Ω-cm^2)	r_{bulk} (Ω-cm^2)	r_{ch} ($M\Omega/\mu m$)
As prepared	**0.42**	**0.003**	**0.007**	**11.9**
Annealing at 90 °C	**0.80**	**0.235**	**0.432**	**10.1**

*** The resistance of device with different annealing condition obtained under $V_{GS} = -60$ V.**

5.2.3 DC Stress Degradation

The I_D of the TFTs was measured under a continuous DC voltage biases of $V_{GS} = -30$ V. As shown in Figure 5.8, the post-annealing treatment is effective in the reduction of DC stress degradation from more than 50 % to less than 40 %. It is believed that the change of DC bias stress is associated with the traps induced by molecular defects, disorder, and/or impurities. Deep trapping of carriers lead to a decrease of I_D. [26] As a result, the reduction of defects can relieve the phenomenon of charge trapping, thus improving the device stability under DC stress and device performance.

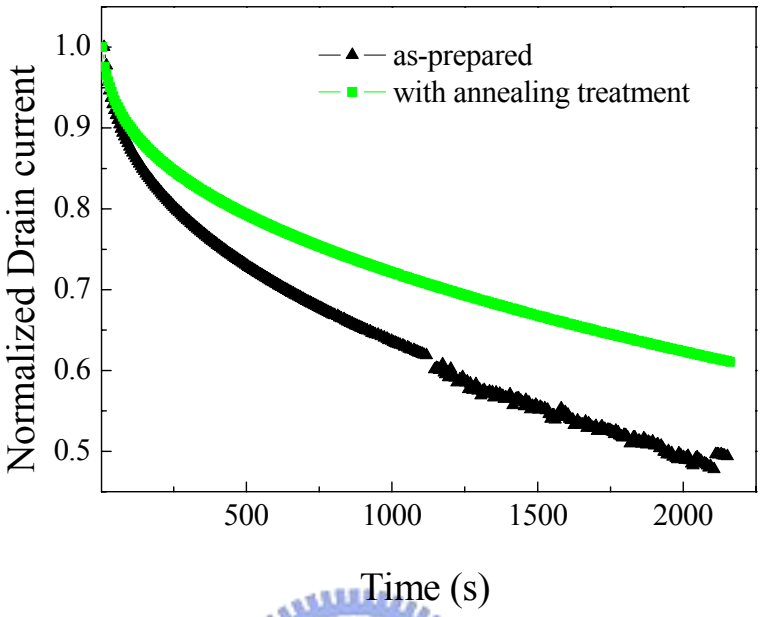


Figure 5.8 The DC stress of the pentacene-based TFTs. The continuous DC voltage bias was V_{GS} = –30 V lasting for 2500 sec.

5.3 Trap Calculation

In the previous sections, the changes of electrical properties, AFM images, and XRD patterns after the post-annealing treatment were systematically studied. In the following parts, experimental results were further discussed by the trap calculation.

5.3.1 Grain Boundaries

The grain boundary trap density (N_{GB}) can easily be estimated from the fitting of the Levinson plot of $\ln(I_D / V_{GS})$ versus $1/ V_{GS}$. [43-44] Here I_D can be approximated by

$$\ln\left(\frac{I_D}{V_{GS}}\right) = \ln\left(\frac{W\mu_{GB}V_D C_i}{L}\right) - \frac{q^3 N_{GB}^2 d}{8\varepsilon kTC_i}\left(\frac{1}{V_{GS}}\right) \tag{5.2}$$

The Levinson plot for our devices is shown in Figure 5.9. According to Equation (5.2) and the slopes of Figure 5.9, N_{GB} of un-annealed and annealed devices are calculated to be 2.6×10^{12} cm^{-2} and 2.3×10^{12} cm^{-2}, respectively. The 11.5 % reduction of N_{GB} proves that traps in grain boundaries are decreased after post-annealing. This result explains why the device performance and channel resistance are improved. From AFM images and XRD spectra, the reduced trap density must be attributed to the decreased *GB* density of AFM images.

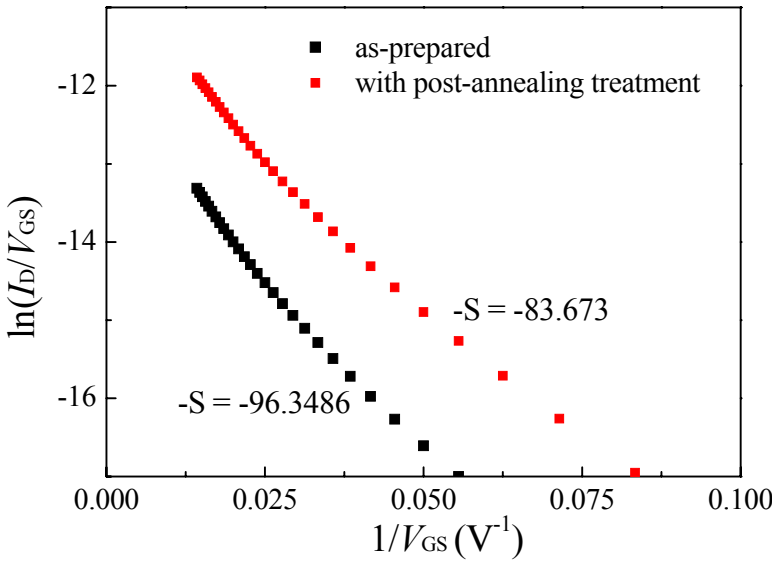


Figure 5.9 Levinson plot of "$\ln(I_D/V_{GS})$ vs. $1/V_{GS}$" for our devices. For these two samples, the trap density at the grain boundary can be estimated by the slope of this diagram.

5.3.2 Interface

For further investigating, we focus on the interface quality of pentacene and PαMS-modified SiO_2. The maximum interface trap density ($N_{it(max)}$) could be estimated by the approximation [45]:

$$N_{it\,(\max)} = \left(\frac{S.S \cdot \log(e)}{kT/q} - 1 \right) \times \frac{C_i}{q} \tag{5.3}$$

where Ci is the capacitance per unit area, k is Boltzmann's constant, T is the absolute temperature, and $S.S$ is the minimum sub-threshold swing deduced from the transfer curve of devices. From our calculation, the approximate $N_{it(max)}$ of PαMS-modified devices was decreased from 3.60×10^{12} $cm^{-2}eV^{-1}$ to 1.97×10^{12} $cm^{-2}eV^{-1}$ after

post-annealing treatment. The decrease of $N_{it(max)}$ might be due to the surface modification of PαMS at the pentacene/SiO_2 interface. The glass transition temperature (T_g) of PαMS at atmosphere is 85 °C. Above T_g, PαMS becomes soft and behaves as rubbery state. During the thermal annealing treatment, the soft PαMS could make the interfacial adhesion better. Defects and voids near the interface are extensively removed and filled, respectively, after the post-annealing treatment, which leads to the decrease of the r_C and $N_{it(max)}$. Further, we made a comparison of devices with and without surface treatment in Table 5.4.

Table 5.4 The parameters of devices with/without surface treatment*

Annealing Condition	Surface treatment	μ_{sat} (cm^2/Vs)	$N_{it(max)}$ ($cm^{-2}eV^{-1}$)	r_{ch} ($M\Omega/\mu m$)
As prepared	no	0.11	6.64×10^{12}	54.2
	PαMS	0.42	3.60×10^{12}	11.9
Annealing at 90 °C	no	0.14	5.54×10^{12}	52.7
	PαMS	0.80	1.97×10^{12}	10.1

*** The device properties were obtained under $V_{GS} = -60$ V.**

The surface treatment is indeed helpful to the decrease of interface traps. The $N_{it(max)}$ of devices without surface treatment was only 17 % decreased after post-annealing. On the contrary, $N_{it(max)}$ of devices with surface treatment was

extremely decreased by 45 % after post-annealing. By combining surface treatment with post-annealing treatment, the $N_{it(max)}$ was significantly decreased by 70 %. Obviously, surface treatment not only improved the device performance but also enhanced the degree of the improvement induced by the post-annealing effect.

5.3.3 Summary

The surface roughness of pentacene at the pentacene/gold interface was decreased after the annealing treatment, leading to a decrease of contact area. This explained the increase of contact resistance. Through the XRD analysis, the lattice distortion became seriously after thermal annealing. The serious lattice distortion gave rise to the increase of bulk resistance.

After thermal annealing, the AFM images showed that the *GB* density was decreased, and the N_{GB} was proved to be decreased from Equation (5.2) In addition, the $N_{it(max)}$ at pentacene/insulator interface was also decreased. The reduction of traps must lead to a decrease of the channel resistance. Furthermore, the reduction of DC stress degradation also explained the reduction of defects and traps. The decrease of $N_{it(max)}$ was more distinct than that of N_{GB}, showing that the post-annealing effect on pentacene/insulator interface was the most critical to the device performance.

Chapter 6

CONCLUSIONS

In this study, we controlled the morphology of pentacene through the post-annealing treatment, followed by studying the correlation between the thin-film morphology of pentacene and TFT device performance. The aims of our research are to find out the effect of post-annealing treatment on the device performance, pentacene crystal structures, and their correlations.

After the post-annealing treatment, the device mobility increased from 0.42 to 0.80 $cm^2V^{-1}sec^{-1}$ and the device became more stable. After investigating the mechanism, the results indicate that thermal annealing treatment reduces the number of defects in the grain boundaries and pentacene/PαMS-modified-SiO_2 interface, leading to the reduction of channel resistance and trap density. Further, results reveal that surface modification of PαMS not only improved the device performance but also enhanced the degree of the improvement induced by the post-annealing effect.

After post-annealing, the decrease of film roughness leads to a raised contact resistance, and the lattice distortion leads to an increased bulk resistance. The increased contact and bulk resistance prohibit the efficiency of charge injection from gold to pentacene and charge transport inside the bulk of pentacene thin-film (perpendicular to the device substrate), respectively. Further, the problem of the increased resistance will

become more noticeable when decreasing the channel length of OTFTs. Therefore, it is necessary to find ways to decrease the bulk and contact resistance.

If we combine post-annealing treatment and other methods, like modification of the pentacene/gold interface, [46] which can enhance the charge injection from gold to pentacene, a better device performance and device mobility higher than 0.80 $cm^2V^{-1}sec^{-1}$ can be expected.

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APPENDIX

The program defines the density of grain boundary from the N × N matrix of AFM images. The authors thank Miss. Ying-Pin Chen for programming.

```
function GB_count (file)

rgb=imread (file);
rgb=imresize(rgb, [512 512]);
r=rgb(:,:,1);
gray2log=(r>131);                          % the pink value should be modulated
                                           % to a proper image.

figure; imshow(gray2log);                  % for user to judge the pink value

[u,v]=meshgrid(-255:256, -255:256);        % to define a space for Fourier
highpass=1-1./(1+(sqrt(u.^2+v.^2)/60).^4);   transform
                                           % highpass filter
F=fftshift(fft2(double(gray2log)));
y=real(ifft2(fftshift(highpass.*F)));

Y=(y>0.1);                                 % to show the pattern obviously


image_i = Y;
dimension = size(image_i);
target = 0;                                % to count how many white pixels is
```

```
for i=1 : dimension(1,1)
       for j = 1 : dimension(1,2)
             if image_i(i,j) == 1
                          target = target + 1;
            end;
     end;
end;

ratio = target/(dimension(1,1)*4)              % 4 makes the result to a unity
```