

# 介面信號相位鎖定之低溫多晶矽電晶體電路之研究

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## 摘要

顯示器中的電路如：數位/類比轉換器, 畫素驅動電路, 移位暫存器, 以及許多利用低溫多晶矽電晶體已經被提出相關解決元件變動性所造成電路上的問題。但是在顯示器中一樣重要的介面電路卻很少被提及。在這論文中, 提出一個用於顯示器介面電路上, 介於影像訊號源跟積體電路中間的鎖相迴路電路被當成時脈產生器使用來討論。

論文中目的在於討論在介面電路上使用低溫多晶矽電晶體來實現的相關問題, 而我們主要討論在介面上把鎖相迴路電路當作時脈產生器使用上的各種問題, 並使用模擬的方式將各個電路作妥善的調整達到對元件的變動性有很高的容忍度。有部分的電路在經過實際製作之後量測得到妥善的結果, 希望在之後能夠達成整個系統在小尺寸低功率面版上實現。

# **A low temperature polycrystalline silicon thin film transistor circuit used for interface signal phase locking**

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## **Abstract**

Circuits in a display panel such as digital-to-analogue (D/A) converter, pixel driving circuit, shift register, and several buffer circuits based on LTPS TFTs have been proposed to solve the problem of device variation. Many circuits have been proposed to solve the problem of device variation for the LTPS TFT. However, the interface circuit is seldom mentioned. In this thesis, a LTPS TFT phase locked loops (PLL) circuit is proposed to be a clock regenerator for the usage at the interface between the video source and the integrated circuit on a panel.

This thesis aims at the discussion of interface circuit of display panel realizing by LTPS TFT. Specifically, we focus on the clock regenerator using PLL in the interface. Furthermore, each circuit is adjusted to be of high tolerance with device variation. Some of circuits have been measured and works functionally. It is expected to realize proposed PLL on small size and low power consumption display panel.

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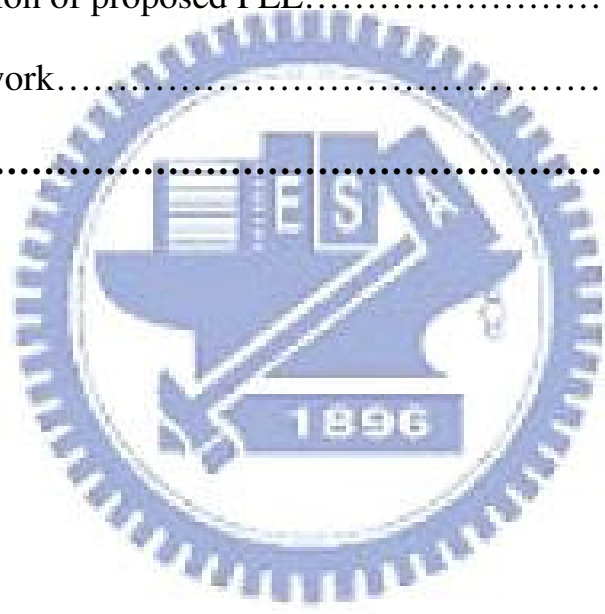
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