

# Chapter 1

## Introduction

### 1-1. Development of Displays

In recent years, with the flat-panel display technology development, flat-panel displays have replaced the traditional cathode ray tube (CRT) application for many aspects. Liquid crystal display (LCD) is one of the popular displays. Especially, thin film transistor liquid crystal display (TFT-LCD) is the most common display at present. According to the manufacture technique of thin film transistor (TFT), the TFT-LCD was categorized into amorphous-silicon (a-Si) TFT and low-temperature poly-silicon (LTPS) TFT and high-temperature poly-silicon (HTPS) TFT.

Among these TFTs, LTPS has been widely investigated as a material for mobile applications such as digital cameras and note book computers. In polysilicon film, the carrier mobility larger than  $100 \text{ cm}^2/\text{Vs}$  can be easily achieved, that is about 500 times larger than that of the conventional amorphous-silicon TFTs and fast enough to make peripheral driving circuit including n- and p-channel devices. This enables the monolithic fabrication of peripheral circuit and TFT array on the same glass substrate, bringing the era of system-on-glass (SOG) technology [1]. There are considerable interests in poly-Si thin film transistors (TFTs) because of their wide application in active matrix liquid crystal displays (AMLCDs) [2]. They also have been applied into some memory devices such as dynamic random access memories (DRAMs) [3], static random access memories (SRAMs) [4], electrical programming read only memories (EPROMs) [5], electrical erasable programming read only memories (RRPROMs) [6], linear image sensors [7], thermal printer heads [8],

photo-detector amplifier [9], scanner, neural networks [10] and three dimension LSIs [11].

In the future, the application fields of LTPS TFTs will not be limited to displays but will be expanded to other electronic devices, such as LSIs [11], printers and sensors. Among these, the application of poly-Si TFTs in AMLCDs is most noticeable and brings about rapid process in poly-Si TFT technology.

Therefore, it is possible to integrate poly-Si TFTs and surrounding driving circuit on the same substrate. This will reduce the assembly complication and the cost dramatically. In addition, since the mobility of poly-Si is higher, the dimension of poly-Si TFTs can be made smaller than that of amorphous silicon ones. This is beneficial to fabricate high density and high resolution AMLCDs.

## 1-2. LTPS TFTs

LTPS TFT technology appears to be one of the most promising technologies for the ultimate goal of building fully-integrated AMLCD system on glass. The LTPS TFT LCDs achieve high resolution, high luminance displays as well as “System on glass” displays, which allow us to integrate various functional circuits on display panels. The so-called system on glass (SOG) TFT-LCD with LTPS technology enables to spare the silicon driver ICs and to enhance the productivity by reducing the module process steps. System-on-panel (SOP) has the merits of high brightness, low power consumption, thin thickness, light weight, fast response, high integration, high reliability, and good image quality. Comparing with the conventional a-Si TFT LCD with silicon ICs on it, the SOG-LCD requires high-performance TFTs such as high carrier mobility ( $\mu$ ), low threshold voltage ( $V_T$ ), and large sub-threshold swing to meet the high speed driving circuits that result in good display quality and a small

form factor. The LTPS TFT has also the possibility for realizing far more value-added circuit monolithically with the pixels on the array glass. Therefore, the research efforts also have been focused on realization of system integration for LTPS TFT LCDs and have been developed various types of circuit-integrated LCDs so far.

### **1-3. Integrated Circuit of System on Panel**

Fig.1 shows the system block diagram of this panel. As shown in Fig.1, this panel consists of the following seven circuits: the interface circuit for changing input logic level to higher level needed for TFT circuitry, the timing generator for generating control pulses for drivers, the reference driver for generating 64-step voltage, the VCOM driver for generating common voltage, the source driver for supplying analog voltage to source lines according to input digital signals, the gate driver for selecting gate lines, and the DC-DC converter for supplying negative voltage of gate drivers. The signal processing in the module works with following flows. Data signals are supplied to a driver IC from an external circuit by way of the following interfaces (I/Fs) including parallel CPU I/F or serial CPU I/F or RGB I/F. Then the signals are stored to frame memories. Data signals in the frame memories are read out at a constant frequency, and then transferred to D/A converters, which output data to an LCD panel. Output signals include serially composed RGB signals.

The most fundamental display driver circuit (for both active- and passive-matrix displays) is the shift register. Assuming the simplest driving scheme, the rows and the columns of the display matrix are activated one by one, which is accomplished by the active shift register output (which can be high or low level signal) being shifted to the next bit, and eventually cycled to the register's input (Hsync or Vsync) again.

When the characteristics of the LTPS TFT are improved by the evolution of the design rule and processing, the high-speed operation of the circuit becomes possible.

It means that shift registers can be operated easily more than MHz. However these circuits appear to succeed the application of real products suffers from significant high variation of threshold voltage and mobility.

## 1-4 Motivation

Circuits in a display panel such as digital-to-analogue (D/A) converter, pixel driving circuit, shift register, and several buffer circuits based on LTPS TFTs have been proposed to solve the problem of device variation [13]. Through the design, the issue arisen by device variation and many hedges have been adopted to avoid variation is discussed. Many circuits have been proposed to solve the problem of device variation for the LTPS TFT. However, the interface circuit is seldom mentioned.

The interface part of display is responsible for transmitting signals from video source to the display panel. In the interface circuits shown in Fig1-4.1(a) and Fig1-4.1(b), phase locked loop (PLL) is both in the part of graphics IC and the timing controller (TCON). Every time when images change on display, circuits start working and sending order signals to change voltage amount on pixels. The interface circuits transmit clock, synchronous signals, and different color pixel changing amount signals to the TCON part, through the process voltage on pixels change according to the order signals coming from graphics IC and traveling to the TCON part.

In this thesis, a LTPS TFT phase locked loops (PLL) circuit is proposed to be a clock regenerator for the usage at the interface between the video source and the integrated circuit on a panel. PLL in interface part avoids phase difference from graphic IC by correctly regenerating input signals. Namely it is used as a clock regenerator to receive signals from graphic IC part and regenerates them at the TCON

part.

This thesis aims at the discussion of interface circuit of display panel realizing by LTPS TFT. Specifically, we focus on the clock regenerator using PLL in the interface.

## **1-5 Test sample Preparation and Thesis Organization**

About the verification test, the process flow of top gate LTPS TFTs is described below. Firstly, the buffer oxide and a-Si:H films with thickness of 50 nm were deposited on glass substrates with PECVD. The samples were then put in the oven for dehydrogenation. The XeCl excimer laser of wavelength 308 nm and energy density of  $400 \text{ mJ cm}^{-2}$  was applied. The laser scanned the a-Si:H film with the beam width of 4 mm and 98% overlap to recrystallize the a-Si:H film to poly-Si. After poly-Si active area definition, 100 nm  $\text{SiO}_2$  was deposited with PECVD as the gate insulator. Next, the metal gate was formed by sputter and then defined. For n-type devices, the lightly doped drain (LDD) and the n+ source/drain doping were formed by  $\text{PH}_3$  implantation with dosage  $2 \times 10^{13} \text{ cm}^{-2}$  and  $2 \times 10^{15} \text{ cm}^{-2}$  of  $\text{PH}_3$  respectively. The LDD implantation was self-aligned and the n+ regions were defined with a separate mask. The LDD structure did not use on p-type devices. The p+ source/drain doping was done by  $\text{B}_2\text{H}_6$  self-align implantation with a dosage of  $2 \times 10^{15} \text{ cm}^{-2}$ . Then, the interlayer of  $\text{SiN}_x$  was deposited. Subsequently, the rapid thermal annealing was conducted to activate the dopants. Meanwhile, the poly-Si film was hydrogenated. First of all, the PLL circuit and each block functions of it are discussed. Next, the discussion on tolerance of device for is discussed in the third chapter. Finally, the conclusion and future work is given in chapter fourth.

The thesis outlines are listed below:

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## Chapter 2

### Phase Locked Loop Circuit

#### 2-1. Function Blocks of Phase Locked Loop

Fig2-1.1 shows a referred configuration of PLL, which is composed of five individual blocks, namely, phase and frequency detector (PFD), level shifter, charge pump, voltage-controlled oscillator (VCO), and frequency divider. Each part will be discussed in the aspects of its function in PLL, typical circuit design and the improvement we proposed to solve device variation in detail in the following sections. Here we briefly describe the operation of a PLL circuit. PLL uses PFD to detect phase error between input signal and clock regenerated by VCO. With the detecting function of PFD, a caution signal can occur to indicate the relationship between input signal and clock. These caution signals are enlarged by level shifter and translated to a level signal by charge pump. Charge pump sends this level signal to VCO which controls the frequency of the output clock. Before clock compared to input signal in PFD, divider is used to divide the output signal of frequency to proper range with respect to the input signal. In this thesis, the variation induced from LTPS TFTs is considered in implementation. Target of this thesis is to complete a PLL functionally at a 3.3V input clock signal with 2MHz frequency.

Referring to the configuration shown in Fig2-1.1, our approaches to improve the PLL are based on two concepts. First, we implement circuit by logic method as possible. Because output signals of logic circuits which are in the form of high and low voltages are not easily affected as much as to the opposite logic level by device



variation. Second, for the circuit can not be implemented by logic ones, match TFTs are most adopted once it is proved that devices within small range have minimum variation.

## **2-2. Phase and Frequency Detector (PFD) circuit**

A PFD circuit detects the phase difference of the input signals. The input signals of PFD are initial input signal and clock regenerated by PLL. The output signal is a caution signal to be the input of level shifter.

A PFD shown in Fig2-2.1 has an input signal and a reference signal as inputs, and an output signal to indicate the difference of input signals. Fig 2-2.2 illustrates the relationship of input and output signals in the time chart. The output signal sets at low state when there is no phase error between input signals and delivers pulse when phase error appears. In such a way, PFD translates the phase difference between the input signals to a caution signal in the form of pulses.

Fig 2-2.3 shows the schematic diagram of one popular design of PFD called Gilbert cell, which is based on two source follower circuits with four input nodes and two output nodes. The input of the Gilbert cell are in the form of logic differential signals. Gilbert cell detects the leading of  $V_{in1} (+)$  to  $V_{in2} (+)$  in the left part of circuit and detects the leading of  $V_{in1} (-)$  to  $V_{in2} (+)$  in the right part in the same configuration. Its output is also a differential signal between the two output nodes. Fig2-2.4 illustrates the input signals with different phases to the Gilbert cell and shows the corresponding wave forms of output signals in (a) and (b), respectively.

For general purpose, Gilbert cell is designed to detect input signal leading or lagging cases. But PFD detects leading and lagging cases like Gilbert cell may be too complicated. Furthermore, Gilbert cell relies much on the device uniformity for its

complicate structure.

As far as what PFD provides is a function of detecting phase matching of input signals and provides the caution signal. In our assumption, the signals used in interface circuit can be pulse form treated as logic signals. Though some interfaces use differential input signals, we assume the logic signals can still be used. LTPS circuit handles signal with relatively low frequency about several MHZ.

Therefore a logic approach is adopted here. Referring to Fig 2-2.2, to achieve the specific goal, a logic equation is derived:

$$\text{Output} = (A \otimes B) \dots (1)$$

We use a XOR gate as equation (1) at first to detect the phase matching of 2 input signals where A is input signal and B is the regenerated clock respectively. As mentioned, Gilbert cell detects both leading and lagging part, so the pulses corresponding to the case of leading or lagging are distinguished by adding and an AND gate as equation (2) and equation (3). Equation (2) shows the connection of detecting leading of signal A, and equation (3) shows the connection of detecting lagging of signal A.

$$\text{Output} = (A \otimes B) \cdot A \dots (2)$$

$$\text{Output} = (A \otimes B) \cdot B \dots (3)$$

The logic equation (2) can be further reduced as equation (4).

$$(A \otimes B) \cdot A = (A \cdot \bar{B} + \bar{A} \cdot B) \cdot A = A \cdot \bar{B} \dots (4)$$

And the logic equation (3) can also be further reduced.

Fig2-2.5(a) illustrates the input signals of the logic equation (4), and Fig2-2.5(b) illustrates the output signals of the logic PFD circuit.

In order to examine the function of the circuit, layout and sample fabrication of

EQ(4) are completed. Fig 2-2.6 shows the measurement result where input A and B both the same signal source and output signal is observed to be logic 0. Fig2-2.7 and Fig2-2.8 further show two other connections of conditions. In Fig2-2.7, input B a pulse as shown in the upper of picture, while input A stays logic high. As can be seen, an output with inverse phase of B for this test, verifying equation (4). In Fig2-2.8, the input A is set to logic low and input B keeps a periodic pulse. The output is at logic 0 as expected. The function of the proposed logic PFD is therefore verified. Fig 2-2.9 is the layout picture of PFD.

### 2-3. Level shifter circuit

In the reference PLL, the output signal of PFD is also the input signal of level shifter, while the output of level shifter is the input signal of charge pump. After PFD, level shifter raises signals to a proper range. Furthermore it is expected to eliminate a error signal arisen from unexpected reasons such as electromagnetic interference (EMI).

Based on the idea, a level shifter adopted to test in our circuit is shown in Fig 2-3.1. It compares the caution signals from PFD and a DC voltage. And the difference of caution signal from PFD and DC voltage descides the current on drain side. The Current flow on M1 induce a voltage drop on resistance R which equals the gate input voltage difference of four match TFTs in Fig2-3.1. If M1 receives a signal at low state, most of current flows to M2 and the ouput signal is set at low state. On the contrary, M1 receives a signal at high state, most of current flows through M1 and outputs signal at high state. Through the procedure, only when caution signal from PFD is larger than DC voltage the output signal sets to high, and the error signal is eliminated. Fig 2-3.2 shows the simulation result which input signal is only 3V

comparing to the DC voltage of 1.5V an output signal about 18V. Fig 2-3.3 is the layout picture of the level shifter.

But in consideration of our target of 2MHz input signal and capacitor induced from combination with other circuits in PLL, the falling edge of output signal is bended as shown in Fig 2-3.2. For this reason, another level shifter circuit [12] is chosen to replace as shown in Fig 2-3.5. With a 4V reference voltage in Fig 2-3.4, a 3.3V input signal can be raised to 17V as shown in Fig 2-3.5. With matched TFTs of same parameters used in circuit, the variation induced from device is expected to be eliminated.

## 2-4. charge pump circuit

Fig 2-4.1 shows a schematic of charge pump used as a level shifter. When PFD sends a caution signal to level shifter, level shifter changes output signal states under different situations as following :

Situation (a):  $V_{UP}=V_{DN}=0$ , implies VCO and REF is at the same phase and VCI remains the same as previous.

Situation (b):  $V_{UP}=1, V_{DN}=0$ , implies REF leads VCO and VCO should increase frequency so that VCI increases.

Situation (c):  $V_{UP}=0, V_{DN}=1$ , implies VCO leads REF and VCO should decrease frequency so that VCI decreasing.

As shown in Fig 2-4.2, a charge pump circuit proposed [13] [14] [15] to turn input pulses into levels is proposed here. With two different input nodes representing

signals to pull output high or pull down separately, this circuit outputs ascending levels or falling levels. In our designation, the output signal from PFD provides caution signal to increase or decrease VCO output frequency. Thus the charge pump receives two different input signals separately and sends different output levels. Fig 2-4.3 shows the output signal of receiving pull high and pull low signal in (a) and (b) separately. Fig 2-4.3(a) shows the output signal when input signal is a pull low signal and (b) shows the output signal when input signal is a pull high signal. This circuit can output ascending levels and falling levels according to different input signals. And with matched TFTs applied, it is expected to perform well under variation situation.

## **2-5. Voltage-Controlled Oscillator (VCO) circuit**

The input signal of voltage controlled oscillator (VCO) is the output signal of charge pump. In PLL, input signal compared with clock which is regenerated by VCO. VCO produces pulse of different frequency according to different input signal from charge pump. In our design, VCO keeps on producing higher frequency pulse until PFD receives two signals of matched phase. At the same time VCO outputs pulses of same frequency unless input signal changes.

At first, the circuit shown in Fig 2-5.1 [16] is evaluated. It is a ring oscillator composed of 3 inverters. A voltage input connecting all the gate nodes of the NTFT in the inverter chain is used to control the drain current. By controlling the discharging current with different voltages at the gate, pulse with different frequencies can be created. This design puts high emphasis on the working point of each inverter. But in considerations of the high device variation of LTPS TFT and the small range of linear region of each inverter, this circuit is not suitable.

Next, another VCO circuit shown in Fig 2-5.2 is investigated. This circuit is based on Schmitt-Trigger which is shown in Fig2-5.3(a). Fig.2-5.3(b) shows the relationship between input and output signals of Schmitt-Trigger. When Schmitt-Trigger receives an increasing input signal, its output signal starts to increase. After input signal increases over a specific range and the output voltage will keep at its maximum. Output signal starts to fall while input signal is getting lower. Once input signal is lower than a specific range the output signal starts to decrease. In the VCO circuit, the output signal of Schmitt-Trigger is sent to the gate of the transistor MR shown in Fig2-5.2. When output signal of Schmitt-Trigger is at its high state, and the current at the drain side of TFT MR increases. The current discharges the capacitor in VCO, which will decrease the input signal of Schmitt-Trigger at the same time. When the input signal falls, the output signal of VCO will also decrease. The decrease of the output voltage reduces the current at drain side of TFT MR. And capacitor is charged with the current induced by VCO input. Thus the input of Schmitt-Trigger increases toward its high state. Through the steps, the periodic pulses can be made.

When device variation is considered, the diamond shaped working graph of the Schmitt-Trigger changes its width between falling and rising edges. This phenomenon causes changing on trigger point of starting falling or rising. Thus the frequency of output pulses of VCO is affected. And the issue of variation will be discussed in chapter 3.

As for the realization of the VCO circuit, it is expected to measure the output pulses with different frequencies according to the different DC input voltages. Fig 2-5.6 shows the results measured with several DC input according to the voltages from 5V to 19.1V and the frequency increases with the input signal voltages. Fig 2-5.7 shows the simulation result graph of relationship between input signal voltage and output

signal frequency. This figure shows the output frequency decreasing with the increasing of input signal voltage. Fig2-5.8 shows the picture of layout of VCO.

## 2-6. Divider circuit

In PLL, the frequency of signal produced by VCO can be manipulated by the frequency divider, and the frequency divider is usually implemented by a counter and a path with a reset function. Fig 2-6.1(a) shows a circuit of divider. The counter is counting from 0 to 7 set by S0, S1 and S2, and a reset function is presented. QA, QB, and QC in Fig2-6.1 are the output signal after dividing. For example, when S1, S2, and S3 are all set to 1 (logic high), the frequency of QC is the seventh of input clock from VCO. When S1 and S2 are 0, S3 is 1, the frequency of QC is the fourth of the input clock from VCO.

Fig2-6.1(b) shows another type of the counter using D-type flip flop. As discussed above, a counter made of flip-flop changes different type through different control signals easily. Divider divides clock into parts to catch on input signal according different S inputs as shown in Fig 2-6.1. One way to define S to divide clock is to find the relationship between input signal of PFD and external clock signal. And we use the relationship to define S shown in Fig2-6-1. The other way is to assume the input signal frequency range and design corresponding VCO and divider. In our design, counter with an outward clock dose not meet our goal to regenerate clock by PLL itself. And the frequency range of our input pulses is predicted, thus an adjustable counter is not as well as important here. So a divider without an external clock which only divides input signal frequency into half is adopted.

Fig 2-6.2(a) shows a divider adopted in our PLL which is a T-flip flop. The logic algorithm of divider is shown in Fig 2-6.2(b). With its characteristic of changing

every next output only when input is at its logic high. This provides a 50% duty-cycle signal with half frequency of input signal. Fig 2-6.3 shows the simulation result of input signal and output signal. For its simple logic structure, divider proposed here is expected to have high tolerance of device variation.

Fig 2-6.4 shows the measured result of input signal and output signal of divider. Fig 2-6.5 is the layout picture of divider. Owing to an error in the layout, we did not succeed in the measurement.

## 2-7. Proposed PLL Configuration

These sections above show how PLL does to generate a clock and the function of each building block. According to the referred PLL some adjustments are adopted with the same blocks in Fig 2-1.1, Fig 2-7.1 shows the adjustment from Fig2-1.1.

First, in section 2-4 the input signal of PFD is 10V pulse but our target is to handle 3V input signal. In order to meet the target, a level shifter changes to the first block of PLL. For the configuration in Fig 2-1.1, the referred PLL requests input signal high enough to be detected by PFD. This modification can change input signals level from 3V to specific voltage level for PLL.

Second, the pull down and pull high signal of charge pump is considered in a different way. In our designation, proposed VCO decreases output signal frequency with increasing input voltage as shown in Fig2-5.7. Thus, the output signal of charge pump called “pull high” and “pull down” represent the opposite meanings in our PLL.

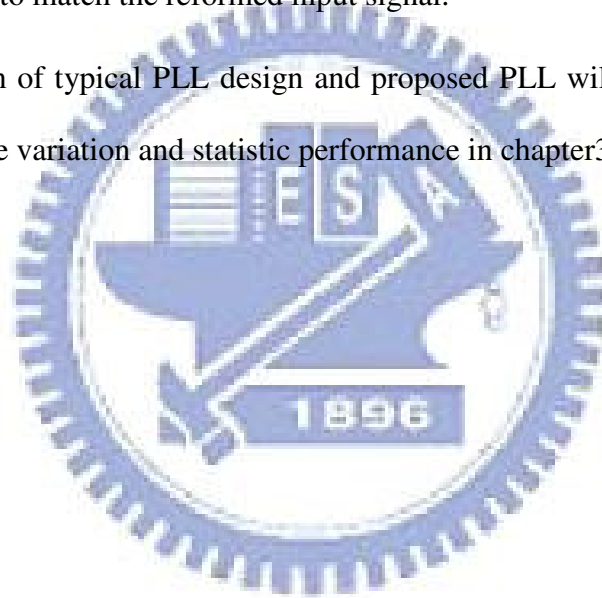
Third, the special situation of 2 different duty-cycles but same frequency pulses as shown in Fig 2-7.2. In order to prevent this situation, a divider is added before PFD to reform input signal to 50% duty-cycle. Besides, 2 dividers are connected to output of VCO for 50% duty-cycle and transmit the clock to PFD to match input signals



without changing the settings of other blocks in PLL.

Accordingly, the function and the settings of each block are not basically changed, either. The new organization of each block and the corresponding roles are shown as below. Level shifter and divider reform the pulse of input signal in our new configuration. PFD detects the match of reformed input and clock regenerated by VCO and sends a caution signal to charge pump. Charge pump and VCO create different frequency pulses until PFD detects two matched signals. Before clock regenerated by VCO is detected by PFD, two dividers are sequentially connected to change frequency to match the reformed input signal.

The comparison of typical PLL design and proposed PLL will be discussed about tolerance of device variation and statistic performance in chapter3.



## Chapter 3

### Discussions on device variation of circuits

This thesis aims at the discussion of interface circuit of display panel realizing by LTPS TFT. And this section discusses simulation under the situation with device variation and the hedges taken for each block.

Before individual evaluation in detail, a brief analysis is performed conceptually. The variation of output signal of logic circuits is less important than other circuit, for the variation seldom changes the logic of signal. So, the divider and PFD proposed are expected with high tolerance of device variation. Next, circuits like level shifter and charge pump with pair TFTs of matched parameters with simple structure are expected to works functionally with small variation on output voltage level. Thus VCO is identified as the main source of variation on PLL. The detail discussions are as follows.

#### 3-1. Level shifter circuit

Fig 2-7.1 shows the proposed PLL, and a level shifter is put at the first block for receiving 3V input signal without changing settings of other circuits. Fig 3-1.1 shows the simulation result with no device variation, which input signal is a 3 V pulse and output signal is about 16V pulse signal.

In device variation simulation we take both n type and p type TFT variation of mobility and threshold voltage into consideration. The detail conditions are shown as

below:

$$\mu_0 = \mu_0 \pm 10\%$$

$$V_{th} = V_{th} \pm 1V$$

The variation range of mobility is 20% of its average value and the threshold voltage is  $\pm 1V$  of its average value. With device variation, the whole simulation uses the method of Monte Carlo in H-spice. With this method computer randomly chooses different parameters for both n and p type TFT in the range shown above according to the probability of Gaussian distribution.

After Monte Carlo simulation of 40 times, Fig 3-1.2 shows the simulation result on level shifter which the high state of output voltage varies 0.26 volt from the highest to lowest and the low state of output varies almost 0V from the highest to lowest. Parameters used in simulation here for the TFT pairs are assumed to be matched as described in section 2-1, for which the circuit is less affected by device variation.

Through device variation test, it is shown that level shifter proposed here less depends on device uniformity.

### 3-2. PFD circuit

Logic equation of PFD proposed in section 2-2 is as below:

$$\text{Output} = (A \otimes B) \cdot A$$

$$\text{Output} = (A \otimes B) \cdot B$$

A represents the regenerated clock by VCO and B represents input signal. According to our design, the AND gate enables PFD to detect two different types of phase unmatched with these two equations separately and sends a caution signal. And the following discussion on variation focuses on the equation below:

$$(A \otimes B) \cdot A = (A \cdot \bar{B} + \bar{A} \cdot B) \cdot A = A \cdot \bar{B}$$

Fig3-2.1(a) shows 2 input signals and Fig3-2.2(b) shows the output signal. Without device variation applied, it is shown that PFD proposed here provides significant output signal for usage as discussed in section 2-2. The PFD proposed is expected to have high tolerance of device variation for its logic design.

Under the same condition and method in section 3-1, Fig 3-2.2 shows the result of Monte Carol 40 times of simulation. The output signal of PFD logic high level varies about 0.3 V, and Fig 3-2.3 shows logic low level of PFD which varies about 1 V. According to the simulation result, it is revealed that device variation does not affect the circuit performance enormously.

### 3-3. Divider circuit

Without using tunable divider, a T type flip-flop divider is adopted in our proposed PLL. Divider discussed here is shown in Fig2-6.2(a) and its logic algorithm is shown in Fig2-6.2(b). With the characteristic that output signal changes only when input signal is at its high level, thus a signal with half frequency of input signal and 50% duty-cycle can be achieved.

Fig 3-3.1 shows the simulation result of divider without device variation. Under same condition in section 3-1, the result of individual circuit variation test of 40 times Monte Carol simulation is shown in Fig3-3.2. Through the individual circuit simulation, it is proved of its high tolerance of device variation which perfectly output signal with half frequency of input signal and 50% duty cycle.

Accordingly, circuits of logic design are expected with high tolerance of device variation which are examined as above, and other circuits are evaluated as main

sources of variation discussed in the following sections.

### **3-4. charge pump circuit**

Fig 3-4.1 shows the simulation result of output signal with no device variation applied for the charge pump circuit which translates input pulses into levels. According to limitation of device shown in section 3-1, by using the same method to examine the charge pump proposed here. Fig3-4.2 shows the result of simulation under device variation for pulling low, and Fig 3-4.3 shows the case of pulling high. The part of pulling down reveals variation of 1.3V and the part of pulling high varies as large as 0.64V. The variation of charge pump affects the output voltage, thus the time for input voltage of VCO set to correct voltage is affected. Though the function of charge pump performs well under device variation, the effects on PLL should be noticed and valued with respect to other building blocks together.

### **3-5. VCO circuit**

In our proposed PLL, the clock regenerated by VCO highly influences the performance of PLL. VCO is adopted to create pulses of different frequency according to different input signal levels. A VCO circuit based on ring oscillator and a control port added to change the charging and discharging time to adjust the frequency of output signal as shown in Fig 2-5.1. Fig 2-5.2 shows the proposed VCO which is expected to have high tolerance of device variation. Fig3-5.1 shows the simulation result which turns input DC signal into pulses. According to the same method to simulate under variation situation as before, Fig 3-5.2 shows the result under 40 times of variation test. But it is hard to define caliber of variation, so by tracing current of capacitor of VCO proposed shown in Fig 3-5.3 which shows 0.124

mA difference between the largest and the smallest currents at same time in simulation. The difference of 0.124mA makes a 30KHz difference on frequency which equals to 1.5% variation of our 2MHz target.

After the device variation simulation toward every individual circuit in PLL, whole PLL is taken into consideration in the next section.

### **3-6. Evaluation of proposed PLL**

Typical PLL is shown in Fig2-1.1 and through some adjustments a proposed PLL is shown in Fig2-7.1.

In the aspect of variation, issues of device variation and prevention for each circuit have discussed in previous section. Fig 3-6.1 shows the proposed PLL, with a simple classification the path can be sorted to 2 different types. Type (a) path represents way from logic circuit to logic circuit which also less influenced by device variation. Only path from VCO to divider of type (a) is from normal circuit to logic circuit, but divider divides input signal into half frequency as shown in Fig 3-6.2 which is not affect by device variation as discussed in section 3-3.

As mentioned before, circuits in proposed PLL implemented by logic way as possible and other circuits are pair TFTs with matched parameters to ease the amount of variation. Path type (b) represents way from normal circuit to normal circuit. The output variation of PFD is the input of charge pump which influence the time for charge pump to meet specific output range. The output variation of charge pump decides the output frequency of VCO thus induced variation of steady time of PLL. For the purpose above the variation of PLL mainly relies on the variation of charge pump output which influences the output frequency of VCO.

In the discussion of variation, the amount of variation should focus on the

relationship between the variation of VCO input and the frequency variation according to the input voltage. Section 3-4 shows the output of charge pump varies 0.64V for pulling high and 1.3V for pulling down. The corresponding output frequency variation of 0.64V and 1.3V swing from 10V is 0.04% variation which is almost equal to simulation result with all devices in proposed PLL varying.



## Chapter 4

### Conclusion and Future work

#### 4-1 Conclusion of proposed PLL

In the beginning, our target is to handle 3V input signal with 2MHz and high tolerance of device variation. But with device limitation, the target is not achievable.

Fig 4-1.1 shows the wave forms at 3 specific nodes. Namely, Fig 4-1.1(a) is the output of charge pump, as shown in the figure it is not at steady state. Fig4-1.1(c) is the output of 2 dividers, which shows that dividers fail to divide immediately. For the delay from divider, PFD always detects signals unmatched as shown in Fig4-1.1(b). So the divider with logic way is not available for input signal of 2MHz. With a compromise of input signal frequency to 200KHz, Fig4-1.2 shows the simulation result of charge pump output signal wave form. The swing of charge pump output signal induces at most 47% variation of output frequency but PFD receives signals from VCO varies less than 47% for the transmission delay.

#### 4-2 Future work

A LTPS PLL circuit is proposed to be used as clock regenerator with high tolerance of device variation. In the realization, some of the blocks have been measured with correct result, but all system does not meet the initial target of 2MHz input signal. PLL proposed here works under a not perfectly balance with a variation of output signal but the tolerance of device variation is eliminated. So, it is expected to realize



proposed PLL for high input frequency and more steady output frequency.



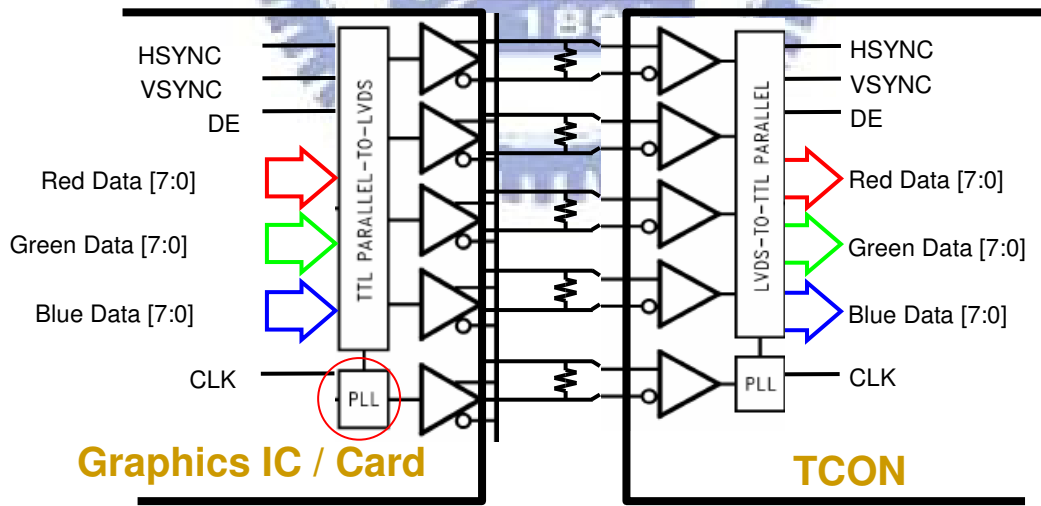
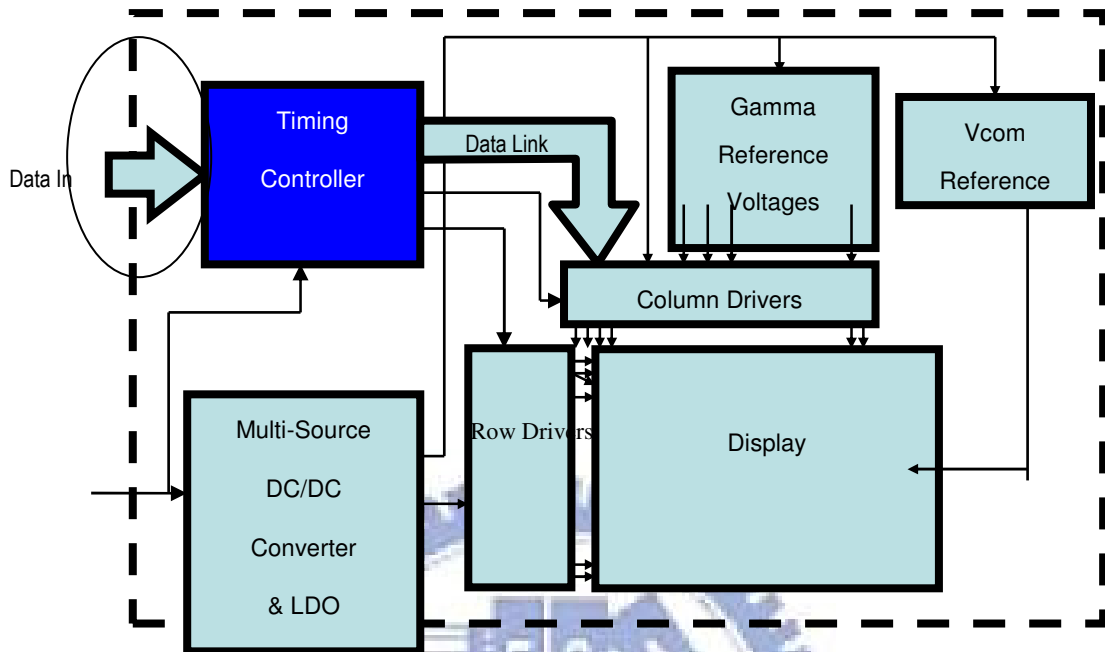


Fig1-4.1(a) A system block of a display and the circle is the interface part and (b) the interface part.

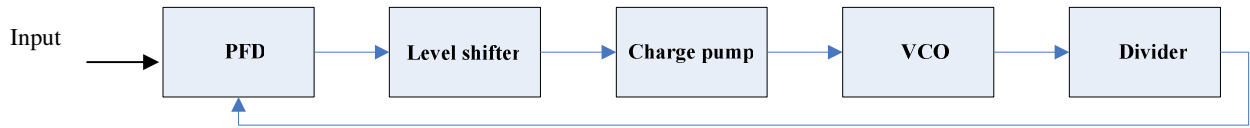


Fig2-1.1 Block diagram of PLL.



Fig2-2.1 PFD with 2 input nodes and an output node.

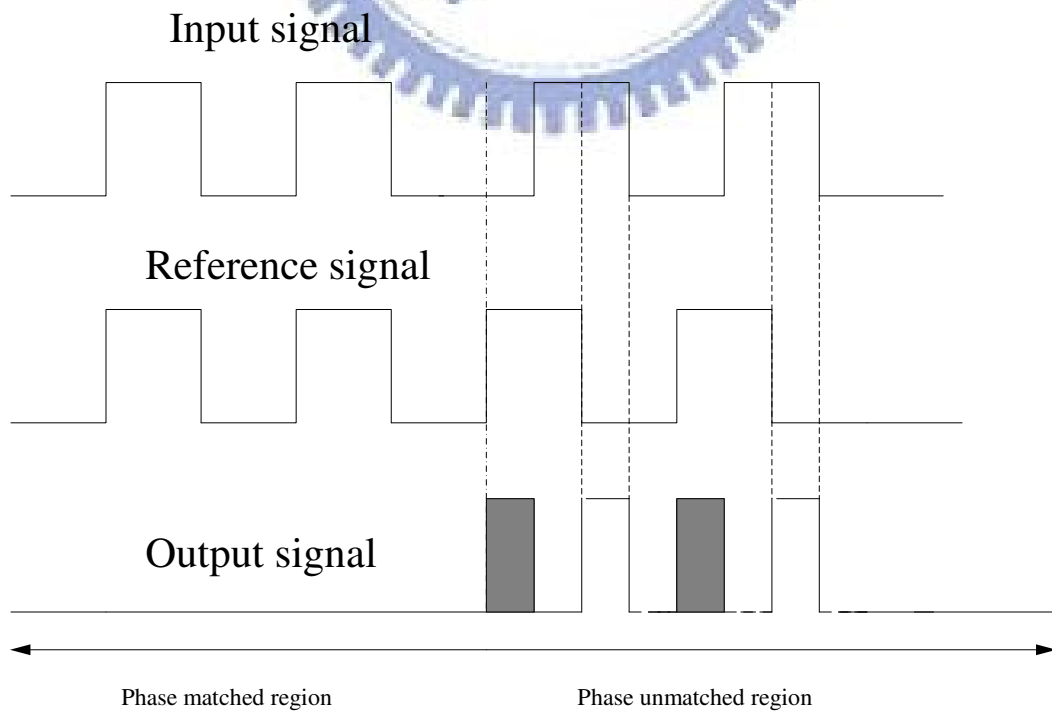


Fig2-2.2 Time chart of the input and output signals for a PFD.

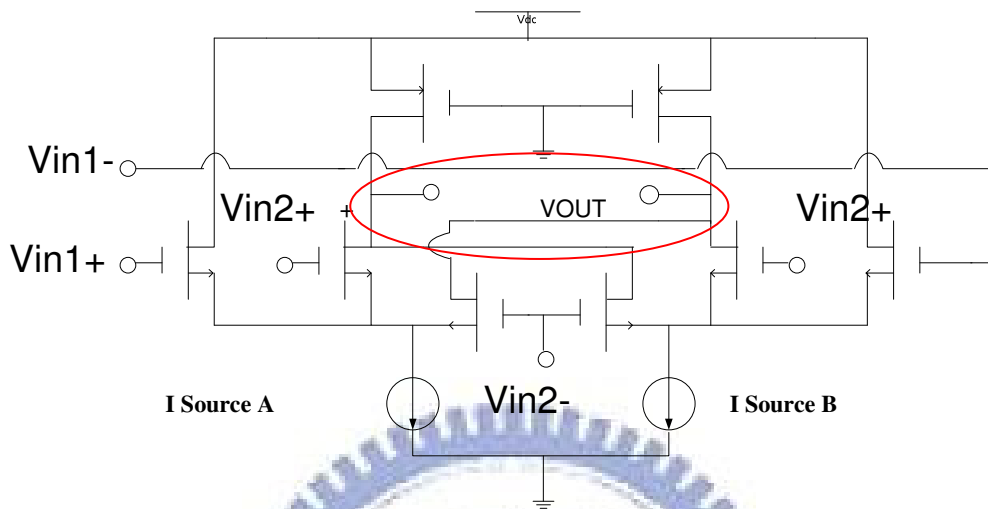


Fig 2-2.3 A typical Gilbert cell schematic diagram.



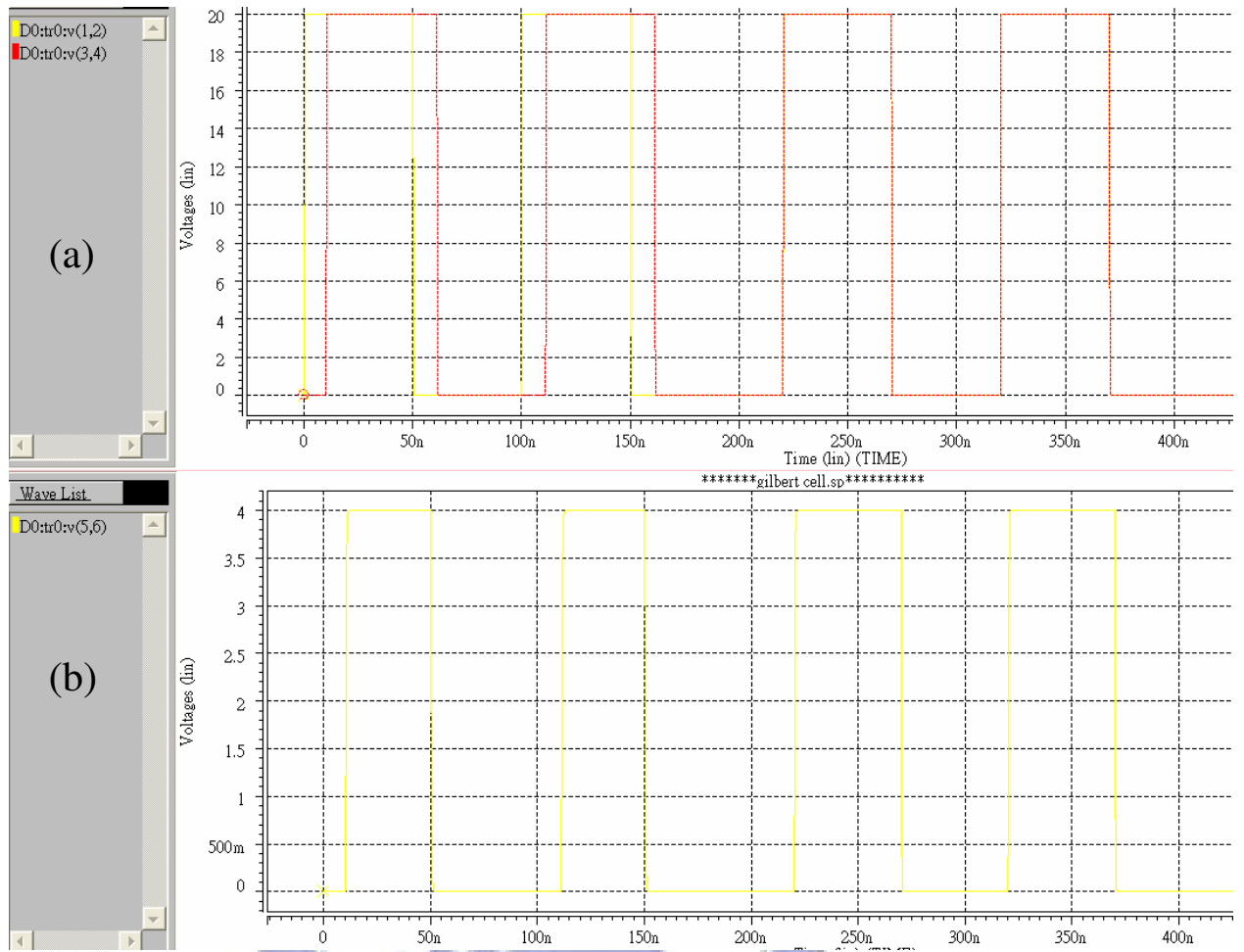
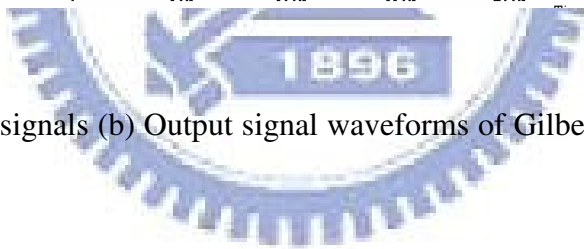


Fig 2-2.4 (a) Input signals (b) Output signal waveforms of Gilbert cell PFD simulated by H-spice.



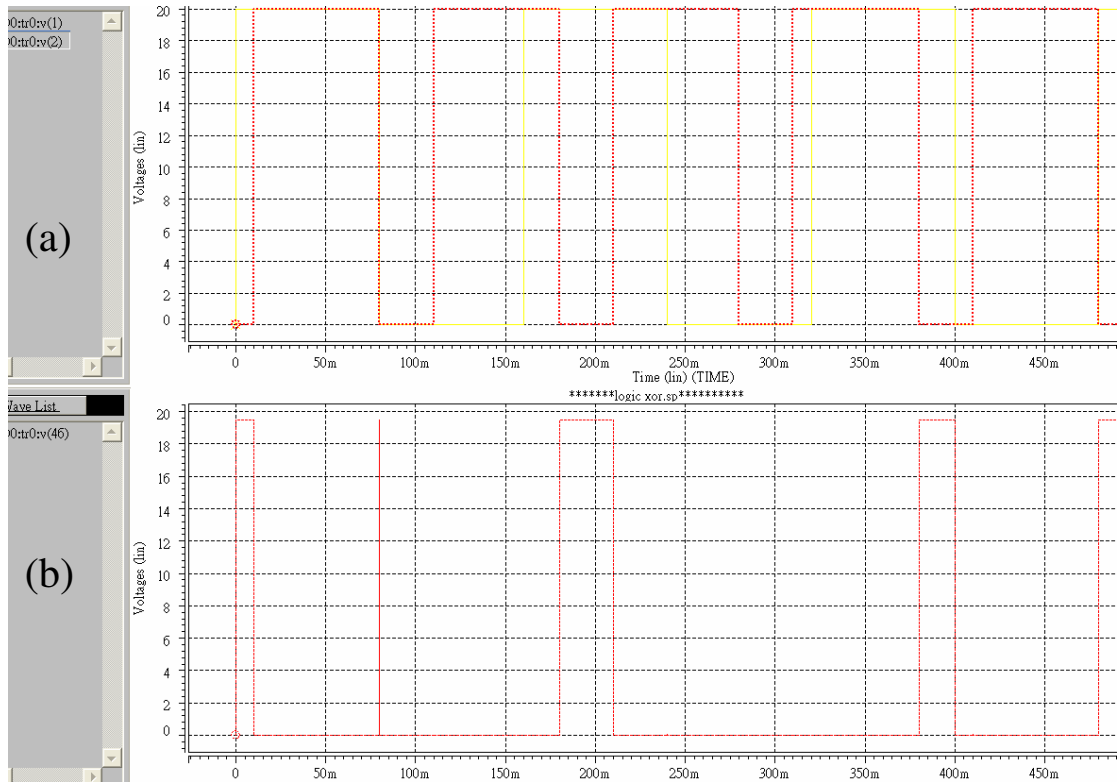


Fig 2-2.5 Logic PFD simulation result, (a) Input signal and (b) Output signal.

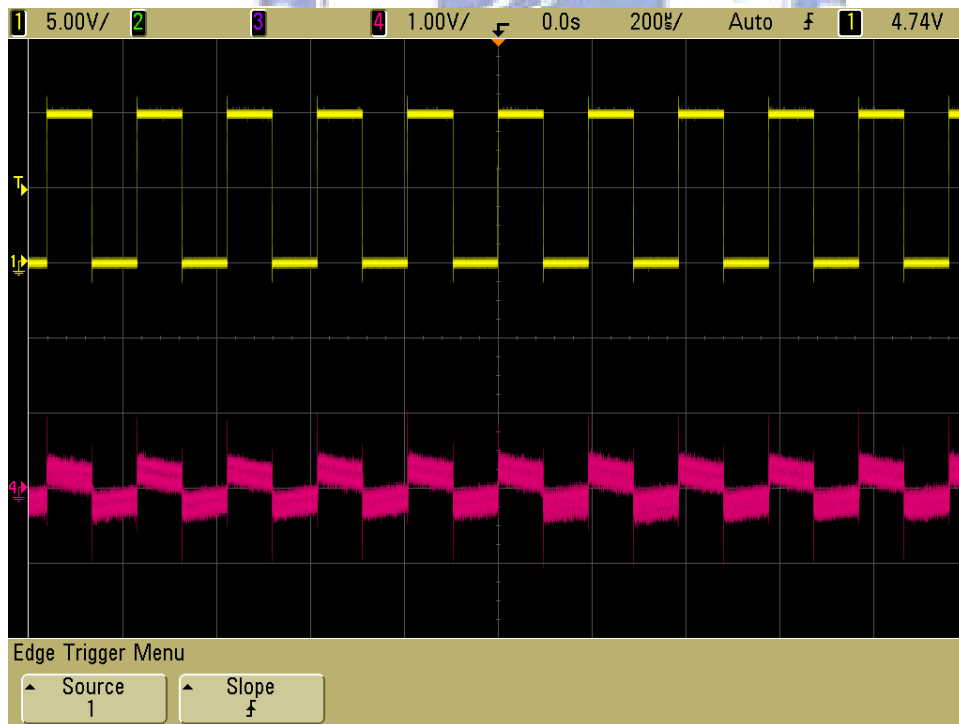


Fig 2-2.6 Measured result with 2 inputs of the same signal and the output at logic 0.

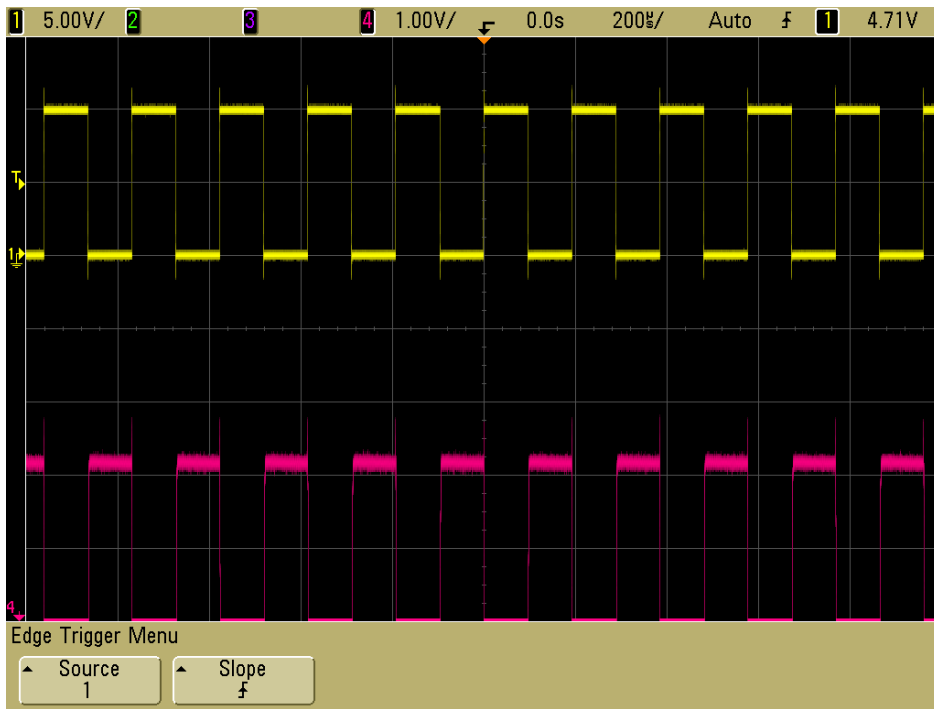


Fig 2-2.7 The measurement results of logic PFD circuit with input A of logic high, input B of pulse, and the correct output to be the inverse of input B.

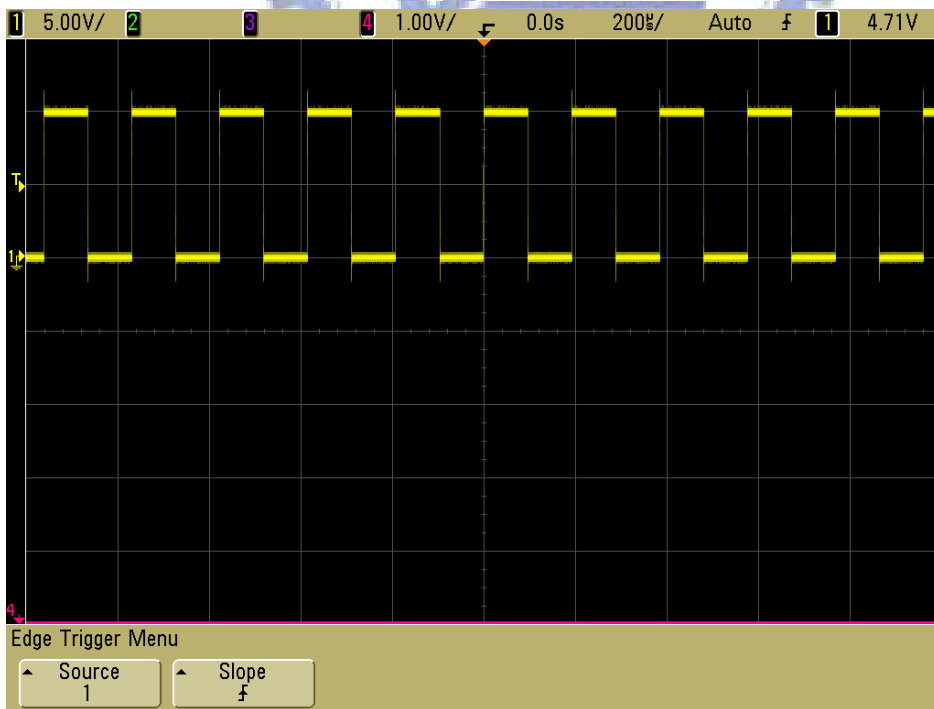


Fig 2-2.8 The measurement results of logic PFD circuit with input A of logic low,

input B of pulse, and the correct output to be logic 0.

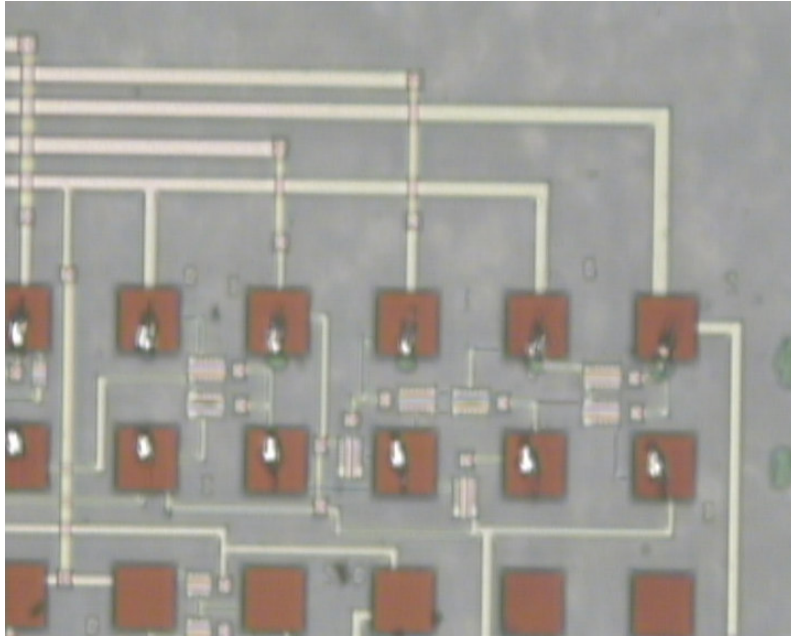


Fig 2-2.9 The picture of a PFD.

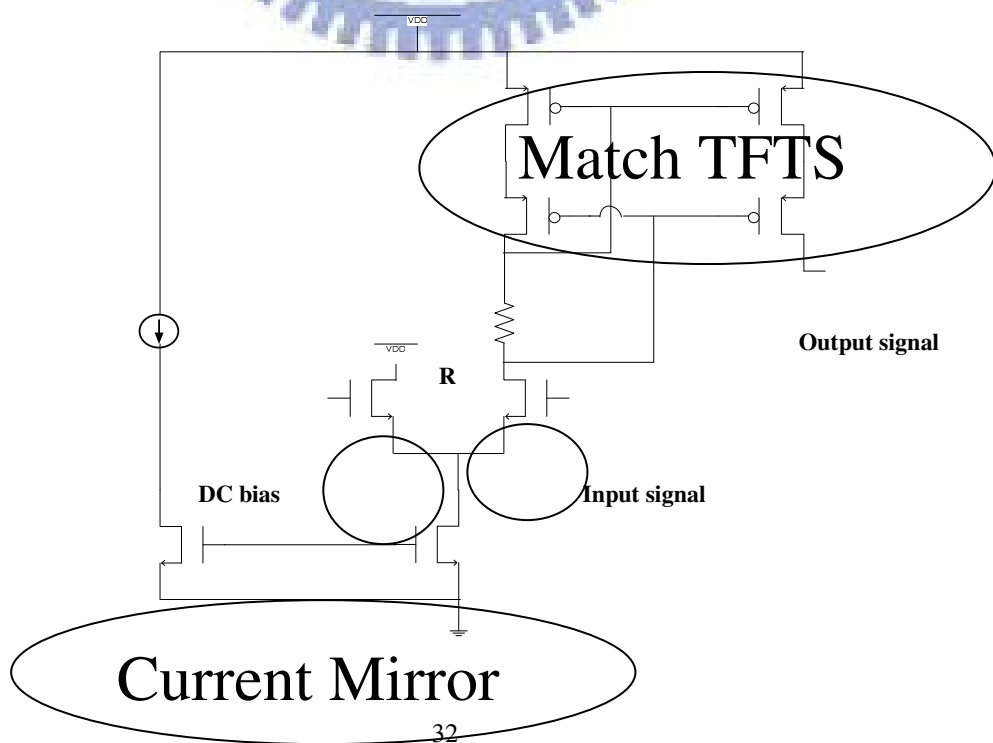




Fig 2-3.1 Level shifter circuit with an input end and a DC bias input ; DC bias input M2 TFT and Input signal input M1TFT.

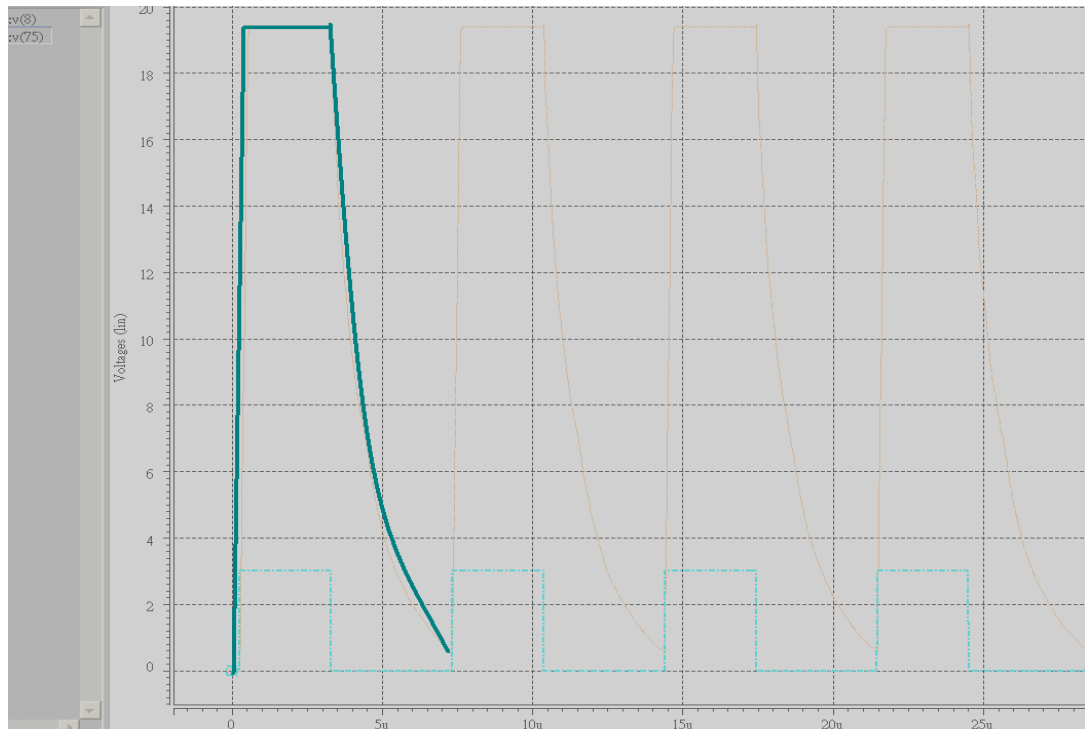


Fig 2-3.2 Level shifter circuit pumps input signal of 3 volts and sends out a 18 volts.

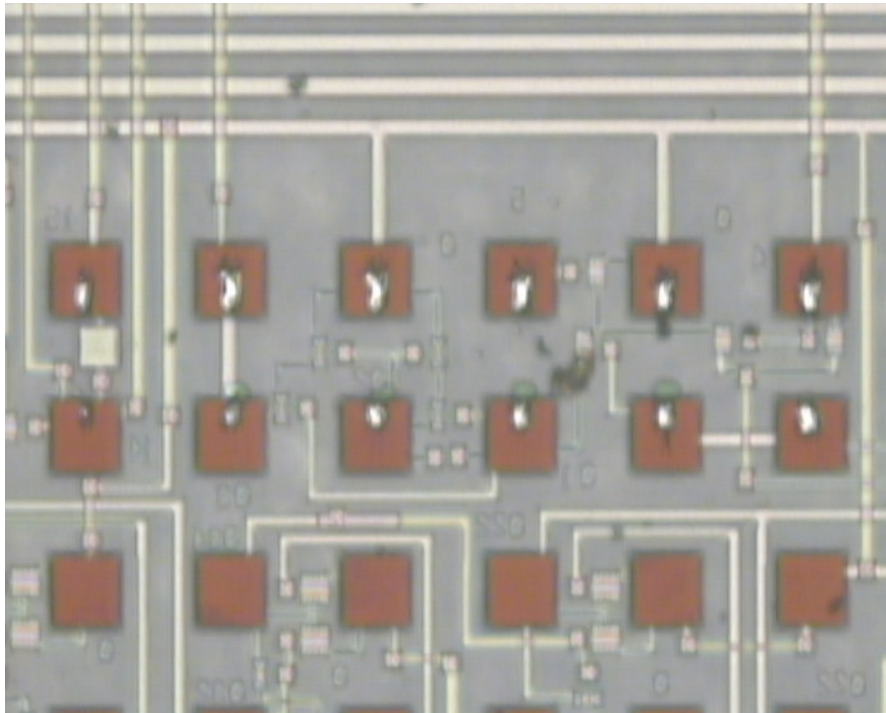


Fig 2-3.3 The layout picture of level shifter.

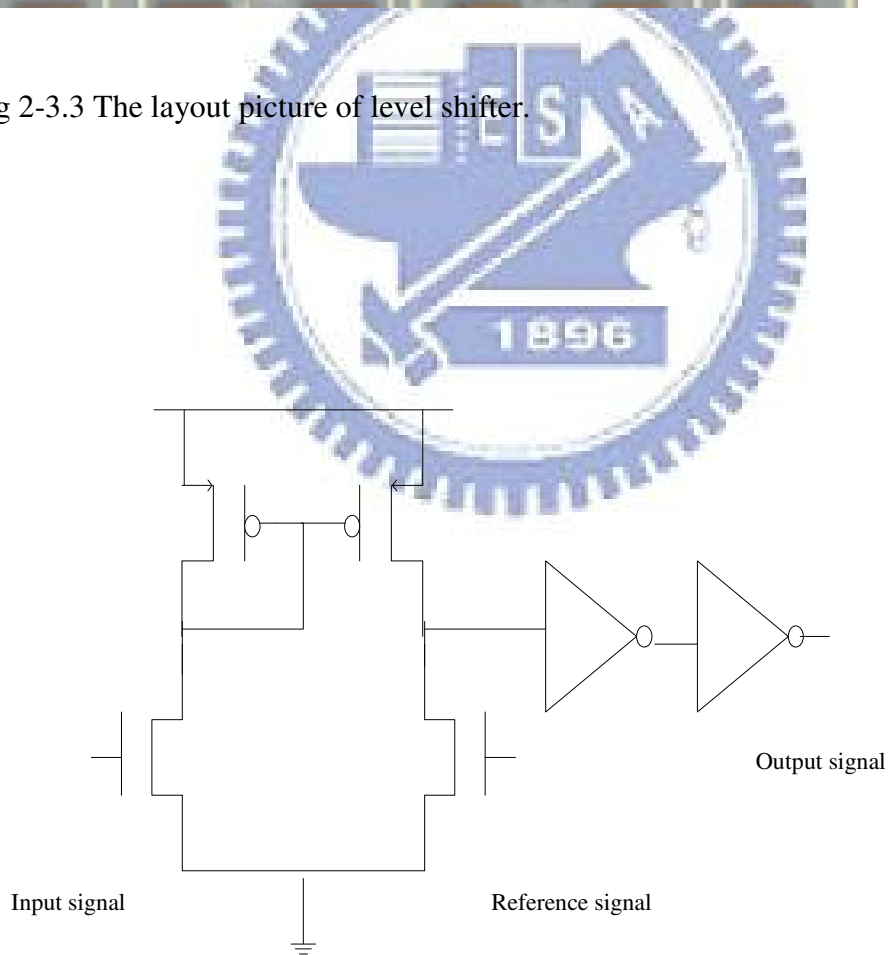


Fig 2-3.4 The schematic of a level shifter.

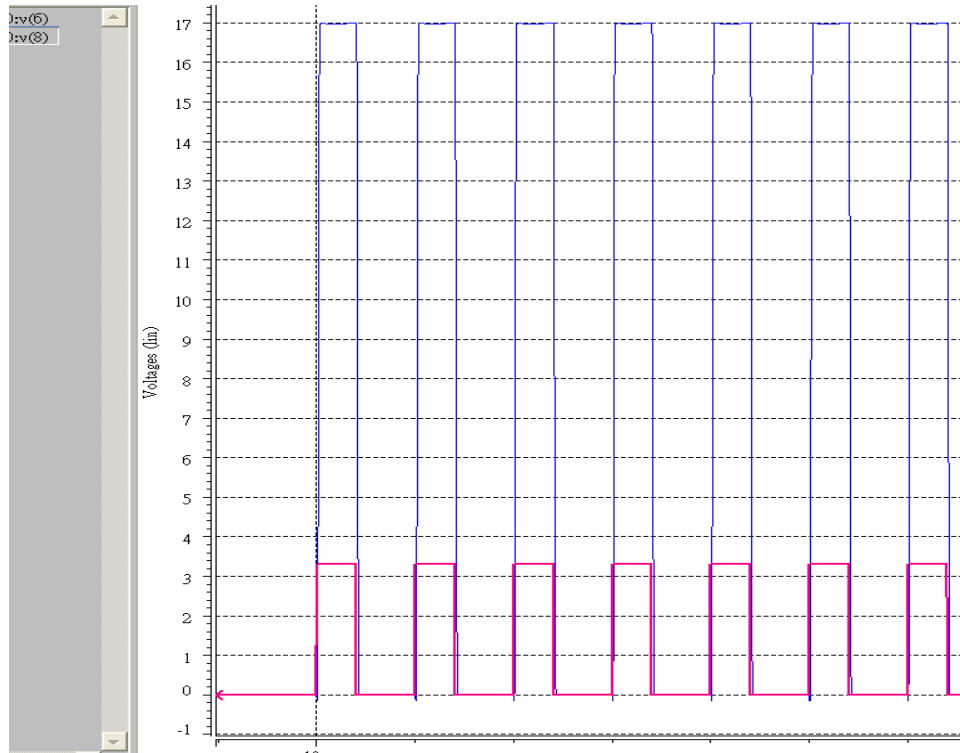
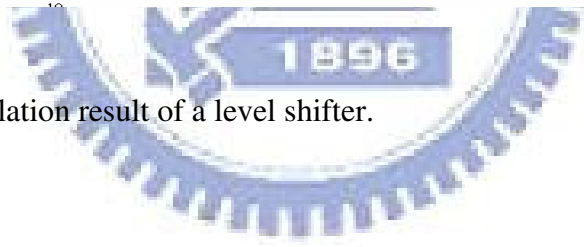


Fig 2-3.5 The simulation result of a level shifter.



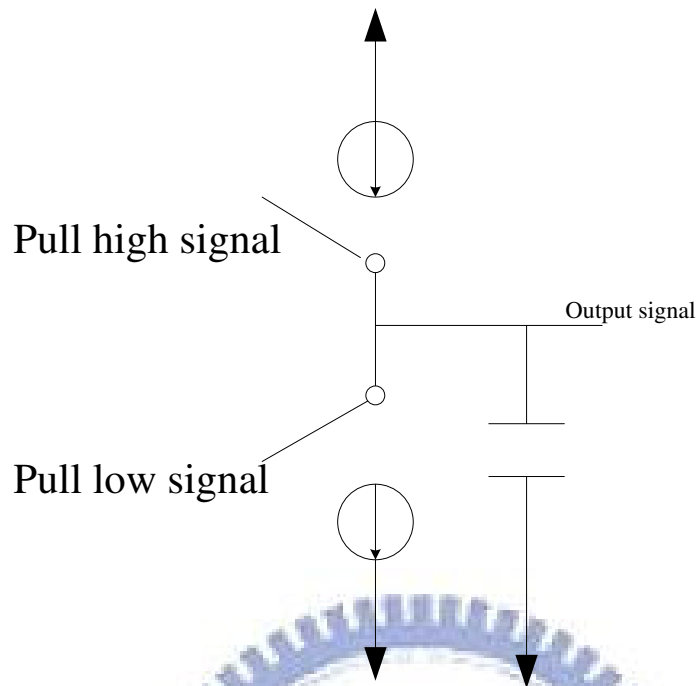


Fig 2-4.1 Schematic of charge pump.

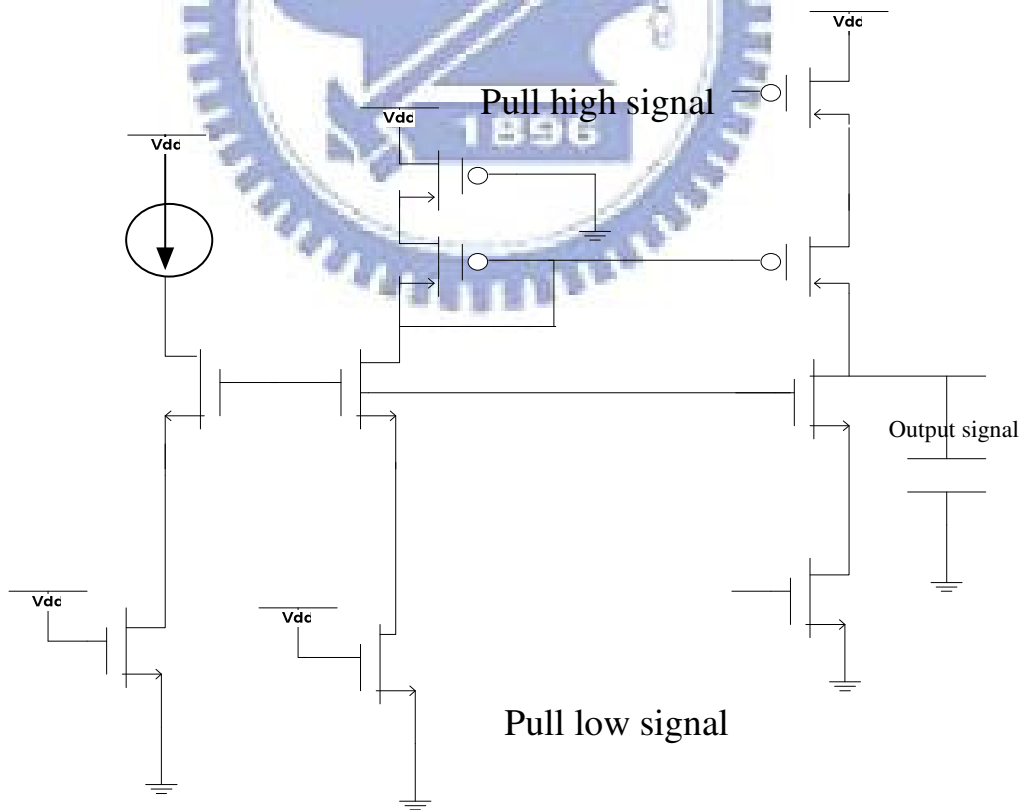


Fig 2-4.2 A charge pump circuit.

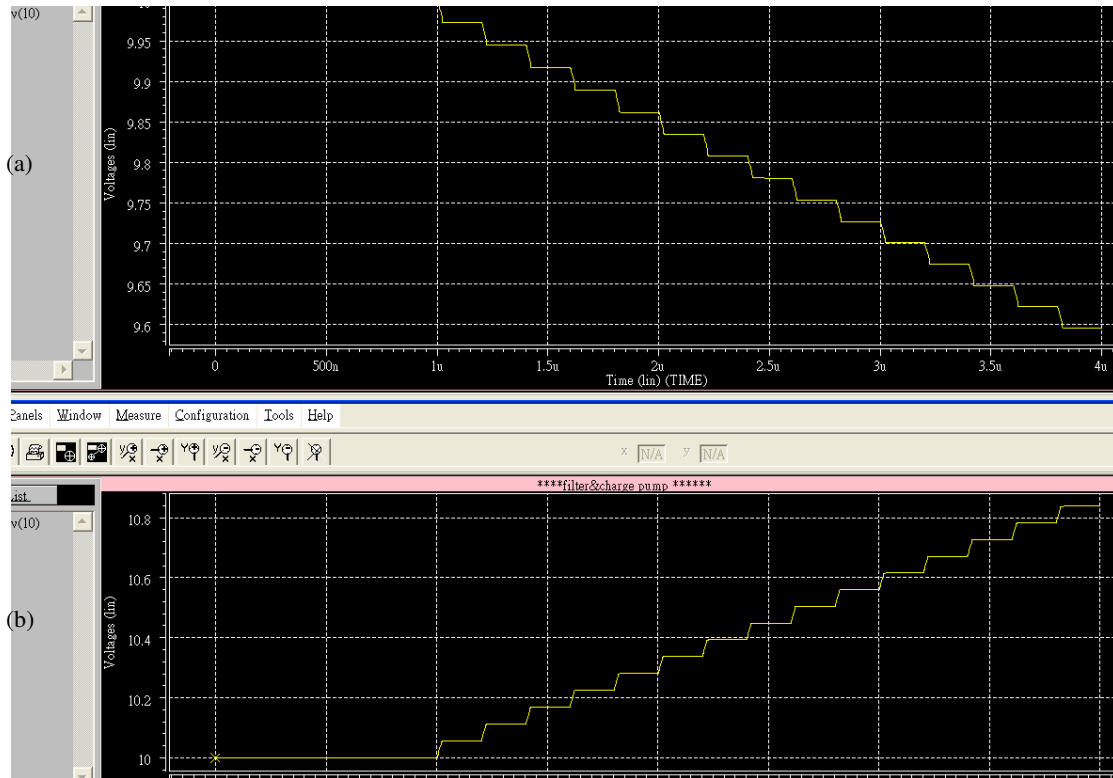


Fig 2-4.3 The output signal of receiving pull low signal and pull high signal separately..

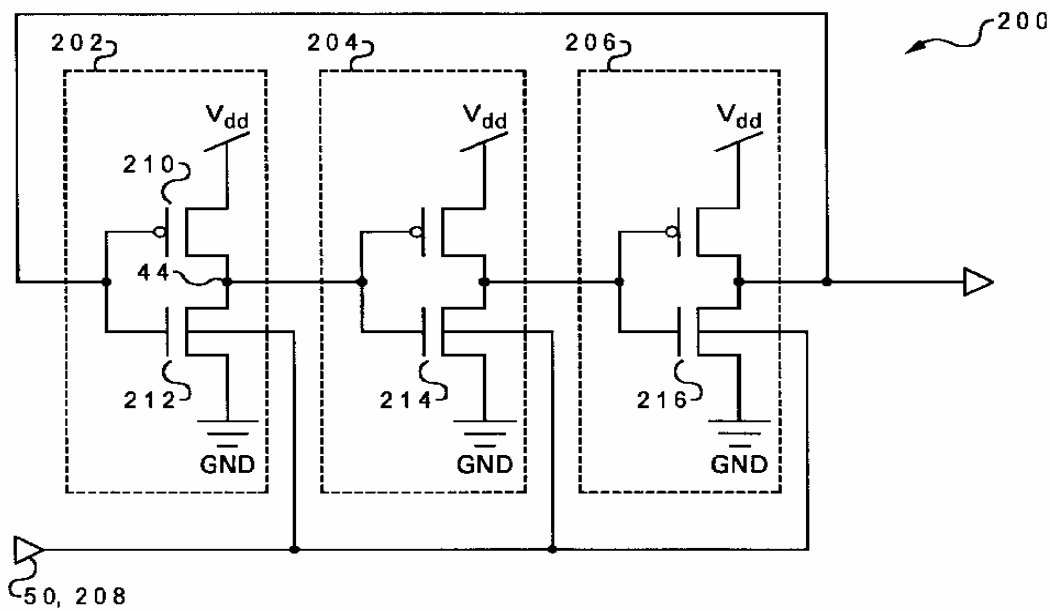


Fig 2-5.1 The schematic of a VCO circuit based on ring oscillator.

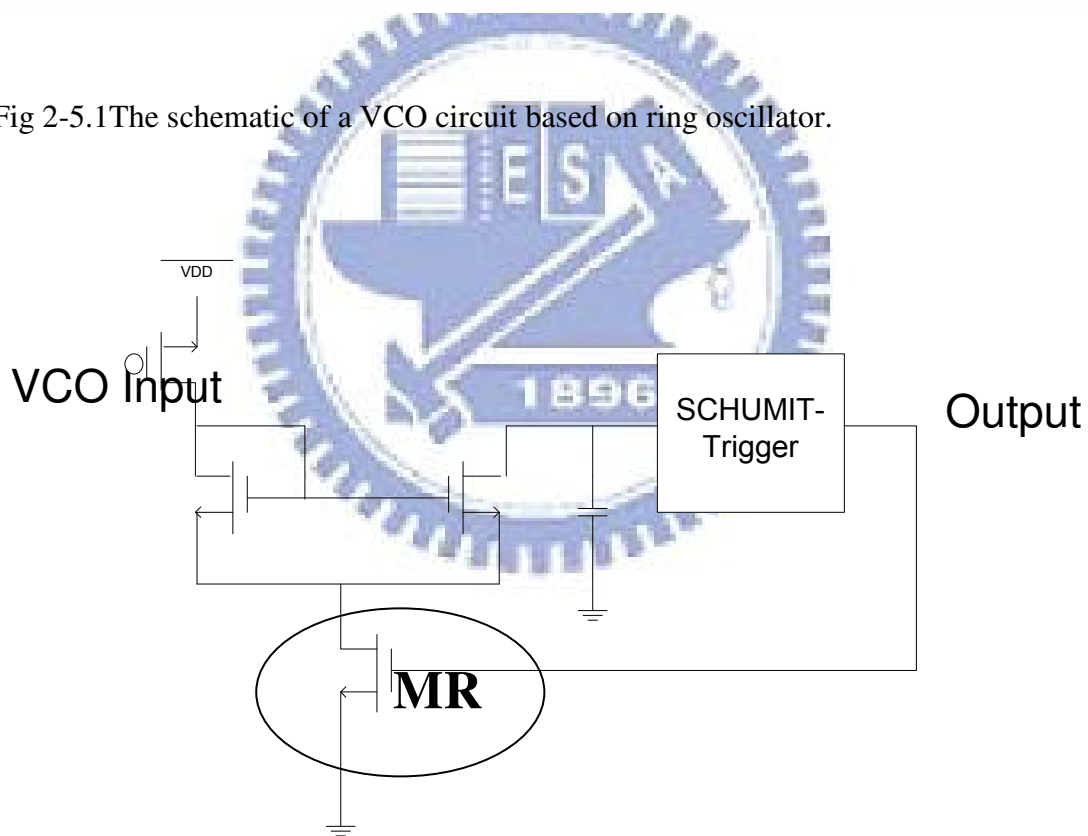


Fig 2-5.2 The circuit diagram of the VCO composing a Schmitt trigger and a feedback path.

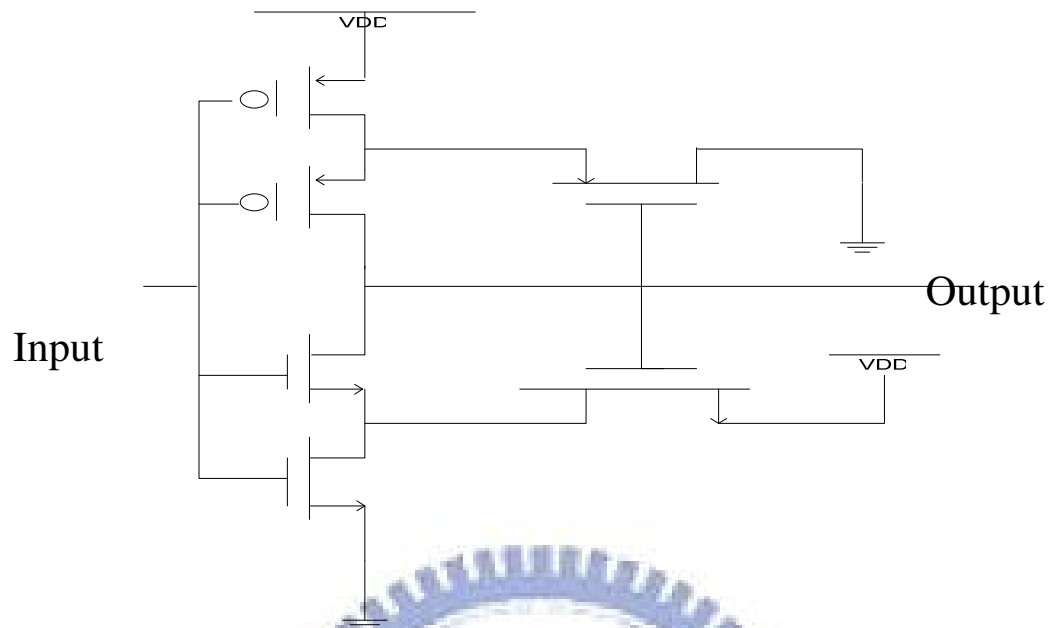


Fig 2-5.3(a) Circuit diagram of Schmitt-Trigger

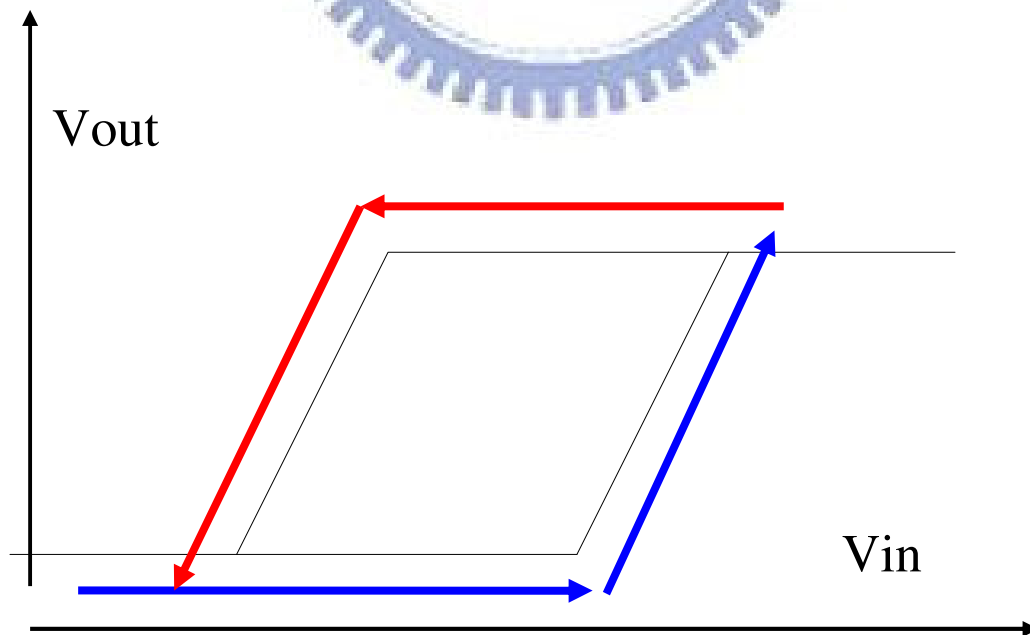


Fig 2-5.3(b) The relationship between input and output signals of a Schmitt-Trigger.

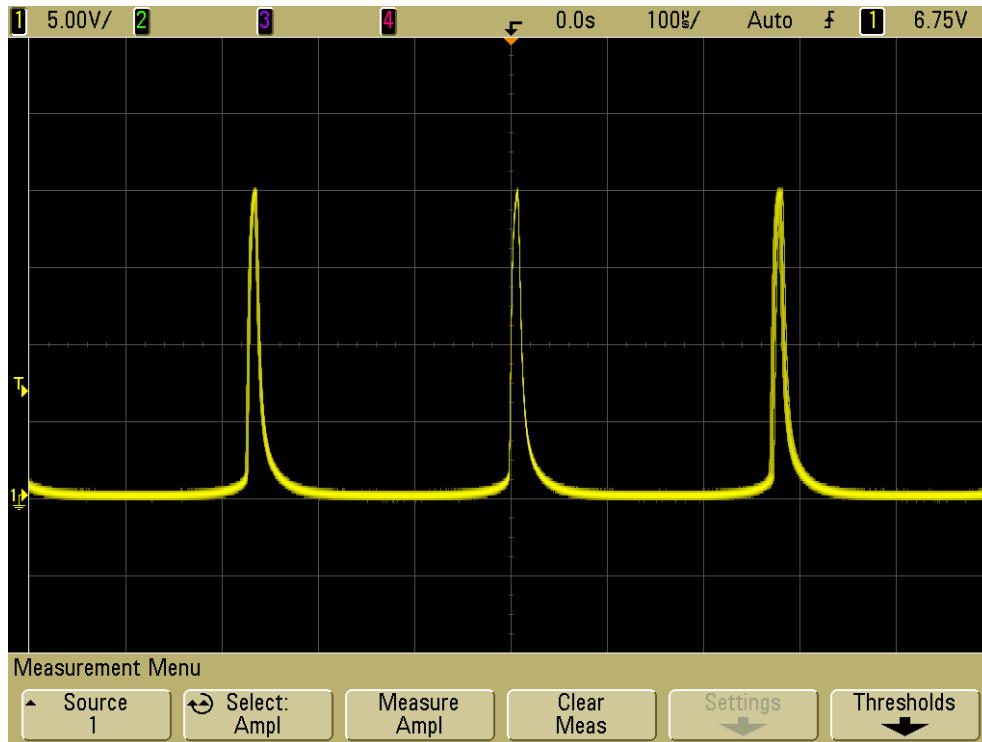


Fig 2-5.6(a)



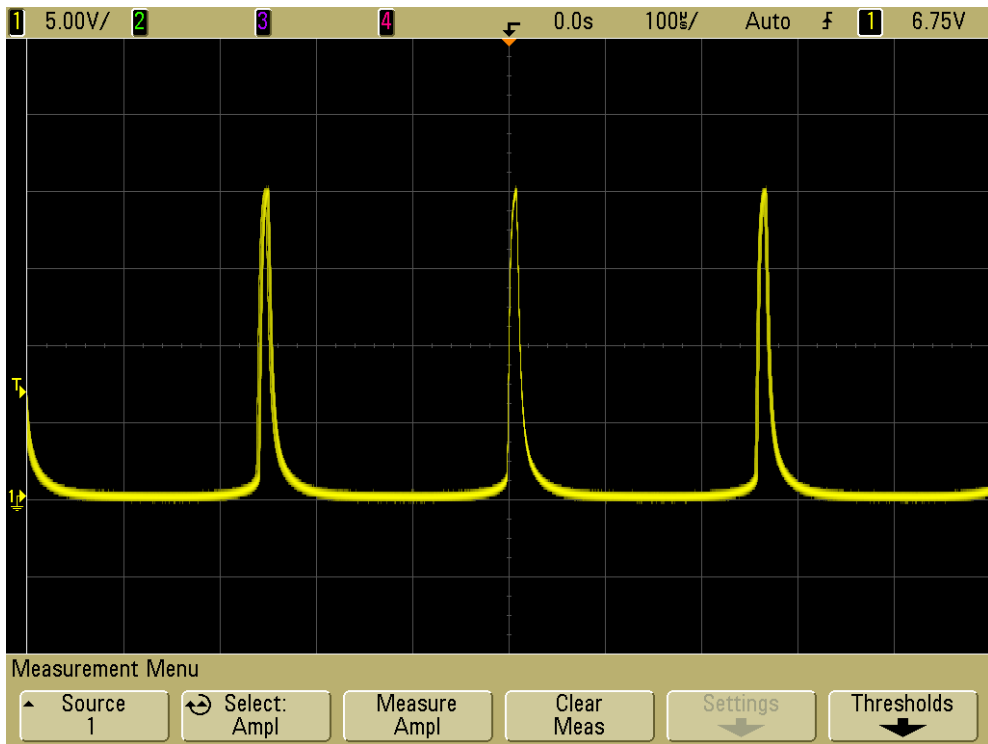


Fig 2-5.6(b)

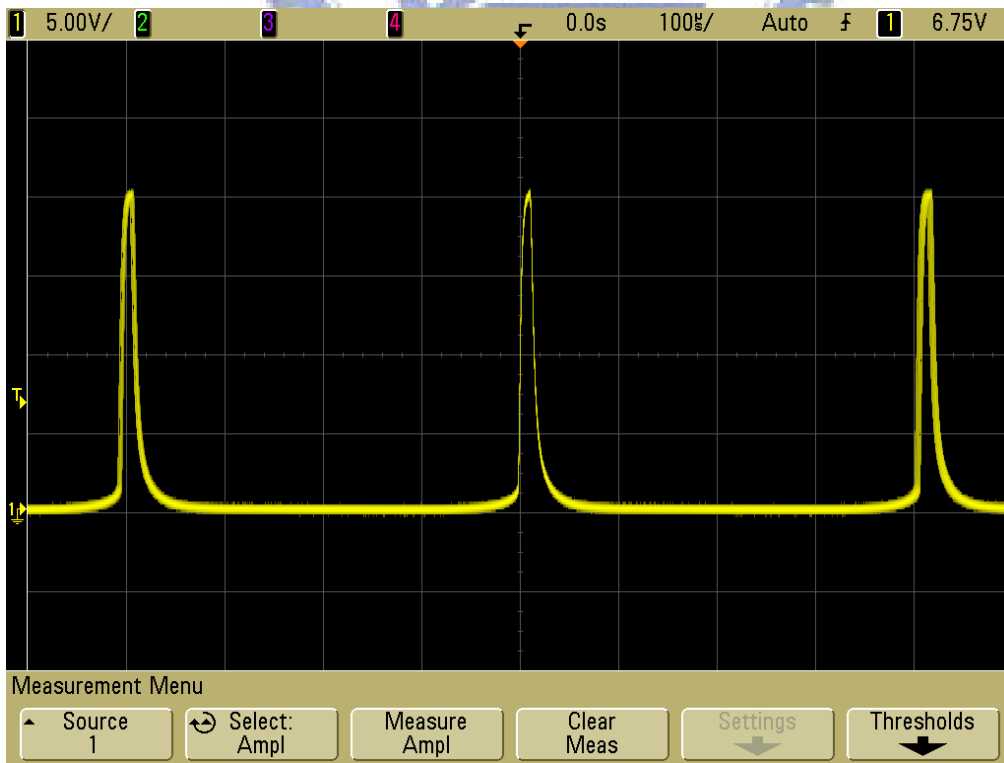


Fig 2-5.6(c)

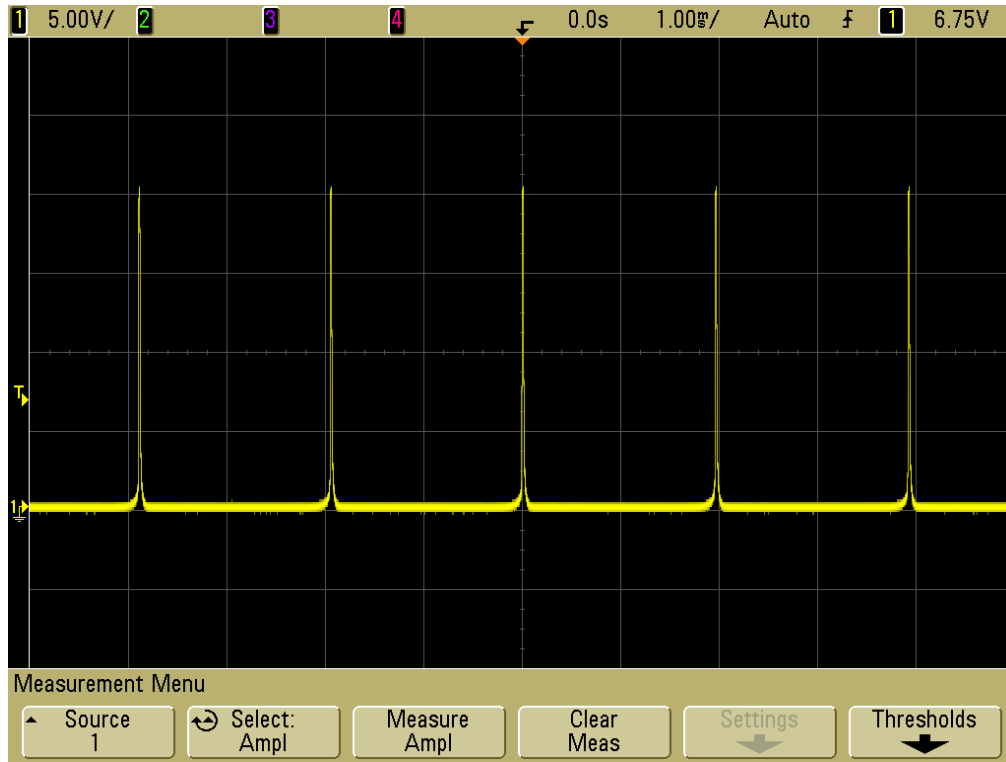


Fig 2-5.6(d)The wave form of the VCO output voltages with DC input of (a)5V (b)16V (c)18.3V and (d)19.1V

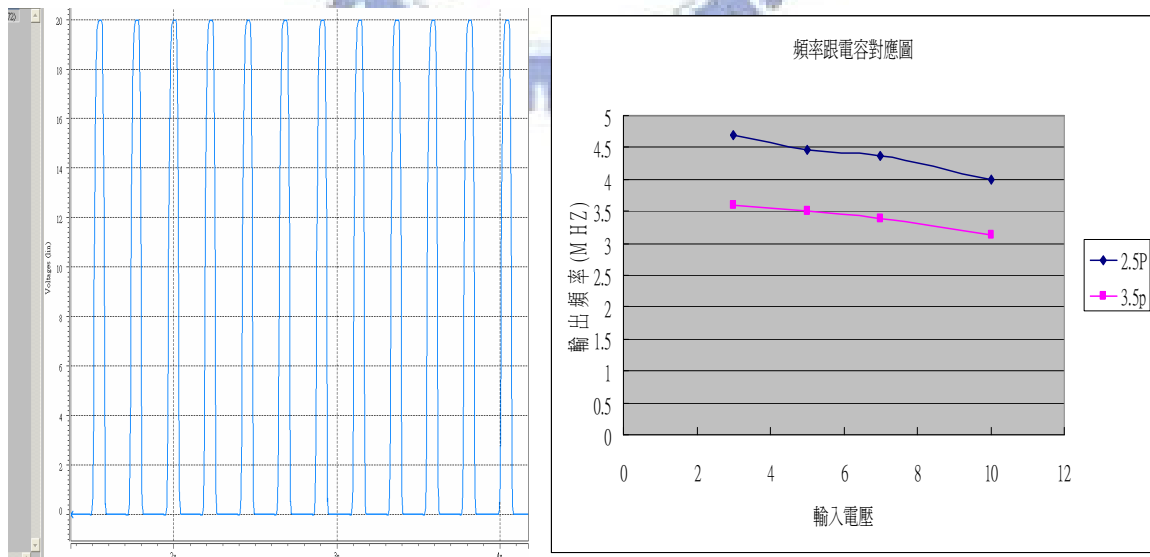


Fig 2-5.7 The relationship between the input signal and output frequency of VCO.

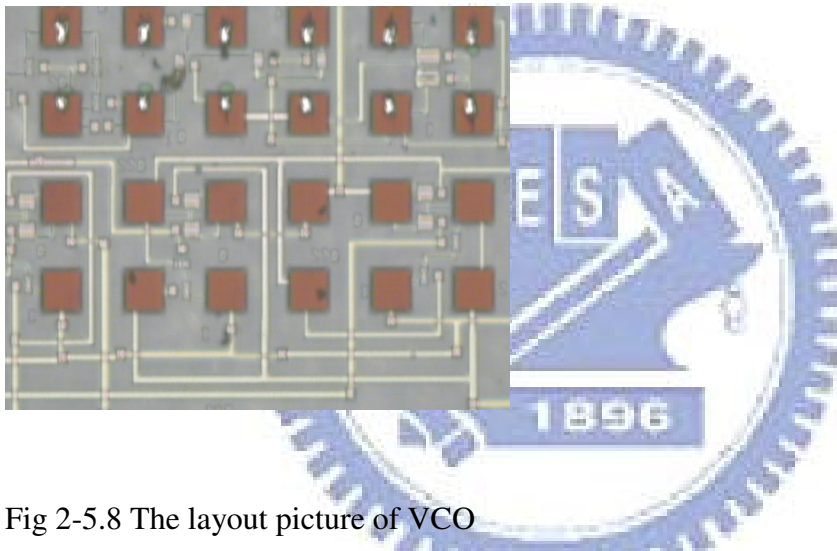
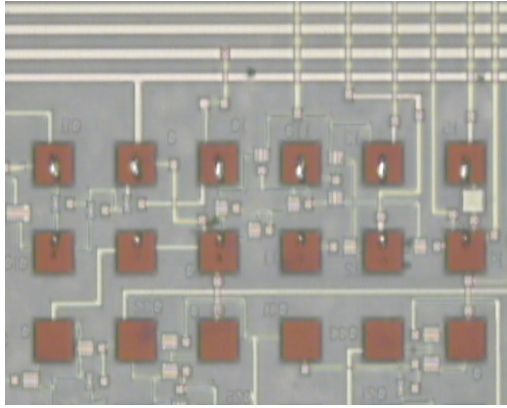


Fig 2-5.8 The layout picture of VCO

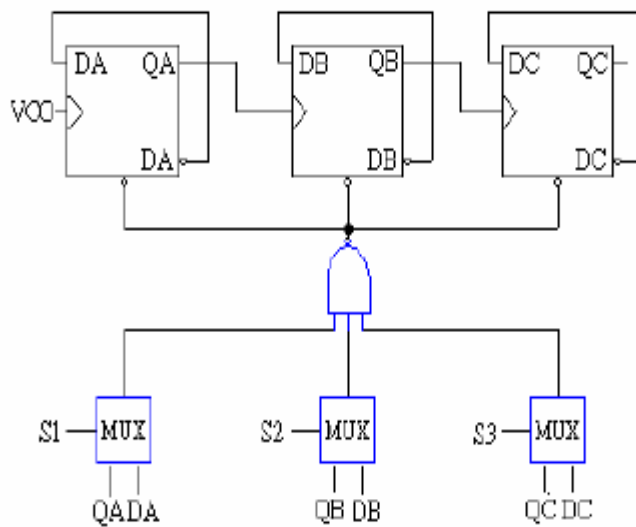
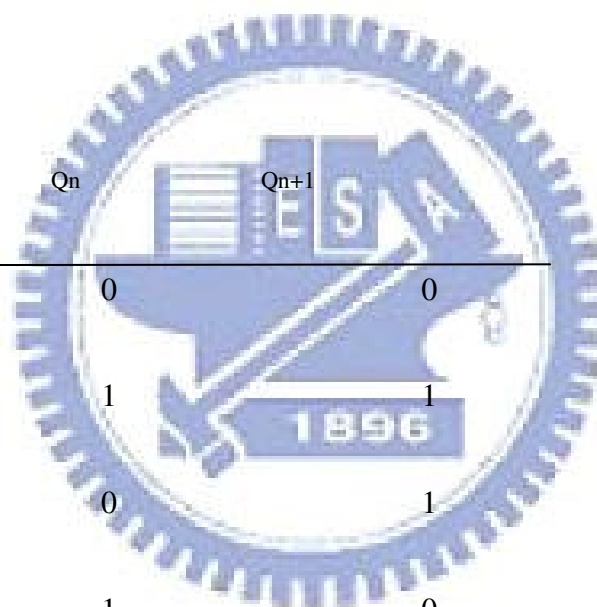




Fig 2-6.2(a) A logic diagram of a T-flip flop.



Input	$Q_n$	$Q_{n+1}$
0	0	0
0	1	1
1	0	1
1	1	0

Fig 2-6.2(b)  $Q_{n+1}$  is the (n+1)th output, and differs from  $Q_n$  only when Input is at its high level.

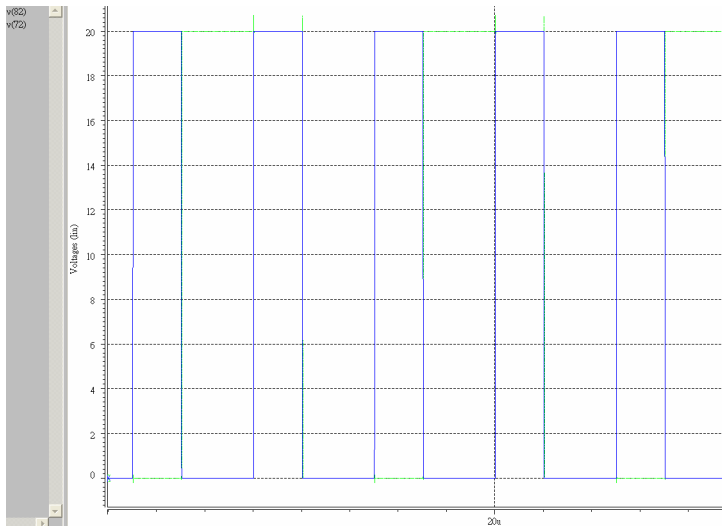


Fig 2-6.3 Simulation result of input signal and an output signal with half frequency.

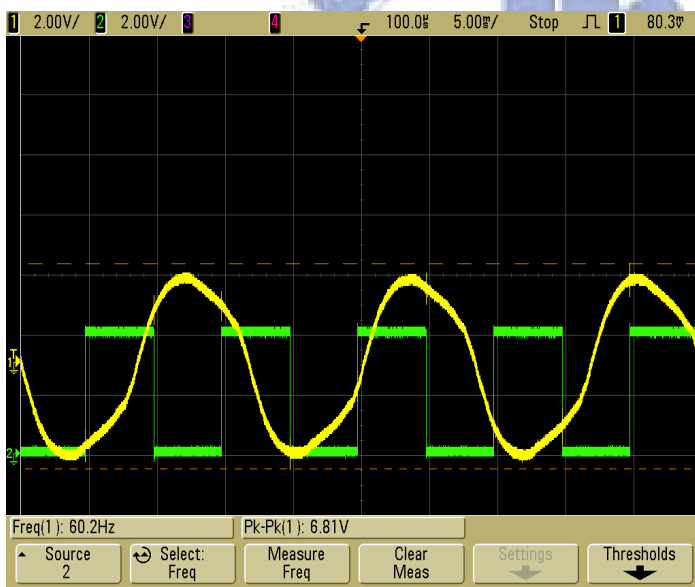


Fig 2-6.4 Output signal and input signal of divider.

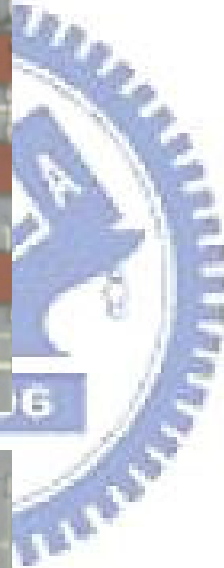
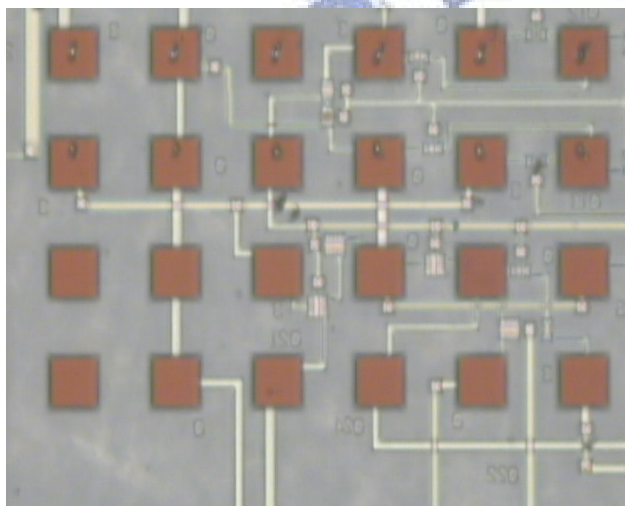
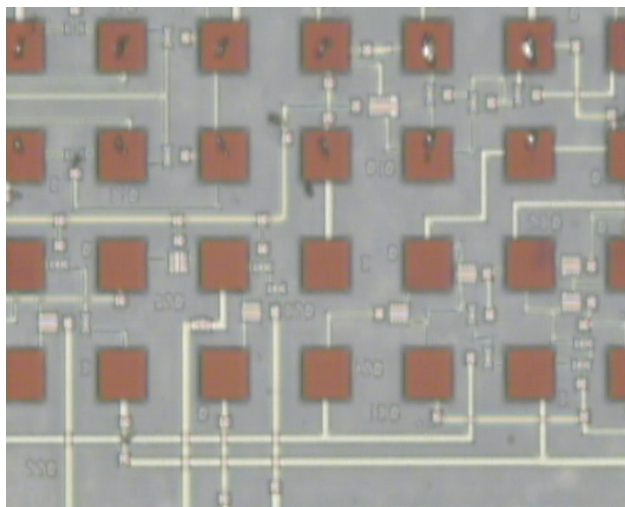
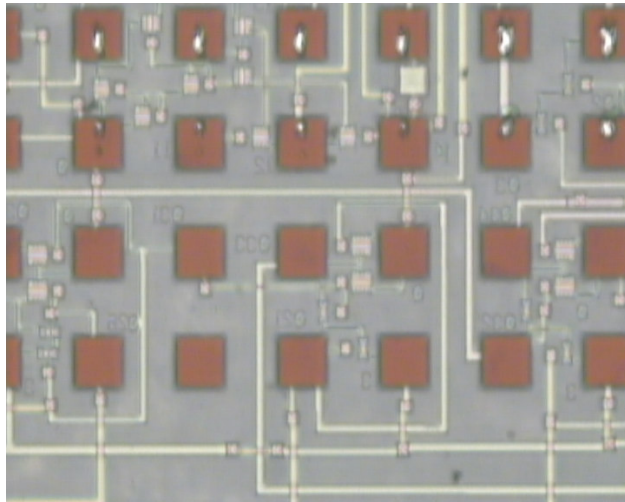


Fig 2-6.5 The layout picture of T-flip flop.

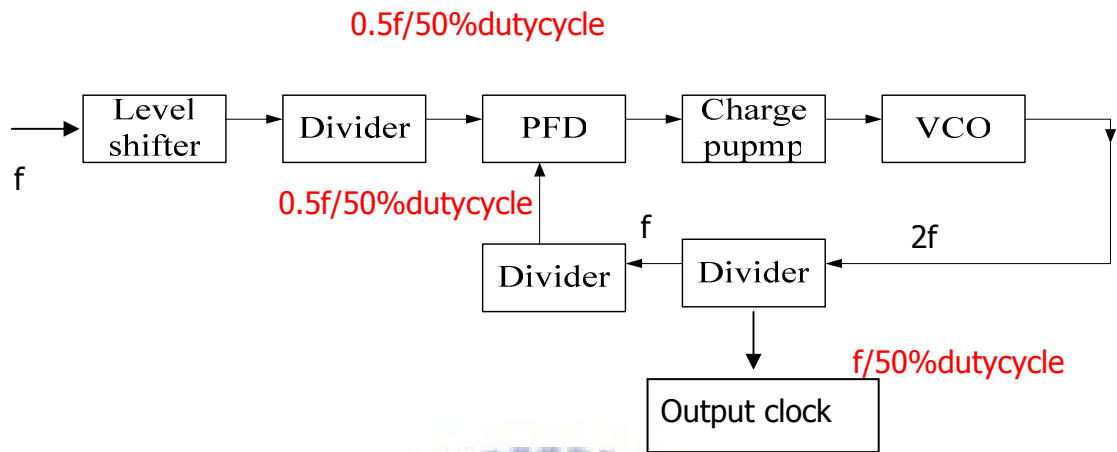


Fig 2-7.1 Proposed PLL function blocks.

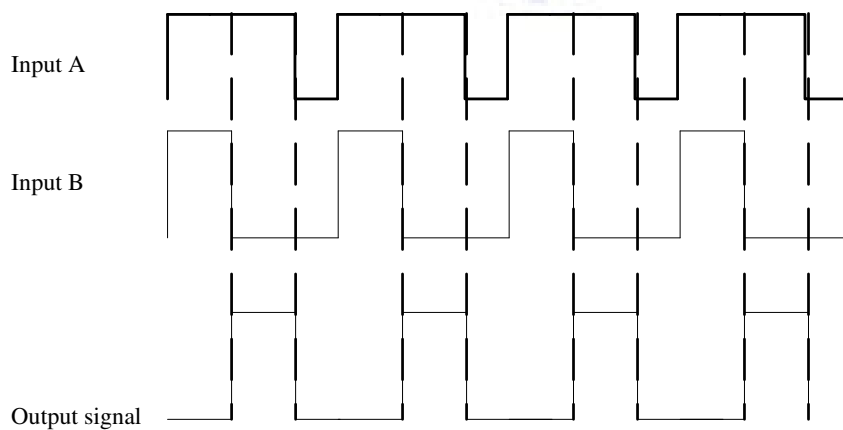
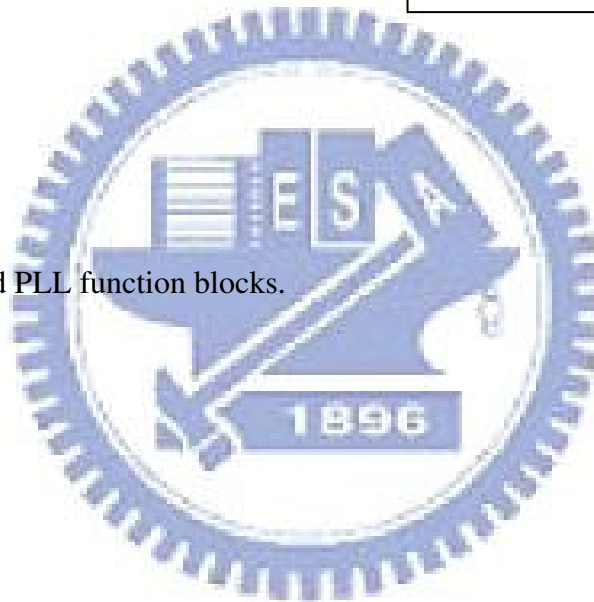


Fig 2-7.2 Proposed PLL function blocks.



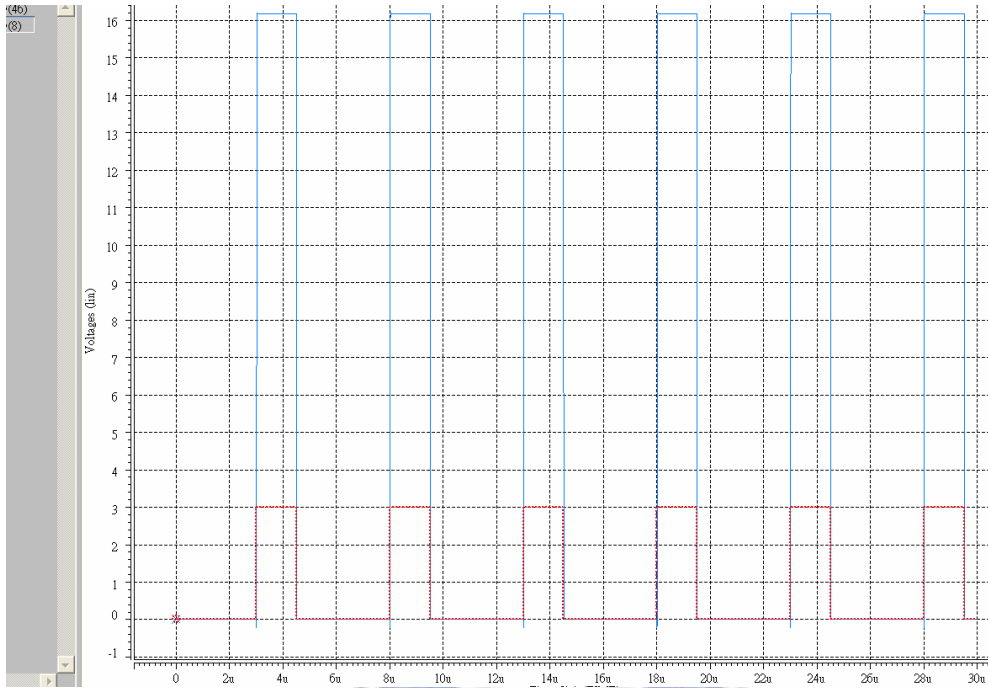


Fig3-1.1 Statistic state of a level shifter input (3V) and output (16V) signals.

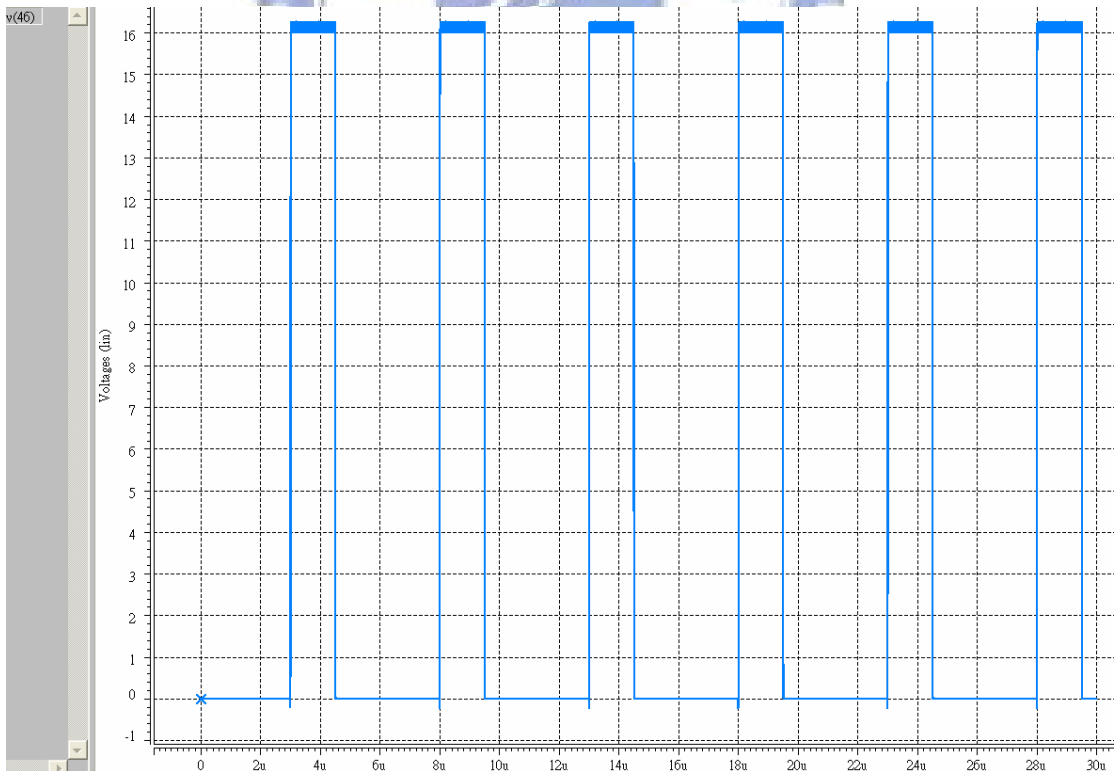
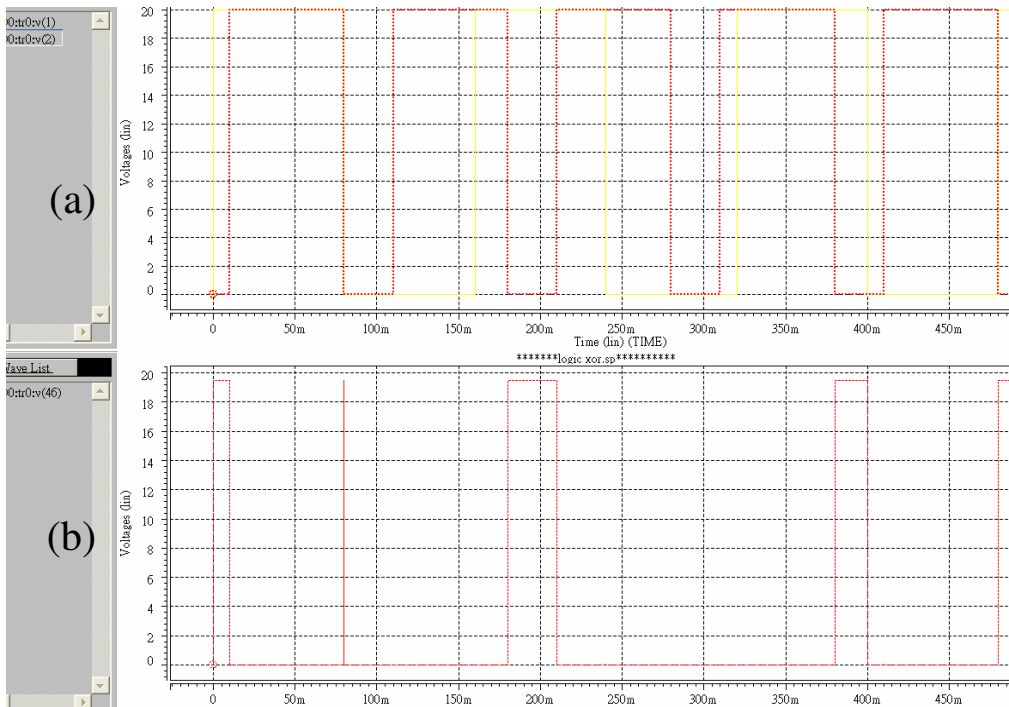
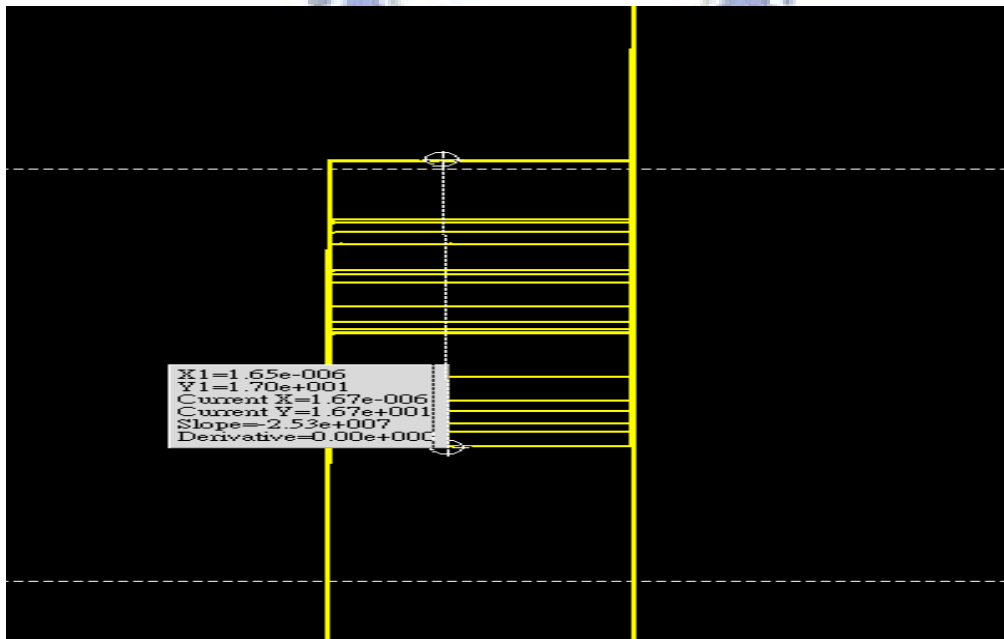


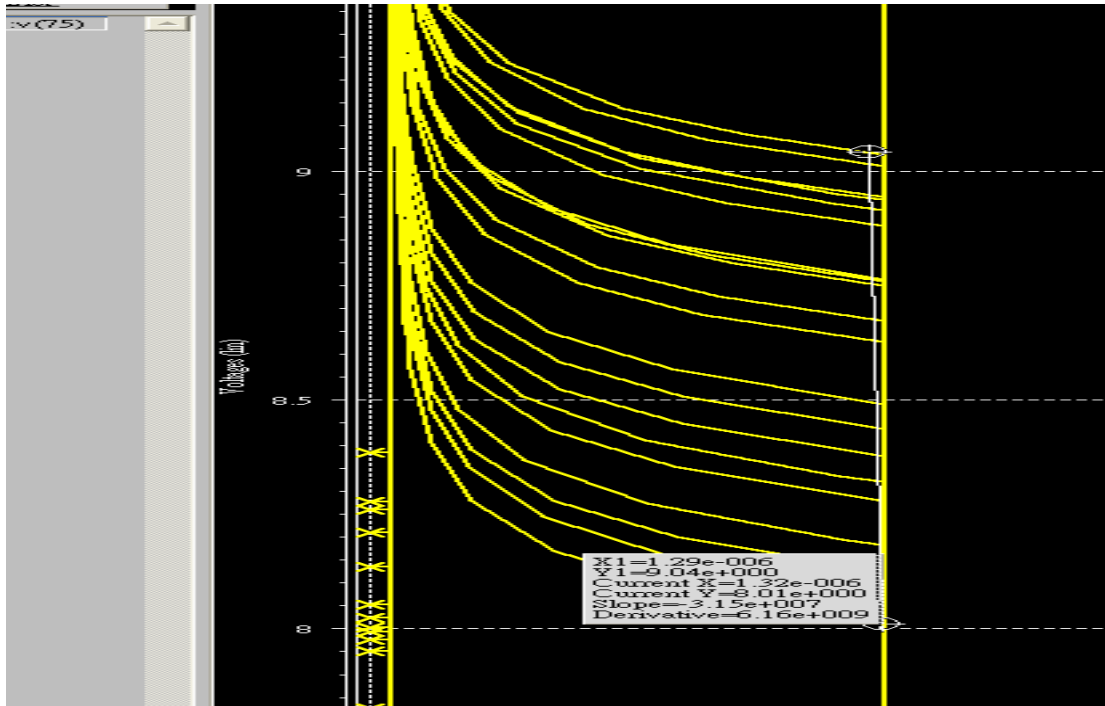
Fig3-1.2 40 times of variation test on level shifter output signal.



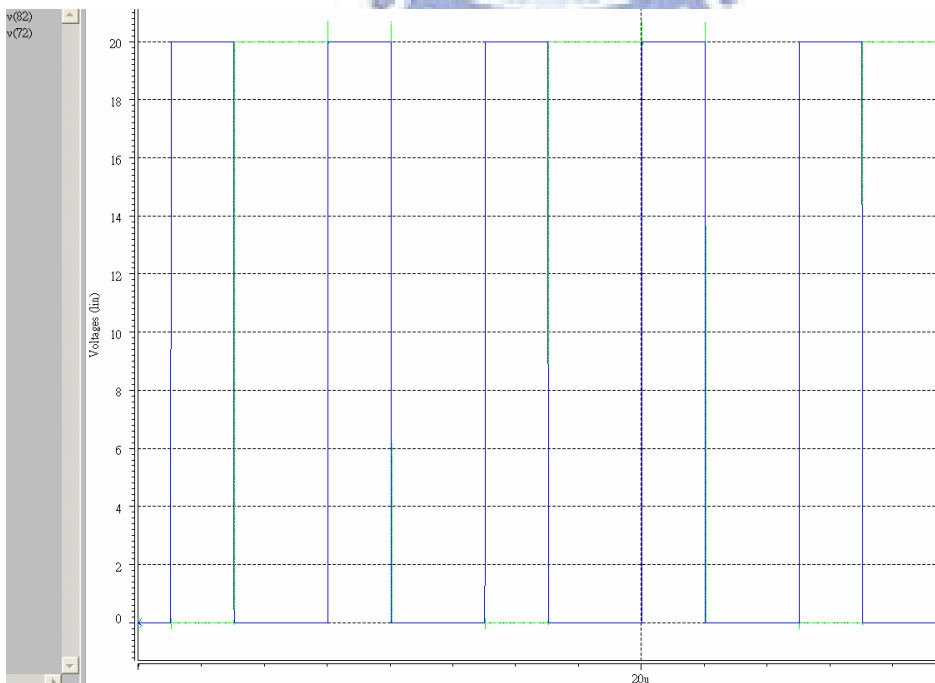
3-2.1 (a) Input signal ,and (b) output signal of PFD.



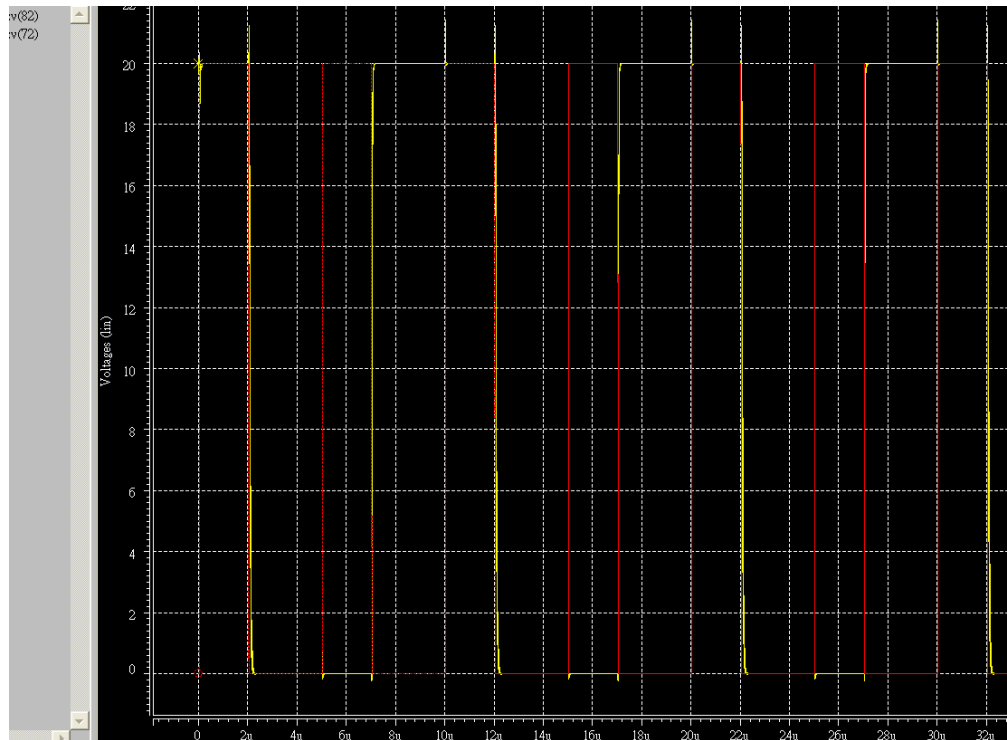
### 3-2.2 Logic high of PFD output signal.



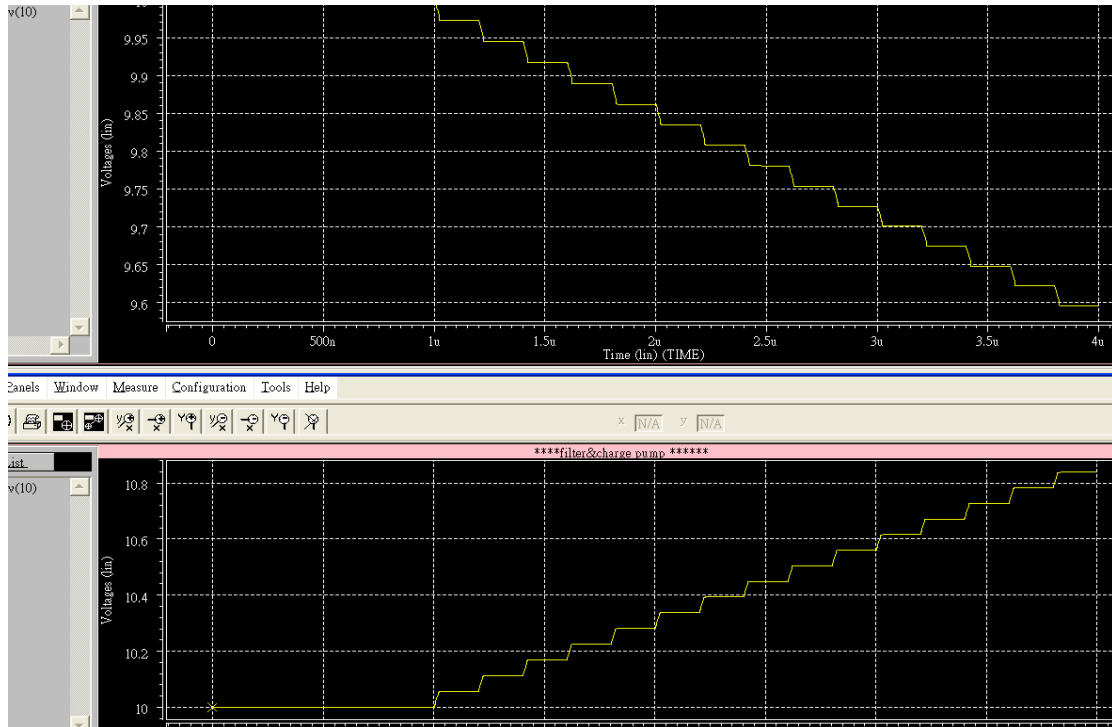
### 3-2.3 Logic low of PFD output signal.



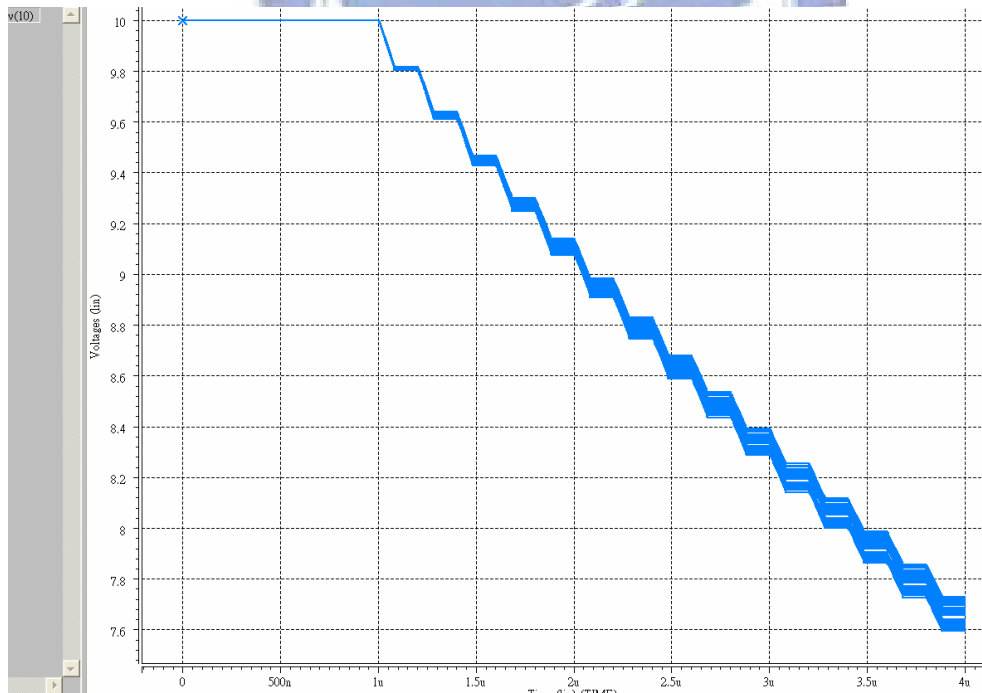
### 3-3.1 Divider input and output simulation result.



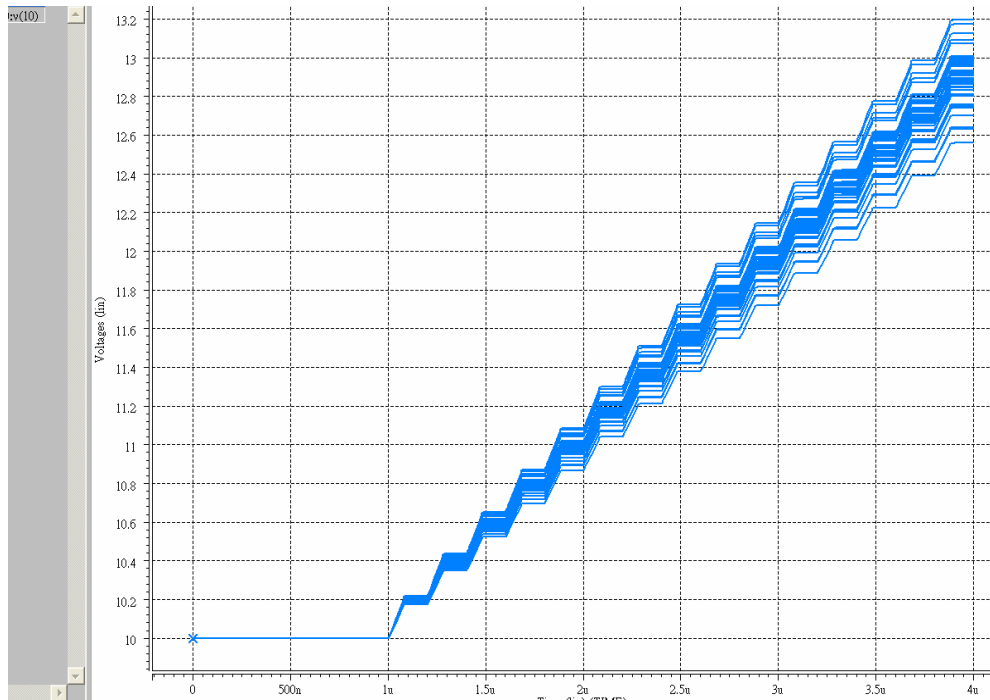
### 3-3.2 Simulation result of 40 times of Gaussian test



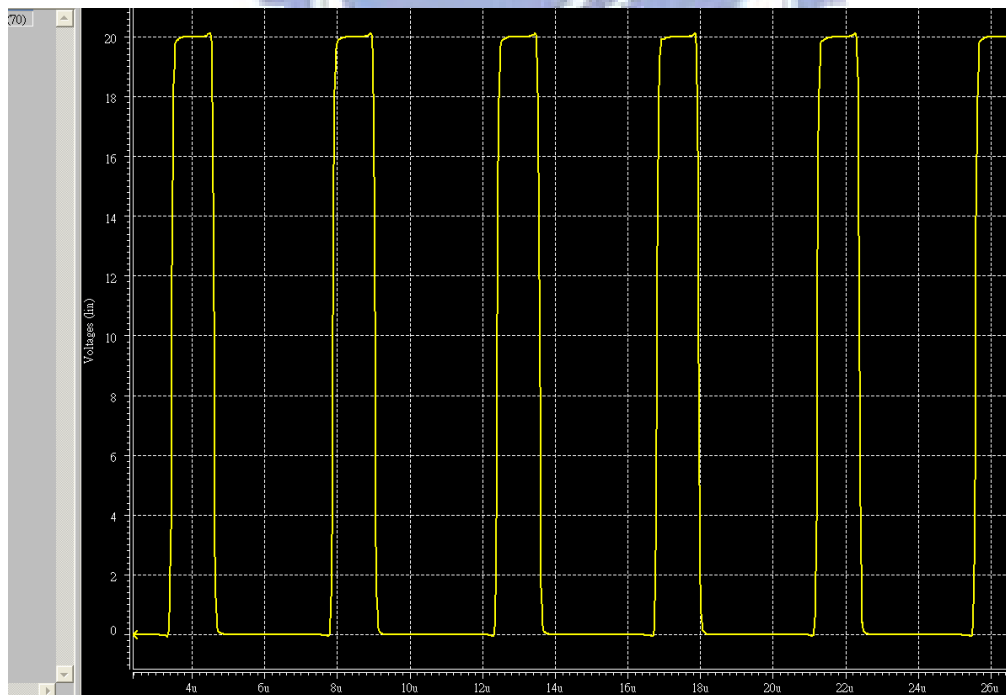
### 3-4.1 Simulation of charge pump under statistic situation.



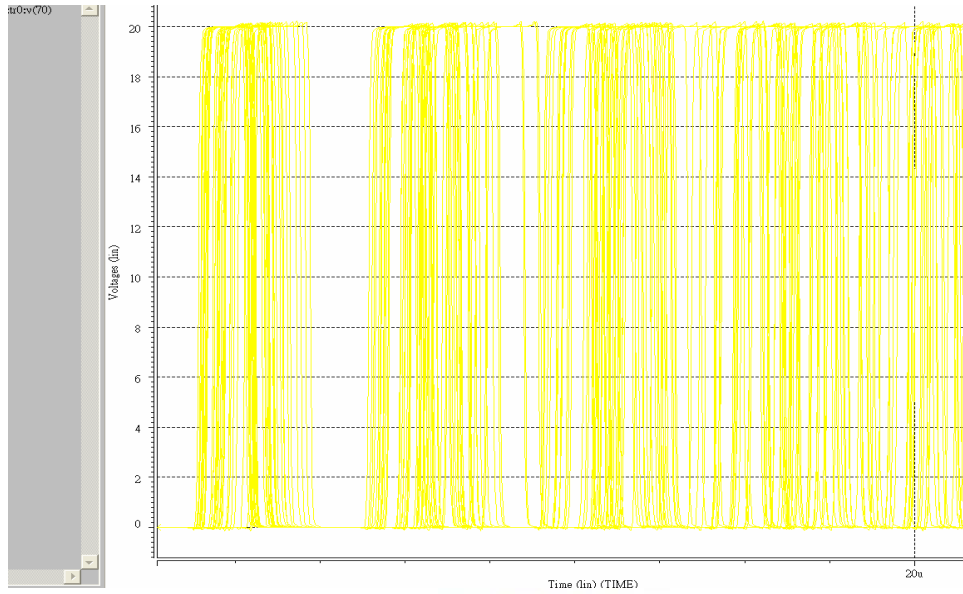
### 3-4.2 Simulation of pulling low under device variation situation



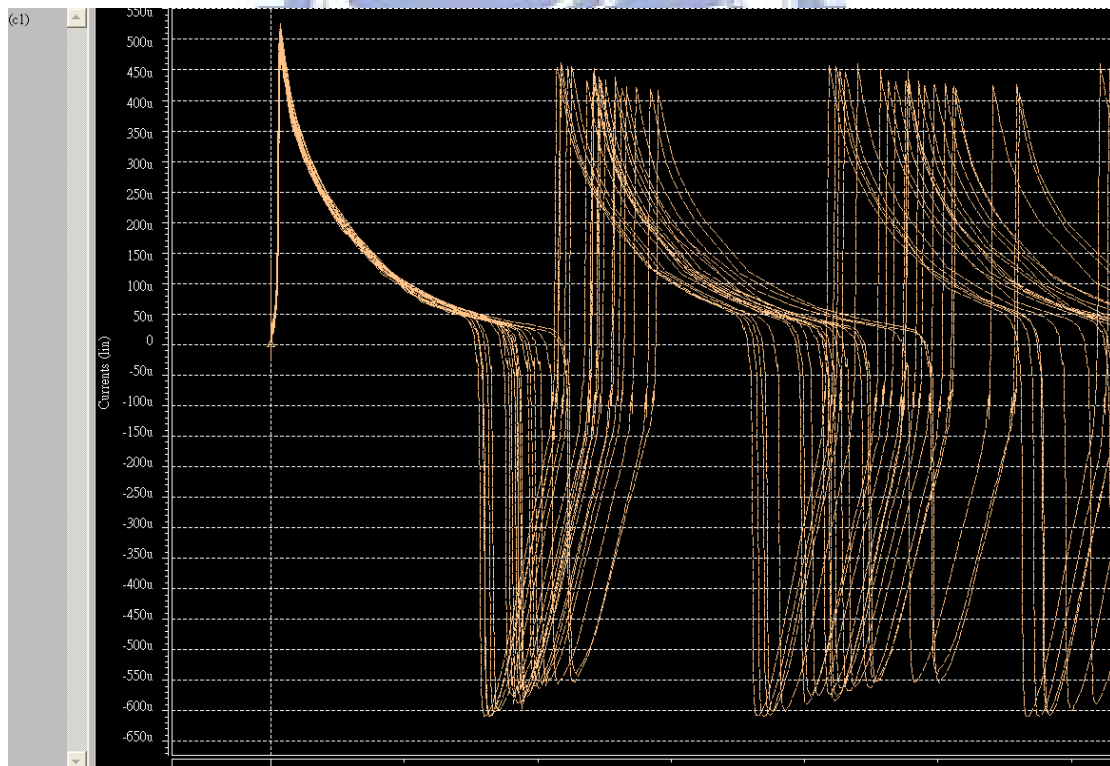
### 3-4.3 Simulation of pulling high under device variation situation



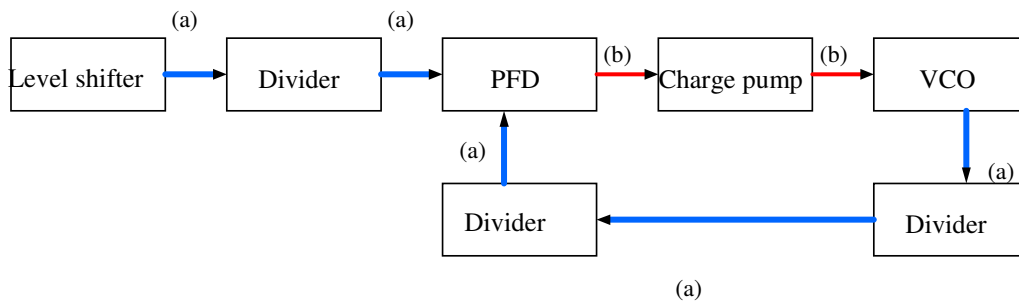
### 3-5.1 Simulation of VCO under variation situation



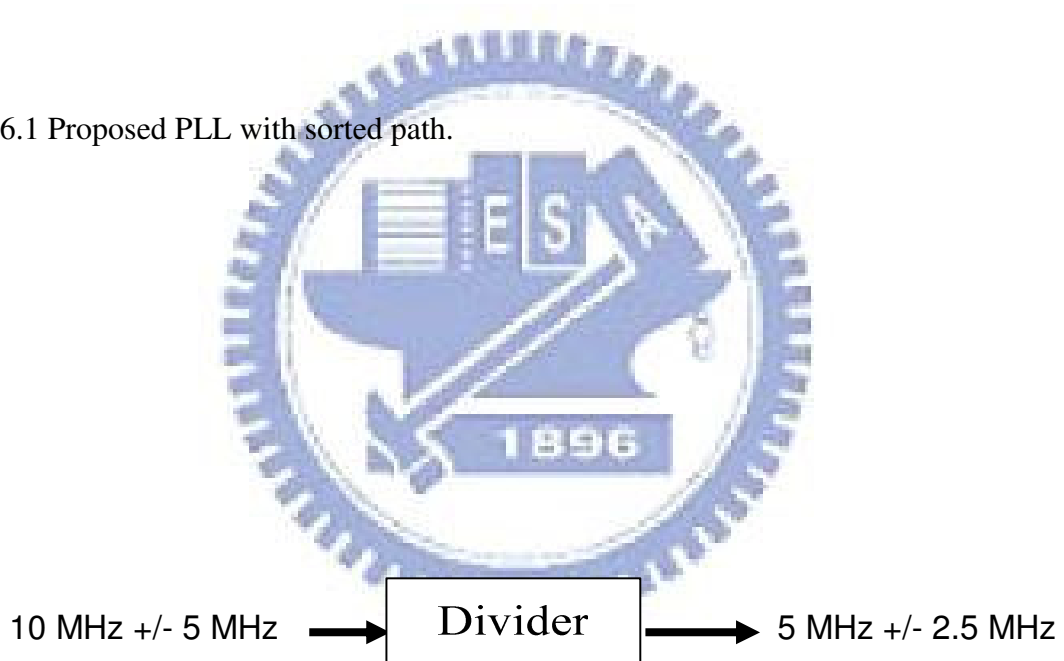
3-5.2 40 times simulation of VCO under variation result.



3-5.3 Simulation of VCO by examining the parameter of current in capacitor under device variation situation

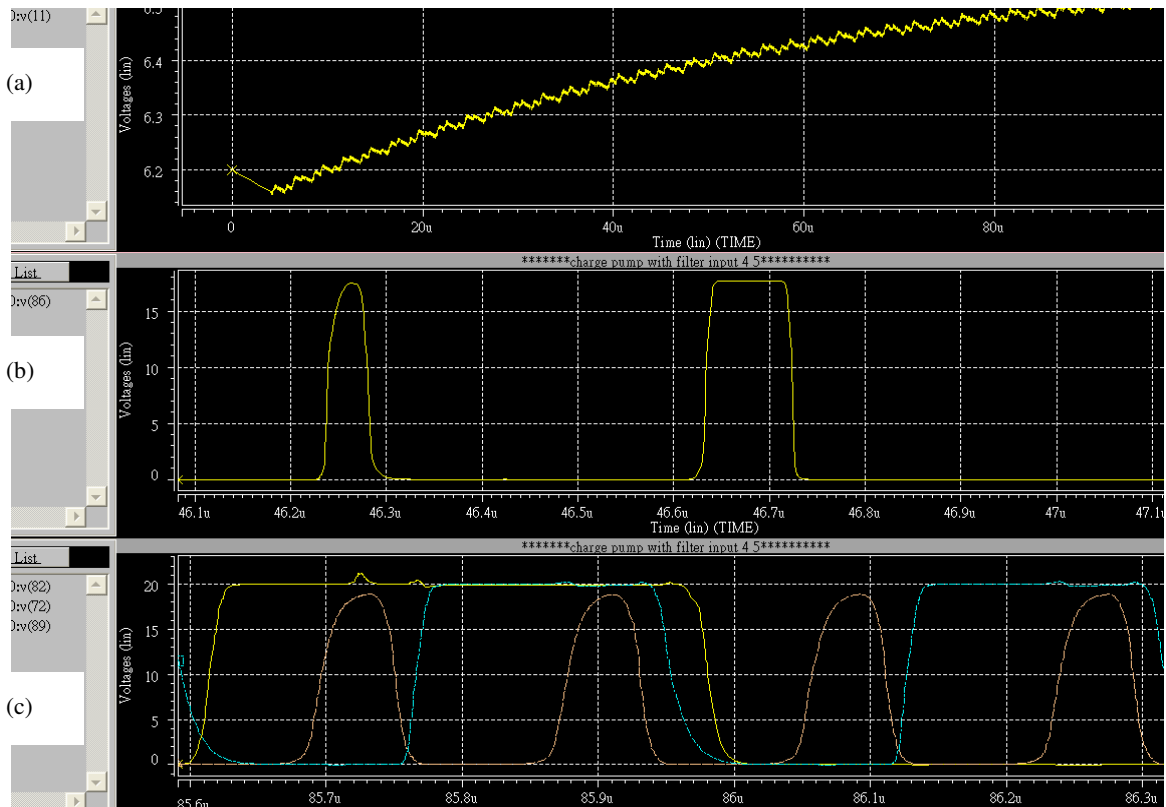


3-6.1 Proposed PLL with sorted path.



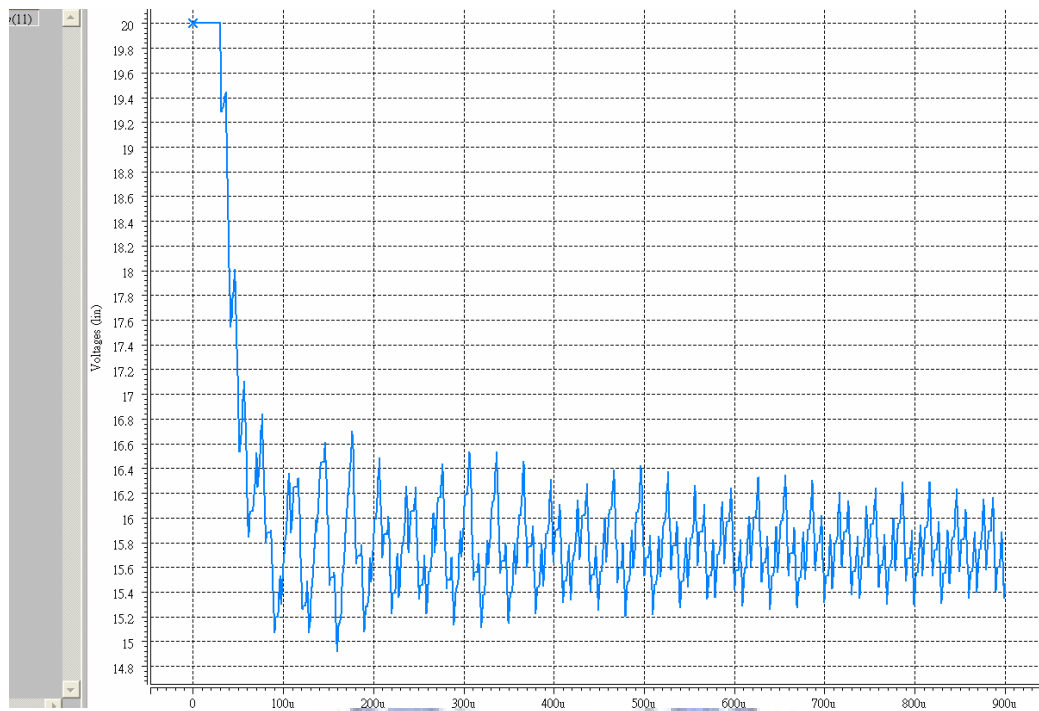
3-6.2 Divider divides input signal into half.



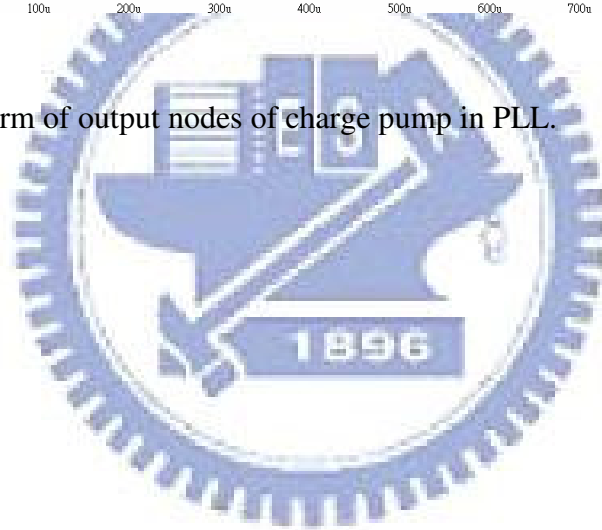


4-1.1 Wave forms of nodes in PLL.





4-1.2 The wave form of output nodes of charge pump in PLL.



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