國立交通大學

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碩士論文

全閘極複晶矽薄膜電晶體暨電路數值模擬之研究

Numerical Simulation of Gate-All-Around Polysilicon Thin-Film Transistors and Circuits

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中華民國 九十六 年 六 月

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摘　　要

本論文主要探討全閘極複晶矽薄膜電晶體暨電路數值之模擬。首先吾人運用數值方法離散載子流連續程式及泊松方程式，這些方法包含有 Gummel’s 疊代法，有限體積近似法，以及牛頓法來解一組半導體偏微分方程式。在薄膜電晶體模式中應該考慮適當的晶粒邊界效應，一般而言晶粒邊界的位障模式和電位能是複雜的非線性函數關係，當代入半導體偏微分方程式時，會造成離散複雜化，使得網格加切數量增加以及計算時間增長。經由與實驗數據之校估，萃取出晶粒邊界之缺陷濃度以及缺陷能障。

藉由萃取出的晶粒邊界參數，分析縮小通道尺寸的問題。當通道尺寸在三百奈米時，也就是約等於一個晶粒大小時，元件會面臨到有、無晶粒邊界的問題，吾人探討單晶粒邊界發生在通道不同位置所造成元件特性漂移的情形。相較於晶粒邊界發生在通道中間或者沒有晶粒邊界的情形，汲極端若有晶粒邊界會產生顯著的臨界電壓變化。晶粒邊界變小，臨界電壓變化會逐漸降低。研究結果的比較顯示，深次微米全閘結構複晶矽薄膜電晶體，比傳統單閘結構複晶矽薄膜電晶體特性來的穩定性好兩倍以上。全閘結構複晶矽薄膜電晶體更有以下優點: (1) 電子遷移率上升，(2) 因有較好的閘極控制通道能力，故有較低的汲極電壓致使能障降低效應 (DIBL)、較低的次臨界震盪 (S.S)，並且藉由輕汲極摻雜(LDD)，提高開/關電流比，加快元件切換速度。(3) 較小的臨界電壓變化，提升主動式矩陣電路驅動電流的穩定性。

研究上更探討量子修正模式之九十奈米全閘結構複晶矽薄膜電晶體，晶粒邊界大小及發生位置對臨界電壓變化的影響，也一併分析。若晶粒邊界的大小可以控制2奈米以下，臨界電壓的變化和晶粒邊界發生的位置就無關。

因為全閘極複晶矽薄膜電晶體沒有相對應的模式，無法萃取出元件的等效

參數，若要進行電路模擬必有極大困難。吾人研究一套不需要萃取出元件參數的方法，而直接進行三維度元件暨電路模擬(Mixed-Mode)。結果顯示，以全閘極結構複晶矽薄膜電晶體組成之電路具有快速切換開關的能力，和工業標準之單閘極複晶矽薄膜電晶體電路比較，有9倍以上的改良。

總之，本研究已經藉由元件結構的改良，研究了複晶矽薄膜電晶體基本電特性以及驅動電路的性能；期盼低溫複晶矽製程技術的成長，未來希望能將顯示電路應用在玻璃基板上，使得面板電路積體化可以實現。

Numerical Simulation of Gate-All-Around Polysilicon Thin-Film Transistors and Circuits

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ABSTRACT

This thesis numerically simulates gate-all-around (GAA) poly-Si thin film transistors and circuits. Firstly, the Poisson's and drift-diffusion equations are decoupled according to Gummel's procedure. Based on adaptive one-irregular mesh, each decoupled partial differential equation (PDE) is discretized and then solved iteratively using Newton's method. Since the barrier height and potential of the grain boundary (GB) are complex non-linear functions, the computational time is very large. After calibration with reference to measurements, the barrier height of GB equals 0.15 eV and the concentration of GB is approximately 3×10^{13}/cm^2.

Based on the extracted parameters of GB, the performance of poly-Si TFTs on the sub-micron scale is analyzed. When the channel length is 300 nm, it is approximately the size of one grain. The effects of GB at various positions are investigated. The position near the drain side exhibits a large variation in the threshold voltage (V_{th}). This effect can be suppressed by GAA poly-Si TFTs: the variation of V_{th} can be reduced to 5 % of that of single gate (SG) poly-Si TFTs. GAA poly-Si TFTs also have the following advantages. (1) The mobility of the electron increases. (2) The excellent channel controllability due to the natural infinite gate is such that the drain-induced barrier is lowered (DIBL) and the subthreshold swing (S.S) reduced. A lightly doped drain (LDD) profile is considered to reduce the leakage currents; the On/Off ratio increases. (3) The smaller variation of V_{th} makes the current in the active-matrix driving circuit more stable. Additionally, 90 nm GAA poly-Si TFTs are simulated using quantum correction models. If the size of GB is

maintained within 2 nm, the variation of V_{th} is independent of the position of GB.

Since the GAA poly-Si TFTs have no compact device models, the simulation of the active-matrix driving circuit seems to be impossible. A three-dimensional simulation of devices coupling circuits is developed and compact models are not required. The procedure is called the mixed-mode method. For 2T1C and 4T2C active-matrix driving circuits, the results reveal that the switching speed of GAA poly-Si TFTs can be improved by a factor of nine above that obtained using SG poly-Si TFT circuits. We further simulate Goh's active-matrix driving circuit and the variation of OLED is reduced to 0.01 V.

Changing the structure of poly-Si TFTs can markedly improve the performance of devices and circuits. We hope for many display applications and the successful use of integrated circuits.

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李柏賢　謹誌

中華民國九十六年六月 于風城交大

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Chapter 1

Introduction

In recent years, polycrystalline silicon thin-film transistors (poly-Si TFTs) present great interest for applications. The higher performance of active-matrix liquid crystal displays (AMLCDs) employ many thin-film transistors (TFTs) in each pixel [1, 2].

The poly-Si TFTs papers are appearing in many professional journals and the clear trend is that the number increases constantly. The ploy-Si TFTs integrate drivers from the structures and reduce the device size [3]. If reducing the size of devices, they have the advantages including larger on-state current, smaller chip area, smaller consuming power, and higher aperture ratio. Although amorphous silicon (a-Si) technology is less expensive than poly-Si TFT technology, the effective electron mobility in a-Si is typically less than $1\mathrm{cm}^2/\mathrm{Vs}$, it is not practical to implement a significant portion of the display-driver circuitry using a- Si TFTs, particularly for video-rate displays [4]. The poly-Si TFTs allow a higher resolution and have a higher aperture ratio in each pixel than a-Si. The most important is that poly-Si TFTs exhibit higher mobility values and deliver higher driving current [5]. The other popular area is organic light emitting diodes display (OLED). They are presently of great interest due to their potential application in high efficiency displays. Driving the OLEDs with an active matrix leads to lower voltage operation, lower peak pixel currents, and a display with much greater efficiency and brightness. Since the brightness is proportional to the current driving through the OLED, the role of the active matrix is to provide a constant current throughout the entire frame time and eliminate the high peak currents in the passive matrix. Based on above results, the powerful driving current of devices are developed. The symmetric double-gate (DG) [6–11] and gate-all-around (GAA) [12–20] poly-Si TFTs have been of great interest. Those structures not only improve the characteristics and short channel effects but also increase the driving current and mobility. Some groups fabricated large size of grain and eliminate the probability of grain boundary [21–25].

In this thesis, the numerical simulation of gate-all-around (GAA) poly-Si TFTs thin film transistors and circuits are explored. Because the barrier height and potential of grain boundary (GB) are the complex non-linear function, it makes the computational time increase largely. After calibrating with measurement data, the barrier height and the concentration of GB are extracted. Using the extracted parameters of GB, I analyze the short channel of poly-Si TFTs. When the channel length is equal to 300 nm (about one single grain size), it maybe exists single grain boundary. The position near the drain side has a significant effect on device performance. The influence can be suppressed with GAA poly-Si TFTs. Using GAA structure, the variation of threshold voltage (V$_{th}$) can be reduced. The simple active-matrix driving circuit is including two transistors and one capacitor (2T1C). We also demonstrate the 2T1C active-matrix driving circuit using GAA and SG poly-Si TFTs for OLED device [26], and the results are fairly encouraging. Compared to the circuits of SG poly-Si TFTs, the circuits with GAA poly-Si TFTs exhibit a great improvement in switching speed, driving current, and higher stability of output voltage.

1.1 Background and Literature Review

Fully numerical modeling of a semiconductor device based on partial differential equations which describe all different regions of a device was first suggested by Gummel in 1964 [27] for one dimensional bipolar transistor. This approach was further developed and applied to p-n junction by DeMari [28]. A two dimensional solution of Poisson's equation with application to a MOS structure was first published by Leob et al. [29]. Kennedy and O'Brien [30] in 1969 investigated the junction field transistor by means of two dimensional numerical solution of Poisson's equation and one continuity equation. At the same time, Slotboom [31] presented a two dimensional analysis of the bipolar transistor solving Poisson's equation and both continuity equations. Since the two dimensional modeling has been applied to nearly all important devices. Many activities have been concentrated on the simulation of MOS devices due to their two dimensional nature in 1982 [32] and 1983 [33]. Two dimensional transient simulation of MOSFET's have been carried out by Mock [34], Oh et al. [35] and Yamaguchi [36]. Three dimensional static modeling has been reported in [37].

In order to obtain high chip density, low power dissipation, and high speed for devices [38], the reduction of the gate oxide thickness and channel length are necessary .This results in a narrow and deep potential well at the semiconductor-insulator interface. According to quantum-mechanics (QM), electrons are now confined in such a potential well and then quantized to many discrete energy levels consequently force the motion of the electron in the direction perpendicular to the silicon-insulator interface . Since the quantum effect becomes noticeable in the deep-submicron MOSFETs and a mere classical description of the physics is not sufficient for an accurate calculation of the inversion-layer [39,40]. In order to understand the characteristics of a nano scale device, it is important to take quantum mechanical effects into account [41].

The important of quantum effects in semiconductor inversion layers was recognized in recent twenty years. In principle, the Schrödinger and Poisson (SP) equations are the most accurate way to handle the problem of the inversion-layer charge density, but it is not suitable for engineering applications especially for the two- and three-dimensional cases [42]. It is expensive computationally and is difficult to generalize to the multi dimension case. Thus, it is important to find a method that can produce a result similar to the Schrödinger and Poisson method but requires similar computation cost as that of the classical calculation. Over the last two decades, various research groups devoted themselves on developing quantum mechanical correction methods. The density-gradient method is another approximation quantum treatment. It is a macroscopic approach to the quantum confinement problem. In the early 1980's, M. G. Ancona and H. F. Tiersten generalized the state of the electron gas to include density-gradient dependence [43, 44]. Later it was extended to describe the quantum mechanical behavior of electrons exhibited in strong inversion layers. Recently, Ancona and his coworkers made further progress on this physically based approach and pointed out that the density-gradient approximation is an effective tool for engineering-oriented analysis of electronic devices in which quantum confinement and tunneling phenomena are significant [45]. The density-gradient method has been fast and accuracy [46].

In 1991, Little et al. showed the results that the current of Off state was 0.1 pA, On/Off ratio was 3×10^8, and the mobility was more than 20 cm^2/V-s [47]. Organic light-emitting diodes (OLED) was required current source, and low-temperature poly-Si (LTPS) can easily deliver at one order of magnitude current for the same size devices.

Those symmetric structures not only improve the device characteristics but also increase the driving current. It is possible to integrate poly-Si TFTs. A. Kumar et al. knew the kink-free polycrystalline silicon double-gate elevated-channel TFTs [10]. In 2001, S. Zhang et al. developed a self-aligned double-gate TFT (DG) [9]. The device operating in the DG mode showed significant performance gains compared to simple top-gate or bottom-gate. In 2005, A. Orouji et al. investigated the double-gate poly-Si TFT with modified channel conduction mechanism for highly reduced leakage current [11]. Y. C. Wu et al. reduced the leakage current in metal-induced lateral crystallization poly-Si TFTs with double-gate and multiple-nanowire channels [12]. S. Miyamoto et al. provide high performance gate-all-around (GAA) TFTs for high density for SRAMs [17]. They also found that the GAA poly-Si were more effective on the decrease of the individual variation than the single-gate poly-Si TFTs in low-voltage operation. Moreover, the Off-state of the GAA poly-Si TFTs with the LDD was almost the same as that of the single-gate poly-Si TFTs. With decreasing the length of channel, the problems of grain boundary would become serious in poly-Si TFTs. Poly-Si TFTs were used with laser annealing to become crystalline and get large size of grain [48–52]. After the fabrication, P. Walker et al. explored effects of grain boundary on subthreshold behavior in single grain-boundary nanoscale TFTs . In order to shorten the time and know the results of TFTs quickly [53], some groups tried to develop the models and simulator. Models of short channel single grain- boundary TFTs were developed by H. Mizuta [54]. H. Watanabe used statistics to describe grain boundaries and understood nanoscopics fluctuation in leakage current [53]. F. V. Farmakis et al. developed the On-state models of large size of grain [55].

In this thesis, we simulate the active -matrix driving circuit and the lighting device is OLED. The luminance of OLED diplay is known to be higher than 500 cd/m^2. Not using a backlight system, it provides a wide viewing angle of over 160°. It also has fast response time of 10 μs. The OLED is nearly proportional to the current flowing. As result, circuit design methods based on typical VLSI technologies cannot be directly applied for designing poly-Si TFTs circuits. Threshold voltage is another parameter to consider. Ohtani et al. have reported the threshold voltages of 0.12 V and -1.00 V for n- and p-channel poly-Si TFTs [56]. In micro scale, the threshold voltages are usually controlled to have 2 V to 3 V [57]. The traps states associated grain boundaries greatly affect the noise characteristics of poly-Si TFTs. Currently, well-established SPICE model of GAA poly-Si TFTs is not available for circuit simulation. Therefore, we develop a circuit-device coupled mixed mode simulation technique to explore the circuit behavior. The mixed-mode methods contains devices and circuits simulation [58, 59]. The characteristics of OLED are taken from the measured [26].

1.2 Motivation

Reproduction is an important issue in electronic industry. For high performance, application high mobility, a large grain size, and a short channel length become necessary. With decreasing the channel length, it increases the characteristic variation of poly-Si TFTs. It will result in unacceptable levels of display uniformity and power dissipation. One of the important issues in poly-Si TFTs is how to produce perfect crystal of silicon on glass. Unfortunately, we still encounter grain boundary happening in poly-Si TFTs; therefore, we must think about other ways to improve the device performance. Adopting new structure is a promising way in modern technology. In our research group, we explore the GAA structure of poly-Si TFTs and try to find the better performance. I have surveyed special structures of poly-Si TFTs in many professional journals. Very clear, the trend is that the number of such research activities increases constantly. The circuit simulation using mixed-mode methods is popular and interesting. It is necessary and accurate because the compact models of novel devices are lacked. The mixed mode methods contains devices and circuits simulation and we develop a device coupling circuit technique to explore the behavior. It is my motivation to study this topic in my master thesis.

1.3 Outline

The outline of the thesis is as follows. The device structures and physics of the poly-Si TFTs are shown in Chap. 2. In Chaps. 3 and 4, I discuss the relative models and the detail of numerical methods. The simulation of poly-Si TFTs with different structures from 5μm to 300 nm are listed in Chap. 5. Besides, I also consider the positions and the size of grain boundary. Moreover, the performance of 90 nm poly-Si TFTs using quantum mechanical models is also explored. I study the active-matrix driving circuit (2T1C) with 300 nm gate-all-around poly-Si TFTs and analyze the stability of circuit in Chap. 6. Our adaptive circuit simulation is mixed-mode method and compact model is needless. The chapter 7 includes a summary of this work and suggestion for future work. A source code for the numerical solution of the 2D Poisson equation is listed in Appendix A and the explored mixed mode code is listed in Appendix B.

Chapter 2

Device Structures and Physics

The chapter focuses on devices of poly-Si TFTs. For each structure, the fundamental advantages and disadvantages of device will be described. If we have better driving capability of poly-Si TFTs, the panel will become brightly colored. The off-state current of poly-Si TFTs, referred to as leakage current, is due to traps in the channel. To improve the performance of poly-Si TFTs, we explore and compare the electrical characteristics of the poly-Si TFTs with different gate structures. By evaluating the transfer and output characteristics, the gate-all-around poly-Si TFTs demonstrate better driving capability. It mainly results from that the gate-all-around poly-Si TFTs with a large coverage ratio, and can improve short channel effects. Before simulating, we must know the device structures and physics.

2.1 Device Structures

There are some ways to fabricate different structures of poly-Si TFTs. The first production of active-matrix LCDs for pocket TV in 1984 [60]. It was used the top gate poly-Si TFTs with the high temperature process. Since 1980s, the low temperature poly-Si crystallization methods have been developed. Because of the simple structures, single-gate poly-Si TFTs is the popular devices in recent years, shown in Fig. 2.1(a). Based on the technology, large size, integrated driving LCDs has been in production using the top gate poly-Si TFTs [61].

The concept of the double-gate transistor dates back to 1984 [61]. The double-gate (DG) has two gates. One is above and the other is below the channel of poly-Si. If the second gate is connected to first gate, it results in excellent controlling the potential of channel. The structure is shown in Fig. 2.1(b). S. Zhang et al. develope the self-aligned double gate TFT technology. According to their proposed process for DG, they find out that the On-state current of DG is twice as big as SG. Although the high transconductance and suppression of kink effect have been observed in the DG poly-Si TFTs, a high leakage current is observed. This is improved by adding the LDD regions into the DG. Kumer et al. [10] explore the kink-free I-V characteristics, low leakage current, and higher On-state current compared to conventional poly-Si TFTs.

We know that the variation of the threshold voltage is serious problem when channel length narrows down to sub-micron scale. The threshold voltage will decide the On-state current and we must make it constant as well as possible. Here, we study the new structure of poly-Si TFTs in Fig. 2.2 and Fig. 2.3.

There are two major types in gate-all-around structure. One is circle-shape gate, and the other is square-shape gate. We study the square-shape gate in this thesis. However, one major difference is that the square-shape gate is full of electric field in the corner. Its controlling ability is inferior to circle-shape gate, but the defects cannot obscure the virtues. It still provides the better driving force than the conventional poly-Si TFTs. We will discuss the details in chapter 5. The structures of gate-all-around (GAA) can suppress the variation induced by grain boundaries in the channel. In addition to improve the average performance, it is compared with the conventional single gate TFT (SG) [14] [17]. The results clearly confirm this effect in terms of the current(I)- voltage(V) characteristics. The high performance enables reduction of the size and provides a large On-state current. The fabrication of GAA is shown in Fig. 2.3(c). The GAA poly-Si TFTs show high channel conductance and features of shield structure peculiar to the double-gate poly-Si TFTs. It can also eliminate an anomalous leakage current which appears in the sub-micron regime. Since the GAA poly-Si TFTs require only one additional mask layer if comparing with the conventional single-gate poly-Si TFTs.

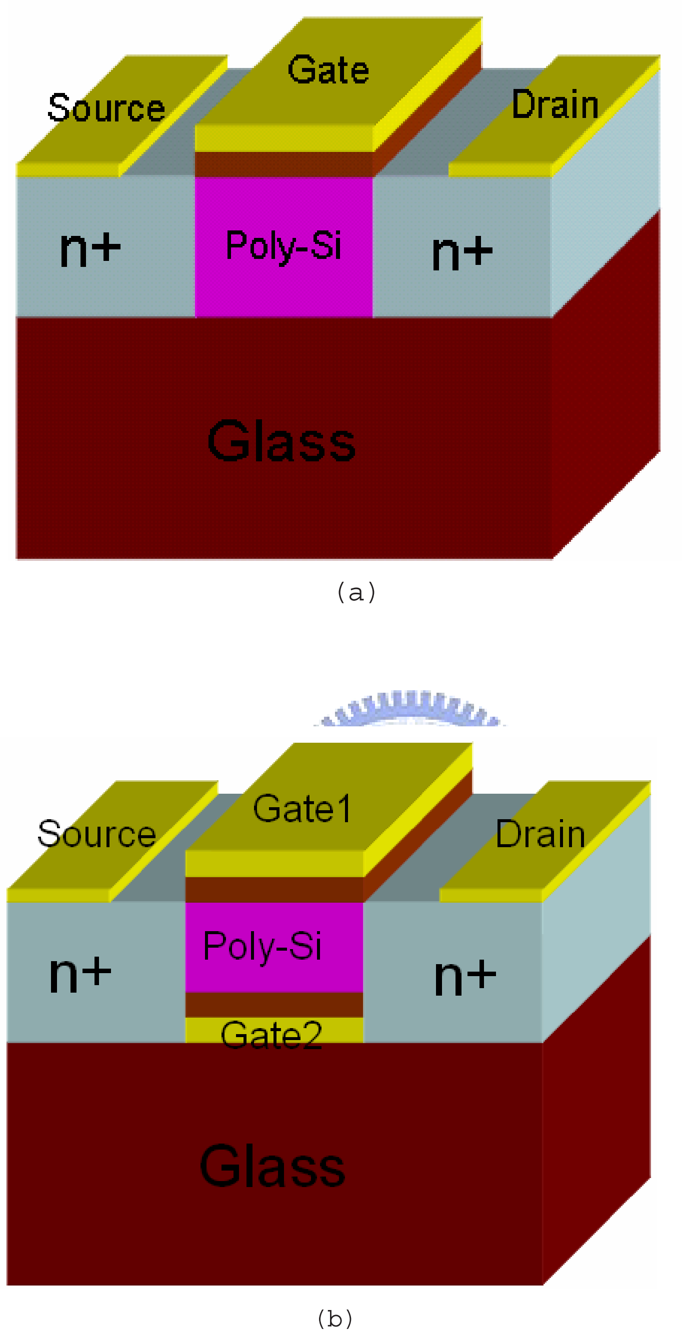
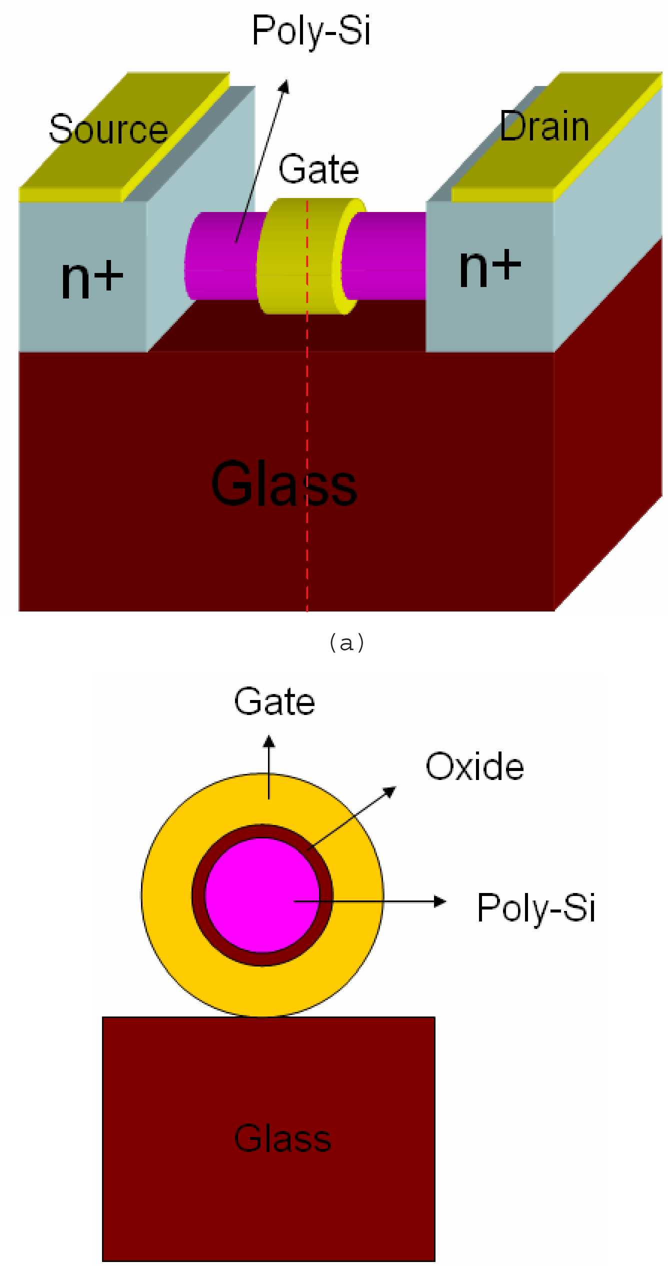


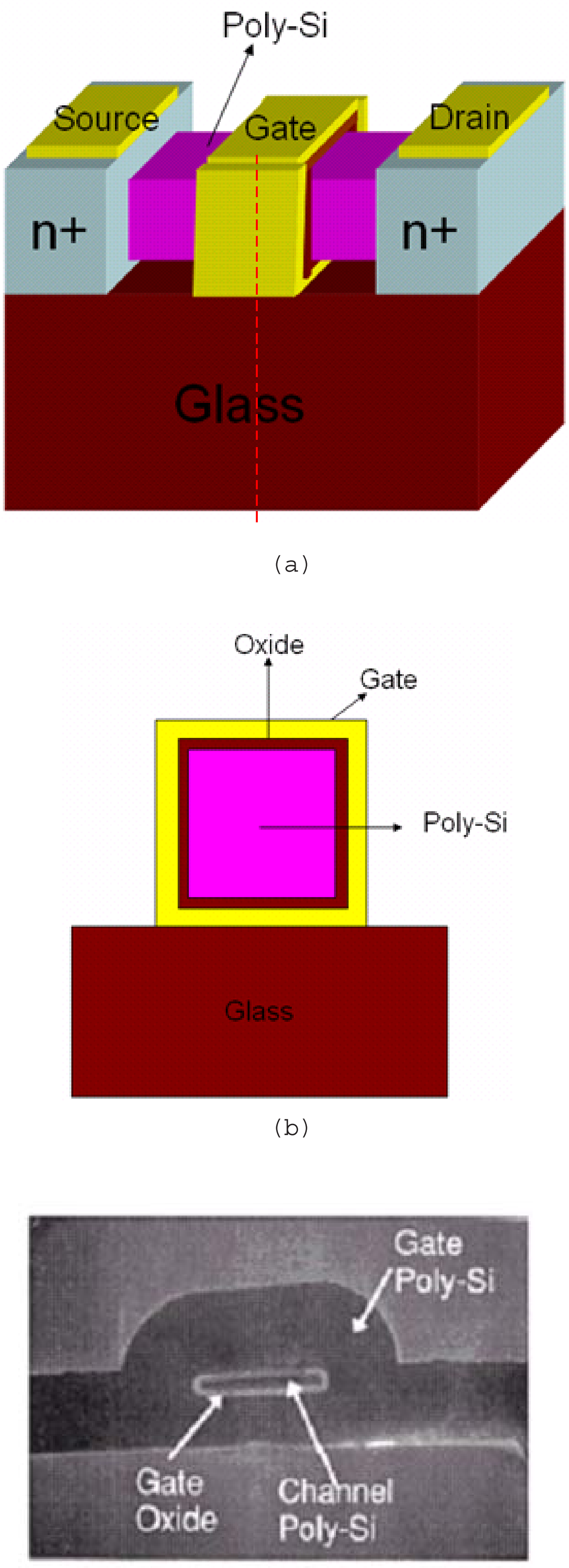
Figure 2.1: (a) A n-type of single top gate structure and (b) a double-gate structure. The source and drain of the device are phosphorous doping and the channel is boron doping.



(a)

(b)

Figure 2.2: (a) The gate-all-around structure (b) and the 2D cross section along the red dash line.



(a)

(b)

(c)

Figure 2.3: (a) Another gate-all-around structure, the square-shape-gate device, (b) the 2D cross section of square-shape gate along the red line, and (c) the SEM micrograph of GAA [17].

2.2 Grain Boundary Effects

The poly-Si TFTs uses a thin poly-Si as the channel layer. It is known that the performance of TFTs is limited by the large amount of randomly oriented grain boundaries (GBs) existing in the channel. The interface between the two grains is called grain boundary. This is because the substrate of TFT is glass. It is different from the MOSFET device. We must fabricate the device under low temperature and grain boundary happens at this time. The random grain orientation leads to significant device-to-device variation and poor circuit yield. So it is important to understand the effects of discrete GBs on conduction [62–66].

The effects of grain boundary can be reduced mainly by enhancing the grain size and reducing the number of grain boundaries present within the channel. We can know the grain size in Fig. 2.4. The grain size is relative to the performance and it can be substituted physically with effective models. Recently, combination of solid phase crystallization (SPC) and excimer laser annealing (ELA) were employed to improve the poly-Si TFTs performance through grain size enlargement and reduction of the grain boundary and in-grain defect density [48–52].

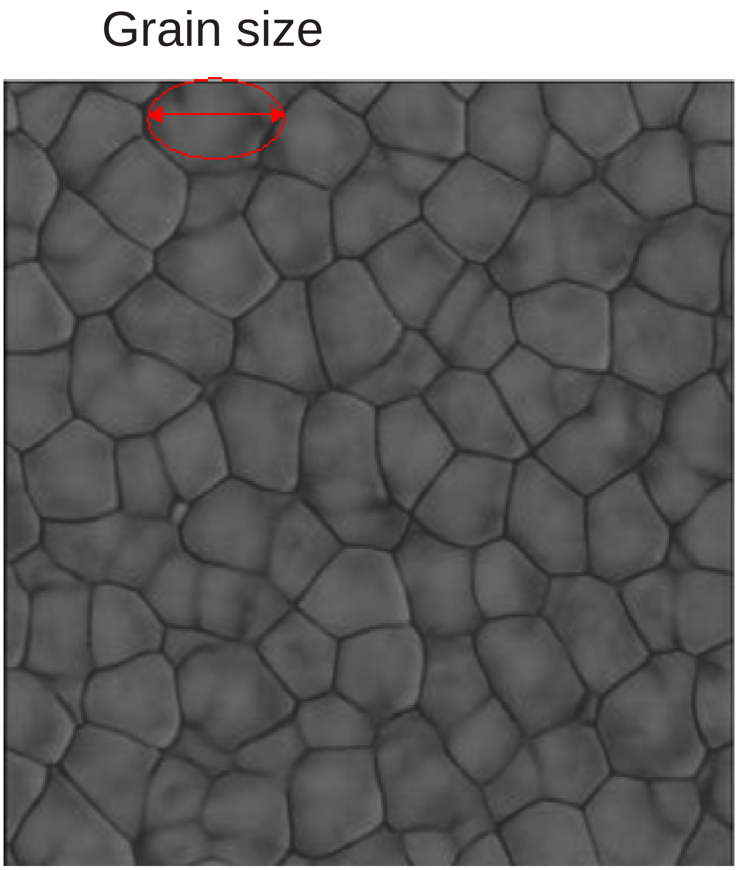


Figure 2.4: Atomic force microscopy (AFM) picture of the real grain and the grain size is about 0.3 μm [62].

2.3 Short Channel Effects

We know the V$_{th}$ will decide the On-state current. On-state current influences to the brightness of OLED. I provide my method to calculate the value of V$_{th}$. Firstly, we calculate the on-state current:

$$I_{turn-on} = \frac{W}{L} \times 20nA, \tag{2.1}$$

where W is channel width, and L is channel length. From the simulated data in I$_D$-V$_G$ curve, we use linear extrapolation method to calculate V$_{th}$. I$_{on}$/I$_{off}$ ratio is another important factor of poly-Si TFTs. Higher I$_{on}$/I$_{off}$ ratio represents not only large On-state current but also small Off-state current. There are many methods to specify the on- and off-state current. The definition of On-state current is maximum current and the Off-state current is the minimum leakage current. The On/Off ratio is:

$$\frac{I_{on}}{I_{off}} = \frac{I_{max}}{I_{min}}. \tag{2.2}$$

Besides, the ratio must be larger than 10^6 and the device can be operated successfully. Under Off-state condition, the potential barrier at the surface prevents electron current from flowing to the surface. The surface potential is controlled by the gate voltage. When the gate voltage is below the threshold voltage, there are only a limited number of electrons injected from the source over the barrier and collected by drain. In long -channel case, source and drain fields only affect the ends of the channel. As the channel length is shortened, the source and drain fields penetrated deeply into middle of the channel, which lowers the potential barrier. This causes a substantial increase of the subthreshold current. The threshold voltage becomes lower than the long-channel value.

When a high drain voltage is applied to a short-channel device, the barrier height is lowered, resulting in further decrease of the threshold voltage. DIBL is one kind of short-channel effects. The DIBL are simply calculated from the threshold altering for different applied drain voltages. In I_D-V_G curve, the DIBL is calculated by:

$$V_{th-off-state} - V_{th-on-state}. \tag{2.3}$$

It has been found a large channel length will cause a smaller DIBL effect. This consequence is reasonable that increasing the gate length will enhance the controlling ability. But the on current will decrease. Base on two conditions, we develop the GAA structure to enhance gate controlling ability .The performance of GAA is still excellent in short channel. The subthreshold swing is simultaneously becoming greater for the shorter gate devices. From the engineering of view, those characteristics will be an important issue for scaling down the devices. Subthreshold swing S.S. (mV/dec) is a typical parameter to describe the control ability of gate toward channel. It is defined as the amount of gate voltage required to increase/decrease drain current by one order of magnitude. The subthreshold swing should be independent of drain voltage and gate voltage. However, in reality, the subthreshold swing might increase with drain voltage due to short channel effects such as charge sharing, avalanche multiplication. The dependence on gate voltage is exponential with a subthreshold slop:

$$S = \left(\frac{\partial(\log_{10} I_{ds})}{\partial V_g}\right)^{-1}. \tag{2.4}$$

For circuits, a steep subthreshold slop is desirable for the case of switching transistors current off. If the value is close to 60 (mV/dec), it means the device is better.

Chapter 3

Device Models

In this chapter, a physical-based nonlinear trap model is introduced which describes the effect of grain topologies on the intrinsic physical quantities, such as potential energy and electron density for poly-Si TFTs. The nonlinear trap model is solved together with Poisson's equation in a set of the two-dimensional (2D) drift-diffusion (DD) equations. In the numerical solution of nonlinear-trap corrected DD equations for poly-Si TFTs, a computationally cost-effective adaptive computing technique is implemented [67–71]. First of all we decouple the three partial differential equations (PDEs) in the set of DD equations according to Gummel's procedure [72, 73]. Based on adaptive 1-irregular mesh [74] and finite volume (FV) approximation [67, 71], each decoupled PDE is discretized and then solved by means of the Newton's iteration [75]. Using a error estimation, the gain boundary induced variation of physical quantities, such as electric field and gradient of electron density, are accurately calculated and automatically tracked. Testing on different poly-Si TFTs, the proposed adaptive computing technique shows the simulation accuracy and numerical robustness. Achieved result shows that our computational approach provides a cost-effective way to solve a set of DD equations with the nonlinear trap model of grain boundary for advanced poly-Si TFTs' simulation.

3.1 The Drift-Diffusion Model

In this section, we state a 2D steady state mathematical model of DD equations together with the nonlinear trap model for poly-Si TFTs, shown in Fig. 3.1. It is known that classical DD equations consist of three coupled PDEs, the Poisson's equation, the current continuity equation of electron, and the current continuity equation of hole [76–78]. By considering the nature of poly-Si TFTs induced grain boundaries [62, 64, 76, 78] in the structure of poly-Si TFTs, a set of 2D DD equations is give by

$$\Delta\phi = \frac{q}{\varepsilon_s}(n - p + D(x,y) + BT(\phi)), \tag{3.1}$$

$$BT(\phi) = N_{TA} f_{n0} exp(-\frac{\phi - E_B}{V_T}), \tag{3.2}$$

$$\frac{1}{q}\nabla\cdot(-q\mu_n n\nabla\phi + qD_n\nabla n) = R(n,p), \tag{3.3}$$

and

$$\frac{1}{q}\nabla \cdot (-q\mu_p p \nabla \phi + qD_p \nabla p) = -R(n, p). \tag{3.4}$$

Equation (3.1) is the so-called Poisson equation, where the unknown $\phi = \phi(x, y)$ to be solved in the domain, shown in Fig. 3.1, is the electrostatic potential. The source code for 2-D Poisson equation is shown in Appendix A. Equations (3.3) and (3.4) are the current continuity equations of electron and hole, respectively, where the unknowns n and p to be solved are the densities of electron and hole. In Eq. (3.1), q is the elementary charge, ε_s is the silicon permittivity, and $D(x, y)$ is the spatial-dependent doping profile [77]. Equation (3.2) is a distribution function of the grain boundary which occurs on the grain boundaries $\overline{gb_i gb'_i}, i = 1, ..., l$, where l is the number of grain boundaries, shown in Fig. 3.2. $BT(\phi)$ in Eq. (3.2) is a nonlinear equation of electrostatic potential ϕ and is solved together with the Poisson equation in Eq. (3.1). N_{TA} is the acceptor-liked trap surface concentration and $f_{n0} exp(-\frac{\phi - E_B}{V_T})$ is the occupation probabilities of electron. E_B is assumed to be the barrier height of the trap. f_{n0} is an initial probability of electron. μ_n and μ_p in Eqs. (3.3) and (3.4) are the mobilities of electron and hole. D_n and D_p are the diffusion coefficients of electron and hole, and $R(n, p)$ is the term of generation-recombination of electron and hole [77].

Eqs. (3.1)-(3.4) are subject to proper boundary conditions for ϕ, n, and p [67, 68, 72, 79, 80], shown in Fig. 3.1. The boundaries $\overline{cd}$, $\overline{fh}$, and $\overline{aj}$ are specified by the type of Dirichlet boundary condition for ϕ, n, and p, respectively. In order to guarantee that the simulated poly-Si TFTs are self contained, the boundaries $\overline{ac}$ and $\overline{hj}$ are assumed to be the homogeneous Neumann boundary condition for ϕ, n, and p, respectively. On the interfaces of Si and SiO_2, the boundaries $\overline{df}$ and $\overline{eg}$, Gauss's law in differential form must be obeyed for ϕ. For the current continuity equations of electron and hole, we assume that the SiO_2 and glass are perfect insulators, and that the surface recombination rate is zero. Under these circumstances, the normal components of the electron and hole currents vanish on the interfaces, the boundaries $\overline{df}$ and $\overline{eg}$. It results in the homogeneous Neumann boundary condition for n and p.

We first investigate the contacts. As a boundary condition for the electrostatic potential we have in general a functional relation between the electrostatic potential and the total current density, which can include first order derivatives with respect to time and the unit vector perpendicular to the boundary and integrals with respect to time and the area of the contacts. We denote this with the following implicit relation:

$$I = \int_{\partial D_0} (\overrightarrow{J_n} + \overrightarrow{J_p}) \cdot d\overrightarrow{A} - I_D(t) = 0, \tag{3.5}$$

where ∂D_0 denotes the parts of the boundary corresponding to contacts. The category of boundaries are interfaces between the semiconductor and insulating material. At such interfaces, the laws of the differential form must be obeyed :

$$\varepsilon_{sem} \cdot \frac{\partial \phi}{\partial \overrightarrow{n}}|_{sem} - \varepsilon_{ins} \cdot \frac{\partial \phi}{\partial \overrightarrow{n}}|_{ins} = Q_{int}, \tag{3.6}$$

where ε_{sem} and ε_{ins} denote the permittivity in the semiconductor and insulator. Q_{int} represents charges at the interfaces.

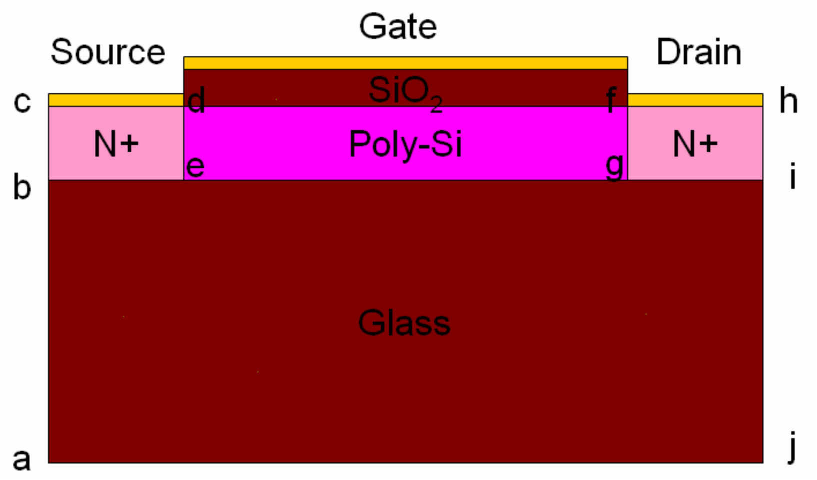


Figure 3.1: A cross-section view of the simulated poly-Si TFTs.

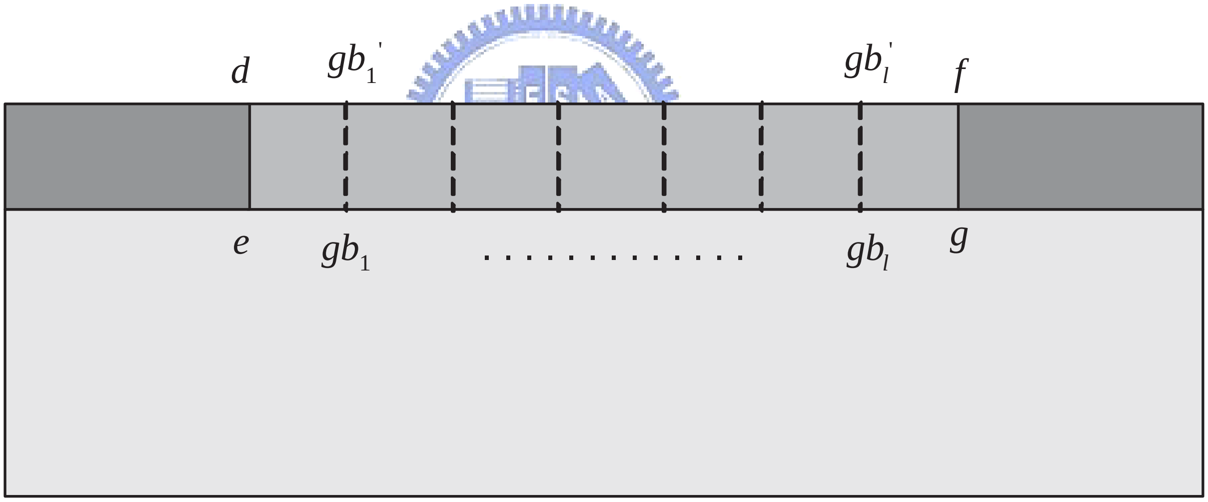


Figure 3.2: An illustration of the cross-section view and boundary conditions of grains.

3.2 The Density Gradient Model

The density-gradient (DG) model is an approximate approach to the QM correction of the macroscopic electron transport equation [40, 43, 81]. In this approach, an extra term is introduced in the carrier flux by making the equation of state for the electron gas density-gradient dependent.

$$\overrightarrow{J_n} = -qn\mu_n\nabla\phi + qD_n\nabla n - qn\mu_n\nabla(2b_n\frac{\nabla^2\sqrt{n}}{\sqrt{n}}), \tag{3.7}$$

where b_n is the density-gradient coefficient which determines the strength of the gradient effect in the electron gas and μ_n, D_n, ϕ, and n are mobility, diffusion coefficient, electric potential and electron density, respectively of electrons. The choice of b_n is crucial. The last term on the right hand side of Eq. 3.7 is referred to as quantum diffusion, making the electron continuity equation a fourth-order partial differential equation. This additional singular perturbation term requires a special numerical treatment when the conventional discretization scheme is used.

3.3 Mobility Models

Many different trap density distributions have been proposed to describe the position and density of the traps within the poly-Si band gap. We have showed the new Poisson equation in Eq. (3.1). Trapped electron and hole concentrations on one energy level are related to occupation probabilities for electrons and holes. These results are consistent with an equivalent circuit model [82] where the channel is composed by grains of size L$_G$ with mobility μ_G and grain boundaries of size L$_{GB}$ with mobility μ_{GB}. With this assumption the overall effective mobility μ is given by [83]

$$\frac{L_G + L_{GB}}{\mu} = \frac{L_G}{\mu_G} + \frac{L_{GB}}{\mu_{GB}}. \tag{3.8}$$

μ_{GB} increases with gate voltage, Eq. 3.8 states that for small L$_G$, μ is controlled by μ_{GB} and therefore it increases with V$_G$.

The University of Bologna bulk mobility model was developed for an extended temperature range between 25°C and 400°C [84]. It should be used together with the University of Bologna inversion layer mobility model. First, attractive and repulsive scattering are separately accounted for, therefore, leading to a function of both donor and acceptor concentrations. A suitable temperature dependence for most model parameters is introduced to predict correctly the temperature dependence of carrier mobility in a wider range of temperatures, with respect to other models. The temperature dependence of lattice mobility is reworked, with respect to the default temperature. The model for lattice mobility is:

$$\mu_L(T) = \mu_{max}(\frac{T}{300K})^{-\gamma + c(\frac{T}{300K})}, \tag{3.9}$$

where μ_{max} denotes the lattice mobility at room temperature, and c gives a correction to the lattice mobility at higher temperatures.

In high electric fields, the carrier drift velocity is no longer proportional to the electric field strength, instead, the velocity saturates to a finite speed v_{sat}. The Canali model is available in different versions (one for drift-diffusion and thermodynamic, and one for hydrodynamic simulations) [85]. The Canali model originates from the Caughey-Thomas formula, but has temperature-dependent parameters, which were fitted up to 430 K.

$$\mu(F) = \frac{\mu_{low}}{[1 + (\frac{\mu_{low}^{F}}{\nu_{sat}})^{\beta}]^{\frac{1}{\beta}}}, \tag{3.10}$$

where μ_{low} denotes the low field mobility. In this thesis, I select overall effective mobility in Eq. 3.8.

3.4 Recombination Models

Recombination through deep levels in the gap is usually labeled Shockley-Read-Hall (SRH) recombination. The following form is implemented:

$$R_{net}^{SRH} = \frac{np - n_{i,eff}^2}{\tau_p(n + n_1) + \tau_n(p + p_1)}, \tag{3.11}$$

with:

$$n_1 = n_{i,eff} e^{\frac{E_{trap}}{kT}} \tag{3.12}$$

and

$$p_1 = n_{i,eff} e^{\frac{-E_{trap}}{kT}}, \tag{3.13}$$

where E_{trap} is the difference between the defect level and intrinsic level. τ_n is the minority lifetime of electron and τ_p is the minority lifetime of hole.

The radiative (direct) recombination model expresses the recombination rate as a function of the carrier concentrations n and p, and the effective intrinsic density $n_{i,eff}$:

$$R = C \cdot (np - n_{i,eff}^2), \tag{3.14}$$

where C = 2E-10 cm^3/s for GaAs and C = 0 cm^3/s for other materials.

The rate of band-to-band Auger recombination R^A is given by:

$$R^A = (C_n n + C_p p)(np - n_{i,eff}^2), \tag{3.15}$$

with temperature-dependent Auger coefficients

$$C_n(T) = (A_{A,n} + B_{A,n}(\frac{T}{T_0}) + C_{A,n}(\frac{T}{T_0})^2)(1 + H_n e^{-\frac{n}{N_{o,n}}}), \qquad (3.16)$$

$$C_{np}(T) = (A_{A,p} + B_{A,p}(\frac{T}{T_0}) + C_{A,p}(\frac{T}{T_0})^2)(1 + H_n e^{-\frac{n}{N_{o,n}}}), \qquad (3.17)$$

where T_0 = 300 K. There is experimental evidence for a decrease of the Auger coefficients at high injection levels. This effect is explained as resulting from exciton decay: at lower carrier densities, excitons, which are loosely bound electron-hole pairs, increase the probability for Auger recombination. Excitons decay at high carrier densities, resulting in a decrease of recombination. The detail of parameters are shown in Tab. 3.1.

Electron-hole pair production due to avalanche generation (impact ionization) requires a certain threshold field strength and the possibility of acceleration, that is, wide space charge regions. If the width of a space charge region is greater than the mean free path between two ionizing impacts, charge multiplication occurs, which can cause electrical breakdown. The reciprocal of the mean free path is called the ionization coefficient α. With these coefficients for electrons and holes, the generation rate can be expressed as:

$$G = \alpha_n n \nu_n + \alpha_p p \nu_p, \qquad (3.18)$$

where ν_n and ν_p denote the drift velocity of electron and hole. Junction breakdown due to avalanche generation is simulated by inspecting the ionization integrals:

$$I_n = \int_0^W \alpha_n(x) \cdot e^{-\int_x^W (\alpha_n(x') - \alpha_p(x'))dx'} dx, \qquad (3.19)$$

Table 3.1: Default coefficients of Auger recombination model.

Symbol	A_A	B_A	C_A	**H(1)**	N_0
Electrons	0.67E-31	2.45 E-31	-2.2E-32	3.46667	1E18
Holes	0.72E-31	4.50E-33	2.63E-32	8.25688	1E18

$$I_n = \int_0^W \alpha_p(x) \cdot e^{-\int_0^x (\alpha_p(x') - \alpha_n(x'))dx'} dx, \tag{3.20}$$

where α_n and α_n are the ionization coefficients for electrons and holes, respectively, and W is the width of the depletion zone. The integrations are performed along field lines through the depletion zone. Avalanche breakdown occurs if an ionization integral equals one. Eq. 3.19 describes electron injection (electron primary current) and Eq. 3.20 describes hole injection. Since these breakdown criteria do not depend on current densities, a breakdown analysis can be performed by computing only the Poisson equation and ionization integrals under the assumption of constant quasi-Fermi levels in the depletion region.

In this thesis, we select the model of Shockley-Read-Hall (SRH) recombination.

3.5 Trap Models

Many different trap density distributions have been proposed to describe the position and density of the traps within the poly-Si band gap. We want to model the inclusion of trap states in the forbidden gap, and the space charge term on the right-hand side of Poisson equation is modified by including an additional charge term, BT(ϕ), representing trapped charge. We have showed the new Poisson equation in Eq. (3.1). We assume that the trap states consist of both donor-like and acceptor-like states distributed across the forbidden energy gap, where the donor-like states act as hole traps and the acceptor-like traps as electron traps. So to ensure a realistic model we chose to include both mid-gap and tail states.

The trapped electron and hole charges are given by :

$$\sum_{E_t}(N_{TD} - n_{Dt}) + \sum_{E_t} p_t, \tag{3.21}$$

$$\sum_{E_t}(N_{TA} - p_{Dt}) + \sum_{E_t} n_t. \tag{3.22}$$

The trap concentration is defined as Gaussian distribution. Where N_{TD} is the donor trap concentration, n_{Dt} is the electron concentration of the donor trap level. N_{TA} is the acceptor trap concentration, p_{Dt} is the hole concentration of the acceptor trap level. n_t is the electron concentration of the neutral electron trap level, and p_t is the hole concentration of the neutral hole trap level. E_t represents trap energy levels.

Seto’s model [86] provides the relation with barrier height and the acceptor-liked trap surface density:

$$E_B = \frac{q^2 N_A}{8\varepsilon}(\frac{N_{TA}}{N_A})^2, \tag{3.23}$$

where (E_B) is the the barrier height and (N_{TA}) is the acceptor-liked trap surface density. ε is the semiconductor permittivity. When E_B is fixed, N_A is proportional to $(N_{TA})^2$. In this thesis, we select the Seto’s model in our simulation.

Chapter 4

Solution Techniques

In this chapter, we will introduce the adoptive numerical methods and illustration examples in the following discussion.

4.1 The Gummel's Decoupling Method

The implemented adaptive computing technique for poly-Si TFTs simulation is mainly based on Gummel's decoupling method [72, 79, 80], FV approximation [68, 69], Newton's method [75], a posteriori error estimation [68], and an 1-irregular meshing scheme [67, 72, 79, 80]. This simulation methodology has recently been developed for different device simulation [68–70]. The Gummel's decoupling method controls an iterative loop over two or more coupled equations. It is used when a fully coupled method would use too many resources of a given machine, or when the problem is not yet solved and a full coupling of the equations would diverge.

To explore the transport behavior of poly-Si TFTs, the three coupled PDEs are numerically solved with Gummel's decoupling method. With a given initial guess $\left(\phi^{(0)},\, n^{(0)},\, p^{(0)}\right)$ and for each Gummel's iteration index g, $g = 0, 1, \ldots$, we first solve the nonlinear Poisson equation

$$\Delta\phi^{(g+1)} = \frac{q}{\varepsilon_s}(n^{(g)} - p^{(g)} + D(x,y) + BT(\phi^{(g+1)})). \tag{4.1}$$

The nonlinear Poisson equation is solved for $\phi^{(g+1)}$ given the previous states $n^{(g)}$ and $p^{(g)}$. The current continuity equation of electron is then solved for $n^{(g+1)}$, with now the known functions $\phi^{(g+1)}$ and $p^{(g)}$

$$\frac{1}{q}\nabla \cdot (-q\mu_n n^{(g+1)}\nabla\phi^{(g)} + qD_n^{(g+1)}\nabla_n^{(g+1)}) = R(n^{(g+1)}, p^{(g)}). \tag{4.2}$$

Finally, we solve the current continuity equation of hole with both $\phi^{(g+1)}$ and $n^{(g+1)}$ known

$$\frac{1}{q}\nabla \cdot (-q\mu_p p^{(g+1)}\nabla\phi^{(g+1)} + qD_p^{(g+1)}\nabla_p^{(g+1)}) = -R(n^{(g+1)}, p^{(g+1)}) \tag{4.3}$$

for $p^{(g+1)}$ until all preset stopping criteria are satisfied. Equations (4.1), (4.2), and (4.3) are associated with proper boundary condition, respectively. We note that Eqs. (4.1), (4.2), and (4.3) are now three individual semilinear PDEs to be solved for each Gummel's iteration. An outer iteration in the procedure of LTPS TFT simulation is then defined by Gummel's decoupling method. We note that analyses of Gummel's decoupling method in device simulation have been reported [68–74, 79, 80].

`The Gummel's decoupling method`

```
Begin
   While $\phi$, $n$, and $p$ in outer loop (Gummel's loop) are not convergent
   If $\phi$ is convergent
      Solve the nonlinear Poisson equation
      with adaptive computing technique.
   End If
   If $n$ is convergent
      Solve the current continuity equation of electron
      with adaptive computing technique.
   End If
   If $p$ is convergent
      Solve the current continuity equation of hole
      with adaptive computing technique.
   End If
  End While
  Call for next calculation.
```

```
End The Gummel’s decoupling algorithm
```

A computational procedure for Gummel’s decoupling method is shown above,and the flow chart is shown in Fig. 4.1.We solve each decoupled PDE with adaptive computing technique.

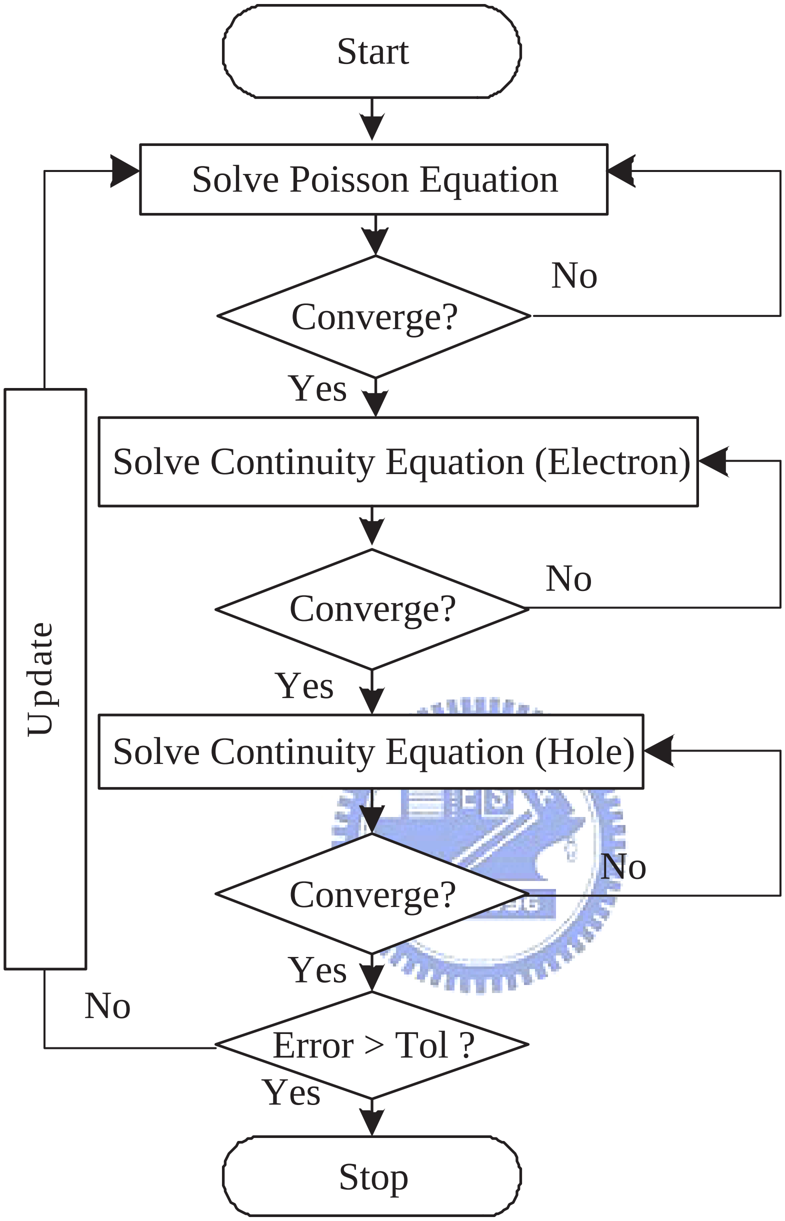


Figure 4.1: A flow chart of the Gummel's decoupling algorithm.

4.2 The Adaptive Finite Volume Method

Based on adaptive 1-irregular mesh [74] and finite volume (FV) approximation. The finite volume method is a numerical method for solving partial differential equations. It calculates the values of the conserved variables across the volume. Before using adaptive finite volume method to solve Poisson equation, we must understand the follow steps:

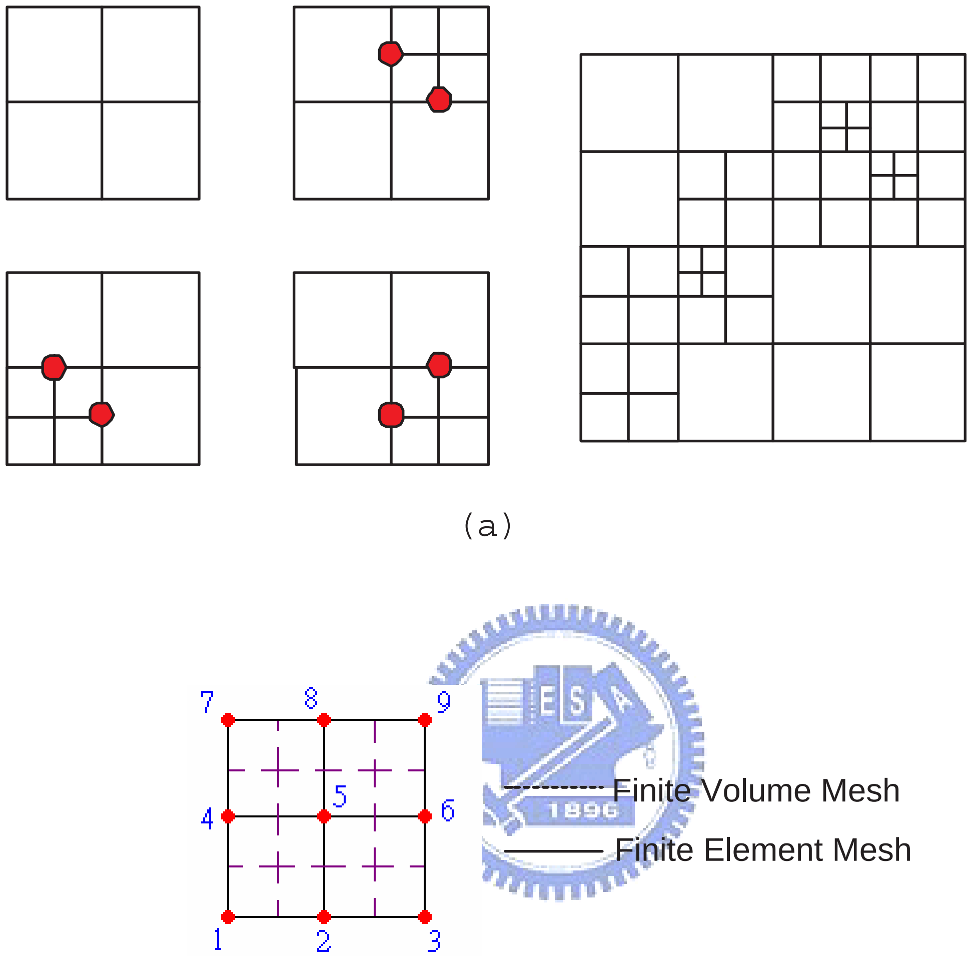
(1) Weak Formulation transforms into weak problem;

(2) Discretize the simulation area by one-irregular mesh;

(3) Form equation **“Ax=B”** by using FV method; and

(4) Error estimation and mesh refinement.

The discretized step divides into structured mesh and unstructured mesh. If according to geometry, it divides into rectangle mesh and triangle mesh. But the rectangle mesh is easier to build than the triangle mesh. The one-irregular method is shown in Fig. 4.2.



(a)

(b)

Figure 4.2: The plot of FV method. (a) One-Irregular mesh (b) and the difference between the finite element mesh and the finite volume mesh.

4.3 The Newton's Iterative Method

The starting solution of initial guess is determined by using a predetermined algorithm. An initial guess of each variable (at each mesh point) in a device required by the solution method including electrostatic potential and quasi-Fermi potentials for electrons and holes. To determine an initial guess for the electrostatic potential and quasi-Fermi potentials, the device is subdivided into wells of n- and p-type doping, such that pn-junctions serve as dividers between wells. Every well is uniquely associated with a contact. The quasi-Fermi potentials in that well are set to the corresponding contact voltage, and the potentials are set to the contact voltage adjusted by the built-in voltage at the contact. For wells that have no contacts, the following equations define the quasi-Fermi potential for the majority carriers:

$$\phi_p = k_{Float} V_{max} + (1 - k_{Float}) V_{min}, \tag{4.4}$$

$$\phi_n = (1 - k_{Float}) V_{max} + k_{Float} V_{min}, \tag{4.5}$$

where k_{Float} is equal to 0. For wells with more than one contact, the well is further subdivided, such that no well is associated with more than one contact.

Newton's method uses the first and second derivatives when the initial point is closed to the solution. In this sections,first, we will show the full coupled solution. For the solution of nonlinear systems, the scheme developed by Bank and Rose [75] is applied. This scheme tries to solve the nonlinear system $g(z) = 0$ by the Newton method:

$$\overrightarrow{g} + \overrightarrow{g}'\overrightarrow{x} = 0 \tag{4.6}$$

$$\overrightarrow{z}^{j} - \overrightarrow{z}^{j+1} = \lambda\overrightarrow{x} \tag{4.7}$$

where λ is selected such that $\|g_{k+1}\| < \|g_k\|$, but is as close as possible to 1. It handles the error by computing an error function that can be defined by two methods.The Newton iterations stop if the convergence criteria are fulfilled. One convergence criterion is the norm of the right-hand side, that is, $\|g\|$ in Eg. 4.6. Natural criterion may be the relative error of the variables measured, such as$\|\frac{(\lambda x)}{z}\|$.

4.4 Illustration Examples

We now present numerical results to demonstrate effect of the proposed physical model and performance of the adaptive computing technique in poly-Si TFTs' simulation. As shown in Fig. 3.1, the simulated TFT device is with $\overline{aj}$ = 4 μm, $\overline{be} = \overline{gi}$ = 1 μm, and $\overline{ac} = \overline{hj}$ = 0.5 μm. The gate oxide thickness of the S_iO_2 layer is equal to 100 nm. The junction depth is with $\overline{bc} = \overline{hi}$ = 0.05 μm. The channel length $\overline{df} = \overline{eg} = 2\mu$m. The 0.3 μm grain size is considered in this work [54, 64]. Hence, there are ten grain boundaries along the direction of channel. The poly-Si TFTs are assumed to have an elliptical-shaped Gaussian doping profile, where the peak concentration is equal to $2 * 10^{20} cm^{-3}$. Fig. 4.3 shows the

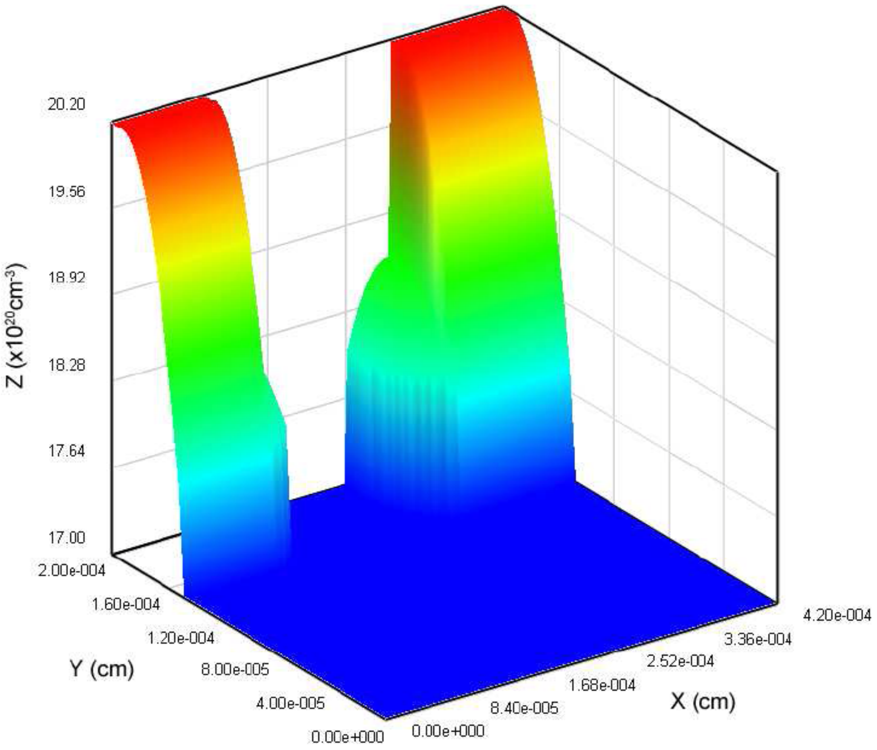


Figure 4.3: An illustration of the doping profile used in the numerical simulation of poly-Si TFTs.

used spatial-dependent doping profile $D(x, y)$ in the poly-Si TFTs simulation. Figs. 4.4 show the process of mesh refinements. The mechanism of 1-irregular mesh refinement is based on the estimation of solution error element by element. Fig. 4.4(a) is the initial mesh which contains 25 nodes, Fig. 4.4(b) is the 4^{th} refined mesh containing 729 nodes, and Fig. 4.4(c) contains 3868 nodes is the 7^{th} mesh. We note that the process of mesh refinement is guided by the result of error estimation automatically. As shown in Fig. 4.4(c), at the 7^{th} refined level we find that most of refined meshes are intensively located near the surface of channel and the junction of the drain side due to large variation of the solution gradient. The distribution of refined mesh is consistent with the profile of computed electrostatic potential, shown in Fig. 4.5. The number of nodes (and elements) versus the number of levels of mesh refinement is shown in Fig. 4.6. The simulations are with and without including the nonlinear trap model to account for the effect of grain boundary. The number of refined elements and nodes is increased as the refinement levels are increased. At the beginning, the number of refined nodes (and elements) is increased fast due to significant variations of computed solution. After several refinements and solution processes, the increasing rate of the number of nodes (and elements) gradually becomes slow when the refinements are increased. It eventually reaches to a saturated condition.

Fig. 4.7 shows the convergence behavior of Gummel's (outer) and Newton's method (inner) when solving the electrostatic potential with and without including the trap model of grain boundary in the simulated TFT device. Here, we also defined an additional linear trap model of grain boundary by setting $BT(\phi) = N_{TA}$. The biasing conditions in all simulation cases are $V_D = 1.0\,V$ and $V_G = 1.0\,V$. The stopping criteria for the inner and outer iteration loops are $1e-6$ and $1e-3$, respectively, for all computed physical quantities. We found that the case of DD simulation without considering any trap models converges quickly among three testing cases. However, the cases of DD simulation with the linear and nonlinear trap models of grain boundary have a similar convergence behavior.

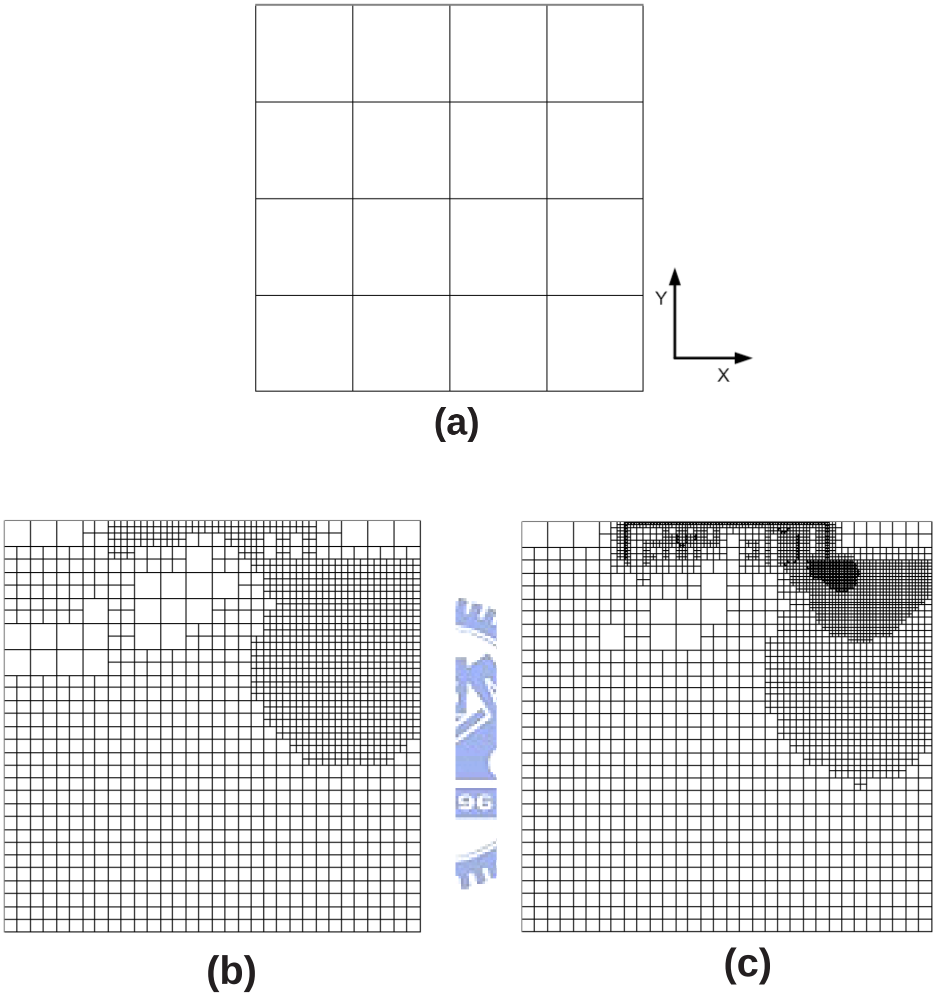


Figure 4.4: (a) The initial mesh used for starting the solution process, (b) the 4^{th} refined 1-irregular mesh which contains 729 nodes, and (c) the 7^{th} refined mesh which contains 3868 nodes.

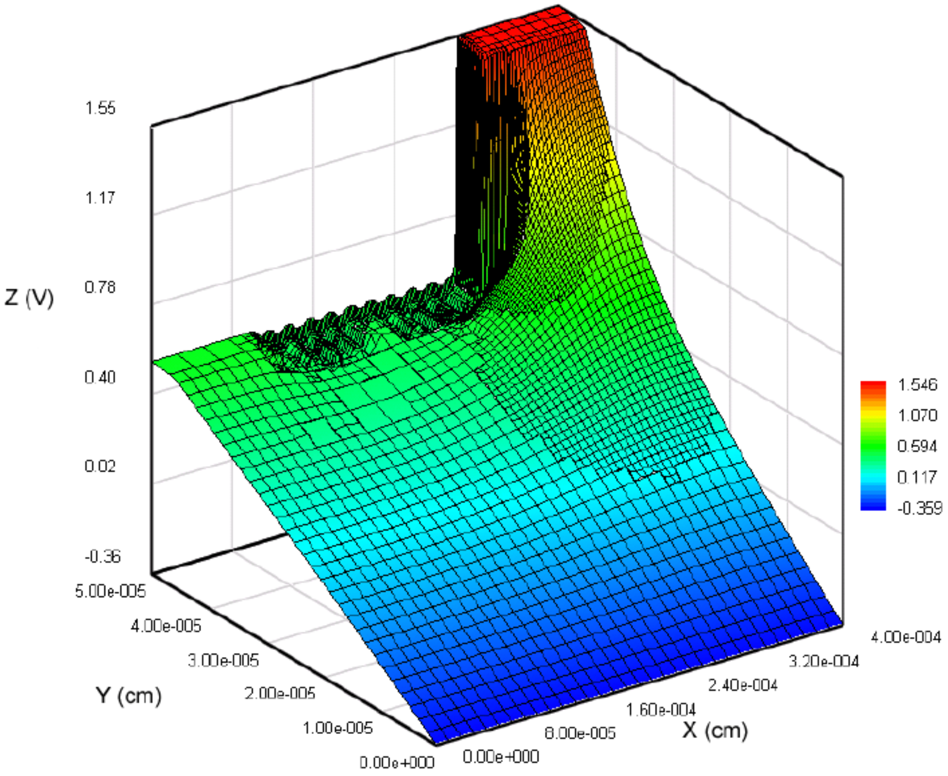


Figure 4.5: The simulated electrostatic potential at the 7^{th} level. The poly-Si TFT is biased at $V_D = V_G = 1.0V$.

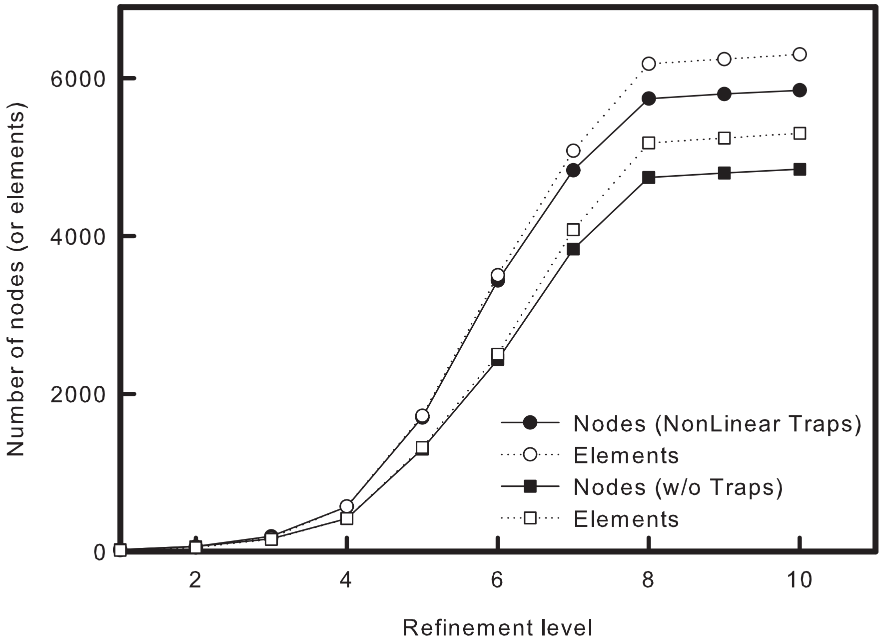


Figure 4.6: The number of nodes and elements versus the refinement levels with and without considering the trap models of grain boundary.

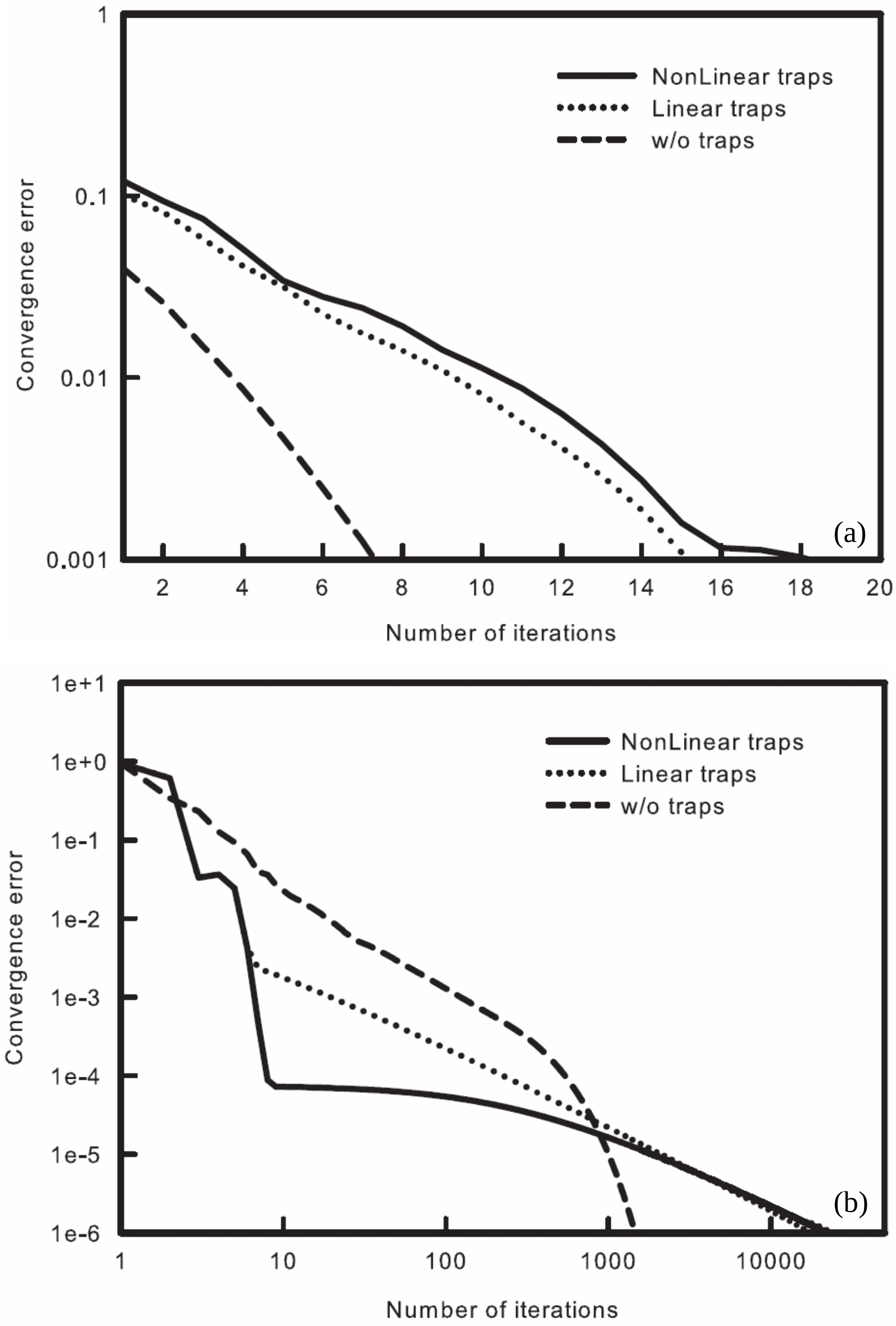


Figure 4.7: (a) A convergence property of Gummel's loop for the numerical solution of DD equations with and without including the trap models of grain boundary, and (b) A convergence behavior for the numerical solution of Poisson equation in the set of DD equations with and without including the trap models of grain boundary, where $V_D = V_G = 1.0$ V .

To explore the effect of grain boundary on the physical characteristics of simulated poly-Si TFT, we examine the computed electrostatic potential and electron density along the channel direction (x direction) shown in Figs. 4.8-4.9, respectively. The upper figure of Fig. 4.8 shows the computed potential profile for the device under bias conditions $V_D = 0.5\ V$ and $V_G = 0.5\ V$, and the lower one in Fig.4.8 is a cross-sectional view of the circled region in the upper figure. The upper figure of Fig. 4.9 shows the electron density and the lower one in Fig. 4.9 is a cross-sectional view of the circled region in the upper figure. Along the channel region of the device, obviously, the simulated potential profile and electron density significantly reveal the effect of grain boundary on the computed physical quantities. As shown in Fig. 4.10, we compare the computed electrostatic potential with different trap models of grain boundary at $V_D = V_G = 0.5\ V$. The case of DD simulation with the nonlinear trap model of grain boundary faithfully describes the traps effect on the charge distribution compared with DD simulation including only the linear trap model. The case of DD simulation without including any trap models does not reflect the effect of grain boundary on the computed potential.

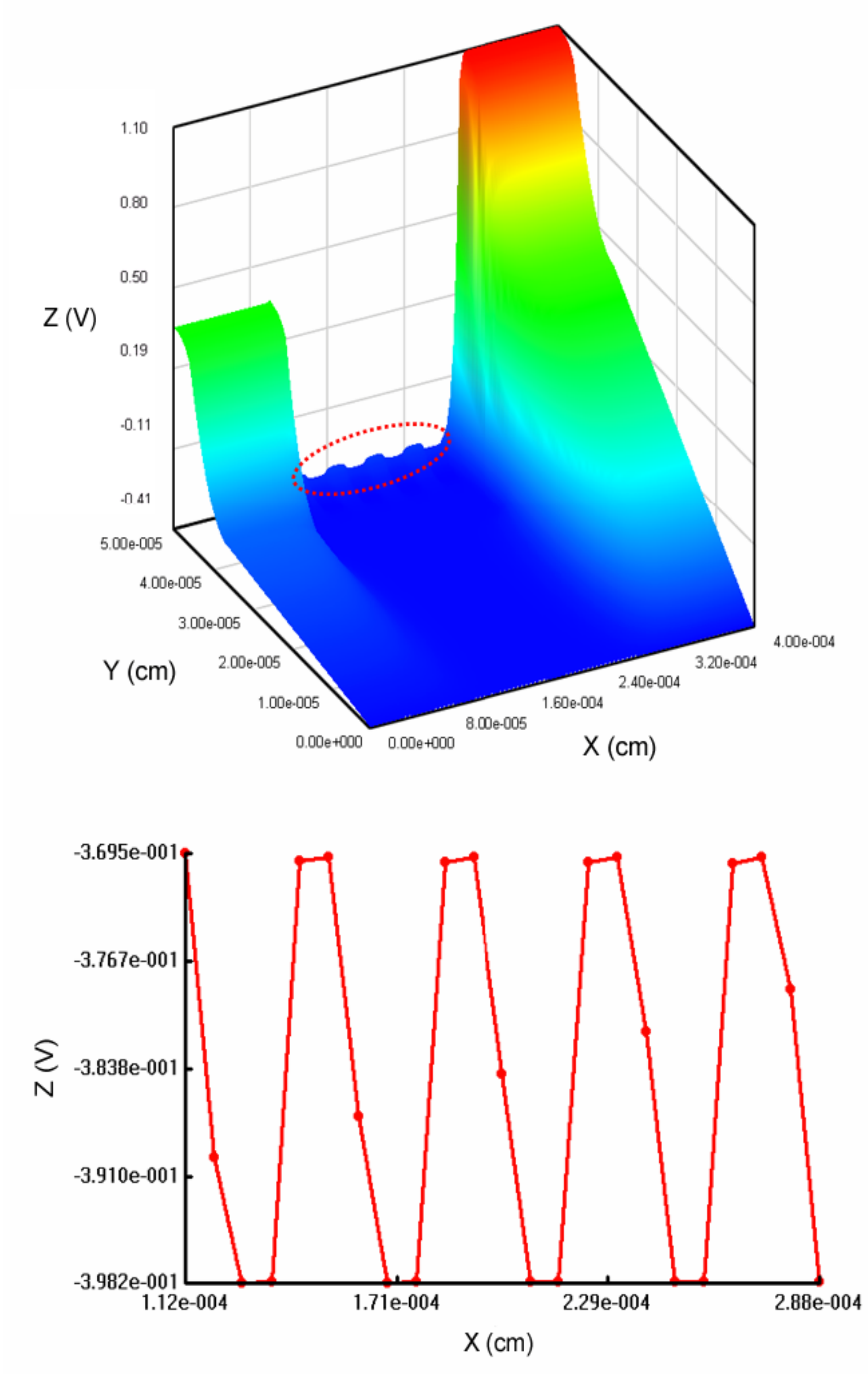


Figure 4.8: The upper figure is the simulated potential of the poly-Si TFT with $V_D = V_G = 0.5\ V$. The lower one is a cross-sectional view of the circled region in the upper figure.

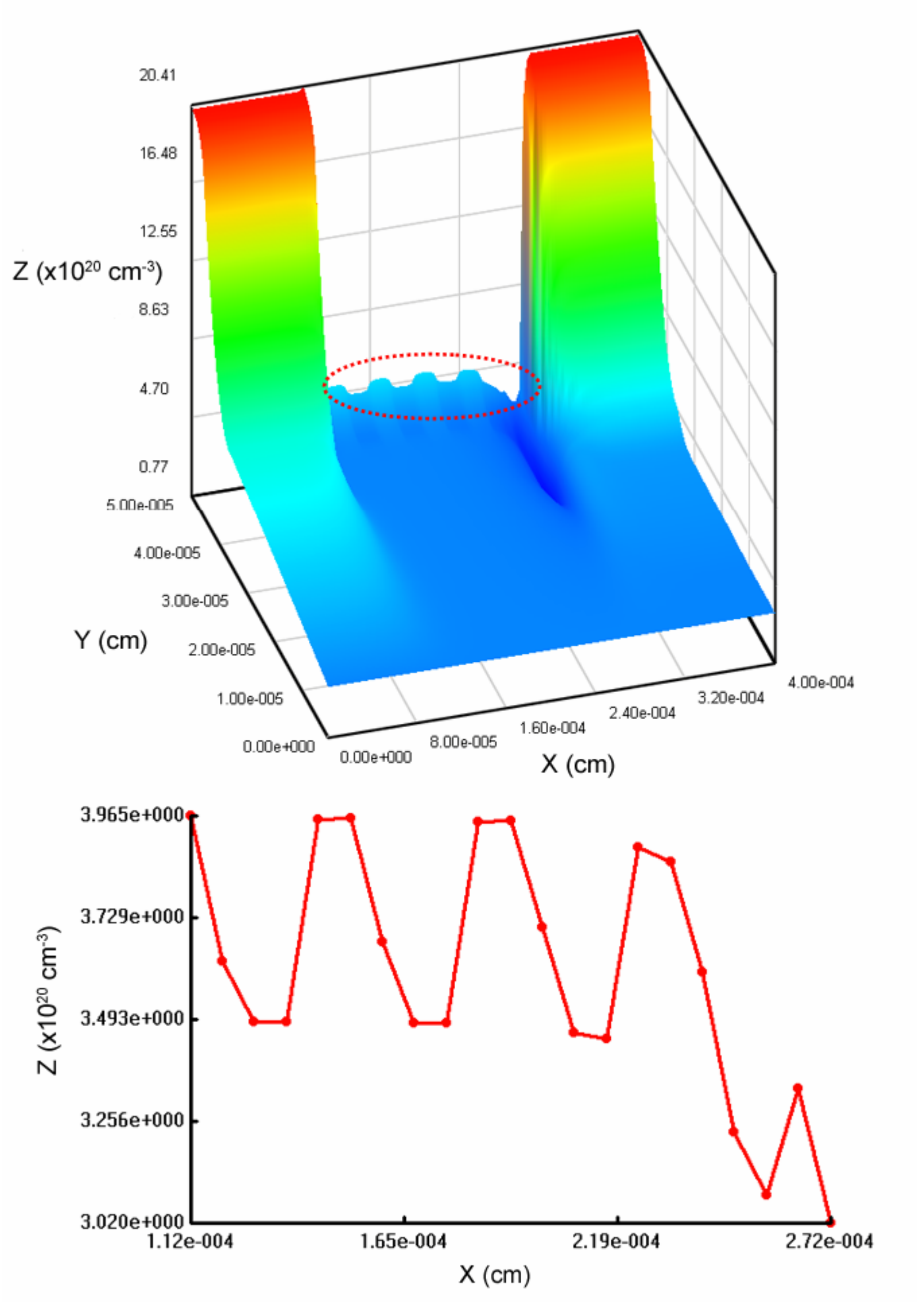


Figure 4.9: The upper figure is the simulated electron density of the poly-Si TFT with $V_D = V_G = 0.5\ V$. The lower one is a cross-sectional view of the circled region in the upper figure.

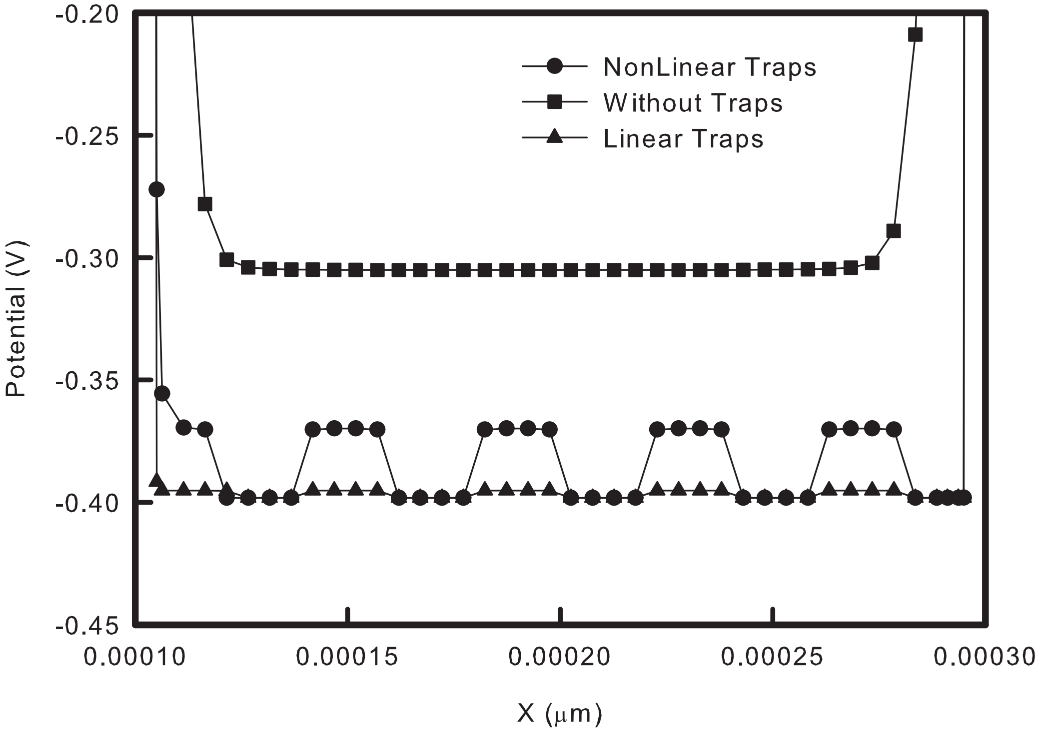


Figure 4.10: Comparison of the computed electrostatic potential for the 2D DD simulation with three different trap models of grain boundary, where $V_D = V_G = 0.5\,V$.

4.5 The Mixed-Mode Solution Procedure

Currently, well-established SPICE model of GAA poly-Si TFTs is not available for circuit simulation. Therefore, we develop a circuit-device coupled mixed mode simulation technique to explore the circuit behavior. The mixed-mode methods contains devices and circuits simulation. A flow chart for decoupling method is shown in Fig. 4.11. When t = 0 s, firstly it solves the Poisson and DD equatios of three devices. If it is convergent, next step will solve coupling the three devices and five nodes circuit equations. It totally contains eight circuit equations. If not convergent, it will restart to solve from device simulation. When all the mixed-mode equations are finished, it will solve the next time until finishing all the time simulation. Here, the increment time is Δt.

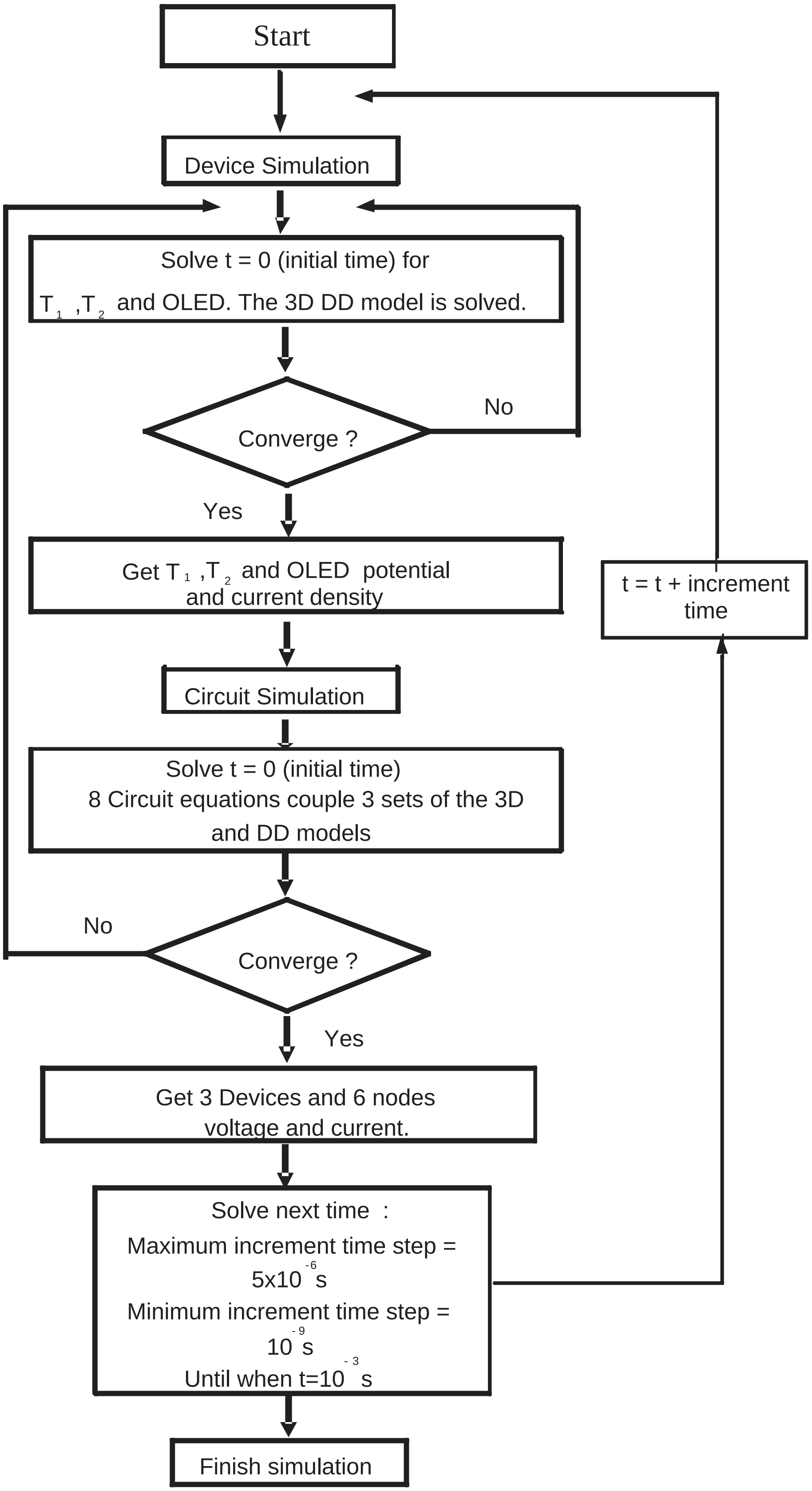


Figure 4.11: A flow chart of the mixed-mode simulation technique, where the increment time is the time step.

Chapter 5

Characteristic Simulation of Poly-Si TFTs with Different Gate Structures

Based on the simulation methods discussed in Chap. 3, we will clearly discuss the effects of different gate structure on the poly-Si TFTs from the long channel to short one.

5.1 Simulation and Calibration of 5 μm Poly-Si TFTs

A. Bolognesi et al. provide the methods to extract trap parameters [62]. The free charges which are trapped at the GB and this result deeply affecting the subthreshold slope. In particular, if we increase the acceptor-liked trap surface concentration, the subthreshold slope decreases. In the beginning, we do not know the acceptor trap level inside the forbidden band and must analyze its effects varying both the concentration and the barrier height (E_B). First, we guess a barrier height equal to 0.15 eV and explore the characteristics for several trap concentrations, shown in Fig. 5.1(a). We notice that the effect of the traps appears only on the subthreshold region. Second, we choose a trap concentration of 3E13 cm^{-2} and analyze the dependence of the characteristic on the barrier height, shown in Fig. 5.1(b). Base on the method of trying error, we conclude that a 3E13 cm^{-2} acceptor-liked trap surface concentration (N_{TA}) and a 0.15 eV barrier height (E_B) of trap.

With such parameters of the trap, we obtain an almost perfect agreement with the experimental data. Here, we show the plots of electrostatic potential and electron density along source to drain direction, and explore the 1D electron density along Z direction. They are shown in Figs. 5.2 and 5.3. In the numerical studies, the simulated oxide thickness (T$_{ox}$) is 250 nm channel length (L$_G$) are 5 μm channel thickness is equal to 0.5 μm and the grain size is about 0.3 μm. In the n-type TFTs, the channel is boron doped and its concentration is equal to 1E19 cm^{-3}. The source and drain is phosphor doped which concentration is equal to 5E17 cm^{-3}. The concentration of LDD is 5E18 cm^{-3}. Fig. 5.4 shows comparison of model and measured characteristics of the various devices.

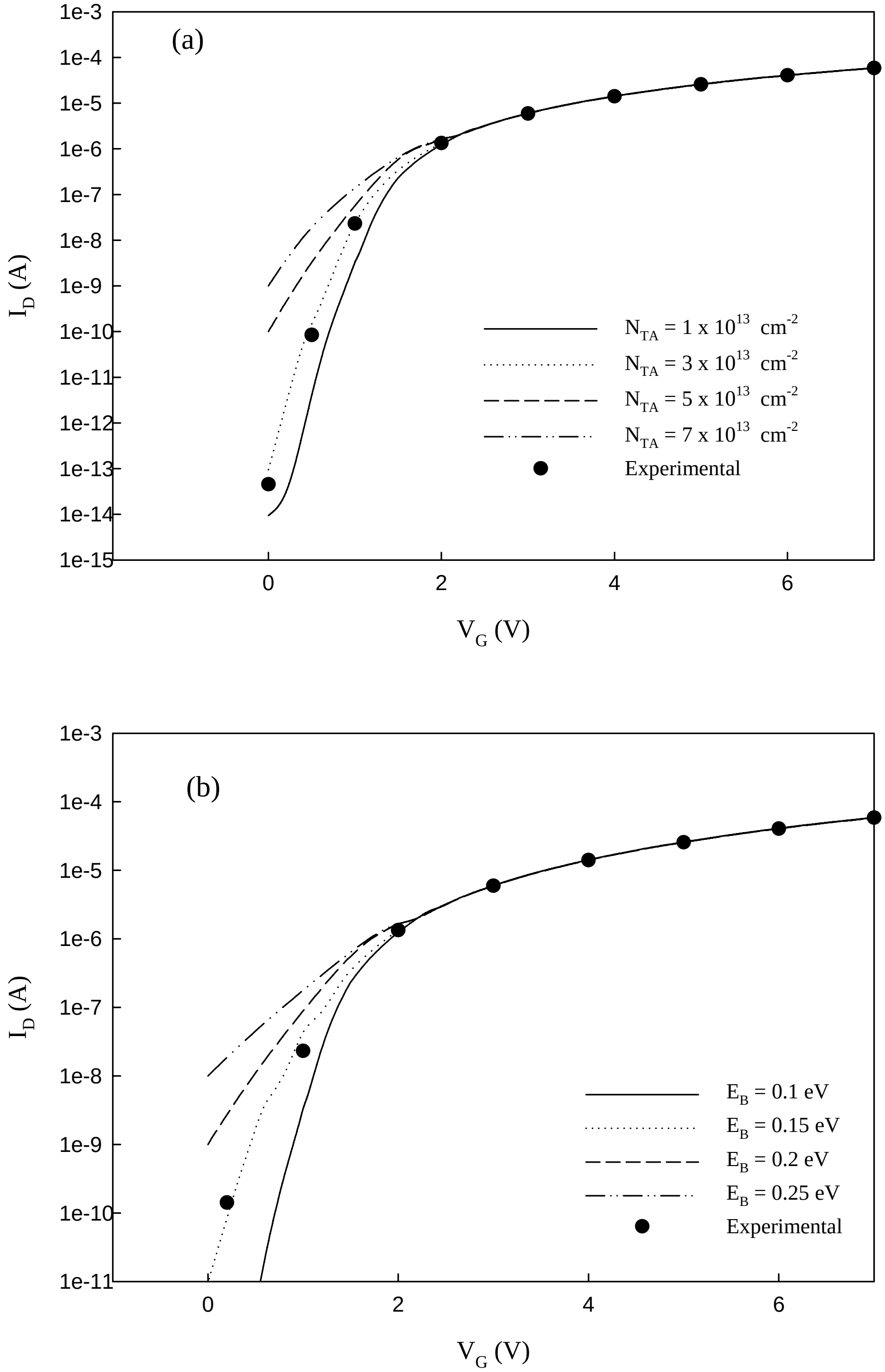


Figure 5.1: (a) Characteristics obtained for the explored device with V_D = 10.1 V, where different concentrations of the trap are investigated. The barrier height is 0.15 eV, and (b) Characteristics obtained for device with V_D = 10.1 V, where different barrier heights of the trap are investigated. The N_{TA} is 3E13 cm^{-2}.

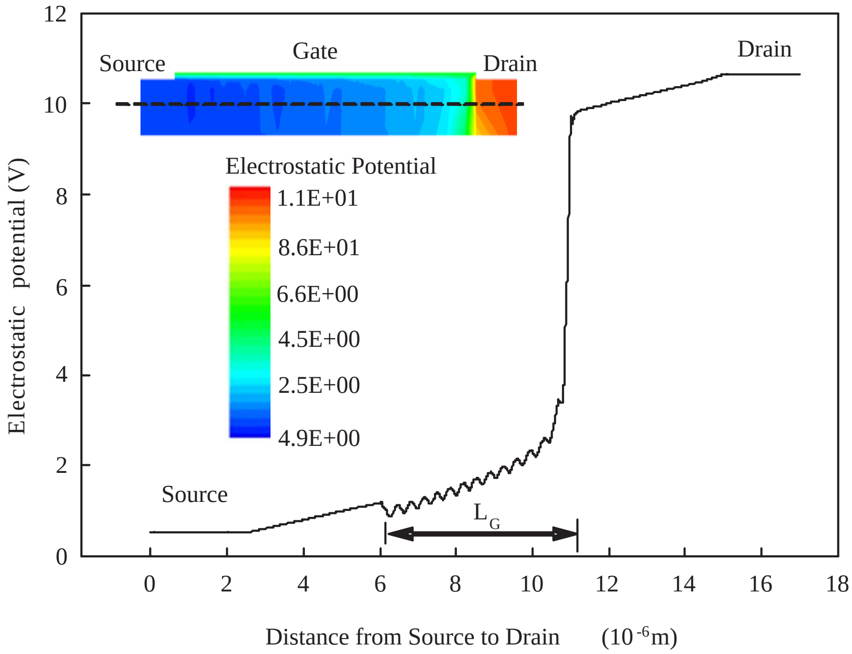


Figure 5.2: The electrostatic potential along the source to the drain is obtained for V_D = 10.1 V and V_G = 5 V. The depth is 25 nm from the interface.

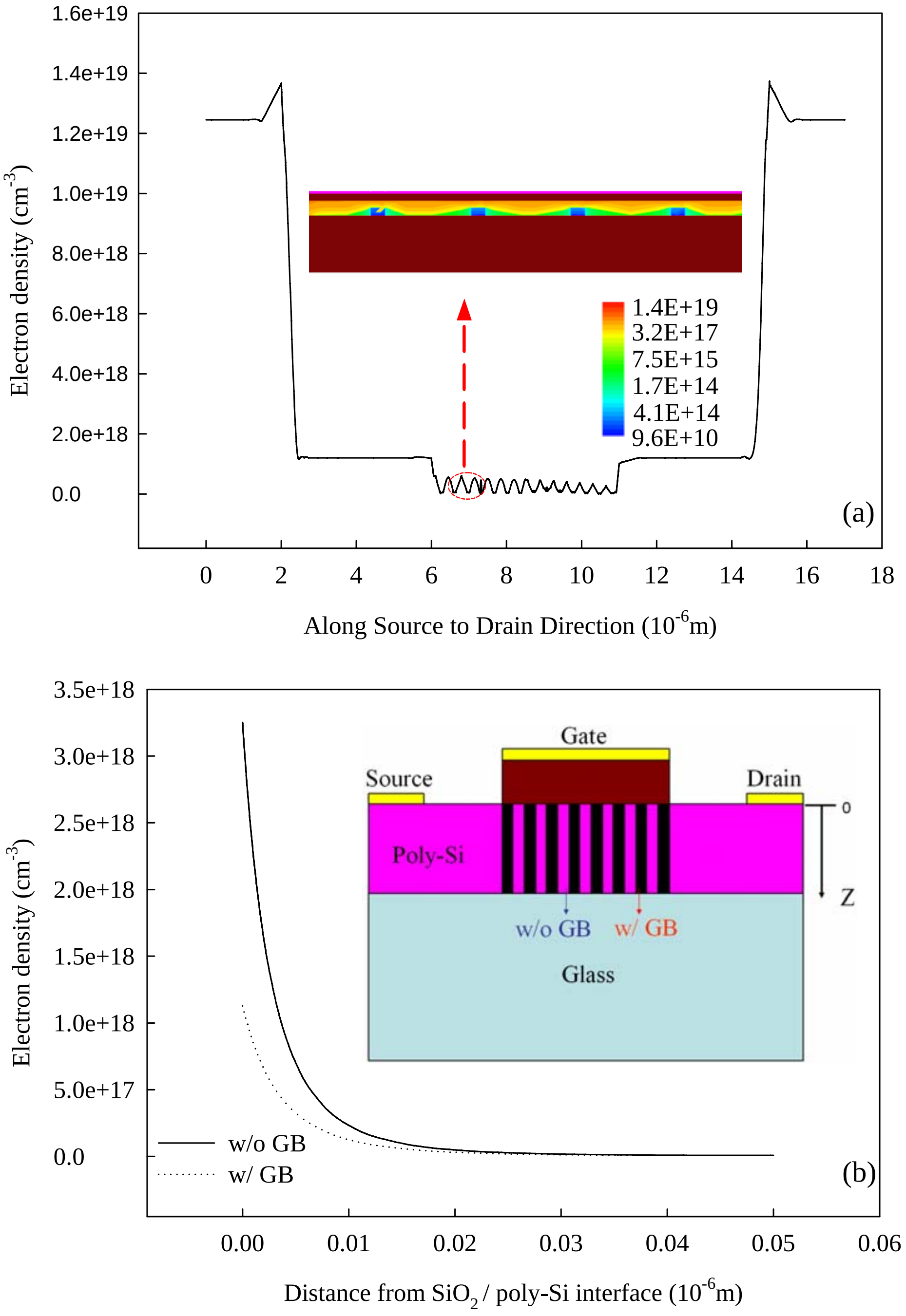


Figure 5.3: (a) The electron density along the source to the drain is obtained for V_D = 10.1 V and V_G = 5 V. The depth is 25 nm from the interface (b) and the plot of electron density w/ and w/o GB along the Z direction.

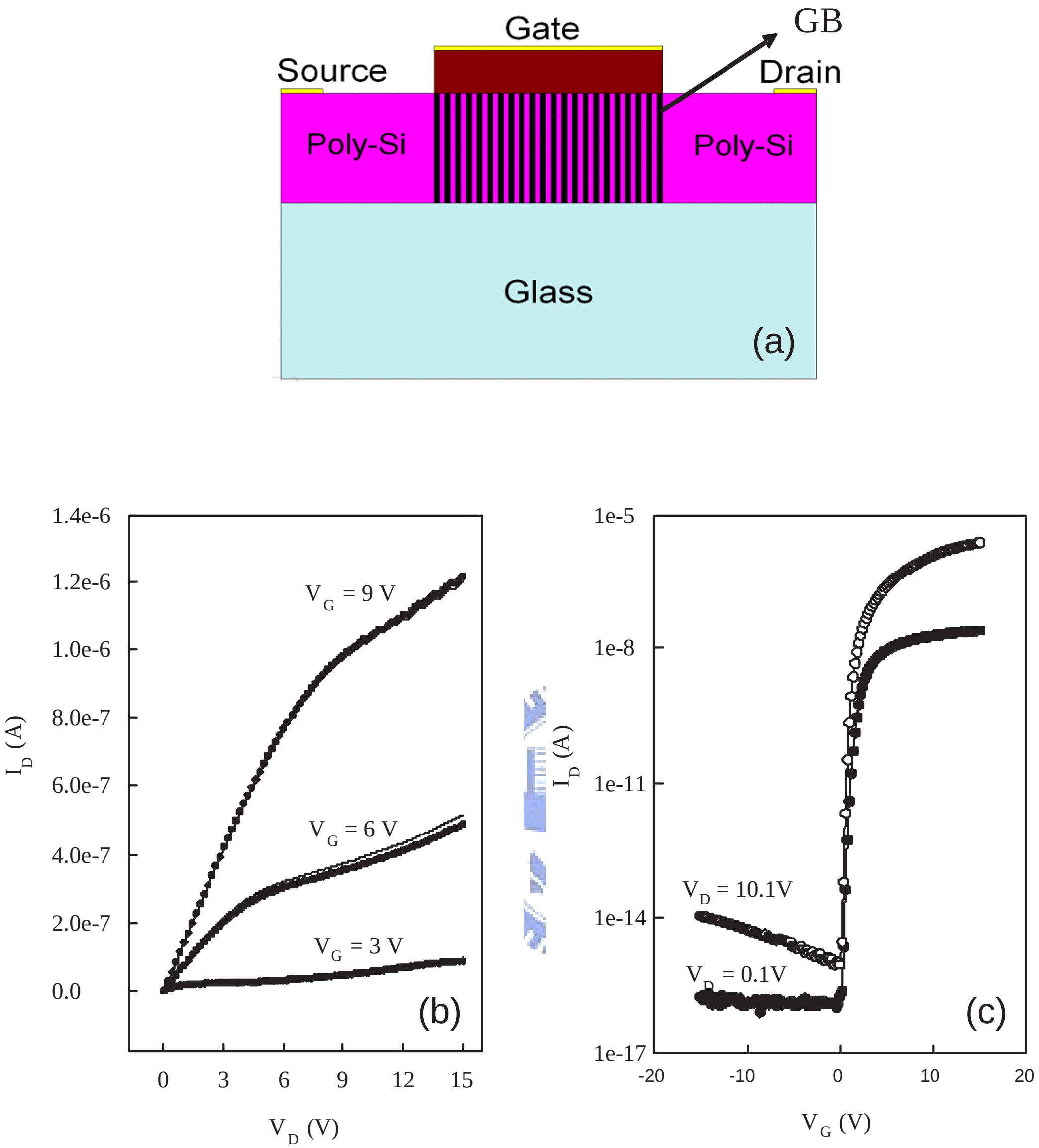


Figure 5.4: (a) The conventional long-channel SG poly-Si TFT, (b) the comparison of I_D-V_D and (c) I_D-V_G between measured (symbol curve) and simulated (solid curve) for n-type poly-Si TFT with W = 5 μm and L = 5 μm.

5.2 Simulation of 300 nm Poly-Si TFTs with Different Gate Structures

Two different TFT devices with 300 nm SG and GAA TFTs are investigated in this section. GAA poly-Si TFT structure has been shown in Fig. 5.5(a). The used parameters of devices are shown in Table 5.1 [87]. Because the size of GB used is 300 nm, only one GB was assumed to exist in the channel and is perpendicular to the channel length. The position of GB was assumed to occur at three different locations, as depicted in Fig. 5.5(b). To explore the potential advantages of GAA poly-Si TFTs, we compare our calculated results with the data of SG poly-Si TFTs. The threshold voltage for these two devices is adjusted with varying channel doping and gate material. The extracted barrier height (E_B) and the acceptor-liked trap surface density (N_{TA}) at the grain boundary were used for GAA and SG structures. The doping concentration (N_A) at the channel is calculated with [86]:

$$E_B = \frac{q^2 N_A}{8\varepsilon}(\frac{N_{TA}}{N_A})^2, \tag{5.1}$$

where ε is the semiconductor permittivity. When E_B is fixed, N_A is proportional to $(N_{TA})^2$. We decrease the concentration of the doping profile and increase the gate work function.

Table 5.1: The used parameters in the 3D device simulation of the 300 nm devices.

Device Parameter	**Setting value**	**Device Parameter**	**Setting value**
Gate length	300 nm	**GB**	15 nm
channel thickness	50 nm	**Work function**	4.55 eV
Channel width	300 nm	**Channel doping**	1E16
Oxide thickness	15 nm	**LDD doping**	2.5E18
LDD length	200 nm	**S/D doping**	2.5E19

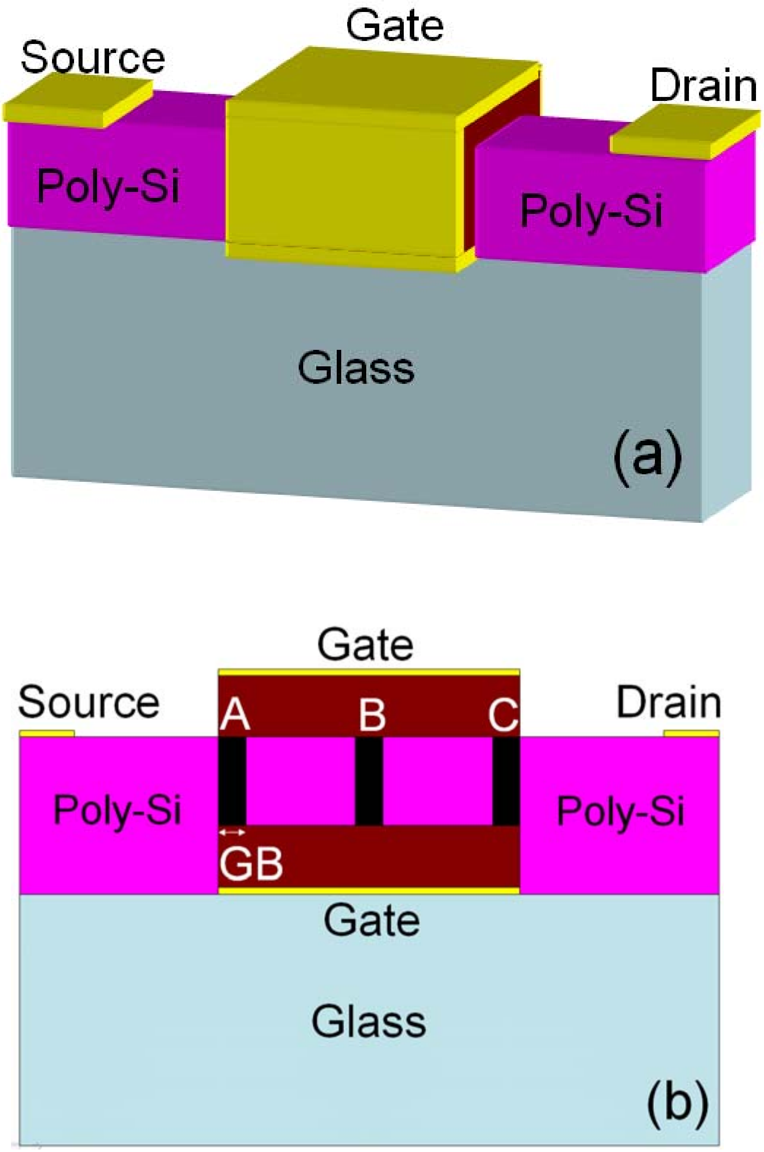


Figure 5.5: (a) A schematic plot of the GAA poly-Si TFT. The device is with a square-shaped-surrounding gate. (b) Single grain boundary occurs at the position of A, B, and C.

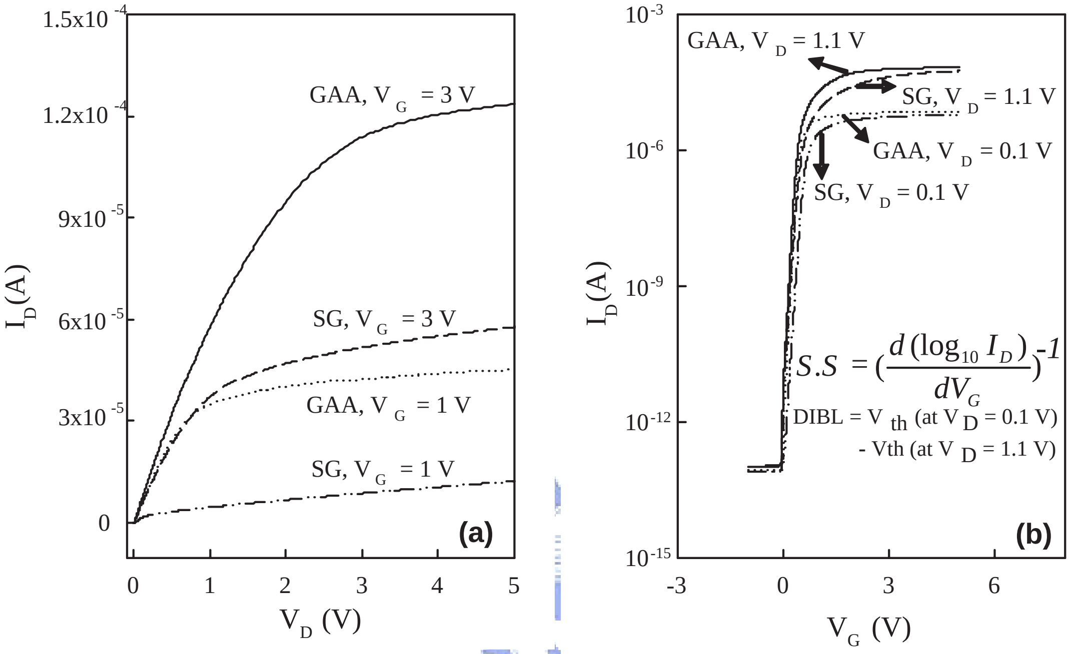


Figure 5.6: The new simulated 300 nm poly-Si TFTs (a) I_D-V_D and (b) I_D-V_G characteristics in GAA and SG without the grain boundary.

Table 5.2: Effects of GB position on the device characteristics of the 300 nm GAA poly-Si TFT, where the size of single GB is 15 nm. I$_{on}$ and I$_{off}$ are the on-state current and off-state current.

Symbol	$\triangle\overline{V}_{th}$	**I$_{on}$/I$_{off}$**	**DIBL(V)**	**S.S(mv/dec)**
w/o GB	–	6e7	0.02	91
GB at A	4.56	5.7e7	0.042	105
GB at B	3.96	5.9e7	0.19	101
GB at C	5.45	5.6e7	0.24	107

Table 5.3: Effects of GB position on the device characteristics of the 300 nm SG poly-Si TFT, where the size of single GB is 15 nm.

Symbol	$\triangle\overline{V}_{th}$	**I$_{on}$/I$_{off}$**	**DIBL(V)**	**S.S(mv/dec)**
w/o GB	–	2e7	0.04	101
GB at A	10.25	1.2e7	0.08	139
GB at B	7.02	1e7	0.06	134
GB at C	15.31	1.3e7	0.09	144

According to the definition in the chapter 2, we arrange the results in Tables 5.2 and 5.3.

Consequently, a reasonable of V_{th} = 0.62 V is obtained for both structures. Characteristics of I_D-V_D and I_D-V_G for devices without GB are firstly shown in Fig. 5.6. The off-state current, shown in Fig. 5.6(b), is suppressed with the 300 nm GAA poly-Si TFT by using a LDD doping profile close to the SG. The on-state current of the 300 nm GAA poly-Si TFT is about 3-times larger than that of the SG, so we expect that the 300 nm GAA poly-Si TFT can have a larger driving capability and yield a higher luminescence output. Effect of single GB on parameters of the short channel effect for GAA and SG devices are then calculated and compared in Tables. 5.2 and 5.3, respectively. $\triangle\overline{V}_{th}$ is the normalized difference of threshold voltages for device with and without GB by the threshold voltage of the device without GB. Comparison shows that GAA poly-Si TFT exhibits good device characteristics compared with the results of SG one. It is observed that the worst case of V_{th} variation on GAA could be reduced from 15% to 5.5% when GAA structure is considered.

$\triangle\overline{V}_{th}$ versus the position of single GB, calculated with respect to different size of single GB, is shown in Fig. 5.7. When the drain and source sides have GB, the variation of V_{th} becomes significant. $\triangle\overline{V}_{th}$ can be reduced when the size of GB is decreased from 15 nm to 3 nm. Effect of GB is independent of the position when the size is relatively small compared with the channel length.

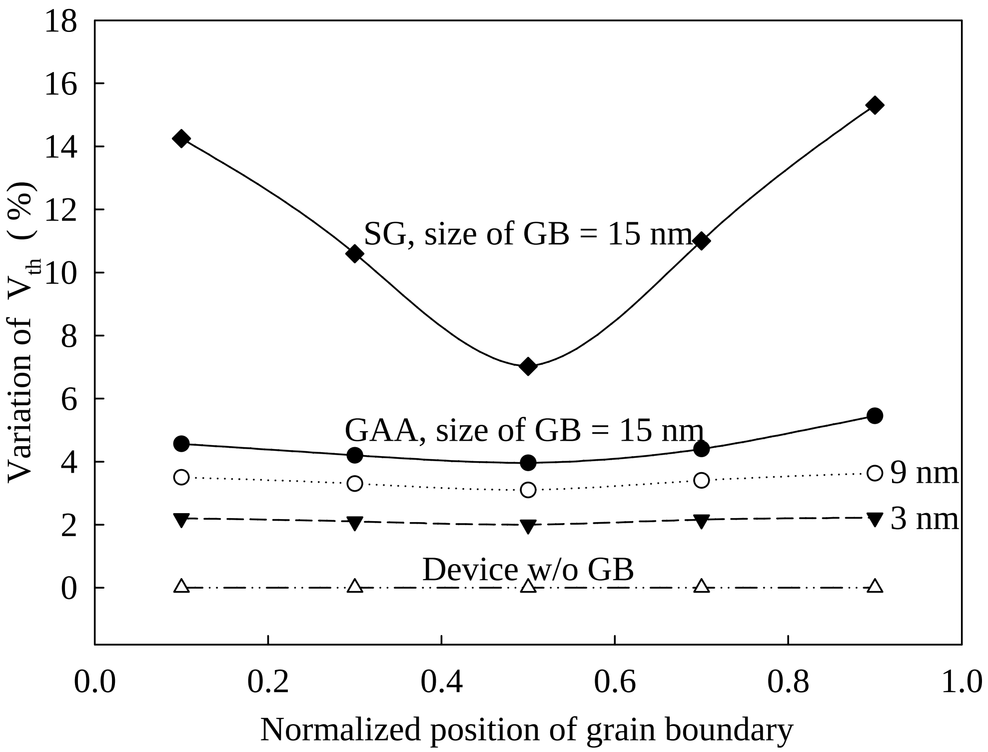


Figure 5.7: The effect of GB position on V_{th} variation of the 300 nm GAA poly-Si TFTs. Suppression of variation is observed when the size of GB is reduced from 15 nm to 0 nm (i.e., device w/o GB).

5.3 Simulation of 90 nm Poly-Si TFTs including Quantum Mechanical Effects

We explore the effect of grain boundary (GB) position and size on electrical characteristics in 90 nm poly-Si thin film transistors (Poly-Si TFTs). To estimate the effect of GB, three-dimensional (3D) density-gradient- based drift-diffusion model is self-consistently solved with grain trap model for the square-shaped surrounding-gate (i.e., gate-all-around, GAA) poly-Si TFTs. The trap concentration and trap level are calibrated and extracted from the fabricated samples. Compared with device without GB, quantum mechanical simulation shows that the 90 nm GAA poly-Si exhibits significant threshold voltage variation (7.4%) when single GB locates at the drain side of device channel due to a largest shift of total inversion charge. The variation could be suppressed when the size of single GB is reduced. For the same threshold voltage, the 90 nm GAA poly-Si TFT suffers more serious performance degradation than that of 300 nm device. It is mainly resulted from the short channel effect and quantum-confined GB trap near the drain side.

According to a scaling rule, the adopted parameters in our 3D simulation are shown in Tab. 5.4. We explore the intrinsic characteristics of the 90 nm GAA poly-Si TFT with and without GB appearing at C (i.e., the drain side) by using the quantum mechanical (i.e., the density-gradient based drift-diffusion model) and the classical transport (drift-diffusion model) simulations, shown in Fig. 5.8. The electron density distributions along the directions of YY' and ZZ' are compared. Along different cutting lines, it is found that for the device without GB, the classical simulated electron density is higher than that of quantum mechanical result due to no dangling bonds and quantum confinement existing in channel region. For device with GB at C, both the classical and quantum mechanical simulations show the electron densities are reduced due to weakened gate controllability. It mainly results from a higher variation of the barrier height and then an enlarged effective oxide thickness. We note that the effect of single GB is significant in quantum mechanical simulation (about 23% reduction), compared with the classical result (14% reduction). The reduction is the averaged relative error of the electron density with GB and without GB. If the size of GB increases, the effect of GB will result in larger reduction. The quantum mechanical computed surface electrostatic potentials, shown in Fig. 5.9, are plotted along the channel direction from the source to drain sides with three different positions of GB. The size of GB is firstly fixed at the 4 nm. It is found that potential distributions are significantly affected by the position of GB compared with the result of device without GB. When GB appearing at C, a large variation of the barrier height (0.3 eV) occurs, shown in Fig. 5.9, which is substantially larger than that (0.2 eV) of classical simulation (not shown here) due to a quantum entanglement with grain trap concentration. If the position of GB could be controlled and locating near the neighborhood of B, the device has a lowest variation of the

Table 5.4: The used parameters in the 3D device simulation of the 90 nm devices.

Device Parameter	**Setting value**	**Device Parameter**	**Setting value**
Gate length	90 nm	**GB**	4 nm
channel thickness	10 nm	**Work function**	4.55 eV
Channel width	90 nm	**Channel doping**	3.3e16
Oxide thickness	3 nm	**S/D doping**	8.25e19

barrier height (it is about 0.04 eV) which means that the device has stable characteristics among the explored device with different positions of GB.

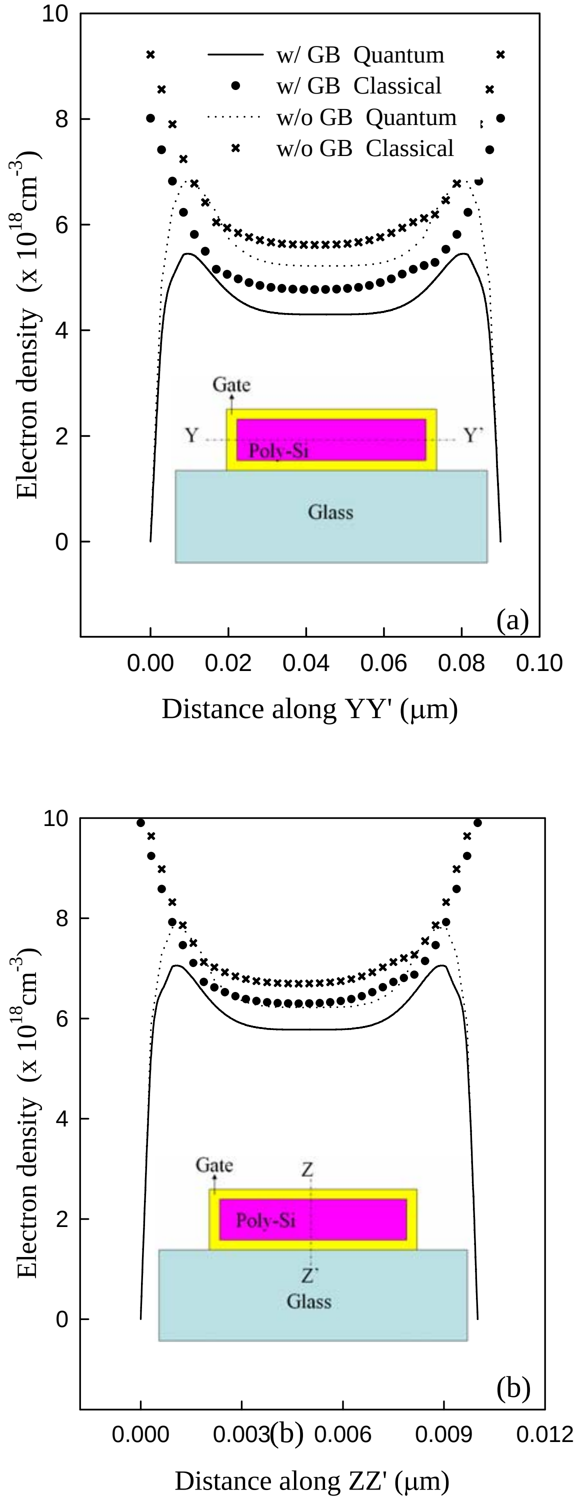


Figure 5.8: Along the (a) YY’ and (b) ZZ’ direction of the inset figures, the plots are the electron density without (w/o) and with (w/) GB when using quantum mechanical and classical models, where the gate voltage $V_G = 1.1$ V.

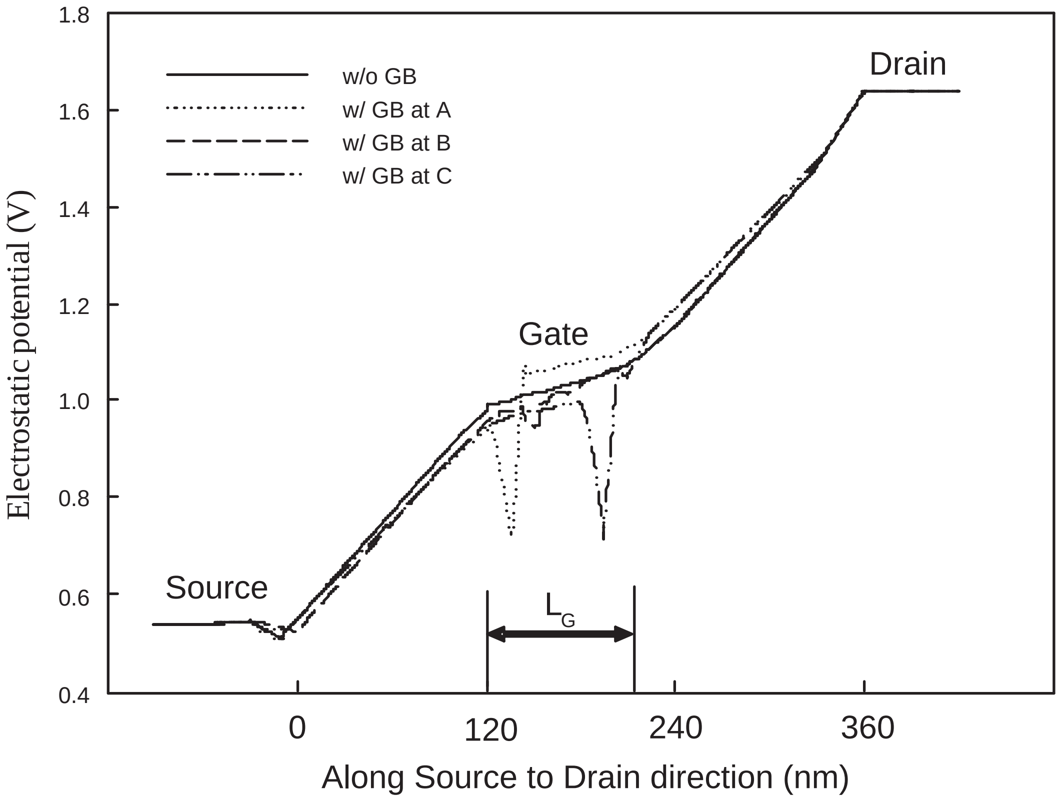


Figure 5.9: The simulated electrostatic potential along the 90 nm device channel with respect to three different positions of GB. The case C (the grain boundary locates at the drain side) has a large peak and baffles the electron current.

Table 5.5: The calculated variation of the total inversion charge of the 90 nm poly-Si TFT, where V$_G$ = 1.1 V and the size of GB = 4 nm. The A, B, and C are the same as shown in Fig. 5.5(b).

	GB at A	**GB at B**	**GB at C**
ΔQ_{inv}	5.4%	3.3%	6.3%

The total inversion layer charge Q$_{inv}$ shown below is quantitatively calculated and compared among three positions of GB:

$$Q_{inv} = \int\int\int q \cdot n(x, y, z)dxdydz, \tag{5.2}$$

where the *n* is the quantum mechanical computed electron density per unit volume. Comparison, shown in Tab. 5.5, is computed by estimating the variation of Q$_{inv}$:

$$\Delta Q_{inv} = \frac{Q_{inv}|_{w/o} - Q_{inv}|_{w/}}{Q_{inv}|_{w/o}}. \tag{5.3}$$

We find that the GB near the drain side has a large variation of the inversion charge under the on-state condition. The calculation confirms the argument discussed that GB locating at C significantly degrades the device performance including the degradation of the transport current and serious short channel effect. A comparison of the characteristics of I$_D$-V$_D$ for the explored device under V$_G$ = 2 V are simulated when the size of GB is equal to the 4 v, shown in Fig. 5.10. It shows that the device with GB at C exhibits a largest reduction of the magnitude of the drain current. More than 2.5 times reduction is observed for the device without GB and with GB at C. The further reduction of the drain current appears for the device with GB and A and C, compared with the device with GB at B and without GB, which confirms the examination in Tab. 5.5.

Effect of the GB's size and position on the variation of threshold voltage of the 90 nm GAA poly-Si TFT is explored, shown in Fig. 5.11 The open-triangular shows the device without GB in the channel. When the drain and source sides have GB, a large variation of the threshold voltage is introduced. For the device with GB locating at B, the variation of the threshold voltage is less dependent on the grain trap. The variation of the threshold voltage could be suppressed when the size of GB is reduced from the 6 nm to 2 nm. Effect of GB is independent to the position of GB when the size of GB is relatively small enough. With an increasing of the size of GB, the variation of the threshold increases and then the current decreases.

We further explore the short channel effect including the drain induced barrier lowering (DIBL), the subthreshold swing (S.S.), and the ratio of the on-state and the off-state currents between the 90 nm and 300 nm GAA poly-Si TFTs. The DIBL and the S.S. are computed by:

$$S.S. = \frac{\partial(log_{10} I_D)}{\partial V_G}|_{V_D=0.25V}, \tag{5.4}$$

$$DIBL = V_{th}|_{V_D=0.25V} - V_{th}|_{V_D=1.1V}. \tag{5.5}$$

Compared with the 300 nm GAA poly-Si TFT, the 90 nm device shows serious performance degradation that introduced from the effects of GB and quantum confinement, shown in Tabs. 5.7 and 5.6.

In this work, we have studied the dependence of electrical characteristics on the position and size of single GB in the 90 nm poly-Si TFT. The effect of GB in sub-100 nm square-shaped surrounding-gate poly-Si TFTs have been studied by solving the 3D quantum correction transport model. The position and size of single GB significantly affect the intrinsic performance of the 90 nm GAA poly-Si TFT. The GAA poly-Si TFTs suffer serious short channel effect and performance degradation when the device channel is scaled into the sub-100 nm. The device's GB locating at the drain side will result in large characteristic variation. To reduce the short channel effect, the size of GB should be accordingly reduced with the reduction of channel length in the nanoscale GAA poly-Si TFTs era. We are currently exploring the effect of GB in TFT-LCD display using ultra-small poly-Si TFTs.

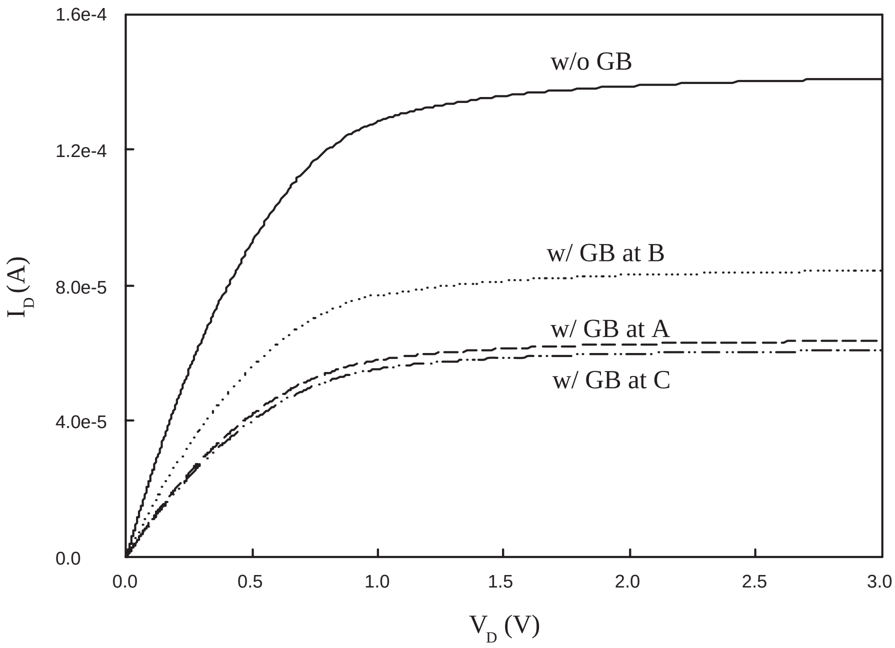


Figure 5.10: A comparison of the computed I_D-V_D for the device with different positions of GB, where the size of GB = 4 nm and V_G= 2 V. More than 2.5 times difference is observed between the 90 nm poly-Si TFT w/o GB and the device w/ GB at C.

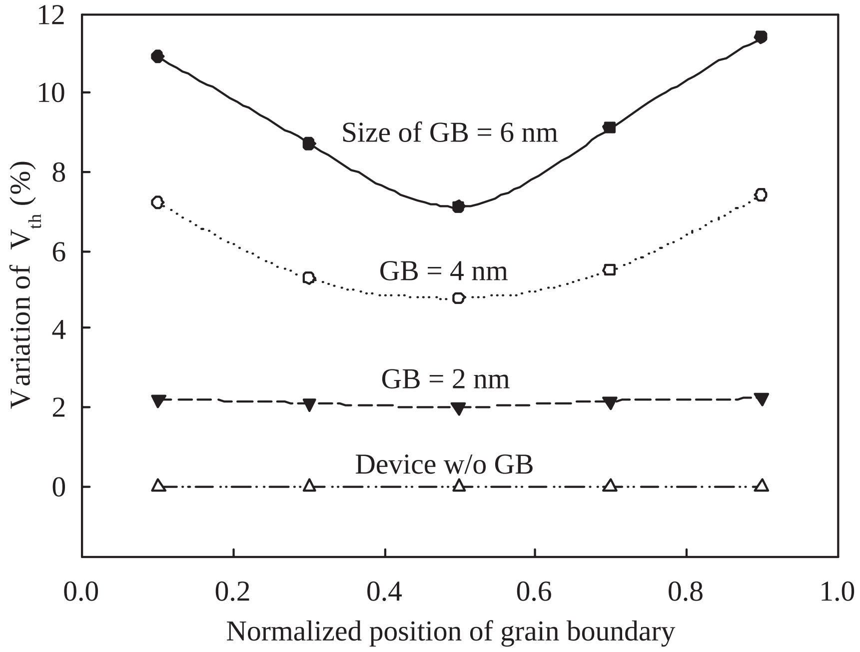


Figure 5.11: The effect of the position of GB on the variation of threshold voltage for the 90 nm GAA poly-Si TFT. The open-triangular is the device without GB in the channel. The variation is suppressed when the size of GB is reduced from the 6 nm to 2 nm.

Table 5.6: The computed short channel effect of the 300 nm GAA poly-Si with different positions of GB.

Symbol	$\triangle\overline{V}_{th}$	$\mathbf{I}_{on}/\mathbf{I}_{off}$	**DIBL(V)**	**S.S(mv/dec)**
w/o GB	–	6e7	0.02	91
GB at A	4.56	5.7e7	0.042	105
GB at B	3.96	5.9e7	0.19	101
GB at C	5.45	5.6e7	0.24	107

Table 5.7: The computed short channel effect of the 90 nm GAA poly-Si with different positions of GB.

Symbol	$\triangle\overline{V}_{th}$	$\mathbf{I}_{on}/\mathbf{I}_{off}$	**DIBL(V)**	**S.S(mv/dec)**
w/o GB	–	9e7	0.04	101
GB at A	7.2	6.4e7	0.07	120
GB at B	4.75	6.8e7	0.06	113
GB at C	7.4	6.1e7	0.09	123

Chapter 6

Performance of Poly-Si TFT Circuit Drivers

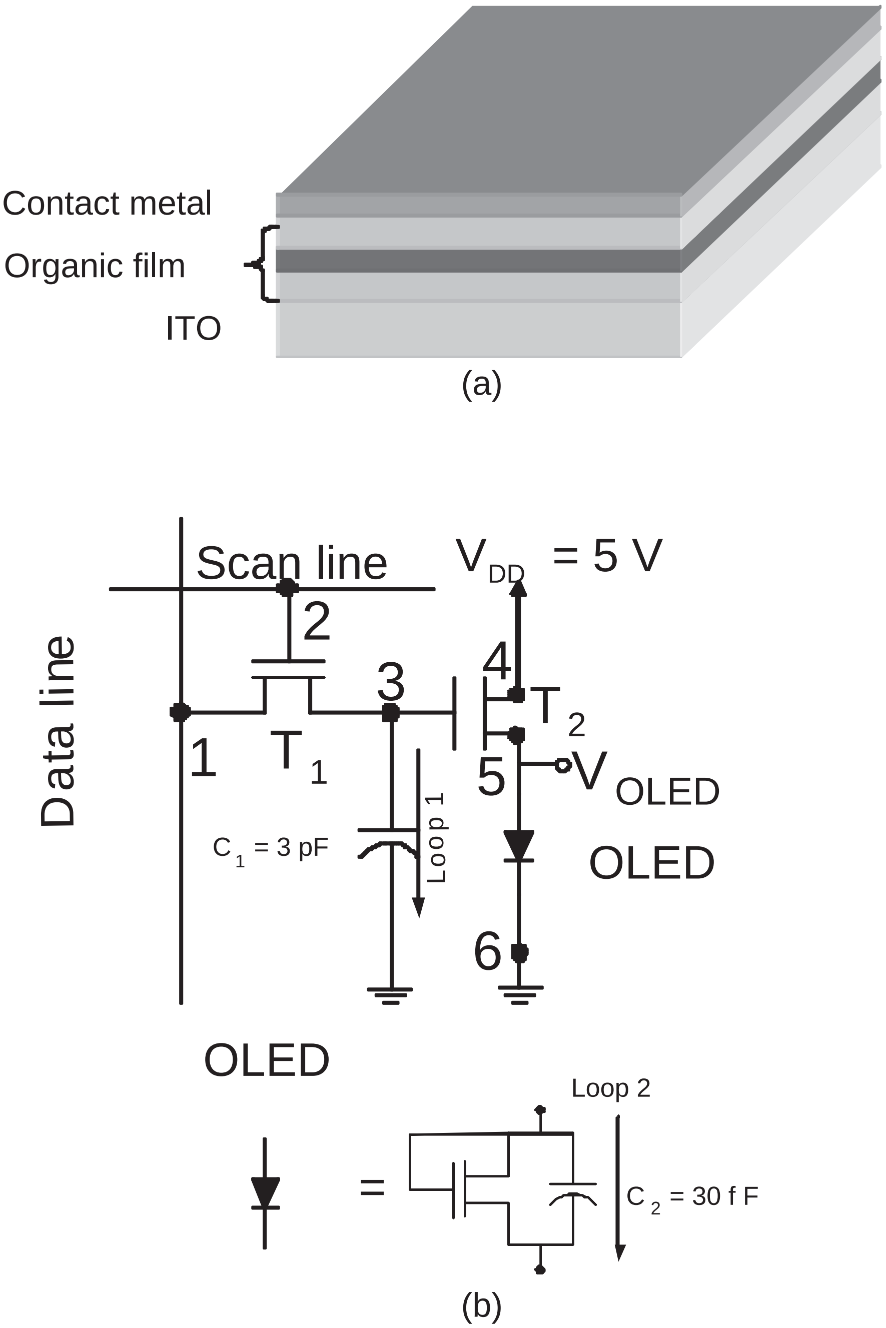
The chapter investigated the methods for the driving circuit and covers the organic light emitting diode(OLED). OLED display has several advantages over TFT-LCDs and penetrate into various applications. Because of the effects of GB, it is hard to simulate the active-matrix circuit. We develop the mixed-mode method.

In the mixed-mode simulation, the solution of the basic transport equations for the semiconductor devices is directly embedded into the solution procedure for the circuit equations. Compact modelling is thus avoided and much higher accuracy is obtained.

6.1 The Explored Poly-Si TFT Circuit

Currently, well-established SPICE model of GAA poly-Si TFTs is not available for circuit simulation. We develop a circuit-device coupled mixed mode simulation technique to explore the circuit behavior. The mixed mode methods contains devices and circuits simulation.

We also employ a numerical simulation to explore the OLED devices. The numerical simulation of the continuity and Poisson equations has been carefully extended to treat the interfaces of multi-layer organic structure.The experimental structure is shown in Fig. 6.1 which implies that a simulation is necessary. One OLED device is equal to one poly-Si TFT coupling one capacitance. From the results shown in the figures 6.2-6.3 exhibit the comparison results for our model with the measured OLED data with red, green, and blue color, respectively. Our simulation presents good accuracy when describing the OLED physical characteristics in both the cut-in and the on-state regions. We also compare our OLED simulation with others [26], shown in Fig. 6.3. This OLED device is used in my thesis. After the discussion of OLED, we show the simulation of our circuit in Fig. 6.1. The mixed mode source codes is listed in appendix B. A flow chart of OLED's extracting method is shown in Fig. 6.4, and the extracting parameters of OLED are shown in Tab. 6.1. In the beginning, the work function and doping profile of channel should be tuned. Calibrating with measurement data, we can get a suitable value of threshold voltage. After this step, We must tune the value of capacitor because it decides on-state current. If the target of threshold voltage and on-state current are correct, the extracting steps will finish.



(a)

(b)

Figure 6.1: (a) A diagram of the multi-layers OLED structure (b) and 2T1C active-matrix driving circuit and the OLED compact circuit.

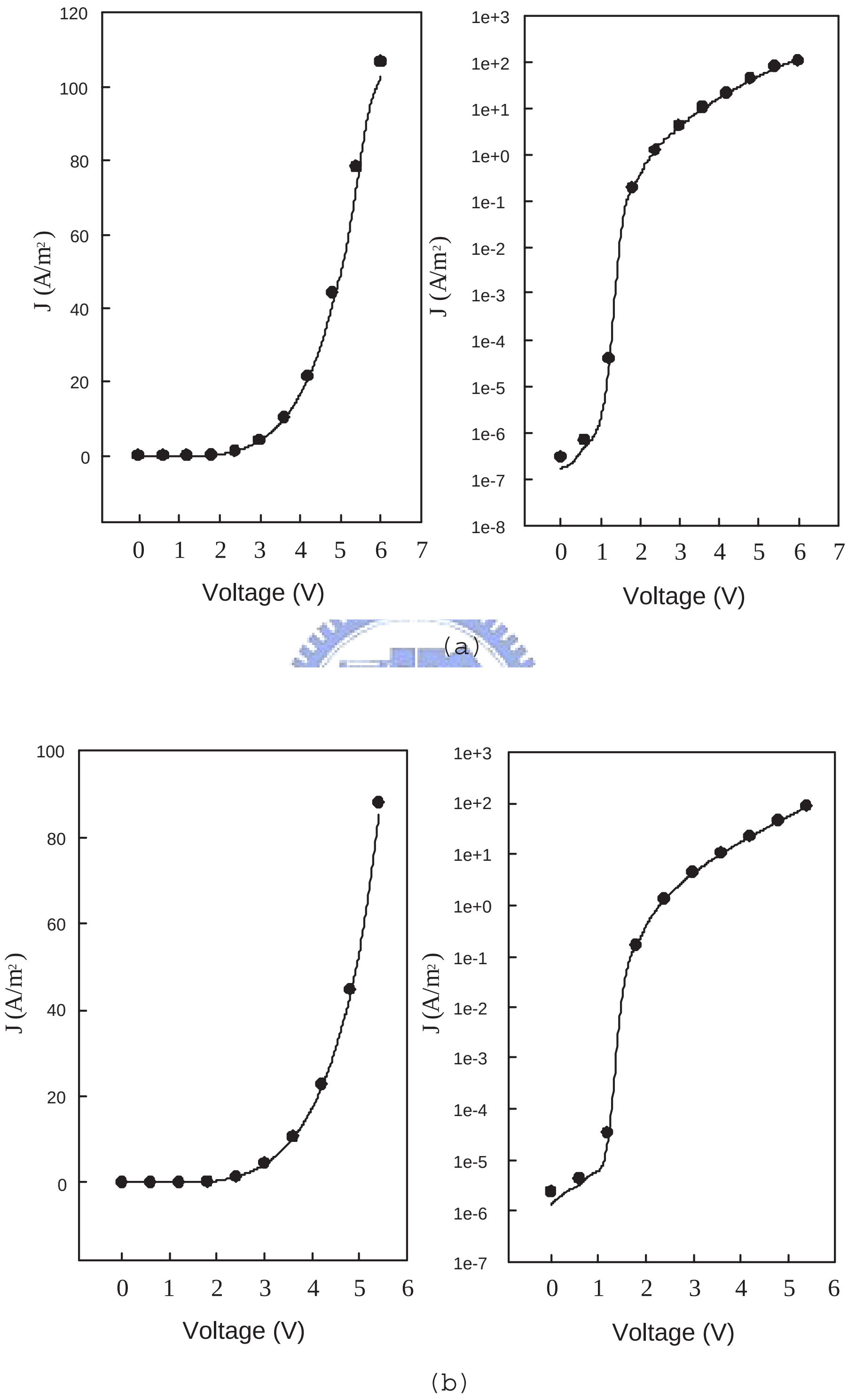
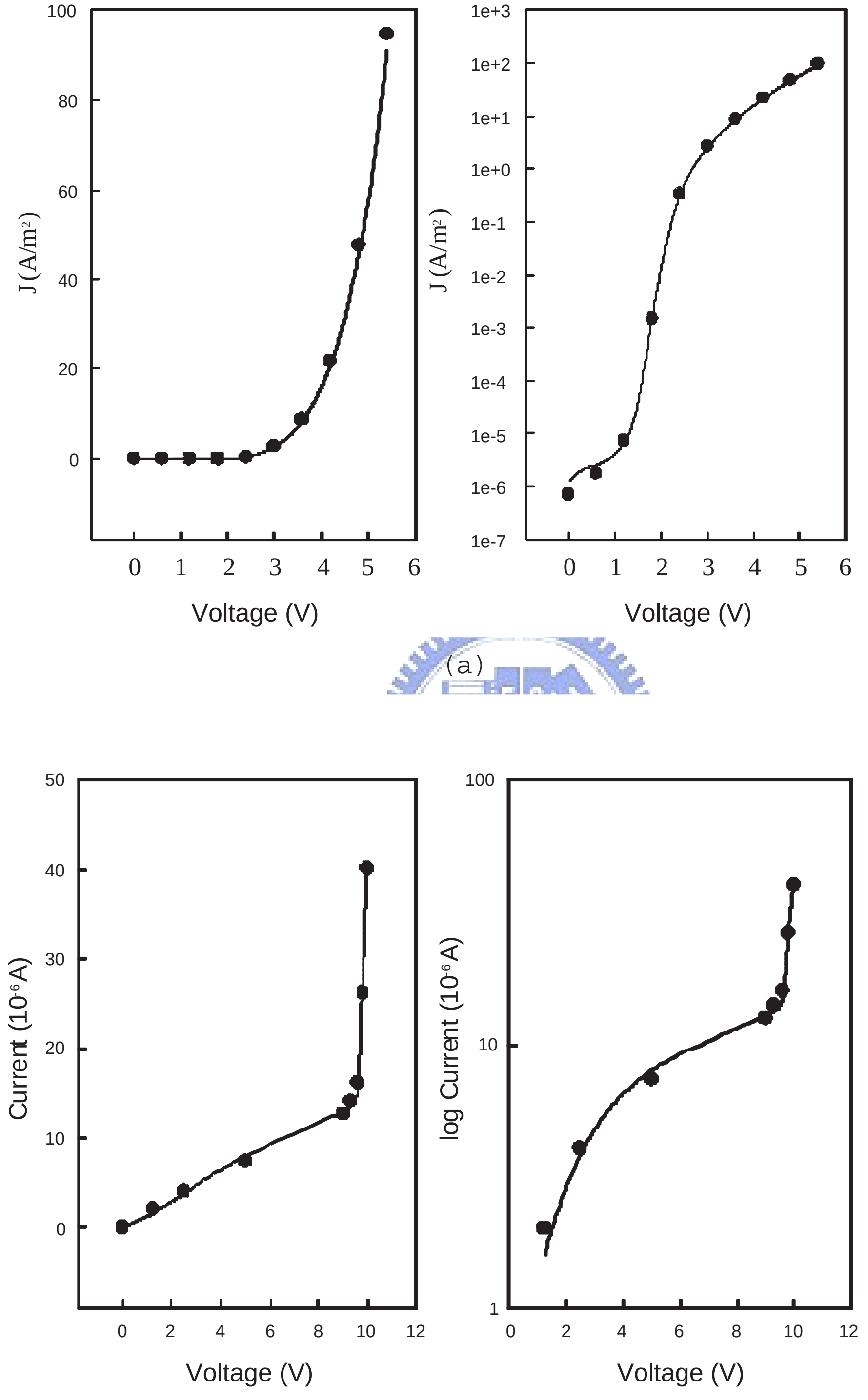


Figure 6.2: Comparison of I-V between measured (symbol curve) and simulated (solid curve) OLED device, where (a) is the red light (b) and is the green light.



(a)

(b)

Figure 6.3: Comparison of I-V between measured (symbol curve) and simulated (solid curve) OLED device, where (a) is the blue light (b) and is our adopted OLED device.

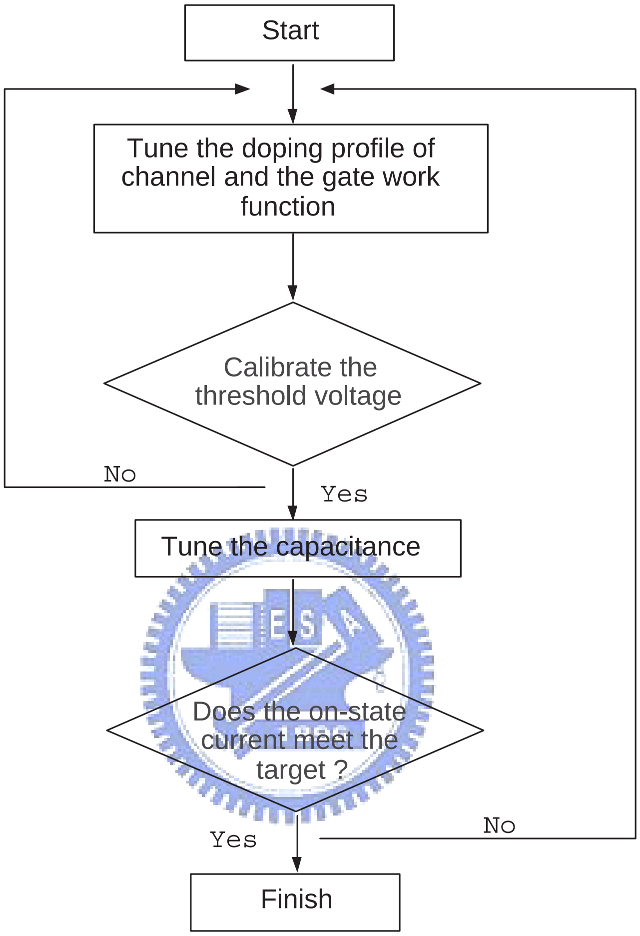


Figure 6.4: A flow chart of OLED's parameters extraction by using device simulation.

Table 6.1: The extracted parameters of OLED.

OLED type	**Red**	**Green**	**Blue**	**adopted OLED**
Capacitor	40 fF	35 fF	36 fF	30 fF
Work function	4.4 eV	4.45 eV	4.45 eV	4.55 eV
Channel doping	1.6E16 cm^{-3}	2E16 cm^{-3}	2E16 cm^{-3}	1E17 cm^{-3}

6.2 The Mixed Mode Equations of the Poly-Si TFT Circuit

The mixed-mode methods contains devices and circuits simulation. Eq. 6.1 - 6.12 are subjects to proper initial and boundary conditions with respect to the node voltage, loop current potential (ϕ) , electron density (*n*), and hole density (*p*).

$$\Delta\phi = \frac{q}{\varepsilon_s}(n - p + N_A - N_D + BT(\phi)), \tag{6.1}$$

$$BT(\phi) = N_{TA} f_{n0} exp(-\frac{\phi - E_B}{V_T}), \tag{6.2}$$

$$\frac{1}{q}\nabla \cdot (-q\mu_n n\nabla\phi + qD_n\nabla n) = R(n,p), \tag{6.3}$$

$$\frac{1}{q}\nabla \cdot (-q\mu_p p\nabla\phi + qD_p\nabla p) = -R(n,p). \tag{6.4}$$

Above three equations are about device simulations. From Fig. 6.1(b), we can write circuit equations:

$$node1 : V_{S1} = V_{Data}, \tag{6.5}$$

$$node2 : V_{G1} = V_{Scan}, \tag{6.6}$$

$$node3 : C_1\frac{dV_{C_1}}{dt} + i_{D1} + i_{G2} = 0, \tag{6.7}$$

$$node4 : V_{D2} = V_{DD}, \tag{6.8}$$

$$node5 : V_{S2} = V_{OLED}, \tag{6.9}$$

$$node6 : V_{GND} = 0, \tag{6.10}$$

$$loop1 : i_1 = C_1 \frac{dV_3}{dt}, \tag{6.11}$$

$$loop2 : i_2 = C_2 \frac{dV_5}{dt}. \tag{6.12}$$

6.3 Results of the Circuit Simulation

Clearly, the left inset shows that the delay time of GAA circuit is about 0.12 μs which is only one ninth of SG circuit. This property may benefit the application of high-resolution display panel. Usually GB appearing on the drain side is the worst situation for devices, where GAA circuit still has an effect to yield higher driving current than that of SG one without GB. 2T1C circuit with GAA poly-Si TFTs can sustain stable currents. We believe similar results can occur for more complicated active matrix circuit, such 4T2C circuit using GAA poly-Si TFTs. Fig. 6.6 shows variation of V$_{OLED}$ with respect to V$_{th}$. High channel doping not only increases V$_{th}$ but also trap concentration of single GB. The latter one results in a serious variation of V$_{OLED}$ for SG circuit. GAA circuit yields more stable driving capability. Finally, we will discuss the device of T_2. The node of V_{OLED} is quite sensitive to the current, moreover, it is mutual influential to V_{gs}. If we can set V_{gs} to a specific constant, we can improve the variation of V_{OLED}. To change T_2 to a p-type poly-Si TFTs is a possible way to make V_{gs} to a given constant because the source becomes the bias of V_{DD}. The degradation of V_{OLED} can be improved efficiently.

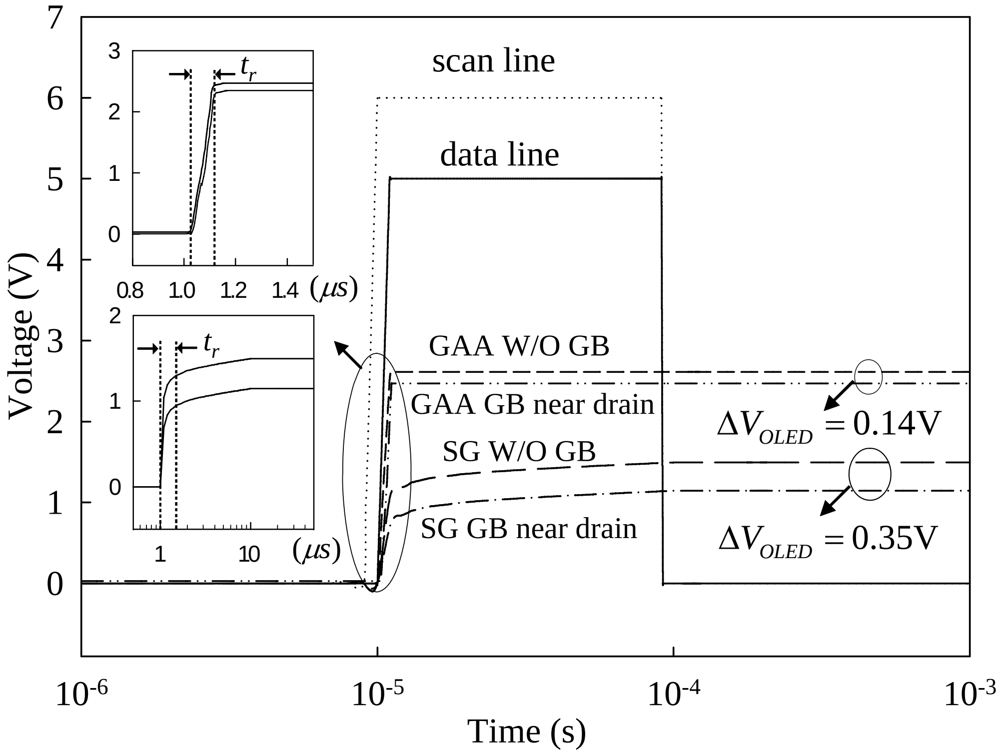


Figure 6.5: The circuit behavior of a 2T1C active matrix driver. As shown in the Fig. 6.1 (b), T_1 is for switching and T_2 is for driving. The GAA circuit exhibits short delay time and stable current.

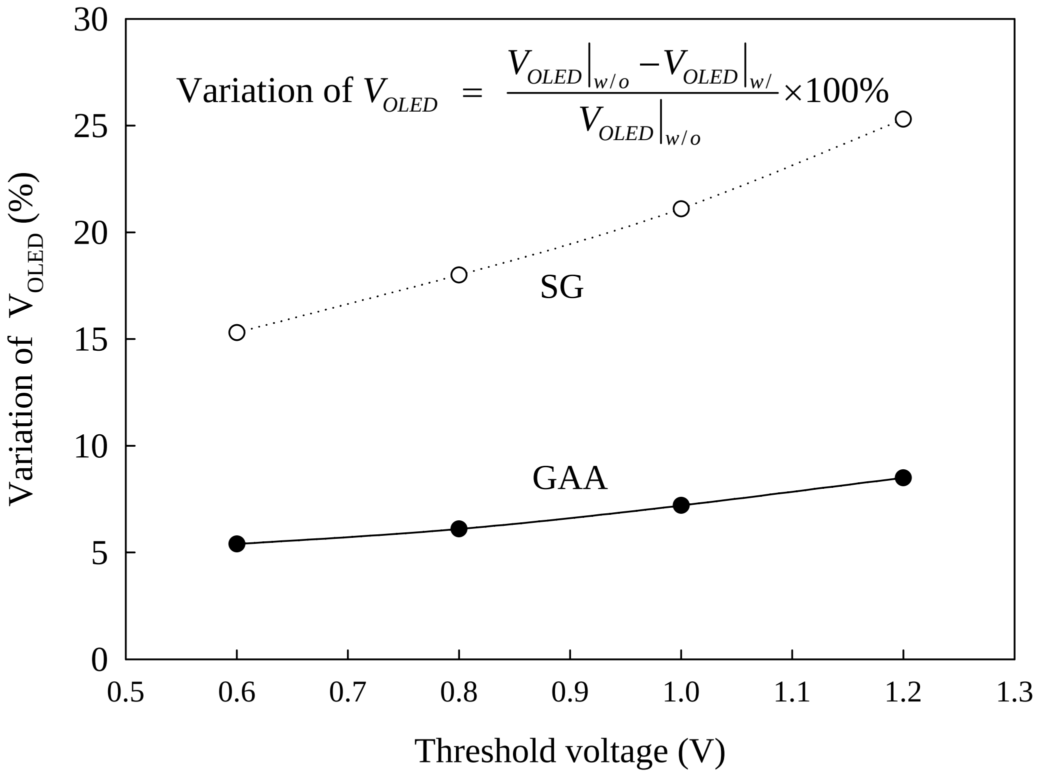


Figure 6.6: The variation of V_{OLED} versus V_{th}. A higher V_{th} implies a serious variation of OLED voltage due to heavy channel doping.

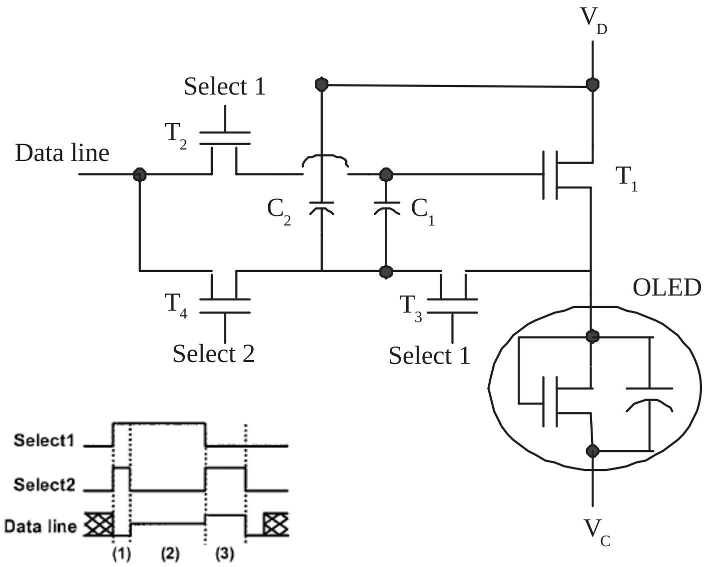


Figure 6.7: Equivalent circuit and driving signals of Goh's proposed pixel circuit. (1) Initialization period, (2) compensation period, (3) and data-input period

Goh proposed a new TFT pixel circuit for active-matrix organic light-emitting diode composed of four TFTs and two capacitors [88]. They indicated that the proposed circuit has high immunity to the variation of poly-Si TFT characteristics. In this thesis, we also simulate Goh's circuit and the equivalent circuit is shown in Fig. 6.7. In an initialization period, T_2, T_3 and T_4 are turned on and the data line is at ground. The gate of T_1 and anode of OLED are initialized to ground. In a compensation period, only T_4 is turned off and a compensation voltage V_{comp} is applied to the data line. The gate of T_1 becomes V_{comp} and source of T_1 settles to V_{comp} - ΔV. Since ΔV is the V_{GS} of T_1 and the drain current of T_1 is in the subthreshold region, the ΔV corresponds to V_{th} of T_1. This is stored in C_1. In a data-input period, only T_4 is turned on and the data line is at an input voltage. Due to the bootstrapping effect, the gate of T_1 becomes V_{input} + V_{th}. Because the driving current of T_1 is within subthreshold region as described above, the source of T_1 becomes V_{input} - ΔV_{input}. The ΔV_{input} depends on the subthreshold slope of T_1. If the drain currents of T_1 in compensation period and data-input period are I_{comp} and I_{out}, the subthreshold slope, S_t (V/dec) of T_1 can be written as:

$$S_t = \frac{\Delta V_{GS}}{\Delta Log(I_{DS})} = \frac{(V_{th} + \Delta V_{input}) - V_{th}}{Log(I_{out}) - Log(I_{comp})}, \tag{6.13}$$

and thus

$$\Delta V_{input} = [Log(I_{out}) - Log(I_{comp})] \times S_t. \tag{6.14}$$

The ΔV_{input} is approaching to zero as S_t decreases. Therefore, the pixel circuit controls the OLED current by changing V_{input}, regardless of the threshold voltage and mobility variations of the poly-Si TFTs. The compensation voltage, V_{comp} can be set to a constant voltage or to the input voltage (V_{comp} = V_{input}). The used parameters in the circuit simulation is shown in Tab. 6.2.

Fig. 6.8 and 6.9 show a transient response result for SG and GAA structures. In compensation period, the difference between data line voltage and anode voltage of an OLED is stored in C_1 and this corresponds to a threshold voltage. Therefore, the anode potential of an OLED is independent of the threshold voltage of a driving TFT. If using GAA poly-Si TFTs, the ΔV_{OLED} is only 0.01 V and has great improvement. The Goh's driving circuit

Table 6.2: The used parameters in the circuit simulation.

Device size	**Supply voltage**	**Period times**
L/W = 300 nm	V_D = 5 V	T_1 = 1 μs
C_1 = C_2 = 0.4 pF	V_C = 0 V	T_2 = 14 μs
C_{OLED} = 30 fF	$V_{select1,2}$ = 0∽5 V	T_3 = 4 μs

is effective to provide a uniform output current against the variation. The ΔV_{OLED} and switching time of active-matrix driving circuits are also shown in Tables 6.3 and 6.4.

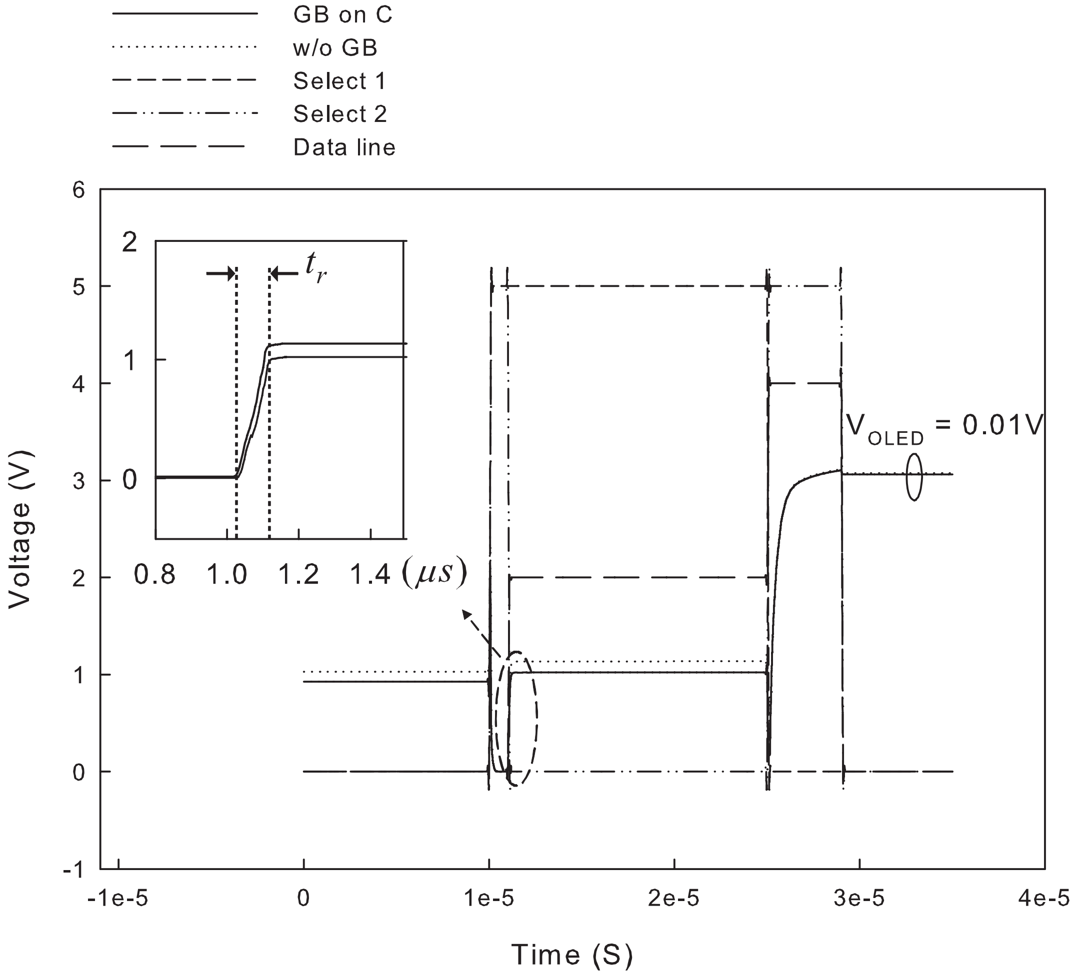


Figure 6.8: The simulation of the GAA poly-Si TFT driving circuit (4T2C) at V_{comp} = 2 V and V_{input} = 4 V.

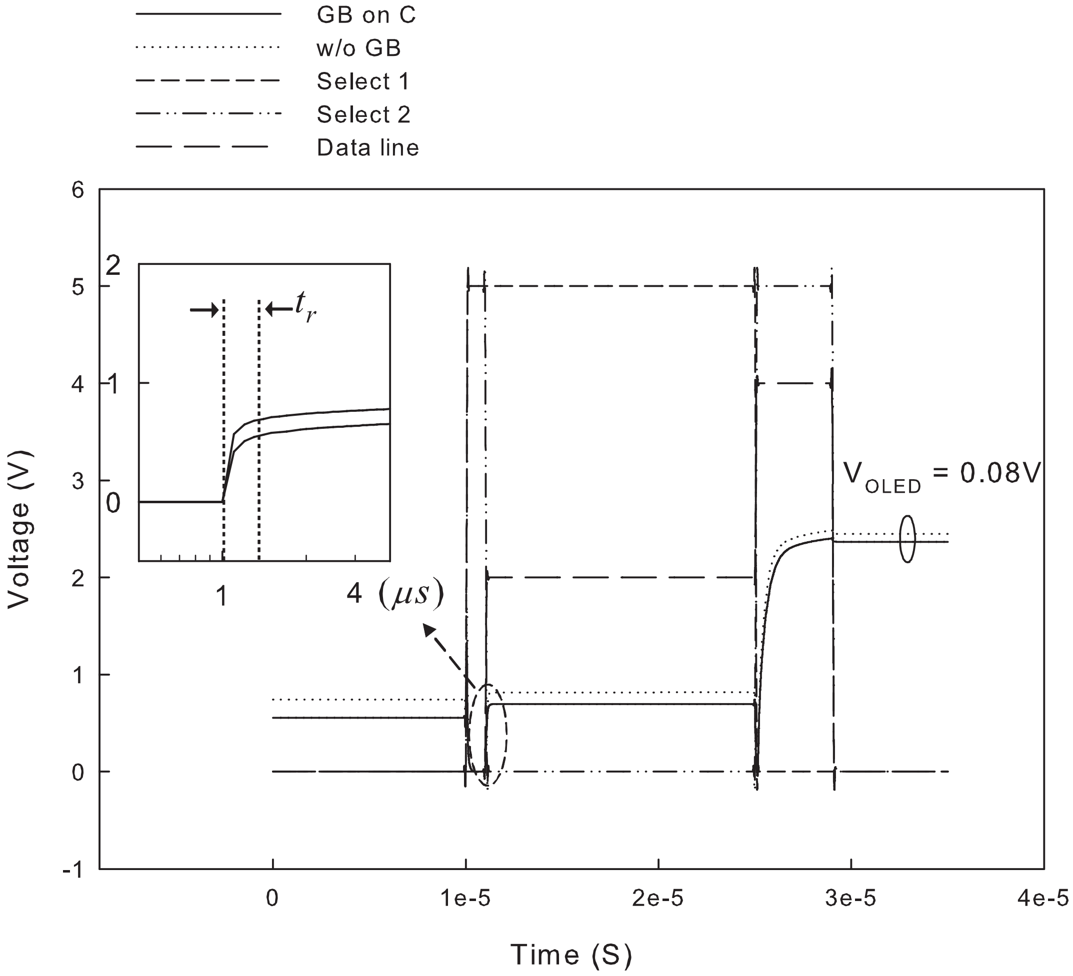


Figure 6.9: The simulation of the SG poly-Si TFTS driving circuit (4T2C) at V_{comp} = 2 V and V_{input} = 4 V.

Table 6.3: The ΔV_{OLED} of 2T1C and 4T2C active-matrix driving circuit.

Driving Circuit	**2T1C**	**4T2C**
SG poly-Si TFTs	ΔV_{OLED} = 0.35 V	ΔV_{OLED} = 0.08 V
GAA poly-Si TFTs	ΔV_{OLED} = 0.14 V	ΔV_{OLED} = 0.01 V

Table 6.4: The switching time of 2T1C and 4T2C active-matrix driving circuits.

Driving Circuit	**2T1C**	**4T2C**
SG poly-Si TFTs	1.1μs	1.1μs
GAA poly-Si TFTs	0.12μs	0.12μs

Chapter 7

Conclusions

In this thesis, we have successfully simulated the poly-Si TFTs with the develpoed adaptive numerical methods. The important parameters of GB have been extracted exactly. The barrier height of GB is equal to 0.15 eV and the concentration of GB is about 3E13/cm^2. When the channel length is equal to 300 nm, (it is about one single grain size), the variation of V_{th} is serious when the GB is near drain side. But if using GAA poly-Si TFTs, the variation of V_{th} can be significant reduced. (there is only 5.45% variation). We further simulated the 90 nm of GAA poly-Si TFTs with the density gradient model. If we control the size of GB within 2 nm, the performance of poly-Si TFTs is independent of the position of GB in the channel.

In the chapter 6, we have explored successfully the behavior of the 2T1C active-matrix driving circuit by using the mixed-mode method simulation in a TCAD tool. The results show that the switching speed of GAA poly-Si TFTs can be improved by nine times, compared with the circuits of SG.

In the section 7.1, I summarize the work. Finally, we suggest future work.

7.1 Summary

A nonlinear trap model has been introduced to describe the effect of grain boundary on the electrical characteristics of poly-Si TFTs. Computed physical quantities, such as potential distribution and electron density, and drain current have demonstrated the effect of traps on the device characteristics. I have studied the dependence of electrical characteristics on the boundary position and size of single grain trap in the poly-Si TFTs from long channel to nano scale. The grain boundary effect in GAA poly-Si TFTs have been model and solved with the 3D device simulation. Compared with the GAA poly-Si TFTs, the boundary position and size of single grain significantly affect the intrinsic performance of the SG poly-Si TFTs. The SG poly-Si TFTs suffer serious short channel effect and performance degradation when the device channel is scaled into the short channel regime. It has been found that the grain boundary locating at the drain side will result in large characteristic variation.

I also have explored the characteristics of GAA poly-Si TFTs and behavior of 2T1C active-matrix driving circuit. Effects of position and trap concentration of single GB on electrical characteristics of device and circuit have been examined using circuit-device coupled mixed-mode technique. Variation on threshold voltage and short channel effect near source and drain sides was studied.

7.2 Suggestion for the Future Work

Listed below, some topics are suggested for further investigation.

One can study the new and efficient numerical methods to simulate the poly-Si TFT devices. Quantum correction models using in poly-Si TFTs can be further studied in the future. Moreover, the design of new active-matrix driving circuit could be explored in order to reduce abd control the variation.

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Appendix A

A List of C++ Source Codes of the Numerical Solution of Two-Dimensional Poisson Equation for P-N Diodes

In this appendix, a copy of source codes for the numerical solution of the 2D Poisson equation is listed. We discrete the Poisson equation with uniform mesh and solve it by Newton's Method. After iteration and obtaining the maximum error convergence, the results will output to a file. The plot is shown in Fig. A.1.

```
    #include”/MosfetDDSimulator/MosfetDDSimulator.h”
#include ⟨cfloat⟩
```

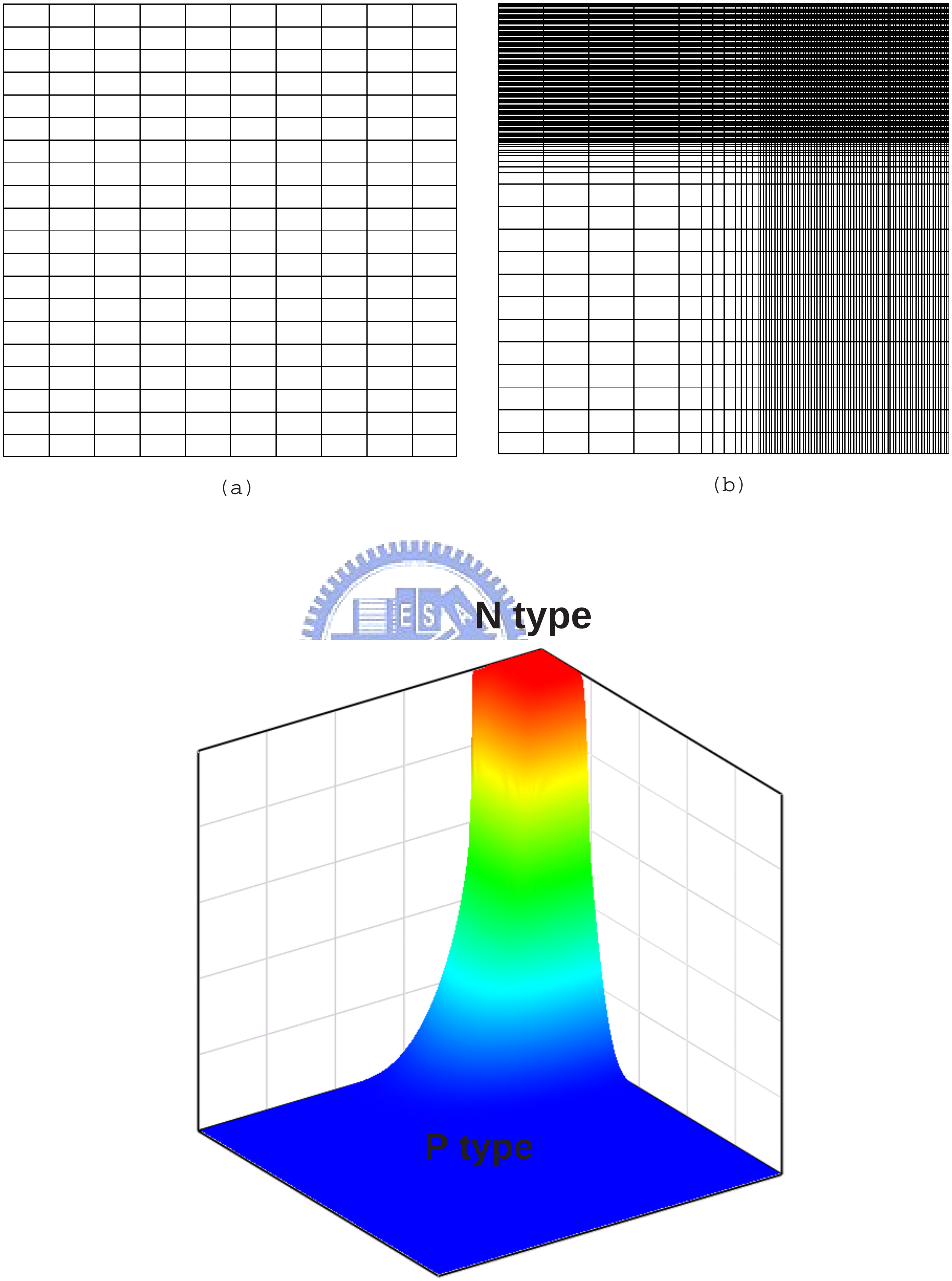
```
void MosfetDDSimulator::MJacobiMethodForPotential()
{
    int NosPhiLoop = 0;
    double MaxError = 0;
    double NowError = 0;
    int i=0,j=0;
    double Lambda = 0;

         vector < vector <double> > TempPHI(Device->NosYLines);
    for(int a=0;a<Device->NosYLines;a++)

     TempPHI[a].resize(Device->NosXLines);

         vector<vector<Node> >::iterator yPtr;
    vector<Node>::iterator xPtr;
    for(j=0;j<Device->NosYLines;j++)
    {
        for(i=0;i<Device->NosXLines;i++)
        {
```

```
                TempPHI[j][i] = PhiMatrix[j][i];
        }
    }
do


        NosPhiLoop++;
        MaxError = 0;
        for(j=1;j<Device->NosYLines-1;j++)
        {
for(i=1;i<Device->NosXLines-1;i++)
{
double a1=UMatrix[j][i]*exp(PhiMatrix[j][i]/VT);
double a2=VMatrix[j][i]*exp(-PhiMatrix[j][i]/VT);
double a=(a1+a2);
double b=(Beta/VT);
Lambda = a*b;



     TempPHI[j][i] = (1.0/(Lambda+AlphaPHI(i,j)))*(FPHI(i,j)+RPHI(i,j)+Lambda*PhiMatrix[j][i]);
}
```

```
}

// update N Bdy

// Left side and Right side N Bdy

for(int a=0;a<Device->NosYLines;a++)

{

TempPHI[a][0] = TempPHI[a][1];

TempPHI[a][Device->NosXLines-1] = TempPHI[a][Device->NosXLines-2];

}

// upper left/right N bdy and Robin Bdy

for(int b=1;b<Device->NosXLines-1;b++)


if(Device->Mesh[Device->NosYLines-1][b].type == 5 ——

Device->Mesh[Device->NosYLines-1][b].type == 7) // left upper N bdy

{

TempPHI[Device->NosYLines-1][b] = TempPHI[Device->NosYLines-2][b];

}

else if((Device->Mesh[Device->NosYLines-1][b].type == 61)—— // Middle R bdy

Middle R bdy

(Device-<Mesh[Device-<NosYLines-1][b].type == 62)——
```

```
(Device-<Mesh[Device-<NosYLines-1][b].type == 63))

{

if(SimDeviceType == 2)

{

TempPHI[Device-<NosYLines-1][b] = PhiToxM[0][b-Device-<LeftGateSurf];



else

{

double aa = TempPHI[Device-<NosYLines-2][b]*Device-<Tox*11.9*Es0;

double bb = Device-<GetVG()*3.9*Es0*K[Device-<NosYLines-2];

double cc = 3.9*Es0*K[Device-<NosYLines-2];

double dd = Device-<Tox*11.9*Es0;

TempPHI[Device-<NosYLines-1][b] = (aa + bb)/(cc + dd);

}



else ;

}

// check error only for this MOSFET

for(int j=0;j<Device-<NosYLines;j++)
```

```
{
for(int i=0;i<Device-<NosXLines;i++)
{
NowError = fabs(TempPHI[j][i] - PhiMatrix[j][i]);
if(MaxError<NowError)
MaxError = NowError;
PhiMatrix[j][i] = TempPHI[j][i];
}
}
}while(MaxError > MTolErrorPHI);
cout << ”Compute PHI Loop :” << NosPhiLoop <<endl;
}
```



(a)

(b)

(C)

Figure A.1: (a) The initial mesh, (b) the final uniform refined, and (c) the 3D plot of the potential.

Appendix B

A List of Mixed Mode Source Codes for the Device-Circuit Simulation

The appendix B lists a copy of the mixed-mode source codes. The codes were used in the simulation of the poly-Si TFT circuit drivers, as discussed in Chap. 6.

```
    Device NTFT
( Electrode (
( name="S"voltage=0.0)
( name="D"voltage=0.0)
( name="G"voltage=0.0 Work function=4.55)
```

```
)
File
(
Grid = ”@grid@”
Doping = ”@doping@”
Plot = ”@dat@”
Current = ”@plot@”
)
Physics
(
Mobility(DopingDependent HighFieldSaturation Enormal)
Recombination(Band2Band(E2))
)
)
File
(
Output = ”@log@”
)
Plot
```

```
(
Doping SpaceCharge
EffectiveIntrinsicDensity
ElectricField/Vector
Band2band
eQuasiFermi hQuasiFermi
eGradQuasiFermi/Vector hGradQuasiFermi/Vector
eGapStatesRecombination
hGapStatesRecombination
eTrappedCharge
hTrappedCharge
eMobility hMobility
eCurrent/Vector hCurrent/Vector TotalCurrent/Vector
)
Math
(
Extrapolate
Derivatives
RelErrControl
```

```
DirectCurrent

Method=UMF

-VoronoiFaceBoxMethod

NaturalBoxMethod

)

System(

Vsource pset vdd (dd 0) (dc = 0.0)

Vsource pset vdata (data 0)

(

pulse = (0.0 dc

8 amplitude

10e-6 td

10e-6 tr

10e-6 tf

80e-6 ton

120e-6) period

)

Vsource pset vscan (scan 0)

(
```

```
pulse = (0.0 dc
10 amplitude
10e-6 td
10e-6 tr
10e-6 tf
80e-6 ton
120e-6) period
)
NTFT nTFT1 ( ”D”=data ”S”=out ”G”=scan )
NTFT nTFT2 ( ”D”=dd”S”=vth ”G”=out )
NTFT nTFT3 ( ”D”=vth ”S”=0 ”G”=vth )
Capacitor pset cout1 ( vth 0 )( capacitance = 3e-12 )
Capacitor pset cout ( out 0 )( capacitance = 3e-14 )
Plot ”n@node@ sys des.plt” (time() v(vth) v(scan) v(data) v(dd) v(out) i(nTFT2,out) i(r,0))
)
Solve
(
Coupled(Iterations=100)( Poisson )
Coupled( Poisson Electron Hole Contact Circuit )
```

```
Quasistationary
(
InitialStep=1e-3 Increment=1.35
MinStep=1e-5 MaxStep=0.05
Goal( Parameter=vdd.dc Voltage= 10 )
)
( Coupled( nTFT1.poisson nTFT1.electron nTFT1.contact
nv2.poisson nTFT2.electron nTFT2.contact
nTFT3.poisson nTFT3.electron nTFT3.contact
circuit )
)
Transient
(
InitialTime=0 FinalTime=120e-6
InitialStep=1e-6 Increment=1
MaxStep=5e-6 MinStep=1e-9
)
( Coupled (nTFT1.poisson nTFT1.electron nTFT1.contact
nTFT2.poisson nTFT2.electron nTFT2.contact
```

```
nTFT3.poisson nTFT3.electron nTFT3.contact circuit))
```

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Publication List:

Conference papers

1. Yiming Li, Jung Y. Huang, **Bo-Shian Lee** and Chih-Hong Hwang, "Effect of Single Grain Boundary Position on Surrounding-Gate Polysilicon Thin Film Transistors" To appear in Proceedings of the 7th IEEE Conference on Nanotechnology (**IEEE-Nano 2007**), Hong Kong, Aug. 2-5, 2007

2. Yiming Li and **Bo-Shian Lee**, "Grain Boundary Effect in Sub-100 nm Surrounding-Gate Polysilicon Thin Film Transistors," Accepted by *The 6th IEEE Conference on Nanotechnology* (**IEEE- NANO 2006**), Cincinnati, Ohio, U.S.A., July 16-20, 2006.

3. Yiming Li and **Bo-Shian Lee**, "Three-Dimensional Simulation of Polysilicon Thin Film Transistors with Single-, Double-, and Surrounding-Gate Structures," Accepted by *The 2006 NSTI Nanotechnology Conference and Trade Show* (**Nanotech 2006**), Boston, Massachusetts, U.S.A., May 7-11, 2006.

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