Chapter 1

Introduction

1.1 Development of display

In recent years, with the development of display, the traditional cathode ray tube has been replaced by the flat-panel display in many applications. Liquid crystal display (LCD) is one of the popular displays. Especially, thin film transistor (TFT) liquid crystal display (LCD) is the most common display at present.

The amorphous silicon thin-film transistor (a-Si) TFT technology is mature and has been widely adopted for active matrix liquid crystal display (AMLCD) due to its low-cost fabrication, low processing temperature, and good uniformity of the electronic characteristic over large panel. As is well known, scan drivers are needed for selectively addressing different rows of pixels in a LCD array. A typical gate driver consists of shift registers (SRs), level shifters, and digital buffers. The shift register produces a single pulse signal from 0V to 5V, then the signal is amplified to -5V~25V by level shifter. Finally, the amplified signal is sent to digital buffer and released to scan line to control the TFT switches in pixels. In conventional LCD, as shown in Fig. 1.1-1, the gate driver is implemented external to the LCD back panel in complementary metal-oxide-semiconductor (CMOS) technology.

1.2 a-Si TFTs

Good electronic properties of a-Si:H such as a high photoconductivity [1-3], and the ability to achieve low cost deposition of the a-Si:H films at low temperatures over large surfaces were strong motivating factors for the employment of this material in large area electronics. Typical applications of a-Si:H include displays, digital scanners,

fax machines, video cameras, medical x-ray imagers, and solar cells. In most of these applications, a-Si:H TFT [4] function either as simple switching elements in, for example, passive matrix imagers or, as active elements in electronic devices such as AMLCD and active matrix flat panel imagers (AMFPIs). For most of these applications, a high resolution, long lifetime, low power consumption and acceptable performance in adverse conditions are crucial.

1.3 Integrated a-Si scan driver (ASGD)

In the past few years, the markets demand for high resolution images such as pictures, maps, and information-rich content on advanced portable personal digital assistants and mobile phones. However, higher resolution needs more external connections and driving ICs. The back panel gate drivers necessitate a large number of output pads which means a larger number of level-shifting buffers in CMOS adding to the driving ICs manufacturing cost significantly. As a result, the cost for driving ICs would be more expensive and it would be difficult to create more and more external pads in limited space.

In order to overcome the problem mentioned before, a integrated a-Si scan driver [5-14] for TFT-LCD should be a ideal solution for this problem, as shown in Fig. 1.3-1. Integrating driver circuits on the panel is important in LCD technology because it can not only reduce the cost of driver ICs, but also provides symmetric, narrow edges, which allow for a larger usable area for panel. Many researchers focus their attention on poly-Si technology for this purpose, since it provides superior device performance such as high mobility and more stable device characteristics for driving circuit [15-18], relative to a-Si TFT. However, the poor uniformity [19-21] and one additional crystallization process [22-26] of a-Si is needed for poly-Si. Recently, a-Si technology has been studied as a key solution for integration of gate drivers (row

drivers) on glass substrates, because it requires no additional processing and is also a technology well adapted for mass production.

1.4 Instability of a-Si TFT

Although a-Si:H TFTs are economical, these devices have the disadvantages of metastable changes of threshold voltage after a prolonged application of gate bias stress called threshold voltage shift [27]. The creation of extra defect states in the band gap of a-Si:H close to the gate dielectric interface, and the charge trapping in the silicon nitride (SiN) gate dielectric are the most commonly considered instability mechanisms of threshold voltage [28-30]. As can be seen in Fig. 1.4-1(a), the most outstanding characteristic is an apparent positive parallel shift of the curve, when a positive bias is applied to the gate electrode of the TFT. The threshold voltage increases with respect to positive bias stress time with small changes of mobility and subthreshold slope. In contrast, the threshold voltage of TFTs decreases after the application of a negative bias stress as shown in Fig. 1.4-1(b) [12]. In addition to DC gate bias stress, the AC gate voltage stress also causes the threshold voltage shift in a-Si TFT [31]. Figure 1.4-2 shows the threshold voltage shift versus effective stress time under both positive and negative bias stress for different pulse conditions. The effective stress time is the accumulated time when the gate voltage is high (ON). For positive pulsed gate bias stress, threshold voltage shift (ΔV_T) is slightly smaller than that for DC gate bias stress and does not depend apparently on gate bias pulse width. For negative pulsed gate bias stress, ΔV_T has strong pulse width dependence, the wider the pulse width, the greater the magnitude of ΔV_T [27].

The instability of a-Si TFT will reduce a circuit lifetime. For a-Si scan driver, it is composed of several TFTs that have different bias stress condition depending on their position in the gate driver circuit. Therefore, different bias stresses on TFTs

leads to different changes in transistor characteristics. As the threshold voltage increases with operating time, the output of circuit becomes unreliable and failed finally. The insufficient lifetime of circuits has been the critical barrier preventing a-Si TFT scan driver from becoming a practical technology.

1.5 Thesis organization

Chapter 1 Introduction

1.1 Development of Display

1.2 Amorphous silicon TFTs

1.3 Integrated a-Si gate driver (ASGD)

1.4 Instability of a-Si TFT

1.5 Thesis organization

Chapter 2 Configuration of ASGD

2.1 Typical configuration

2.2 Proposed configuration

2.3 Function of buffer

Chapter 3 Proposed circuits

3.1 Low Pull-Down Voltage (LPDV) ASGD

3.2 Advanced Low Pull-Down Voltage (ALPDV) ASGD

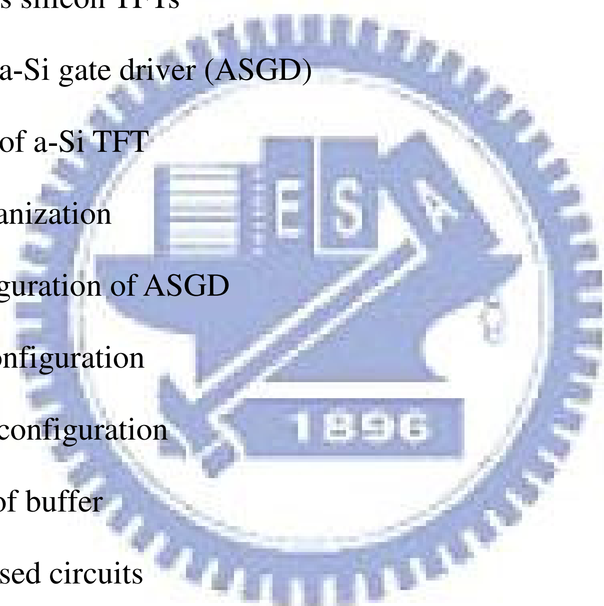
3.3 Robust Low Pull-Down Voltage (RLPDV) ASGD

3.4 The critical TFTs in circuit RLPDV ASGD

3.4.1 The Lifetime of M_5 and M_7

3.4.2 The Lifetime of M_8

Chapter 4 Conclusion



Chapter 2

Configuration of ASGD

2.1 Typical Configuration

Figure 2.1-1 (a) shows the block diagram of a unit circuit in a conventional gate driver using a-Si TFT, which works as a shift register [5-14]. By arrangement of TFTs, circuit1 produces a single pulse signal to P_1 node and circuit2 provides another complementary signal of P_1 for P_2 node, as shown in Fig. 2.1-1 (b). Each unit provides a high voltage output during one horizontal time in one frame time, keeping the gate lines connected to it at a high voltage state and charging pixels controlled by the gate line to given data levels. After the pixels are charged, the gate line is kept low to store the charge in the pixels. In TFT-LCD, the gate lines are maintained at low voltage almost constantly during operation. To stabilize the gate line in a low voltage state, the pull-down transistor remains turned-on. Since each TFT has a different bias stress condition depending on its position in the gate driver circuit, these different bias stresses lead to different changes in transistor characteristics. The P_2 node in the gate driver of Fig.2.1-1 (a) is biased high nearly all the time as show in Fig. 2.1-1 (b), which causes a severe threshold voltage shift in the transistor whose gate electrode is connected to the P_2 node. Therefore, to increase the lifetime of gate drivers, minimizing the threshold voltage shift of TFTs whose gate electrode is connected to the P_2 node is critical. For instance, Figure 2.1-2 (a) and figure 2.1-2 (b) show the typical a-Si scan driver and its clock driving scheme, respectively [5]. The corresponding overall structure on array panel is shown in Fig. 2.1-3. The complete structure needs three clocks and two of them are used in each shift register stage. In

this typical reference circuit, the pull-down TFT M_6 is stressed by about 20V DC voltage during one fram time. As shown in Fig. 2.1-4, the gate voltage V_{P2} of M_6 has 5V AC voltage appended to 20V DC bias. Therefore, the threshild voltage of M_6 will shift seriously after a short operating time [29]. The pull-down system will collapse before long. Finally, the wave shape of output voltage will be failed.

2.2 Proposed Configuration

Figure 2.2-1 shows a simple block diagram of the proposed configuration for gate driver circuit and the timing diagram for the two nodes signals of pull-up and pull-down TFTs. In the new circuit, the bias stress condition for the transistor at the P_2 node can be changed from near DC bias as in Fig. 2.1-1 (a) to almost no stressing bias by means of another pull-down structure. Using the combination of TFTs and clocks, circuit1 in Fig. 2.2-1 (a) produces a single pulse for pull-up TFT and circuit2 in Fig. 2.2-1 (a) produces a shifted single pulse for pull-down TFT. Thus, the duty ratio of the gate voltage on the pull-down TFT is reduced from almost 100% to almost 0%. In other words, the critical pull-down TFT is prevented from large DC stress even when output voltage is low. However, this operation will cause floating at the output node. The floating output can not be connected to the scan bus directly because of the couple from data bus. Therefore, the next buffer stage is required.

2.3 The Buffer Stage

For the buffer stage, the function is to provide the path against the noise coming from panel and keep the data voltage stored in pixel. In other words, the buffer has to be a static logic circuit and the output node is not allowed to be floating. Consequently, one TFT should keep on even when the gate bus is not selected. This TFT will suffer from a long DC stress. Even though this DC bias can not be totally avoided, it can be

minimized as possible. In the proposed buffer stage, as shown in Fig. 2.3-1 (a), an NMOS inverter is formed by M_1 and M_2. The input voltage is V_{out} and the output voltage is V_{P1} for the mentioned NMOS inverter. When V_{out} is logic-zero state, V_{P1} will be logic-one state. Therefore, the path of anti-noise M_3 will keep on while V_{out} is off state. In order to fix a little gate voltage of M_3, M_1 and M_2 are used to be two resistors by their W/L ratio. Thus, the pull-down path is M_3 and its bias voltage is set to near 5V by an additional 1V power supply. By this way, the TFTs in the buffer are subject to little DC stress, while the gate bus is constantly driven to resist the coupling noise. Figure 2.3-1 (b) shows the timing diagram for V_{out} and V_{P1}, where V_H' is much lower than V_H.

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Chapter 3

Proposed Circuits

3.1 Low Pull-Down Voltage (LPDV) ASGD

Figure 3.1-1 (a) and figure 3.1-1 (b) show the first version of the proposed circuit and the corresponding clock driving scheme, respectively. The proposed circuit includes shift register stage and buffer stage. The arrangement of clocks for the proposed circuit is shown in Fig. 3.1-2. It needs six clocks and four of them are used in each shift register stage. The shift register stage is to provide a correct shifted pulse signal. In the proposed shift register, upon the input pulse, during the period T_1, capacitors C_1 and C_5 will be charged to logic-one voltage because M_1 and M_6 are turned on by Φ_1 and Φ_2. So the nodes Pa and Pc are high voltages in T_1 period. In the period T_2, the pull-up TFT M_3 and M_9 will be turned on by Φ_1 bar while the output voltage is high. The TFTs M_6 and M_5 are turn off by Φ_2 and Φ_3, respectively. The Pc node is still high voltage during T_2 period. And then, after aonother clock, during the period T_3, the signal of Φ_3 is logic-one, so the Pd node is charged to high voltage by the Pc node, and TFT M_4 will turn on to pull the output voltage down. Thus, the two TFTs M_3 and M_9 will go off while the output voltage is low. As shown in Fig.3.1-3, the gate voltage V_{Pd} of pull-down TFT M_4 goes back to low in quickly. Thus, the duty ratio of the gate voltage on the pull-down TFT is reduced from almost 100% to almost 0%. In other words, the critical pull-down TFT M_4 is prevented from large DC stress even when output voltage is low. However, this operation will cause floating at the output node. The floating output can not be connected to the scan bus directly because of the noise coupled from data bus. Therefore, the next buffer stage is required.

As mentioned in chapter 2.3, the function of the buffer stage is to provide the path against the noise coming from panel and keep the data voltage stored in pixel. Consequently, M_8 should keep on even when the gate bus is not selected. This TFT will suffer from a long but small DC stress. As shown in Fig. 3.1-3, the gate-source voltage of M_8 is stressed by a 5V DC bias. Therefore, M_8 can have a long lifetime while the circuit keeps operating.

Table 3.1-1 lists the stress conditions for every TFT in LPDV ASGD at stady state. In table 3.1-1, the stress types can be classified into AC and DC stresses. Among the TFTs which are stressed by AC voltage, M_3 is the critical one because of not only the most severe ΔV_T tolerance for the circuit but thee high AC stress of -30V at the gate, where ΔV_T tolerance is the threshold voltage shift that causes malfunction of the circuit. For the same reason, M_9 is the critical TFT for the DC stress case.

For proposed LPDV ASGD, as many as eleven TFTs are used and thus a large layout area is required. In addition, as shown in Fig. 3.1-3, the swing of output voltage is not steep enough. Furthermore, the TFT M_9 is stressed at a large negative DC voltage which will induce a seriously threshold voltage shift. In order to correct these disadvantages, a second shift register is proposed and will be introduced in next section.

3.2 Advanced Low Pull-Down Voltage (ALPDV) ASGD

Figure 3.2-1 (a) and figure 3.2-1 (b) show the second proposed circuit and its clock driving scheme, respectively. The proposed ALPDV ASGD includes shift register stage and buffer stage. The corresponding overall structure on array panel is shown in Fig.3.2-2. The complete structure needs two clocks and all of them are used in each shift register stage. In shift register stage, after the input pulse, M_1 and M_4 are turned on by clock Φ_1 and P_1 will be charged during the period T_1. One clock later, in

the T_2 period, the pull-up TFTs M_2 will pull the output voltage up to logic one voltage by clock Φ_2 while the signal of is Φ_2 high. And then, during the T_3 period, the P_1 node is discharged because of the logic-one of clock Φ_1. The TFT M_2 will go off and the TFT M_3 will turn on to pull the output voltage down while clock Φ_1 is high voltage. Figure 3.2-3 shows the simulated wave diagram for some important nodes in circuit ALPDV ASGD. In order to level down the AC stress voltage for pull-down TFT M_3, an additional 10V DC power supply V_{DD} is appended to shift register stage. Using the coupling effect of clock Φ_1 on TFT M_4 [32], the swing of AC stress on gate voltage V_{P2} can be decrease to about 15V, as shown in Fig. 3.2-3.

Table 3.2-1 shows the stress condition for every TFT in ALPDV ASGD at stady state. In table 3.2-1, the TFTs M_5, M_6 and M_7 are less important because they have small DC stress and very large ΔV_T tolerance attribute to the clock pull-down signal on V_{P2}. The other four TFTs all have significant AC stress on gate. Especially, TFT M_2 has about -30V AC stress on gate-drain voltage and only -4V ΔV_T tolerance. So M_2 is the critical TFT in circuit ALPDV ASGD. Compared with LPDV ASGD, there are only seven TFTs used in ALPDV ASGD. And further, as shown in Fig. 3.2-3, the wave of output voltage is sharper. In addition, the stress siruration for M_2 in ALPDV ASGD is better than that for M_9 in LPDV ASGD. Nevertheless, the ΔV_T tolerance of M_2 is not wide enough and TFTs have significant AC stress in ALPDV ASGD. This might reduce the reliability for circuit ALPDV ASGD. To improve furthermore, another novel shift register RLPDV ASGD will be proposed in next section.

3.3 Robust Low Pull-Down Voltage (RLPDV) ASGD

Figure 3.3-1 (a) and figure 3.3-1 (b) show the final version of the latest proposed circuit in this work and its clock driving scheme, respectively. The proposed RLPDV ASGD includes shift register stage and buffer stage. The corresponding overall

structure on array panel is shown in Fig.3.3-2. The complete structure needs two clocks and one of them is used in each shift register stage. Upon the input pulse, during the period T_1, the P_1 node will be charged and the output voltage is low while the signal of Φ_1 is low. One clock later, the two pull-up TFTs M_2 and M_8 will pull the output voltage up to logic one voltage in T_2 period. In the T_3 period, the P_1 node is discharged by signal V_{n+1} while the gate voltage of M_4 is high. Therefoer, The TFTs M_2 and M_8 will go off and the TFT M_3 will turn on to pull the output voltage down. The corrsponding wave diagram is shown in Fig. 3.3-3. The gate voltage of pull-down TFT M_3 goes back to low in a very short period because of the V_{n+1} signal. Thus, the critical pull-down TFT M_3 is prevented from a large DC stress even when output voltage is low. The effect of TFT M_8 is to protect TFT M_2. The TFT M_2 is protected from a large negative AC gate bias because the screen of M_8. In addition, the noise of output voltage induced by leakage of the pull-up TFT is suppressed. Therefore, the ΔV_T tolerance for pull-up TFT will increase. For the output signal of RLPDV ASGD, it is still floating, so the buffer stage is in demand. The function of the buffer stage is mentioned before and its operation is the same with LPDV ASGD and ALPDV ASGD.

Table 3.3-1 shows the stress condition for every TFT in RLPDV ASGD at stady state. Look the TFTs M_1, M_2, M_3, M_4, M_6, no matter what kind stress of them, the stress voltage is quite snall; moreover, they all have broad ΔV_T tolerance. Therefore, the reliability for TFTs M_1, M_2, M_3, M_4, M_6 are less important than that for M_5, M_7 and M_8 in RLPDV ASGD. M_5, M_7 and M_8 are the three critical TFTs. First, keep an eye on M_5 and M_7. They have almost DC gate bias stress about 5V and 4V ΔV_T tolerance. The 4V ΔV_T tolerance looks little, but it will be confirmed that is a large tolerance for 5V DC stress in chapter four. Second, the stress siturations for M_8 are about -20V AC gate-drain volatge and -8V ΔV_T tolerance. Compare M_8 with the

pull-up TFT M_2 in ALPDV ASGD, the ΔV_T tolerance of M_8 is twice as big as that of M_2 and the stress voltage is reduced from -26V AC gate-drain volatge to -20V AC gate-drain volatge. Furthermore, in circuit RLPDV ASGD, there is no large positive AC gate bias such like clock Φ_1 in circuit ALPDV ASGD. Consequently, the reliability of RLPDV ASGD is much better than that of LPDV ASGD and ALPDV ASGD. The lifetime for proposed circuit RLPDV ASGD will be evaluated in next chapter.

3.4 The critical TFTs in circuit RLPDV ASGD

For proposed circuit RLPDV ASGD, as explained in the last section of chapter 3, M_5, M_7 and M_8 are three critical TFTs because of their high stress voltage and low ΔV_T tolerance. Therefore, the reliability for thease three key TFTs dominate the lifetime of the proposed circuit. In cause of predicting the lifetime for circuit RLPDV ASGD, these three key TFTs are analyzed in this chapter.

3.4.1 The Lifetime of the critical TFTs with DC stress

From table 3.3-1, the stress voltage and ΔV_T tolerance for the two crytical TFTs M_5 and M_7 in buffer stage are 5V DC voltage and 4V, respectively. The Id-Vg curve of them will parallel shift with the operating time, as shown in Fig. 3.4-1. Furthermore, when the magnitude of shifted threshold voltage reaches to 4V, the unreliable output will exhibits and then the function of circuit is failed. Figure 3.4-2 shows the wrong output of the proposed circuit RLPDV ASGD while the threshold voltage shift in M_5 and M_7 is 4V. For the buffer stage, the pull-down path will not function if the two crytical TFTs can not be turned on because of the 4V ΔV_T shift. In such a case the leakage current from the shift register stage charges C_{load} and thus, the output voltage in the off period goes up, as shown the in Fig. 3.4-2. According to the reported paper

[27], V_T shift for DC stress follows a power law with gate-voltage stress and time as mapped in the following equation:

$$\Delta V_T(t) = A\,|V_{ST} - V_{Ti}|^{\alpha}\, t^{\beta} \qquad (1)$$

where V_{ST} is the stress voltage (gate to source voltage), V_{Ti} is the initial threshold voltage, A, α, β are constants. To realize how long the ΔV_T of a TFT does reach to 4V under 5V DC stress, the reliability measurement and data curve fitting were done. Figure 3.4-3 shows the curve of ΔV_T versus stressing time for 5V DC stress and the fitting result for equation (1). According to the fitting curve in Fig. 3.4-3, the three parameters, A, α, β for M_5 and M_7 were extracted, and listed in table 3.4-1. For the ΔV_T of 4V, accordingly, the lifetime of M_5 and M_7 were predicted to be about 7.6 years.

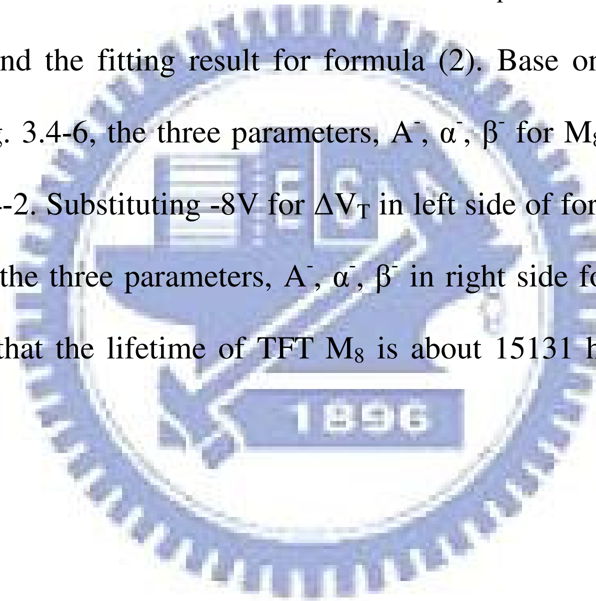
3.4.2 The Lifetime of the critical TFT with AC stress

According to table 3.3-1, the TFTs used in shift register stage are stressed by AC voltages. Among these TFTs, M_8 is the most critical one in shift register stage because it has the largest AC stress on gate-drain voltage and the narrowest ΔV_T tolerance, which are -20V AC gate-drain voltage and -8V, respectively. For the shift register stage, the TFT M_8 is continuously stressed by -20V AC gate-drain voltage corresponding to clock Φ_1 or Φ_2. Therefore, the threshold voltage of M_8 will decrease and the Id-Vg curve of the TFT M_8 will parallel negatively shift with the stressing time [33], as shown in Fig. 3.4-4. When the V_{th} of M_8 negatively shift, the TFT will be normally on and equivalent to one capacitor. Then, the voltage on P_1 node is affected by Φ_1 through the M_8 capacitor and the overlape capacitance of M_2. Finally, the output voltage will be coupled through C_1 and possibly failed. Figure 3.4-5 shows the bad output of the proposed circuit RLPDV ASGD while the threshold voltage shift in M_8 is -8V. When the output voltage is possibly failed, the off-state for gate voltage in

pixel TFT is affected. Therefore, the V_{com} compensation in LCD panel is not correct and the DC residue will exhibit. According to the previous paper [27], V_T shift for AC stress follows another power law with gate-voltage stress, time, and duty cycle as mapped in the following equation:

$$\Delta V_T(t) = A^{-}(V_{ST} - V_{Ti})^{\alpha^{-}}[t \cdot (1 - Dc)]^{\beta^{-}} \quad (2)$$

where V_{ST} is the stress voltage (gate to source voltage), V_{Ti} is the initial threshold voltage, A^{-}, α^{-}, β^{-} are constants, and Dc is the duty cycle of the stressing voltage. To estimate the lifetime of TFT M_8, the reliability measurement and data curve fitting were done. Figure 3.4-6 shows the measurement of ΔV_T versus stressing time under -20V AC stress and the fitting result for formula (2). Base on the fitting curve of formula (2) in Fig. 3.4-6, the three parameters, A^{-}, α^{-}, β^{-} for M_8 can be extracted, as shown in table 3.4-2. Substituting -8V for ΔV_T in left side of formula (2) and the data in table 3.4-2 for the three parameters, A^{-}, α^{-}, β^{-} in right side formula (2). Finally, it can be predicted that the lifetime of TFT M_8 is about 15131 hours, which is about 1.73 years.



Chapter 4

Conclusion

A new a-Si scan driver is developed to be integrated on array panel. A highly reliable amorphous silicon thin film transistor gate driver circuit is achieved. The TFTs in the proposed circuit are subject to almost no DC stress except the critical DC stress condition with reduced voltage of 5V. According to the reliability measurement data of the a-Si TFTs, the lifetime of proposed circuit RLPDV ASGD is evaluated and it is estimated to over 1.7 years.

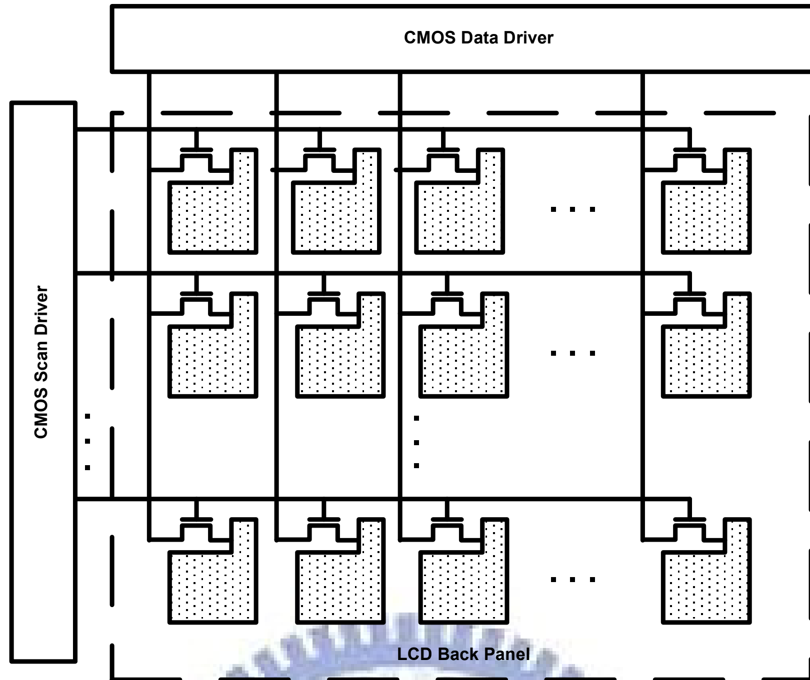


Fig. 1-1.1 A back panel structure of a typical LCD.

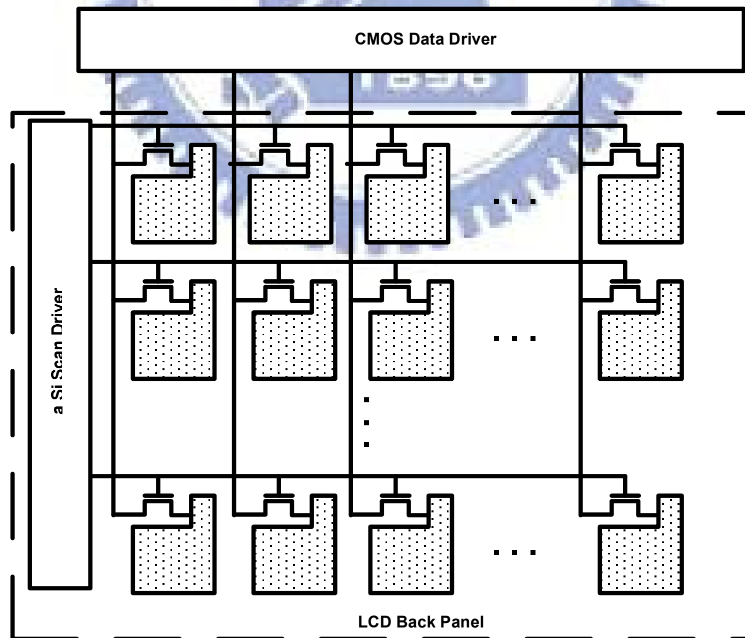
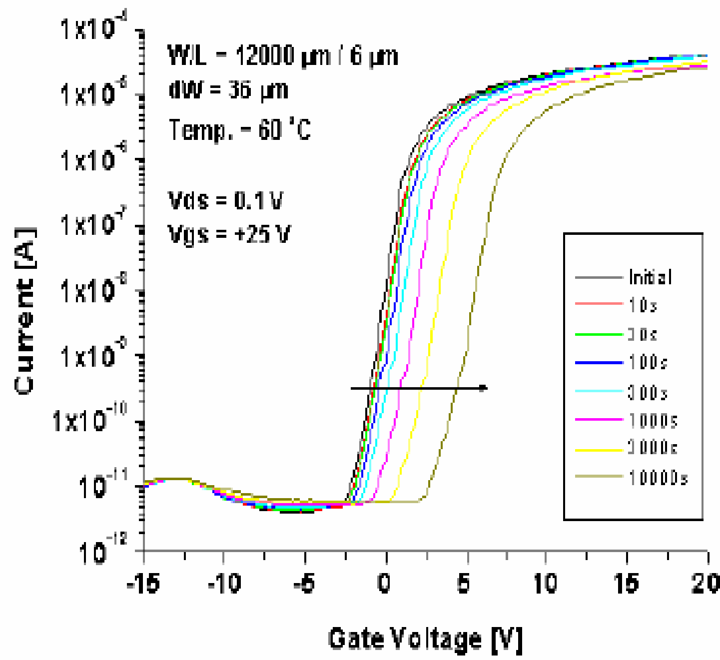
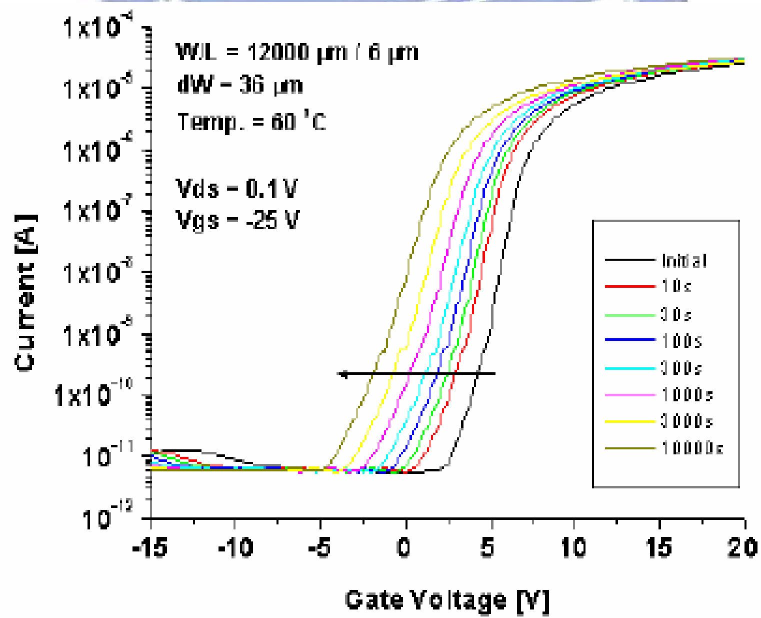


Fig. 1.3-1 A structure of back panel integrate a-Si scan driver.



(a)



(b)

Fig. 1.4-1 Threshold voltage shift of a-Si TFTs with various bias stress times (a) Vgs = +25V and (b) Vgs = -25V. [SID05, P-172L]

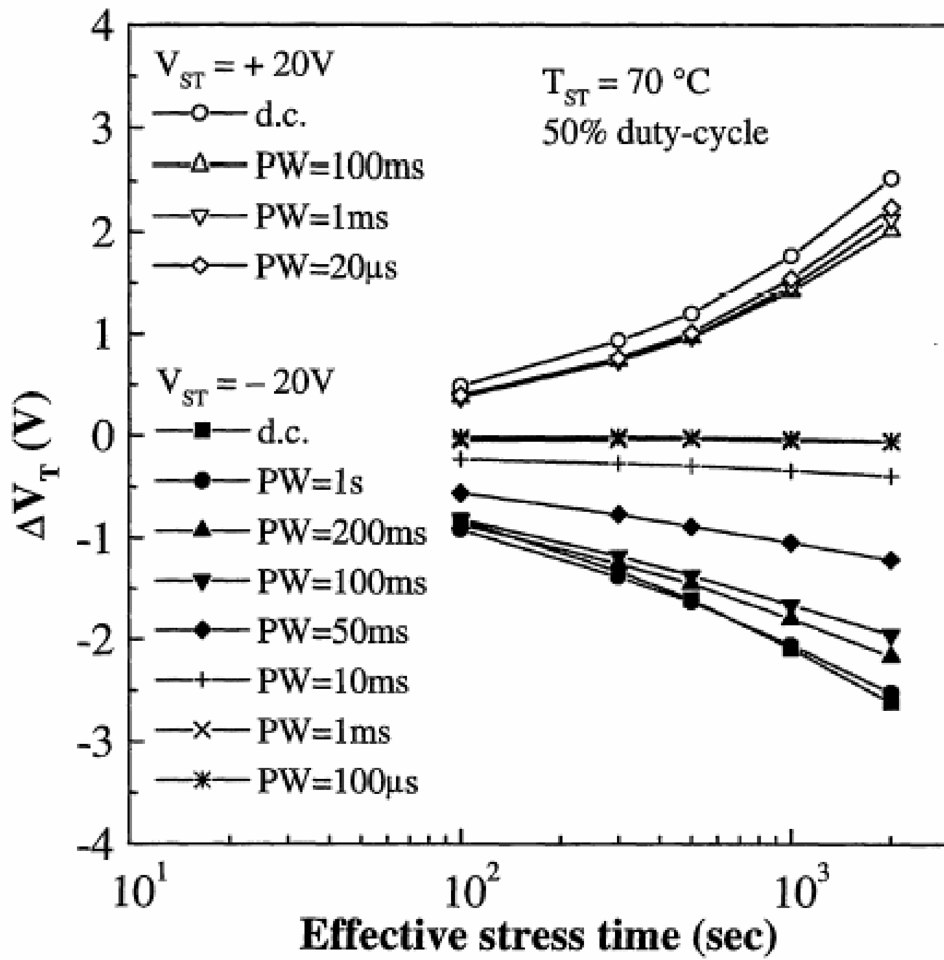
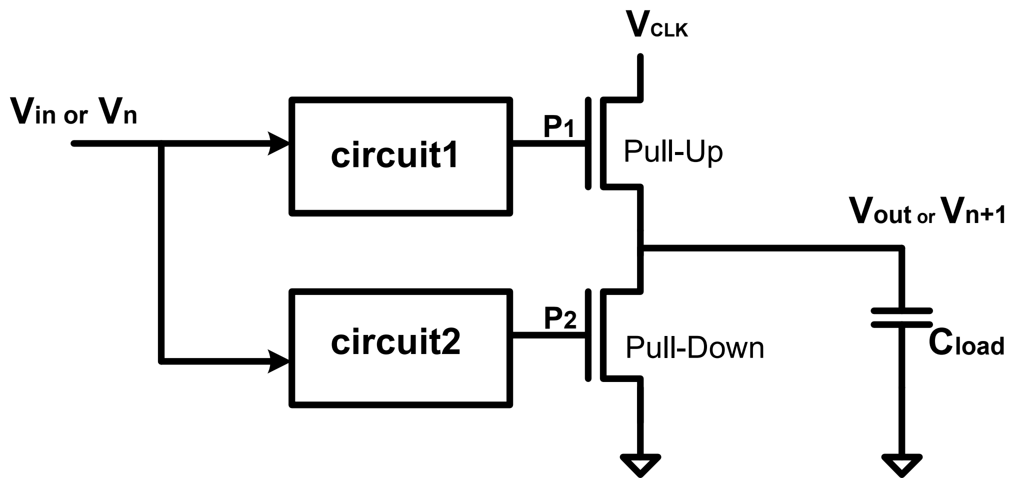
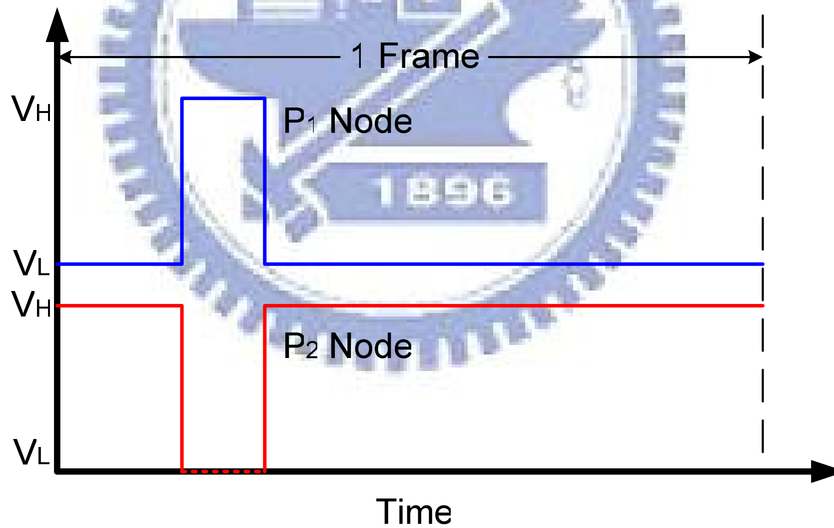


Fig. 1.4-2 ΔV_T versus effective stress induced by positive and negative gate bias stress for different pulse conditions. The effective stress time is the accumulated time when the gate voltage is high (ON). [Jpn. J. Appl. Phys. Vol. 37 (1998) Pt. 1, NO.9A]

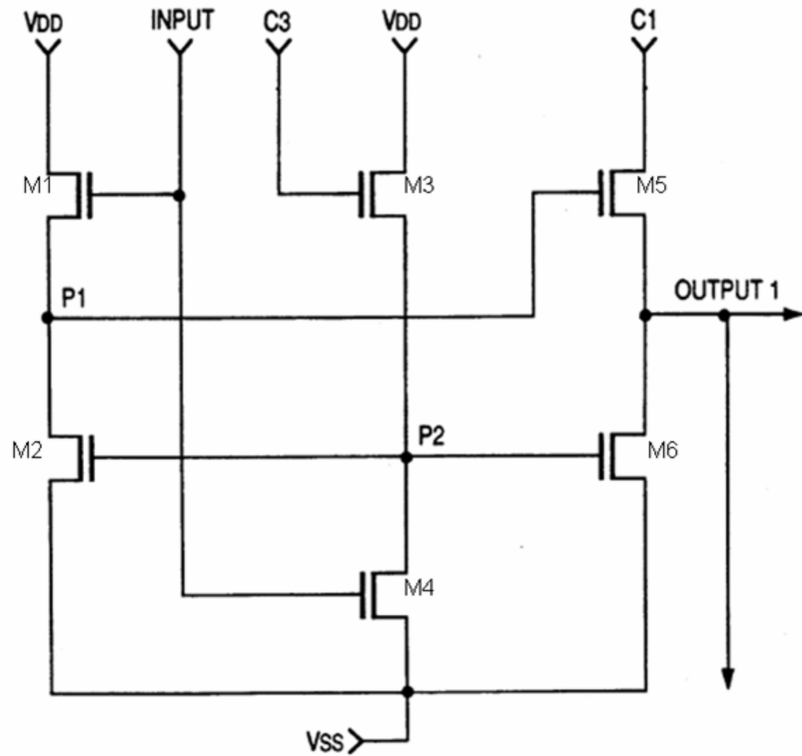


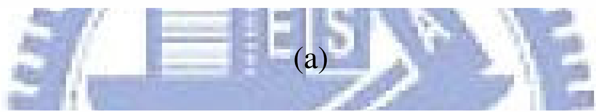
(a)



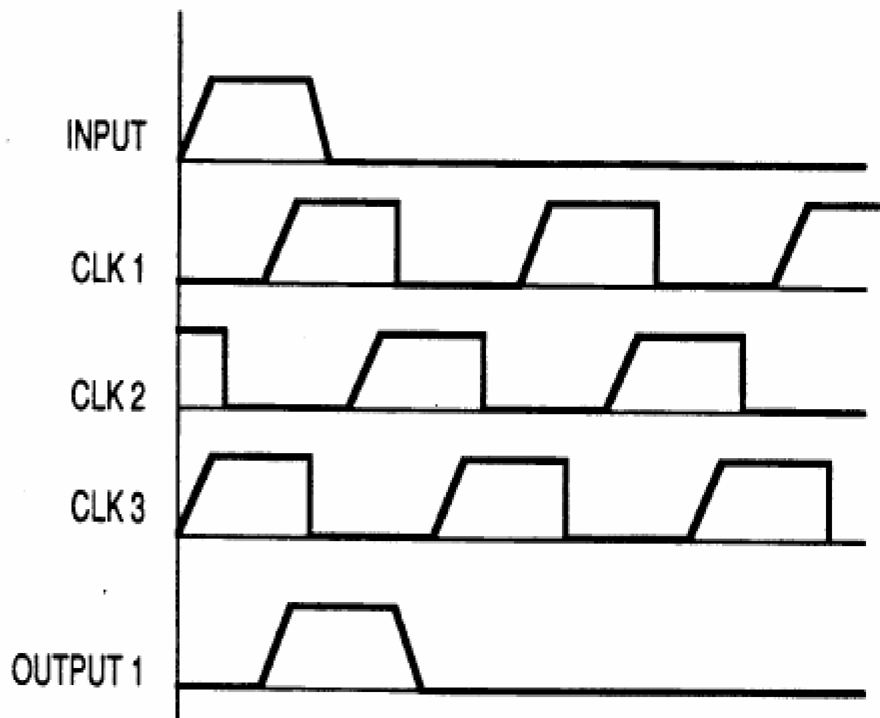
(b)

Fig. 2.1-1 (a) Schematic block diagram of conventional gate driver unit using a-Si TFT and (b) timing diagram on P_1 and P_2 nodes in the circuit.





(a)



(b)

Fig. 2.1-2 A typical scan driver cricuit. (a) schematics (b) clock driving scheme

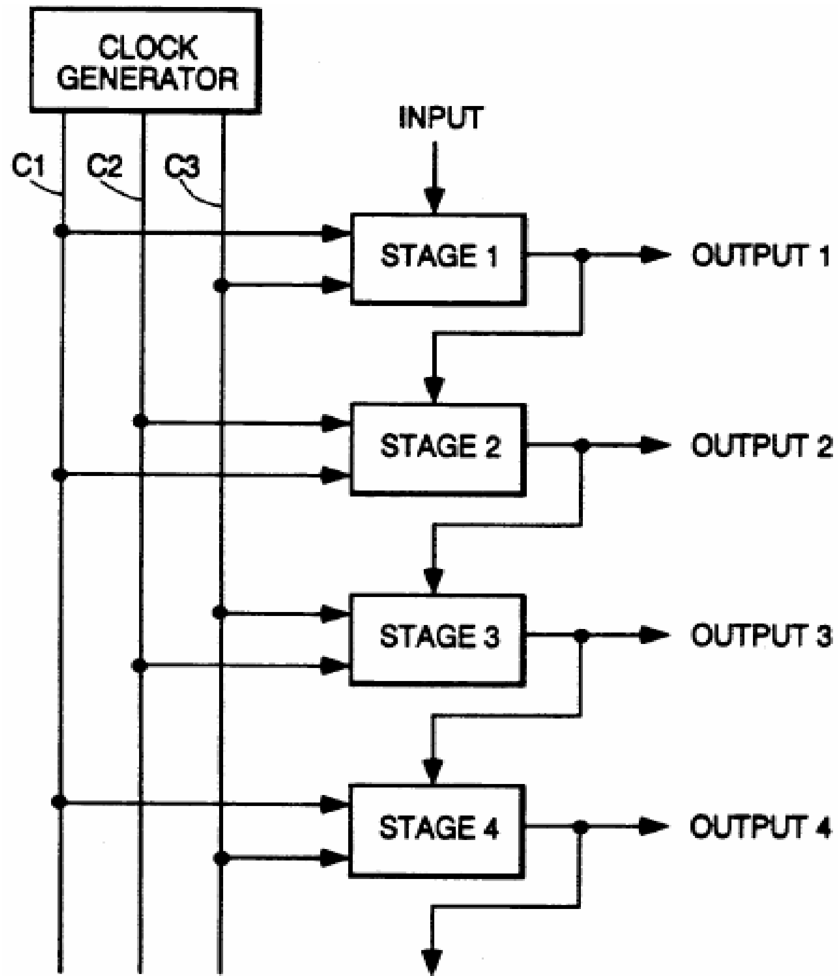


Fig. 2.1-3 Overall structure of typical circuit on array panel.

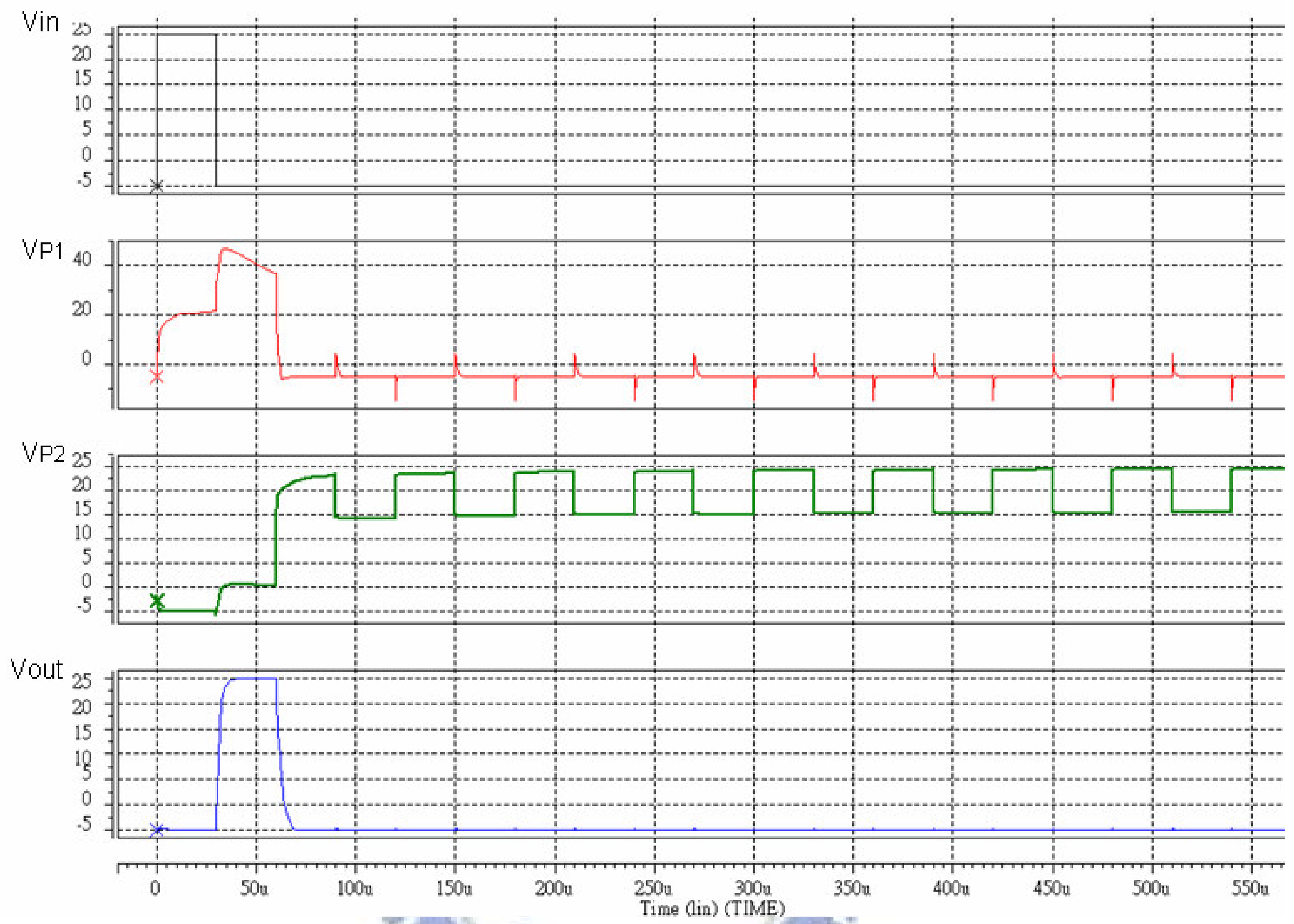
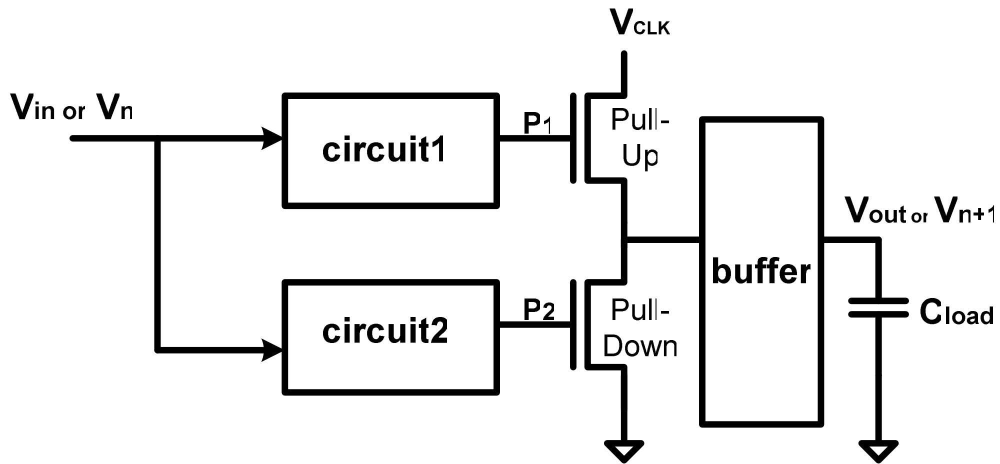
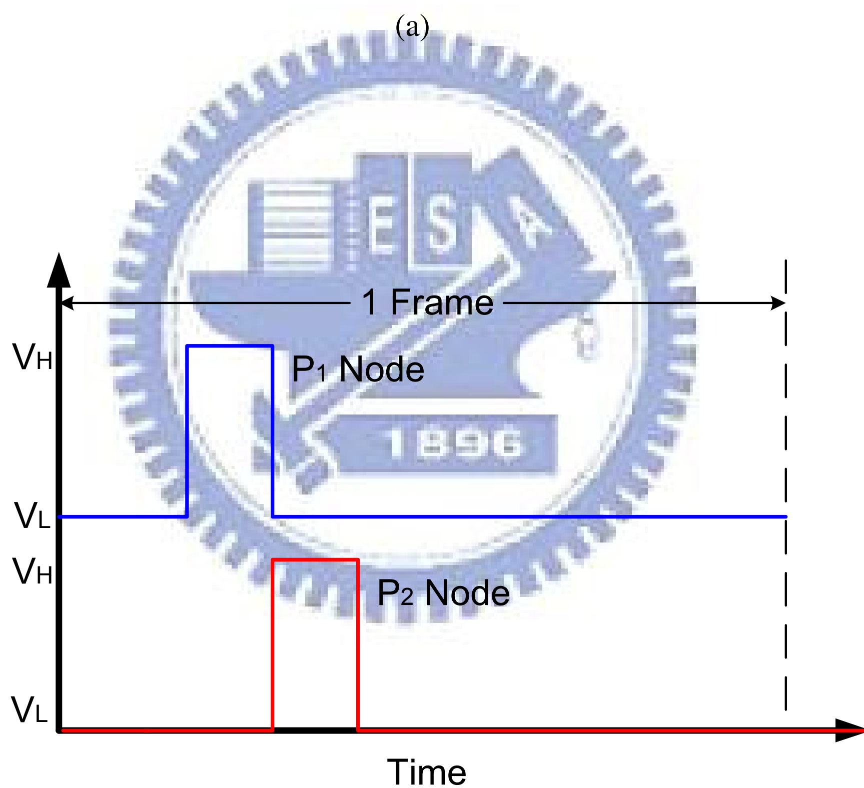


Fig. 2.1-4 The simulated results at some nodes in typical circuit.

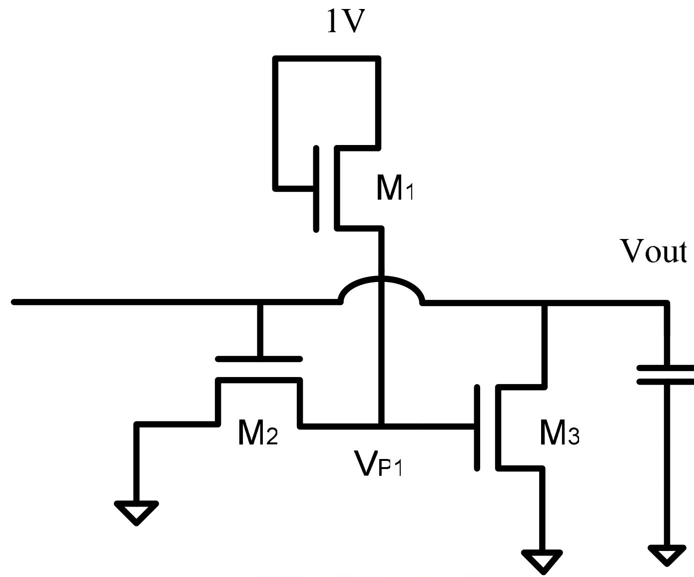


(a)

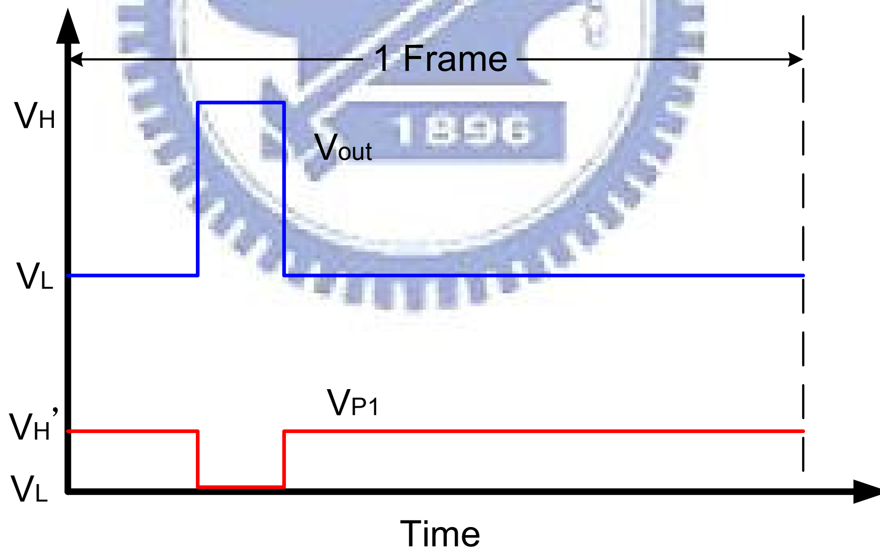


(b)

Fig. 2.2-1 (a) Schematic block diagram of proposed a-Si TFT gate driver and (b) timing diagram on P_1 and P_2 nodes in the circuit.

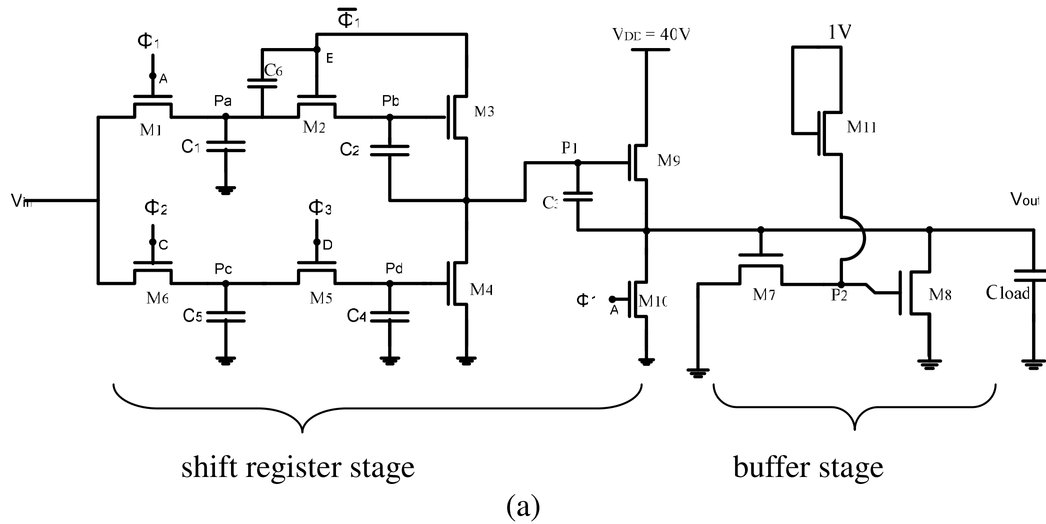


(a)

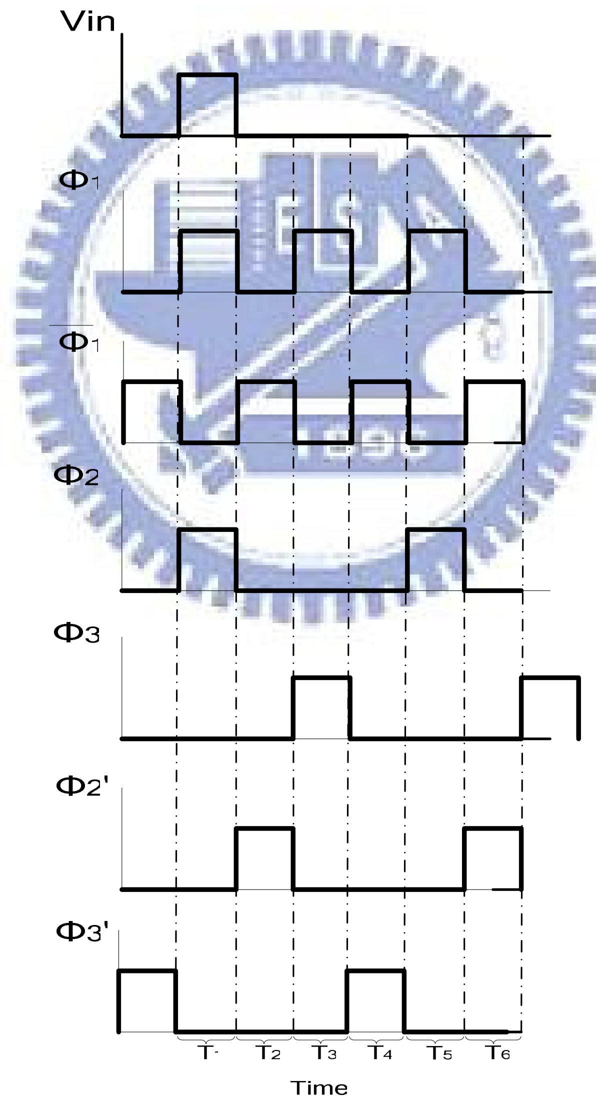


(b)

Fig. 2.3-1 (a) The circuit diagram for buffer stage and (b) timing diagram on P_1 and P_2 nodes in the circuit.



(a)



(b)

Fig. 3.1-1 The proposed scan driver cricuit LPDV ASGD . (a) schematics (b) clock driving scheme

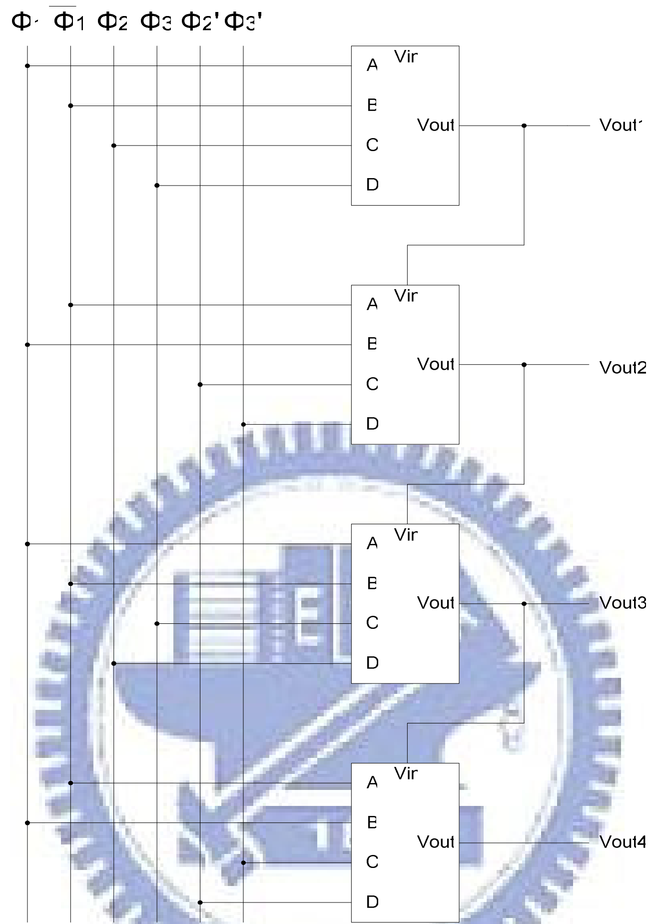


Fig. 3.1-2 Overall structure of LPDV ASGD on array panel.

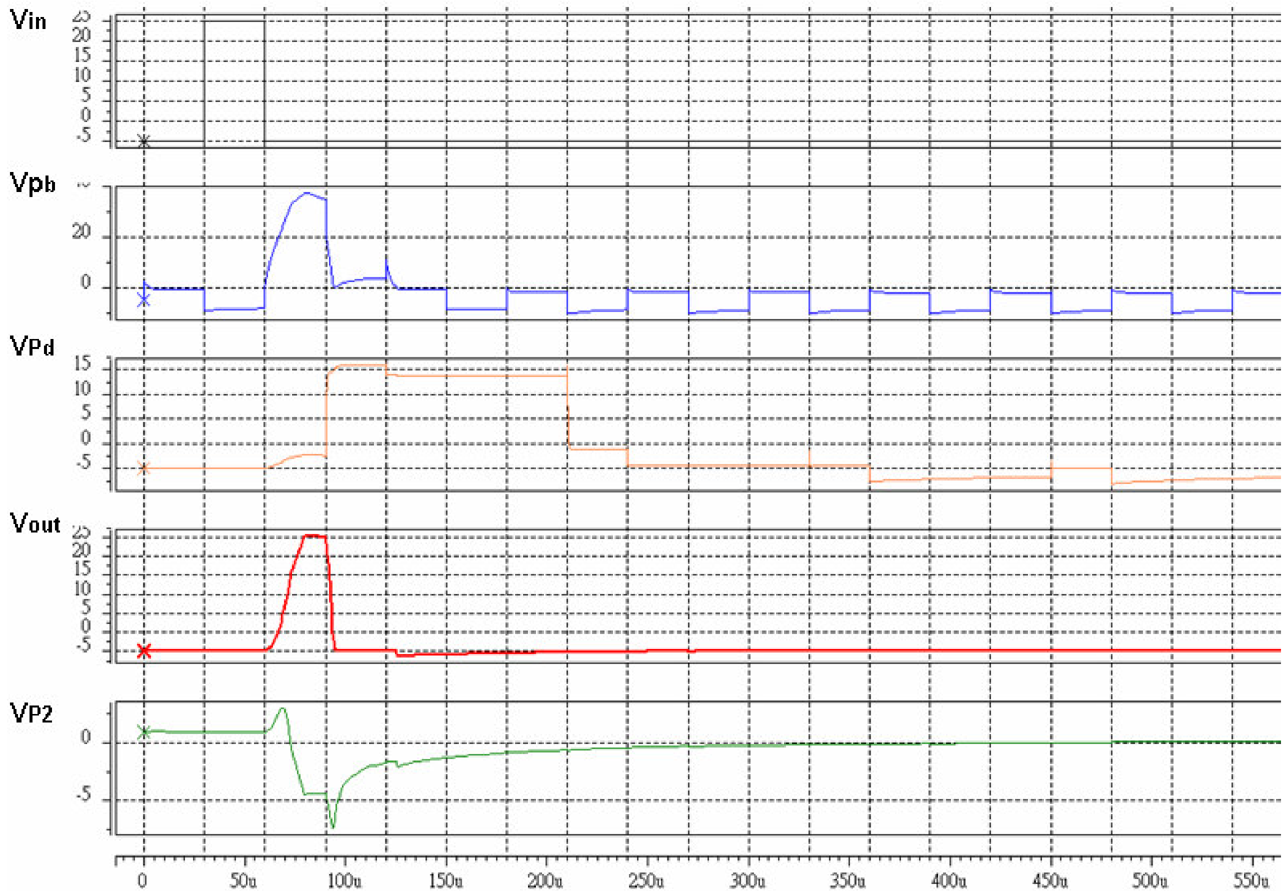
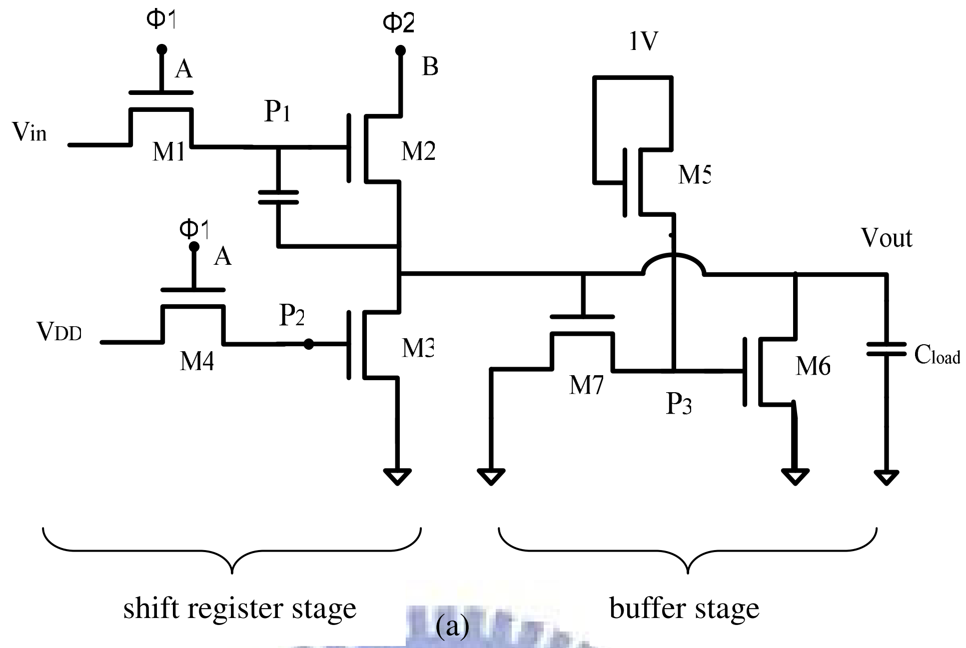


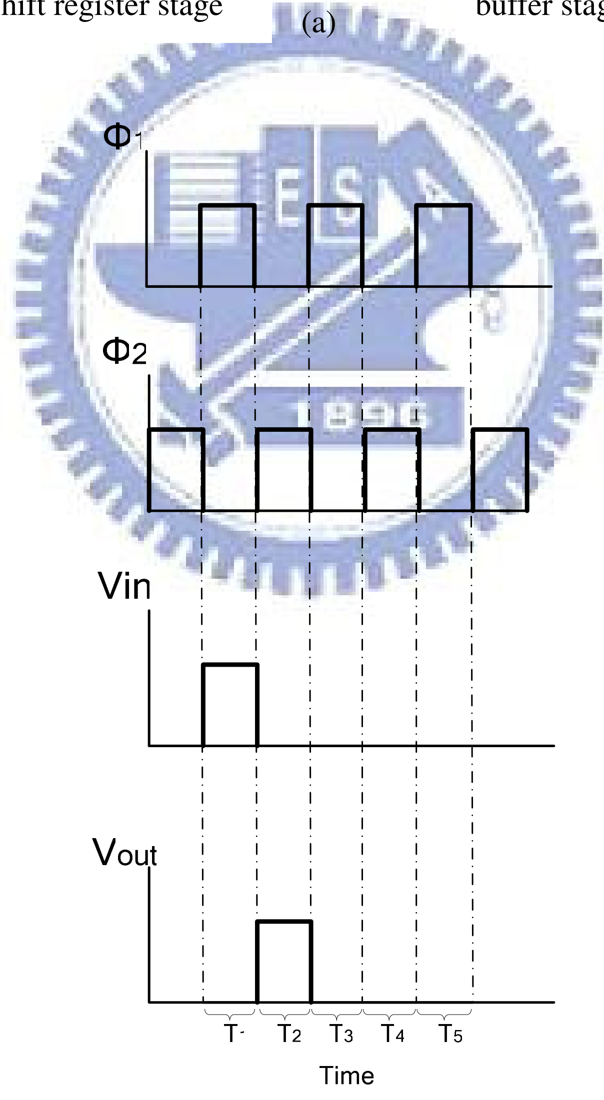
Fig. 3.1-3 The simulated results at some nodes in LPDV ASGD.

Table 3.1-1 Stress conditions for every TFT in LPDV ASGD. (50%) means the 0.5 duty ratio and (25%) means the 0.25 duty ratio.

TFT	Vgs (V)	Vds(V)	AC/DC	ΔVt Tolerance
M1	-3/+30 (50%)	-3/0 (50%)	AC	6.5V
M2	+5/+27 (50%)	0/+5 (50%)	AC	6.5V
M3	-6/+2 (50%)	0/+30 (50%)	AC	- 3V
M4	-3/0 (25%)	0.8/+1 (25%)	AC	>15V
M5	+3/+30 (25%)	0/+3 (25%)	AC	>15V
M6	0/+30 (25%)	0/+0.6 (25%)	AC	>15V
M7	0	+10	DC	- 5V
M8	+10	0	DC	4V
M9	+0.6	+40	DC	- 3.5V
M10	0	0	DC	>15V
M11	+0.3	+0.3	DC	4V



(a)



(b)

Fig. 3.2-1 The proposed scan driver cricuit ALPDV ASGD . (a) schematics (b) clock driving scheme

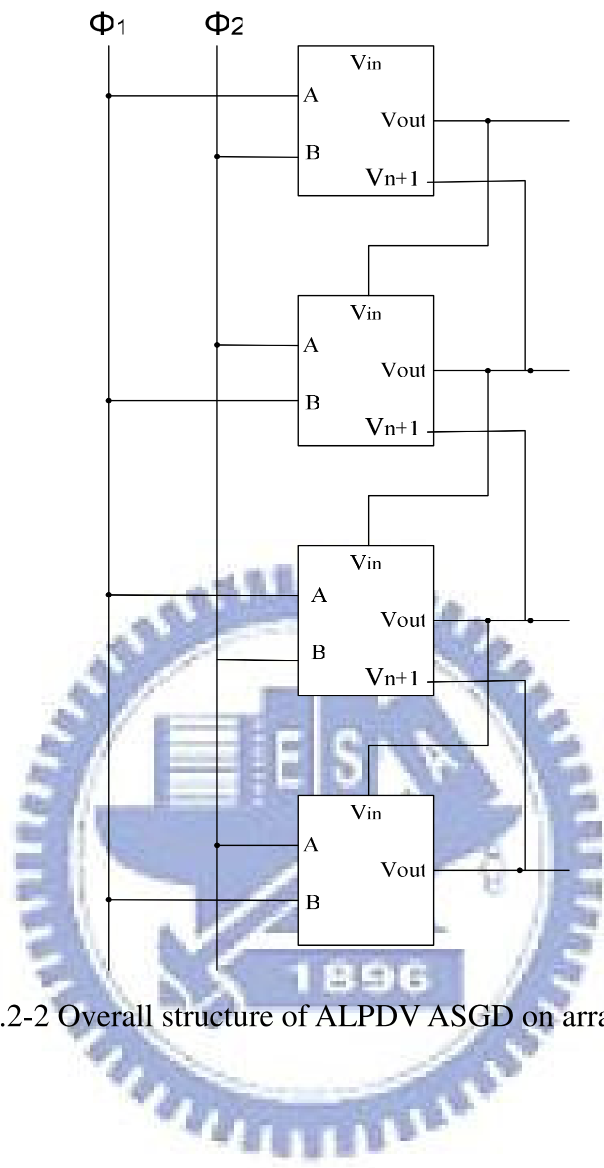


Fig. 3.2-2 Overall structure of ALPDV ASGD on array panel.

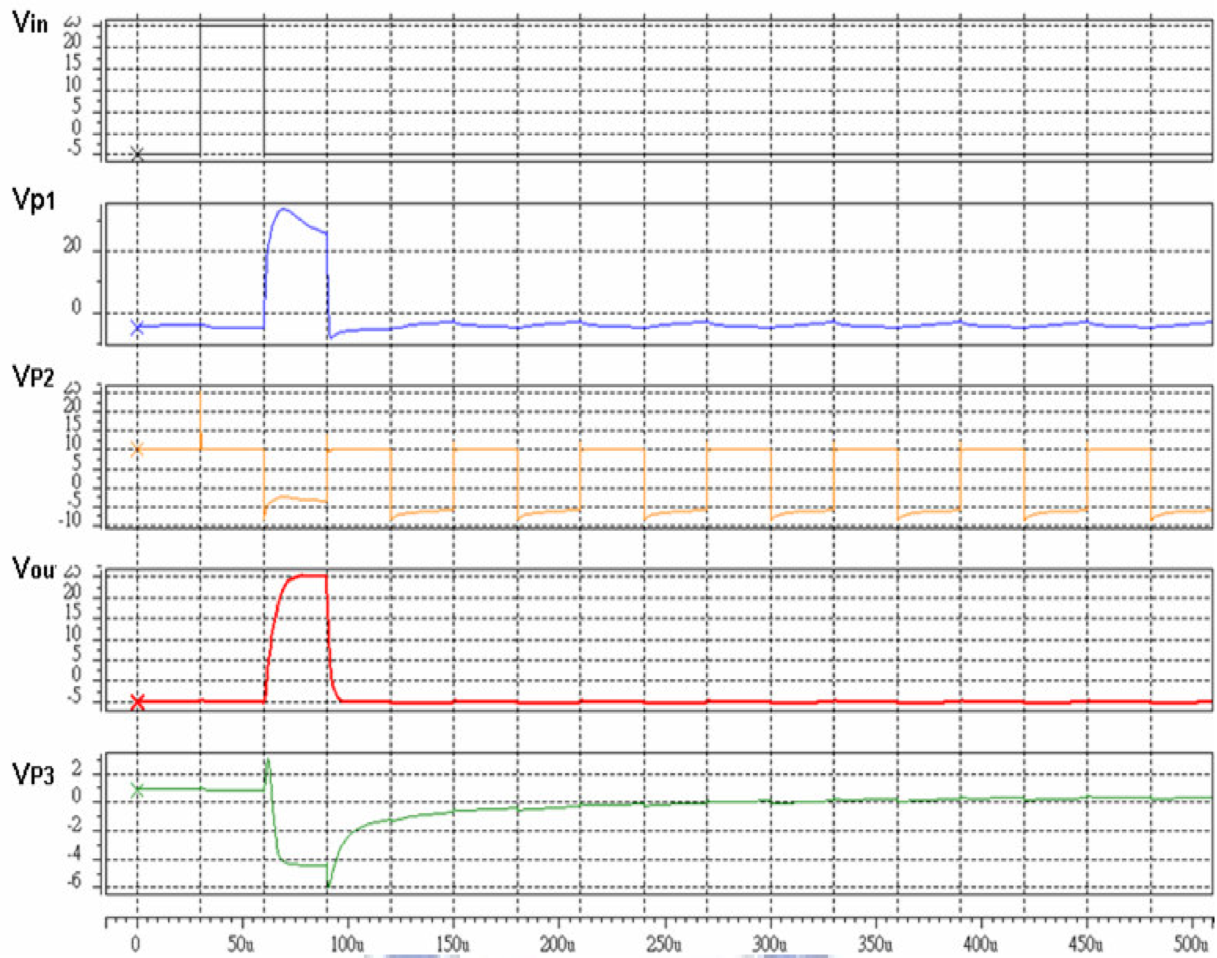
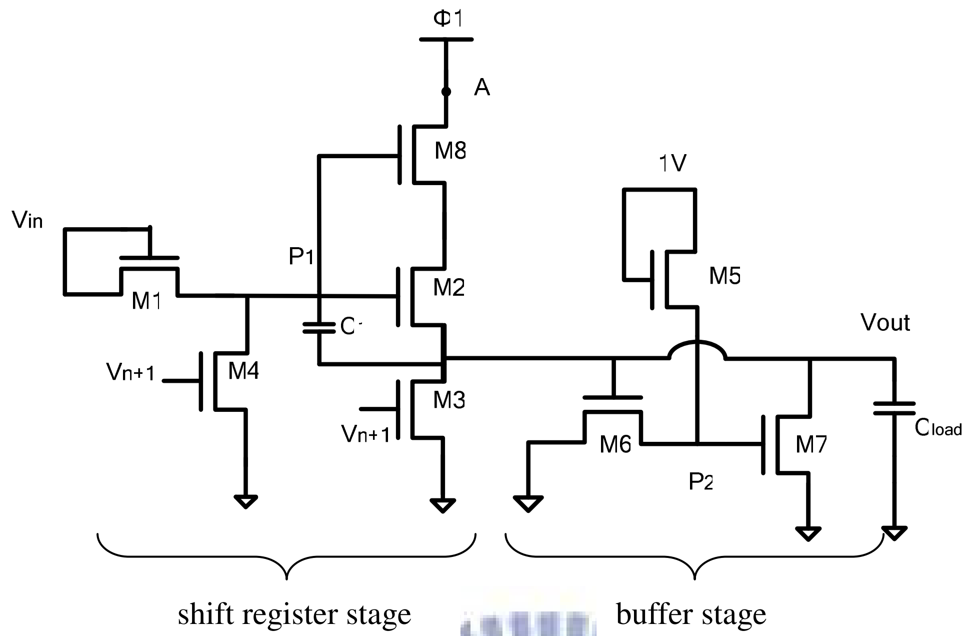


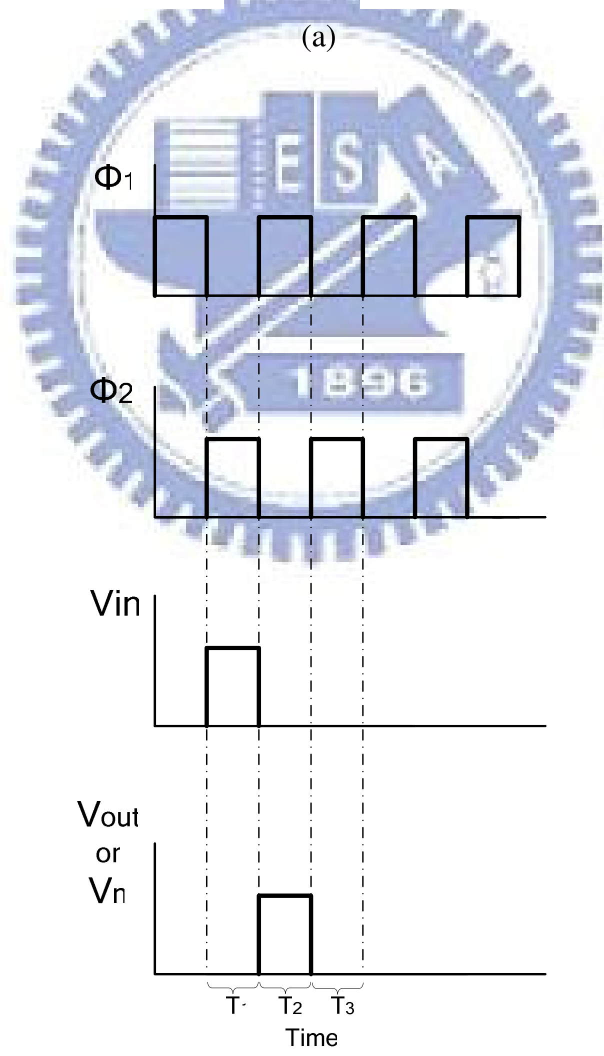
Fig. 3.2-3 The simulated results at some nodes in ALPDV ASGD.

Table 3.2-1 Stress conditions for every TFT in ALPDV ASGD. (50%) means the 0.5 duty ratio.

TFT	Vgs (V)	Vds(V)	AC/DC	ΔVt Tolerance
M1	-3.37/+30 (50%)	-3.35/+0.01 (50%)	AC	7V
M2	-0.03/+3.03 (50%)	0/+29.6 (50%)	AC	- 4V
M3	-1.37/+15 (50%)	-0.15/+2.29 (50%)	AC	10V
M4	+1.42/+15 (50%)	-0.01/+16.4 (50%)	AC	7V
M5	+0.15/+0.26 (50%)	+0.15/+0.26 (50%)	AC(～DC)	>15V
M6	+5.7/+5.82 (50%)	0/+0.33 (50%)	AC (～DC)	>10V
M7	0/+0.33 (50%)	+5.7/+5.82 (50%)	AC (～DC)	15V



(a)



(b)

Fig. 3.3-1 The proposed scan driver cricuit RLPDV ASGD . (a) schematics (b) clock driving scheme

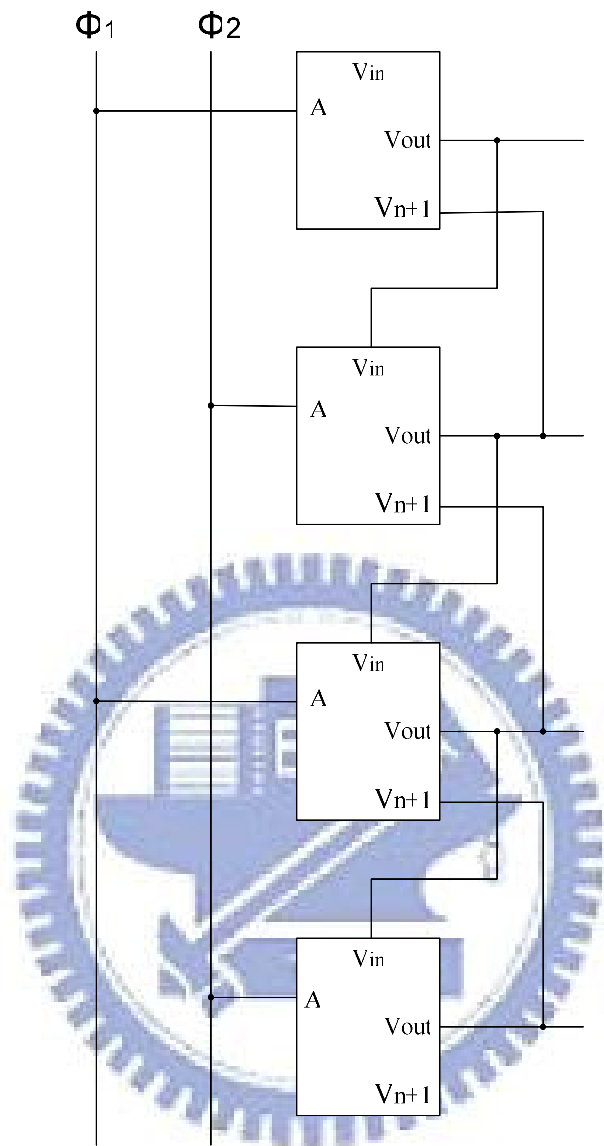


Fig. 3.3-2 Overall structure of RLPDV ASGD on array panel.

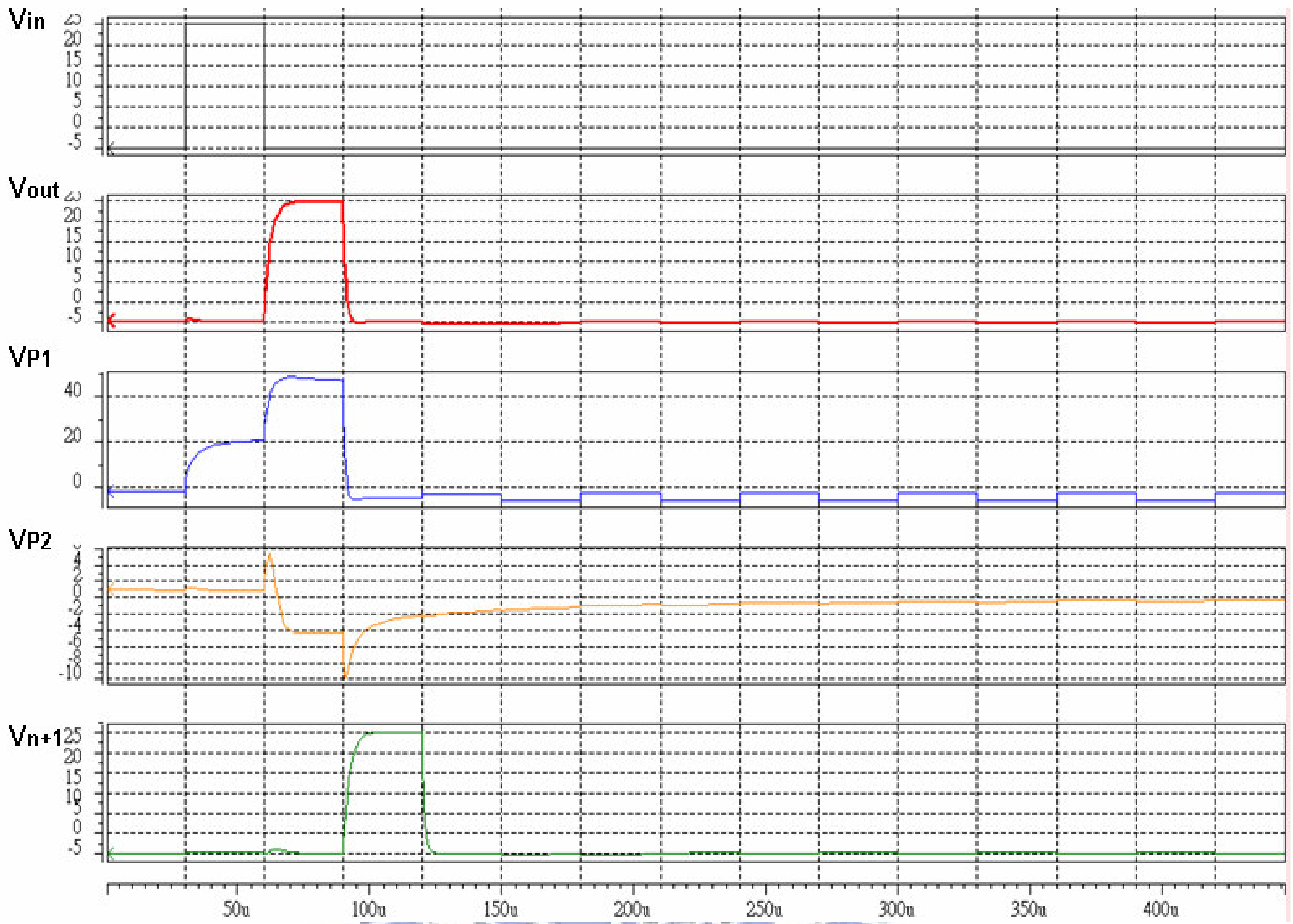
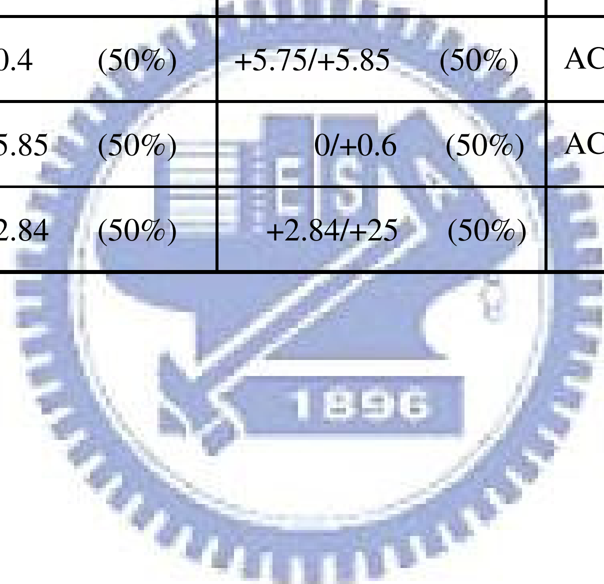


Fig. 3.3-3 The simulated results at some nodes in RLPDV ASGD.

Table 3.3-1 Stress conditions for every TFT in RLPDV ASGD. (50%) means the 0.5 duty ratio.

TFT	Vgs (V)	Vds(V)	AC/DC	△Vt Tolerance
M1	-2.89/+0.56 (50%)	-2.89/+0.56 (50%)	AC	12V
M2	-0.014/+5.47 (50%)	+ 0.466/+5.94 (50%)	AC	12V
M3	0	0/0.36 (50%)	AC	12V
M4	0	-0.55/+2.92 (50%)	AC	>15V
M5	+5.62/+5.95 (50%)	+5.62/+5.95 (50%)	AC (～DC)	4V
M6	+0.06+/0.4 (50%)	+5.75/+5.85 (50%)	AC (～DC)	>15V
M7	+5.75/+5.85 (50%)	0/+0.6 (50%)	AC (～DC)	4V
M8	+1.17/+2.84 (50%)	+2.84/+25 (50%)	AC	- 8V



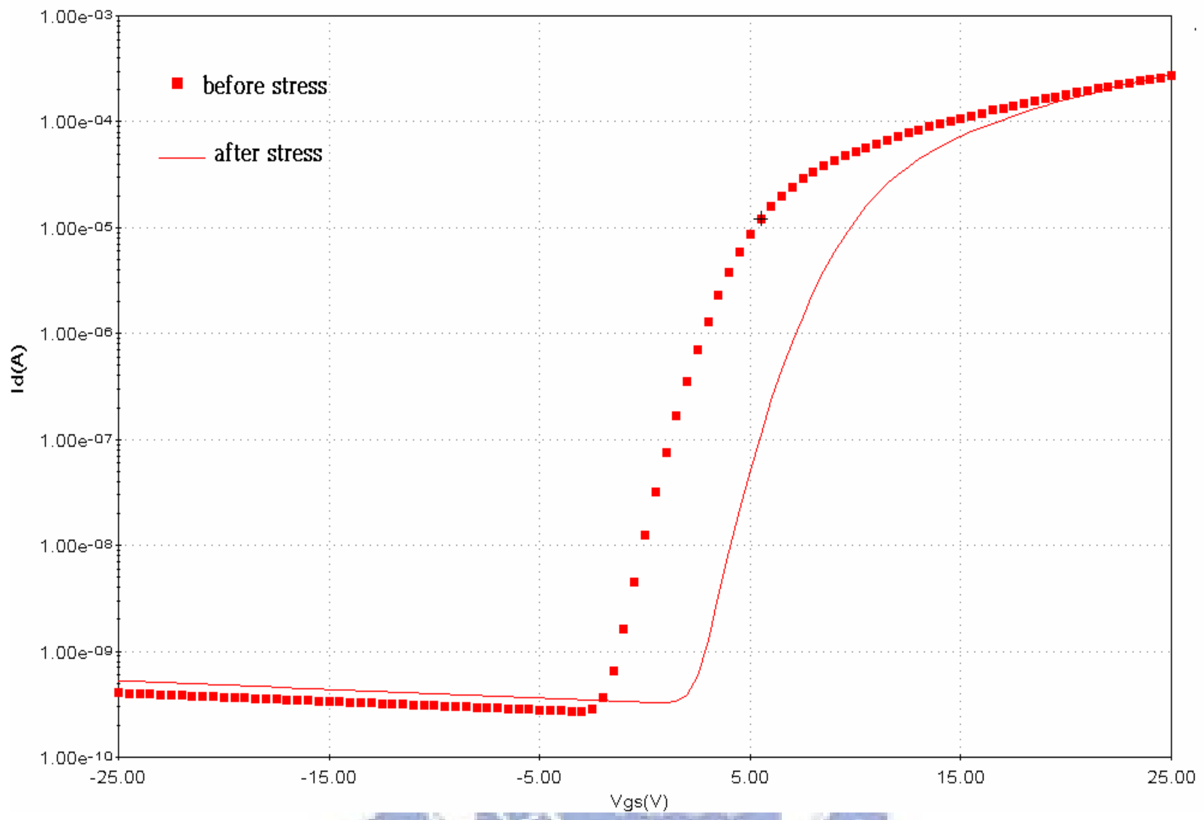


Fig. 3.4-1 The simulated Id-Vg curve of a-Si TFT for $\Delta V_T = 4V$.

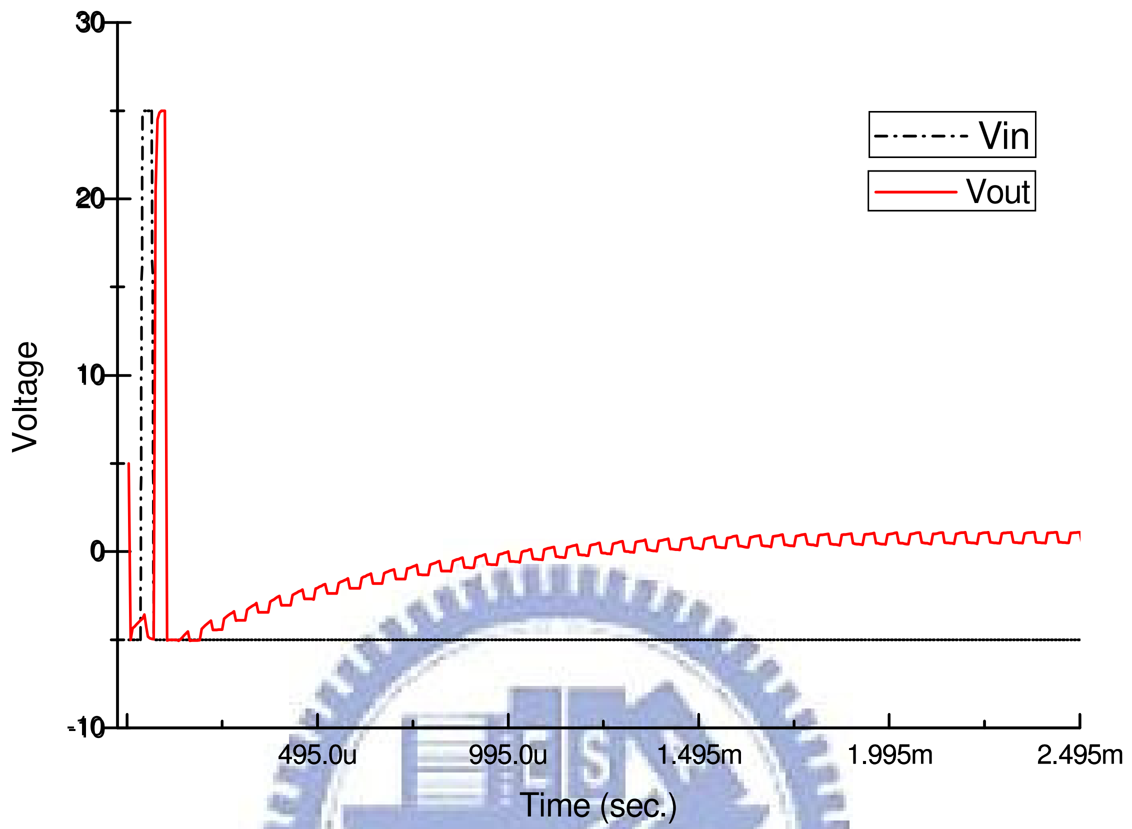
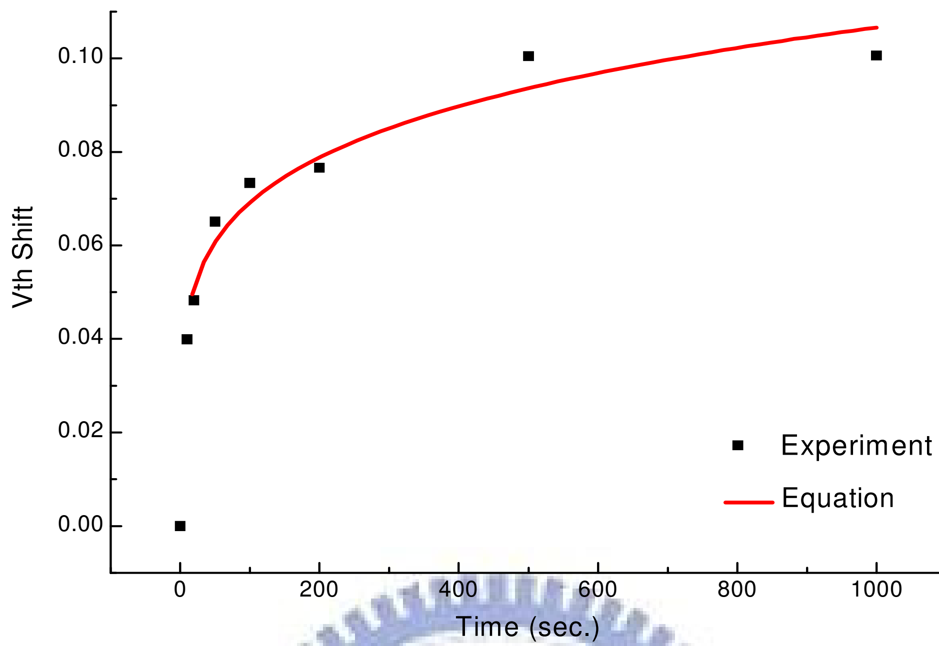


Fig. 3.4-2 The simulated result of proposed circuit RLPDV ASGD when the threshold shift of M_5 and M_7 is 4V.



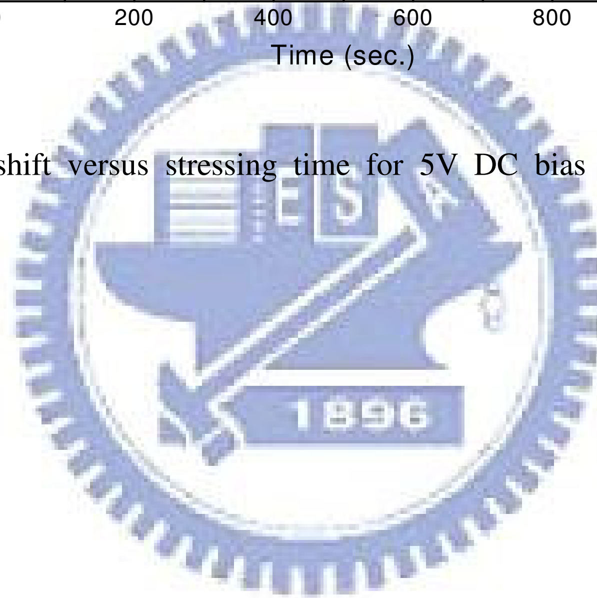

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Fig. 3.4-3 Vth shift versus stressing time for 5V DC bias and fitting curve of formula .

Table 3.4-1 Extracted parameters from ΔV_T induced by positive 5V DC bias-stress.

Vgs	A	α	β
5V (DC)	0.01	2.0763	0.18786

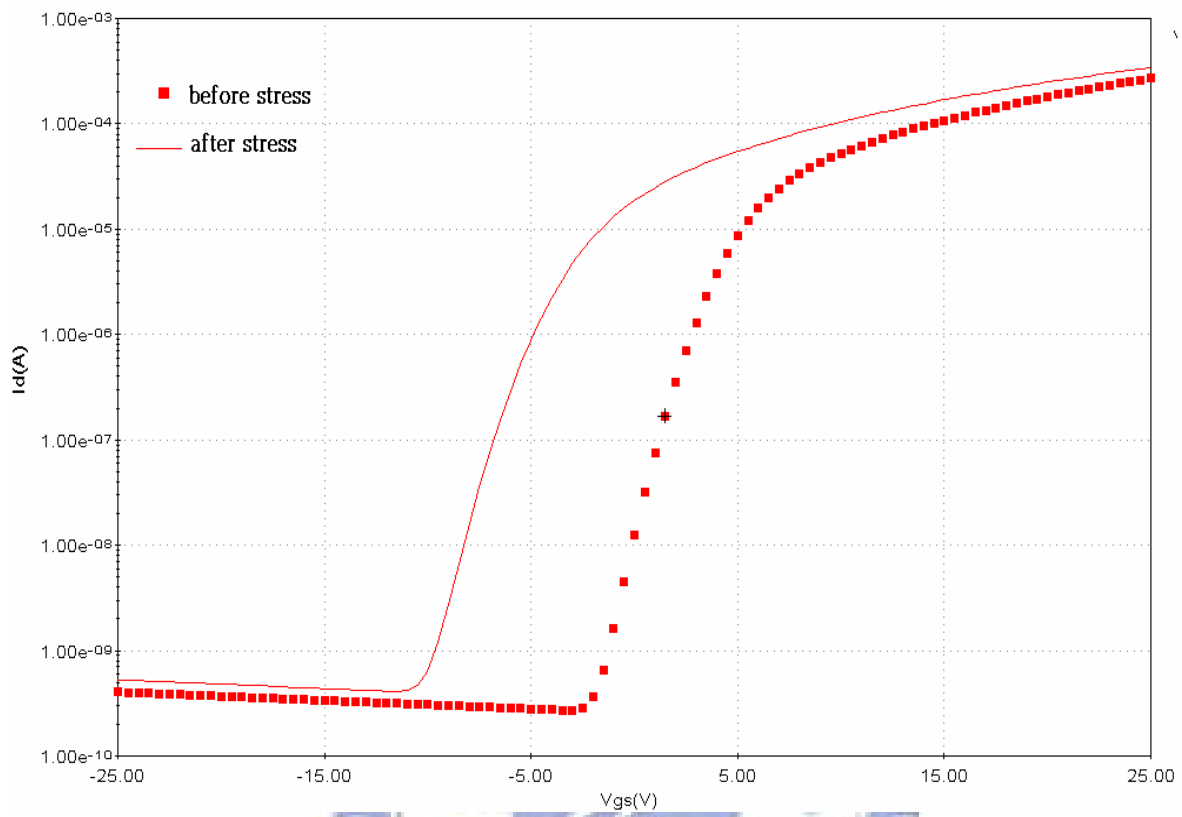

Fig. 3.4-4 The simulated Id-Vg curve of a-Si TFT for ΔV_T = -8V.

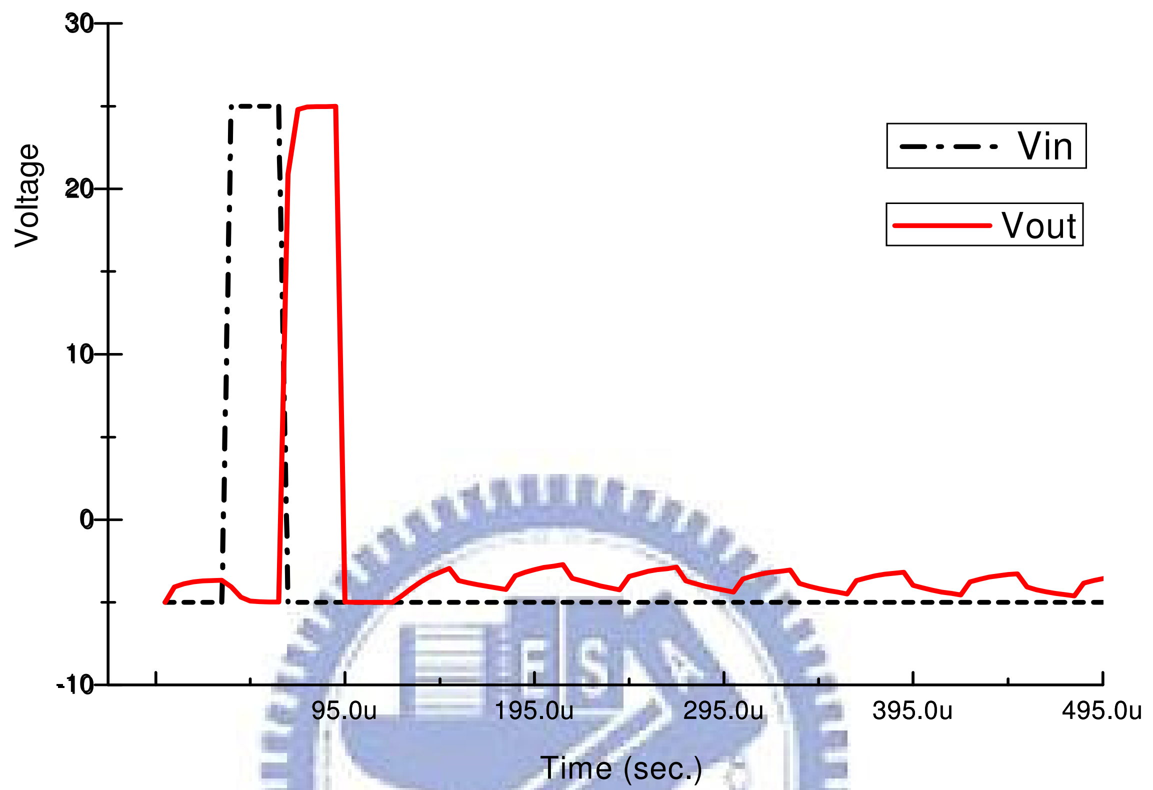

Fig. 3.4-5 The simulated result of proposed circuit RLPDV ASGD when the threshold shift of M_8 is -8V.

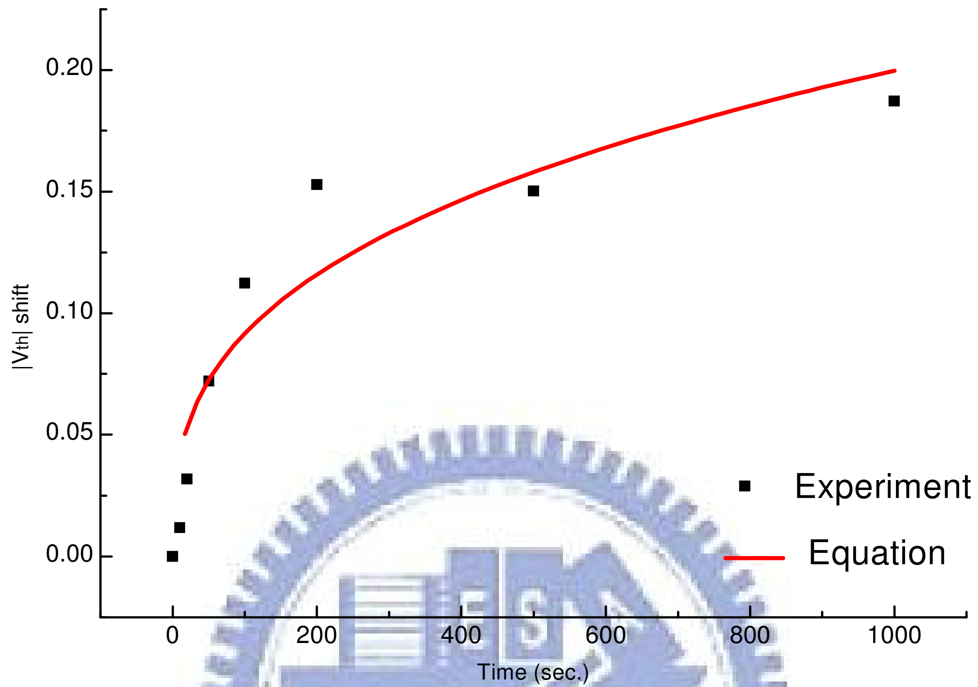

Fig. 3.4-6 |Vth| shift versus stressing time for -20V AC bias and fitting curve of formula.

Table 3.4-2 Extracted parameters from ΔV_T induced by positive -20V AC bias-stress.

Vgd	A^-	α^-	β^-	Dc
-20V (AC-33KHz)	2×10^{-4}	1.737	0.33835	0.5

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