Investigation on Board-Level CDM ESD Issue in IC Products

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***Abstract*—The impacts caused by board-level charged-device-model (CDM) electrostatic-discharge (ESD) events on integrated-circuit products are investigated in this paper. The mechanism of board-level CDM ESD event is introduced first. Based on this mechanism, an experiment is performed to investigate the board-level CDM ESD current waveforms under different sizes of printed circuit boards (PCBs), charged voltages, and series resistances in the discharging path. Experimental results show that the discharging current strongly depends on the PCB size, charged voltage, and series resistance. Moreover, the chip- and board-level CDM ESD levels of several test devices and test circuits fabricated in CMOS processes are characterized and compared. The test results show that the board-level CDM ESD level of the test circuit is lower than the chip-level CDM ESD level of the test circuit, which demonstrates that the board-level CDM ESD event is more critical than the chip-level CDM ESD event. In addition, failure analysis reveals that the failure in the test circuit under board-level CDM ESD test is much severer than that under chip-level CDM ESD test.**

***Index Terms*—Board-level charged-device model (CDM), chip-level CDM, electrostatic discharge (ESD), failure analysis.**

I. Introduction

With THE advance of CMOS processes, integrated circuits (ICs) have been fabricated with thinner gate oxides to achieve higher speed and lower power consumption. However, electrostatic discharge (ESD) was not scaled down with CMOS technology. Thus, ESD protection design in nanoscale CMOS processes becomes a challenging task. Among the three component-level (or called as chip-level) ESD test standards, which are human-body model (HBM) [1], machine model (MM) [2], and charged-device model (CDM) [3], [4], CDM becomes more and more critical because of the thinner gate oxide in nanoscale CMOS devices and the larger die size for the application of system on chip (SoC). The thinner gate oxide causes a lower gate-oxide breakdown voltage, and an IC with larger die size can store more static charges, which leads to larger discharging current during CDM ESD events. CDM ESD current has the features of huge peak current and short duration. Furthermore, CDM ESD current flows from the chip substrate to the external ground, whereas HBM and MM ESD currents are injected from the external ESD source into the zapped pin. Thus, effective on-chip ESD protection design against CDM ESD stresses has become more challenging to be implemented.

Aside from the chip-level CDM ESD issue, the board-level CDM ESD issue becomes more important recently, because it often causes the ICs to be damaged after the IC is installed to the circuit board of electronic system. For example, board-level CDM ESD events often occur during the module function test on the circuit board of electronic system. Even though the IC has been designed with good chip-level ESD robustness, it could have a reduced CDM level in board-level CDM ESD test. The reason is that the discharging current during the board-level CDM ESD event is significantly larger than that of the chip-level CDM ESD event. There are several papers addressing the phenomenon of board-level CDM ESD events on IC products [5]–[8]. In previous works, the ICs which already passed the component-level ESD specifications were still returned by customers because of ESD failure. After performing the field-induced CDM ESD test on the ICs which have been mounted on the printed circuit board (PCB), the failure is the same as that happened in the customer-returned ICs. This indicates that the real-world charged-board-model (CBM) ESD damage can be duplicated by the board-level CDM ESD test [5], [6]. The previous works have demonstrated that the board-level CDM ESD events indeed exist, which should be taken into consideration for all IC products.

In this paper, the board-level CDM ESD issue for ICs is comprehensively addressed [9]. The mechanisms of both chip- and board-level CDM ESD events are developed and compared in Section II. The discharging current waveforms during board-level CDM ESD events under different measurement conditions are investigated in Section III. The chip- and board-level CDM ESD stresses are applied to some test devices and test circuits in Section IV. Moreover, failure analysis is also performed to investigate the difference between the failure mechanisms under chip- and board-level CDM ESD tests.

II. CDM ESD Events

A. Chip-Level CDM ESD Event

During the assembly of IC products, charges could be stored within the body of IC products due to induction or tribocharging. Once a certain pin of the IC is suddenly grounded, the static charges originally stored within the IC will be discharged through the grounded pin, which is called the CDM ESD event and is shown in Fig. 1. The CDM ESD event delivers a large amount of current in a very short time. There are many situations that the pins of an IC are grounded. An example is

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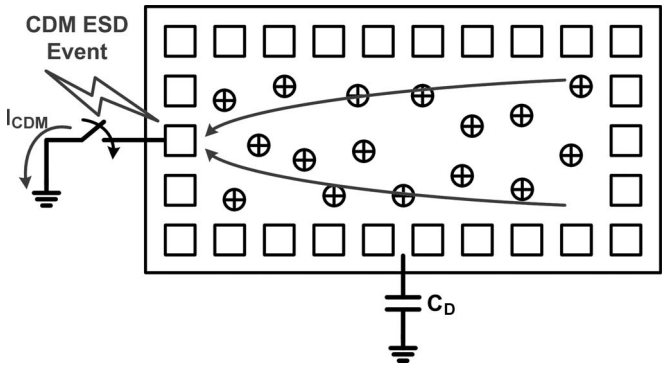


Fig. 1. CDM ESD event: When a certain pin is grounded, the stored charges in the IC will be quickly discharged through the grounded pin.

when the pin touches the grounded metallic surface or the pin is touched by the grounded metallic tools. Different ICs have different die sizes, so their equivalent parasitic capacitances (C_D) are totally different from one another. Thus, different ICs have different peak currents and robustness under CDM ESD tests. When a device under test (DUT) with the equivalent capacitance of 4 pF is under 1-kV CDM ESD test, the CDM ESD current rises to more than 15 A in 50–200 ps [10]. As compared with HBM and MM ESD events, the discharging current in CDM ESD event is not only larger but also faster. Since the duration of CDM ESD event is much shorter than that of HBM and MM ESD events, the IC may be damaged during CDM ESD events before the ESD protection circuit is turned on. The capacitor becomes a low-impedance device when the signal frequency is increased. Thus, the CDM ESD current is most likely to flow through the capacitive structures in ICs. In CMOS ICs, the gate oxides of MOS transistors are capacitive structures, so the gate oxide is most likely to be damaged under CDM ESD events. In nanoscale CMOS processes, the gate-oxide thickness becomes thinner, which makes the equivalent capacitance per unit area larger. Consequently, the gate oxides of MOS transistors in nanoscale CMOS processes are more vulnerable to CDM ESD stresses. Furthermore, since more functions are integrated into a single chip, this makes the die size larger. Under the same charged voltage, larger capacitance stores more static charges, so the CDM ESD current is larger with larger DUT capacitance. Since larger die size denotes larger equivalent capacitance, the CDM ESD current is larger for ICs with larger die sizes. Therefore, with larger die size and MOS transistors using thinner gate oxide, nanoscale CMOS ICs are very sensitive to ESD, particularly CDM ESD events.

During the manufacturing of IC products, some of the steps had been reported to cause chip-level CDM ESD events, which leads to yield loss. There are several works addressing the cause of chip-level CDM ESD events during manufacturing of IC products [11]–[13]. In the packaging process of plastic-leaded-chip-carrier packages, the chips are induced to store static charges when they are carried by the carrier of the machine. When a certain pin of the charged chip is connected to the external ground, a CDM ESD event may occur. To solve this problem, the balanced ionizer can be utilized in the manufacturing environment to neutralize the static charges stored in the chips and the machines [11].

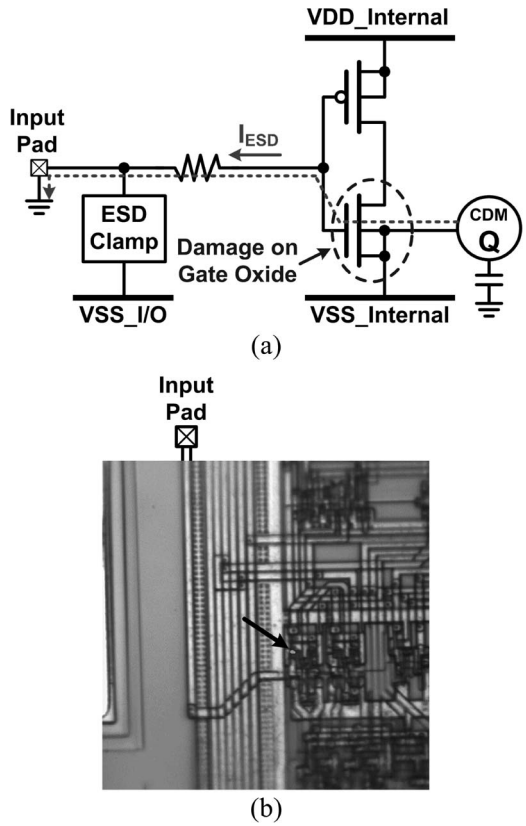


Fig. 2. (a) CDM ESD current path in an input buffer. (b) Failure point is located at the gate oxide of the input NMOS.

An IC fabricated in a 0.8-μm CMOS process had been found to have leakage current when it was normally biased, but it worked well during the function test after fabrication. Failure analysis demonstrated that the gate oxide of the NMOS in the input buffer was damaged by the CDM ESD event. After the study, it was found that the socket of the IC tester was charged during the function test, which induced the tested IC to store static charges. After finishing the function test, the charged IC was placed on the grounded metallic table, and the CDM ESD event occurred to damage the IC which passed the function test [12].

During fabrication of ICs, separating the tape and die after cutting the die from the wafer causes substantial charge accumulation in the die. Measured by the Faraday cup, it was reported that the CDM ESD voltage could be more than 1000 V during the separation of the tape and die. Such a high CDM ESD voltage may damage the IC product [13].

B. Case Study on Chip-Level CDM ESD Damage

An input buffer fabricated in a 0.8-μm CMOS process is shown in Fig. 2(a). This chip passes the 2-kV HBM and 200-V MM ESD tests. Although this chip is equipped with ESD protection circuit at its input pad, it is still damaged after the 1000-V CDM ESD test. As shown in Fig. 2(b), the failure point after the CDM ESD test is located at the gate oxide of the NMOS in the input buffer. Due to consideration of noise isolation between I/O cells and internal circuits, the VSS of I/O cells (VSS_I/O) and the VSS of internal circuits (VSS_Internal)

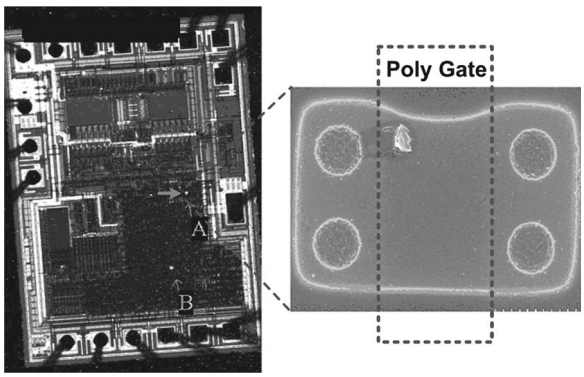


Fig. 3. After the chip-level CDM ESD test, the failure point is located at the gate oxide of an NMOS in the internal circuit.

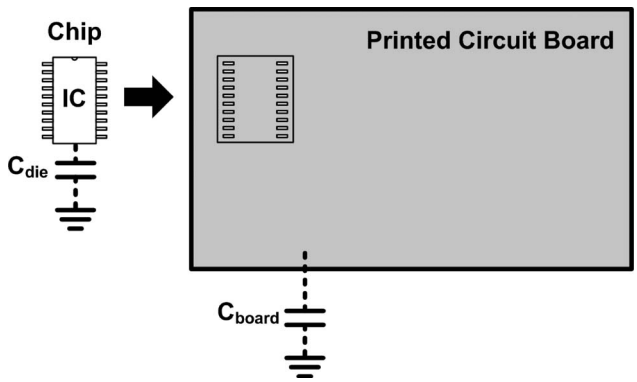


Fig. 4. Charges stored in the PCB and the charges stored in chip will be redistributed when the chip is attached to the PCB.

are separated in the chip layout. As a result, the ESD clamp device at the input pad cannot effectively protect the gate oxide during CDM ESD stresses, because there is no connection between VSS_I/O and VSS_Internal. The CDM ESD current which damages the gate oxide of NMOS is shown by the dash line in Fig. 2(a). Fig. 3 is the failure photograph of another IC after the CDM ESD stress test. This IC was fabricated in a 0.5-μm CMOS process. The scanning-electron-microscope (SEM) photograph had proven that the failure caused by the CDM ESD event is located at the poly gate of a MOS transistor in the internal circuit that is connected to some input pad. In these two aforementioned cases, the charges stored in the body of the chip still flow through the gate terminal of the input MOS transistor in the internal circuits to damage its gate oxide during CDM ESD stresses, even though the ESD protection circuit has been applied to the input pad. According to previous works, the pins near the corners in IC products are more prone to suffer CDM ESD events, because the corner pins are usually first touched by the external ground during transportation or assembly [14]. Therefore, in addition to HBM and MM ESD protection, how to design an efficient CDM ESD protection circuit for IC products is another important consideration in component-level ESD protection design.

C. Board-Level CDM ESD Event

In microelectronic systems, IC chips must be attached to the PCB. Before the attachment, static charges could be stored in

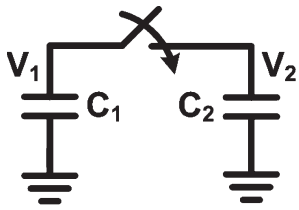


Fig. 5. When two capacitors with different voltages are shorted, charge redistribution will occur.

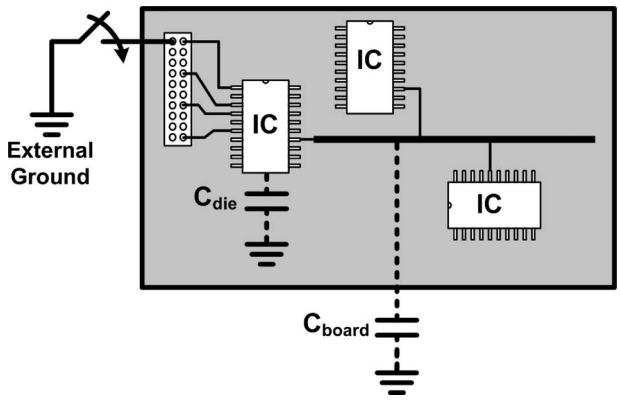


Fig. 6. When a certain pin of the PCB is grounded during the function test, huge current will flow from the PCB to the IC.

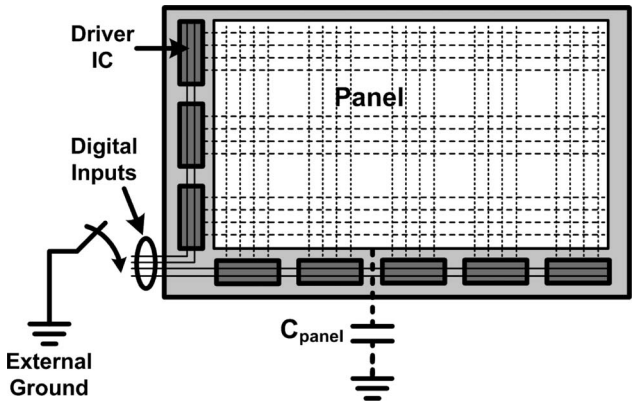


Fig. 7. When the driver IC is attached to the LCD panel during manufacturing, the charges originally stored in the LCD panel will be transferred to the driver IC, which causes the board-level CDM ESD event. During the function test, connecting the pins of the driver IC to ground will also induce the board-level CDM ESD event.

the substrate of the chip or the metal traces on the dielectric layer in the PCB. During the attachment, the static charges originally stored in the IC chip and the PCB will be redistributed, as shown in Fig. 4. Fig. 5 shows the charge redistribution mechanism. C_1 and C_2 denote the parasitic capacitances of the IC chip and the PCB, respectively. Usually, C_2 is much larger than C_1. The initial voltages across C_1 and C_2 are V_1 and V_2, respectively. C_1 and C_2 are not connected in the beginning. When the IC chip is attached to the PCB, C_1 and C_2 are shorted. Consequently, the voltages across C_1 and C_2 will become $(C_1 \times V_1 + C_2 \times V_2)/(C_1 + C_2)$ after they are connected together. The instantaneous current during the attachment of the IC chip to the PCB will be increased if the initial voltage difference between the IC chip and the PCB is increased. The instantaneous current during the charge redistribution may be larger

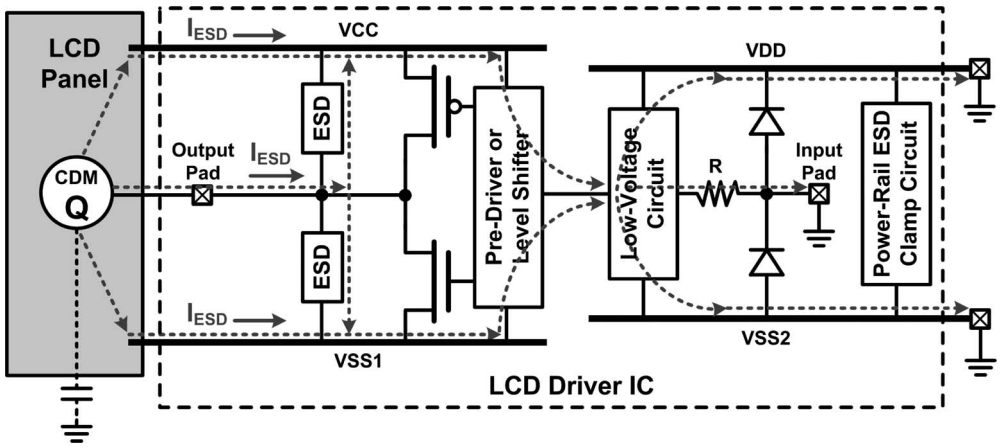


Fig. 8. When the pins of the driver IC are grounded, the board-level CDM ESD current will flow from the LCD panel to the interface circuits within the driver IC to the grounded pins.

than 10 A, which can easily damage the IC to cause a CDM-like failure. This is one of the examples of board-level CDM ESD events. Moreover, installing the modules to the system during the assembly of microelectronic products also causes board-level CDM ESD events. To mitigate this impact, the balanced ionizer can be utilized in the manufacturing environment to neutralize the static charges stored in the chips and PCBs.

After the chips are attached to the PCB, certain pins in the PCB may be connected to low potential or grounded during the module function test, as shown in Fig. 6. In this situation, the charges originally stored in the chips and the PCB will be quickly discharged through the grounded pin to damage the chips on the PCB. If the voltages across the equivalent capacitances of the chips and PCB are larger, more charges are stored, which leads to larger discharging current. To solve this problem, ESD dischargers consisting of large resistances (approximately in megaohms) can be used to ground the pins of the PCB before the module function test. Although there is still current flowing through the chips, the current peak can be significantly reduced by the large series resistance. As a result, the chip can be protected from being damaged by the board-level CDM ESD event during the module function test.

In the assembly and testing of LCD monitor, board-level CDM ESD events may often occur, too. As shown in Fig. 7, when the driver ICs are attached to the LCD panel, charge transfer occurs, which causes board-level CDM ESD current flowing between the driver ICs and LCD panel to damage them. Moreover, the driver IC can be also damaged by such board-level CDM ESD events when a certain pin of the driver IC on the panel is connected to ground during the panel function test. The charges stored in the LCD panel will be discharged through the pins of the driver ICs to the external ground during the panel function test. The ESD current paths are shown by the dash lines in Fig. 8. Since the on-glass thin-film transistors in the LCD panel have higher operation voltage than that of most digital ICs, the core circuits and I/O cells of LCD driver ICs have different operation voltages. Such ICs with multiple power domains have individual power pads and ground pads for each power domain. Once the aforementioned board-level CDM ESD events occur, ESD current will flow from the LCD panel through the output pad of the driver IC into the driver IC. Although ESD protection circuits have been applied to each output pad of the driver IC to bypass ESD current to the power pad (VCC) or ground pad (VSS1) within the power domain, the interface circuits between different power domains are often damaged during such board-level CDM ESD events due to the disconnection between the power pads or ground pads in different power domains. To solve this problem, ESD protection devices should be inserted between the power pads or ground pads in different power domains to provide ESD current paths between the separated power domains [15].

III. Dependence of Current Waveforms on the Board Size in Board-Level CDM ESD Event

Recently, the simulation of CBM ESD event had been performed to evaluate the discharging current under different charged-board dimensions [16]. In this section, different PCB sizes, charged voltages, and series resistances in the discharging path are measured to explore their effects on board-level CDM ESD events.

A. Discharging Without Series Resistor

In the board-level CDM ESD event, ESD current is discharged from the charged PCB to the grounded pin of the chip on the PCB. To emulate the board-level CDM ESD event, the measurement setup with the two-sided PCB shown in Fig. 9 was utilized in this paper. The top side of the PCB was charged with some potential level, whereas the bottom side of the PCB was relatively grounded. Four PCB sizes are used in the experiment, which are the A4 size (30 cm $\times$ 20 cm), 1/2 A4 size (20 cm $\times$ 15 cm), 1/4 A4 size (15 cm $\times$ 10 cm), and 1/8 A4 size (10 cm $\times$ 7.5 cm). The charged voltage ranges from 20 to 600 V. With the identical dielectric thickness, the capacitances of the PCBs are linearly proportional to the size of the PCB. The capacitances of the A4-, 1/2-A4-, 1/4-A4-, and 1/8-A4-sized PCBs in this paper are 1.94 nF, 970 pF, 485 pF, and 242.5 pF, respectively. The top side of the PCB was charged by the curve tracer through a 10-MΩ resistor, which was used to limit the charging current. A multimeter was used to monitor the charged voltage on the top side of the PCB. After the top side of the PCB was charged to some specified voltage level, it was grounded manually, and the

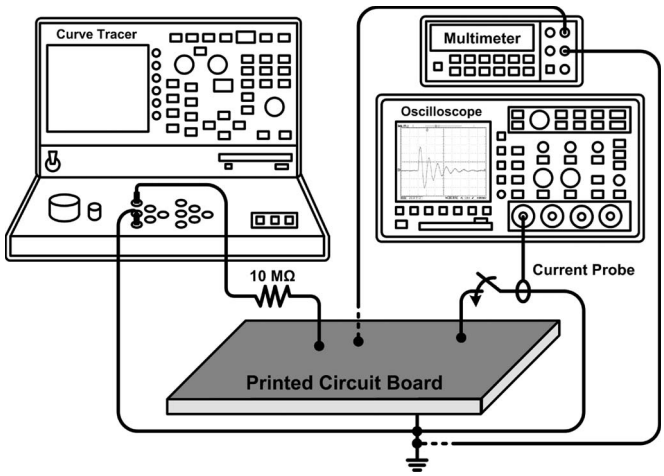


Fig. 9. Experimental setup to investigate the current waveforms under board-level CDM ESD events.

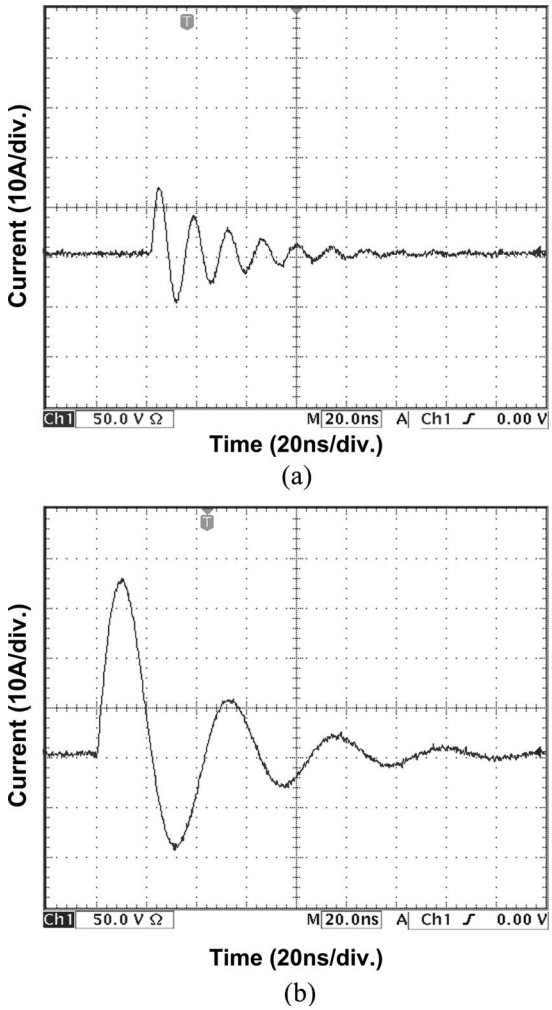


Fig. 10. Measured board-level CDM ESD current waveforms from (a) 1/8-A4-sized PCB and (b) A4-sized PCB under 100-V charged voltage.

discharging current waveform was observed by the oscilloscope with the current probe.

The measured discharging current waveforms from the 1/8-A4- and A4-sized PCB under the charged voltage of 100 V are shown in Fig. 10(a) and (b), respectively. Under the charged

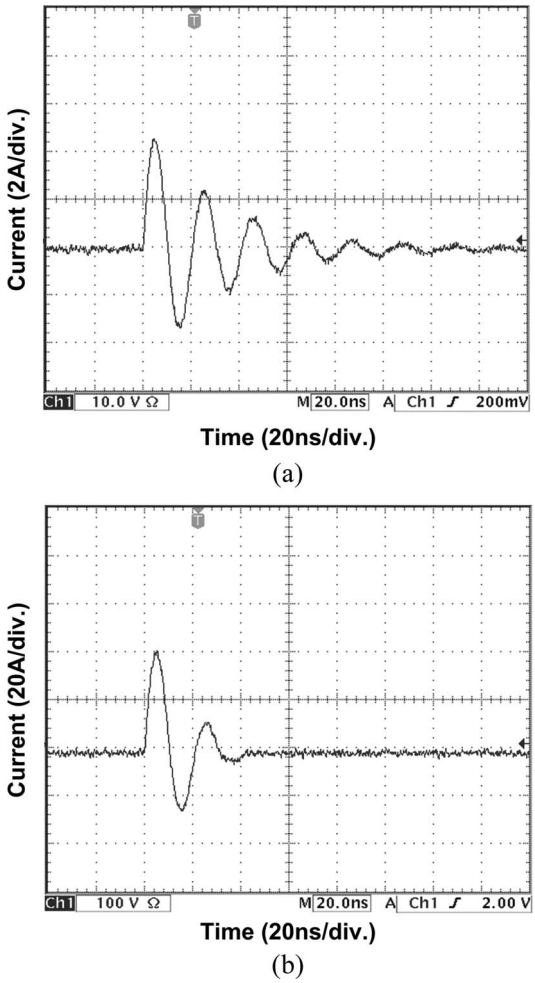


Fig. 11. Measured board-level CDM ESD current waveforms from 1/4-A4-sized PCB under (a) 20-V and (b) 200-V charged voltages.

voltage of 100 V, the peak discharging currents of the 1/8-A4- and A4-sized PCBs are 14 and 36 A, respectively. With the same PCB size of 1/4 A4, the measured discharging current waveforms under the charged voltages of 20 and 200 V are shown in Fig. 11(a) and (b), respectively. The peak discharging current from the 1/4-A4-sized PCB is increased from 4.4 A (under the charged voltage of 20 V) to 42 A (under the charged voltage of 200 V). The peak discharging currents under different PCB sizes and different charged voltages are compared in Fig. 12. Under the same PCB size, higher charged voltage leads to larger peak discharging current. Under the same charged voltage, larger PCB provides larger peak current since larger PCB has larger capacitance, which can store more charges in the PCB. Without the series resistor along the discharging path, all of the discharging current waveforms exhibit underdamped sinewavelike characteristics.

B. Discharging With Series Resistor

In the board-level CDM ESD experiment without the series resistor, the peak discharging currents are quite large. To reduce the peak discharging current, a series resistor was inserted along the discharging path to investigate the reduction on the discharging current, as shown in Fig. 13. The series resistances

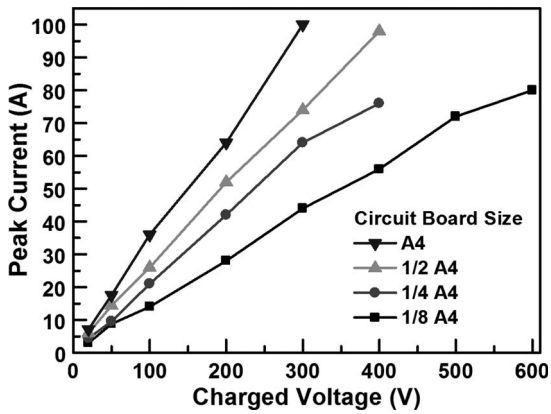


Fig. 12. Board-level CDM ESD peak currents under different charged voltages and different PCB sizes.

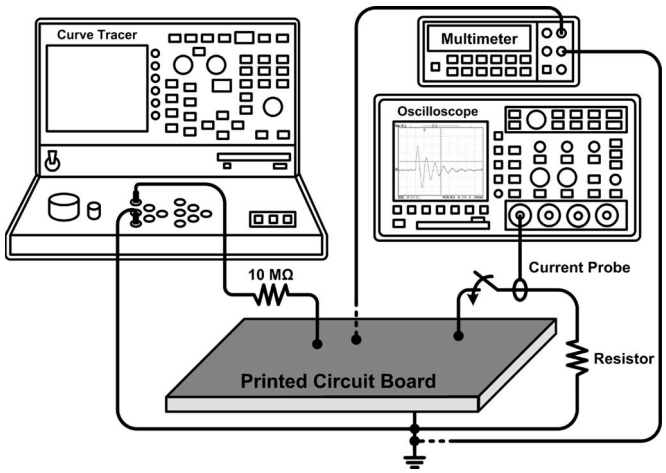
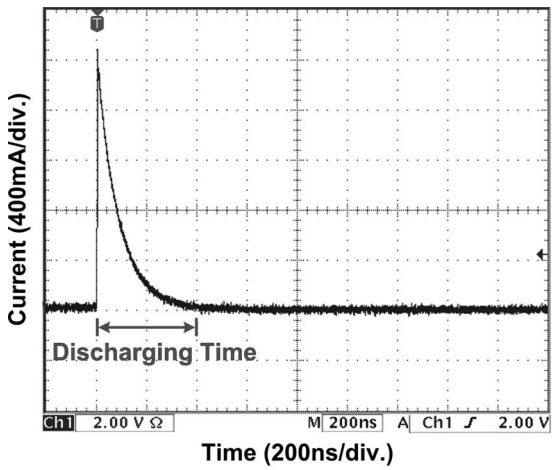
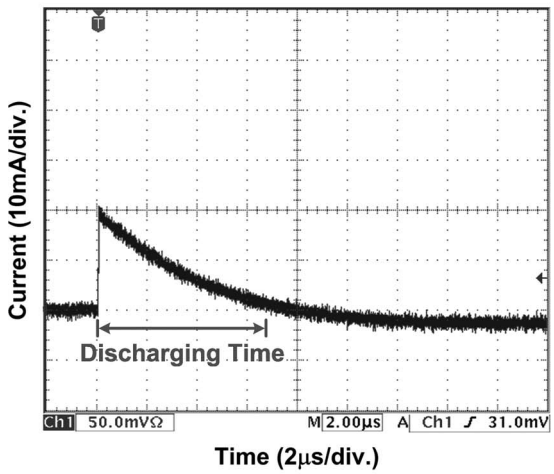


Fig. 13. Experimental setup to investigate the current waveforms under board-level CDM ESD events with a series resistor along the discharging current path.

ranging from 10 Ω to 100 kΩ are used in this paper. With this measurement setup, the dependence of the discharging current on series resistance can be investigated. Fig. 14(a) and (b) shows the measured discharging current waveforms of the 1/2-A4-sized PCB with 100-Ω and 10-kΩ series resistances under 100-V charged voltage, respectively. As compared with the same PCB size and charged voltage without series resistance, the peak discharging currents with the series resistances of 100 Ω and 10 kΩ were reduced from 26 to 2.08 A and 20 mA, respectively. With the series resistor along the discharging path, the peak discharging current can be significantly reduced. In addition, no underdamped sinewavelike characteristics were observed when the series resistances were larger than 10 Ω. The peak discharging currents under different series resistances are compared in Fig. 15. The duration in which the discharging current is larger than 5% of its maximum value is defined as the discharging time. The discharging time becomes longer if a larger series resistance is used. The discharging times under different series resistances are compared in Fig. 16. Larger series resistance leads to longer discharging time due to the larger RC time constant. This experiment successfully demonstrates the effectiveness of the ESD discharger proposed in Section II, which consists of large series resistances to suppress the discharging current during board-level CDM ESD events.



(a)



(b)

Fig. 14. Measured board-level CDM ESD current waveform of the 1/2-A4-sized PCB with (a) 100-Ω and (b) 10-kΩ series resistances under 100-V charged voltage.

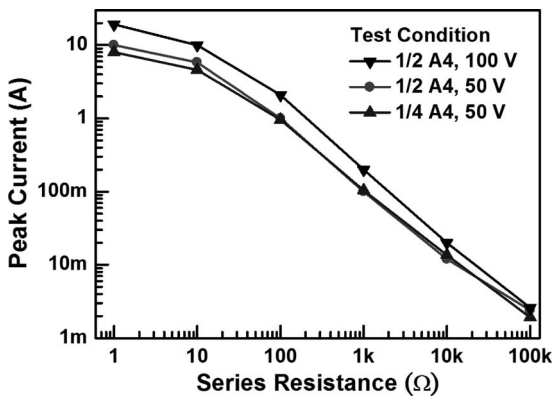


Fig. 15. Board-level CDM ESD peak currents under different series resistances.

IV. Verifications With Test Devices and Test Circuits

After the investigation on the mechanism of board-level CDM ESD events under different conditions, the board-level CDM ESD test is performed to the CMOS ICs. There are several components to be tested, which are the stand-alone gate-grounded NMOS (GGNMOS), N+/P-well diode, dummy

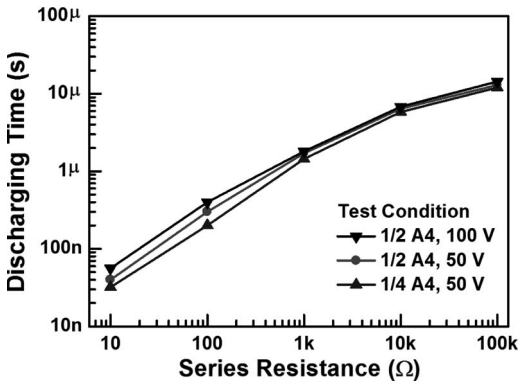


Fig. 16. Discharging times of board-level CDM ESD events under different series resistances.

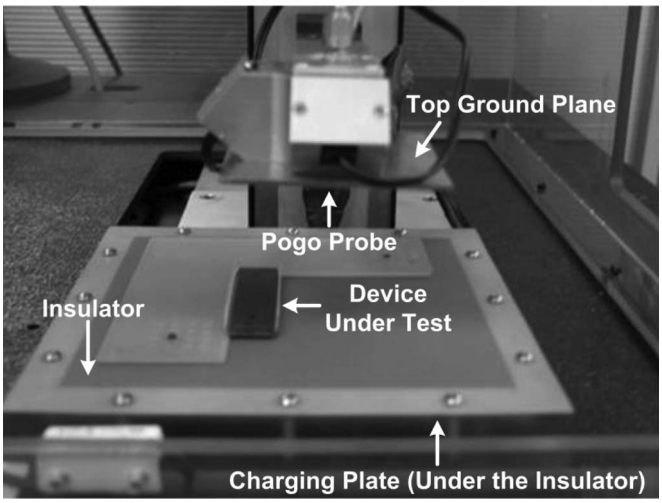


Fig. 17. Field-induced chip-level CDM ESD measurement setup.

receiver NMOS (RX_NMOS), and 2.5-GHz high-speed receiver circuit. The packages used in all of the chip- and board-level CDM ESD tests are the 40-pin dual-in-line (DIP) package. In the traditional chip-level CDM ESD test, only the IC chip (DUT) is put on the charging plate of the field-induced CDM ESD tester, as that shown in Fig. 17. However, both the IC chip and the test board on which the IC chip is mounted are put on the charging plate of the field-induced CDM ESD tester in the board-level CDM ESD test, as that shown in Fig. 18. The equivalent capacitance of the test board in the board-level CDM ESD test setup is ~274 pF. The main difference between the board- and the chip-level CDM ESD test is that the test board is also charged in the former test. Since the equivalent capacitance of the test board is significantly larger than that of the DUT, more charges are stored and discharged in board-level CDM ESD tests. Therefore, it is expected that the board-level CDM ESD test is more critical than the traditional chip-level CDM ESD test. The measured results on the chip- and board-level CDM ESD levels with different test components are compared. In addition, failure analysis is performed to characterize the failure mechanism.

A. Test With Gate-Grounded NMOS and N+/P-Well Diode

A GGNMOS fabricated in a 0.18-μm CMOS process was used as the DUT for the chip- and board-level CDM ESD

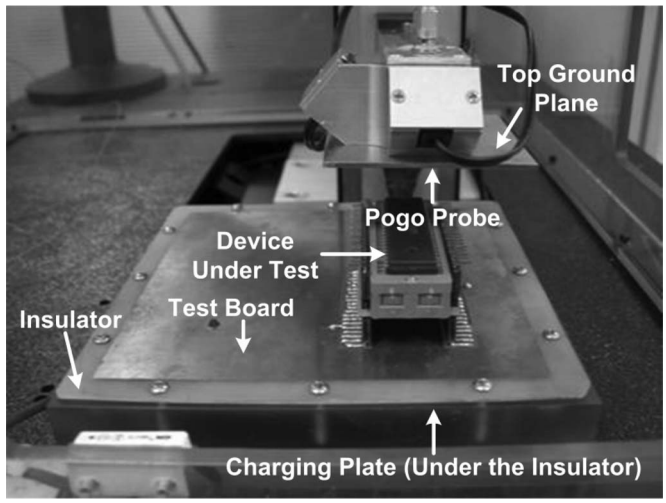


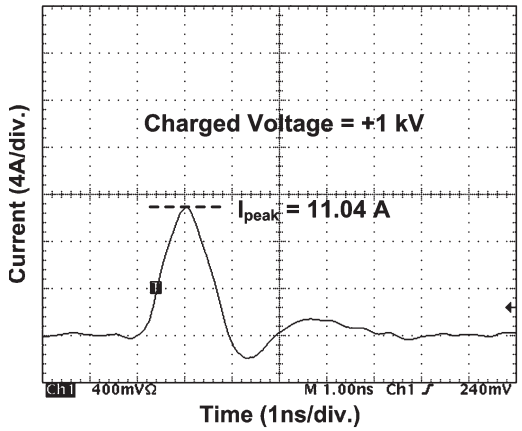
Fig. 18. Field-induced board-level CDM ESD measurement setup.

tests. The equivalent capacitance between the drain terminal and substrate of the GGNMOS in the 40-pin DIP package is ~6.2 pF. In the chip- and board-level CDM ESD tests, the drain terminal of the GGNMOS is tested. Fig. 19(a) and (b) shows the measured current waveforms under the chip- and board-level CDM ESD tests with the charged voltage of 1 kV, respectively. The peak currents under the chip- and board-level CDM ESD tests are 11.04 and 19.5 A, respectively.

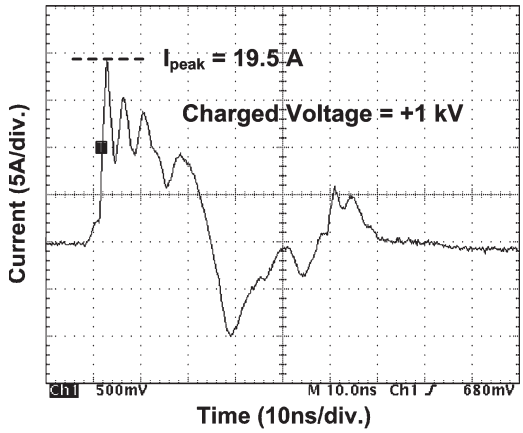
The current waveforms of the N+/P-well diode fabricated in a 0.18-μm CMOS process under 1-kV chip- and board-level CDM ESD tests are shown in Fig. 20(a) and (b), respectively. The peak currents under 1-kV chip- and board-level CDM ESD tests are 8.13 and 13.3 A, respectively. As compared with the GGNMOS, the N+/P-well diode has smaller peak currents under the chip- and board-level CDM ESD tests with the same charged voltage. The difference between the peak currents of the GGNMOS and N+/P-well diode is attributed to the turn-on resistance of the device, which is dominated by the device size drawn in the chip. Under the same charged voltage, the measured results showed that the discharging current under the board-level CDM ESD test is significantly larger than that under the chip-level CDM ESD test. Although the rise time of the board-level CDM ESD event is slower than that of the chip-level CDM ESD event, such a huge discharging current with a fast rise time during board-level CDM ESD events can easily damage the GGNMOS. Furthermore, the duration of the board-level CDM ESD event is longer than that of the chip-level CDM ESD event.

B. Test With Dummy Receiver NMOS (RX_NMOS)

A test circuit with dummy receiver NMOS (RX_NMOS) and on-chip ESD protection circuits fabricated in a 0.13-μm CMOS process was also used as the test circuit. As shown in Fig. 21, the gate terminal of the RX_NMOS is connected to the input pad to emulate the connection of a typical input NMOS in a receiver. The drain, source, and bulk terminals of the RX_NMOS are connected to VSS. On-chip ESD protection circuits are applied in the chip with the RX_NMOS. The typical double-diode ESD protection scheme is applied

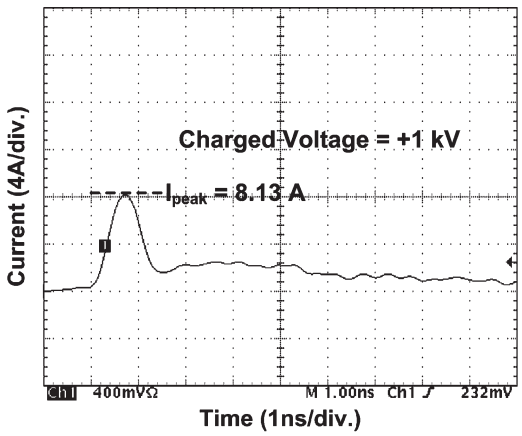


(a)

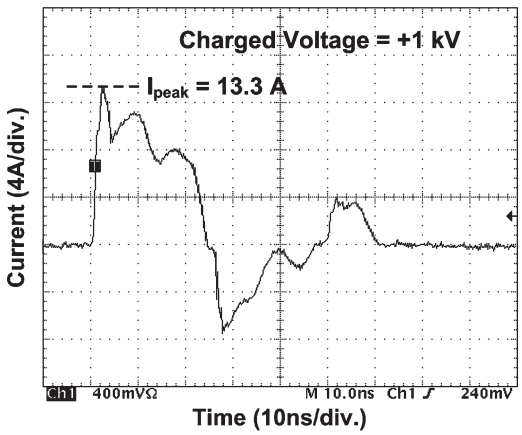


(b)

Fig. 19. Measured current waveforms of the GGNMOS under (a) +1-kV chip-level CDM ESD test and (b) +1-kV board-level CDM ESD test.



(a)



(b)

Fig. 20. Measured current waveforms of the N+/P-well diode under (a) +1-kV chip-level CDM ESD test and (b) +1-kV board-level CDM ESD test.

to the input pad. The power-rail ESD clamp circuit consists of an RC timer, an inverter, and an ESD clamp NMOS. The equivalent capacitance between the input pad and substrate of the RX_NMOS in the 40-pin DIP package is ~6.8 pF. By performing board-level CDM ESD tests to the RX_NMOS, the robustness of the typical receiver circuits to board-level CDM ESD events can be evaluated. The current waveforms of the RX_NMOS with the power-rail ESD clamp device realized with NMOS under 200-V chip- and board-level CDM ESD tests are shown in Fig. 22(a) and (b), respectively. The peak currents and measured results of chip- and board-level CDM ESD tests on the dummy receiver NMOS with the power-rail ESD clamp device realized by NMOS are listed in Table I. The RX_NMOS passes the 200-V chip-level CDM ESD test but fails the 200-V board-level CDM ESD test. This demonstrates that the board-level CDM ESD robustness is lower than the chip-level CDM ESD robustness, because the board-level CDM ESD event has a much larger discharging current than the conventional chip-level CDM ESD event. For example, the peak current is 3.13 A in the 200-V chip-level CDM ESD test, whereas the peak current in the 200-V board-level CDM ESD test is 4.24 A.

Another RX_NMOS with the power-rail ESD clamp device realized with the P-type substrate-triggered silicon-controlled rectifier (P-STSCR) [17] is shown in Fig. 23. This test circuit was also fabricated in a 0.13-μm CMOS process. The two

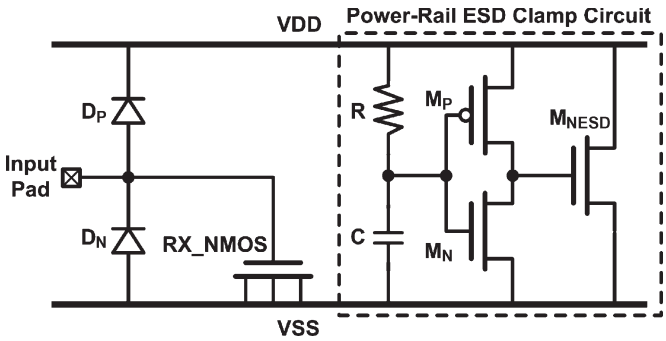


Fig. 21. RX_NMOS with the power-rail ESD clamp device realized by NMOS for chip- and board-level CDM ESD tests.

RX_NMOS circuits shown in Figs. 21 and 23 are identical except the power-rail ESD clamp device. To compare with the CDM ESD currents shown in Fig. 22, the 200-V chip- and board-level CDM ESD tests have been performed to the RX_NMOS with the power-rail ESD clamp device realized with P-STSCR. The measured current waveforms under the chip- and board-level CDM ESD tests are shown in Fig. 24(a) and (b), respectively. The current waveforms in Fig. 24 are almost identical to those in Fig. 22. Under the 200-V chip-level CDM ESD test, the RX_NMOS circuits with the power-rail ESD clamp device realized by NMOS and P-STSCR have

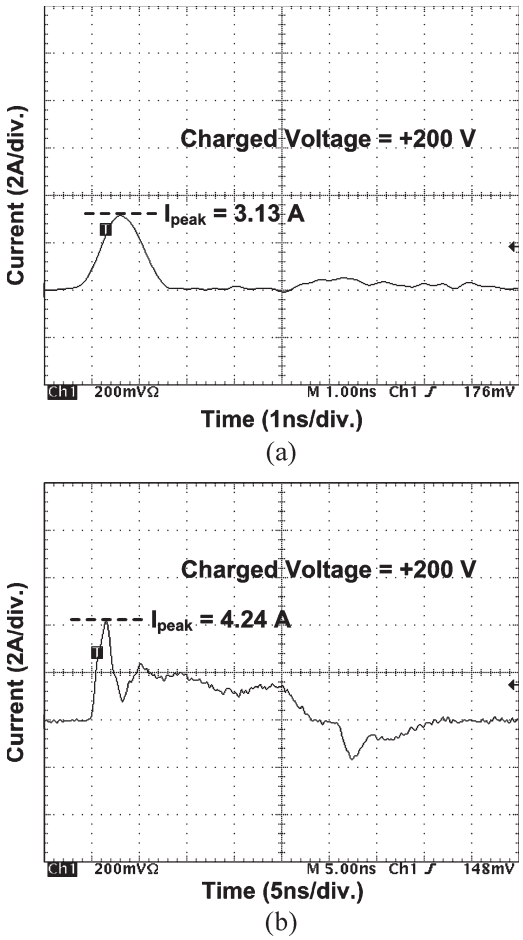


Fig. 22. Measured current waveforms of the RX_NMOS with the power-rail ESD clamp device realized by NMOS under (a) +200-V chip-level CDM ESD test and (b) +200-V board-level CDM ESD test.

TABLE I
MEASURED RESULTS ON CHIP- AND BOARD-LEVEL CDM ESD ROBUSTNESS OF THE DUMMY RECEIVER NMOS (RX_NMOS)

	Charged Voltage	Chip-Level CDM	Board-Level CDM
Peak Current	+100 V	N/A	1.72 A (Pass)
	+150 V	N/A	2.71 A (Pass)
	+200 V	3.13 A (Pass)	4.24 A (Fail)
	+400 V	8.43 A (Fail)	N/A

peak currents of 3.13 and 3.01 A, respectively. Under the 200-V board-level CDM ESD test, both of the RX_NMOS circuits with the power-rail ESD clamp device realized by NMOS and P-STSCR have the same peak current of ∼4.24 A. Since the ESD current path is through the ESD protection diode D_N, which is identical in both RX_NMOS circuits, the current waveforms in Figs. 22 and 24 are almost identical.

C. Test With 2.5-GHz High-Speed Receiver Interface Circuit

A 2.5-GHz differential high-speed receiver interface circuit fabricated in a 0.13-μm CMOS process was also verified with the chip- and board-level CDM ESD tests. Fig. 25 shows the circuit schematic of the 2.5-GHz differential high-speed receiver interface circuit with on-chip ESD protection design.

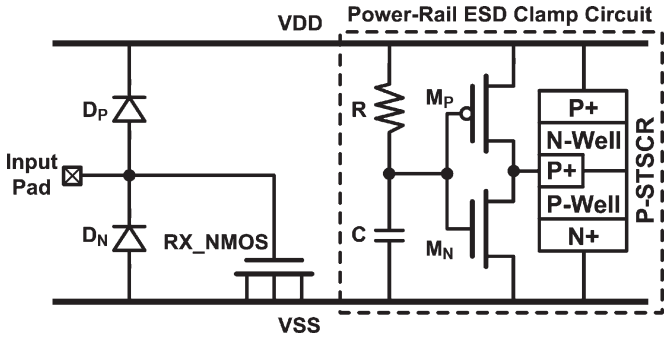


Fig. 23. RX_NMOS with the power-rail ESD clamp device realized by P-STSCR for chip- and board-level CDM ESD tests.

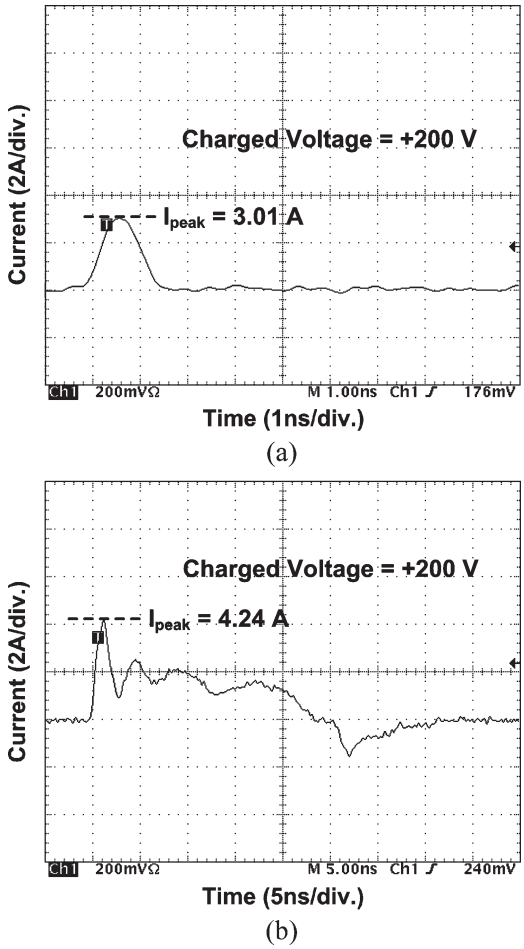


Fig. 24. Measured current waveforms of the RX_NMOS with the power-rail ESD clamp device realized by P-STSCR under (a) +200-V chip-level CDM ESD test and (b) +200-V board-level CDM ESD test.

The differential receiver interface circuit has the differential input stage realized by PMOS transistors. The double-diode ESD protection scheme is applied to each differential input pad, and the P-STSCR is used in the power-rail ESD clamp circuit. Because of high-speed application, the dimensions of the ESD diodes under the input pads are limited to reduce the parasitic capacitance at the pads. The equivalent capacitance between the Vin_1 pad and substrate of the ESD-protected 2.5-GHz differential high-speed receiver interface circuit in the 40-pin DIP package is ∼5.4 pF. Moreover, a reference

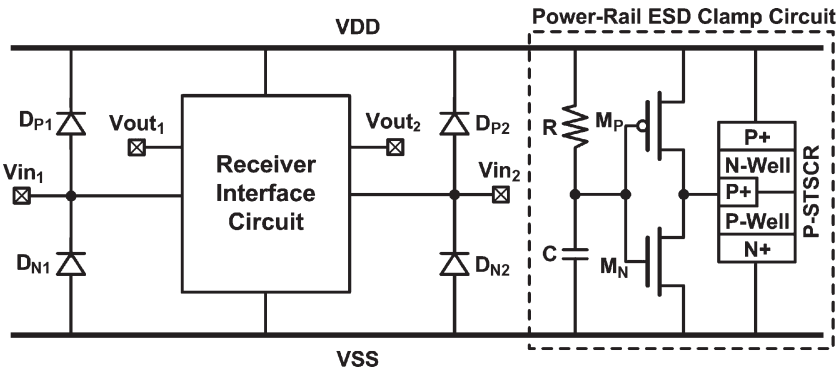


Fig. 25. Test circuit of the 2.5-GHz high-speed receiver interface circuit for chip- and board-level CDM ESD tests.

TABLE II
MEASURED CHIP-LEVEL CDM ESD ROBUSTNESS OF THE 2.5-GHZ HIGH-SPEED RECEIVER INTERFACE CIRCUIT

	Without ESD Protection		With ESD Protection	
Polarity	+	-	+	-
Failure Voltage	100 V	100 V	2000 V	1300 V

TABLE III
MEASURED BOARD-LEVEL CDM ESD ROBUSTNESS OF THE 2.5-GHZ HIGH-SPEED RECEIVER INTERFACE CIRCUIT

	Without ESD Protection		With ESD Protection	
Polarity	+	-	+	-
Failure Voltage	50 V	50 V	1300 V	900 V

high-speed receiver interface circuit without the on-chip ESD protection circuit was also fabricated in the same process to compare its ESD robustness. The tested pin under CDM ESD tests is the Vin_1 pad. The measured chip- and board-level CDM ESD levels of the 2.5-GHz high-speed receiver circuits with and without on-chip ESD protection circuits are listed in Tables II and III, respectively. The chip- and board-level CDM ESD levels of the reference high-speed receiver interface circuit are quite poor, which fail at ± 100 and ± 50 V, respectively. With the on-chip ESD protection circuits, the failure voltages during the chip- and board-level CDM ESD tests can be greatly improved to -1300 and -900 V, respectively. Similarly, the board-level CDM ESD level is lower than the chip-level CDM ESD level. Failure analysis had been performed on the ESD-protected high-speed receiver interface circuits after the chip-level CDM ESD test of -1300 V and the board-level CDM ESD test of -900 V. The SEM failure photographs after the chip- and board-level CDM ESD tests are shown in Fig. 26(a) and (b), respectively. The failure points are located at the P+/N-well ESD diode D_{P1}. Although the ESD protection devices are successfully turned on during CDM ESD tests, huge current during CDM ESD tests still damages the ESD protection devices. According to the SEM failure photographs, the failure is much worse after the board-level CDM ESD test than that after the chip-level CDM ESD test. This again demonstrates that board-level CDM ESD events are more critical than chip-level CDM ESD events.

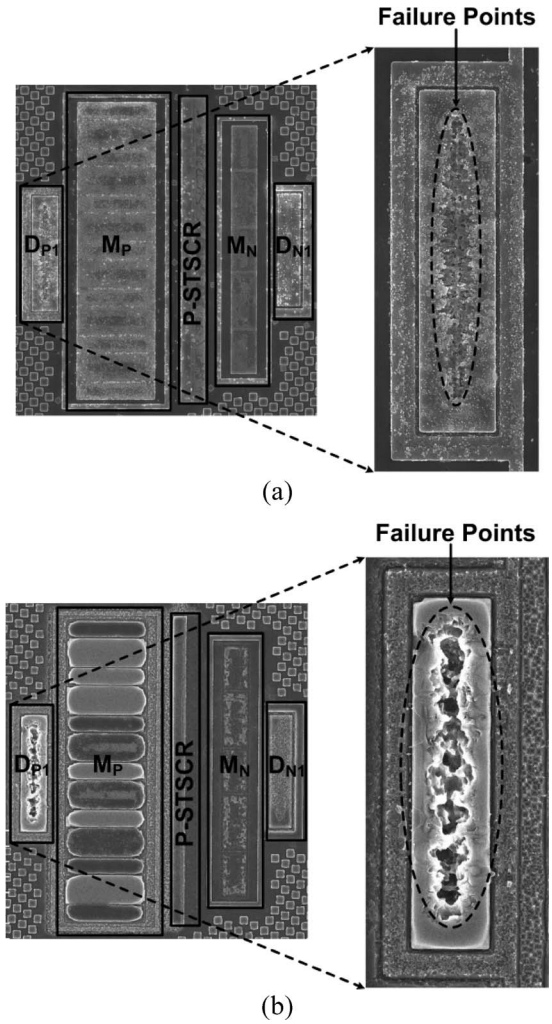


Fig. 26. SEM photographs of the failure points on the 2.5-GHz high-speed receiver interface circuit after (a) -1300-V chip-level CDM ESD test and (b) -900-V board-level CDM ESD test.

V. CONCLUSION

In this paper, the board-level CDM ESD issue has been comprehensively addressed. The causes of both chip- and board-level CDM ESD events are introduced first. Then, the discharging current waveforms during board-level CDM ESD events under different PCB sizes, different charged voltages, and different series resistances are investigated. Finally, the

board-level CDM ESD test was performed to several test devices and test circuits fabricated in 0.18- and 0.13-μm CMOS processes. The measured results have shown that the board-level CDM ESD events are more critical than the chip-level CDM ESD events. There were several designs reported for chip-level CDM ESD protection [18]–[24]. However, no design against board-level CDM ESD events is reported so far. In the nanoscale CMOS processes, the gate oxide of MOS transistor becomes thinner, which degrades the CDM ESD robustness of CMOS ICs. In high-speed or radio-frequency applications, large ESD protection devices cannot be applied to the I/O pad due to the limitation on parasitic capacitance, which further increases the difficulty of CDM ESD protection design. Moreover, the die size becomes larger in SoC applications, which means that more charges will be stored in the substrate of the chip. Consequently, CDM ESD issues, including chip- and board-level CDM ESD events, will become more critical and should be taken into consideration in ICs and microelectronic systems which are realized in nanoscale CMOS processes.

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