Chapter 1
Introduction

1.1 General Background

In recent years, the study of device for high frequency application has become more and more popular. With the rapid development of the wireless communication systems, the requirements of low cost, low power consumption, high-level integration and high frequency operation devices become more and more significant. For high frequency applications, compound semiconductor devices such as the GaAs-based pseudomorphic high electron mobility transistors (PHEMTs), metamorphic HEMTs (MHEMTs), and the InP-based conventional lattice-matched or pseudomorphic InP-HEMTs have shown superior performance over Si MOS devices for high-frequency applications.

1.2 Overview of High Electron Mobility Transistors (HEMTs)

III-V based High electron mobility transistors (HEMT) rely on the use of heterojunctions for their operation. Fig.1.1 shows a conventional HEMT structure. The heterojuctions formed between III-V semiconductors materials of different compositions and bandgaps. As compared with the silicon-based transistors, such as metal-oxide-semiconductor field effect transistors (MOSFETs) and bipolar-junction transistor (BJTs), GaAs-based transistors exhibit several advantages over Si-based transistors in high frequency applications due to the their superior material natural such as high peak drift

velocity, high mobility and wide bandgap.【1】

The first GaAs HEMT was invented in 1979 by Takashi Mimura 【2】, ever since then, HEMT devices have been successfully manufactured and commercialized for many applications. The epitaxial layers of the HEMT structure are designed to form two-dimension electron gas (2-DEG) in the channel layer with an un-doped spacer in the high band gap material to separate the ionized donors from the channel to reduce the couloum scattering effect and increase the electron mobility. Consequently, GaAs HEMTs have superior carrier transport properties due to the band-gap engineering design.

Conventional HEMT structure is consisted of AlGaAs barrier layer and GaAs channel structure. The bandgap discontinuity between AlGaAs/GaAs increases as the Al content increases, in the meanwhile, the large discontinuity in the bandgap causes better confinement of the electrons in the channel. However, the deep-complex center (DX center) phenomenon exists while Al content is over 20% which traps the electrons and degrades the device performance. In order to avoid the DX center effect and increase the electron mobility, AlGaAs/InGaAs/GaAs pseudomorphic HEMT (PHEMT) structure was developed. InGaAs was a preferred channel material over GaAs for HEMTs because of its superior transport properties as compared to GaAs. The In content in the channel was increased to enhance the electron transport properties and improve the confinement of the carriers in the channel. However, InGaAs channel in PHEMTs is limited to an indium content of 25%【3】to avoid lattice relaxation of the channel that will induce the misfit dislocations and degrade the

electronic properties of devices.

Higher In mole fractions are feasible in the HEMT structure on InP substrates, e.g., lattice-matched $In_{0.52}Al_{0.53}As/In_{0.53}Ga_{0.47}As$ heterostructures. InP-based HEMTs have shown very high frequency characteristics, such as lower noise figure, high gain, and high efficiency, compared to the GaAs-based PHEMTs. 【4】 However, InP substrates are more expensive, smaller in size, and more brittle than the GaAs substrates. GaAs substrates of 6-inch diameter are commercially available, while the largest available InP substrates are only 4-inch in diameter.【5】Therefore, a new device structure, metamorphic HEMT (MHEMT) structure, was proposed and developed on GaAs substrates. In the MHEMT structure, the device active layers are grown on a strain relaxed, compositionally graded metamorphic buffer layer. The buffer layer accommodates the lattice mismatch between the InGaAs channel and the GaAs substrate. Therefore, the high indium content in the InGaAs channel can be achieved in spite of the large lattice mismatch between the active epitaxial layers and GaAs substrate. The relationship between the lattice constant and the bandgap of $In_xAl_{1-x}As$ and $In_yGa_{1-y}As$ is shown in Fig. 1.2. Using the metamorphic buffer layer, the $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ structure with lattice matched to InP can be grown on the GaAs substrates which results in a substantial cost reduction and manufacturability improvement. According to Table 1-1【6】, MHEMT has the advantages over InP HEMT in cost and fabrication yield. Consequently, to achieve high-speed performance for the device, the high indium content in the channel layer is necessary.

1.3 The methods to improve device performance for high frequency application

Cut-off frequency (f_T) and maximum frequency of oscillation (f_{max}) are important parameters which indicate the high frequency capability of the device. The cut-off frequency of a device expressed as Eq.1.1 is the frequency at which the short circuit current gain becomes unity, and the maximum frequency of oscillation in a device showed as Eq.1.2 is the frequency at which the power gain becomes unity.

$$f_T = \frac{g_m}{2\pi C_G} = \frac{Z_G V_{sat}\varepsilon}{W} \cdot \frac{W}{\varepsilon Z_G L_G} \cdot \frac{1}{2\pi} = \frac{V_{sat}}{2\pi L_G} \tag{1.1}$$

$$f_{\max} \approx \frac{f_T}{2\sqrt{(R_g + R_s + R_i)\left(g_d + g_m \frac{C_{Miller}}{C_{gin}}\right)}} \tag{1.2}$$

From Eq.1.1 and Eq.1.2, it is clear that reducing gate length (L_g) or increasing the electron saturation velocity will enhance the device performance at high frequencies. The smaller gate length can be obtained by using electron beam lithography technique; however, the high electron mobility and high electron saturation velocity can be achieved by using high indium content channel. The relationships between indium content in the channel layer and the electron mobility and saturation velocity are expressed in Table 1-2.

1.4 Motivation and dissertation outline

In recent year, GaAs-based MHEMTs and InP-based HEMT with remarkable device performances for high frequency applications have been published and these results are listed in Table.1-3【7】【8】. From this table, high indium content channel material with InP or metamorphic GaAs substrate is the main method to enhance device performance. However, the metamorphic GaAs substrate has some advantages over InP substrate as mentioned in the previous section. So this study will focus on the development of metamorphic HEMTs. The high frequency performance of HEMT can be improved by using high indium content super-lattice channel. The higher indium content in the channel is very essential for achieving superior RF performance.

In chapter 2, use of superlattice channel to increase the indium content in the InGaAs channel to proposed. I will introduce the advantages of using superlattice channel and discuss about device structure in this study.

In chapter 3, details of device structure and fabrication process are included. And the DC and RF characteristics measurements of the device are also discussed in detail, with the DC data of I_{DSS}, g_m and breakdown voltage, along with RF data of f_T and f_{max}.

In chapter 4, the experimental results are presented and discussed in details for the super-lattice channel and conventional InGaAs channel devices. In the last chapter, the conclusion of this research will be given.

Tables:

Property	InP HEMT	MHEMT
Substrate Availability, Cost	- 4-inch now, higher cost	+ 6-inch available now
MBE Growth Time	+ ～1/2 hour	- 1-2 hours
Process Difficulty Yield	- Higher breakage, more difficult /slower backside process	+ Lower breakage, standard GaAs backside process
Performance, Impedance char.	No difference	No difference
Achievable Channel Indium Content	53-80 %	30-80 %
Thermal Resistance	+ InP has 50% higher thermal conductivity than GaAs	Comparable to GaAs PHEMT, effect of buffer unclear
Reliability	Proven for low noise, unproven for power	Excellent initial data for low noise, power unknown

Table 1.1 Comparison of lattice-matched InP HEMT and metamorphic GaAs HEMT.

	Si	*GaAs*	*$In_{0.53}Ga_{0.47}As$*	*InAs*	*InSb*
Electron Mobility ($cm^2V^{-1}S^{-1}$) ns = $1 \times 10^{12}/cm^2$	600	4600	7800	20000	30000
Electron Saturation Velocity (10^7 cm/s)	1.0	1.2	0.8	3.5	5.0
Ballistic Mean Free Path (nm)	28	80	106	194	226
Energy Bandgap	1.12	1.42	0.72	0.36	0.18

Table 1-2. Channel material properties at 295K

Devices	**In (%)**	**L_g (nm)**	**g_m (S/mm)**	**f_T (GHz)**	**f_{max} (GHz)**	**Published**	**Affiliation**
InP HEMT	65	**50**	1.25	286	207	2003, 11th GaAs sym.	Chalmers Univ.
GaAs MHEMT	53	**70**	1.45	293	337	2003, 11th GaAs sym	IAF., Germany
InP HEMT	70	**30**	1.5	547	400	May. 2004, *IEEE, EDL.*	CRL., Fujitsu.
GaAs MHEMT	53	**50**	1.028	440*	400	Nov., 2005, *IEEE, EDL*	Glasgow Univ.

Table 1-3. Best performance of InP HEMT and GaAs-based metamorphic HEMT published in recent years.

Figures:

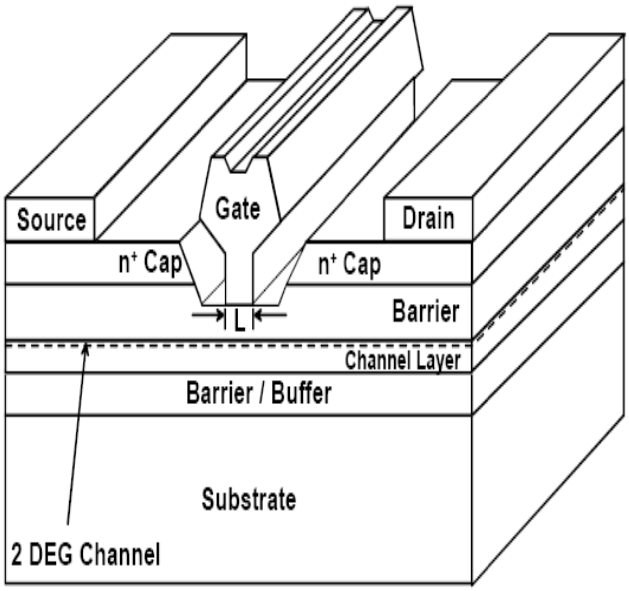

Fig.1.1 Conventional HEMT structure

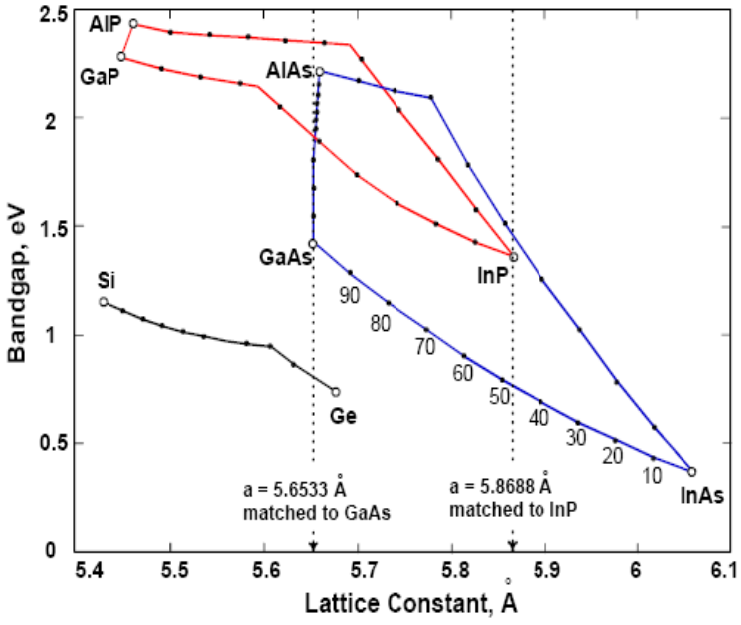

Fig.1.2 Energy band gap v. s. lattice constant for the $In_xAl_{1-x}As/In_yGa_{1-y}As$ system

Chapter 2

Study of Superlattice Channel

The device performance is improved by using high indium content channel layer, but also limited by disorder scattering in the channel and defects due to lattice mismatch between InGaAs channel layer and InAlAs buffer layer. This chapter will introduce superlattice channel with high indium content to replace the conventional InGaAs channel to enhance the device performance.

2.1 Indium-rich InGaAs channel v.s. critical thickness

In-rich InGaAs materials can be applied as channel layer on GaAs substrate with InAlAs metamorphic buffer to improve the device performances due to their lower effective electron mass, higher electron mobility, higher conductance band discontinuity and a large T-L intervalley separation within InAlAs/InGaAs heterojunction. However, the misfit dislocations and defects could be produced because of the lattice mismatch between InGaAs channel layer with higher indium content and InAlAs buffer layer. Consequently, the device performance will be degraded due to the strain produced by the large lattice mismatch between InGaAs channel layer and InAlAs buffer layer. Fig.2.1 shows the lattice constant of InGaAs layer varies with indium fraction in the channel. From Fig.2.2. it is clear that the thickness of InGaAs layer is limited to a critical value. So the high quality channel layer can be obtained without structural defects such as 3D islands or dislocations generated, if the thickness is less than the critical value. Use of superlattice structure may be a suitable method to obtain high

quality layer, because the thickness of each layer in superlattice structure is thin enough.

2-2 High indium content superlattice channel

In $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ metamorphic HEMT, the electron mobility of $In_{0.53}Ga_{0.47}As$ is limited by disorder scattering in addition to polar optical photon and ionized impurity scattering. The disorder scattering is due to random arrangement of constituent atoms, that is, indium and gallium in this case. The disorder scattering reduces the electron mobility, especially in high purity material at low temperature. Therefore, the electron mobility of the 2-DEG is reduced by the disorder scattering and the performance of high speed FET's with the 2-DEG will be limited.

One way to enhance the transport properties was predicted by Yao【9】that replaced the InGaAs channel with a strain-accommodated $(InAs)_m/(GaAs)_n$ short-period superlattice (SPSL). In this highly ordered binary material system, higher mobility is calculated due to the absence of disorder scattering becoming especially predominant at low temperatures ($T < 50$ K). So far, the GaAs-based and InP-based HEMT with superlattice channel had been well developed and exhibited well device performance. 【10】【11】【12】

Insertion of InAs layer is the most effective method for the high indium content channel. However, the thickness will be limited due to large lattice mismatch between InAs channel and $In_{0.52}Al_{0.48}As$ buffer. In the superlattice

structure, the thickness of each layer is smaller than critical thickness, which doesn't allow the dislocations and defects to be produced between each layer. In the other way it can be said that the high quality channel with high indium content can be obtained by using superlattice channel.

In this study, the $(In_{0.53}Ga_{0.47}As)_m/(InAs)_n$ superlattice has been used as the channel layer so that the average indium content in the channel increases which is the major factor to enhance device performance. Because of lower energy level of InAs, the electron distribution will be confined in InAs wells, therefore, the device exhibits 2-D characteristics in the channel which are mostly based on InAs properties. However, the binary arrangement of InAs quantum wells and small effective electron mass of InAs and the high electron mobility of InAs will improve the device performance.

Figures:

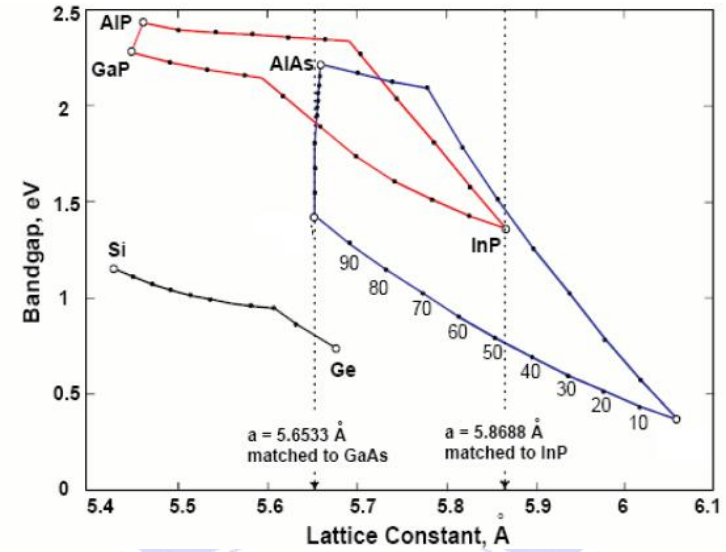

Fig.2.1 Energy band gap v.s. lattice constant for the $In_xAl_{1-x}Ga/In_yGa_{1-y}As$ system

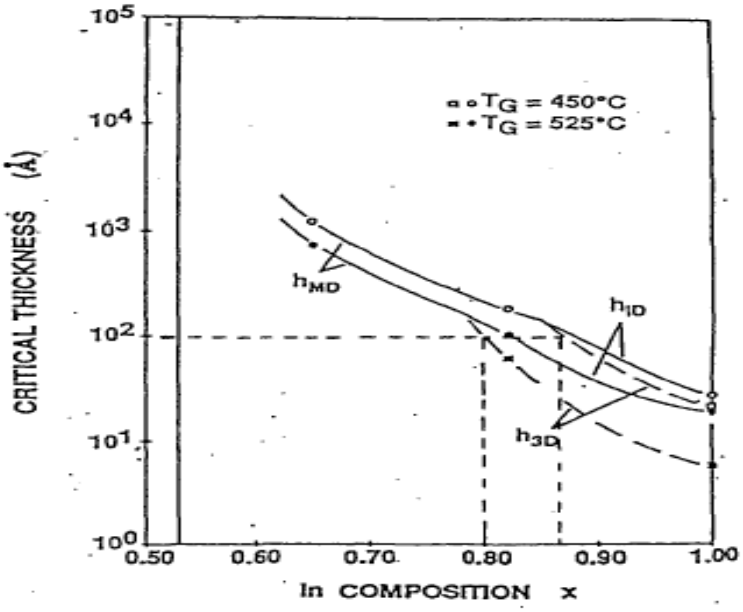

Fig. 2.2 Critical thickness curves corresponding to onset of 3D growth (h_{3D}), plastic relaxation through misfit dislocation (h_{MD}), and through 3D island dislocation (h_{ID}) as a function of In composition and growth temperature. 【13】

Chapter 3

Fabrication and DC & RF measurement of MHEMT

3.1 Device structure

In this study, the epitaxial layers of the metamorphic HEMT with $In_xAl_{1-x}As$ grading buffer layer were grown by molecular beam epitaxy (MBE). A cross-section structure of superlattice MHEMT is shown in Fig. 3.1. The indium graded $In_xAl_{1-x}As$ metamorphic buffer layer was grown on a 3-inch semi-insulating GaAs wafer, followed by an un-doped $In_{0.52}Al_{0.48}As$ buffer layer. The metamorphic buffer was graded from the GaAs substrate to that of high indium content active layers, these layers traps the dislocations and prevent them from propagating into the superlattice channel. Following the buffer layer, 15 nm - 10 period $(In_{o.53}Ga_{0.47}As)_m/(InAs)_n$ superlattice was chosen as the channel layer. The Si-planar doped (4.5×10^{12} cm^{-2}) layer was separated from the channel layer by 5 nm thin undoped $In_{0.52}Al_{0.48}As$ spacer layer in order to increase the mobility of the electrons in the channel by decreasing the Coulomb scattering effect from the ions in the donor layer. The $In_{0.52}Al_{0.48}As$ Schottky layer was 20 nm. Then, the 20 nm thick $In_{0.52}Ga_{0.48}As$ cap layer heavily doped with Si of 5×10^{18} cm^{-3} was grown for Ohmic contact formation.

3.2 Device Fabrication

The fabrication processes of the MHEMTs in this study include:

1. Mesa/device isolation

2. Ohmic contact formation

3. Gate formation

4. Device passivation

5. Airbridge formation

The details will be described in the following sections.

3.2.1 Mesa/Device isolation

Device isolation is the first step of the whole HEMT fabrication process which was used to define the active region on the wafer. These defined areas by lithography technique as depicted in Fig.3.2, the current flow is restricted to the desired path and each active device is isolated from each other. There are three typical ways to achieve device isolation: wet etching, ion bombardment, and selective implantation. Wet etching is the simplest method among them. In this study, Mesa isolation was formed by using a phosphoric based solution. The active areas were masked by Shipley S1818 photo resist. According to the device structure, the inactive area was etched to the buffer layer to provide good isolation. In order to avoid from the photo resist peeling during the etching process, the wafer surface was pre-treated before resist coating by Hexamethyldisilazane (HMDS) coating. Finally, the etching depth was measured by α-step or surface profiler after the photo-resist was stripped and the etched profile was checked by Scanning electron microscopy (SEM). To inspect the mesa isolation process, a test pattern with a 10 μm gap was used to measure the leakage current.

3.2.2 Ohmic contact formation

After wafer cleaning by using ACE and IPA, the negative photo resist and I-line contact aligner were used to define the ohmic patterns and to form the undercut profile for the metal lift-off process shown in Fig.3.3. Then the ohmic metals, consisted of Au 200 Å/ Ge 400 Å/ Ni 140 Å/ Au 2000 Å from the bottom to the top, were deposited in the appropriate composition by e-gun evaporation system shown in Fig.3.4 and Fig.3.5. After lift-off process, source and drain ohmic contacts were formed with rapid thermal annealing at 250 ℃ for 25 sec in forming gas. The annealing condition was decided by monitoring the drain-to-source current at different temperatures as shown in Fig.3.6. Au-Ge ohmic system was used for the process stability. Germanium atoms diffuse into the heavily doped InGaAs cap layer during the thermal annealing process. After ohmic contact formation, the specific contact resistance was checked by the transmission line method (TLM) in the process control pattern monitor (PCM). The typical measured contact resistance was less than 10^{-6} Ω-cm^2 shown in Fig.3.7.

3.2.3 T-shaped gate process

For high frequency and high speed application, short gate length with low gate resistance is expected. T-shaped gate structure was the most common method for obtaining low gate resistance. According to the T-gate structure design, the small gate foot forms the Schottky contact with the HEMT, while the wilder gate head offers a low gate resistance.

T-shaped gates were achieved by using a multilayer resist technique with E-beam lithography. In this study, ZEP/PMGI/ZEP was used as the resist system to form the 100 nm T-shaped gates.

After patterning the T-shaped gate, the exposed HEMT channel was recessed to achieve the desired depth to obtain optimal channel current and pinch-off voltage. That means a groove is fabricated in the exposed surface of the wafer to “recess” the gate. This process is done by wet etch technique in this study, although dry etching methods may also be used. The recess was etched with using PH-adjusted solution of succinic acid (SA.) and H_2O_2 mixture to perform selective etching of the heavily doped InGaAs cap layer over InAlAs Schottky layer. The concentration of the etchant should be adjusted to provide an etch rate that is sufficiently slow to allow good control over the recess process, thus enable the operation to approach the target current value without over etching it. The etching selectivity of InGaAs cap layer over InAlAs Schottky layer was beyond 100. The schematic of the HEMT with recessed gate is shown in Fig.3.8 and the SEM Micrograph of T-shaped gate is shown in Fig.3.9.

The target current after the gate recess process is a critical parameter affecting the HEMT performance. In order to obtain the desired recess depth, the recess process was controlled by monitoring the drain-to-source current during the etching process. For the low noise MHEMT, the saturation current and the slope of the linear region went down as the recess groove was etched deeper and deeper. The wet etchant usually leaves a thin oxide on the InAlAs surface, and HCl-based solution was used to remove the surface oxide. After recess etching, Ti/Pt/Au gate metal was evaporated and lifted off as shown in Fig.3.10.

3.2.4 Device passivation and contact via formation

FETs are very susceptible to the surface condition, especially in the gate region. As the device scales down, the gate length and spacings of source-to-drain and gate-to-drain become smaller, the devices are very sensitive to the damages and contaminations such as chemicals, gases, and particles. The passivation layer protects the device from damage during following processes handling (such as “airbridge”) and wafer probing. The dielectric layer SiN_x is a common choice for device passivation.

In this study, the silicon nitride (SiN_x) was deposited by the Samco PECVD system. Fig.3.11 depicted the cross section of the passivated surface and Fig.3.12 is the SEM cross-section Micrograph of the device after passsivation. The precursors used were silane, ammonia, and nitrogen while the process pressure was 100 Pa, the process temperature was 300 °C and process time was 10 minutes in order to form the silicon nitride film of 1000 Å. The reflection index was inspected by Ellipsometer and was measured to be about 2.0.

Then the contact openings of the devices were formed by photo lithography as shown in Fig.3.13. The RIE was used to define the contact via hole of the source and drain pads for interconnection. The plasma gases source for SiN_x etching were mixture of CF_4 and O_2.

3.2.5 Airbridge formation

In order to reduce the total device area, finger-type layout was adopted. So,

the airbridge process was necessary to contact the fingers. The airbridges have several advantages including lowest dielectric constant of air, low parasitic capacitance, and the ability to carry substantial currents.

Analog GaAs devices operating at high current density benefit from airbridges with thick plated metal layer. Low parasitic capacitance (between the airbridges and any metallization beneath) follows from the large spacing and low dielectric constant of the intervening medium. The capacitance is a function of the thickness, and the dielectric constant of the intervening material. Air (dielectric constant = 1.0) has a much lower dielectric constant than any other dielectric. These considerations mean that airbridges crossovers are less capacitive than the dielectric type by a factor of five to twenty.

The following process steps were used for the airbridge formation

1. The first photolithography for plating via holes.
2. Thin metal (Ti/Au) deposition
3. The second photolithography for plating areas.
4. Au electroplating.
5. Second photo-resist removal
6. Thin metal etching
7. First photo-resist removal.

The first layer of photo-resist was opened at the regions of the source and drain pads as shown in Fig.3.14. The thickness of the first layer of photo-resist determines the spacing between the bridge and the material beneath. The thickness of the photo-resist was about 3 μm. In order to remove the photo-resist

residues in the exposed region, an O_2 descum process was required after the photolithography. The wafer was plate baked immediately after the ICP descum process in order to evaporate the remaining solvent in the photo-resist. On the other hand, the first photo-resist must be sufficiently baked to prevent the "bubbling" after thin metal deposition and the later thermal bake of the second photolithography.

The thin seed metal Ti/Au was deposited by e-gun evaporation system shown in Fig.3.15. Ti serves as the adhesion layer and Au serves as the seed layer and conductive layer for electroplating. The thicknesses of these two metals were 300 Å and 1000 Å, respectively. The second layer photo-resist was defined for the regions of the gold plating as shown Fig.3.16. Same as the first lithography, O_2 descum is necessary to remove the residues after development. The wafer was cleaned before plating to prevent contamination. After Au electroplating as shown in Fig.3.17, the samples were immersed in ACE to remove the second photo-resist of the airbridges as shown in Fig.3.18. The thin Au layer of the Ti/Au seed metal was etched by KI/I_2 solution in about 60 seconds. The etching rate of this step is high, so that the etching of Au stops at the underlying Ti metal as the color on wafer turned from red to grey shown in Fig.3.19. Ti thin metal was also etched by diluted HF solution (HF: H_2=1:100). HF is the active ingredient in the etchant, so it also etches oxides. Raising the fraction of HF in the solution increases the etching rate. Titanium is readily oxidized, so it is likely to form an oxide layer from the water, which is readily etched by the HF in this solution, resulting in the formation of bubbles of oxygen.

The samples were dipped in ACE for twenty minutes to remove the first photo-resist for plating. The photo-resist residues were stripped by O_2 plasma using ICP, and then the specimens were dipped in IPA for 5 min. They were finally immersed in D.I. water, and then followed by compressed air drying as shown in Fig.3.20. After airbridge formation, the RF characteristics of the devices were measured. The SEM images of the airbridge are given in Fig.3.21 (a) and (b).

3.3 Device Characterization

After the device fabrication process, DC and RF performance of the GaAs MHEMTs must be measured using on-wafer measurement. For the DC measurement, the I-V characteristics were obtained easily by using an HP4156B Modular DC Source/Monitor and SUSS PA200 Semi-Auto Probe Station. The Transmission Line Model (TLM) method for determining specific contact resistance was obtained by using 4-point measurement and Keithley 2400 Source-Meter. The S-parameters for the MHEMT devices were measured by HP8510XF Vector Network Analyzer using on-wafer GSG probes from Cascade MicroTech. However, finding the RF behavior of the device on wafer is a complicated process.

The measurements of the electrical characterization of the device are stated in the following section.

3.3.1 I-V characteristics

The band diagrams at three different positions along the channel are illustrated in Fig. 3.22. There is a potential drop of channel charge density in the direction parallel to the channel, causing q'_{CH} to be a function of the position x. Therefore, C'_{OX} was defined as a per area gate oxide capacitance, and the channel charge sheet density is expressed

$$q'_{CH} = -C'_{OX}[V_{GS} - V_T - V_{CS}(\chi)] \quad (3\text{-}1)$$

We denote the channel-to-source potential resulting from the applied Gate-Source voltage V_{GS} and Drain-Source voltage V_{DS}. V_T is threshold voltage and the x means the position along the channel. The additional potential $V_{CS}(x)$ is called the channel-source potential. When $V_{DS} \neq 0$, the $V_{CS}(x)$ varies with x. The channel current equation which is familiar with $I = qA\mu_n\varepsilon$ (A = area) is proportional to the cross-section area of the current conduction, the charge density, the mobility μ_n and the electric field. Therefore, we can obtain that:

$$I_{CH}(\chi) = -WC_{OX}\mu_n[V_{GS} - V_T - V_{CS}(\chi)]\frac{dV_{CS}(\chi)}{d\chi} \quad (3\text{-}2)$$

We note that q'_{CH} is a negative quantity in HEMT, since electrons accumulated in the channel are negative charges. In fact, if we choose $x = L$ at the drain, this constant channel current is equal to the negative of the drain current. Hence, we have $I_D = -I_{CH}$, and find:

$$\int_0^L I_{DS}\,dx = -C'O\int_{V_{CS(O)}}^{V_{CS(L)}} C_{OX}\,\mu_n[V_{(GS)} - V_{(T)} - V_{(CS)}(\chi)]dV_{CS}(\chi) \qquad (3\text{-}3)$$

To carry out the integration in Eq. (3-3), we assume temporarily that we are working in the linear region such that current saturation due to channel pinch off at the drain does not occur. The *I-V* characteristics after pinch off will be dealt with shortly. In the linear operating region, the boundary conditions are $V_{CS}(L) = V_{DS}$ and $V_{CS}(0) = 0$. Hence, Eq. (3-3) leads to:

$$I_D = \frac{W_g C'_{OX}\,\mu_n}{Lg}[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}] \qquad (3\text{-}4)$$

Eq. (3-4) is plotted schematically in Fig.3.23, with I_D shown as a function of V_{DS}. The value of V_{DS} corresponding to the attainment of $I_{D,sat}$ is denoted as $V_{DS,sat}$, the saturation voltage. The saturation voltage can be obtained by taking the derivative of I_D will respect to V_{DS} and setting the result to zero. We find that:

$$V_{DS,SAT} = V_{GS} - V_T \qquad (3\text{-}5)$$

At this saturation voltage, q'_{CH} calculated from Eq. (3-1) is identically zero at the drain (pinch off). However, we realize that this conclusion originates from the fact that we are extending the validity of Eq. (3-1) all the way to where $q'_{CH}(L)$ is identically zero. Physically, the channel at the drain does not pinch off completely. Instead, there is a finite thickness of accumulation of charges at which q'_{CH} $x=L$ is nonzero. The drift velocity is high, but nonetheless finite, so a

constant current is maintained throughout the channel. Therefore, a complete model of the drain current is given by:

$$I_{DS} = \frac{W_g C'_{OX} \mu_n}{L g}[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}] \qquad \text{for } V_{DS} < V_{DS,SAT}$$

$$= \frac{W_g C'_{OX} \mu_n}{L g}[\frac{(V_{GS} - V_T)^2}{2}] \qquad \text{for } V_{DS} \geqq V_{DS,SAT} \qquad (3\text{-}6)$$

For HEMTs, it is convenient to define the *saturation index (α)* as:

$$\alpha = 1 - \frac{V_{DS}}{V_{DS,SAT}} \qquad \text{for } V_{DS} < V_{DS,SAT}$$

$$= 0 \qquad \text{for } V_{DS} \geqq V_{DS,SAT} \qquad (3\text{-}7)$$

The drain current increases due to the perturbations in V_{GS} and V_{DS}. The mutual transconductance measures the amount of current increase due to the increment in the gate bias.

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS} = const.} \qquad (3\text{-}8)$$

We also can write:

$$g_m = \frac{W_g C'_{OX} \mu_n}{L g}(V_{GS} - V_T) * (1 - \alpha) \qquad (3\text{-}9)$$

3.3.2 Transmission line model (TLM) 【14】

The most widely used method for determining specific resistance is the method of Transmission Line Model (TLM). In this particular approach, a linear array of contacts is fabricated with various spacings between them as shown in Fig 3.24. The distances between TLM electrodes are 3 μm, 5 μm, 10 μm, 20 μm, and 36 μm, respectively in this study. The resistance between the two adjacent electrodes can be plotted as a function of the space between electrodes. The plot is shown in the Fig.3.25. Extrapolating the data to L = 0, one can calculate a value for the term R_c (Ω-mm).

$$R = 2R_C + \frac{R_S L}{W} \qquad (3\text{-}10)$$

Where R is measured resistance, R_c is contact resistance, R_s is sheet resistance of the channel region, W is electrodes width, and L is space between electrodes. Another important parameter is the specific contact resistance ρ_c (Ω-cm^2), which is defined as

$$\rho_C = \frac{W^2 R^2}{R_S} \qquad (3\text{-}11)$$

This specific contact resistance is a practical figure of merit for contact resistance. It includes a portion of the metal immediately above the metal-semiconductor interface, a part of the semiconductor below the interface, current crowding effects, spreading resistance under the contact, and any

interfacial oxide that may present between the metal and the semiconductor.

3.3.3 Breakdown characteristics 【15】

Breakdown mechanisms and models have been discussed in many articles. One of the models showing it is dominated by the thermionic filed emission (TFE) / tunneling current from the Schottky gate. This model predicts that the two-terminal breakdown voltage is lower at higher temperature because tunneling current increases with the temperature. Higher tunneling current occurs at higher temperature because carriers have higher energy to overcome the Schottky barrier. Other model suggests that impact-ionization determines the final two-terminal breakdown voltage, because the avalanche current decreases with increasing temperature. Lower avalanche current occurs at higher temperature because phonon vibrations as well as carrier-carrier scattering increase with increasing temperature. Either model is incomplete since coupling exists between TFE and impact ionization mechanisms. In addition, different devices may suffer from different breakdown mechanisms, depending on the details of the device design (insulator thickness, recess, channel composition, and so forth). In this study, the gate-to-drain breakdown voltage BV_{gd} is defined as the gate-to-drain voltage when the gate current is 1mA/mm.

3.4 RF Characteristics & Measurements

3.4.1 Scattering parameters 【16】

Scattering parameters, generally referred to as *S*-parameters, are fundamental to microwave measurement. This section discusses *S*-parameters and the motivation for their use. For a device such as field-effect transistor with the input and output terminals can be treated as a two-port network as shown in Fig.3.26. V_1 and I_1 are the voltage and current at the input, and V_2 and I_2 are the voltage and current at the output. Major characteristics, such as gain, return loss, and impedance matching can be calculated from known relationship among the input and output signals. The impedance parameters (*z*-parameters), conductance parameters (*y*-parameters) and hybrid parameters (*h*-parameters) are used to characteristic the devices because the parameter can be measured by open or short termination. The *z*-, *y*- and *h*-parameters can therefore be stated by the following equations:

z-parameters: $$\begin{bmatrix} V1 \\ V2 \end{bmatrix} = \begin{bmatrix} z11 & z12 \\ z21 & z22 \end{bmatrix} * \begin{bmatrix} i1 \\ i2 \end{bmatrix} \quad (3\text{-}12)$$

y-parameters: $$\begin{bmatrix} i1 \\ i2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} * \begin{bmatrix} V1 \\ V2 \end{bmatrix} \quad (3\text{-}13)$$

h-parameters: $$\begin{bmatrix} V1 \\ i2 \end{bmatrix} = \begin{bmatrix} h11 & h12 \\ h21 & h22 \end{bmatrix} * \begin{bmatrix} i1 \\ V2 \end{bmatrix} \quad (3\text{-}14)$$

When the frequency is up to several GHz, the *z*-, *y*-, *h*- parameters can not

be directly obtained by the open or short circuit because of the reflected wave from the open or short terminations. The open or short terminations will induce the network oscillation. Therefore the scattering parameters are used to characterize the performance of a device. Fig.3.27 shows the two-ports 1 and 2. The relation of the microwave signals and *s*-parameters can be described as

s-parameters: $$\begin{bmatrix} b1 \\ b2 \end{bmatrix} = \begin{bmatrix} s11 & s12 \\ s21 & s22 \end{bmatrix} * \begin{bmatrix} a1 \\ a2 \end{bmatrix} \quad (3\text{-}15)$$

a_1: the electric field of the microwave signal entering the component input

b_1: the electric field of the microwave signal leaving the component input

a_2: the electric field of the microwave signal entering the component output

b_2: the electric field of the microwave signal leaving the component output

By the definition, then,

$$s11 = \left.\frac{b1}{a1}\right|_{a2=0}, \quad s21 = \left.\frac{b2}{a1}\right|_{a2=0}, \quad s12 = \left.\frac{b1}{a2}\right|_{a1=0}, \quad s22 = \left.\frac{b2}{a2}\right|_{a1=0} \quad (3\text{-}16)$$

Therefore, s_{11} is the electric field leaving the input divided by the electric field entering the input, under the condition that no signal enters the output. The measurement includes instruments for the DC and RF measurement. Where a_1 and b_1 are electric fields, their ratio is a reflection coefficient. Similarly, s_{21} is the electric field leaving the output divided by the electric field entering the input, when no signal enters the output. Therefore, s_{21} is a transmission coefficient and is related to the insertion loss or the gain of the device. Similarly, s_{21} is a transmission coefficient related to the isolation of the device and specifies how

much power leaks back through the device in the wrong direction. s_{22} is similar to s_{11}, but looks in the other direction into the device. The *s*-parameters have both the amplitude and phase.

3.4.2 Current gain cutoff frequency f_T 【17】

Traditionally, transistors are characterized using figures of merit such as the unity current-gain cutoff frequency (f_T). Consider a transistor characterized by the following small-signal *y*-parameters

$$i_1 = y_{11}(\omega)V_1 + y_{21}(\omega)V_2 \tag{3-17}$$

$$i_2 = y_{21}(\omega)V_1 + y_{22}(\omega)V_2 \tag{3-18}$$

The currents and voltages are defined in Fig. 3.26. For example, we use the *y*-parameters of a FET in the common source configuration in Fig. 3.28.

$$i_g = y_{gg}(\omega)V_{gs} + y_{gd}(\omega)V_{ds} \tag{3-19}$$

$$i_d = y_{ds}(\omega)V_{gs} + y_{dd}(\omega)V_{ds} \tag{3-20}$$

The unity short-circuits current-gain cut-off frequency is defined as the frequency at which the short-circuit current gain is unity:

$$h_{21}(\omega) = \left| \frac{y_{21}(\omega_T)}{y_{11}(\omega_T)} \right| = 1 \tag{3-21}$$

Since the HEMT is the common source configuration, the maximum short-circuit current gain can be approximated by

$$\left|\frac{y_{21}(\omega_T)}{y_{11}(\omega_T)}\right| = \left|\frac{y_{ds}(\omega_T)}{y_{gg}(\omega_T)}\right| \approx \frac{g_m}{\omega C_g W_g L_g} \qquad (3\text{-}22)$$

Where g_m is the transconductance. Notice the 1/ω decrease with frequency (20 dB per decade) using 20log (y_{21}/y_{11}) of the short-circuit gain. The intrinsic *S* parameters are used to determine the unity current-gain cut-off frequency (f_T). It can be determined by the extrapolation of the short-circuit current gain $h_{21} = 0$ dB. h_{21} can be defined as

$$h_{21} = \frac{2s_{21}}{(1-s_{11})(1+s_{22})+s_{12}s_{21}} \qquad (3\text{-}23)$$

Fig. 3.29 shows the definition of the cut-off frequency (f_T).

3.4.3 Maximum frequency of oscillation f_{max} 【17】

The microwave performance of a transistor is usually characterized by the maximum stable power gain as a function of frequency. The maximum power gain is obtained by simultaneously matching the input and output to obtain a conjugate match. Conjugate match means that the source impedance Z_S and the load impedance Z_L satisfy simultaneously:

$$Z_S=Z^*_{IN}, \qquad Z_L=Z^*_{OUT}$$

Where Z_{IN} is the input impedance of the two-port network measured at port 1 with the load impedance Z_L connected at port 2 and where Z_{OUT} is the output impedance of the two-port network measured at port 2 with the source impedance Z_S connected at port 1. The maximum power stable gain (G_{max}) consisting of the maximum available gain (MAG) and the maximum stable gain (MSG) were derived from the *S*-parameter data by the equation:

$$G_{MAX}=\left|\frac{S_{21}}{S_{12}}\right|K-\sqrt{(K^2-1)}, \tag{3-24}$$

Where K is the Rollett stability factor

$$K=\frac{1-|S_{11}|^2-|S_{22}|^2+|D|^2}{2|S_{12}||S_{21}|} \tag{3-25}$$

$$D=S_{11}S_{22}-S_{12}S_{21}$$

The MAG is the highest power gain of the two-port network with the impedance-matched input and output. The MAG of a transistor can only be obtained when the transistor is unconditionally stable, *i.e.* $K > 1$. The MSG is the highest power gain of a two-port network with the resistive loaded in both input and output ports. The MSG can be obtained if the transistor where potentially unstable according to:

$$MSG=MAG|_{K=1}=\left|\frac{S_{21}}{S_{12}}\right| \tag{3-26}$$

The device maximum power gain cut-off frequency can then be defined as the frequency at $G_{max} = 0$ dB.

The comparison of the high-frequency performance of two-port devices is usually done using the unilateral power gain U derived by Mason:

$$U = \frac{\frac{1}{2}\left|\frac{S_{21}}{S_{12}} - 1\right|^2}{K\left|\frac{S_{21}}{S_{12}}\right| - Re\left(\frac{S_{21}}{S_{12}}\right)} \qquad (3\text{-}27)$$

U is the maximum available power gain (MAG is introduced in the previous section) of a device once it has been unilateral zed ($y_{12} = 0$) using lossless feedback techniques.

The maximum frequency of oscillation f_{max} is then defined as the frequency at which U is unity. f_{max} is often referred to as the frequency at which a three-port device switches form active to passive. U can then be written

$$U(\omega) = \left(\frac{\omega_{max}}{\omega}\right)^2 \qquad (3\text{-}28)$$

The unilateral power gain will then decrease at a rate of 20 dB per decade (using 10logU) like the short-circuit current gain.

3.5 Noise figure 【18】

Noise is related to the device channel and capacitive coupling between the channel and the gate. The gate noise is represented by a gate-current noise generator i_{ng}^2 and is caused by charge fluctuation in the channel, which in turn induces the fluctuation of compensating charge on the gate electrode. The gate-noise is proportional to f^2 in HEMTs. The channel noise is represented by a drain-current noise generator i_{nd}^2 and is caused by various physical mechanisms driven by the electric field in the channel. In the linear region of the device channel, the channel noise is caused by thermal noise (Johnson noise). A thermal noise voltage caused in the channel leads to a modulation of the channel resistance and causes a drain voltage fluctuation at the channel end (drain). The corresponding drain noise current is inversely proportional to $g_m I_{DS}$. In the high-field region, hot electron scattering, intervalley scattering, and high diffusion noise contribute to the channel noise.

Another noise source is gate leakage. A new model that takes this effect into account by an additional parallel resistor to the gate capacitance and the resistor R_i has been proven to a good correlation between predicted and measured minimum noise figures even at low frequencies. The negative influence of the gate leakage on the noise figure vanishes at higher frequencies. Noise figure reflects the noise added to the signal by the imperfect amplifier, and is defined as the signal-to-noise ratio (S/N) of the input signal divided by the signal-to-noise ratio of the output signal.

$$F = (S_i/N_i)/(S_0/F_0) \quad (3\text{-}29)$$

It is usually expressed in dB:

$$NF = 10\log F \quad (3\text{-}30)$$

We shall use *F* to designate absolute noise figure and NF to designate figure expressed in dB. The noise performance of a FET may be quantified by the noise figure, NF, which is a function of frequency, FET bias voltages, and impedance matching. Another noise figure of FETs structure is shown as the following equation.

$$NF = 1 + \sqrt{2}\frac{f}{f_t}\sqrt{g_m(R_S + Rg)}, f_t = \frac{g_m}{2\pi C_{gs}} \quad (3\text{-}31)$$

In general, high source-drain current contributes to noise by electron scattering, and this noise is reduced as the current is reduced. However, reducing the current too close to pinch-off reduces the transconductance, which causes increased noise figure because of decrease gain. There will exist an optimum gate bias that presents the best compromise.

Figures:

Cap Layer	$In_{0.52}Ga_{0.47}As$ n+ 5E18 200Å
Schottky Layer	$In_{0.52}Al_{0.48}As$ 200Å **Si planar-doped 4.5E12**
Spacer Layer	$In_{0.52}Al_{0.48}As$ 50Å
Channel Layer	$(In_{0.53}Ga_{0.47}As)_m(InAs)_n$ SL 150Å 10 period
Buffer Layer	$In_{0.52}Al_{0.48}As$ 300Å
Buffer Layer	Metamorphic InAlAs Buffer
Substrate	S.I. GaAs Substrate

Fig.3.1 $(In_{0.53}Ga_{0.47}As)_m(InAs)_n$ superlattice MHEMT structure

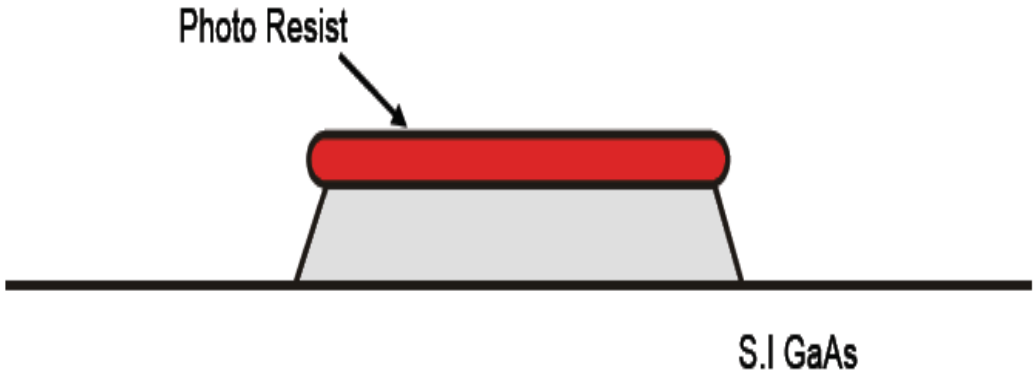

Fig.3.2 Schematic of mesa etching

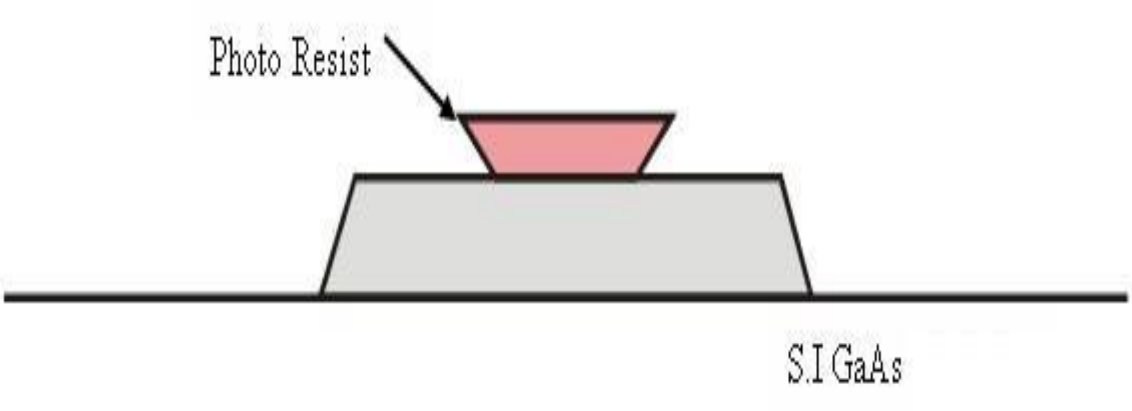

Fig.3.3 Schematic of ohmic photo

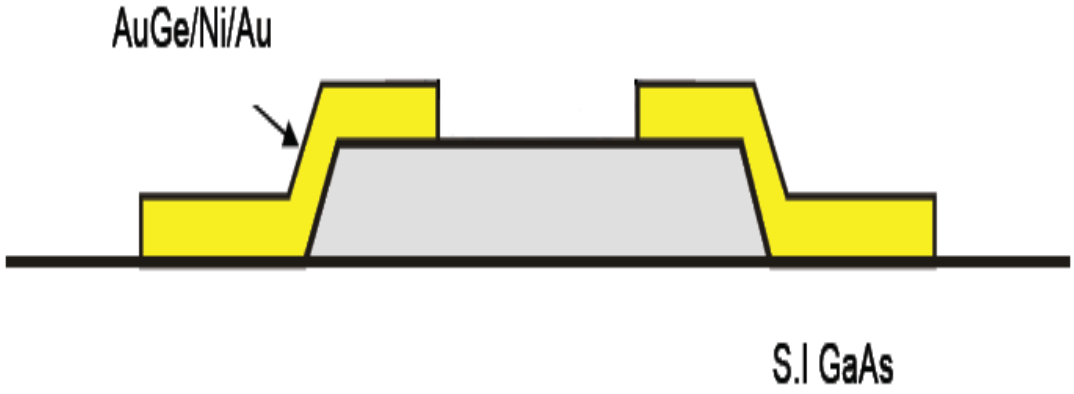

Fig.3.4 Schematic of the cross section of the device after ohmic metal (AuGe/Ni/Au) deposition

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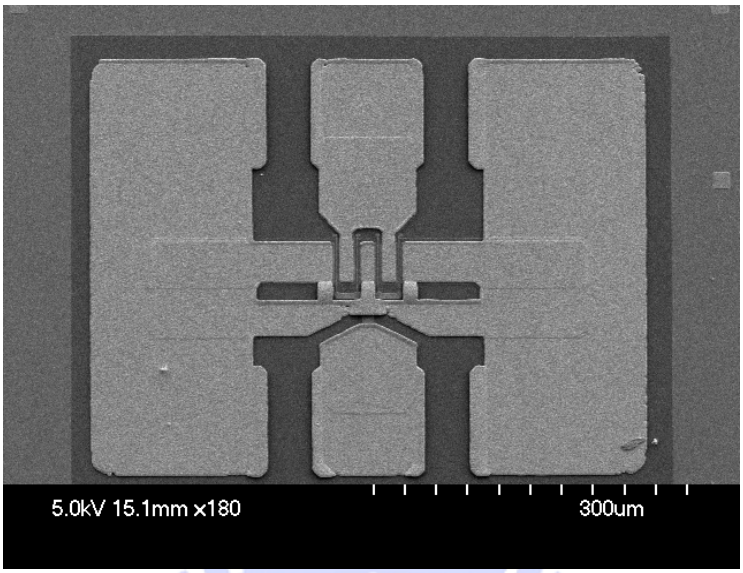


Fig.3.5 Device layout of the sepsration MHEMT

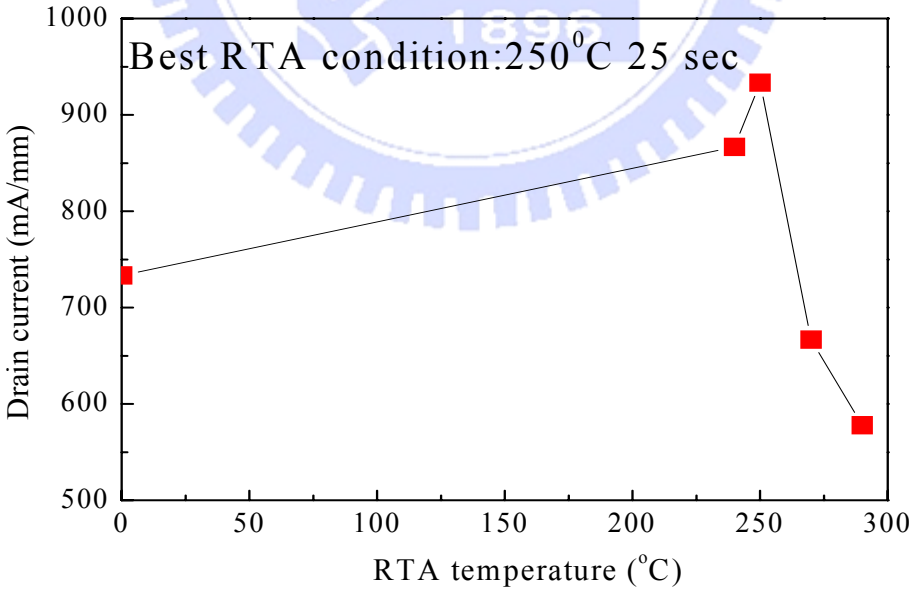


Fig.3.6 Drain current vs. RTA temperature

Space (mm.)	3	5	10	20	36
1	5.742	7.816	14.14	26.807	47
2	5.636	7.99	13.943	26.83	47.11
Orange products (W /[])	9.3011E +01				
Blue products (W /[])	9.3307E +01				
Orange rC boundary line (W-cm^2)	4.2479E-07				
Blue line rC (W-cm^2)	3.9480E-07				

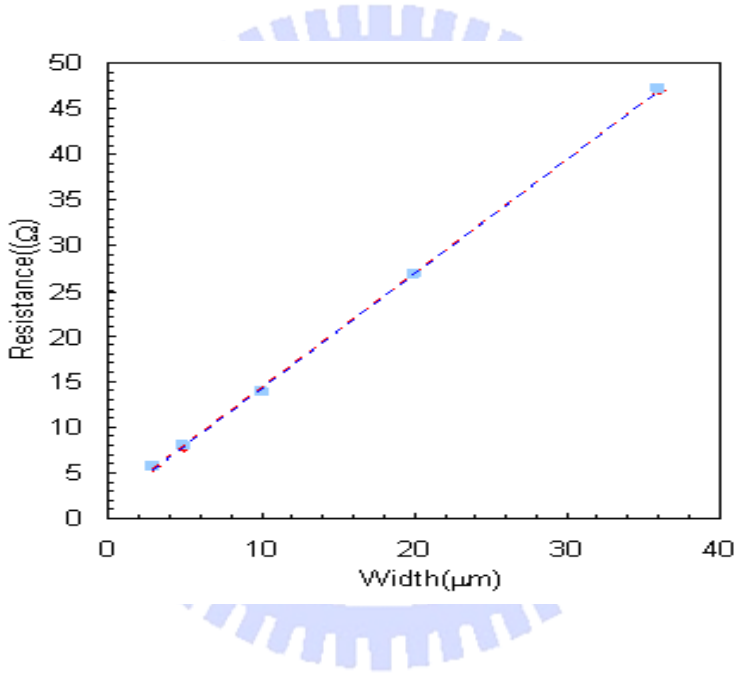


Fig.3.7 Ohmic contact resistance of the superlattice MHEMT

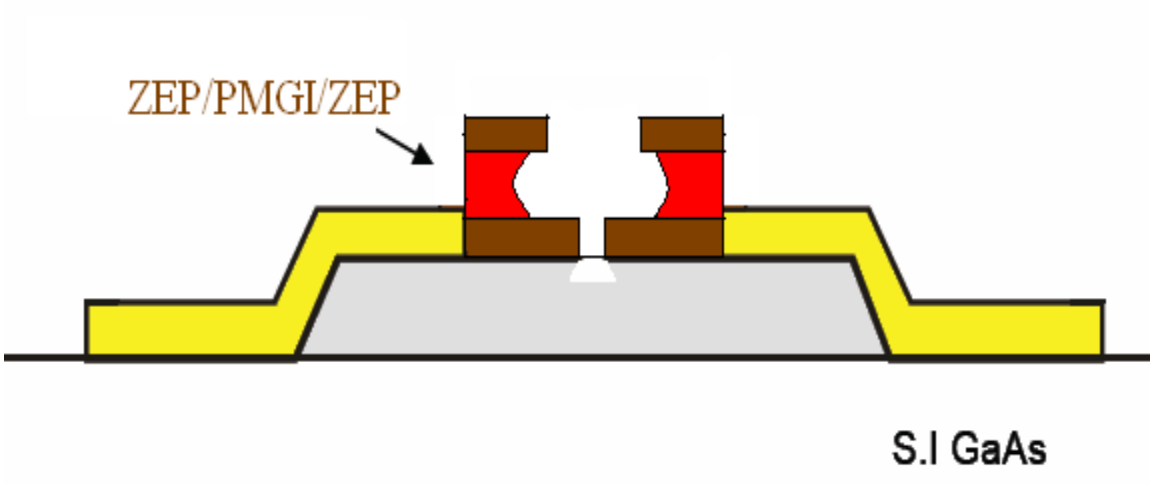


Fig.3.8 Ebeam T-shaped gate followed by recess

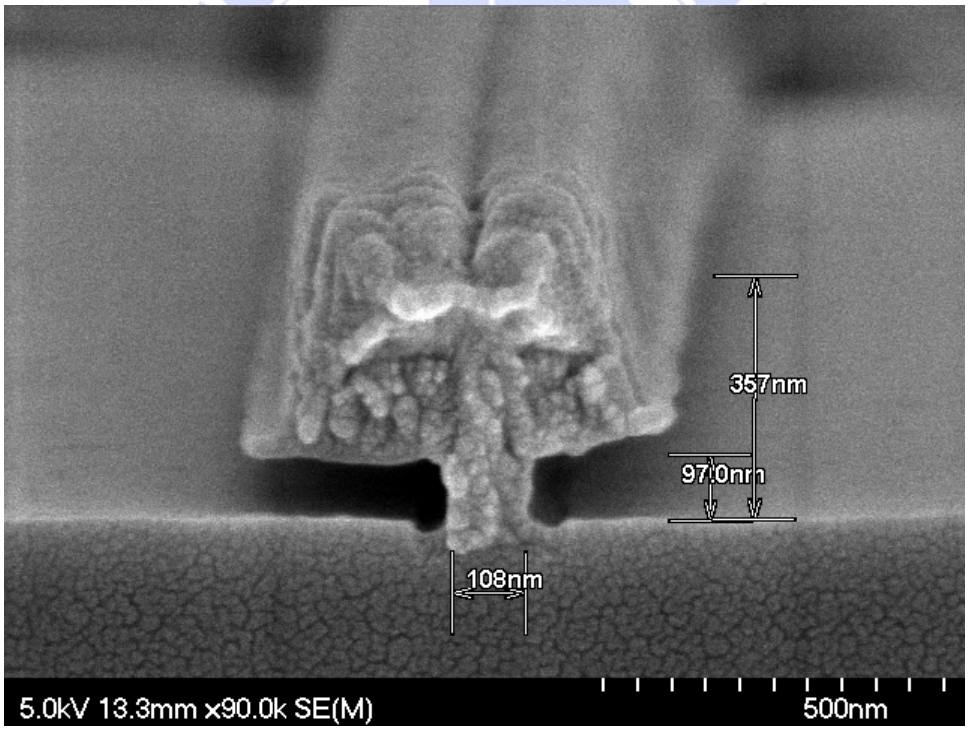


Fig.3.9 SEM Micrograph of the cross section of the T-shaped gate profile

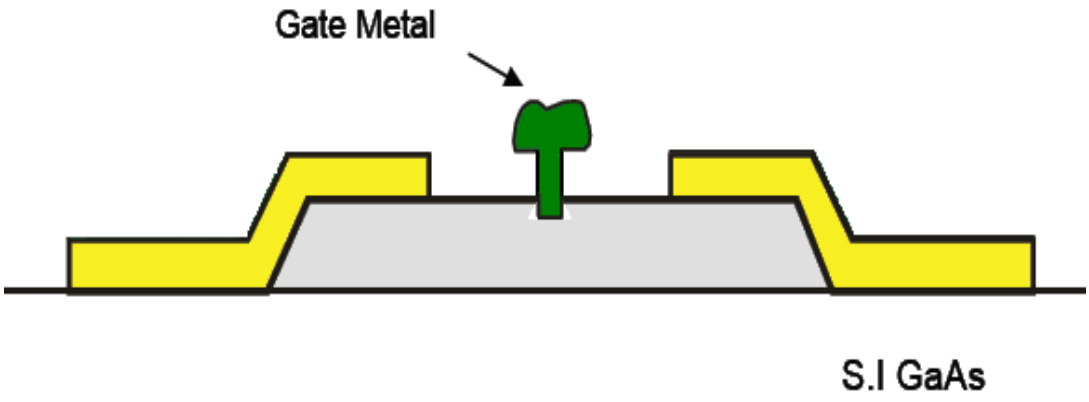


Fig.3.10 Schematic of the device of the gate metal (Ti/Pt/Au) deposition

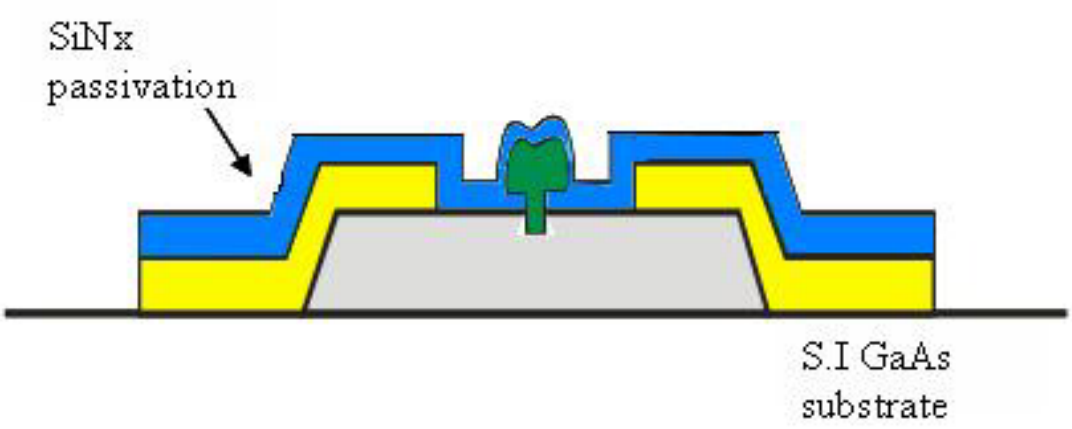


Fig.3.11 Schematic of the cross section of the device after SiN_x passivation

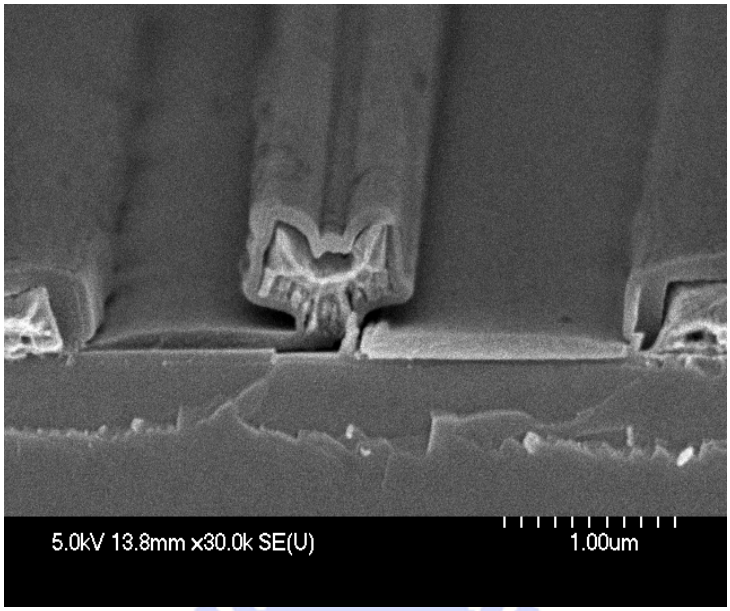


Fig.3.12 SEM Micrograph of the device after SiNx passivation

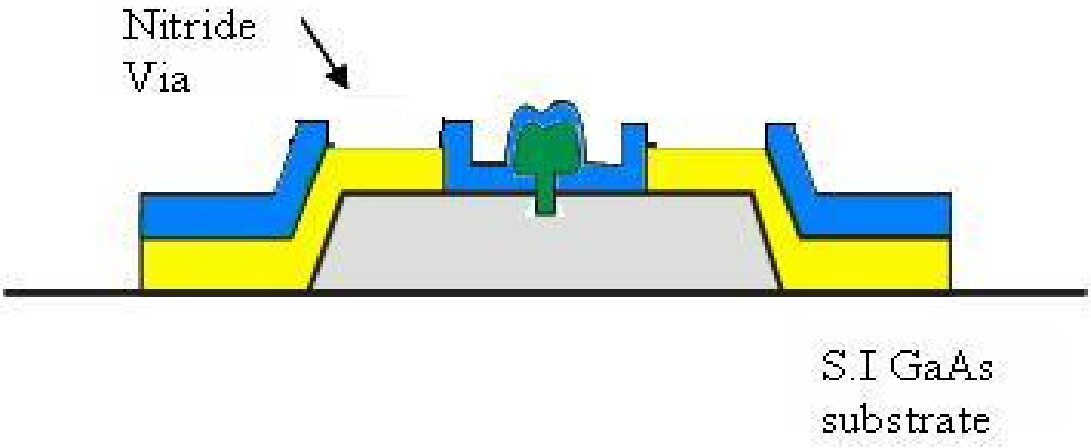


Fig.3.13 Schematic of the device after nitride via holes etching

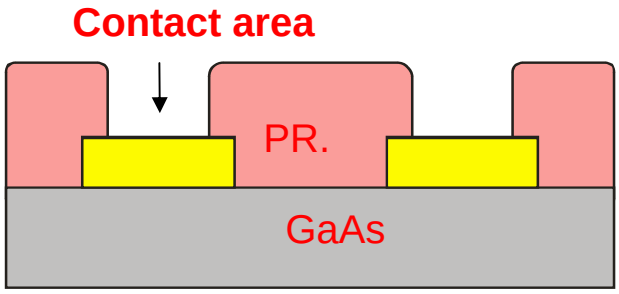


Fig.3.14 Schematic of the device after first photolithography for plating via holes

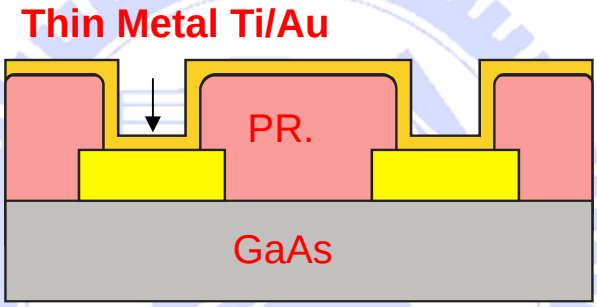


Fig.3.15 Schematic of the device after thin metals Ti/Au deposition

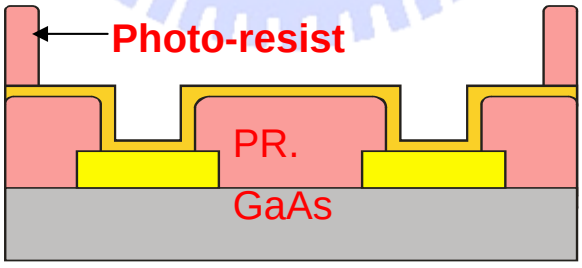


Fig.3.16 Schematic of the second photolithography for airbridge plating

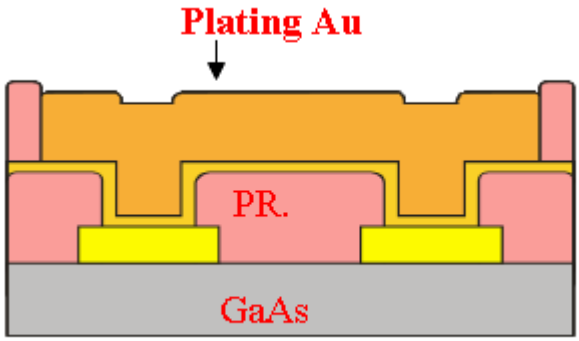


Fig.3.17 Schematic of the device after Au electroplating

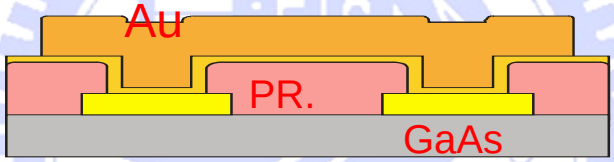


Fig.3.18 Schematic of the device after plating at Second photo-resist removal

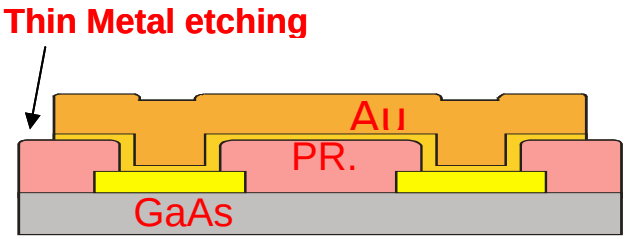


Fig.3.19 Schematic of the device after thin metal etching

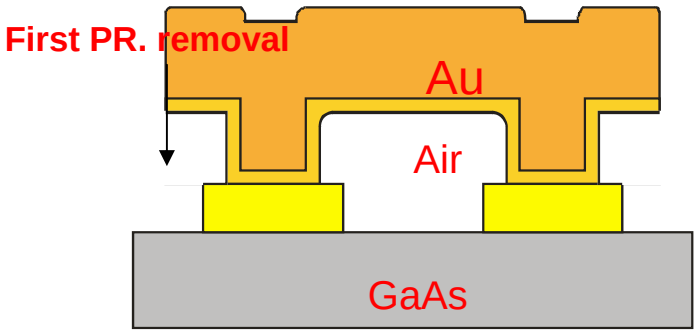
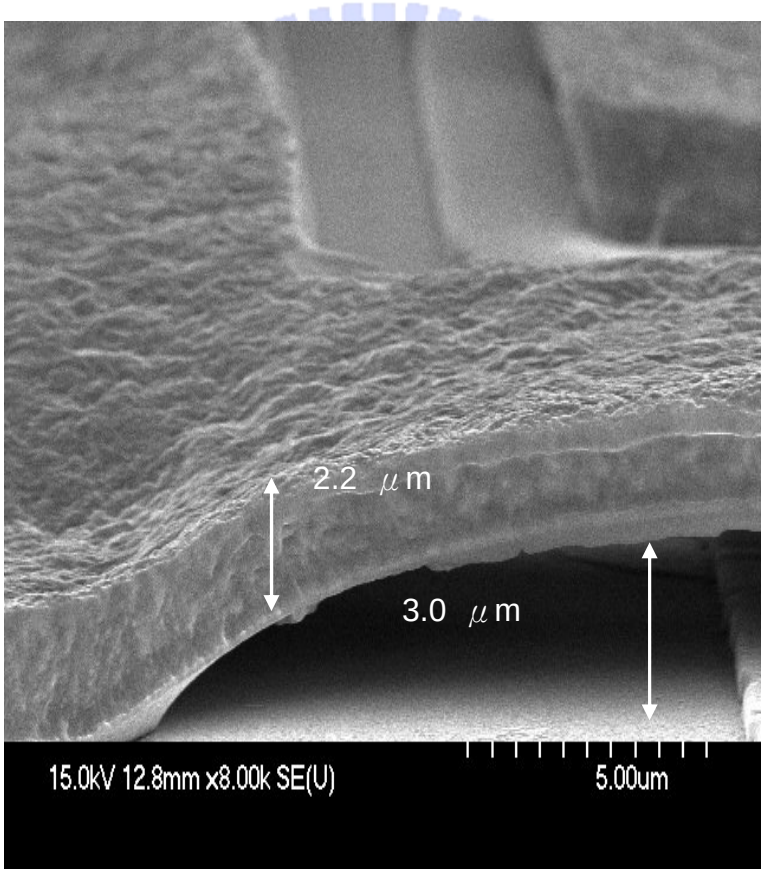
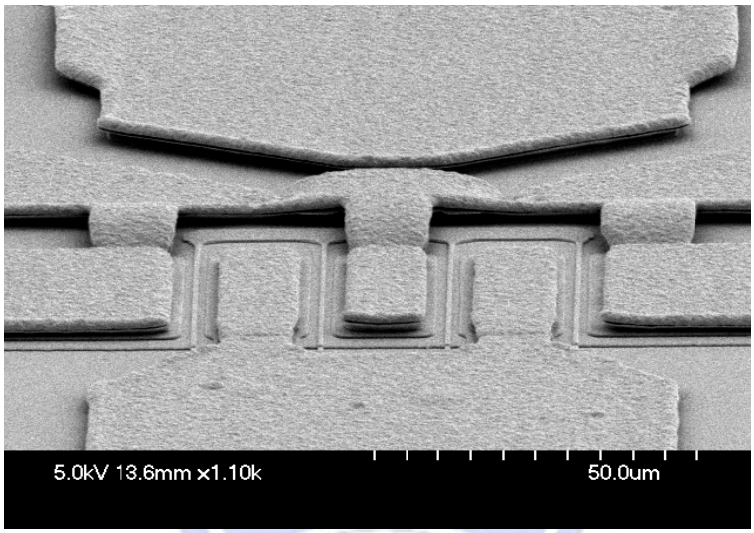


Fig.3.20 Schematic of the airbridge process after first photo-resist removal



(a) SEM Micrograpgy of the side view of the Au airbridges



(b) SEM Micrograph of the front view of the Au airbridges

Fig.3.21 (a) SEM photo of the side view of the airbridges (b) SEM photo of the front view of the airbridges

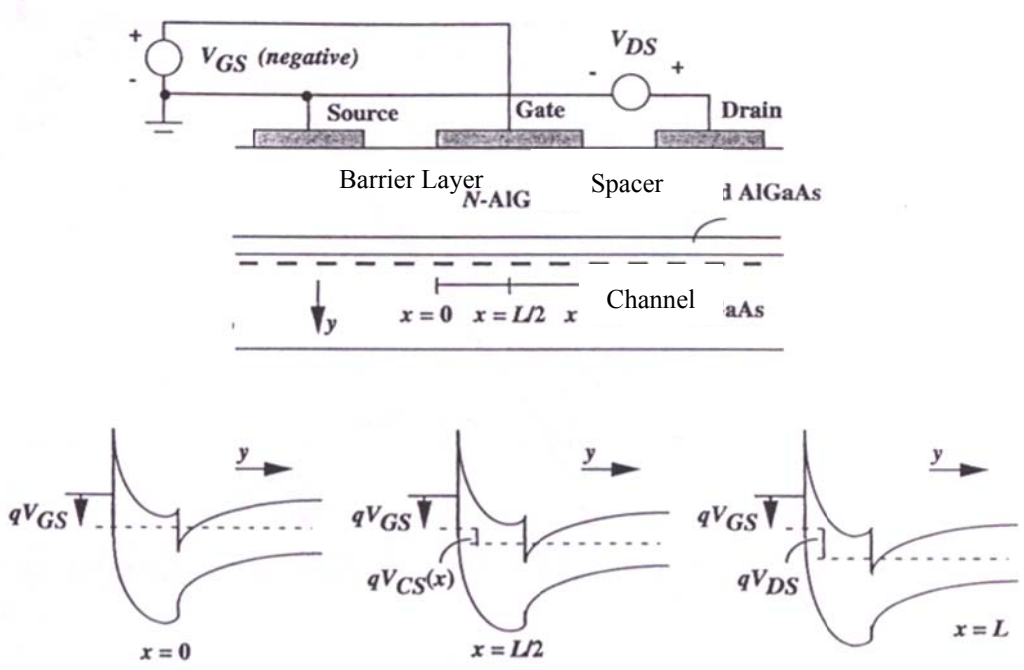


Fig.3.22 Band diagrams at three different locations along the channel of HEMT

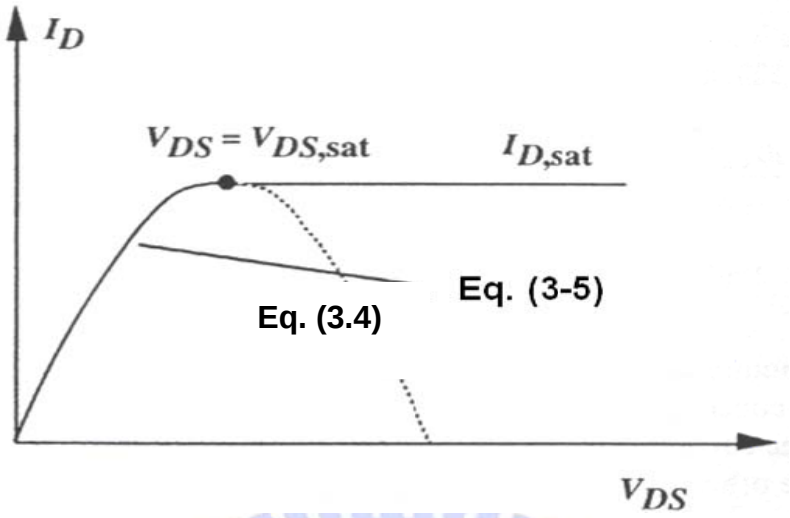
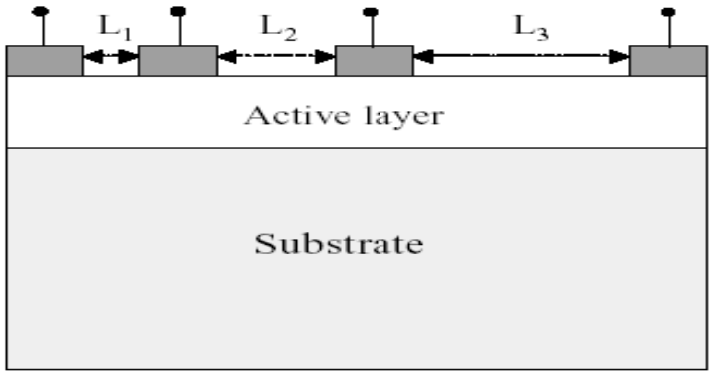


Fig.3.23 Actual I-V characteristics and those predicted by Eq. (3-4)

(a)



(b)

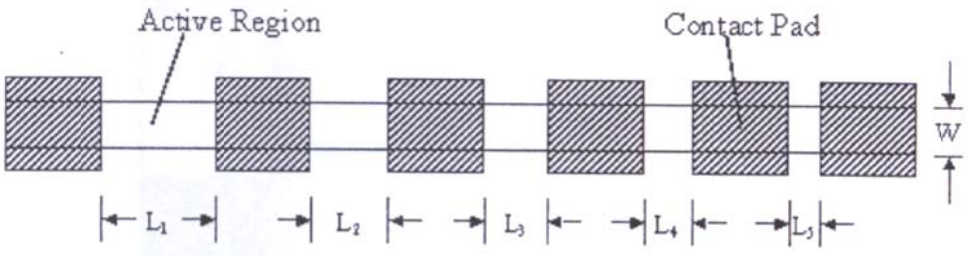


Fig.3.24 (a) The side view of the TLM patterns, (b) The top view of TLM patterns.

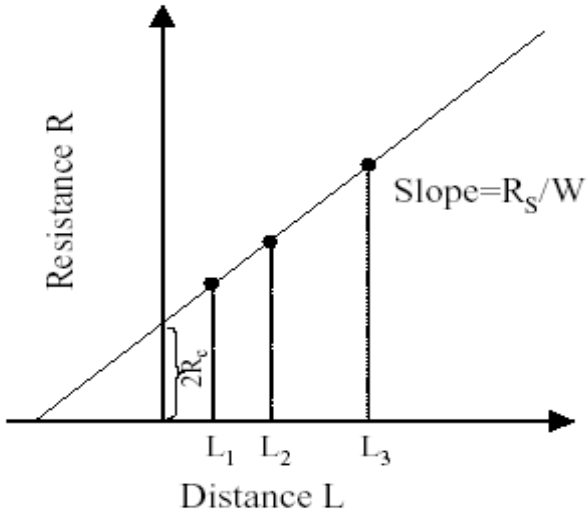


Fig.3.25 The illustration of utilizing TLM to measure ohmic contact resistance

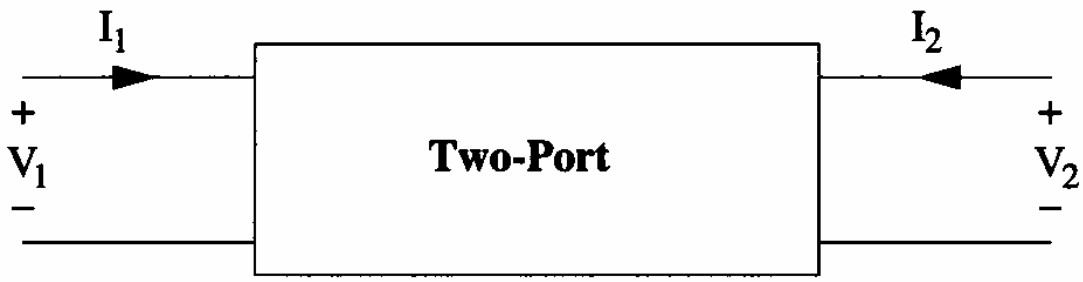


Fig.3.26 The equivalent two-port network schematic at low frequency

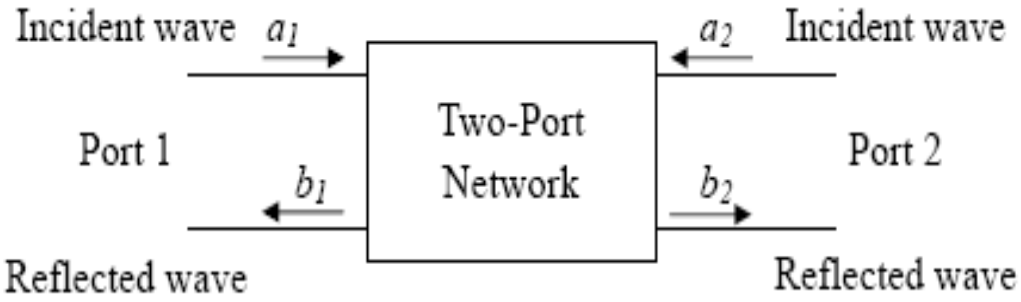


Fig.3.27 The equivalent two-port network schematic at high frequency

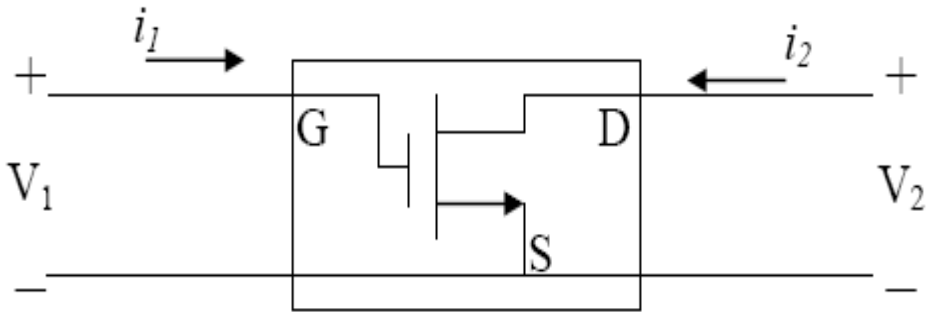


Fig.3.28 Small signal representation of a common source FET

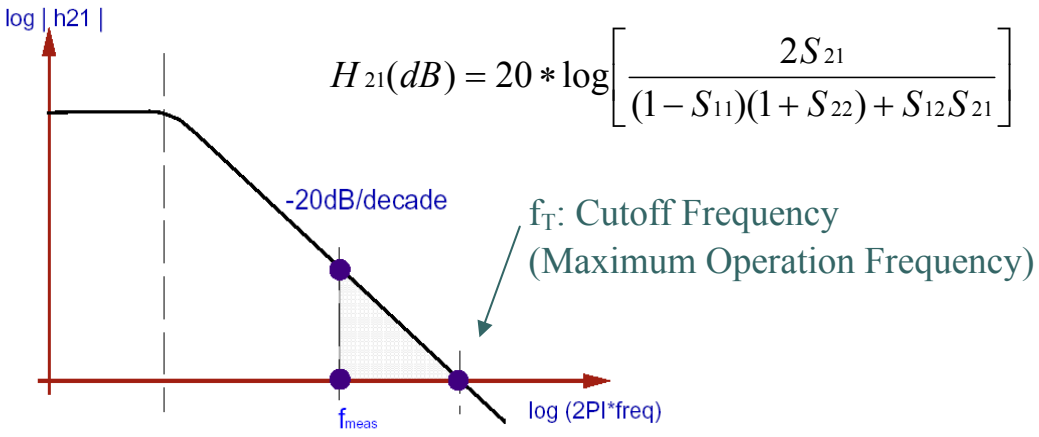


Fig.3.29 Definition of the Cutoff Frequency f_T

Chapter4

Results and discussions

In order to characterize and compare the device performance of different structures, devices with two kinds of channel layer were fabricated. Sample A is GaAs-based metamorphic HEMT structure with $In_{0.53}Ga_{0.47}As$/InAs superlattice channel, while sample B is GaAs-based metamorphic HEMT structure with $In_{0.53}Ga_{0.47}As$ channel. The DC and RF performances of these two samples are presented and compared as follows.

4.1 DC characteristics

4.1.1 *I-V* characteristics

The current-voltage characteristics of the 2×50 μm devices with samples A and B have the same gate length of 100 nm and were measured on wafer by using HP4156. The characteristics of the drain-source voltage vs. drain current are shown in Fig.4.1. The characteristics of gate-source voltage vs. transconductance at different drain voltages are shown in Fig.4.2. Sample A exhibits a higher $I_{ds,sat}$ (476 mA/mm) than sample B (344 mA/mm). At the same applied bias condition, the maximum transconductance ($g_{m,max}$) of sample A was 886 mS/mm at a gate bias voltage of -0.35 V which was higher than $g_{m,max}$ of sample B which was 709 mS/mm at a gate bias voltage of -0.2V. Sample A which has higher electron mobility and higher indium content due to InGaAs/InAs superlattice channel shows larger $I_{DS,sat}$ and g_m than that of sample

B.

However, when the low bandgap InAs layers were inserted into the superlattice structure, impact ionization effect occurred at higher drain voltage. As shown in Fig.4.1, the drain-source current increased rapidly when the drain voltage was larger than 0.6 V.

4.1.2 Breakdown voltage

As shown in Fig.4.3, the gate-drain breakdown voltages (V_{br}), defined by 1 mA/mm of drain current, were 4.56 V and 7.92 V for samples A and B for devices with gate length of 100 nm, respectively. The gate-drain breakdown voltage is related to the interface of Schottky barrier. Because the lower bandgap material of InAs layer was adopted in the superlattice structure, the G-D breakdown of the HEMTs with superlattice channel was lower than HEMTs with InGaAs channel.

4.1.3 Impact ionization effect

Because small bandgap InAs layer is used in the superlattice channel, the drain current increases rapidly due to the impact ionization effect. This effect is best understood by considering the energy band diagrams at different gate biases as shown in Fig.4.4. When the V_{gs} is negative, some of the holes that are produced during impact ionization can get across the InAlAs barrier layer and are collected at the gate. As V_{is}, the voltage between gate and InAlAs barrier layer, is made more positive due to the holes at the gate, the energy bands

straighten out and the vertical field drops as in Fig.4.4 (b). Hence, at flat-band state, there is no field to aid hole collection by the gate. In Fig.4.4 (c), when V_{is} is increased beyond flat-band state, the field changes direction, and hole transfer to the gate gets suppressed completely.

In Fig.4.5, the impact ionization can be proved. The gate current increased rapidly as drain voltage was larger than 0.6 V, which is as observed in Fig.4.1 (a). This is because some holes produced during gate voltage increase transferred over the barrier to the gate region due to the impact ionization effect.

4.2 RF characteristics

4.2.1 Unit current gain cut-off frequency (f_T) & maximum frequency of oscillation (f_{max})

Before the RF measurements, optimum DC bias have to be found in order to obtain the maximum current gain and maximum available/stable gain. Fig.4.6 shows the *S*-parameters of samples A and B extracted from 1 to 40 GHz under optimum DC bias. The extrinsic current gain cut-off frequency (f_T) and maximum gain cut-off frequency (f_{max}) are defined as the frequency extrapolated at 40 GHz by a -20 dB/decade slope. As shown in Fig.4.6, the current gains are 12 dB and 11.3 dB at 40 GHz for sample A and B, respectively. The MAG/MSG values are 11.7 dB and 13.1 dB at 40 GHz for samples A and B. Both the f_T and f_{max} values for sample A are 170 GHz and 170 GHz respectively under the bias condition of V_{ds} = 1 V and V_{gs} = -0.3 V. On the other hand, the f_T and f_{max} values of sample B are 150 GHz and 180 GHz under the bias condition of V_{ds} = 1 V

and V_{gs} = -0.3 V. Apparently, the f_T of sample A is higher than that of sample B owing to higher transconductance value.

4.2.2 Noise characteristics

Since higher drain current will lead to high noise due to electron scattering effect, the noise can be reduced as the current decreases. However, decreasing the drain current will lower the transconductance and lower transconductance causes higher noise figure with lower gain. Therefore, there exists an optimum bias condition to achieve the lowest noise performance. Fig.4.7 shows the minimum noise figure (F_{min}) depends on the drain-source current at the fixed frequency of 16 GHz. The applied drain voltage is fixed at 1v. The lowest F_{min} can be observed around Ids of 10.42 mA and 4.74 mA for samples A and B, respectively. The noise performances shown in Fig.4.8 are measured over a frequency range of 1 GHz to 16 GHz with the optimum bias conditions. The measured minimum noise figures (NF) at 16 GHz was 0.75 dB and 0.77 dB for samples A and B, respectively. Both the samples A and B showed low noise performance over a frequency range of 1 GHz to 16 GHz.

4.3 Summary

Table 4.1 summarizes the DC characteristics of the devices with different channel structures. Based on the measured DC performances evaluations, devices with superlattice channel show higher drain saturation current and current gain due to higher indium content in the channel layer. However these devices suffered from lower gate-drain breakdown voltage and impact ionization

effect owing to the small band gap of InAs layers used in the superlattice structure. In addition, the reducing of alloy scattering effect by using superlattice structure is demonstrated both on dc and RF performance.

Tables 4.2 and 4.3 also show a summary of the RF and noise performances. It can be seen that sample A has the higher value of f_T and better noise performance.

Tables:

	Sample A	Sample B
Gate length (Lg)	100nm	100nm
Drain-Source Current (I_{DSS}) @Vd = 1V	476	344
Transconductance (g_m) @Vd = 0.9V	886	709
Threshold Voltage (V_T)	-0.8	-0.8
Breakdown Voltage (V_{br})	5.5	7.92

Table 4.1 Summary of the DC performances between Sample A and Sample B

MHEMT devices	L_g (nm)	H_{21} @40GHz (dB)	MAG/MSG @40GHz (dB)	f_T (GHz)	f_{max} (GHz)
Sample A	100	12	11.7	170	170
Sample B	100	11.3	13.1	150	180

Table 4.2 Summary of RF performances between samples A and B

MHEMT devices	L_g (nm)	F_{min} (dB)	NF_{min} (dB) @ 16GHz
Sample A	100	0.84	0.75
Sample B	100	0.38	0.77

Table 4.3 Summary of noise figure between samples A and B

Figures:

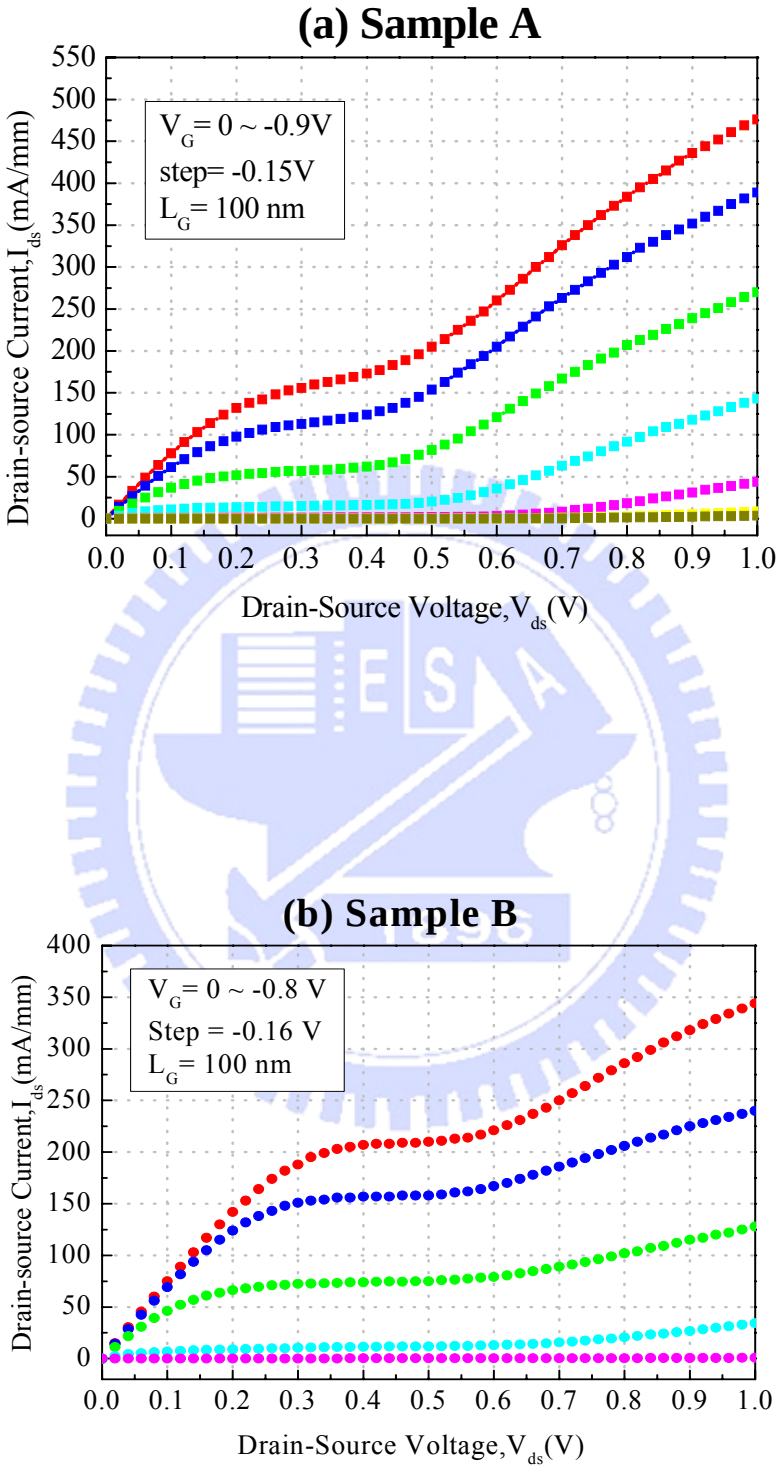


Fig. 4.1 Drain-source current vs. drain-source voltage of (a) sample A and (b) sample B

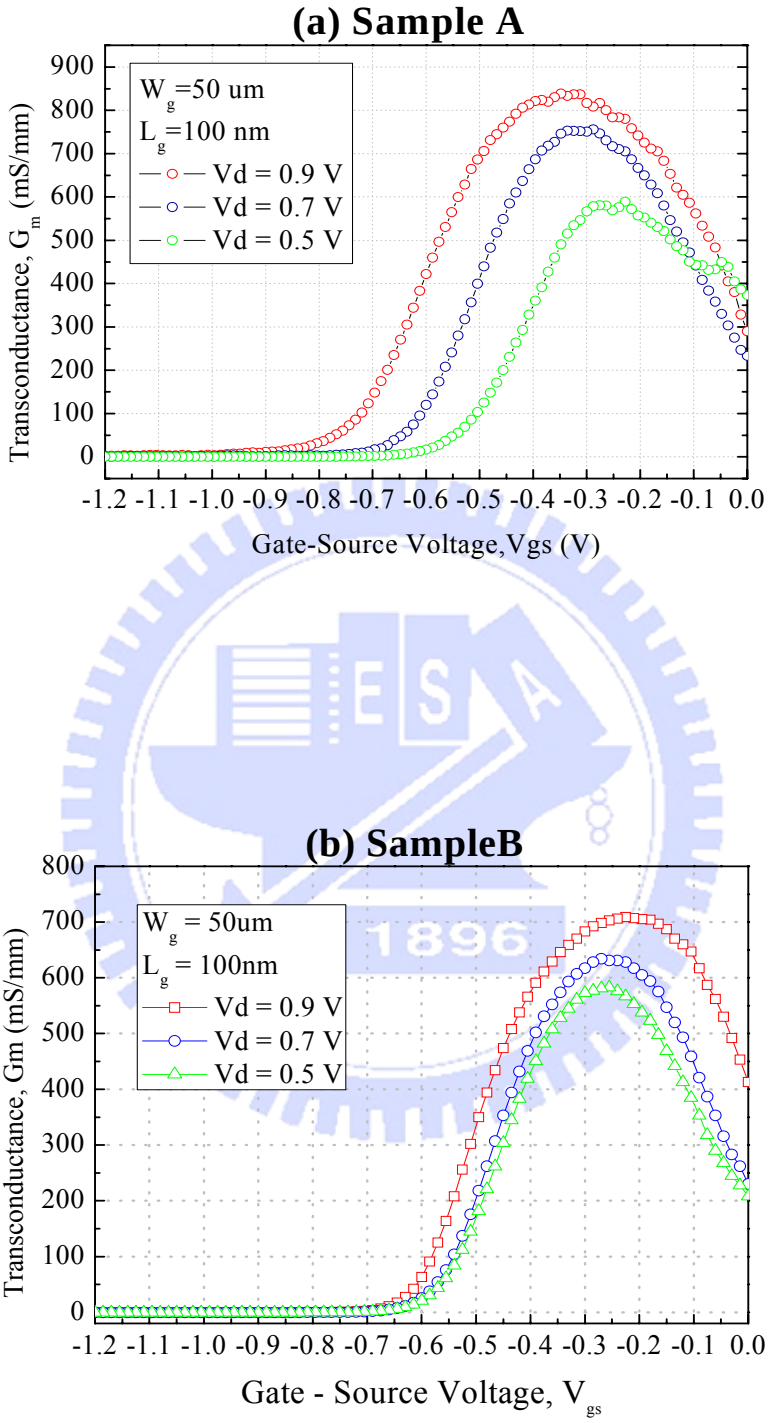


Fig. 4.2 Transconductance vs. gate-source voltage of (a) sample A and (b) sample B

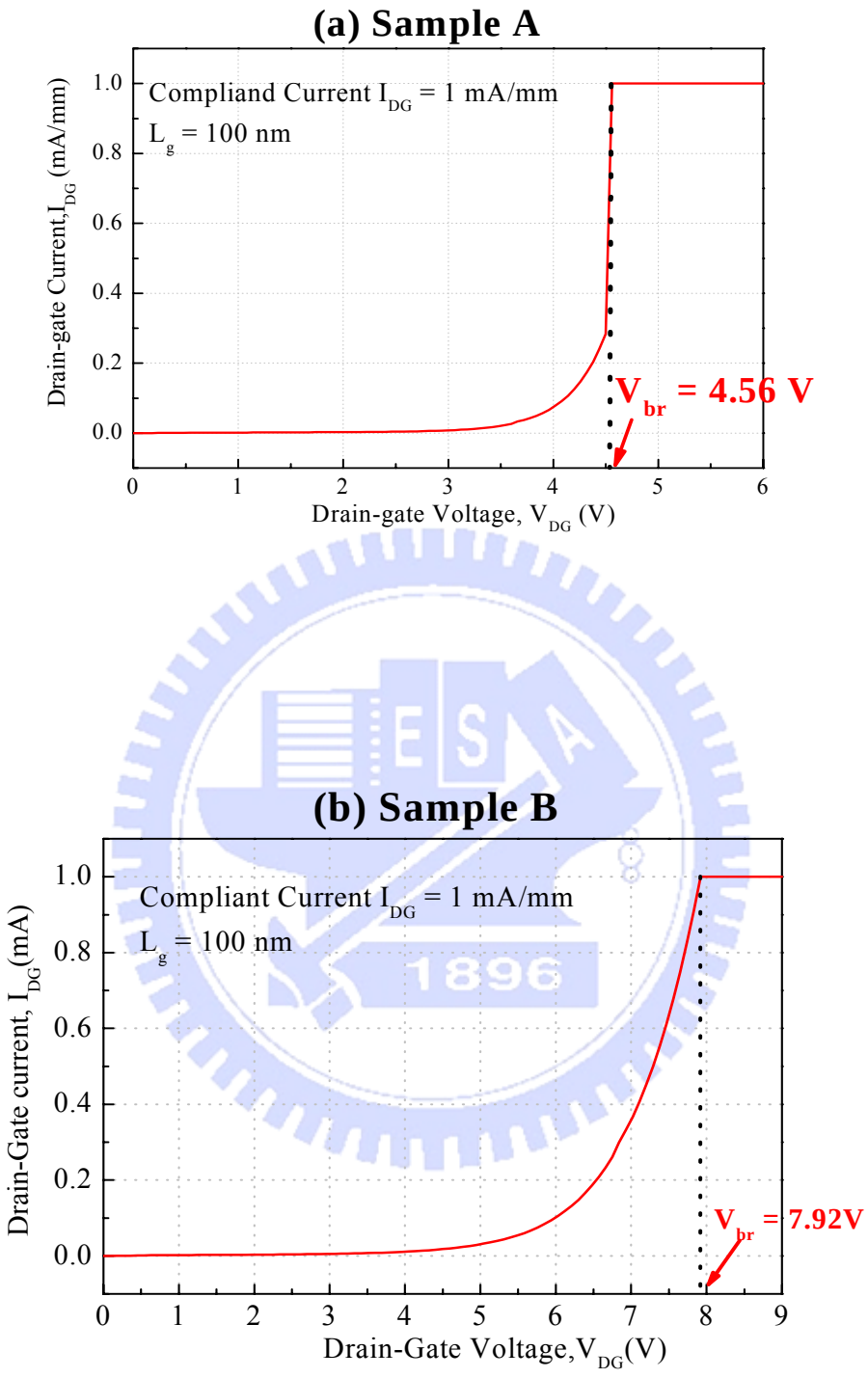
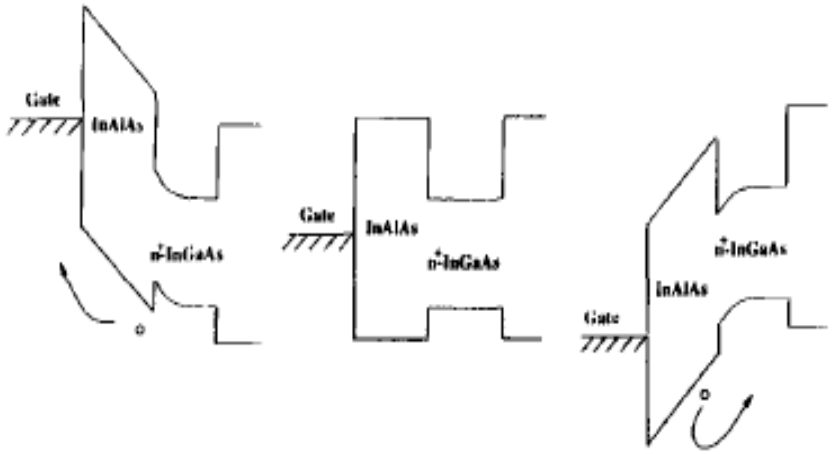


Fig. 4.3 Breakdown voltage, V_{br} of (a) sample A and (b) sample B



(c) depletion (b) Flat-band (a) accumulation

Fig. 4.4 Band diagrams for: (a) depletion, (b) flat-band, and (c) accumulation, indicating the effect of the barrier between the gate and channel on hole extraction by the gate electrode. 【19】

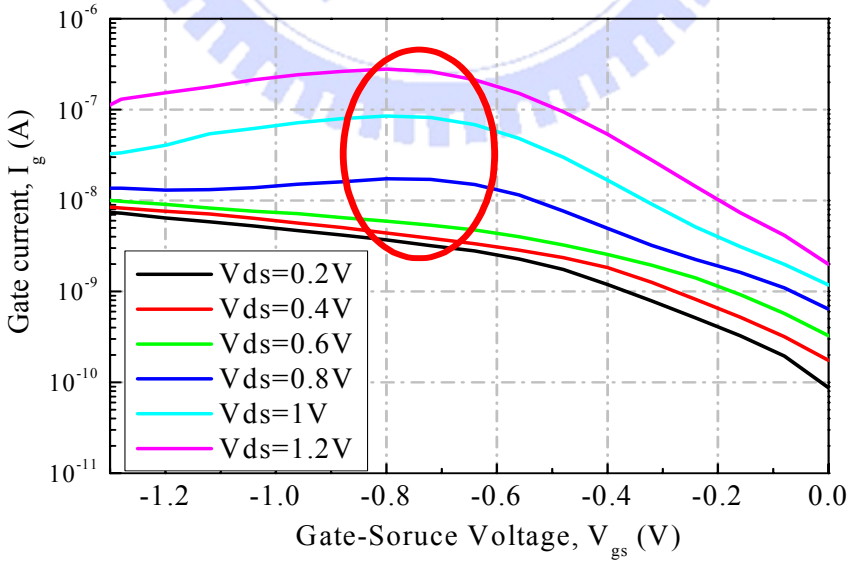


Fig. 4.5 Gate-source voltage, V_{gs} vs. gate current, I_g of sample A

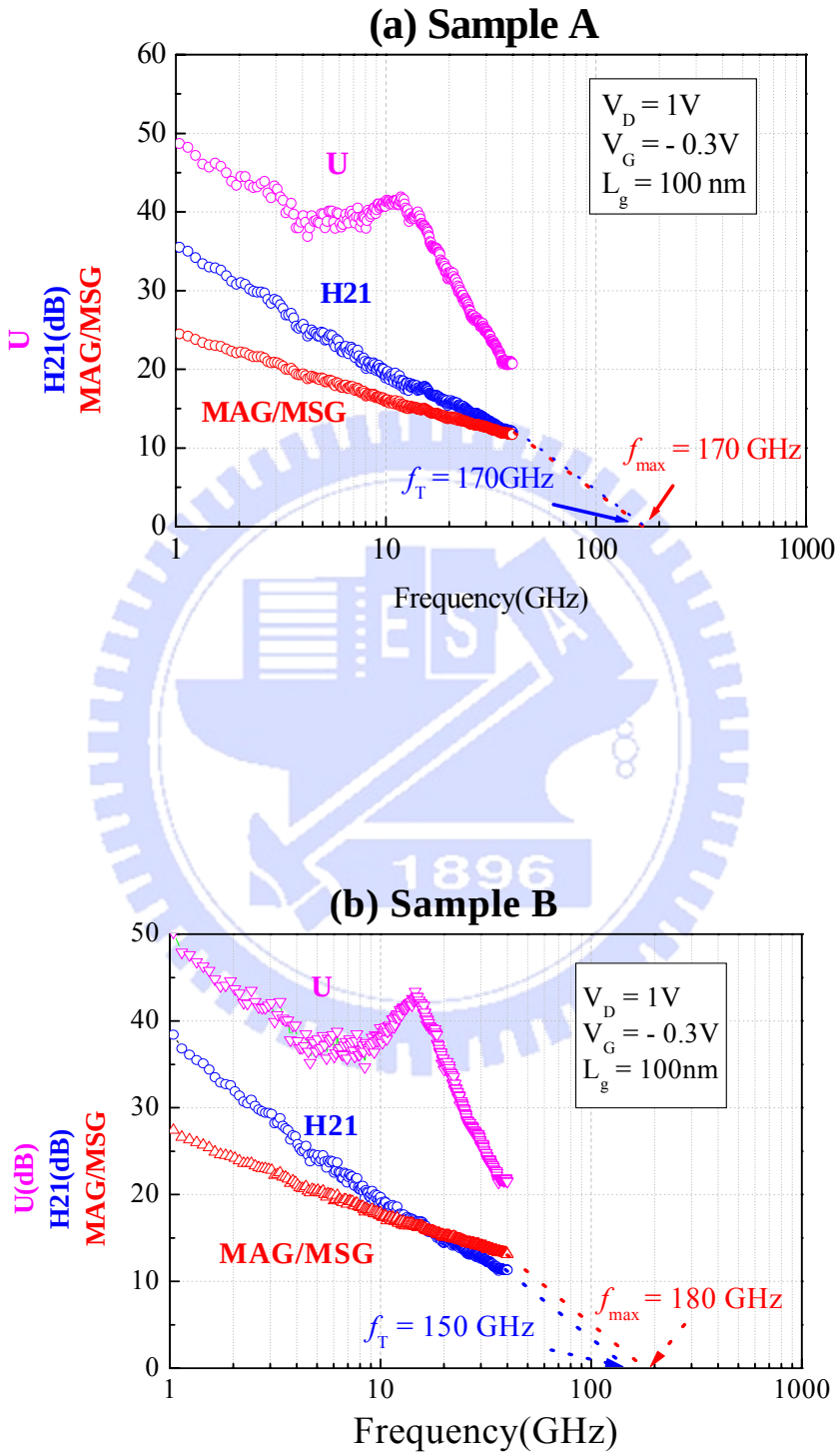


Fig. 4.6 Maximum available/stable power gain and current gain of (a) sample A and (b) sample B

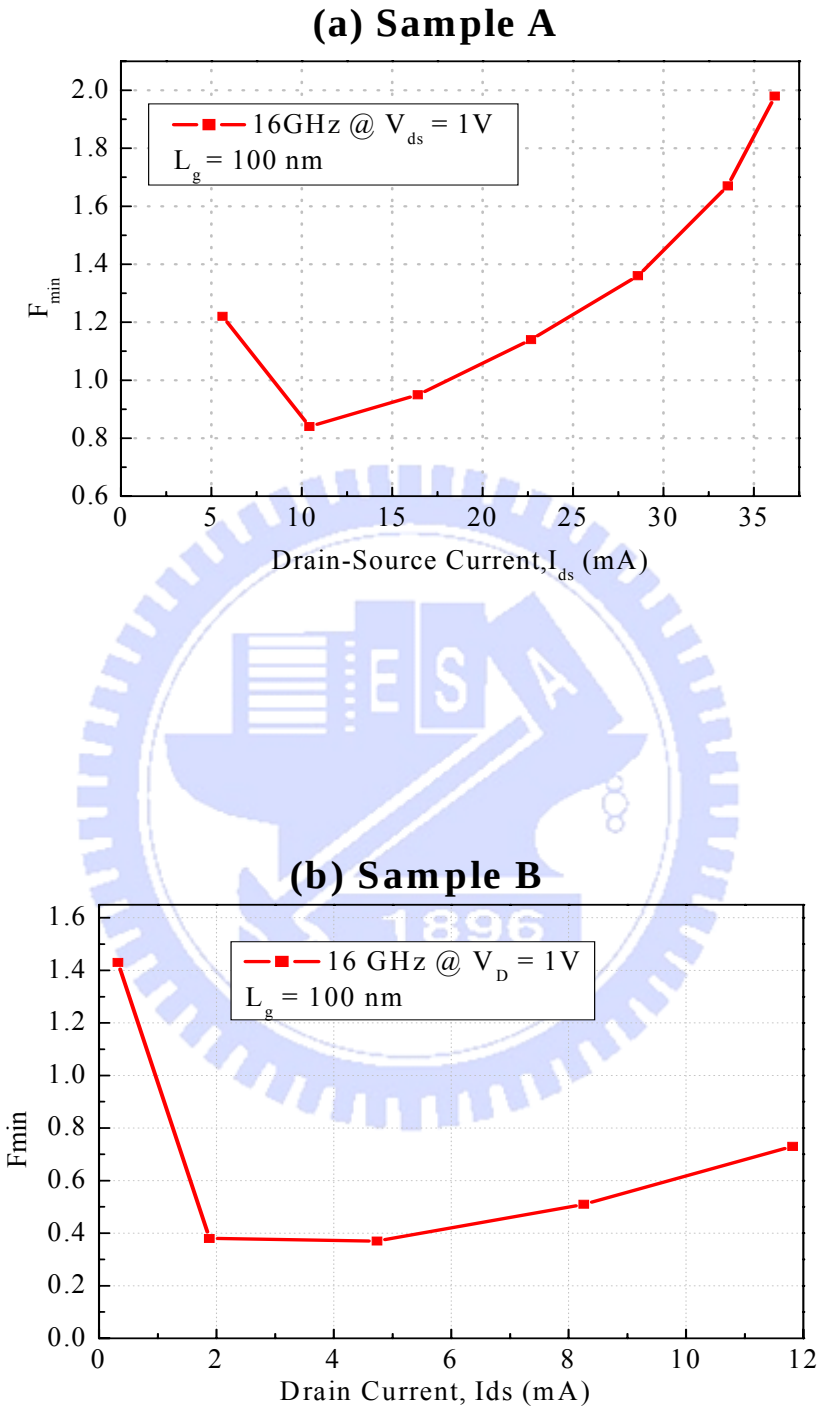


Fig. 4.7 F_{min} vs. I_{ds} at 16GHz of (a) sample A and (b) sample B

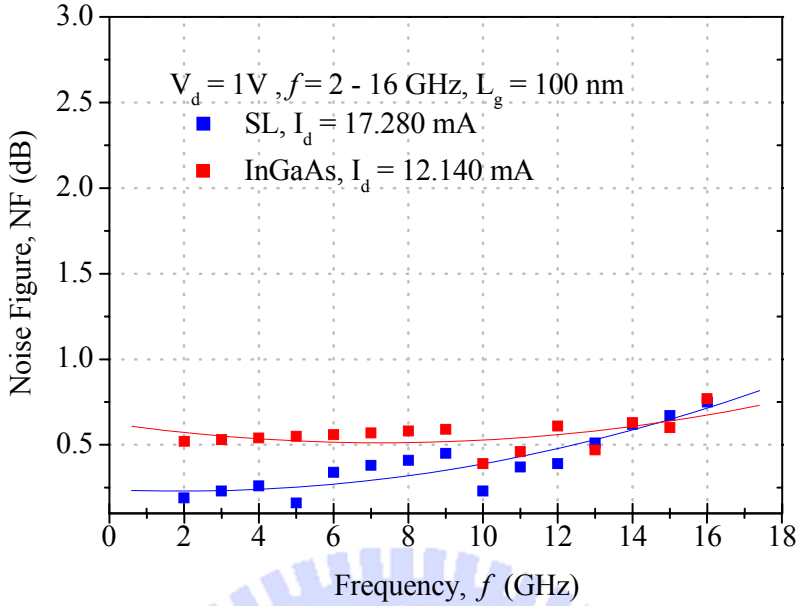


Fig. 4.8 Noise figure vs. frequency of samples A and B

Chapter 5

Conclusion

In this dissertation, the feasibility of using $(In_{0.53}Ga_{0.47}As)_m/(InAs)_n$ superlattice as channel layer in the InAlAs/InGaAs metamorphic high electron mobility transistors (MHEMT) for high frequency and low noise application is studied. The high indium content InGaAs/InAs superlattice channel has been grown successfully on metamorphic GaAs substrate which is more economical than InP substrate. Then high performance can be obtained by using superlattice channel due to high indium content.

In this study, the metamorphic HMET with superlattice channel exhibited improved DC performances with $I_{DS,sat}$ of 476 mA/mm and maximum transconductance ($g_{m,max}$) of 886 mS/mm which is better than $I_{DS,sat}$ of 344 mA/mm and maximum transconductance ($g_{m,max}$) of 709 mS/mm for the metamorphic HEMT which uses $In_{0.53}Ga_{0.47}As$ channel at the same drain bias voltage of 1V and with the same gate length of 100 nm. In addition, the MHEMT with superlattice channel also showed improved high frequency performance, with f_T of 170 GHz and f_{max} of 170 GHz which is better than f_T of 150 GHz and f_{max} of 180 GHz in the conventional MHEMT. Furthermore, the superlattice MHEMT showed lower noise performance over a frequency of 1 to 16 GHz. However, the MHEMT with superlattice channel has lower breakdown voltage because of the low band gap of InAs layers in the superlattice structure.

InAs/InGaAs superlattice channel on metamorphic GaAs substrate has been

designed and fabricated successfully. Overall, the device exhibited superior DC and RF performance than the conventional InGaAs metamorphic HEMT for high frequency and low noise applications.

Chapter 6

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