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Application of fluorine doped oxide (SiOF) spacers for improving reliability in low temperature polycrystalline thin film transistors

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Abstract

The novel process of self-aligned fluorine doped oxide (SiOF) spacers on low temperature poly-Si (LTPS) lightly doped drain (LDD) thin film transistors (TFTs) is proposed. A fluorine doped oxide spacers were provided to generate the lower dissociation Si–F bonds adjusted to the interface of the drain which is the largest lateral electric field region for lightly doped drain structure. The stronger Si–F bonds can reduce the bonds broken by impact ionization. It is found that the output characteristics of SiOF spacers TFTs show the superior immunity to kink effect. The degradations in Vth shifting, subthreshold slope, drain current and transconductance of SiOF spacers after DC stress are improved.
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Keywords: Fluorine doped oxide (SiOF); Poly-Si; Thin film transistor (TFT); Lightly doped drain (LDD); Direct current (DC) stress

1. Introduction

The interest in low temperature polycrystalline silicon thin film transistors (LTPS-TFTs) has increased because of their wide applications on active matrix liquid crystal displays (AMLCDs) [1], organic light-emitting displays (OLEDs) [2], dynamic random access memories (DRAMs) [3], and static random access memories (SRAMs) [4]. This is because the field effect mobility in polycrystalline silicon is significantly higher (by two orders of magnitude) than that in amorphous silicon [5].

However, issue of poly-Si TFT is the main constraints toward the applications due to the granular structure of poly-Si which degrade performance and reliability. Moreover, a low process temperature, i.e. less than 600 °C, also produces numerous defects at the poly-Si\SiO_2 interface and polysilicon boundaries. There are many investigations about the improvement of the poly-Si TFTs reliability. One of the approaches is the passivation of the grain boundary traps by incorporating hydrogen [6–8] or fluorine ion [9–13] in LTPS-TFTs. It is reported that the introduction of fluorine passivation method would provide the better reliability due to its stronger dissociation energy of Si–F bonds.

However, most of the investigations were reported by using fluorine implantation into gate poly-Si, and implantation into channel poly-Si. It needs an extra implantation, which may cause the implantation damage and shifts the threshold voltage. It is known that hot carrier degradation is caused by the energetic electrons generated by impact ionization near the drain of the channel region [14]. So we introduce the self-aligned fluorinated silica glass (FSG) spacer technique to generate the higher dissociation Si–F bonds that adjust to the interface of the drain which is the largest lateral electric field region for lightly doped drain structure. Therefore, this method can achieve the improvement of reliability without any

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additional process step for a conventional top-gate lightly doped drain (LDD) polysilicon TFT structure. This work also can analyze the relationship of reliability behaviors between the fluorine ions in the sideward spacer region near drain side of channel and the defects formation under a DC bias stress.

2. Devices structure and fabrication

The fabrication of devices started by depositing a 50 nm undoped amorphous Si (a-Si) layer at 550 °C in a low-pressure chemical vapor deposition (LPCVD) system on Si wafers covered with a 500 nm thick thermal oxide layer. The a-Si layer was re-crystallized by solid-phase-crystallization (SPC) process in furnace at 600 °C for 24 h in a N_2 ambient. After patterning and etching the active region, the 50 nm thick SiO_2 (tetraethylorthosilicate) and the 200 nm thick poly-Si gate were both deposited by LPCVD system. After gate electrode formation, phosphorus ions at a dose of 5×10^{13} cm^{-2} and an energy of 17 keV were implanted to form the lightly doped source/drain regions and wafers were subjected to a rapid thermal anneal (RTA) at 820 °C for 20 s for dopants activation. Then the wafer was loaded into a plasma enhanced chemical vapor deposition (PECVD) system using the mixture gases of CF_4 and TEOS at 300 °C to grow a 300 nm thick FSG on the exposed gate and source/drain regions. For comparison, wafer with conventional TFTs was also processed on the same run by deliberately depositing only the TEOS oxide without fluorine dopants. Then the FSG layers and the conventional TEOS oxide were anisotropically etched by RIE to form the sidewall spacer abutting the poly-Si gate without additional mask. Phosphorus ions at a dose of 5×10^{15} cm^{-2} and an energy of 17 keV were implanted to form the n^+ gate, source/drain regions and were activated by RTA at 820 °C for 20 s also. The 500 nm thick TEOS oxide were deposited and patterned into the contact holes. The 500 nm thick aluminum (Al) layer was deposited by physical vapor deposition (PVD) and patterned to form metal pads. Finally, the finished devices were sintered at 400 °C for 30 min in an N_2 ambient. In this study, all devices investigated have channel length of 3 μm and width of 10 μm. The device

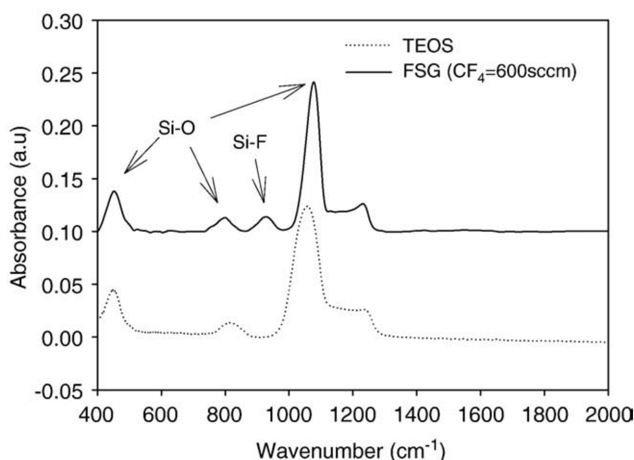

Fig. 1. FTIR spectra of FSG film and TEOS film between 2000 cm^{-1} and 400 cm^{-1}.

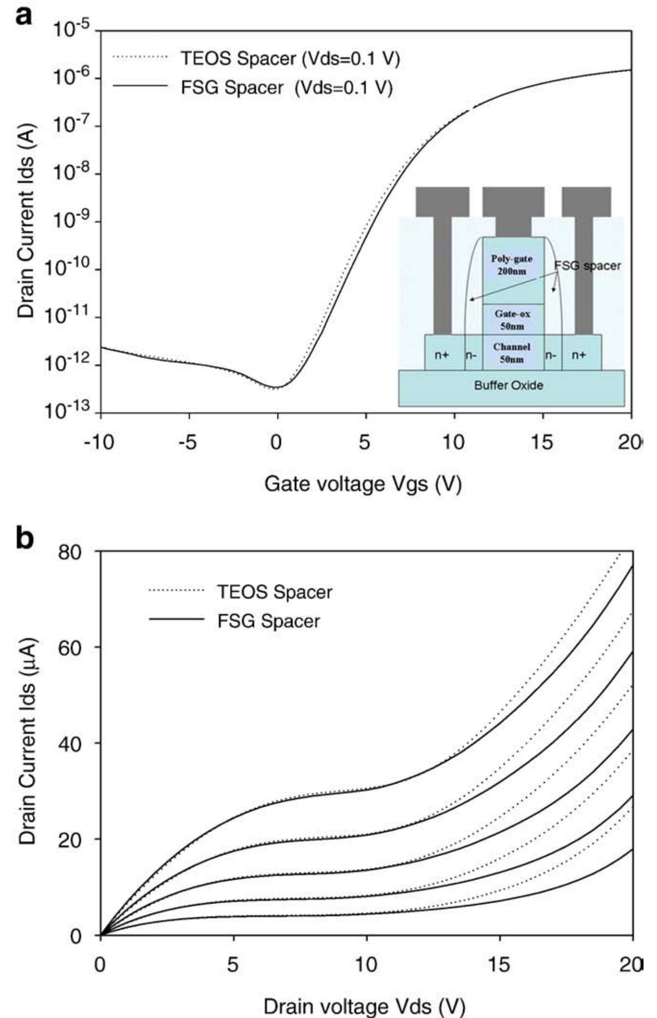

Fig. 2. Comparison of (a) Ids–Vgs characteristics of FSG spacer TFT and TEOS spacer TFT for Vds = 0.1 V (inset is the schematic cross-section of the SiOF spacer TFT structure.) and (b) output characteristics for FSG spacer and TEOS spacer TFT, W/L = 10 μm/3 μm, Vg–Vth = 0, 1, 2, 3, 4 V.

cross-section was shown in the inset of Fig. 2. In this work, a DC stress (Vgs = 15 V, Vds = 30 V) was applied for a maximum duration of 10^4 s to investigate the reliability behaviors.

3. Results and discussion

Fig. 1 shows the Fourier transform infrared (FTIR) spectra of undoped SiO_2 and FSG films between 400 cm^{-1} and 2000 cm^{-1}. The FTIR spectra were measured from an unpatterned wafer with undoped SiO_2 and FSG layer, respectively. The main peak of function group Si–F is around 930 cm^{-1}. The signal of Si–F bonds is clearly observed in the FSG film.

Fig. 2(a) and (b) shows the comparison of transfers and output curves for poly-Si TFTs with TEOS and SiOF spacer, respectively. It is found that the Ids–Vgs characteristics for Vds = 0.1 V of transistor with W = 10 μm and L = 3 μm in both types of poly-Si TFTs were nearly the same. This indicates that the introduction of FSG spacer in poly-Si TFT device does not degrade electrical performance. In Ids–Vds characteristics for

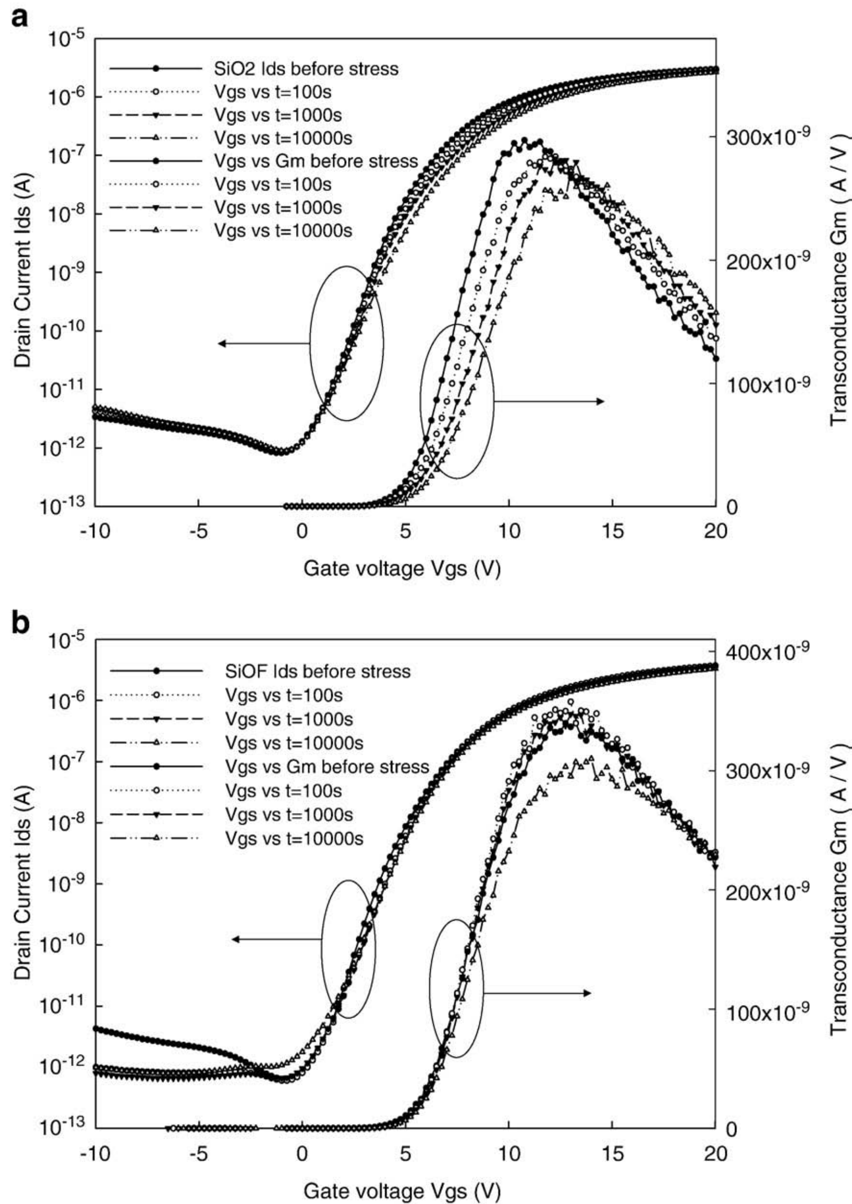

Fig. 3. The degradation of drain current and transconductance by static stress in (a) TEOS spacer structure and (b) SiOF spacer structure under a DC stress (Vgs = 15 V, Vds = 30 V).

Vg–Vth = 0, 1, 2, 3, 4 V, it is found that the kink effect occurs in both poly-Si TFTs. The kink effect attributed to channel avalanche multiplication occurred in the high fields near drain side is especially dramatic for n-channel devices, because of the higher impact-ionization rate of electrons [15]. However, the drain current in the saturation region of TEOS spacer TFT is increasing more seriously than SiOF spacer TFT, especially at high gate voltages. The suppression of kink effect for the poly-Si TFT with FSG spacers is more significant than the TEOS spacer poly-Si TFT due to the fluorine ions in the sideward spacer near drain side that strongly passivate the Si dangling bonds to avoid the occurrence of hot carriers.

Fig. 3(a) and (b) shows the different degradation behaviors of drain current and transconductance between TEOS and FSG spacer under static stress, respectively. For TEOS spacer, the curve of the transconductance decreases monotonically and shows a parallel shift in the positive direction with the increase of the stress time. For FSG spacer, $G_{m,\ max}$ is initially increased and then it starts to decrease after 1000 s stressing, while remains unchanged for Vgs > 17 V. The poly-Si TFT electrical parameters such as threshold voltage (Vth), maximum transconductance ($G_{m,\ max}$), on current (I_{on}), and subthreshold slope (SS) could depend on grain size and orientation, grain boundaries, and/or interface properties. The deep traps existing in grain boundaries have been demonstrated to affect mainly threshold voltage and much less $G_{m,\ max}$. On the other hand, tail states from grain regions in the interface and/or from grain boundaries mainly contribute to the decrease of $G_{m,\ max}$ [16–17]. The subthreshold slope depends mainly on intra-grain traps distributed uniformly inside the poly-Si film and also on the deep interface states [18]. Therefore, it is obvious that depending on the nature of state generation during the stress, electrical parameters can provide

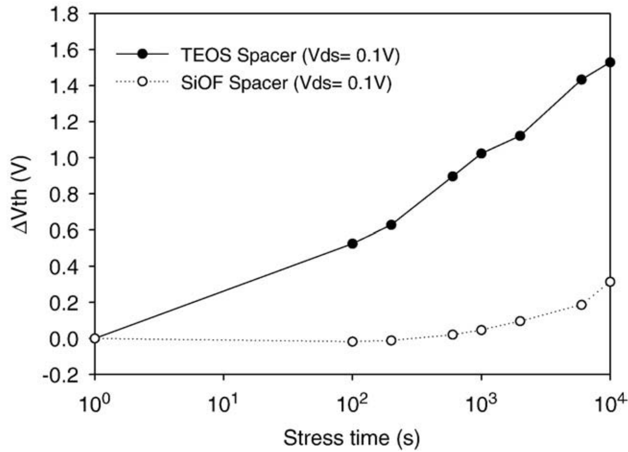

Fig. 4. Comparison of ΔVth behavior of FSG spacer TFT and TEOS spacer TFT measured at Vds = 0.1 V under a DC stress (Vgs = 15 V, Vds = 30 V).

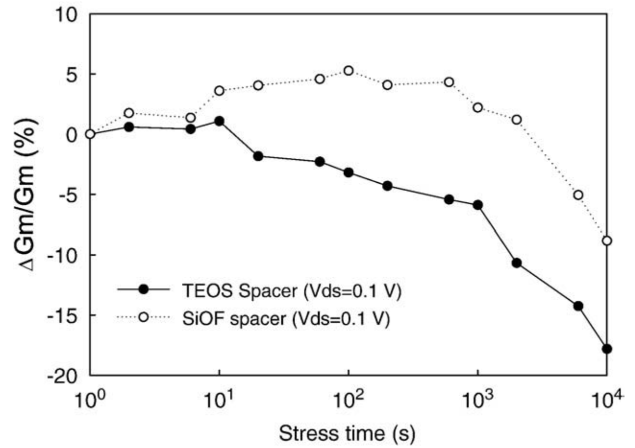

Fig. 6. Comparison of $\Delta G_m/G_m$ behavior of SiOF spacer TFT and TEOS spacer TFT measured at Vds = 0.1 V under a DC stress (Vgs = 15 V, Vds = 30 V).

useful information in order to clarify poly-Si TFTs degradation under stress conditions. Therefore, we can analyze the relationship between the fluorine ions in the sideward spacer near drain side and the defects formation under a DC bias stress by extracting the parameters of the devices as followed.

Fig. 4 shows the threshold voltage variations (ΔVth) during stressing. In poly-Si TFTs, the method to determinate the threshold voltage is constant drain current method. The constant drain current normalized by the size $[I_{\mathrm{normal}} = \mathrm{Ids}/(\mathrm{Weff}/\mathrm{Leff})]$ is specified as 100 nA for Vds = 0.1 V. In contrast with the large Vth shift for the TEOS spacer TFT, Vth shift for the SiOF spacer TFT was smaller. Vth shift is strongly dependent on the deep trap states which originate from the dangling bonds creation in the grain boundaries of the sideward channel [19]. The degradation of TEOS spacer TFT is due to deep states generated in the grain boundaries and at the gate oxide/channel interface with stress duration by breaking the weak and/or strained Si–H, Si–O bonds and even the strong Si–Si bonds. However, for SiOF spacer TFT, the superior reliability is due to the passivation of dangling bonds by fluorine ions near drain side. Since the dissociation energy of Si–F bonds is about twice of the Si–H bonds, Si–F is hardly broken by the stressing and thus generation of positive fixed charges in the gate oxide is suppressed. Moreover, the suppression of kink effect for the poly-Si TFT with FSG spacers also reduces the degree of degradation under the same stress condition.

Fig. 5 shows the comparison of the subthreshold slope variation ΔSS characteristics of TEOS spacer TFT and SiOF spacer TFT for Vd = 0.1 V where $\Delta SS = SS - SS_0$, SS_0 is the initial subthreshold slope and SS is the subthreshold slope for each stress time. Initially, the ΔSS of SiOF spacer TFT is smaller than in the TEOS spacer TFT, but ΔSS is then rapidly degraded to approach the curve of TEOS spacer TFT after 6000 s. Stress induced subthreshold swing is also associated with the interface deep state generation, so less degradation in SiOF spacer TFT is due to its better interface property at spacer regions near drain. But when the Si–F bonds formed only under sidewall spacers were broken in long term stress, SiOF spacer TFT loses the advantage of stronger passivation.

Fig. 6 shows the degradation of the maximum transconductance defined as $\Delta G_{\mathrm{m,\,max}}/G_{\mathrm{m,\,max0}}$, where $\Delta G_{\mathrm{m,\,max}} = G_{\mathrm{m,\,max}} -$

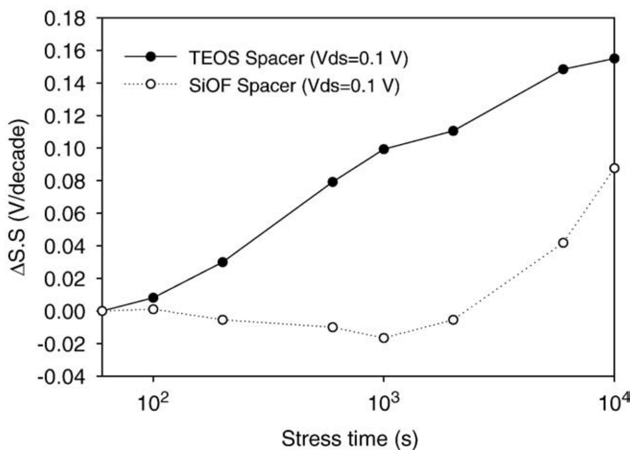

Fig. 5. Comparison of ΔSS behavior of SiOF spacer TFT and TEOS spacer TFT measured at Vds = 0.1 V under a DC stress (Vgs = 15 V, Vds = 30 V).

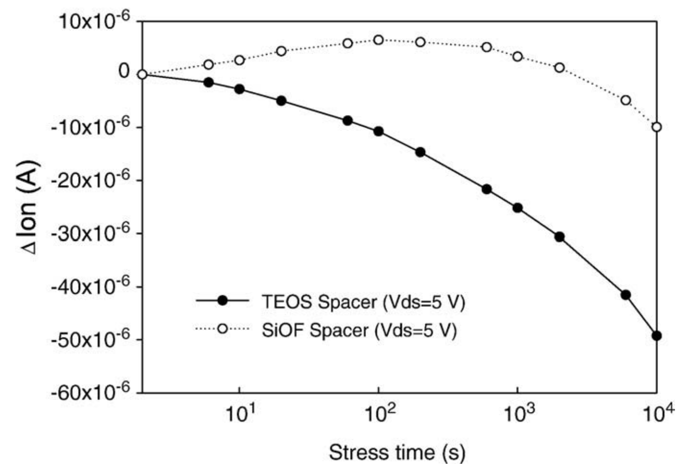

Fig. 7. Comparison of ΔI_{on} behavior of SiOF spacer TFT and TEOS spacer TFT measured at Vds = 5 V under a DC stress (Vgs = 15 V, Vds = 30 V).

$G_{m, max0}$, $G_{m, max0}$ is the initial transconductance and $G_{m, max}$ is the transconductance after stress. The more serious degradation of TEOS spacer TFT in G_m is found. This is because F atoms can terminate dangling bonds and replace weak bonds in the grain boundaries and SiO_2/poly-Si interface and, thus, reduce the trap states in the poly-Si channel. As a result, the transconductance with SiOF spacers was degraded slower due to the decrease in the strain bonds by passivation of boundaries defects. Fig. 7 shows the degradation of on current measured in the saturation region for Vds = 5 V. In practice, the maximum drain current was defined as the on current which was extracted at Vgs = 20 V. The more serious degradation of TEOS spacer TFT in I_{on} is found. This is due to the reducing of potential barrier in the channel by passivating the dangling bonds and traps in grain boundaries by fluorine ions.

4. Conclusion

We have demonstrated the novel poly-Si TFT device with SiOF film as the spacers to enhance the electrical characteristics without any additional process step. The poly-Si TFT with SiOF spacers exhibits superior endurance against hot carrier effect, leading to improved electrical reliability and suppressed kink effect than the TFT with TEOS SiO_2 spacer due to fluorine passivation effect. In addition, the manufacturing processes are compatible with the conventional TFT process. This indicates our proposed poly-Si TFT with SiOF spacers is a promising technology for application in the TFT-LCDs.

Acknowledgments

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