國立交通大學

材料科學與工程學系

博士論文

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研 究 生：張志榜

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摘要

低溫複晶矽薄膜電晶體用來製作畫素元件與周邊驅動電路已成為發展主動式平面顯示器的重要技術。本論文主要在於深入討論並製作有關高性能複晶矽薄膜電晶體的研究，主要分為以下四個部份來探討。

首先，利用固態連續波雷射將非晶矽薄膜再結晶為複晶矽薄膜已成功製作出高效能的低溫複晶矽薄膜電晶體，但是受限於雷射能量的高斯分佈而導致元件的均勻性變差。因此，我們在此提出利用鎳金屬誘發側向結晶的複晶矽薄膜取代傳統的非晶矽薄膜，接著利用不同能量的固態連續波雷射進行再結晶，從實驗的結果得知在較小的照射能量(3.8W)的條件下，就可獲得比傳統 CLC 結晶技術高的性能與均勻性。

在論文的第二個部份，我們探討離子佈植方式下氟離子對於金屬誘發

側向結晶複晶矽薄膜電晶體的影響。從實驗的結果得知，經由氟離子佈植後的金屬誘發側向結晶複晶矽薄膜電晶體可獲得較佳的電特性，其主要原因為氟離子於複晶矽薄膜內可有效的降低缺陷密度，因而獲得較好的元件特性。除此之外，與傳統的金屬誘發側向結晶技術相較下，氟離子的佈植也可使得元件在熱載子劣化下具有較好的對抗能力，使元件具有較佳的可靠度，並且在製作的過程不需額外的熱退火。

經由論文的第二部份的實驗結果得知，利用離子佈植將氟離子植入金屬誘發側向結晶複晶矽薄膜內可使得元件特性與穩定性獲得改善，但是此方式在漏電流的方面並沒有獲得改善，其原因有可能為殘留在薄膜的鎳金屬濃度並沒有改變。因此在論文的第三個部分我們提出利用四氟甲烷(CF_4)電漿蝕刻金屬誘發側向結晶複晶矽薄膜的表面，經由電漿處理後的元件也可獲得電性與可靠度的提升，其主要原因為電漿蝕刻表面後可有效的降低複晶矽薄膜缺陷密度使得元件特性提升，並且有效的產生矽氟鍵結(Si-F bond)因而改善元件的可靠度。除此之外，隨著電漿蝕刻表面時間增加，元件在漏電流方面的表現也可獲得改善。

在論文的最後一部份，我們提出一種新的製作複晶矽薄膜電晶體的技術—”鎳驅入誘發側向結晶”，主要利用氟離子佈植的方式撞擊鍍在非晶矽薄膜表面的鎳金屬，透過圖形的設計形成鎳金屬驅入側向結晶區，由此方式發現，利用氟離子驅入的過程，可有效抑制退火再結晶時所產

生的固相結晶，並降低薄膜中的缺陷密度導致電晶體性能的提升。此外，在與傳統的金屬誘發側向結晶技術相較下，鎳驅入側向結晶技術的實行步驟並沒有複雜化。

Investigation of Electrical Properties, Reliability and Uniformity Issues in Metal-Induced Lateral Crystallization Poly-Si TFTs

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Abstract

Low-temperature processed polycrystalline silicon thin-film transistors (LTPS TFTs) as pixel active elements and in peripheral driver circuits has been an important issue in the development of active matrix flat panel displays (AMFPDs). This dissertation studies a number of processing techniques for the high performance poly-Si TFTs. The main focus of this dissertation can be divided into four parts.

Initially, continuous-wave (CW) laser crystallization (CLC) of amorphous Si (α-Si) has previously been employed to fabricate high-performance low-temperature polycrystalline silicon (poly-Si) thin-film transistors (TFTs). Unfortunately, their uniformity was poor because the shape of beam profiles was Gaussian. Therefore, α-Si film was replaced by Ni metal-induced laterally crystallized Si (MILC-Si). After irradiation by a CW laser (λ ~532

nm and power ~3.8W), it was found that the performance and uniformity of the MILCLC-TFTs were much better than those of the CLC-TFTs. Therefore, the MILCLC-TFT is suitable for application in a system on panel.

Next, the effect of fluorine-ion (F^+) implantation on the performance of metal-induced lateral crystallization (MILC) polycrystalline silicon thin film transistors (poly-Si TFTs) was investigated. It was found that fluorine ions minimize effectively the trap-state density, leading to superior electrical characteristics such as high field-effect mobility, low threshold voltage, low subthreshold slope, and high on/off current ratio. F^+-implanted MILC TFTs also possess high immunity against the hot-carrier stress and thereby exhibit better reliability than that of typical MILC TFTs. Moreover, the manufacturing processes are simple (without any additional thermal annealing step), and compatible with typical MILC poly-Si TFT fabrication processes.

As discussed in part of second, fluorine ion (F^+) implantation was employed to improve the electrical performance of MILC TFTs. It was found that fluorine ions effectively minimize the trap state density, leading to superior electrical characteristics and better reliability. However, the minimum off-state currents were nearly unchanged. This might because the Ni concentration was unchanged. Therefore, in the part of third, MILC poly-Si TFTs with etching channel surface by CF_4 plasma etching treatment were use to improve the electrical properties and reliability in this study. It was found that CF_4 plasma etching

treatment effectively minimized the trap state density, leading to superior electrical characteristics. Besides, the leakage current was also suppressed with the increase on etching time. Moreover, CF_4 plasma-treated MILC TFTs also possess high immunity against the hot-carrier stress and thereby exhibit better reliability than that of conventional MILC TFTs, which is due to the storng Si-F bonds formed in the MILC poly-Si channel region.

At the last part of the thesis, a new manufacturing method for polycrystalline silicon thin film transistors (poly-Si TFTs) using Ni drive-in induced laterally crystallization (DILC) was proposed. The DILC poly-Si was prepared by collision between F ion implantation and Ni film through the designed pattern into amorphous-Si (α-Si). It was found that the drive-in by F atoms effectively suppresses the nucleation of solid phase crystallization grain and reduces trap-state density, and lead to improve electrical characteristics. Moreover, the manufacturing processes are simple and compatible with MILC TFT processes.

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Chapter 1

Introduction

1.1. Overview of low temperature polycrystalline silicon thin-film transistors (TFTs)

In 1980, high temperature polycrystalline silicon TFTs had been introduced [1]. They used chemical-vapor deposited poly-Si to achieve good carrier mobility and electrical characteristics. With mobility around 50 $cm^2/V\text{-}s$, these high temperature poly-Si TFTs were employed gate insulator SiO_2 grown thermally at 1050°C. This approach requires a high strain temperature substrate such as quartz, incompatible with the commercially available large area non-expensive glass substrate.

Recently, many researchers have developed various techniques for crystallization of α-Si at low temperature (below 600°C), and then transformation it to poly-Si; the motivation for pushing up the mobility to be able to integrate drive circuitry [2], [3]. as well as providing pixel TFTs and more compatible with the glass substrate. In fact, the field effect mobility of poly-Si TFTs is significantly higher than that of α-Si about two orders of magnitudes. The higher drive current allows small TFTs dimension to be used as the pixel switching elements, resulting in higher aperture ratio and lower parasitic gate-line capacitance for improved display performance [4].

Unlike MOSFETs, where the active layer is part of the substrate, in the case of TFTs the active layer needs to be separately formed on the host substrate. The crystallization method affect the microstructure quality of the resulting poly-Si film, which means that the performance of poly-Si TFT will be affected by the selection of techniques for the crystallization of Si films.

A various techniques have been investigated for crystallization of α-Si at low temperature such as: (1) solid phase crystallization (SPC) (2) excimer laser crystallization (ELC) (3) continuous-wave laser crystallization (CLC) (4) Ni metal induced/Ni metal induced lateral crystallization (MIC/MILC). In the following section, we will review the crystallization method that the above-mentioned.

1.2. Low temperature polycrystalline silicon crystallization methods

Crystallization of α-Si films has been considered as the most important process step in the fabrication of LTPS TFTs. The quality of crystallized poly-Si films is quite sensitive to the performance of poly-Si TFT. In poly-Si films, most defects are generated at the grain boundaries. Enlarging the grain size can promote the quality of poly-Si, as deposited poly-Si generally exhibits small grain size. In general, the poly-Si crystallized from α-Si usually has larger grain size than that of as-deposited poly-Si. Historically, solid phase crystallization was the first technology to produce poly-Si films for display applications [5], followed by laser crystallization. The ultimate goal of the LTPS technology is to integrate the pixel-driving circuits on the display substrate. Fig. 1-1 shows the anticipated evolution of poly-Si technology development and its impact on the degree of on-panel integration [6].

Year	2004	2006	2008	2010
SOP Generation	1st	2nd	3rd	4th
Display Resolution	300ppi	400ppi		
Power Supply	12V	3-5V	1.5-3V	1.5V
TFT Mobility	200-300$\mathrm{cm^2V^{-1}s^{-1}}$	300-500$\mathrm{cm^2V^{-1}s^{-1}}$	500$\mathrm{cm^2V^{-1}s^{-1}}$	
Design Rule	3μm	1.5μm	0.8μm	0.5μm
Logic Frequency	~3MHz	10MHz	20-50MHz	50-100MHz
Key Process Crystallization Gate Insulator Patterning	CGSi	Advanced CGSi Thin GI Fine Patterning	Texture-control CGSi Ultra-thin GI Sub-μm Patterning	
Monolithic Integration	Digital Driver	Timing Generator Photo Sensor Amplifier	Display controller Image processor LN Amplifier	ULC Driver RF Capability Advanced MPU

Fig. 1-1 Roadmap of poly-Si TFT technology. [6]

1.2.1.Solid phase crystallization (SPC) method

Deposited α-Si thin films were transformed to poly-Si using SPC method has obtained better TFT device electrical performance than as-deposited poly-Si films [7]. For the SPC method, α-Si films are crystallized in a furnace at temperature about 600°C for duration time (about 24 h). The polycrystalline grains are generally in oval-shaped and large defect density exists in poly-Si films. Amorphous Si is a thermodynamically meta-stable phase possessing a driving force for transformation to polycrystalline phase given a sufficient energy to overcome the initial energy barrier.

A key factor affecting crystallization is the nucleation rate in the α-Si films. The nucleation rate is strongly influenced by the selected deposition method and condition [8], [9]. The structural order/disorder in the α-Si films affects the films to form stable nuclei. Higher disorder structure increases the energy barrier required to form the Si nuclei; this concept has been used in the past to increase the grain size of poly-Si films. Ideally, a small number of fast-growing nuclei are needed to maximize the grain size. However, the reality of the situation is that the probability that additional nucleation events will occur within the volume separating growing nuclei increases geometrically with the separation distance

1.2.2.Excimer laser crystallization (ELC) method

Excimer laser annealing is suitable for fabrication of LTPS TFTs on large area glass substrate. Development of the ELA method has provided poly-Si material with high quality than SPC method. This is attributed to the melt-induced poly-Si growth. For the crystallization process, the laser is irradiated at the α-Si and the silicon is heated above 1200°C. However, only sustained for a very short time; therefore, it will not damage the glass substrate. Moreover, as shown in Fig. 1-2, there are two major transformation regimes (occurring at low and high laser energy, respectively) and one minor transformation regime in between (that so-called superlateral growth, or SLG) [10], [11]. The low laser energy regime describes a situation where the incident laser is sufficient to induce melting of the silicon films, but it is low enough that a continuous layer of silicon at the maximum extent of melting. For this reason, this regime is referred to as the partial melting regime. The high laser energy regime corresponds to a situation that the laser energy is sufficiently high to completely melt the silicon film; this regime is also referred to as complete melting regime. In addition to these two regimes, a third regime has been found to exist within a very narrow experimental window in between the two main regimes. Despite the small extent of this region, it is nonetheless one with great technological significance, because the poly-Si films within the regime feature large-grained polycrystalline microstructures [12]. The stable grain size of ELA poly-Si films is typically limited to 0.3~0.6 μm. Larger grain size is possible within the SLG window, but this regime is intrinsically unstable.

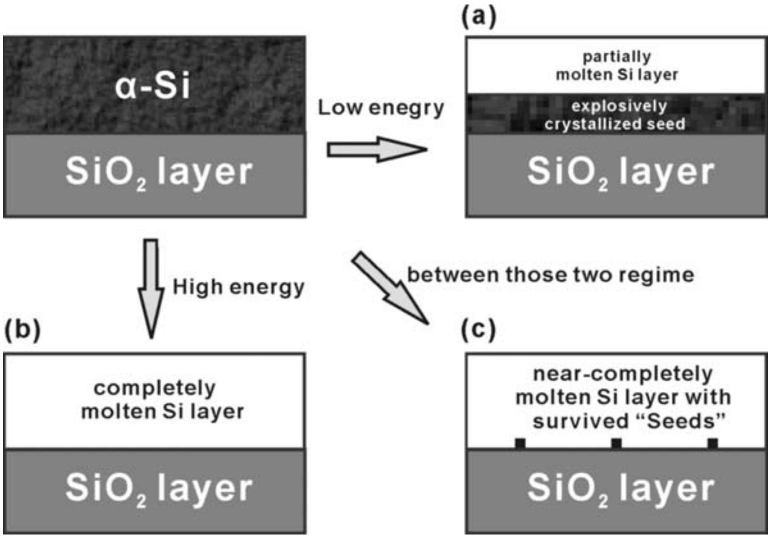

Fig. 1-2 Illustration of transformation scenarios during the ELA process. Correspond to (a) partial melting, (b) completely melting and (c) near-completely melting of the initial Si film.

The surface roughness in ELA poly-Si films is localized at the planes and point of congruence of grain boundaries. The mechanism for the formation of roughness is well understood and is attributed to the specific density difference between molten Si (2.53 g cm^{-3}) and solid Si (2.30 g cm^{-3}). In other words, as the molten Si solidifies, it simultaneously expands. Solidification starts from neighboring seed areas, and the last region to solidify is the volume at the vicinity of the two colliding lateral fronts. As that happens, the generated solid Si can only expand upward, as shown in Fig. 1-3, thus generating the ridge associated with the formation of the grain boundary at the location.

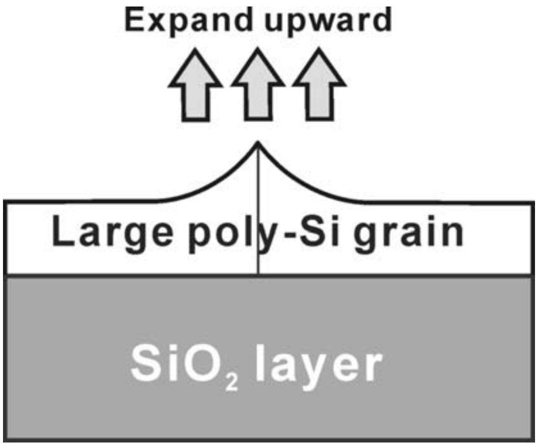

Fig. 1-3 Solidification of the molten Si film. Resulting in the higher surface roughness

Although the highest quality poly-Si films were fabricated by ELA method, the poor grain size uniformity and high roughness ELA poly-Si films degraded the performance of TFT [13].

1.2.3.Continuous-wave laser crystallization (CLC) method

Hara et al. in 2001 announced highly crystalline poly-Si films on large-area glass substrates by continuous-wave (CW) laser crystallization (CLC) [14]. In CLC, power instability of diode pumped solid state (DPSS) CW laser (532nm (second harmonics (2ω) of Nd:YVO4)) is less than 1%, which value is superior to that of XeCl excimer lasers and Ar lasers. Moreover, CLC processes were conduced at room temperature and in ambient environment. TFTs on such CLC poly-Si layers on glass substrates were fabricated at process temperature below 450℃; field-effect mobilities for n-channels and p-channels were as high as 566 cm2/Vs and 200 cm2/Vs, respectively. CLC easily forms ~20 μm large grains and low roughness in crystallized layers, in a quite wide energy range as shown in Figure 1-3, because of continuous laser-energy supply, directional solidification caused by laser scanning, and slow cooling rate of molten Si due to the dwell time of laser beam is about 100 μs during scanning.

In 2007, Ogawa et al. [15] introduced CLC technologies to perform a low power (~ 50mW) and high resolution (332ppi) VGA LCD with integrated 6-bit digital data drivers. Excellent uniformity in threshold voltage, as compared to that of conventional ELA-TFTs, is shown in Fig. 1-4 and Fig. 1-5.

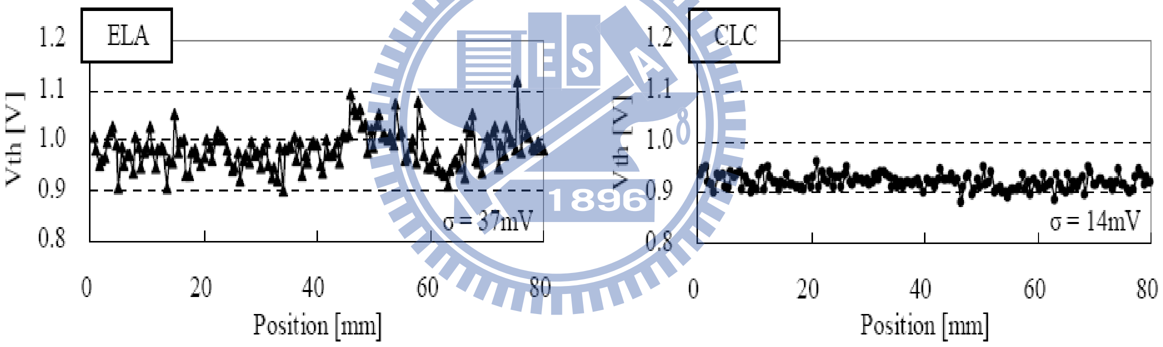

Fig. 1-4 Global variation in NMOS threshold voltage: ELA (left), CLC (right). (L/W = 5.4μm/20μm, Tox = 30nm, TFT distance = 0.5mm) [15].

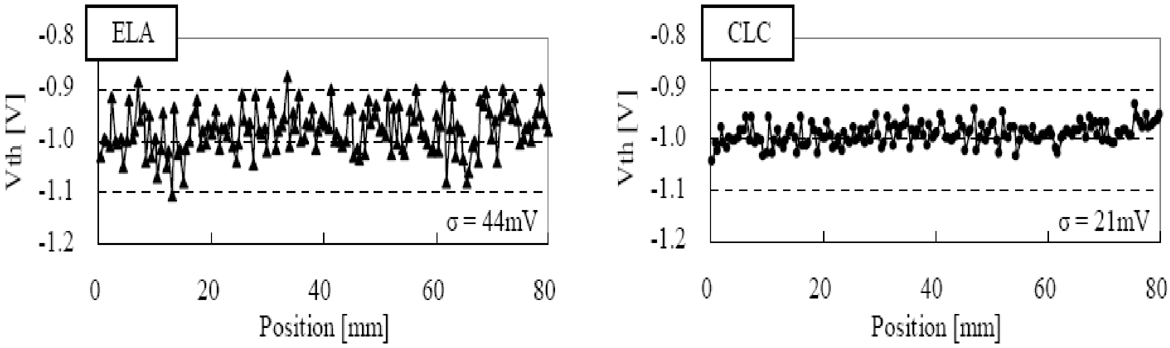

Fig. 1-5 Global variation in PMOS threshold voltage: ELA (left), CLC (right). (L/W = 2.7μm/20μm, Tox = 30nm, TFT distance = 0.5mm) [15].

1.2.4.Ni metal-induced crystallization (MIC) / Ni metal-induced lateral crystallization (MILC) methods

Solid phase crystallization of α-Si needed a high temperature and longer annealing time for furnace annealing process. In the NIC/NILC method, the annealing time and temperature could be reduced, and the grain size of NILC poly-Si films uniformly over large area could be obtained [16]-[19]. In 2000, Sharp Corp. and SEL (Semiconductor Energy Lab.) propose the CGSi (Continuous Grain Silicon) technique to fabricate the 60 inch HDTV rear projector [20]. When thin Ni is deposited on α-Si and annealed, Ni disilicide ($NiSi_2$) forms [21]. The nickel disilicide is cubic with CaF_2 structure and has a very close lattice parameter match to c-Si (-0.4%), the lattice constant of $NiSi_2$, 5.406A, is nearly equal to that of Si, 5.430A. The disilicide is actually the species that mediates the transformation of α-Si to c-Si. As shown in Fig. 1-6, the c-Si formed below the Ni-pad is called NIC and the lateral growth is called NILC.

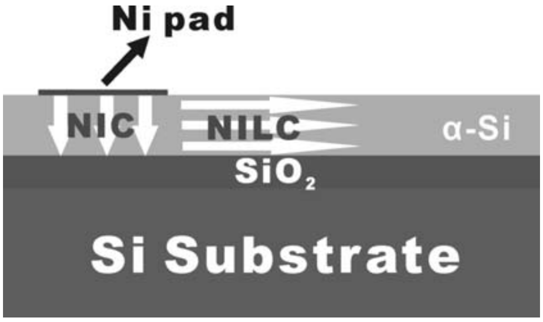

Fig. 1-6 Schematic illustration of the Ni-metal induced Crystallization (MIC) and Ni-metal induced lateral crystallization (MILC)

The silicide mediate growth of silicon occurs in three stages. In the first stage, precipitation and growth of $NiSi_2$ occur in the temperature range of 325~400°C. In the second phase, crystalline Si nucleates on one or more the eight {111} faces of the octahedral $NiSi_2$, as shown in Fig. 1-7. Finally, in the third phase, c-Si growth proceeds with a $NiSi_2$ precipitate at the planar advancing growth front.

As shown in Fig. 1-7, for <110>-oriented precipitates, four of the {111} planes exhibit surface normal within the planes of the film, which makes extensive growth possible. On the other hand, the <100>- and <111>-oriented precipitates exhibits {111} planes normal that intersect the upper and lower surface of α-Si films.

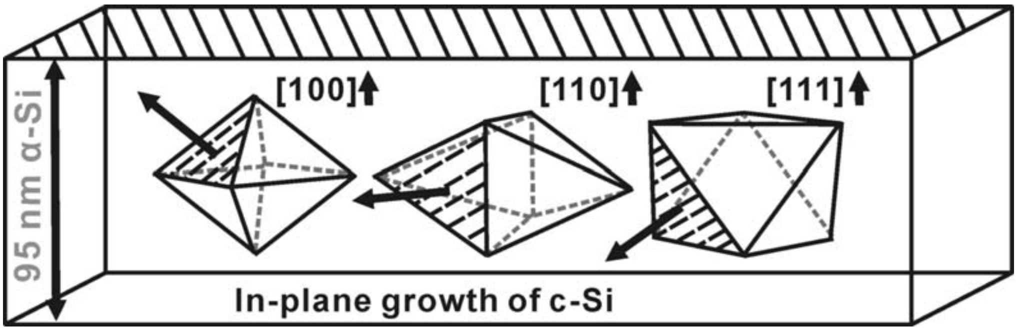

Fig. 1-7 Schematic representation of favorable precipitate orientations for long-range growth of epitaxial Si within the plane of the α-Si.

The driving force for the migration of $NiSi_2$ precipitates is reduction in the free energy associated with the transformation of meta-stable α-Si to stable c-Si. An equilibrium free-energy diagram is provided for explanation, as shown in Fig. 1-8 [21]. It is well known that the α-Si has a higher free energy than c-Si. In the case of Ni silicide mediated crystallization, the free energy difference between Ni and Si atoms at the $NiSi_2$/α-Si and $NiSi_2$/c-Si interface acts as the driving force for Ni diffusion [21]. The free energy of the Ni atom is lower at the $NiSi_2$/α-Si interface than at the $NiSi_2$/c-Si interface, whereas the free energy of the Si atom is lower at the $NiSi_2$/c-Si interface. Therefore, with the dissociative model [21], the $NiSi_2$ layer dissociates to provide free Si for epitaxial growth of c-Si at the c-Si/$NiSi_2$ interface by the diffusion of Ni atoms. The Ni atoms diffuse to α-Si following by formation of a fresh $NiSi_2$/α-Si interface. Repetition of this process results in migration of $NiSi_2$ precipitates through α-Si and growth of needlelike Si. Fig. 1-1Fig. 1-9 shows a schematic representation of a possible growth process incorporating the formation of intermediate thin layer of c-Si on the leading edge of migrating $NiSi_2$ precipitate [21]. As a result of this growth mechanism, NILC poly-Si films demonstrate a needlelike microstructure, with each needle grain attribute to c-Si growth from an individual disilicide precipitate.

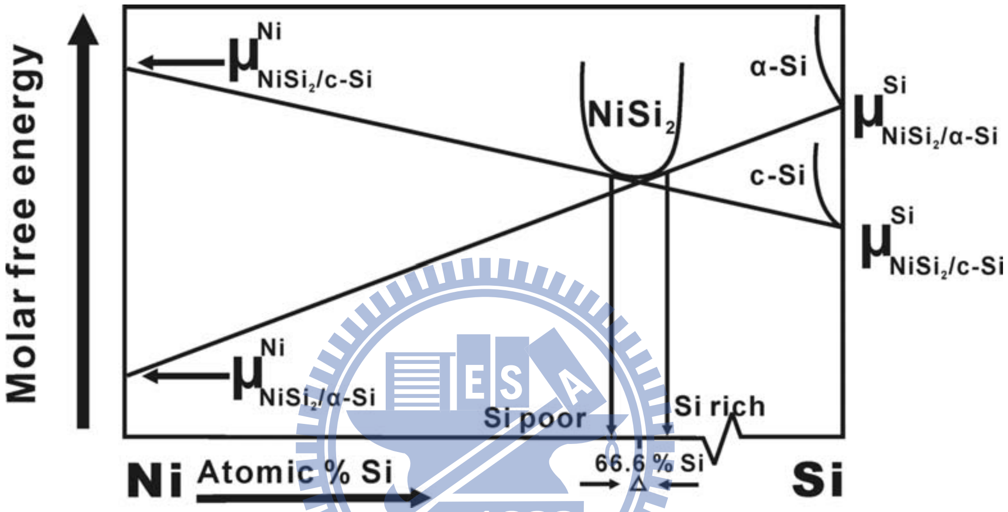

Fig. 1-8 Schematic equilibrium molar free-energy diagram for $NiSi_2$ in contact with α-Si

In addition to Ni, other metals have been investigated as far as their effectiveness in enhancing Si crystal growth. These include Au [22], Al [23] and Sb [24] which form eutectic with Si, and Pd [25], [26], which forms silicide with Si.

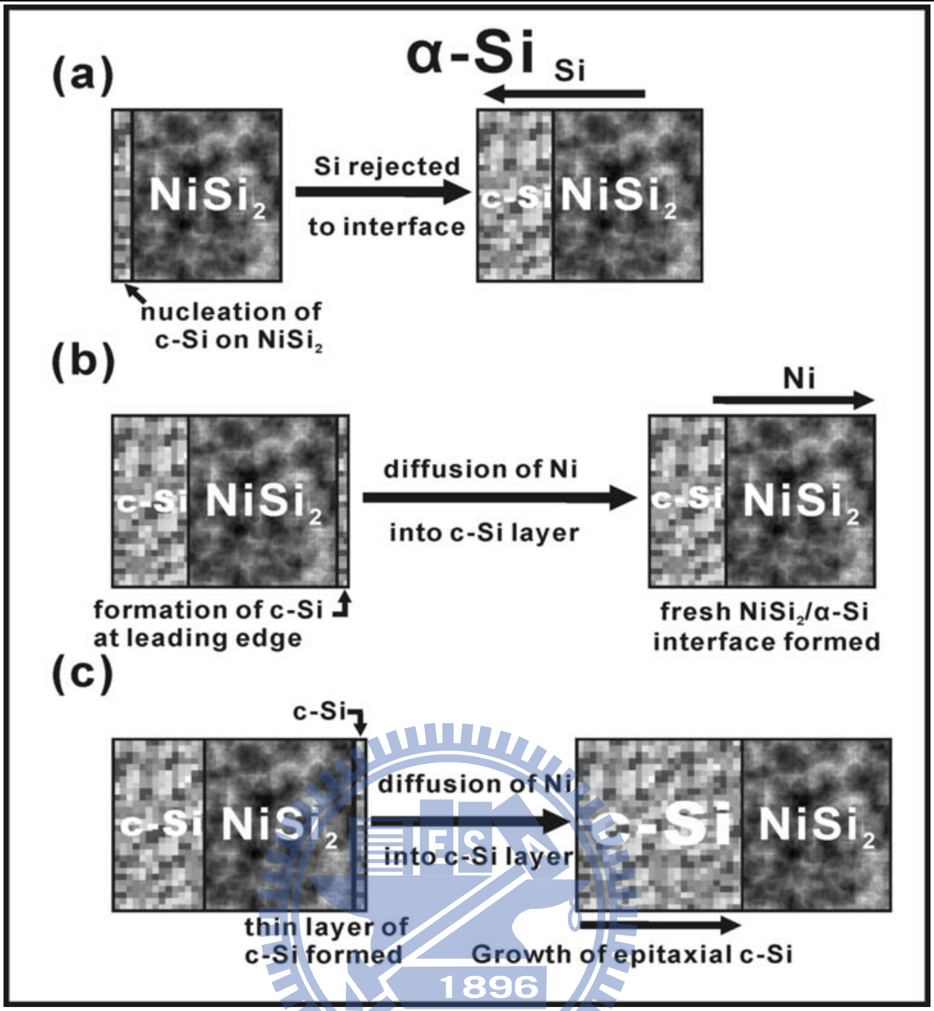

Fig. 1-9 Schematic representation of a possible growth mechanism involoving the formation of a thin layer of c-Si at the NiSi$_2$/α-Si interface

As a result, Ni remains the undisputed metal of choice for silicide-assisted crystallization. It should be noted that traces of NiSi$_2$ also remain within the c-Si that is left behind after the growth phase. This would have presented an insurmountable obstacle had it not been for the existence of an efficient gettering process [27], [28]. This process utilizes the implantation of phosphorous, followed by low-temperature annealing to generate electrically inactive compounds. Previous studies have demonstrated the effectiveness of the gettering process in removing the remaining silicide in the film after Si crystallization [20], [29]. In practice, the necessity to maintain a low processing temperature poses certain limitations on the quality of the poly-Si microstructure. One way to boost the poly-Si quality is by combining MILC with laser annealing process to produce high quality and good uniformity poly-Si films to realize the system-on-panel technology [30]-[33].

In this thesis, we will focus on the Ni Metal induced lateral crystallization method. To produce high performance LTPS TFTs by combined MILC and CLC method. Moreover, discuss the growth mechanism of MILC and utilized fluorine ion implantation and CF_4 plasma etching treatment to fabricate the LTPS TFT. And develop a simple method to reduce the nickel impurity and passivate the trap-state density within the MILC polycrystalline silicon films by drive-in method.

1.3. Electrical properties of Ni metal-induced lateral crystallization (MILC) thin-film transistors (TFTs)

The MILC method has some advantages over other crystallization methods such as: lower equipment cost, better uniformity than ELC method, and lower thermal budget than SPC method. However, several intrinsic growth characteristics of MILC method always resulted in poor TFT performance, such as higher leakage current (I_{lk}) and poor electrical stability due to large defect (trap state) density in MIC/MILC interface and MILC/MILC grain boundary and high Ni metal contamination [34]-[38]. Fig. 1-10 illustrates the leakage current model using band diagrams [39]-[41], the first situation in Fig. 1-10 (a) is described only the thermal activation of an electron from the valence band to the conduction band. The second situation in Fig. 1-10 (b), the leakage current is induced by the trap or surface state in the band gap. With increase the drain bias, the activation energy of leakage current decreases, which suggests that the high field in the drain depletion region has reduced the barrier that the electron must overcome. This situation comprises two steps: the first step is the thermal activation of an electron from the valence band to a trap state (E_t) in the band gap, and the second step is electron tunneling through this reduced barrier to the conduction band. As such, the dominant leakage current mechanism is thermionic field emission. The third situation in Fig. 1-10 (c) is induced under strong electric field, in which the dominant leakage current mechanism is pure tunneling. With the increase of the electric field, the tunneling length decreases. The presence of the trap state in the band gap assists the process by shorting the effective tunneling length of the electron. In addition, the trap state in the band gap plays an important role in the leakage current model. In the traditional MOSFET, those situations do not occur easily because the trap state is low. This causes different leakage current between MOSFET and TFTs.

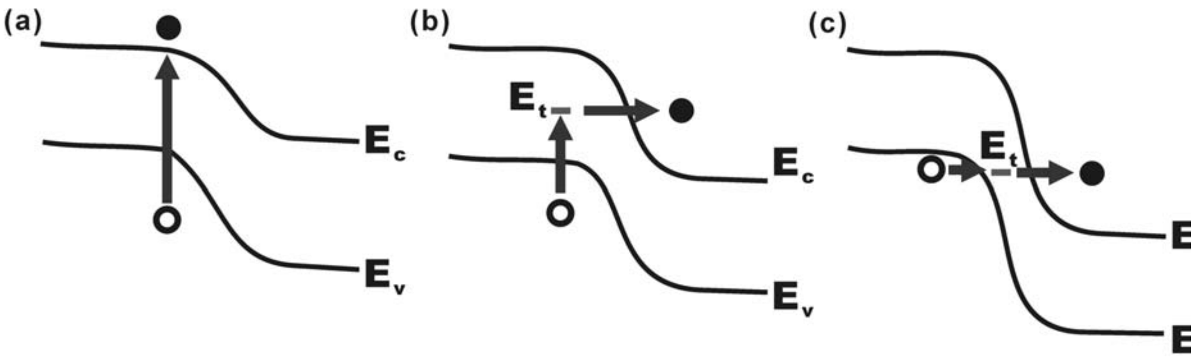

Fig. 1-10 The band diagram for the leakage current model. (a) Case of weak electric field. (b) Case of medium electric field. (c) Case of strong electric field.

Moreover, the Ni contamination of the MILC poly-Si films can degrade the minority carrier life time and increase the leakage current. The leakage current is proportional to the impurity concentration [42]-[43]. In order to solve the above problems, the post-annealing treatment was proposed to reduce the MILC/MILC grain boundary defect density [44]-[46]. In the following, we will discuss the effects of grain boundary and Ni-metal impurity on the electrical performance of MILC TFTs.

1.4. Reliability issue of poly-Si TFTs

The continuous development of poly-Si TFTs was considered to construct high-speed circuits such as processors, memories, and drivers, etc. on non-silicon substrates, such that reliability of poly-Si TFTs, like transistors in integrated circuits on Si substrates, was also a concern. Polycrystalline silicon films consist of a high density of in-grain, grain boundary defects, and broken Si-H bonding so that stressed devices on poly-Si layers normally show significant degradation in electrical characteristics [47]-[50]. In addition, appropriate circuit and device design, the injection of energetic carriers into the gate insulator and subsequent parameter shift through carrier trapping and trap state generation poses one of the most significant long-term reliability concerns in the poly-Si TFTs. It has been known that the application of high drain voltage and a relatively high gate voltage (hot-carrier stressing) in poly-Si TFTs, decreases the maximum transconductance and causes the shift of turn-on voltage. Therefore, a systematical study of the poly-Si TFTs aging with stress time is required.

1.5. Motivation and organization of this thesis

In this thesis, the major research subject is Ni metal induced lateral crystallization of amorphous silicon, which involved of the trap-state density, reliability and uniformity effects on the MILC poly-Si TFTs electrical properties. It has been reported that continuous-wave (CW) laser crystallization (CLC) of α-Si has also been recently employed to fabricate high-performance LTPS TFTs. Compared with excimer laser crystallization (ELC) process; the CLC process was simpler, easier and relatively inexpensive. Unfortunately, their uniformity was poor because the shape of beam profiles was Gaussian. In addition, In MILC, Ni islands are selectively deposited on top of α-Si films and allowed to crystallize at a temperature below 600°C. Three stages have been identified in the MILC crystallization process: (1) the formation of $NiSi_2$ precipitates, (2) the nucleation of crystalline silicon (c-Si) on {111} faces of octahedral $NiSi_2$ precipitates and (3) the subsequent migration of $NiSi_2$ precipitates and crystallization of needlelike Si grain.

Unfortunately, the needlelike grain boundaries easily trap Ni and $NiSi_2$ precipitates which increase the leakage current and shift the threshold voltage. In order to eliminate the trap states of poly-Si film a hydrogen plasma treatment process has been utilized to improve the device performance. However, the hydrogen concentration in the poly-Si film was hard to control, and the formed Si-H bonds were too weak to resist the hot carrier generation. Therefore, the TFT devices of MILC poly-Si in order to provide high performance, the improvement of the uniformity, trap-state density, Ni contamination and reliability were need to be investigated.

This thesis is organized into five parts:

In Chapter 2, to improve the uniformity of CLC-TFT and MILC-TFT, a new method for fabricating MILCLC-TFT was proposed. Instead of α-Si, MILC-Si film was irradiated by CW laser of various output powers.

In Chapter 3, a sample manufacture method using fluorine-ion implantation was proposed for MILC poly-Si TFTs. The advantage of this technique is to provide an uncomplicated and effective method to originate fluorine atoms into MILC poly-Si films.

In Chapter 4, CF_4 plasma was employed to improve the electrical performance of conventional MILC TFTs. This uncomplicated and effective method involves etching away the top surface of MILC poly-Si and passivating the trap states.

In Chapter 5, a novel fabrication process has been developed to reduce the Ni concentration and minimizes the trap-state density of MILC TFTs using nickel drive-in induced laterally crystallization (DILC). The DILC poly-Si was prepared by collision between fluorine ion (F^+) implantation and Ni through the designed pattern into α-Si layer.

In Chapter 6, conclusions and future works are summarized respectively.

Chapter 2

Electrical characteristics and stability of poly-Si TFTs fabricated by continuous-wave laser annealing of metal-induced lateral crystallized silicon films

2.1. Introduction

Low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) have attracted considerable interest for their application in organic emitting diode displays and liquid crystal displays, since they exhibit good electrical properties and can be integrated in peripheral circuits on inexpensive glass substrates [51]. For the application to system on panel and solar cells, the uniformity of polycrystalline silicon (poly-Si) grain size and crystallinity should be improved.

As LTPS TFTs require glass substrates, intensive studies on reducing the crystallization temperature of amorphous silicon (α-Si) films have thus been carried out.

Ni-metal-induced lateral crystallization (MILC) is one of these efforts. In MILC, Ni islands are selectively deposited on top of α-Si films and allowed to crystallize at a temperature below 600°C [32], [52]. Continuous-wave (CW) laser crystallization (CLC) of α-Si has also been recently employed to fabricate high-performance LTPS TFTs[53]-[56]. Compared with excimer laser crystallization (ELA) process, the CLC process was simpler, easier and relatively inexpensive. Unfortunately, their uniformity was poor because the shape of beam profiles was Gaussian [57].

To improve the uniformity of CLC-TFT, a new method for fabricating MILCLC-TFT was proposed in this letter. Instead of α-Si, MILC-Si film was irradiated by CW laser of various output powers.

2.2. Experiment procedure

Two kinds of Si films (α-Si and MILC-Si) were irradiated by CW laser at room temperature in an air atmosphere. Samples designated as “CLC” were α-Si films and those designated as “MILCLC” were MILC-Si films irradiated by CW laser.

2.2.1. CLC poly-Si TFTs

A four-inch quartz wafer with a 500-nm-thick wet oxide layer was used as the substrate. To form the α-Si film, a silane-based undoped α-Si layer of 100 nm thick was deposited using low-pressure chemical vapor deposition (LPCVD). To form the CLC-Si film, α-Si films were then irradiated using a CW laser of various output powers (2.5 W, 3.8 W and 5 W). Reactive ion etching (RIE) was employed to form islands of poly-Si regions on the wafers. Next, a 100-nm-thick tetraethylorthosilicate/O_2 oxide layer was deposited as the gate insulator by plasma-enhanced chemical vapor deposition (PECVD). Then a 200-nm-thick poly-Si film was deposited as the gate electrode by LPCVD. After defining the gate, self-aligned 40 keV phosphorous ions were implanted at a dose of 5×10^{15} cm^{-2} to form the source/drain and gate. Dopant activation was performed at 600°C in N_2 ambient for 24 h. Contact holes were formed and a 500-nm-thick Al layer was then deposited by thermal evaporation and patterned as the electrode. Sintering process was performed at 400°C for 30 min.

2.2.2.MILCLC poly-Si TFTs

A four-inch quartz wafer with a 500-nm-thick wet oxide layer was used as the substrate. To form the α-Si film, a silane-based undoped α-Si layer of 100 nm thick was deposited using low-pressure chemical vapor deposition (LPCVD). To form the MILC-Si film, Ni lines were deposited on the α-Si film and subsequently annealed at 550°C for 12 h [58]. MILC-Si films were then irradiated using a CW laser of various output powers (2.5 W, 3.8 W and 5 W). When fabricating the MILCLC poly-Si, the scanning direction of the CW laser was parallel to the MILC needlelike poly-Si grains. Reactive ion etching (RIE) was employed to form islands of poly-Si regions on the wafers. Next, a 100-nm-thick tetraethylorthosilicate/O_2 oxide layer was deposited as the gate insulator by plasma-enhanced chemical vapor deposition (PECVD). Then a 200-nm-thick poly-Si film was deposited as the gate electrode by LPCVD. After defining the gate, self-aligned 40 keV phosphorous ions were implanted at a dose of 5×10^{15} cm^{-2} to form the source/drain and gate. Dopant activation was performed at 600°C in N_2 ambient for 24 h. Contact holes were formed and a 500-nm-thick Al layer was then deposited by thermal evaporation and patterned as the electrode. Sintering process was performed at 400°C for 30 min.

2.3. Results and discussion

2.3.1. SEM analysis of CLC poly-Si films

Fig. 2-1 to Fig. 2-3 shows SEM images of the Secco-etched CLC irradiated under various laser output powers. As can be seen, the CLC poly-Si comprises grains of various sizes distributed in three distinct regions [57]. As shown in Fig. 2-1, at laser output power of 2.5 W, CLC-2.5 was found in the solid phase crystallization (SPC) region with fine grains. With increasing laser output power, CLC-3.8 was in the partially melted region with large ELC poly-Si-like grains, as shown in Fig. 2-2. [57]. When the laser output power reached 5.0 W, CLC-5.0 was in the completely melted region. As seen in Fig. 2-3, the uniformity of CLC-5.0 grains was poor. It contained both ELC poly-Si-like grains and very large directional grains.

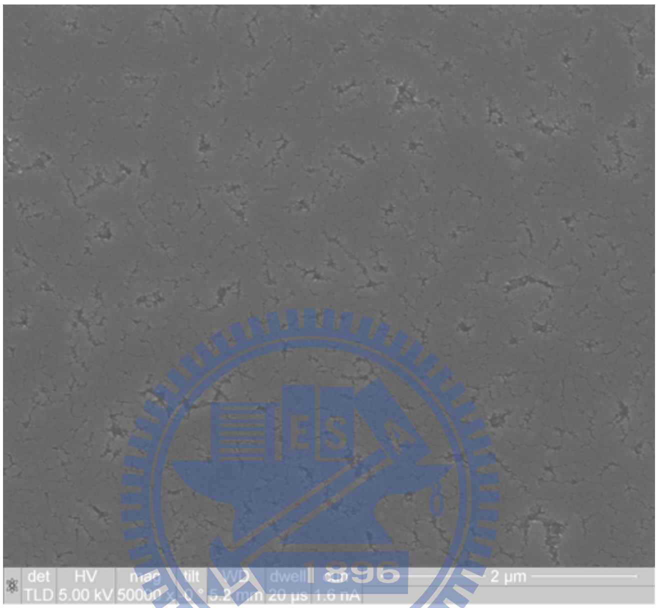

Fig. 2-1 SEM images of Secco-etched poly-Si grains irradiated by CW laser with CLC-2.5 W

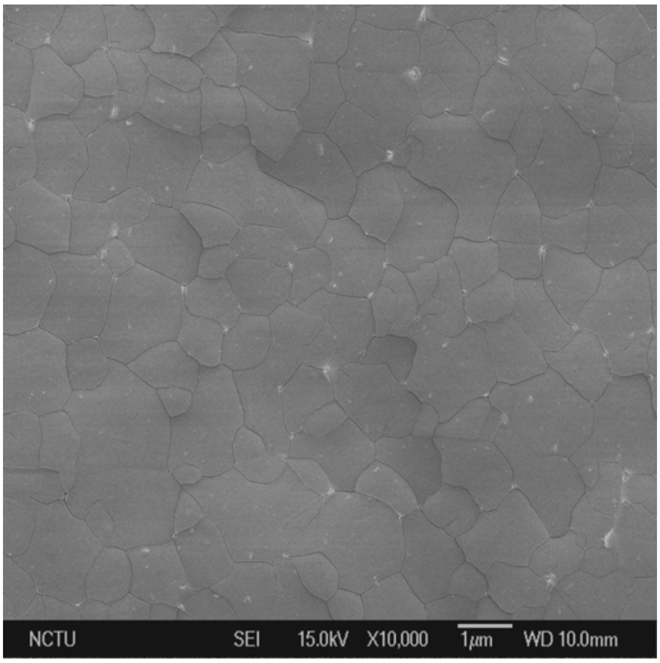

Fig. 2-2 SEM images of Secco-etched poly-Si grains irradiated by CW laser with CLC-3.8 W

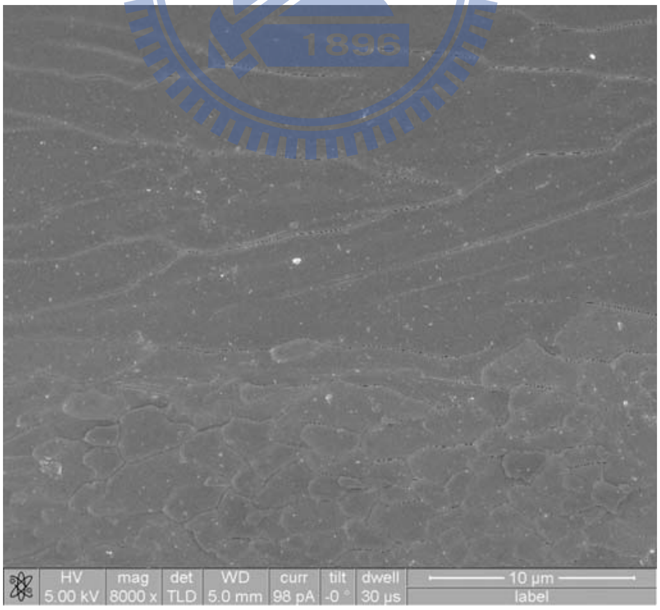

Fig. 2-3 SEM images of Secco-etched poly-Si grains irradiated by CW laser with CLC-5.0 W

2.3.2.SEM analysis of MILCLC poly-Si films

Fig. 2-4 to Fig. 2-6 shows SEM images of the Secco-etched MILCLC irradiated under various laser output powers. As for the fabrication of the MILCLC poly-Si, Fig. 2-4 shows that at lower laser output power, the sizes and shapes of MILCLC-2.5 needle Si grains were similar to those of MILC poly-Si. This is because MILCLC-2.5 was in the SPC region. Only some of the α-Si regions among Si grains were melted and crystallized. When the laser output power reached 3.8 W, the width of MILCLC-3.8 grains increased to 3 μm, as shown in Fig. 2-5. Compared with that of CLC-3.8, the grain size of MILCLC-3.8 was larger and the uniformity was better. We believe that most of the a-Si and small MILC grains in this regime were molten. However, the large grains were only molten partially and served as predetermined nuclei for grain growth. The width of these grains increased markedly due to the geometrical coalescence of Si needle grains. Geometrical coalescence can be simply described as an encounter of grains whose relative orientations are similar during grain growth [59]. The grain boundary between grains disappears and results in sudden development of a much larger grain. This coalescence is an important phenomenon for grains having a strong preferred orientation. In this study, MILC needle Si grains had a strong preferred orientation of <111>.

The crystal structure of MILCLC-5.0 was similar to that of CLC-5.0. It contained both ELC poly-Si-like grains and very large directional grains. As shown in Fig. 2-6, the uniformity of MILCLC-5.0 grains was poor. This is because MILCLC-5.0 was in the completely melted region.

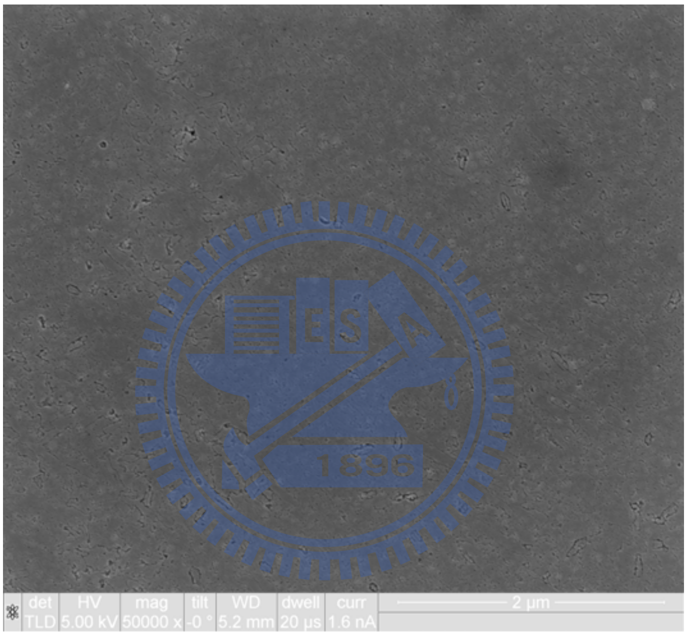

Fig. 2-4 SEM images of Secco-etched poly-Si grains irradiated by CW laser with MILCLC-2.5 W

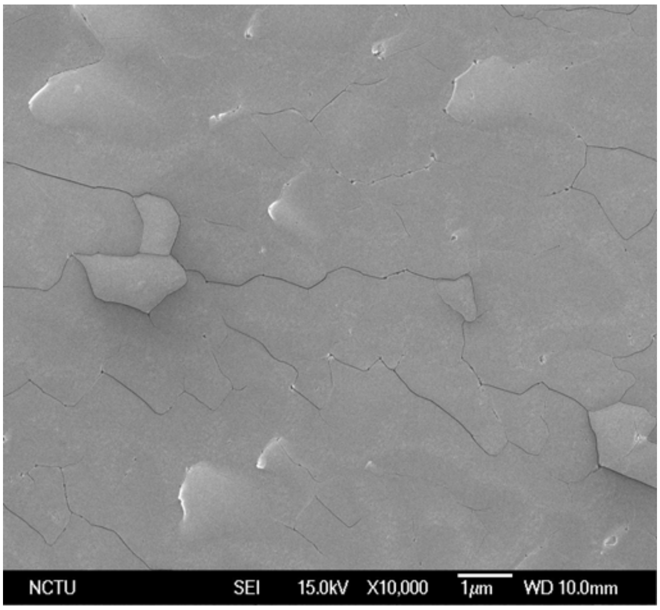

Fig. 2-5 SEM images of Secco-etched poly-Si grains irradiated by CW laser with MILCLC-3.8 W

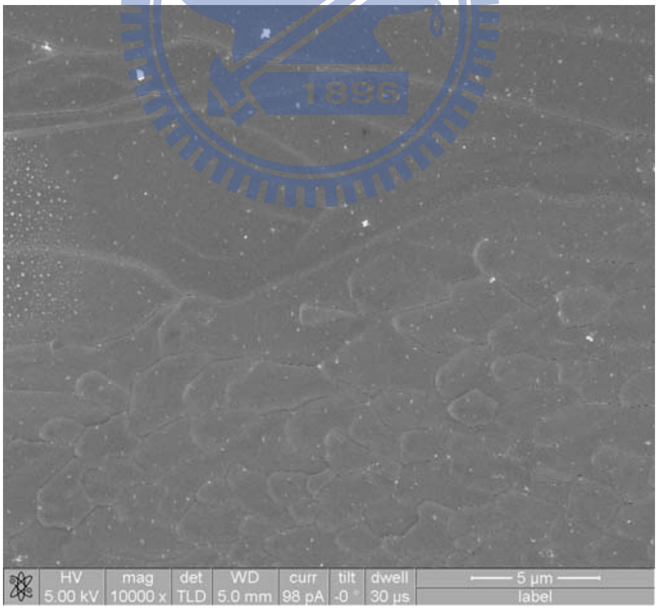

Fig. 2-6 SEM images of Secco-etched poly-Si grains irradiated by CW laser with MILCLC-5.0 W

2.3.3.Electrical properties of CLC and MILCLC TFTs

Fig. 2-7 shows the transfer characteristics and field-effect mobility versus the gate voltage of TFTs in the random grain structure for $W = L = 20$ μm at $V_{DS} = 5$ V and $V_{DS} = 0.1$ V, respectively. The measured and extracted key device parameters are also summarized in Fig. 2-7. The threshold voltage (V_{th}) was defined as the gate voltage required to achieve a normalized drain current of $I_{DS} = (W / L) \times 100$ nA at $V_{DS} = 5$ V. It was found that when the laser output power was 5.0 W, the electrical performance of MILCLC-5.0 and CLC-5.0 were similar, both showing excellent performance. This is because they were in the completely melted region. Both Si films had very large directional grains.

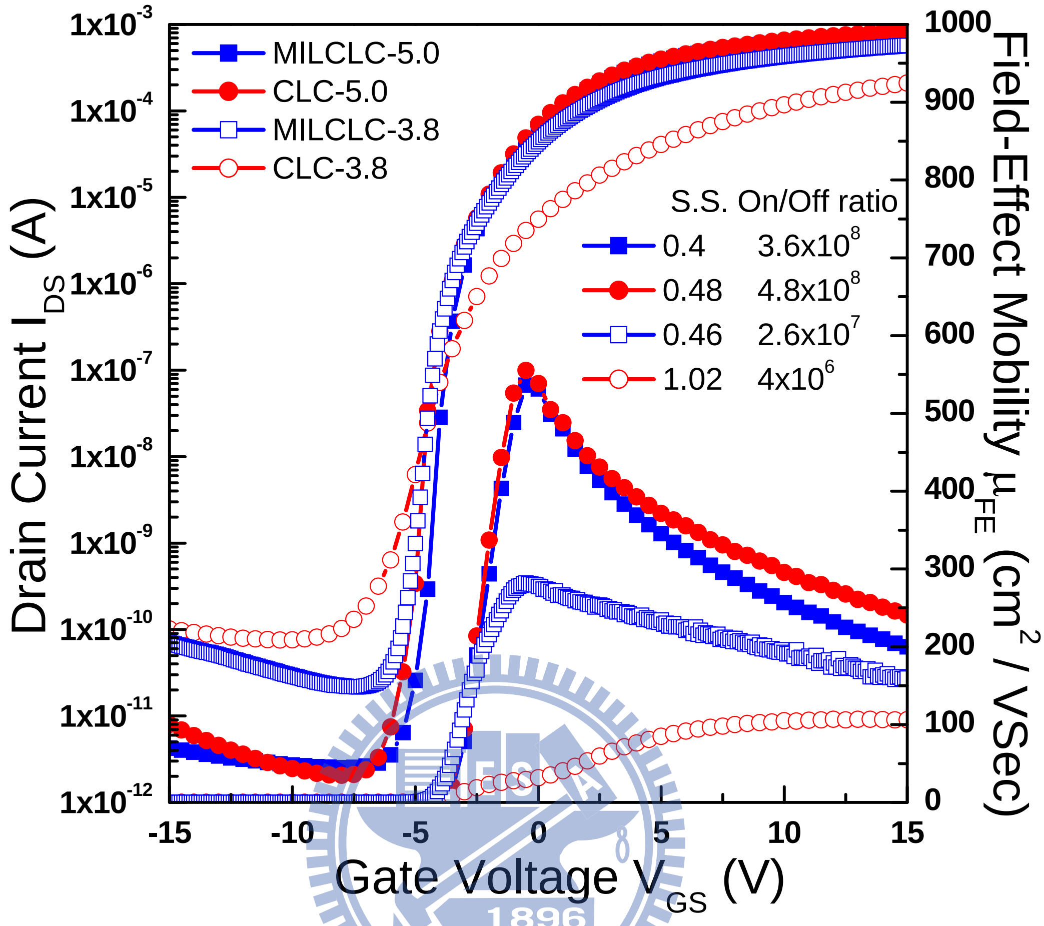

Fig. 2-7 Typical I_{DS}-V_{GS} transfer characteristics and field-effect motilities of MILCLC and CLC TFTs (W/L=20 μm/20 μm)

However, the performance of MILCLC-3.8 and CLC-3.8 TFTs were quite different when the laser output power was 3.8 W. Compared with CLC-3.8 TFTs, MILCLC-3.8 TFTs exhibited higher field-effect mobility, superior subthreshold slope (SS), lower threshold voltage (V_{th}), and higher ON/OFF current ratio. The superior performance of MILCLC-3.8 is attributed to the quality of large silicon grains. As seen in Fig. 2-5, the size of MILCLC-3.8 coalescence grains was larger than that of CLC-3.8 grains. Moreover, most of these coalescence grains and their boundaries were parallel to the drain current (I_{ds}), which reduced the impedance to carrier flow. This in turn decreased the threshold voltage and increased greatly the mobility and I_{on}/I_{off} current ratio.

The electrical characteristics of both CLC-2.5 and MILCLC-2.5 were not as good as those of other TFTs. The performance of CLC-2.5 TFT was similar to that of SPC since CLC-2.5 film contained SPC poly-Si-like grains. On the other hand, the performance of MILCLC-2.5 TFT was similar to that of MILC-Si since only some of the α-Si regions among MILC grains were melted. As a result, the mobility of CLC-2.5 was 4.1 cm^2/Vs, while that of MILCLC-2.5 was 50 cm^2/Vs [60].

2.3.4.Uniformity of CLC and MILCLC TFTs

The other important issue of poly-Si TFTs is their uniformity for the application on SOP and solar cells. As shown in Fig. 2-8, 10 TFTs were measured in each case to investigate the device-to-device variation. TABLE 2-1 lists the average values of the field-effect mobility and threshold voltage of TFTs with standard deviations in parentheses. Since the electrical characteristics of CLC-2.5 and MILCLC-2.5 were poor, their uniformities were not listed here. Although the mobility of both MILCLC-5.0 and CLC-5.0 was high, their uniformity was poor and their standard deviations were large. This is because both films contained two different kinds of grains: ELC poly-Si-like grains and very large directional grains. The uniformity of CLC-3.8 and MILCLC-3.8 was much better and their standard deviations were small. As mentioned previously, MILCLC-3.8 has uniformly distributed geometrical coalescence grains. As a result, MILCLC-3.8 has the smallest standard deviation.

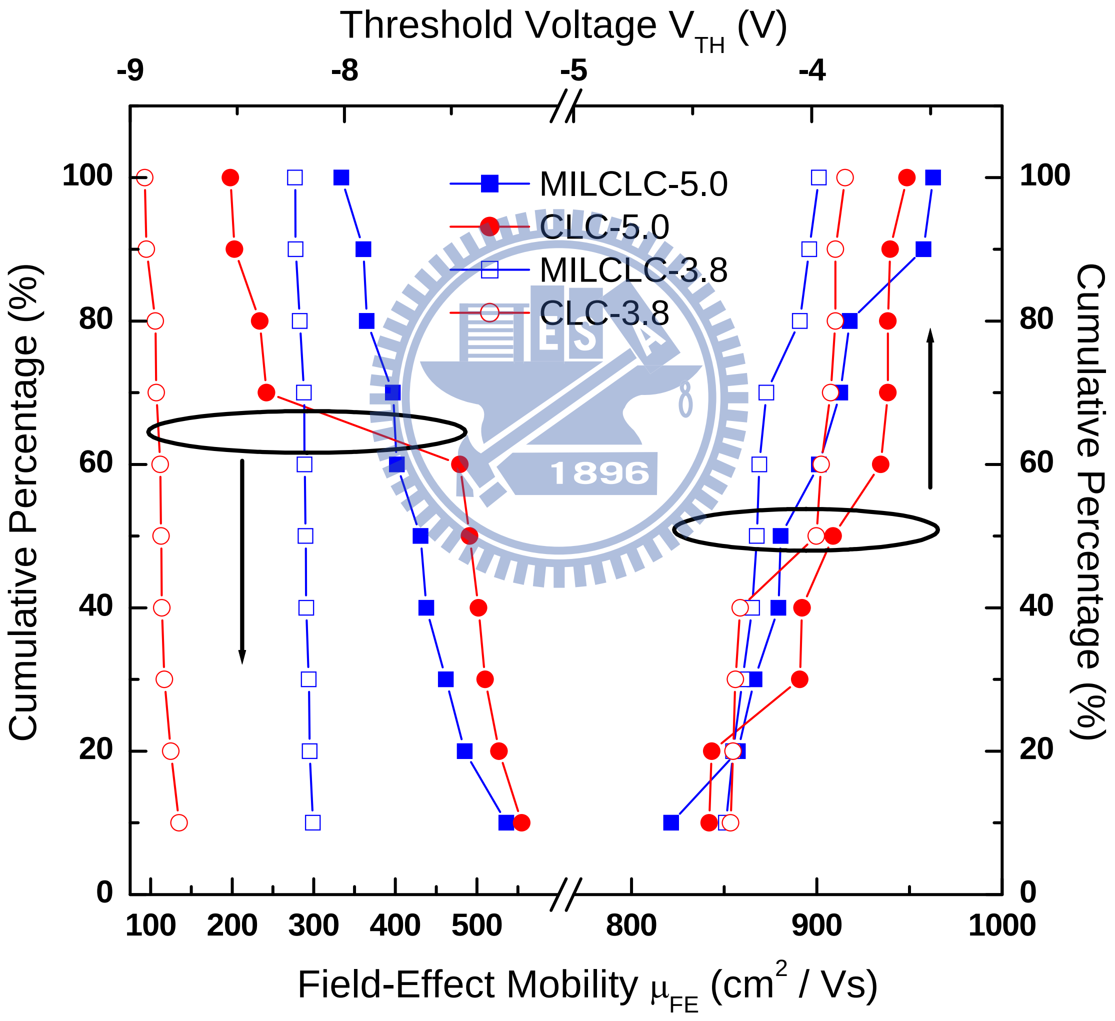

Fig. 2-8 Ten TFTs were measured in each case in field-effect mobility and threshold voltage to investigate the device-to-device variation.

TABLE 2-1 Average values of field-effect mobility and threshold voltage of two different structures with standard deviations in parentheses.

TFT (W = L = 20 μm)	Field-effect Mobility (cm^2/Vs) μ_{FE}	Threshold Voltage (V) V_{TH}
MILCLC-5.0	421 (62)	-4 (0.34)
CLC-5.0	394 (152)	-3.9 (0.31)
MILCLC-3.8	288 (7.2)	-4.19 (0.13)
CLC-3.8	112 (13)	-4.08 (0.21)

2.4. Conclusion

To improved uniformity and electrical performance of CLC-TFTs, two kinds of Si films (α-Si and MILC-Si) were used in this study. After irradiated by CW laser of various output powers (2.5 W, 3.8 W and 5 W), it was found that the performance and uniformity of MILCLC-TFTs were better than those of CLC-TFTs. When the laser output power was low (2.5 W), both films were in the SPC region. Only some of the α-Si regions were melted. The electrical characteristics of CLC-2.5 and MILCLC-2.5 were poor. When the laser output power reached 5.0W, CLC-5.0 and MILCLC-5.0 were in the completely melted region. They both showed excellent performance. Unfortunately, the uniformity was poor because they contained two kinds of grains: ELC poly-Si-like grains and very large directional grains. When the laser output power was median (3.8 W), CLC-3.8 and MILCLC-3.8 were in the partially melted region with large ELC poly-Si-like grains. The performance and uniformity of MILCLC-3.8 were much better than those of CLC-3.8. This is because the width of the MILCLC-3.8 grains increased dramatically due to the geometrical coalescence of MILC-Si needle grains. Moreover, the uniformity of MILCLC-3.8 was far superior to that of CLC-5.0 and MILCLC-5.0, and therefore was suitable for SOP application.

Chapter 3

Effect of the F^+ implantation on the electrical characteristics and reliability of MILC poly-Si TFTs

3.1. Introduction

In recent years low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) have attracted considerable interest for their use in active-matrix liquid crystal displays (AMLCDs) since they exhibit good electrical properties and can be integrated in peripheral circuits on inexpensive glass substrates [51]. Since poly-Si thin film transistors (TFTs) require glass substrates, intensive studies have been carried out reducing the crystallization temperature of amorphous silicon (α-Si) films. Ni-metal-induced lateral crystallization (MILC) is one of these efforts. In MILC, Ni islands are selectively deposited on top of α-Si films and allowed to crystallize at a temperature below 600°C [32], [52]. Three stages have been identified in the MILC crystallization process: (1) the formation of $NiSi_2$ precipitates, (2) the nucleation of crystalline silicon (c-Si) on {111} faces of octahedral $NiSi_2$ precipitates and (3) the subsequent migration of $NiSi_2$ precipitates and crystallization of needlelike Si grain [21].

Unfortunately, the needlelike grain boundaries easily trap Ni and $NiSi_2$ precipitates which increase the leakage current and shift the threshold voltage [34], [36], [37], [61], [62]. In order to eliminate the trap states of poly-Si film a hydrogen plasma treatment process has been utilized to improve the device performance [63]. However, the hydrogen concentration in the poly-Si film was hard to control, and the formed Si-H bonds were too weak to resist the hot carrier generation.

In this section, a sample manufacture method using fluorine-ion implantation was proposed for MILC poly-Si TFTs. The advantage of this technique is to provide an uncomplicated and effective method to originate fluorine atoms into MILC poly-Si films. The electrical characteristics including I-V measurement, trap-state density, activation energy (E_A), on/off ratio, and hot carrier stress on threshold voltage shift (ΔV_{TH}) are reported in this work.

3.2. Experiment procedure

As shown in Fig. 3-1, the process of poly-Si films began with four-inch Si(100) wafer substrates where a 100 nm thick undoped amorphous silicon (α-Si) layer was deposited on a 500 nm thick oxide coated silicon wafer by low pressure chemical vapor deposition

(LPCVD) system. The photoresist was patterned to form the desired Ni lines, and a 20-Å-thick Ni film was deposited on the α-Si. The samples were then dipped into an acetone for 5 min to remove the photoresist, and subsequently annealed at 540°C for 18 h to form the MILC poly-Si film. To reduce Ni contamination, the unreacted Ni metal was removed by chemical etching. Reactive ion etching (RIE) was employed to form islands of poly-Si regions on the wafers. Fluorine ions were then implanted into the MILC film. The projection range of fluorine-ions was set at the middle of MILC layer thickness. The dosage of fluorine ions and ion accelerating energy were 2×10^{13} cm^{-2} and 30 KeV, respectively. Next, a 100 nm thick SiH_4/N_2O oxide layer was deposited as the gate insulator by plasma-enhanced chemical vapor deposition (PECVD). Then, a 200 nm thick poly-Si film was deposited as gate electrode by LPCVD. After defining the gate, self-aligned 40 KeV phosphorous ions were implanted at a dose of 5×10^{15} cm^{-2} to form source/drain and gate. The F^+-implanted MILC film and the P^+_{31}-implanted source/drain/gate were then annealed/activated at 600°C for 24 h. A 500 nm thick SiO_2 film was deposited by PECVD to serve as a passivation layer. Contact holes were opened through the oxide layer, and 500 nm of aluminum (Al) was deposited, defined, and etched to form the metal pads. Finally, the finished MILC poly-Si TFT devices were sintered in a thermal furnace at 350°C for 30 min. For the purpose of comparison, heavy F^+-implanted

MILC TFTs (2×10^{14} cm^{-2} and 2×10^{15} cm^{-2}) were also investigated.

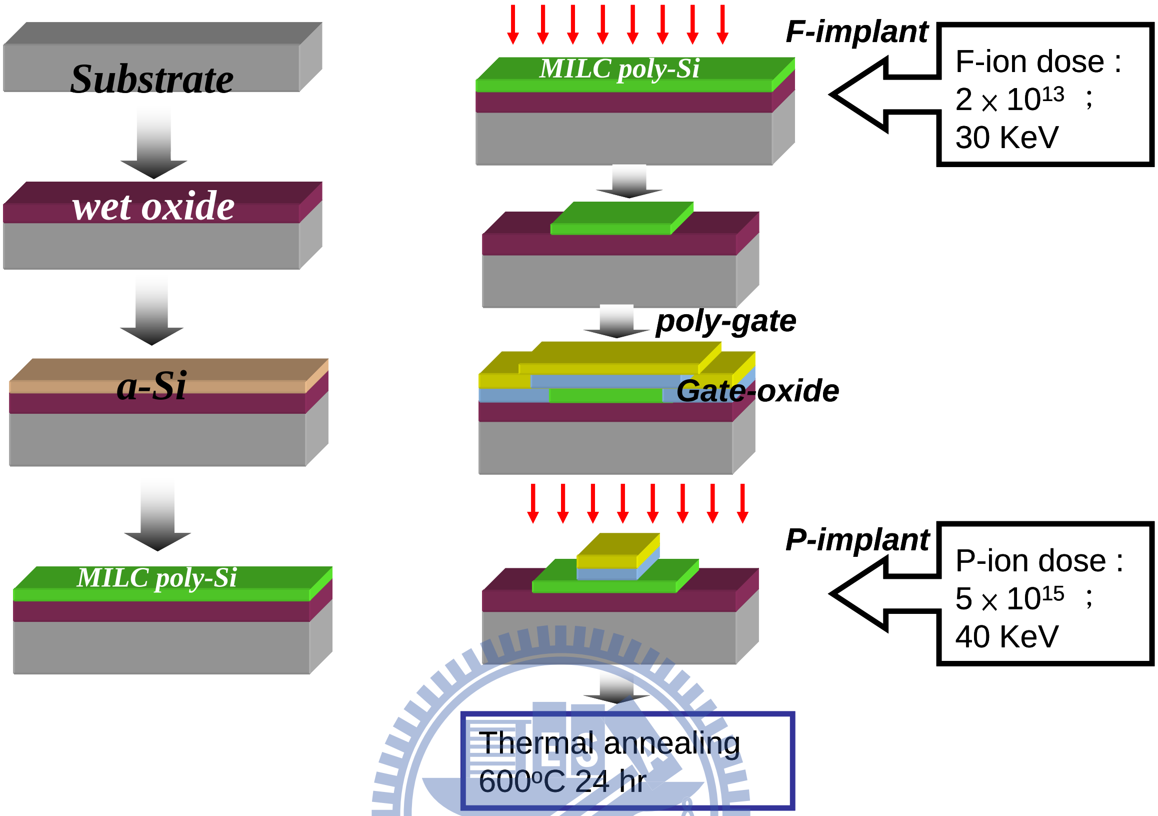

Fig. 3-1 Schematic diagrams of process flow of MILC poly-Si TFTs with and without F$^+$ implantation.

3.3. Results and discussion

3.3.1. Electrical properties of MILC-TFTs with and without F$^+$ implantation

Fig. 3-2 shows the transfer characteristics and field-effect mobility versus the gate voltage of MILC poly-Si TFTs with and without F$^+$ implant treatment. The measured and extracted key device parameters are summarized in TABLE 3-1. The measurement were performed at V_{DS} = 0.1 and 5 V. The threshold voltage (V_{th}) was defined as the gate voltage required to achieve a normalized drain current of $I_{DS} = (W / L) \times 100$ nA at $V_{DS} = 5$ V. The subthreshold slope (SS) and V_{th} of the F^+-implanted MILC TFTs were 1.1 V/dec. and 5.9 V, which were superior to 2.0 V/dec. and 9.2 V of MILC TFTs. The ON/OFF current ratios of the MILC poly-Si TFTs with and without the F^+ implant treatment were 9.91×10^6 and 3.72×10^6 at $V_{DS} = 5$ V, respectively. The output characteristic is shown in Fig. 3-3, exhibiting the better improvement at a drain current of the F^+-implanted MILC TFTs at $V_{GS} = 12$ V and 20 V. These improvements were attributed to the reduction of the defects in the poly-Si film. In MILC poly-Si, Ni-related defects may degrade electric performance because they introduce trap states including dangling bonds and strain bonds. Most of these defects were located at the MILC poly-Si/buffer-oxide interface since high Ni contents have been observed at the interface [64].

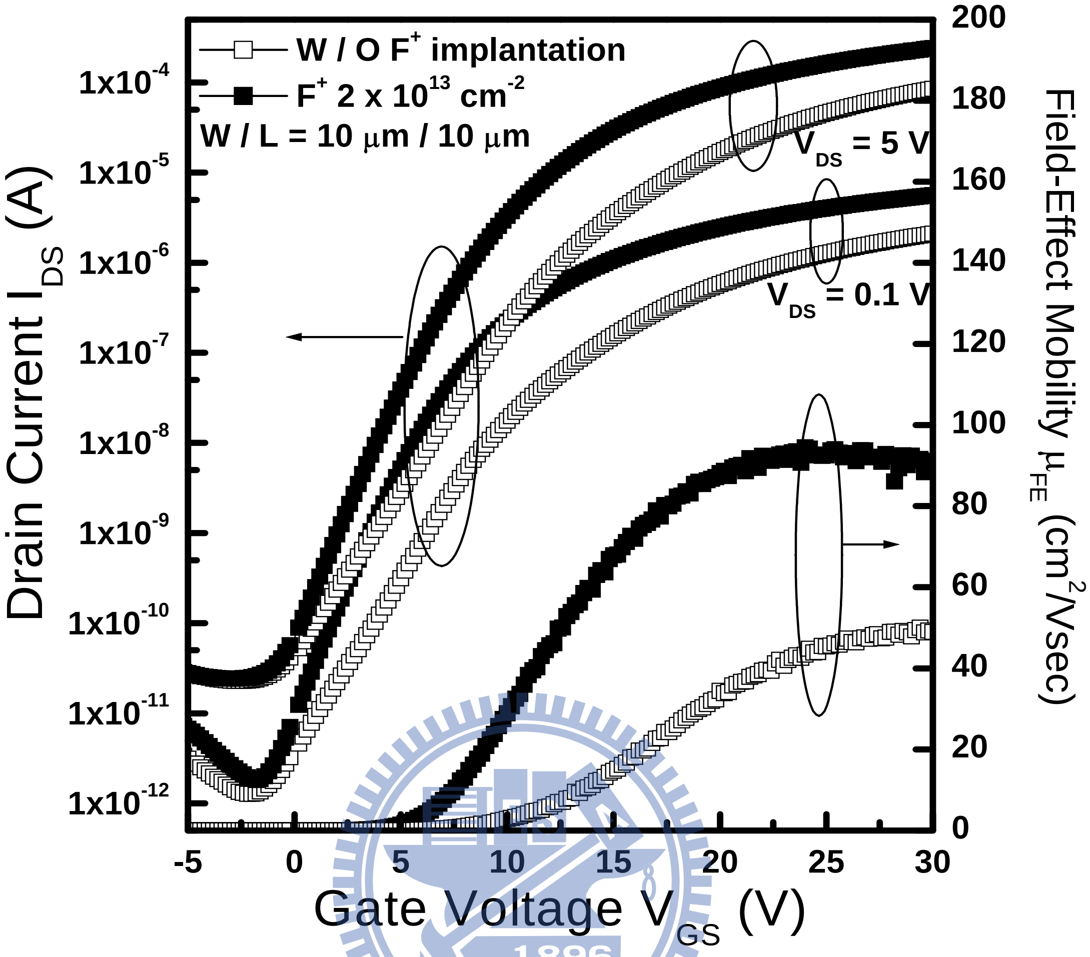

Fig. 3-2 The transfer characteristics and field-effect mobility of the MILC poly-Si TFTs with and without F$^+$ implantation.

TABLE 3-1 Device characteristics of the MILC poly-Si TFTs with and without F$^+$ implantation

Device Parameters	Without F$^+$-implantation	F$^+$-implantation 2×10^{13}cm^{-2}	F$^+$-implantation 2×10^{14}cm^{-2}
Field-effect mobility (cm^2 / V^{-s})	**49**	**95**	**70**
Subthreshold slope (V / dec)	**2.0**	**1.1**	**1.5**
Threshold voltage V$_{th}$ (V)	**9.2**	**5.9**	**7.9**
ON/OFF current ratio	**3.72 × 10^6**	**9.91 × 10^6**	**5.69 × 10^6**

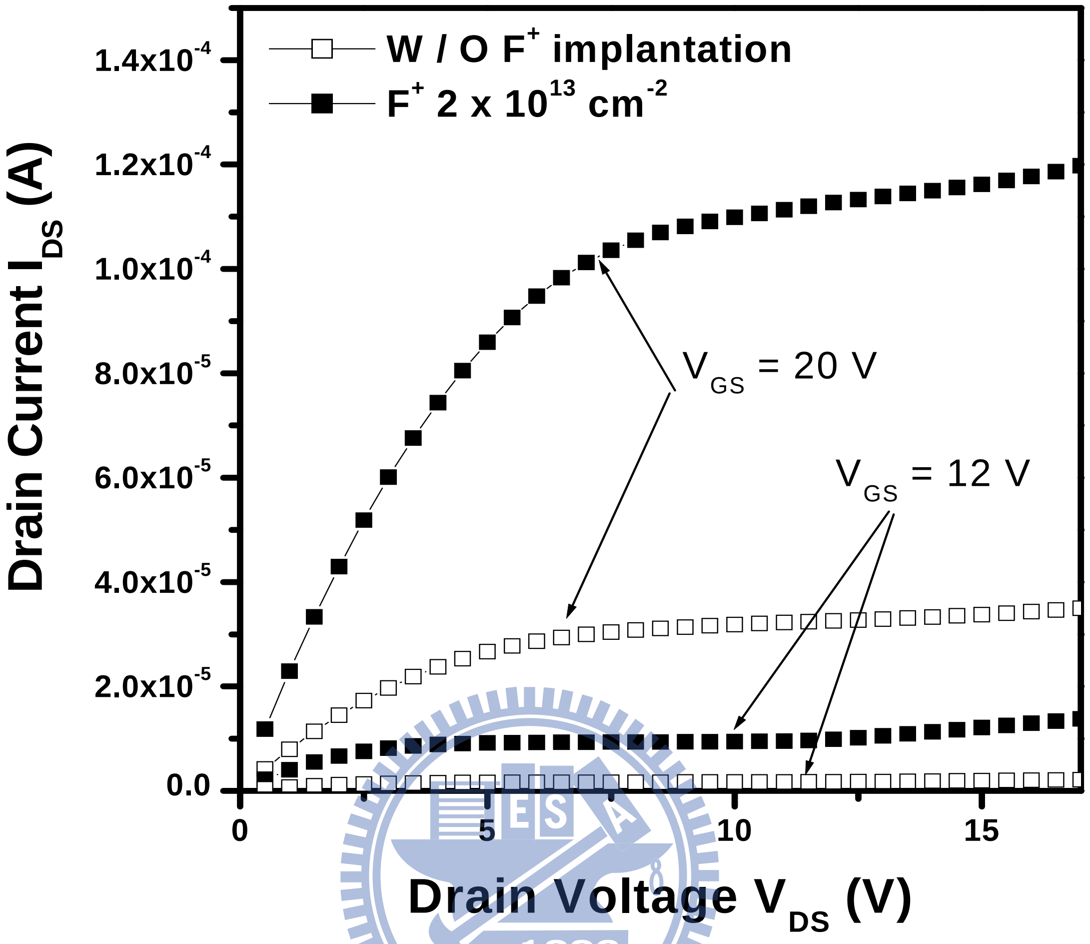

Fig. 3-3 Output characteristics of the MILC poly-Si TFTs with and without F^+ implantation.

3.3.2.SIMS analysis of F^+ implantation Poly-Si film

As shows in Fig. 3-4, secondary ion mass spectrometry (SIMS) depth profile analysis revealed that a high level of fluorine concentration was present at the poly-Si/buffer-oxide interface after thermal annealing at 600°C for 24 h. This result suggests, during the thermal annealing process, fluorine ions diffused to the poly-Si/buffer-oxide interface to passivate the Ni-related defects (trap states) in the MILC poly-Si film, and lead to improve electrical characteristics.

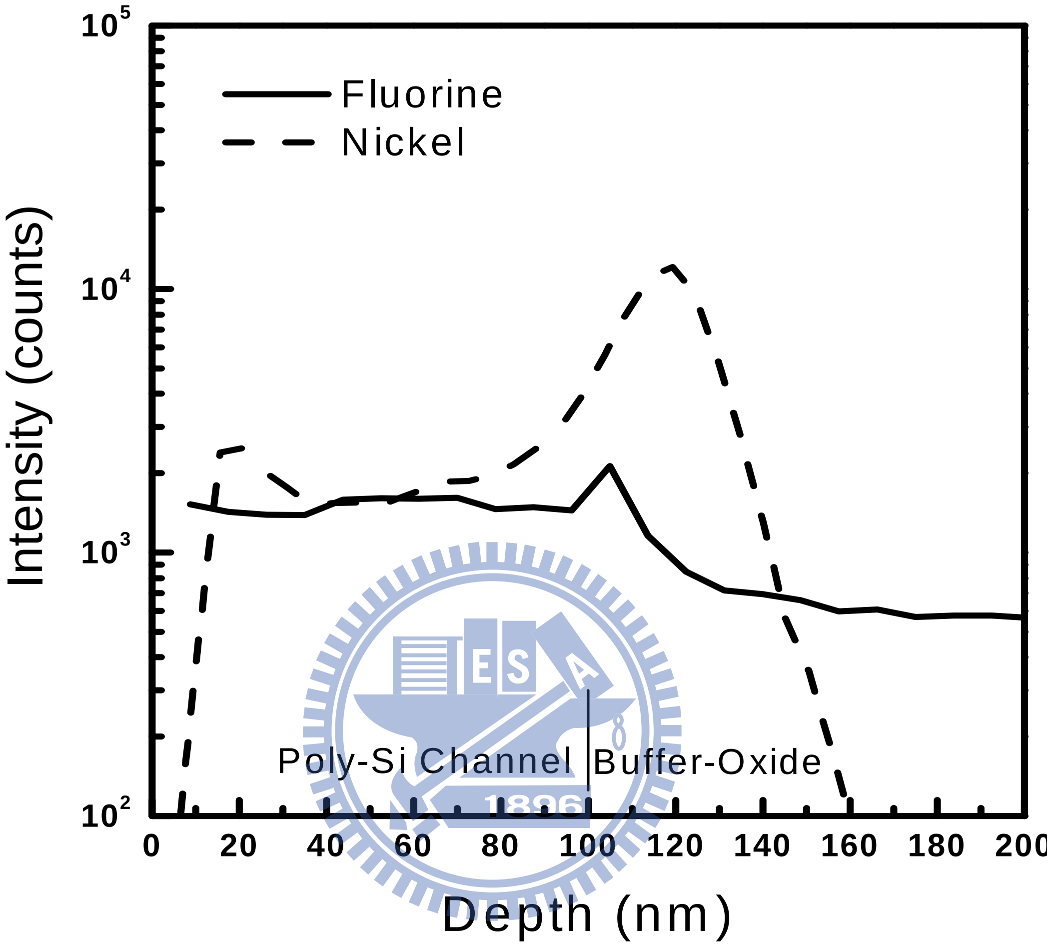

Fig. 3-4 SIMS depth profile of fluorine and nickel in the structure of interface of MILC poly-Si/buffer oxide film after annealing at 600℃ for 24 hr

3.3.3.Influence of F^+ implantation on trap-state density

The trap state densities (N_t) of TFTs were extracted using Levinson and Proano's method, which can estimate the N_t from the slope of the linear segment of ln [I_{DS} / (V_{GS}-V_{FB})] vs. 1 / $(V_{GS}-V_{FB})^2$ at low V_{DS} and high V_{GS}, where V_{FB} is defined as the gate voltage that yields the minimum drain current at V_{DS} = 0.1 V [65], [66]. As shown in Fig.

3-5, the conventional MILC poly-Si TFT exhibits a N_t of 6.29×10^{12} cm^{-2}, whereas the F^+ implantation 4.24×10^{12} cm^{-2}. The reduction in N_t values implies that those defects have been effectively terminated using F^+ implantation.

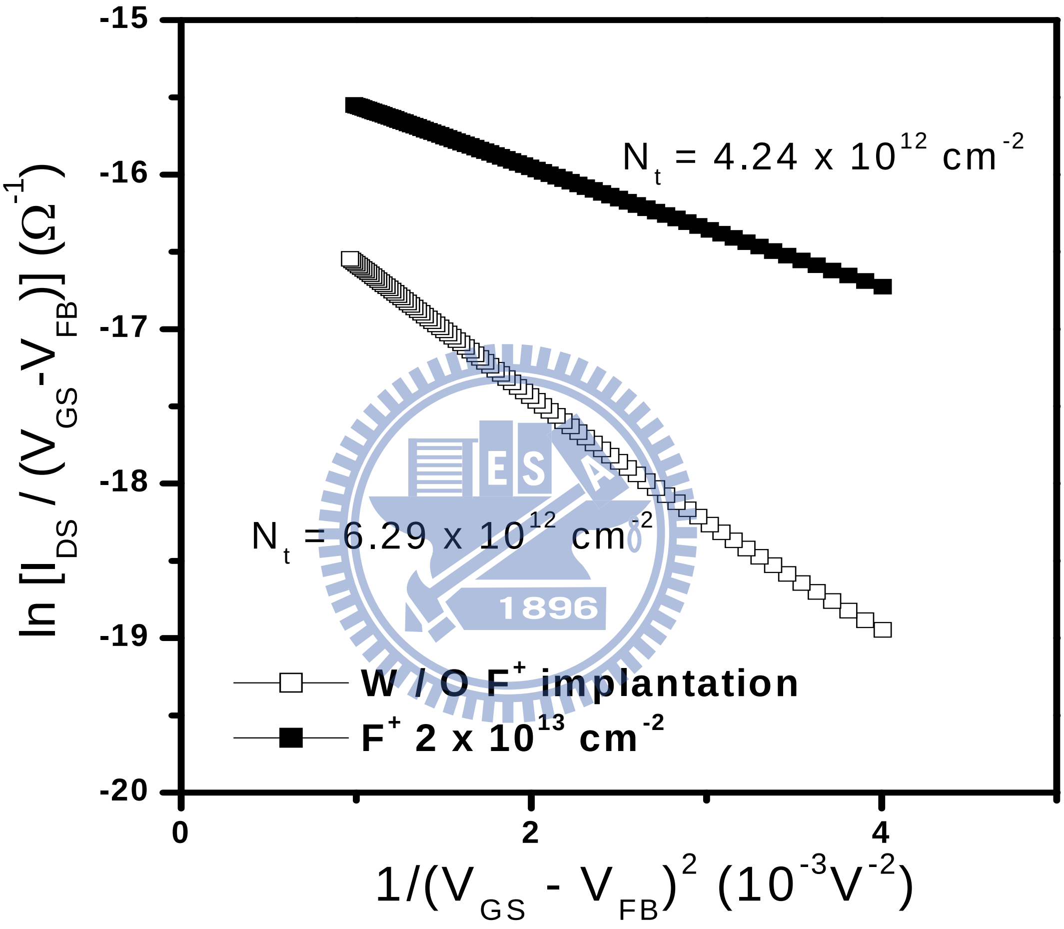

Fig. 3-5 The trap state densities (N_t) of TFTs. They can be estimated from the slope of the linear segment of ln $[I_{DS} / (V_{GS}-V_{FB})]$ vs. $1 / (V_{GS}-V_{FB})^2$ at low V_{DS} and high V_{GS}.

The N_t reduction was also confirmed by the measurement of activation energy (E_A) of drain current. E_A was obtained by the measurement of transfer characteristics at temperature ranging from 25 to 125℃ [67]. It reflects the carrier transportability, which is related to the barrier height in the poly-Si channel. The lower the E_A, the lower the carrier transport barrier will be. Fig. 3-6 shows the E_A of drain current as a function of gate voltage measured at $V_{DS} = 0.1$ V. The E_A of F^+-implanted MILC TFTs was less than that of MILC TFTs. In other words, during the thermal annealing process, fluorine ions lowered the barriers (passivated the trap states) in the MILC poly-Si film, and led to improve the electrical characteristics. However, as shown in TABLE 3-1, the reduction in the N_t did not suppress the minimum off current of the F^+-implanted device. Similar results have been reported in other poly-Si TFTs which were passivated by the F^+ implantation and CF_4 plasma treatment [68]-[70]. The F^+ implantation did not improve the minimum off current of the device.

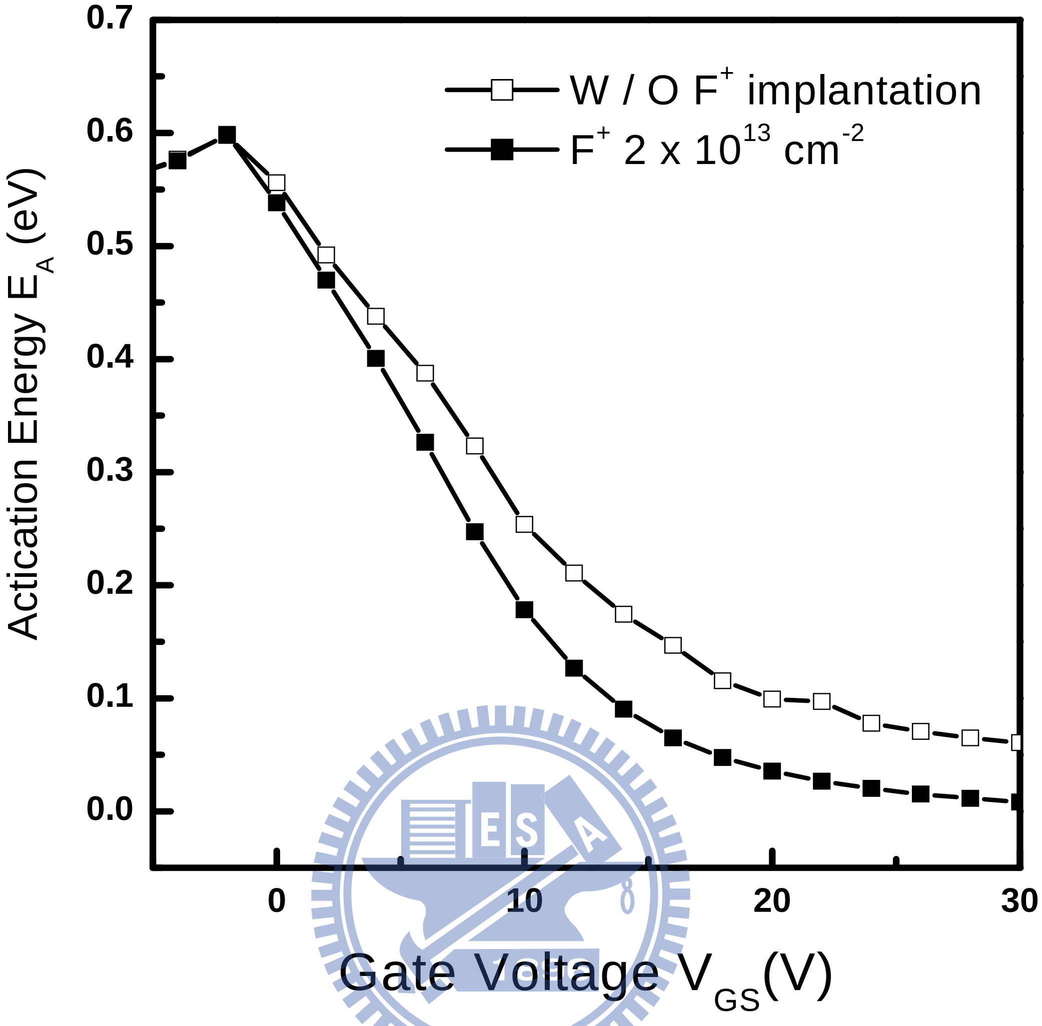

Fig. 3-6 The activation energy (E_A) of drain current as a function of gate voltage measured at V_{DS} = 0.1 V.

Electrical properties of the F^+-implanted MILC poly-Si TFTs with different dosages were also studied in this work. Fig. 3-7 shows the electrical characteristics of MILC poly-Si TFTs with various fluorine ion implantation dosages. The measured and extracted key device parameters are summarized in TABLE 3-1. It was found that the electrical characteristics of F^+-implanted TFTs were improved. A minimum of V_{th} was obtained with an optimal F^+ implantation dosage of 2×10^{13} cm^{-2}. However, the electrical characteristics of F^+-implanted TFTs are degraded as the implantation dosage increases. This is because when the dosages were higher than Si solid solubility, the trap-state density and fluorine clusters increased with the dosage [71]. When dosage reached 2×10^{15} cm^{-2}, the device performance was very poor.

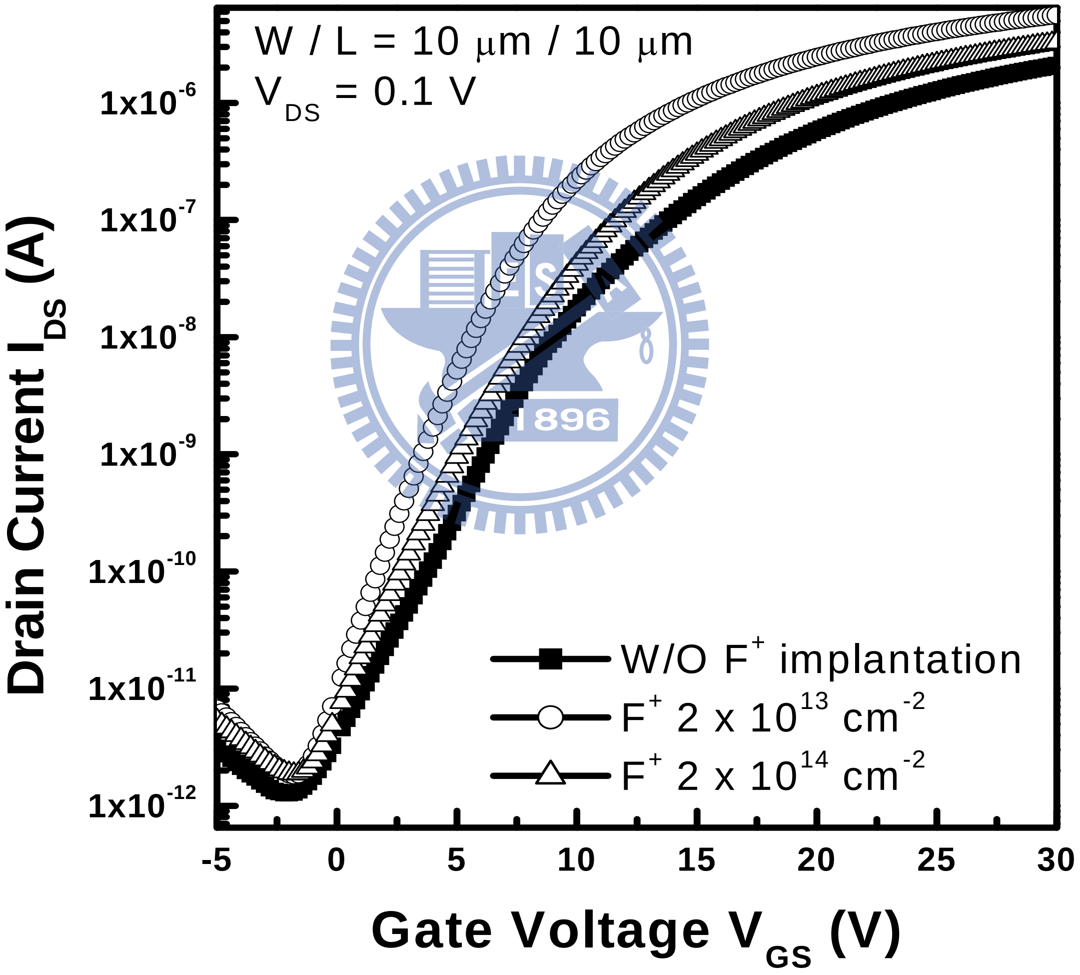

Fig. 3-7 Typical I_{DS}-V_{GS} transfer characteristics of MILC poly-Si TFTs and F^+-implanted MILC poly-Si TFTs with various dosages.

3.3.4.Reliability of MILC poly-Si with and without F^+ implantation

The other important issue of poly-Si TFTs is their reliability, which was examined under hot-carrier stress. Fig. 3-8 is a plot of the ΔV_{TH} versus stressing time at $V_{GS} = 15$ V and $V_{DS} = 25$ V. The threshold voltages of TFTs were degraded because dangling bonds were created at weak Si-Si bonds and Si-H bonds, which trapped electrons [72], [73]. Fortunately, this threshold voltage degradation was improved by F^+ implantation. F^+-implanted TFTs possessed high immunity against the hot-carrier stress and thereby exhibit lower ΔV_{TH} than that of typical MILC TFTs. This is because weaker Si-H and Si-Si bonds were replaced by stronger Si-F bonds. As a result, the electrical reliability of F^+-implanted TFTs was improved.

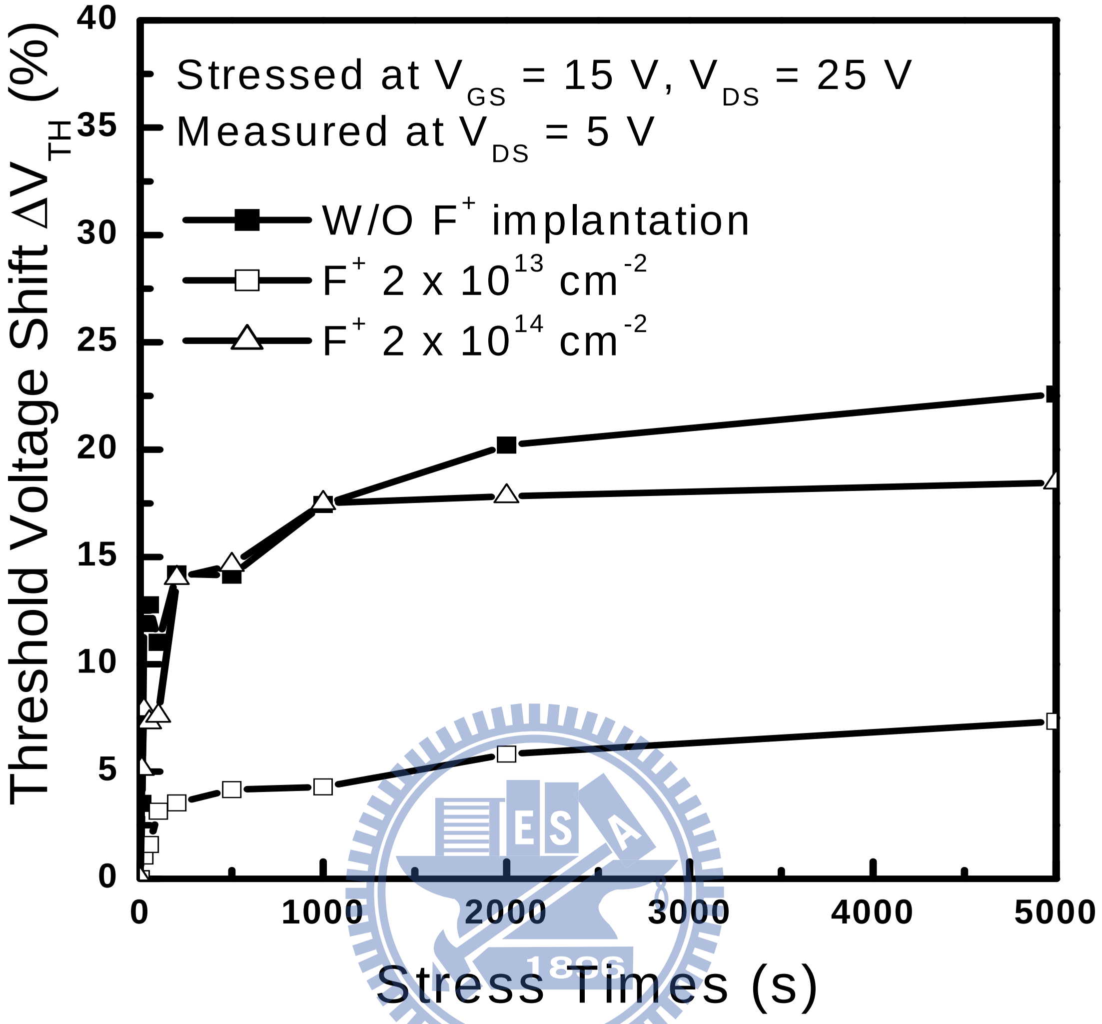

Fig. 3-8 Threshold voltage variation versus stress time of the MILC poly-Si TFTs with and without F^+ implantation.

3.4. Conclusion

In summary, the effect of the F^+ implantation on the electrical characteristics and reliability of MILC poly-Si TFTs was investigated. The fluorine ion accelerating energy was 30 KeV. After annealing at 600°C for 24 h, it was found that F^+-implanted TFT exhibited higher field-effect mobility, superior subthreshold slope, lower threshold voltage, higher ON/OFF current ratio, and lower trap state density (N_t) as compared with typical MILC TFT. It was also found F^+ implantation process can greatly improve the electrical reliability under a hot-carrier stress. This is because weaker Si-H and Si-Si bonds were replaced by stronger Si-F bonds. As a result, F^+-implanted TFTs possessed high immunity against the hot-carrier stress and thereby exhibit lower ΔV_{TH} than that of typical MILC TFTs.

Chapter 4

Influence of etching treatment on electrical and reliability of MILC poly-Si TFTs using CF$_4$ Plasma

4.1. Introduction

In recent years low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) have attracted considerable interest for their use in active-matrix liquid crystal displays (AMLCDs) since they exhibit good electrical properties and can be integrated in peripheral circuits on inexpensive glass substrates [51]. Since poly-Si thin film transistors (TFTs) require glass substrates, intensive studies have been carried out reducing the crystallization temperature of amorphous silicon (α-Si) films. Ni-metal-induced lateral crystallization (MILC) is one of these efforts. In MILC, Ni islands are selectively deposited on top of α-Si films and allowed to crystallize at a temperature below 600°C [32], [52]. Three stages have been identified in the MILC crystallization process: (1) the formation of $NiSi_2$ precipitates, (2) the nucleation of crystalline silicon (c-Si) on {111} faces of octahedral $NiSi_2$ precipitates, and (3) the subsequent migration of $NiSi_2$ precipitates and crystallization of needlelike Si grain [21].

Unfortunately, the poly-Si grain boundaries trap Ni and $NiSi_2$ precipitates which increase the leakage current and shift the threshold voltage [34], [36], [37], [61], [62]. This problem can be solved using Ni-gettering method [58]. However, the crystal quality of Ni-gettering poly-Si film was poorer than that of conventional MILC poly-Si film. In order to eliminate the trap states of poly-Si film a hydrogen plasma treatment process has been utilized to improve the device performance [63]. However, it was hard to control the hydrogen concentration in the poly-Si film. Besides, the formed Si-H bonds were not strong enough to avoid the hot carrier generation. Recently, fluorine ion (F^+) implantation was employed to improve the electrical performance of MILC TFTs. It was found that fluorine ions effectively minimize the trap state density, leading to superior electrical characteristics and better reliability. However, the minimum off-state currents were nearly unchanged [74]. This might because the Ni concentration was unchanged.

In this section, CF_4 plasma was employed to improve the electrical performance of conventional MILC TFTs. This uncomplicated and effective method involves etching away the top surface of MILC poly-Si and passivating the trap states. The electrical characteristics including I-V measurement, trap-state density (N_t), activation energy (E_A), the density of states (DOS) distribution in the bandgap, and hot carrier stress on on-current degradation $(\Delta I_{on} / I_{on})$ are reported in this work.

4.2. Experiment procedure

The schematic diagram of the fabrication process is illustrated in Fig. 4-1. The process of poly-Si films began with four-inch Si (100) wafer where a 120 nm thick undoped amorphous silicon (α-Si) layer was deposited on a 500 nm thick oxide coated silicon wafer by low pressure chemical vapor deposition (LPCVD) system. The photoresist was patterned to form the desired Ni lines, and a 20-Å-thick Ni film was deposited on the α-Si. Samples were then dipped into an acetone for 5 min to remove the photoresist, and subsequently annealed at 540°C for 18 h to form the MILC poly-Si film. To reduce Ni contamination, the unreacted Ni metal was removed by chemical etching. Samples were subjected to the CF_4 plasma treatment conducted in a plasma enhanced chemical vapor deposition (PECVD) system at 350°C for 1, 3, 6, and 10 min, under a pressure of 100 mTorr and a power of 5 W. Reactive ion etching (RIE) was employed to form poly-Si islands on the wafers. After the RCA-clean process, a 100 nm thick SiH_4/N_2O oxide layer was deposited as the gate insulator by plasma-enhanced chemical vapor deposition (PECVD). Then, a 200-nm-thick poly-Si film was deposited for gate electrodes by LPCVD. After defining the gate, self-aligned 40 KeV P ions were implanted at a dose of 5×10^{15}

cm^{-2} to form the source/drain and gate. The dopant activation was performed at 600°C furnace for 24 h. Followed by a deposition of the passivation layer and a definition of contact holes. A 500-nm-thick Al electrode was deposited and patterned. Finally, the finished MILC poly-Si TFT devices were sintered in a thermal furnace at 350°C for 30 min. It is worthy to note that, the manufacturing processes of CF_4-plasma-etched TFT do not need any additional thermal annealing step and are compatible with conventional MILC TFT processes.

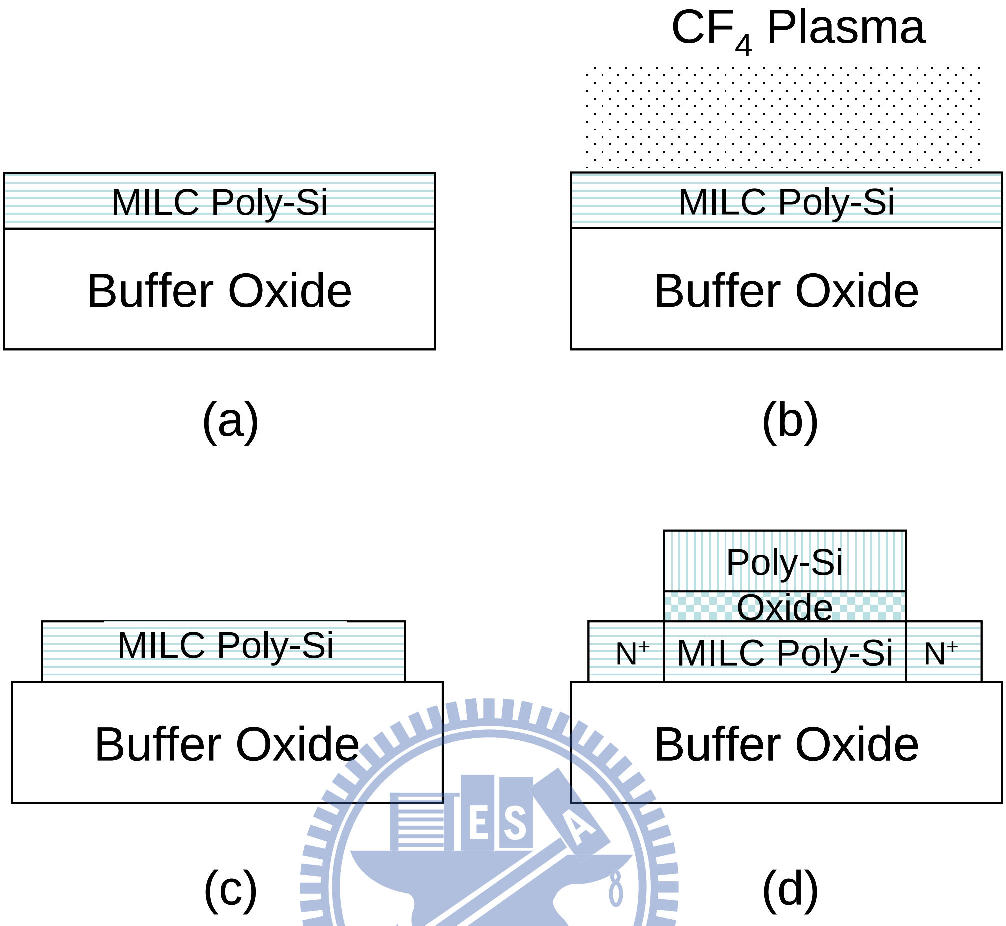

Fig. 4-1 Schematic diagram of the MILC poly-Si TFT by using CF_4 plasma etching treatment.

4.3. Results and discussion

4.3.1. Electrical properties of MILC poly-Si TFTs and CF_4 poly-Si TFTs

Fig. 4-2 shows the transfer characteristics versus the gate voltage of the MILC poly-Si TFTs with and without CF_4 plasma etching treatment. The measured as well as extracted key device parameters are summarized in TABLE 4-1. The field-effect mobility (μ_{FE}) is extracted from the transconductance measurement at V_{DS} = 0.1 V. The threshold voltage

(V_{th}), the subthreshold swing (S.S.), the maximum on-current (I_{on}) and the minimum off-current (I_{off}), were measured at V_{DS} = 5 V. The threshold voltage (V_{TH}) was defined as the gate voltage required to achieve a normalized drain current of $I_{DS} = (W/L) \times 100$ nA at V_{DS} = 5 V.

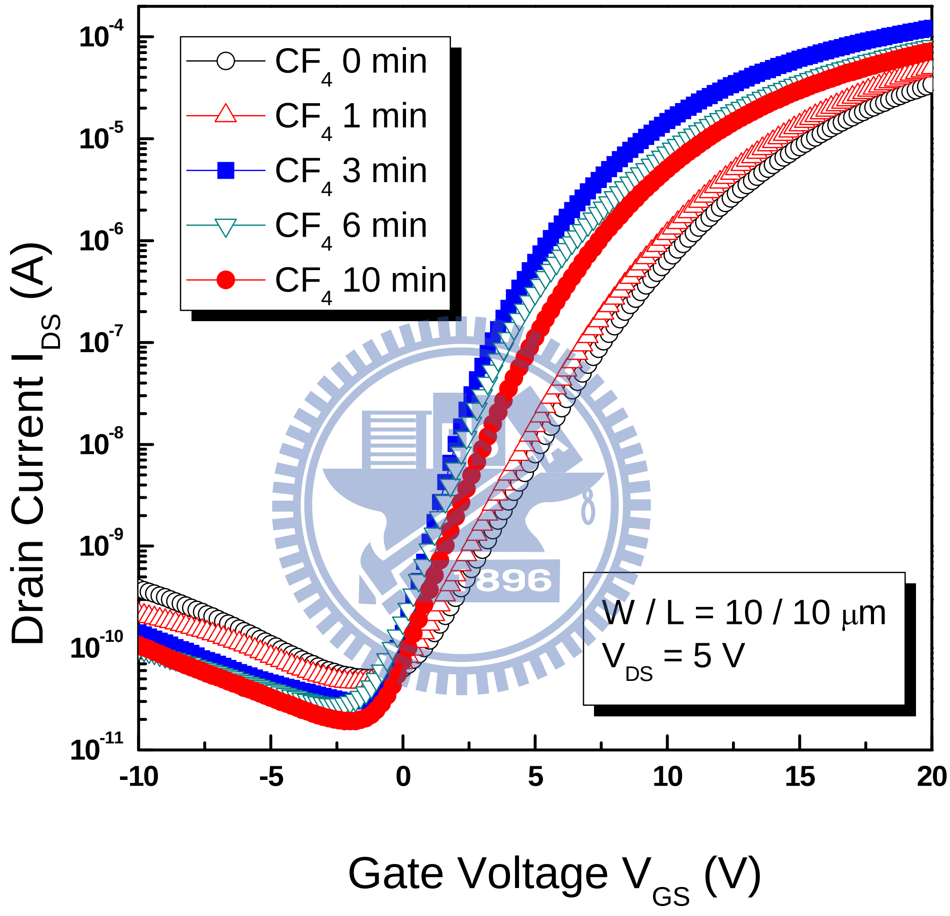

Fig. 4-2 Comparison of transfer characteristics of MILC poly-Si TFTs with and without CF_4 plasma etching treated.

It was found MILC TFTs with CF_4 treatment exhibit better electrical properties than that without CF_4 treated. As shown in TABLE 4-1, the μ_{FE} of the conventional MILC TFTs is

46.6, which is smaller than those of CF_4-plasma-etched TFTs. The V_{TH} of the conventional MILC TFTs is 8.2 V, which is larger than those of CF_4- etched TFTs. The S.S. of the MILC TFTs is 2.08, which is larger than those of plasma-etched TFTs . The I_{on} of the conventional MILC TFTs is 34.1 μA, which is smaller than those of plasma-etched TFTs. All these improvement suggested that CF_4 plasma etching treatment can effectively reduce the trap states, which leads to better device performance.

TABLE 4-1 Device characteristics of the MILC poly-Si TFTs with and without CF_4 plasma treated.

Device Parameters	Convention	CF_4			
	0 min	1 min	3 min	6 min	10 min
Field-Effect Mobility μ_{FE} (cm^2 / V · s)	44.6	59	76.6	60.2	57
Threshold Voltage V_{TH} (V)	8.2	6.9	3.3	4.0	4.9
Subthreshold Slope S.S. (V / dec)	2.08	1.99	1.01	1.23	1.36
On-state Current (10μA)	3.41	5.00	11.23	8.05	7.24
Off-state Current I_{off} (pA)	50.94	46.16	29.86	27.86	19.1
Surface Roughness R_{rms}	0.389	0.412	0.596	0.757	0.858

4.3.2.Influence of CF_4 etching treatment on trap-state density

The measurement of trap state density (N_t) was using Levinson and Proano’s method, which can estimate the N_t from the slope of the linear segment of ln [I_{DS} / (V_{GS}-V_{FB})] vs. 1

/ $(V_{GS}-V_{FB})^2$ at low V_{DS} and high V_{GS}, where V_{FB} is defined as the gate voltage that yields the minimum drain current at V_{DS} = 0.1 V [65], [66]. They were shown in Fig. 4-3 andTABLE 4-1. The N_t of the conventional MILC TFTs is 5.49×10^{12} cm^{-2}, which is larger than those of CF_4-plasma-etched TFTs. The reduction in N_t values implies that those defects have been effectively terminated using CF_4 plasma etching treatment.

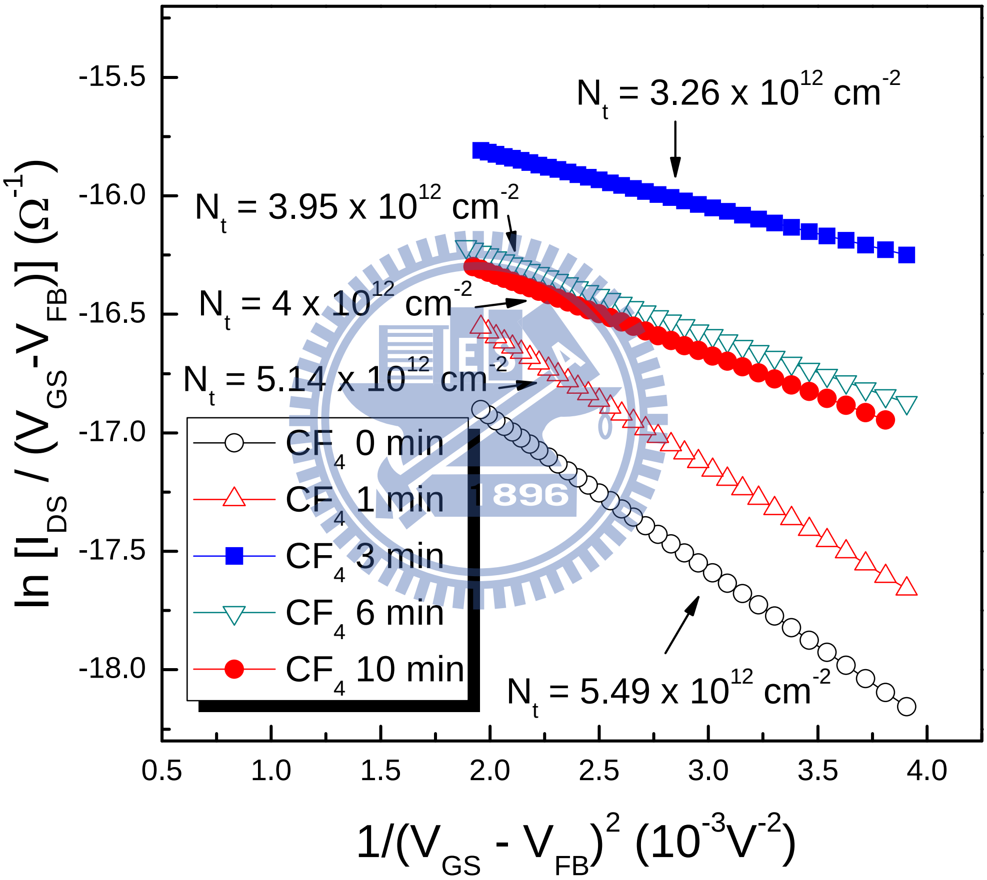

Fig. 4-3 ln $[I_{DS} / (V_{GS}-V_{FB})]$ vs. 1 / $(V_{GS}-V_{FB})^2$ at low V_{DS} and high V_{GS} for with and without CF_4 plasma etching treatment.

In MILC poly-Si, there are two major kinds of defects related to trap states: (1) grain boundary defects and (2) Ni-related defects. These defects would degrade electric performance because they introduced dangling bonds and strain bonds [63], [74]. CF_4 plasma can reduce these defects by (1) passivating the trap states and (2) etching away the MILC poly-Si surface where trapped most Ni-related defects [58]. Ellipsometry analysis revealed when CF_4 plasma etching time increased from 3 to 10 min, the removed thickness of Si increased from 6 to 18 nm. At the same time, it suggested that the top Ni-related defects were etched away during the plasma etching treatment.

4.3.3.SIMS analysis of CF_4 treated poly-Si film

Secondary-ion mass spectroscopy (SIMS) analysis shows high F content present on the top of MILC poly-Si surface, as shown in Fig. 4-4. This suggested that F atoms terminate trap states near the top interface [58]. These observations clearly explain why N_t was reduced after CF_4 plasma etching treatment. As a result, the carrier mobility increases due to the decrease in the scattering by the reduction of Ni-related defects and the passivation of trap states.

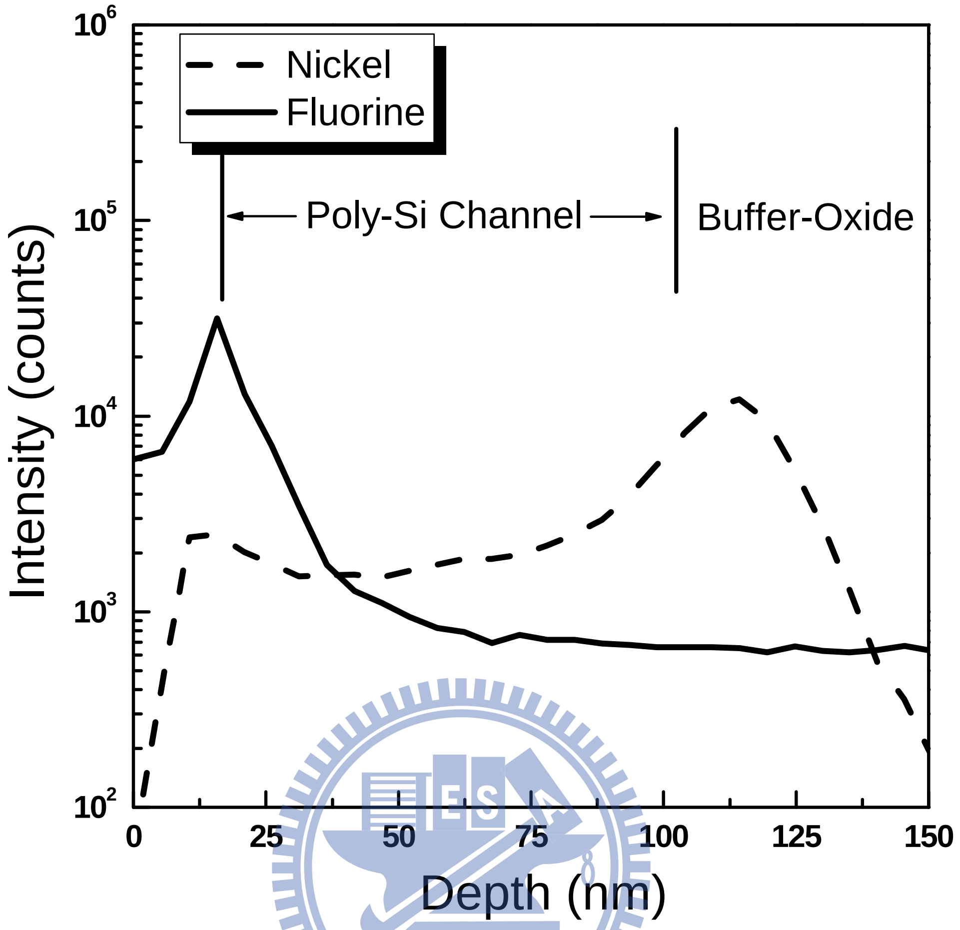

Fig. 4-4 SIMS depth profile of Nickel for the MILC poly-Si films and fluorine for the MILC poly-Si films after CF_4 plasma etching treatment.

4.3.4.Density of states before and after CF_4 plasma treated

The distributions of trap-state density in the forbidden band were calculated by using the field-effect analysis [75]. As shown in Fig. 4-5, compared with those in conventional MILC TFTs, both deep states and tail states are effectively reduced by CF_4 plasma etching treatment. The reduction of deep-state density can explain the improvement of V_{TH} and S.S. These two parameters are strongly influenced by the deep trap state, associated with the dangling bonds, which have energy states near the middle of the silicon band-gap [63]. In other words, CF_4 plasma treatment can effectively terminate the dangling bonds in MILC poly-Si. On the other hand, the reduction of tail-state density can explain the enhancement of the field-effect mobility, which significantly affected by the tail states near the band edge, which resulted from the strain bonds in gate-oxide/MILC poly-Si interface [63]. The reduction of deep states and tail states implies that the CF_4 plasma etching treatment not only terminate the dangling bonds, but also relieve the strain bonds.

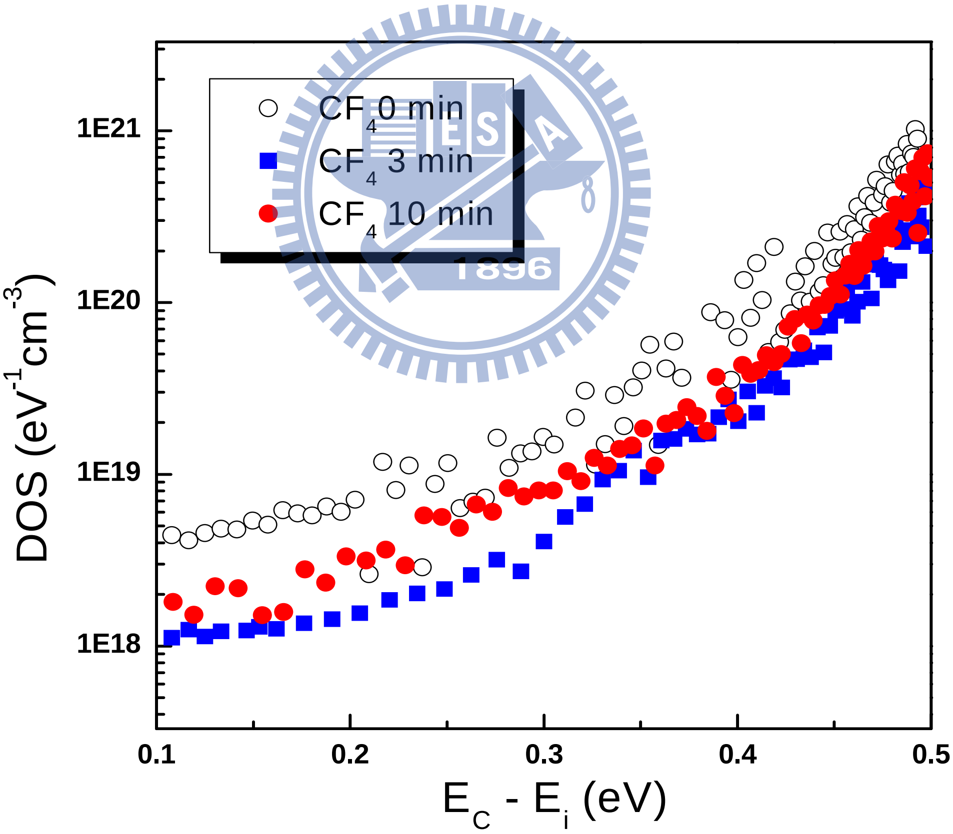

Fig. 4-5 The density of state (DOS) distribution in the bandgap of the MILC poly-Si TFTs with and without CF_4 plasma etching treatment.

4.3.5. Activation energy before and after CF_4 plasma treated

The activation energy (E_A) was also used to investigate the change of trap state. E_A reflects the carrier transportability, which is related to the barrier height in the poly-Si channel. The lower the E_A, the lower of the carrier transport barrier of the trap state. It was obtained by the measurement of transfer characteristics at temperature ranging from 25 to 125℃. From the equation $I_{DS} = I_0 e^{-(Ea/KT)}$, E_A could be extracted from the slope of the linear segment of ln (I_{DS}) vs. 1/KT, in which K is Boltzmann constant and T is the temperature. Fig. 4-6 shows the E_A of drain current as a function of gate voltage measured at V_{DS} = 5 V. Compared with the conventional MILC TFT, the E_A of the CF_4-etched TFTs decreased in the on-state and increased in the off-state. The decreased of E_A in the on-state is because fluorine atoms passivate the trap states and hence reduce the barrier height for the carrier's transport. On the other hand, the increased in the off-state is because the trap-assisted leakage current is suppressed due to the passivation of trap states.

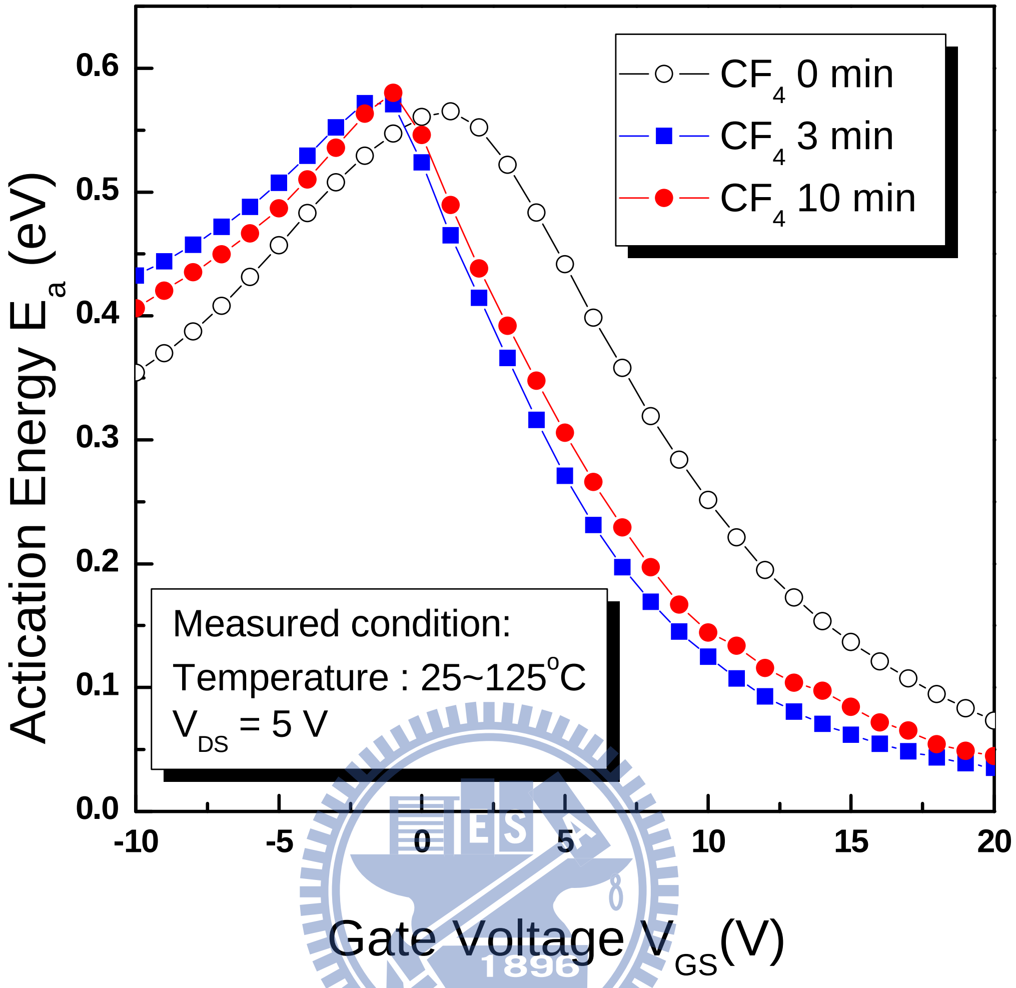

Fig. 4-6 The activation energy (E_A) of the MILC poly-Si TFTs with and without CF_4 plasma etching treatment.

4.3.6.Reliability before and after CF_4 plasma treated

The other important issue of poly-Si TFTs is their reliability, which was examined under hot-carrier stress. As shown in Fig. 4-7, the on-current of TFTs were degraded because dangling bonds are created due to the trapping of electrons at weak Si-Si bonds and Si-H bonds [72], [73]. Compared with those of conventional MILC TFTs, the on-current degradations of CF_4 plasma-treated MILC TFTs are greatly improved by the CF_4 plasma etching treatment. CF_4 plasma-treated TFTs also possess high immunity against the hot-carrier stress and thereby exhibit lower $\Delta I_{ON}/I_{ON}$ than that of conventional MILC TFTs. This is because weaker Si-H and Si-Si bonds were replaced by stronger Si-F bonds [76], [77], which could not be broken under hot-carrier stress, thus leading to improved electrical reliability.

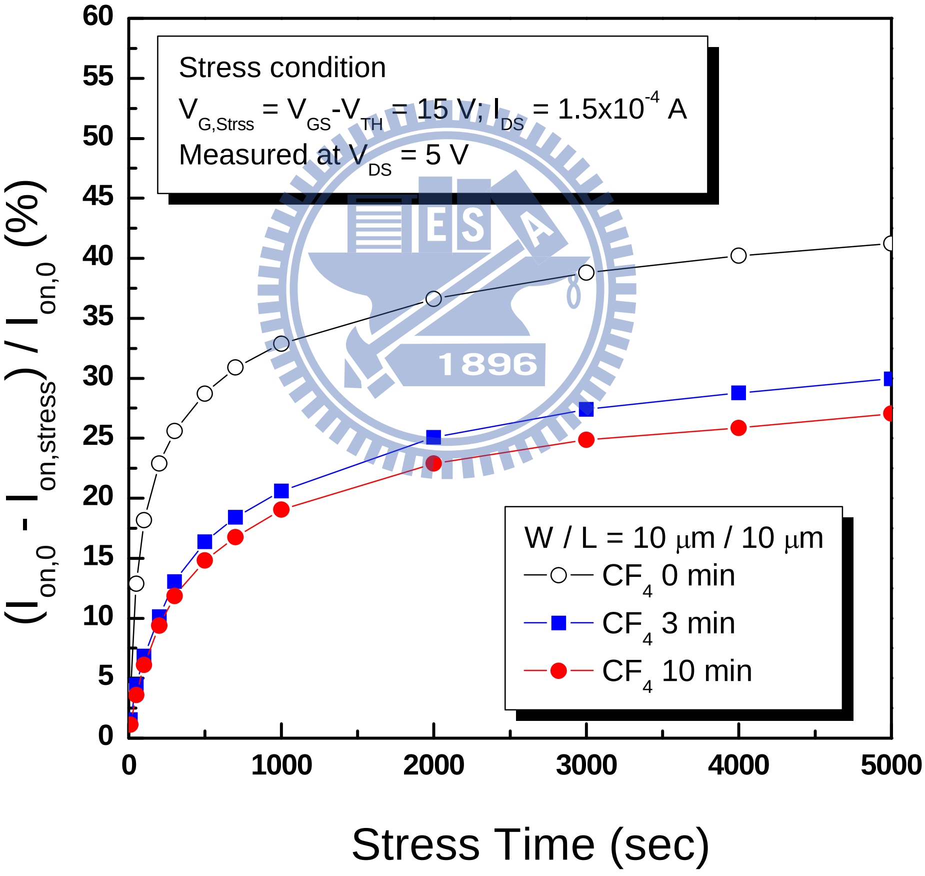

Fig. 4-7 The on-current degradation versus stress time for the MILC poly-Si TFTs with and without CF_4 plasma etching treatment.

4.3.7. AFM analysis before and after CF_4 plasma treated

TABLE 4-1 also indicates the performance of plasma-etched TFTs improved with the plasma-etched time. As the etching time increased from 0 to 1 and 3 min, the μ_{FE} of CF_4-etched TFTs increased from 44.6 to 59.0 and 76.6 cm^2 / V · s. The V_{TH} decreased from 8.2 to 6.9 and 3.3 V. The S.S. decreased from 2.08 to 1.99 and 1.01 V / dec. The I_{on} increased from 34.1 to 50.0 and 112.3μA. However, when etching time reached 6 min, the performance of TFTs degraded. This degradation was mainly due to the the increase of surfaces roughness caused by CF_4 plasma etching.

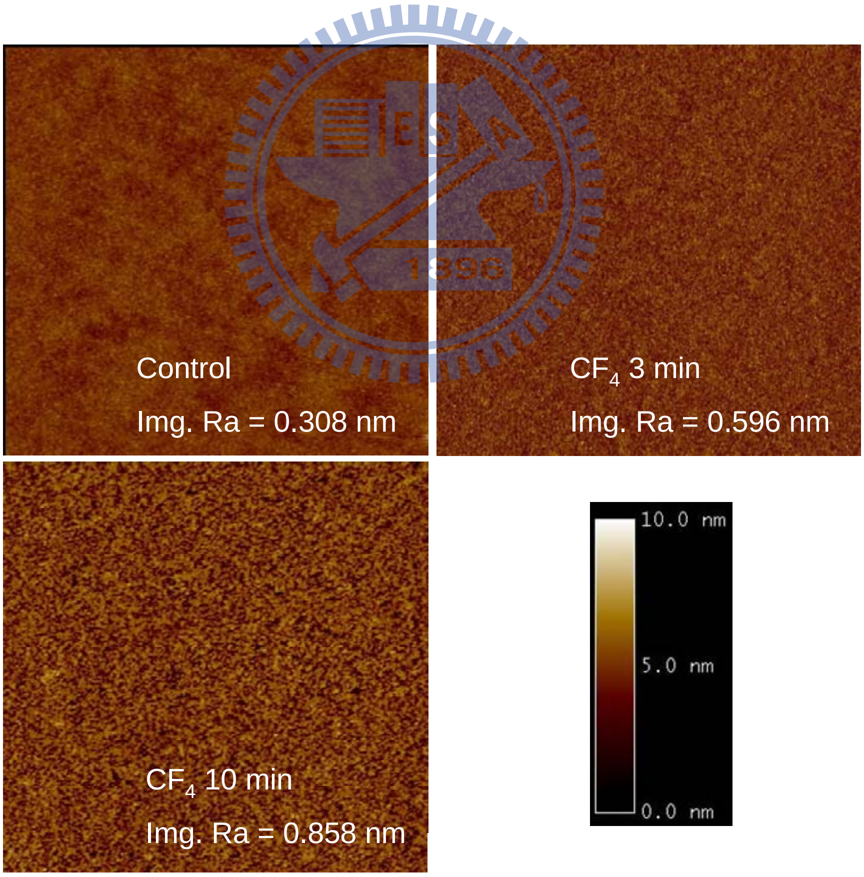

Fig. 4-8 Surface roughness of CF_4 plasma treatment poly-Si film by AFM analysis.

The surface roughness (before gate insulator was deposited) was measured by atomic force microscopy (AFM) as shown in Fig. 4-8. The root mean square (rms) roughness of the MILC surface without CF_4 plasma etching treatment was only 0.389 nm. As shown in TABLE 4-1, when the plasma etching time increased from 1 to 3, 6 and 10 min, the rms roughness increased from 0.412 to 0.596, 0.757 and 0.858 nm, respectively. This increase of surfaces roughness implies that more damages have been made on the MILC channel when plasma etching treated time over 3 min. As a result, when etching time reached 6 min, the device performance decreased. This behavior is consistent with N_t measurement. As shown in TABLE 4-1, N_t decreased with the etching time when etching time less than 3 min. However, when etching time greater than 6 min, N_t increased with the etching time.

4.4. Conclusion

An investigation of the effects of CF_4 plasma etching process on the electrical characteristics and reliability of MILC poly-Si TFTs, has led to the development of a simple, effective process to improve the TFT electrical properties. It was found that CF_4 plasma etching treatment TFT exhibited higher field-effect mobility, superior subthreshold slope, lower threshold voltage, higher ON/OFF current ratio, and lower trap state density (N_t) as compared with typical MILC TFT. It was also found CF_4 plasma etching process can greatly alleviate the on-current degradations under a hot carrier stress. The CF_4

plasma-treated MILC TFT has high immunity against the hot carrier stress and thereby exhibited lower $\Delta I_{ON}/I_{ON}$ as compared with conventional MILC TFT. This is because the weaker Si-H and Si-Si bonds were replaced with stronger Si-F bonds, which were hard to be broken under hot carrier stress and leading to improve the electrical reliability.

Chapter 5

Electrical properties and uniformity of poly-Si thin-film transistors using nickel drive-In induced laterally crystallization

5.1. Introduction

Low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) have attracted considerable interest for their application in active-matrix organic emitting diode displays (AMOLED), since they exhibit good electrical properties and can be integrated in peripheral circuits on inexpensive glass substrates [51]. For the application to AMOLED, the luminance of the OLED material is proportional to the amount of current passing through it. Therefore, pixel to pixel array needs to give uniform currents to the OLED material for the sake of creating uniform light [78].

As LTPS TFTs require glass substrates, intensive studies on reducing the crystallization time and temperature of amorphous silicon (α-Si) films have been carried out.

Ni-metal-induced lateral crystallization (MILC) is one of these efforts. In MILC, Ni islands are selectively deposited on top of α-Si film and allowed to crystallize at a temperature below 600°C [32], [52]. Unfortunately, poly-Si/oxide interfaces and poly-Si grain boundaries trap Ni and $NiSi_2$ precipitates (Ni-related defects), thus degrading uniformity result in increasing leakage current and shifting the threshold voltage [61], [79]. There have been several attempts to reduce the Ni contamination such as metal-induced crystallization of α-Si through a cap layer (MICC) [80], reducing the Ni silicide concentration in the MILC region [81], and Ni-gettering method [58]. However, complexity steps were needed even though they could effectively reduce the Ni contamination.

Recently, fluorine ion (F^+) implantation and CF_4-plasma treatment were employed to improve the electrical performance of MILC TFTs [74], [82]. It was found that fluorine atoms effectively minimize the trap state density, leading to superior electrical characteristics.

In this letter, a novel fabrication process has been developed to reduce the Ni concentration and minimizes the trap-state density of MILC TFTs using nickel drive-in induced laterally crystallization (DILC). The DILC poly-Si was prepared by collision between fluorine ion (F^+) implantation and Ni through the designed pattern into α-Si layer.

5.2. Experiment procedure

The preparation of nickel DILC poly-Si films began with four-inch Si (100) wafer substrates as shown in Fig. 5-1. A 120-nm-thick undoped α-Si layer was deposited onto a 500-nm-thick oxide-coated Si wafer by low pressure chemical vapor deposition (LPCVD) system. A 65-nm-thinck cap-oxide was deposited and patterned to form 20-μm-wide lines, and a 20-Å-thick Ni film was then deposited. Samples were subjected to the fluorine ions (F^+) implantation to form Ni drive-in process. For the α-Si layer under the Ni line, the projection range of F^+ was set at the middle of α-Si layer. At the same time, for the α-Si layer under the oxide layer, the projection range was located at the cap-oxide/α-Si interface. The dosage of F^+ was from 2×10^{12} cm^{-2} to 2×10^{15} cm^{-2}. The ion-accelerating energy was 35 KeV.

The unreacted Ni film and cap-oxide were then removed by chemical etching, and subsequently annealed at 590°C for 3 h to form the DILC poly-Si. The islands of poly-Si regions on the wafer were defined by Reactive ion etching (RIE) with the channels at the lateral growth region, which was ~10 μm away from Ni line and the front of DILC poly-Si grains. After the clean process, a 100-nm-thick gate insulator was deposited by plasma enhanced chemical vapor deposition (PECVD). Then, a 200-nm-thick poly-Si film was deposited for gate electrodes by LPCVD. After defining the gate, self-aligned 40 KeV P ions were implanted at a dose of 5×10^{15} cm^{-2} to form the source/drain and gate. The dopant activation was performed at 600°C furnace for 20 h. Followed by a deposition of the passivation layer and a definition of contact holes. Finally, a 500-nm-thick Al electrode was deposited and patterned. For the purpose of comparison, conventional MILC was prepared without F^+ drive-in process. It is worthy to note that this DILC processes do not need any additional thermal annealing step and are compatible with convention MILC TFT processes.

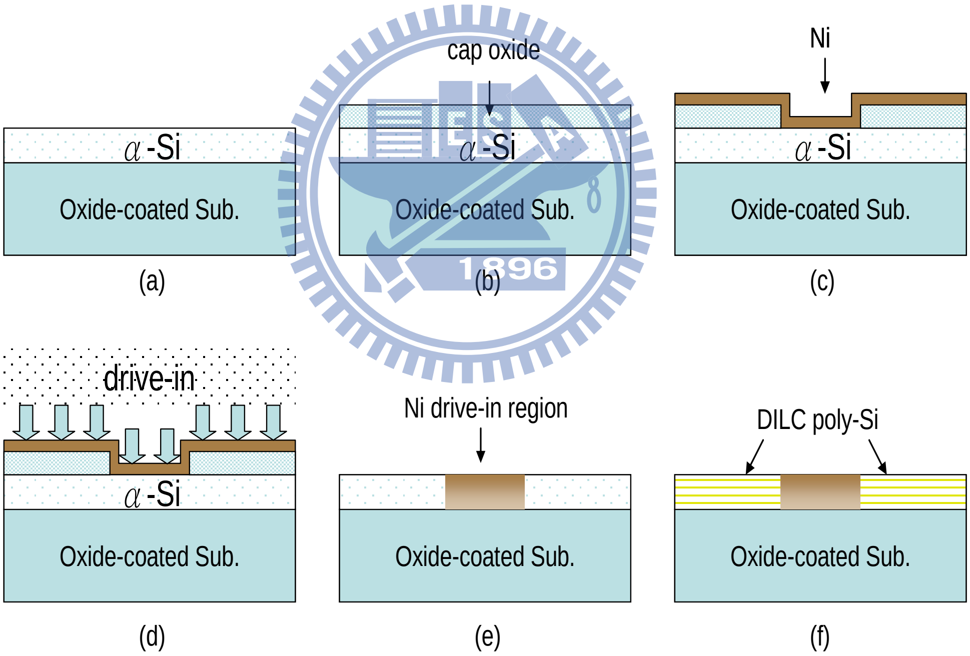

Fig. 5-1 Schematic illustration of DILC poly-Si process: (a) deposition of α-Si on oxide-coated Si wafer, (b) deposition of cap-oxide, (c) deposition of Ni film, (d) fluorine ions (F^+) implantation, (e) removal of unreacted Ni film and cap-oxide layer, (f) and annealing at 590°C for 3 h.

5.3. Results and discussion

5.3.1. The relation between drive-in dosage and lateral crystallization length

Fig. 5-2 shows the average length of MILC and DILC with various drive-in dosages growth perpendicular to the edge of the Ni lines as a function of annealing time at 590℃. The MILC growth length was saturated around 30 μm of annealing time for 2 h. The growth length of DILC with various drive-in dosages was higher than that of MILC. Furthermore, the growth length was without saturated at DILC of annealing time for 2 h. The saturation of MILC length was cause by lateral crystallization, which was stopped by random poly-Si grains resulting from the background solid phase crystallization (SPC) [83]. Moreover, we also found that the increase in drive-in dosages from 2×10^{12} cm^{-2} to 2×10^{15} cm^{-2} increase the saturation length. When the drive-in dosage reached 2×10^{15} cm^{-2}, the growth length increase to 68 μm without saturated. As mentioned previously, the saturation of MILC length was due to the formation of SPC grain. SPC grain exists as an inhibitor of the MILC process [83]. Therefore, the saturation length enhancement of DILC was attributed to the retardation in the nucleation rate in SPC owing to the higher degree of disorder at the cap-oxide/α-Si interface by F^+ implantation [84].

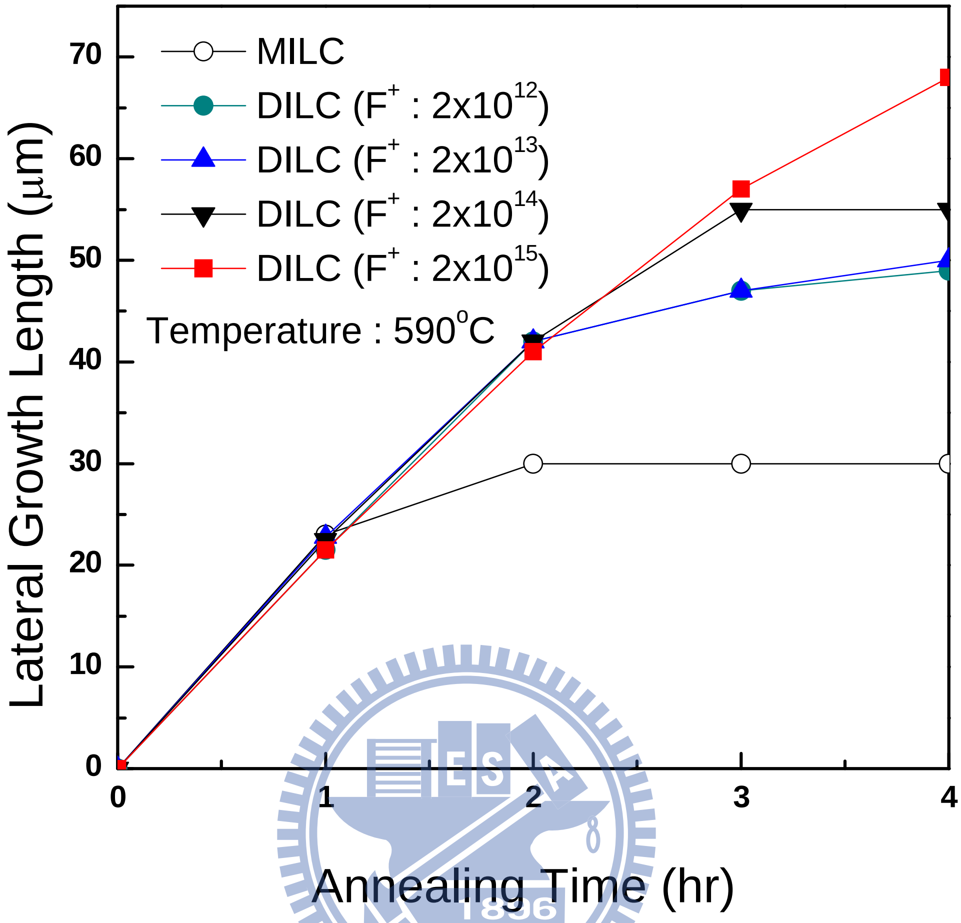

Fig. 5-2 MILC and DILC growth lengths as function of annealing time.

5.3.2.Electrical properties of DILC and MILC TFTs

Fig. 5-3 shows the I_{DS}-V_{GS} transfer characteristics and field-effect mobility (μ_{FE}) of MILC TFTs and DILC TFTs with drive-in dosage greater than 2×10^{14} cm^{-2}. It was found that DILC TFTs have superior electrical characteristics such as high field-effect mobility, low threshold voltage, low subthreshold slope, high on-state current and low off-state leakage current. This indicates the trap state density (N_t) in DILC poly-Si was effectively reduced. The performances of DILC TFTs with dosage less than 2×10^{13} cm^{-2} were not shown in Fig. 3 since their performances were similar to that of MILC TFTs. This might because the F^+ dosage was not high enough.

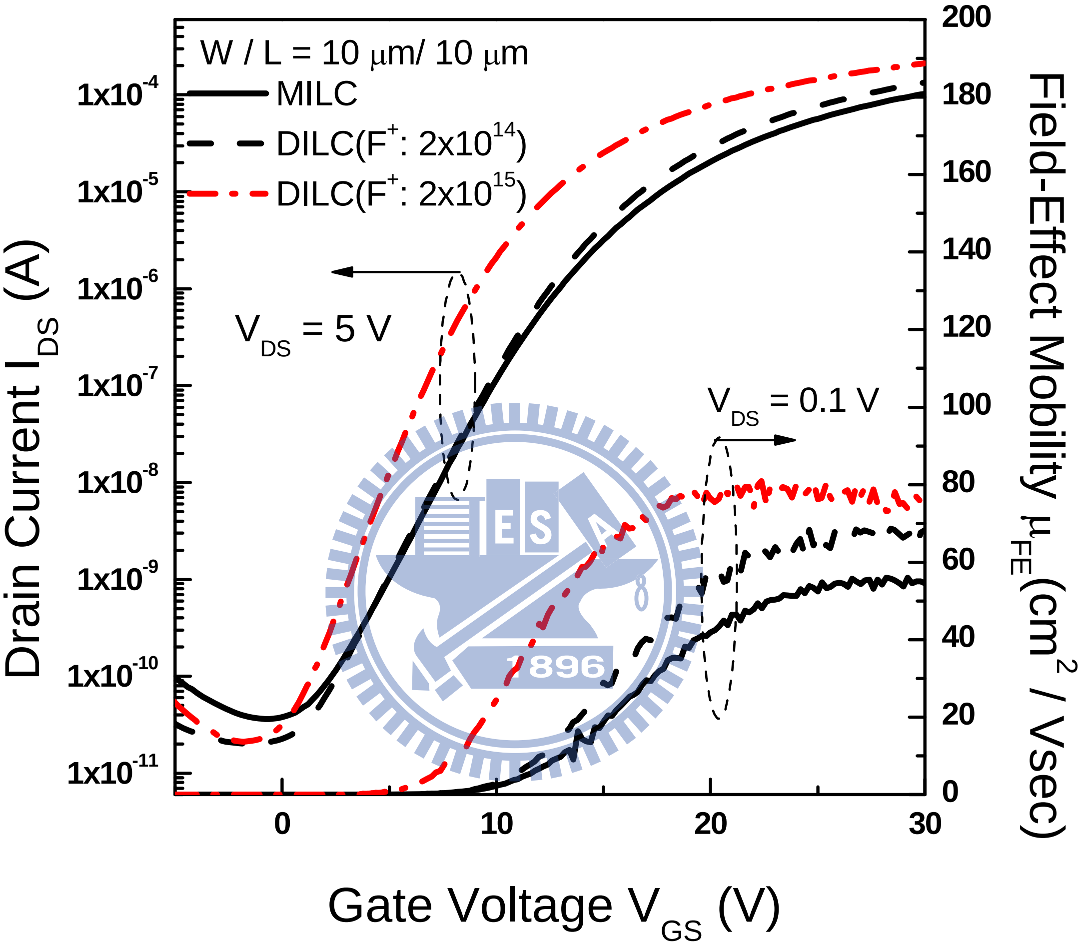

Fig. 5-3 Typical I_{DS}-V_{GS} transfer characteristics and filed-effect mobility of MILC TFTs and DILC TFTs with various F^+ dosages.

5.3.3.Influence of nickel drive-in by F^+ implantation on trap-state density

In MILC poly-Si, there are two major kinds of defects related to N_t: (1) grain boundary defects and (2) Ni-related defects. These defects would degrade electric performance because they introduced dangling bonds and strain bonds [74], [82]. The trap state density of the TFTs was extracted using Levinson and Proano's method, which can estimate the N_t from the slope of the linear segment of ln $[I_{DS} / (V_{GS}-V_{FB})]$ vs. $1 / (V_{GS}-V_{FB})^2$ at low V_{DS} and high V_{GS}, where V_{FB} is defined as the gate voltage that yields the minimum drain current at $V_{DS} = 0.1$ [65], [66]. As the F^+ dosage increased from 0 (MILC) to 2×10^{14} and 2×10^{15} cm^{-2}, the trap density decrease from 5.95×10^{12} to 5.78×10^{12} and 4.58×10^{12} cm^{-2}, respectively.

The reduction in N_t values implies that those defects have been terminated in DILC poly-Si. Secondary-ion mass spectroscopy (SIMS) was used to study the distribution of F atom. As shown in Fig. 5-4, the F content in DILC increased with F dosage, as expected. Besides, high F contents were found at the DILC poly-Si/buffer-oxide interface. In other words, F ions have diffused to the interface/boundaries to terminate Ni-related trap states [74]. This observation suggested that drive-in F atoms effectively reduce trap-state density in the DILC poly-Si film, and lead to improve electrical characteristics.

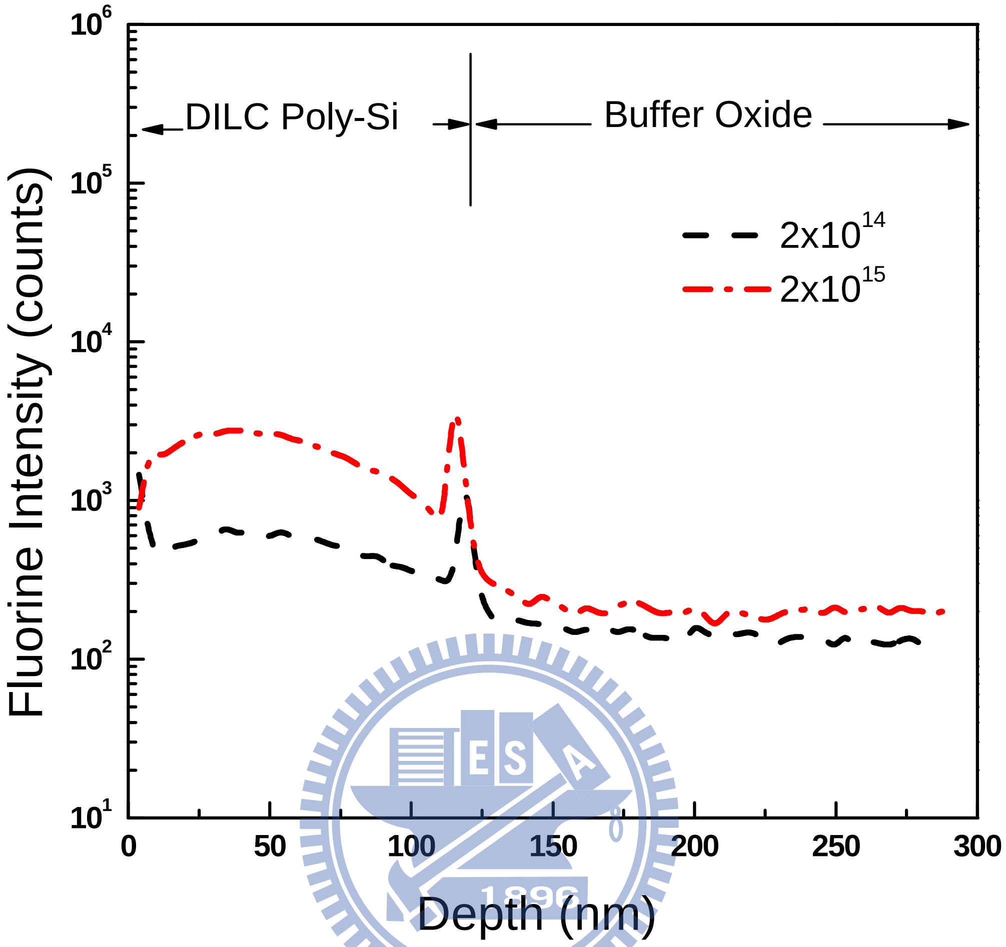

Fig. 5-4 SIMS depth profile of fluorine in the structure of interface of DILC poly-Si/buffer oxide film after annealing at 590℃ for 3 hr.

5.3.4.Uniformity of DILC and MILC TFTs

The other important issue of poly-Si TFTs is their uniformity for the AMOLED application. As showed in TABLE 5-1, the device parameters were extracted at *W* / *L* = 10/10 μm, and ten TFTs were measured in each case to investigate the device-to-device variation. The threshold voltage (V_{th}) was defined as the gate voltage required to achieve a normalized drain current of $I_{DS} = (W / L) \times 100$ nA at $V_{DS} = 5$ V. The subthreshold slope (S.S.), the on-state current (I_{ON}) and the off-state leakage current (I_{OFF}) were measured at V_{DS} =5 V, while the field-effect mobility (μ_{FE}) was measured at V_{DS} =0.1 V. As showed in TABLE 5-1, the standard deviations of DILC TFTs were smaller than that of MILC TFTs. In other words, the uniformity of MILC TFTs was improved through DILC process. This improvement was also due to the reduction of Ni concentration and the suppression of SPC nucleation.

TABLE 5-1 Average values of the field-effect mobility, threshold voltage, subthreshold slope, on-state current and off-state leakage current of TFTs with standard deviations in parentheses.

Device Parameters	MILC	DILC	
W/L=10μm /10μm		2×10^{14}	2×10^{15}
Field-Effect Mobility μ_{FE} (cm^2 / V · s)	56.11 (12.59)	69.68 (3.14)	79.92 (7.11)
Threshold Voltage V_{TH} (V)	9.72 (0.72)	9.66 (0.25)	6.76 (0.21)
Subthreshold Slope S.S. (V / dec)	2.32 (0.22)	2.26 (0.08)	1.66 (0.69)
On-state Current I_{ON} (10^5 A)	10.40 (3.17)	13.52 (0.99)	20.52 (2.57)
Off-state Leakage Current I_{OFF} (pA / μm)	3.85 (0.71)	2.03 (0.05)	2.20 (0.06)

5.4. Conclusion

An investigation of poly-Si TFTs using Ni drive-in induced laterally crystallization (DILC) had led to the development of a suitable process for AMOLED manufacturing. The DILC poly-Si was prepared by collision between fluorine ion implantation and Ni film through the designed pattern into α-Si layer. After annealing at 590°C, it was found that DILC saturation lengths and TFT performance were increased with the drive-in dosage. This is because drive-in F atoms effectively suppress the nucleation of SPC grain and reduce trap-state density in the DILC poly-Si film. As a result, DILC TFTs exhibit high field-effect mobility, low threshold voltage, low subthreshold slope, high on-state current, low off-state leakage current, lower trap state density (N_t), and smaller standard deviations compared with conventional MILC TFTs.

Chapter 6

Conclusions and future works

6.1. Conclusions

This thesis studies a number of techniques for the fabrication of high performance low temperature processed poly-Si TFTs (LTPS-TFTs), including the MILC-Si films irradiated by CW laser process (MILCLC), fluorine ion implantation MILC TFTs, CF_4 plasma etching treatment MILC TFTs, and nickel drive-in lateral crystallization (DILC) technique.

In chapter 2, to improved uniformity and electrical performance of CLC-TFTs, two kinds of Si films (α-Si and MILC-Si) were used in this study. After irradiated by CW laser of various output powers (2.5 W, 3.8 W and 5 W), it was found that the performance and uniformity of MILCLC-TFTs were better than those of CLC-TFTs. When the laser output power was low (2.5 W), both films were in the SPC region. Only some of the α-Si regions were melted. The electrical characteristics of CLC-2.5 and MILCLC-2.5 were poor. When the laser output power reached 5.0W, CLC-5.0 and MILCLC-5.0 were in the completely melted region. They both showed excellent performance. Unfortunately, the uniformity was poor because they contained two kinds of grains: ELC poly-Si-like grains and very large directional grains. When the laser output power was median (3.8 W), CLC-3.8 and

MILCLC-3.8 were in the partially melted region with large ELC poly-Si-like grains. The performance and uniformity of MILCLC-3.8 were much better than those of CLC-3.8. This is because the width of the MILCLC-3.8 grains increased dramatically due to the geometrical coalescence of MILC-Si needle grains. Moreover, the uniformity of MILCLC-3.8 was far superior to that of CLC-5.0 and MILCLC-5.0, and therefore was suitable for SOP application.

In chapter 3, the effect of the F^+ implantation on the electrical characteristics and reliability of MILC poly-Si TFTs was investigated. The fluorine ion accelerating energy was 30 KeV. After annealing at 600°C for 24 h, it was found that F^+-implanted TFT exhibited higher field-effect mobility, superior subthreshold slope, lower threshold voltage, higher ON/OFF current ratio, and lower trap state density (N_t) as compared with typical MILC TFT. It was also found F^+ implantation process can greatly improve the electrical reliability under a hot-carrier stress. This is because weaker Si-H and Si-Si bonds were replaced by stronger Si-F bonds. As a result, F^+-implanted TFTs possessed high immunity against the hot-carrier stress and thereby exhibit lower ΔV_{TH} than that of typical MILC TFTs.

In chapter 4, an investigation of the effects of CF_4 plasma etching process on the electrical characteristics and reliability of MILC poly-Si TFTs, has led to the development of a simple, effective process to improve the TFT electrical properties. It was found that CF_4 plasma etching treatment TFT exhibited higher field-effect mobility, superior subthreshold slope, lower threshold voltage, higher ON/OFF current ratio, and lower trap state density (N_t) as compared with typical MILC TFT. It was also found CF_4 plasma etching process can greatly alleviate the on-current degradations under a hot carrier stress. The CF_4 plasma-treated MILC TFT has high immunity against the hot carrier stress and thereby exhibited lower $\Delta I_{ON}/I_{ON}$ as compared with conventional MILC TFT. This is because the weaker Si-H and Si-Si bonds were replaced with stronger Si-F bonds, which were hard to be broken under hot carrier stress and leading to improve the electrical reliability.

In chapter 5, an investigation of poly-Si TFTs using Ni drive-in induced laterally crystallization (DILC) had led to the development of a suitable process for AMOLED manufacturing. The DILC poly-Si was prepared by collision between fluorine ion implantation and Ni film through the designed pattern into α-Si layer. After annealing at 590°C, it was found that DILC saturation lengths and TFT performance were increased with the drive-in dosage. This is because drive-in F atoms effectively suppress the nucleation of SPC grain and reduce trap-state density in the DILC poly-Si film. As a result, DILC TFTs exhibit high field-effect mobility, low threshold voltage, low subthreshold slope, high on-state current, low off-state leakage current, lower trap state density (N_t), and smaller standard deviations compared with conventional MILC TFTs.

6.2. Future works

According to the results in this thesis, there are some interesting topics that are valuable for the future research:

6.2.1. Fluorine ion implantation into the buffer-oxide layer of MILC TFTs

The results of fluorine ion effectively reduce trap-state densities and improve electrical properties were demonstrated by implantation into the middle of channel through the surface of MILC film and CF_4 plasma etching the surface of MILC film, however, the higher fluorine concentration and surface roughness were degraded electrical properties and reliability. Therefore, to develop a suitable concentration of fluorine into the MILC channel and undamaged MILC channel were required. Fluorine ion implantation into the buffer-oxide to form FSG layer can be control the fluorine concentration and without induce surface roughness.

6.2.2. Nickel drive-in induce crystallization TFTs

The Ni contamination within the MILC poly-Si films can degrade the performance and reliability of TFT. In this study, poly-Si TFTs using Ni drive-in induced laterally crystallization (DILC) had led to the development of a suitable process for AMOLED manufacturing. The DILC poly-Si was prepared by collision between fluorine ion implantation and Ni film through the designed pattern into α-Si layer after annealing at 590°C for 3 hr. To consider the production cost and yield, must to decrease the fabrication processes. One of the solutions is to combine the crystallization with activation process at the same time. Another way is to develop nickel drive-in induced crystallization to reduce fabrication process.

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鎳金屬誘發側向結晶複晶矽薄膜電晶體中電特性、可靠度與均勻性課題之研究

Investigation of Electrical Properties, Reliability and Uniformity Issues in Metal-Induced Lateral Crystallization Poly-Si TFTs

Publication list

Journal Paper

1. **Chih-Pang Chang** and Y. S. Wu, "Improved Electrical Characteristics and Reliability of MILC Poly-Si TFTs Using Fluorine Ion implantation," *IEEE Elec. Device Lett*. 28 (2007) PP990-992.
2. **Chih-Pang Chang** and Y. S. Wu "Improved Uniformity and Electrical Performance of Continuous-Wave Laser Crystallized TFTs Using Metal-Induced Laterally Crystallized Si Film, “*J. Elect. Mater*. 37(2008), No11, PP. 1653-56
3. **Chih-Pang Chang** and Y. S. Wu "High Performance Poly-Si TFTs Fabricated by Continuous-Wave Laser Annealing of Metal-Induced Lateral Crystallized Silicon Films," *IET Elect. Lett*. 44(2008), No 19, PP1157-58.
4. **Chih-Pang Chang** and Y. S. Wu, "Improved Electrical Performance of MILC Poly-Si TFTs Using CF_4 Plasma by Etching Surface of Channel," *IEEE Elec. Device Lett.* 30 (2009) No 2, 130-132.
5. **Chih-Pang Chang** and Y. S. Wu, "Improved Electrical Performance and Uniformity of Metal-Induced Lateral Crystallization Polycrystalline Silicon Thin Film Transistors Using Nickel Drive-in Induced Lateral Crystallization," submitted to *IEEE Elec. Device Lett.*.
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Conference Paper

1. **Chih-Pang Chang**, YewChung Sermon Wu, Meiyi Li, Tzu-Ming Yang, Hung-Yu Wu “Etching Effect of Electrical and Reliability of Metal-Induced Lateral Crystallization Polysilicon Thin Flim Transistors by CF_4 Plasma”, in *Symp. On Nano Device Technol.*, 2009.
2. **Chih-Pang Chang**, Y. S. Wu, C. Chen and M. Lai “Etching Treatment of MILC Poly-Si TFTs Using CF_4 Plasma to Improve Electrical Performance”, Thin Film Transistors 9, Honolulu, Hawaii, USA, October, 2008 .(oral presentation)
3. Y. S. Wu and **Chih-Pang Chang** “Improved Electrical Characteristics of MILC Poly-Si TFTs Using Fluorine Ion implanation” Thin Film Materials, Processes, and

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4. YewChung Sermon Wu, **Chih-Pang Chang** and Ching-Chieh Tseng “High Performance of MILC Poly-Si TFTs Using Fluorine Ion implantation” 材料年會, 11月, 2007年

Patent:

1. **張志榜**，吳耀銓，“利用氟離子形成金屬誘發結晶的製作方法”，中華民國專利(申請中）
2. **張志榜**，吳耀銓，“利用電漿改善金屬誘發側向結晶層特性的方法” ，中華民國專利(申請中）