國立交通大學

機械工程系

博士論文

驅動壓電式材料之多級放大電路架構研究

Multi-Level Amplifier for Driving Piezoelectric Loads

研究生：童永成

指導教授：成維華　教授

中華民國九十七年七月

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研 究 生：童永成　　Student：Yung-Cheng Tung

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國 立 交 通 大 學

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(英文) Multi-level Amplifier for Driving Piezoelectric Loads

合於博士資格水準、業經本委員會評審認可。

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驅動壓電式材料之多級放大電路架構研究

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摘要

本研究提出一多級式放大電路架構用以驅動壓電式負載，此放大器利用多級浮動訊號模組的疊加，產生一高電壓增益的輸出。文中首先介紹壓電式負載放大器電路的特性以及研究方法，隨後藉由多級式放大電路架構的分析及模擬，來探討此電路模型的可行性。此多級式放大電路系統，各級供應相同的輸出電壓以及電流，系統總功率消耗平均分配至各級電路當中，以致於多級式放大電路擁有高功率輸出的特點。文中提出一由六級浮動訊號模組所組成的電路原型，用以實現高輸入頻率以及不同電容式負載下的精密線性操作。其頻寬約為 100 KHz、並可在 400V 的輸出擺幅下驅動 0.1μF 的電容式負載；電路的迴轉率(Slew Rate) 高達 115 V/μs，最大輸出電流為±2.6 A。

Multi-level Amplifier for Driving Piezoelectric Loads

Student : Yung-Cheng Tung Advisor : Dr. Wei-Hua CHieng

Department of Mechanical Engineering

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Abstract

This study proposes a multi-level amplifier with connecting floating signal modules in series to drive piezoelectric devices. The amplifier generates a high voltage gain by summing the individual module gains. In the first instance this literature introduces the characteristic and various researching methods of driving piezoelectric loadings. Then the feasibility of multi-level amplifier topology will be discussed by simulations and analyses. Multi-level amplifier provides a means of achieving high power, and can divide the total power dissipation among the modules, because each module delivers the same output voltage and current. A prototype circuit that consists of six floating signal modules exhibits precise linear operation over a wide range of input frequencies and capacitive loads. The circuit provides a 400V output swing with a corner frequency of around 100 kHz at a driving capacitive load of 0.1 μF. The slew rate is as high as 115 V/μs and the maximum output current is ±2.6 A.

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Nomenclature

$A_{o,d}$, $A_{o,cm}$ = Open-loop differential mode gain and common mode gain, respectively

$A_{CL,d}$, $A_{CL,cm}$ = Close-loop differential mode gain and common mode gain, respectively

$A_{iso,d}$, $A_{iso,cm}$ = Differential and common mode gain of the isolation amplifier, respectively

C_L = Capacitive load

f_{max} = The maximum operational frequency of piezoelectric actuator

f_0 = Resonant frequency of unload actuator

i = The i^{th} level of multi-level amplifier

$I_L(s)$ = Load current of current amplifier in s domain

$I_{LC}(s)$ = Actual Current follow through the load capacitor of current amplifier in s domain

k_T = Piezoelectric actuator stiffness

m_{eff} = Efficient mass applied to the actuator

P_{max} = The maximum peak power delivered to loads

$\dot{q}_L, q_L$ = The applied charge to piezoelectric load and its differentiation in s domain

R_L = Resistive load

R_o = Open-loop output resistance of the amplifier

R_s = Isolation resistance / Sensing resistor used in current amplifier

V_+, V_- = Voltages at the non-inverting and inverting input terminals of the amplifier, respectively

V_b = Reference / Biased ground potential of the floating signal module

$V_{in,d}$, $V_{in,cm}$ = Differential mode and common mode input voltages, respectively

V_{max} = The maximum output voltage swing of amplifier

V_{P-P} = Peak to peak driving voltage of piezoelectric actuator

$V^{+}_{out,iso}$, $V^{-}_{out,iso}$ = Positive and negative differential output voltages of the isolation amplifier, respectively

$V_{out,p}$, $V_{out,n}$ = Output voltages of the floating signal module at non-inverting and inverting terminals, respectively

$V_{ref}(s)$ = Reference voltage of current amplifier in s domain

$Z_{CL,o}$ = Close-loop output impedance of the amplifier

$A_{o,d}(s)$ = Frequency response of the open-loop differential mode gain

$A_{o,d}(0)$ = Differential mode gain at low frequency

ω_c = Cut-off frequency

$\omega_{o,d}$ = Dominant pole frequency of the amplifier

ω_n = Natural frequency of the system

ξ = Damping ratio of the system

Chapter 1 Introduction

1.1 General Introduction

Piezoelectric devices or actuators have been used as positioners or driving motors in many fields such as optics, precision machining and fluid control as well as in optical disk drives, because they offer compactness, high energy density, rapid response and controllable displacement down to nanometers or less. The advantages that piezoelectric actuators offer are the absence of friction that exists in other actuators [1]. This dissertation introduces and proposes a novel circuit concept of driving piezoelectric actuators and two circuit topologies derived from this conception. At the beginning of this dissertation, the characteristic and principle of piezoelectric actuator will be introduced. Two fundamental sorts of driving amplifier, current/charge amplifier and voltage amplifier, and control methods will be introduced in section 1.3, 1.4 and 1.5.

1.2 Characteristics and Principles of Piezoelectric Actuators

The main characteristics of piezoelectric actuators are : extremely high resolution in the nanometer range, high bandwidth up to several kilohertz range, a large force up to a few tons, and very short travel in the sub-millimeter range [2]. Application areas of piezoelectric actuators include: micromanipulation, micro-assembly, add-ons for high-precision cutting machinery and as secondary actuators in macro/micro-motion systems such as dual-stage hard-disk drives. Such actuators are assembled from thin, laminar wafers of ceramic material, electrically connected in parallel. Increasing the voltage increases the length of the stack to a maximum strain for typical maximum input voltage. The applied voltage depends on the thickness of the ceramic and on its material properties. It typically ranges from a few tens of volts to a few hundred volts. The reactive powers induced by the highly capacitive characteristics of the actuators will

detrimentally affect the driving amplifiers [3].

As discussed in [3] and references therein, a piezoelectric actuator behaves as a capacitor when operated well below the resonant frequency. Piezoelectric stack actuators are assembled with thin, laminar wafers of electro-active ceramic material electrically connected in parallel. The equivalent capacitance of piezoelectric stack actuator is N times the capacitance of single layer. And the resonant frequency of piezoelectric stack actuators can be described as

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{k_T}{m_{eff}}}, \tag{1.1}$$

where f_0 [Hz] is the resonant frequency of unloaded actuator, k_T [N/m] is the piezoelectric actuator stiffness and m_{eff} [Kg] is the efficient mass applied to the actuator. The stiffness of a solid body depends on Young's modulus of the material. Stiffness is normally expressed in terms of the spring constant k_T, which describes the deformation of the body in response to an external force. Then the capacitance of actuator increases as the number of layer or the electrode surface area increases, a reasonable consideration is that the mass of actuator will also increase. This increasing mass will decrease the resonant frequency of actuator as eq. (1.1) under the condition that they have the same stiffness. So this is why all the product catalogs [3], [4] provided by manufacturers of the piezoelectric stack actuator show a trend that the lager capacitance actuator have a less resonant frequency, as shown in Table-1.1. The capacitance varies from tens nano–farad to tens micro-farad, and the resonant frequency from hundreds kHz to tens kHz.

Piezoelectric stack actuators are applied in many areas, like fiber optics, stabilizing mechanical arrangements, and kilo-hertz scanning and micro-positioning. From the view of application, most of them are operated in

the positioning modes, that piezoelectric actuators are operated well below their resonant frequencies. To sum up that be mentioned above, alternative application of piezoelectric stack actuator is high frequency with low capacitance or low frequency with high capacitance.

And then from the view of power, the delivered peak power [3] , $P_{\max}$, to load for sinusoidal operation is

$$P_{\max} \approx \pi C V_{\max} V_{p-p} f_{\max}, \tag{1.2}$$

where C is the capacitance of piezoelectric stack actuator, $V_{\max}$ is the maximum output voltage swing of amplifier, V_{p-p} is the peak to peak drive voltage and $f_{\max}$ is the operational frequency.

1.3 Driving in Current / Charge Amplifier

Several approaches of driving circuit topology have been proposed to reduce the inherent hysteretic nonlinearity by driving piezoelectric actuators with charge or current, rather than voltage [5]-[8]. As mentioned in [5] and referred therein, piezoelectric ceramics are ferroelectric materials and for this reason they are fundamentally nonlinear in their response to applied electric fields, showing hysteresis and also time-dependent creep. Such effects become increasingly noticeable the higher the electric field strength and the higher the piezoelectric sensitivity of the material. C. V. Newcomb et al. in 1982 [5] found that if the extension of such an actuator is plotted as a function of applied charge rather than applied voltage, hysteresis and creep virtually disappear and the characteristic becomes much more linear. Therefore, C. V. Newcomb et al. proposed charge drive for piezoelectric ceramic actuators as a means of improving their behavior as Fig. 1.1 shows.

As discussed in [6], [7] and references therein, a simplified current amplifier

had been proposed as Fig. 1.2. In the Laplace domain, at frequencies well within the bandwidth of the control loop, the load current $I_L(s)$ is equal to $V_{ref}(s)/Z_S(s)$. If $Z_S(s)$ is a resistor R_S,

$$I_L(s) = V_{ref}(s)/R_s \tag{1.3}$$

i.e., we have a current amplifier with gain $1/R_S$ *A/V*. If $Z_S(s)$ is a capacitor C_S,

$$\dot{q}_L = I_L(s) = V_{ref}(s)C_s s \tag{1.4}$$

$$q_L = V_{ref}(s)C_s \tag{1.5}$$

i.e., we have a charge amplifier with gain C_S Columbs/V.

The foremost difficulty in employing such devices to drive highly capacitive loads is that of DC current or charge offsets. Inevitably, the voltage measured across the sensing impedance will contain a non-zero voltage offset; this and other sources of voltage or current offset in the circuit will result in a net output offset current or charge. As a capacitor integrates DC current, the uncontrolled output voltage will tend towards infinity and saturate at the power supply rails. Any offset in v_o limits the compliance range of the current source and will eventually cause saturation. To limit the DC impedance of the load, i.e., limiting the DC compliance offset for a certain output offset current, a parallel resistance is often used. With $Z_L(s) = \frac{1}{C_L s} \| R_L$, the actual current $I_{LC}(s)$ following through the load capacitor is now,

$$I_{LC}(s) = I_L(s)\frac{s}{s + \frac{1}{R_L C_L}} \tag{1.6}$$

Additional dynamics have been added to the current source, the transfer function now contains a high-pass filter with cutoff $\omega_c = \frac{1}{R_L C_L}$. That is,

$$\frac{I_{LC}(s)}{V_{ref}(s)} = \frac{1}{R_s} \frac{s}{s + \frac{1}{R_L C_L}} \tag{1.7}$$

In contrast to the infinite DC impedance of a purely capacitive load, the load impedance now flattens out towards DC at $\omega_c = 1/R_L C_L$, and has a DC impedance of R_L. Thus, a DC offset current of i_{dc} results in a compliance offset of $v_{dc} = i_{dc} R_L$. In a typical piezoelectric driving scenario, with C_L= 100nF, and $i_{dc} = 1\mu A$, a 1MΩ parallel resistance is required to limit the DC compliance offset to 1 V. Refer to Eq. (1.7), phase lead exceeds 5 degrees below 18 Hz. Such poor low frequency response precludes the use of current amplifiers in applications requiring accurate low frequency tracking.

The compliance feedback current amplifier [6], [7] and another driving method [8] proposed by A. J. Fleming et al. discussed mainly how to estimate the DC offsets and a perfect result had been verified. As Fig. 1.3 shows, a compliance feedback current amplifier had been presented which is modified from the traditional structure of the current amplifier in Fig. 1.2, and consists of three stages - the differential input stage, the transconductance stage, and the output current stage. With such compliance feedback, current amplifier can efficiently estimate the DC offset and achieve excellent ultra-low frequency tracking upto 100 mHz. For high power current and charge amplifier, A. J. Fleming et al. suggested that the output stage be replaced with a PWM inverter, but a PWM controlled DC-AC inverter will limit the high frequency bandwidth of the amplifier, thus the output signal contains switching noise and current ripple.

Due to the uncontrolled nature of the output voltage, circuit offsets generally result in the load capacitor being charged up. Saturation and distortion occur when the output voltage reaches the power supply rails. The stated

complexity invariably refers to additional circuitry required to avoid charging of the capacitor. Another popular scheme is to short the loading circuit, or periodically discharge the loading capacitance and reset the DC voltage to ground during handling [9], [10]. The resulting loads induce undesirable high-frequency disturbance and considerably distort the control signal that is applied to the piezoelectric load.

K. Furutani et al. [11] in 2006, proposed a driving method by using current pulses, which aimed at the precise displacement control. This method applied pulse density modulation as shown in Fig. 1.4 and composed of a complex feedback loop with high resolution DAC, DSP and PID controller to achieve a performance in displacement as well as to use the voltage linear amplifier. But the operational frequency also ranges in the low frequency as the results presented by A. J. Fleming et al. [8].

1.4 Driving in Voltage Amplifier

Comparing with current or charge driving, voltage amplifiers can also be used to drive piezoelectric actuators because they can precisely generate any driving waveforms. Two topologies of amplifiers have been realized for driving piezoelectric actuators [12], [13]. One is based on switching and the other is a linear amplifier. As mentioned in [12] and references therein, N. Vujic et al. in 2002, proposed a comparison of linear and switching drive amplifiers for piezoelectric actuators. Therein, the well-known analyses are that the linear amplifiers consume significantly more power than the switching amplifiers. The power dissipations of the linear amplifiers increase with the increasing frequency because the capacitors draw more currents at higher frequency. The switching amplifiers show approximately constant power consumption over frequency because they recycle the current through storage capacitors. The constant power consumption represents (small) fixed losses in the amplifiers.

The following paragraphs 1.4.1 and 1.4.2 introduce both switching and linear amplifiers individually and make the comparison between each other.

1.4.1 Switching Amplifier

In a switching amplifier [13]-[15], a setup stage is initially adopted to generate the constant high voltage required by the piezoelectric actuator. The second stage is a half or full bridge as Fig. 1.5 shown in reference [13], which delivers the output voltage to the actuator as dictated by the reference signal. The output voltage is synthesized by appropriately controlling the power transistors using the pulse width modulator. The switches of the power transistors cause a ripple voltage on the top of these mean waveforms. This ripple voltage acts as a disturbance signal on the actuator, causing high-frequency excitation and undesired heating in the actuator. The ripple noise may be reduced by increasing the switching frequency. However, increasing the switching frequency increases the switching numbers of transistor as well as the switching losses in the power transistors. The switching frequency is typically held constant in a pulse width modulation (PWM) controller and is set to be between a few ten kilohertz and a few hundred kilohertz (20~100 kHz). The bandwidth of the switching amplifier is limited because the signal frequency must be much lower than the switching frequency. For a practical realization and application, the bandwidth of the signal to be amplified must be limited to ten percentage of the switching frequency. In addition the blanking time derived from the bridge circuit of switching amplifier will induce nonlinear outputs [16], and the switching harmonic frequency will impact to the quality of the output signal more or less.

Here, a brief discussion for the influence of blanking time would be introduced below. Referring to Fig. 1.5(b), the combination of T1 and T2 switches is the so-called one leg [16] of the full-bridge inverter, and T3/T4

composes the other leg. The turn-on of the other switch in that inverter leg is delayed by a blanking time t_{Δ}, which is conservatively chosen to avoid a "shoot through" or cross-conduction current through the leg. This blanking time is chosen to be just a few microseconds for fast switching devices like MOSFETs and larger for slower switching devices. Therefore, the distortion or nonlinear induced from blanking time is explainable and reasonable. Then a load current is assumed to be sinusoidal and lagging behind the output voltage of full-bridge inverter. The distortion in output voltage at the current zero crossings results in low order harmonics such as third, fifth, seventh, and so on, of the fundamental frequency in the inverter output [16]. These entire disturbance sources influence the performance of amplifier more or less, so how to avoid or reduce these influences is also a popular subject to its region.

In some practical cases, several kilowatts of driving power in needed, at a few tens of kilohertz, for loads that electric impedance changes rather abruptly from capacitive to inductive near some resonant frequencies. The amplifier [13] as shown in Fig. 1.6(a), proposed by K. Agbossou et al. in 2000, utilized a class-D amplifier or inverter to drive piezoelectric loads and proposed a duty cycle varied PWM signal to switch the full bridge circuit and provided approximately 2 kW between 10 and 100 kHz. This method successfully solves the limitation of bandwidth and extends its range to 100 kHz. Although K. Agbossou et al. solved the harmonic nuisance problem by utilizing and designing a second-order Butterworth filter in front of the capacitive load, but the full bridge inverter still has nonlinear characteristic induced from the blanking time on the "legs" of inverter.

D. K. Lindner et al. [14] proposed a low-level input voltage switching amplifier for piezoelectric actuators to stabilize rifle gun system that can eliminate the disturbances induced by the shooter in 2002. The inertial stabilized

rifle (INSTAR) utilized flyback circuit to boost the bus voltage from DC battery which is setup inside the gunstock and a half-bridge circuit to amplify the reference signal. Although INSTAR is dapper and efficient but the operating frequency is designed below 1.2 kHz which is not suitable in most applications. The most significant drawback of "digital" switch-mode (class-D) amplifier, however, is their low bandwidth caused by the fundamental compromise which has to be accepted between signal frequencies, filter cutoff frequency and switching frequency. With the turn-off power semiconductor devices being presently available for the kVA-power region (insulated gate bipolar transistors – IGBTs and MOSFETs), the switching frequency usually is limited to 20-100 kHz. The tasks of the LC filter or other high order filters at the output of the switching stage are the suppression of the switching frequency harmonics without significant influence on the signal components. For the practical realization, this results in the fact that the bandwidth of the signal to be amplified is limited to around 1/10 of the switching frequency, i.e., to values of 2~10 kHz [15].

According to the drawbacks of switch-mode amplifier mentioned above, H. Ertl et al. [15] proposed a Flying-Battery switch-mode amplifier which implements a high power output and reduces efficiently the voltage ripple as Fig. 1.6 shown. This multilevel multicell switch-mode amplifier proposed therein simultaneously solved both output voltage quality and bandwidth of class-D amplifiers. As mentioned in reference [15] and referred therein, a brief introduce of the concept and theory of multilevel multicell switching-mode amplifier would be presented. Figure 1.7 demonstrates the basic stationary operation of the multicell amplifier topology. The control signal $s_{a,i}$ and $s_{b,i}$ of the switching cell i = 1 … N are gained by comparison of the reference voltage $+u_{ref}$ and $-u_{ref}$ with a triangular carrier signal $u_{tri,i}$ of frequency

f_S(switching frequency of the power MOSFETs). From the top drawing of Fig. 1.7, the triangular waves corresponding to each cell have been phase shifted of T/N in a sequence, then the control signals of switches of each cell will be determined after comparing with the reference voltages, $+u_{ref}$ or $-u_{ref}$. The output voltage of each cell, $u_{ab,1}$, $u_{ab,2}$, $u_{ab,3}$ and $u_{ab,4}$ and the voltage summation $\sum u_{ab,i}$ of each cell are shown in Fig. 1.7 clearly. Despite the switching frequency f_S used for MOSFETs is low, the switching signal frequency of entire system output is eight times of f_S. Therefore the drawback and nuisance of insufficient bandwidth of class-D amplifier can be overcome in this topology. Nevertheless, the maximum operational frequency of the system mentioned therein is less than 10 kHz. Also, due to the applied voltage U of system has been divided into N components as U/N which individually serves to each cell as the applied voltage, and a LC filter is used in front of the loading, the output ripple is reasonably and efficiently reduced as described therein.

1.4.2 Linear Amplifier

The linear amplifier has a higher bandwidth, slew rate and linearity a switching amplifier. It also has less noise. However, the linear amplifier consumes more power than the switching amplifier when it is driving capacitive loads which mentioned in [12]. E. Montane et al. [17] found an integrated driving solution based on a full custom design of a high voltage op-amp, compatible with the relevant high-density packaging constraints in 2001. An attractive method proposed in [18] and [19] involves a combination of op-amps and a power stage consists of complementary MOSFETs as Fig. 1.8 shows. The current driving capacity can be readily increased. This method requires appropriate protection circuits to reduce excessive change rates and to operate transistors in the safe working region. As mentioned in [18] and referred therein, this driving amplifier proposed by M. S. Colclough et al. in 2000, provided a

capability of 100 kHz bandwidth, ±200 V output swing, ±340 mA output current and 300 V/μs slew rate. In [19], the driving amplifier proposed by B. Yan et al. in 2003, provided a capability of around 1 kHz bandwidth, ±280 V output swing and ±300 mA output current. S. Robinson [20] proposed a bridge configuration as shown in Fig. 1.9 in 2006, which employs two high voltage op-amps connected in a bridge circuit, can deliver a ±150 V output voltage swing that is double than the voltage delivered by a single device.

1.5 Controlling Strategies for Hysteresis Compensation

Regarding to the nonlinearity caused from hysteresis mentioned in [5]-[8], many methods had been proposed to compensate the hysteresis of the piezoelectric actuator. Y. Okazaki [21] presented a feedback of the displacement of piezoelectric actuators to overcome it in 1990; J. J. Dosch et al. [22] proposed a bridge circuit with additional resistors or capacitors to solve this phenomenon in 1992; C. V. Newcomb et al. [5] address the idea for a supplied charge control by driving a current source in 1982; P. Ge et al. [23] proposed mathematical models with Preisach's model in 1995; S. Chonan et al. [24] submitted the approach of approximation with polynomials in 1996; H. Kaizuka et al. [25] proposed insertion of an additional capacitance in series to solve this phenomenon in 1988; R. Changhau et al. [26] disclosed the method for an inverse control formed by a hysteresis mathematical model to compensate the hysteresis phenomena in 2005; J. M. Cruz-Hernandez et al. [27] presented a phase controller with Preisach's model to compensate and reduce hysteresis phenomenon in 2001. J. J. Tzen [28] proposed a controller design for the linear amplifier application. As discussed in [28] and referred therein, the nonlinearity can be solved by control loop. Therefore, this dissertation develops and designs a novel driving amplifier circuit to support the control loop proposed by J. J. Tzen et al.

Chapter 2 Multi-level Amplifier Topology

2.1 Introduction

The multi-level amplifier proposed in this dissertation provides greater flexibility and wider bandwidth than those that rely on high voltage op-amps. The circuit is easily implemented by connecting floating signal modules in series. The general idea of multi-level amplifier is slightly similar to the circuit topology proposed by H. Ertl et al. [15] in 2002. These floating modules are realized using IC-style op-amps. When configured in this way, the multi-level amplifier can deliver output voltage swings that are the sums of the swings of individual modules. The conception of multi-level amplifier can be illustrated briefly in Fig. 2.1 and 2.2. Figure 2.1 shows a generic difference amplifier, where V_b denotes the reference potential of difference amplifier. In a general application, V_b is defined as the real ground of system and its value equals to zero. Fig. 2.2(a) illustrates this case when V_b equals to zero, the output voltage of difference amplifier is bounded approximately in the range of dual power supplies rail, where solid lines indicate the power supplies rail and dotted line is the output voltage. Therefore, if the reference potential V_b has an un-zero value relative to real ground, then the output voltage of differential amplifier is the value of the summation of V_b and the pure output voltage relative to reference potential V_b as shown in Fig. 2.2(b).

Hence, the amplifier topology applies an un-zero reference potential V_b is named as “floating” module in this dissertation. As shown in Fig. 2.3, applying the conception of floating module, the ground reference in the first side and floating reference in the second side are detached from the isolation amplifier. Such a floating module with difference amplifier is named as “Isolated Floating Difference Amplifier” and IFDA is used for its abbreviation in this dissertation.

And a module which consists of non-inverting configuration and inverting configuration isolated floating difference amplifiers is as shown in Fig. 2.4. It is named as "Balanced Floating Difference Amplifier" and BIFDA is used as its abbreviation.

The goal and idea of this study is to construct a circuit topology by utilizing the cascade of multiply floating modules to provide a large output signal and to own a high operational bandwidth. Each independent floating module, BIFDA, in the cascaded circuit topology is named as one level. As the overall gain is increased by adding floating signal modules, the bandwidth does not change. The power dissipated by the amplifier increases with frequency because capacitors draw more current at higher frequencies. The output of each floating signal module can deliver the same current to the load. The maximum output power may be dissipated by each module. According to the conceptions illustrated above, two circuit topologies are proposed as direct-floating cascaded topology and indirect-floating cascaded topology as shown in Fig. 2.3(a) and Fig. 2.3(b). Following sections will describe both topologies in the detail.

2.2 Cascade Amplifier

According to the conceptions illustrated in section 2.1, how to create floating references for each BIFDA is the key point of the floating amplifier topology which is proposed in this dissertation. Figure 2.5(a) and (b) show two topologies to create and construct the floating amplifiers. Figure 2.5(a) is an indirect-floating cascaded module, where the floating references V_b of non-inverting configuration and inverting configuration in each BIFDA level are connected to each other, and output signal of non-inverting configuration in the i^{th} level is connected to the output signal of inverting configuration in the $(i+1)^{th}$ level. The total output voltage of indirect-floating module is drained from the

non-inverting configuration of n^{th} level into the inverting configuration of the first level. Figure 2.5(b) is direct-floating cascaded module, where the floating reference of non-inverting configuration V_b^+ in the $(i+1)^{th}$ level is supplied and maintained by the output voltage of non-inverting configuration $V_{out,p}$ in the i^{th} level; the floating reference of inverting configuration V_b^- in the $(i+1)^{th}$ level is supplied and maintained by the output voltage of inverting configuration $V_{out,n}$ in the i^{th} level. The total output voltage of direct-floating module is drained between the non-inverting and inverting configuration of n^{th} level.

Figure 2.6(a) and (b) show the gain principle of multi-level balanced isolated floating difference amplifier, which is abbreviated as MBIFDA, in both indirect- and direct-floating cascaded topologies. The indirect-floating cascaded topology as shown in Fig. 2.6(a), each difference amplifier has the same amplified value of G, and a floating reference F' exists in the i^{th} level and F'' is in the $(i+1)^{th}$ level. As mentioned above, the output signal of non-inverting configuration in the i^{th} level is connected to the output signal of inverting configuration in the $(i+1)^{th}$ level.

$$G + F' = -G + F'' \tag{2.1}$$

$$F'' = F' + 2G \tag{2.2}$$

Hence, the system output signal of indirect-floating cascaded topology can be derived as

$$V_{out} = G + F'' - (-G + F') = G + (F' + 2G) + G - F' = 4G \tag{2.3}$$

The output voltage derivation of MBIFDA in an n level system can analogous with Eq. (2.3) as $2nG$. Compared with Fig. 2.6(a), the direct-floating cascaded topology as shown in Fig. 2.6(b) has differences of a floating reference F' exists in the non-inverting configuration and F'' is in the inverting configuration of the i^{th} level. Hence the system output signal drains from the $(i+1)^{th}$ BIFDA is

$$V_{out} = (2G + F') - (-2G + F'') = 4G + F' - F'' \quad (2.4),$$

where the floating reference F' and F'' are not equal to each other. But referring to Fig. 2.5(b), in the first level of direct-floating cascaded MBIFDA, the reference voltages of non-inverting and inverting configuration are identical. Hence, the output voltage derived from direct-floating cascaded MBIFDA is eventually equal to the result of the indirect one, $V_{out} = 2nG$.

In chapter 3, the indirect-floating cascaded topology will be introduced and analyzed in the detail, and chapter 4 presents the direct-floating cascaded topology.

Chapter 3 Indirect-Floating Cascaded Topology

3.1 Difference Amplifier

Referring to Fig. 2.1, a finite open-loop amplifier gain and a nonzero common-mode gain are introduced to analyze the circuit. The output voltage V_o of a non-ideal op-amp may be expressed by the sum of the differential-mode and common-mode signals as follows.

$$V_o = A_{o,d}(V_+ - V_-) + A_{o,cm}\frac{(V_+ + V_-)}{2} \tag{3.1}$$

where $A_{o,d}$ and $A_{0,cm}$ are the open-loop differential-mode gain and the common-mode gain, respectively; V_+ and V_- are the signals applied to the non-inverting and inverting terminals of the op-amp. Based on the superposition concept and existed an infinite input resistance, then assumed that the V_{i+} and V_{i-} equal to zero individually. Two portions of superposition, $V_{o,1}$ and $V_{o,2}$, can be derived as

$$V_{o,1} = A_{o,d}(V_{+,1} - V_{-,1}) + A_{o,cm}\frac{(V_{+,1} + V_{-,1})}{2} \tag{3.2},$$

where

$$V_{+,1} = \frac{R_4}{R_3 + R_4}V_{i+}$$

$$V_{-,1} = \frac{R_1}{R_1 + R_2}V_{o,1}.$$

And

$$V_{o,2} = A_{o,d}(V_{+,2} - V_{-,2}) + A_{o,cm}\frac{(V_{+,2} + V_{-,2})}{2} \tag{3.3},$$

where

$$V_{+,2} = 0$$

$$V_{-,2} = \frac{R_1}{R_1 + R_2} V_{o,2} + \frac{R_2}{R_1 + R_2} V_{i-}.$$

Then using the superposition method

$$\begin{aligned} V_o = V_{o,1} + V_{o,2} = & \frac{A_{o,d}}{M}\left(\frac{R_4/R_3}{1+R_4/R_3} V_{i+} - \frac{R_2/R_1}{1+R_2/R_1} V_{i-}\right) \\ & + \frac{A_{O,cm}}{2M}\left(\frac{R_4/R_3}{1+R_4/R_3} V_{i+} + \frac{R_2/R_1}{1+R_2/R_1} V_{i-}\right) \end{aligned} \quad (3.4),$$

where

$$M = 1 + \frac{A_{o,d}}{1+R_2/R_1} - \frac{A_{o,cm}}{2(1+R_2/R_1)}$$

the differential-mode input voltage is defined as

$$V_{in,d} = V_{i+} - V_{i-} \quad (3.5)$$

and the common-mode input voltage is defined as

$$V_{in,cm} = (V_{i+} + V_{i-})/2 \quad (3.6)$$

Combining Eqs. (3.5) and (3.6) and substituting the result into Eq. (3.4) yields

$$\begin{aligned} V_o = & \left(\frac{R_4/R_3}{1+R_4/R_3}\left(A_{o,d} + \frac{A_{o,cm}}{2}\right) + \frac{R_2/R_1}{1+R_2/R_1}\left(A_{o,d} - \frac{A_{o,cm}}{2}\right)\right)\frac{V_{in,d}}{2M} + \\ & \left(\frac{R_4/R_3}{1+R_4/R_3}\left(A_{o,d} + \frac{A_{o,cm}}{2}\right) - \frac{R_2/R_1}{1+R_2/R_1}\left(A_{o,d} - \frac{A_{o,cm}}{2}\right)\right)\frac{V_{in,cm}}{M} \end{aligned} \quad (3.7)$$

Equation (3.7) describes the net output voltage of the difference amplifier as the sum of the differential-mode input signal and the common-mode input signal, for various close-loop gains. The differential-mode voltage gain $A_{CL,d}$ and the common-mode voltage gain $A_{CL,cm}$ of the difference amplifier are derived

$$A_{CL,d} = \left(\frac{R_4/R_3}{1+R_4/R_3}\left(A_{o,d} + \frac{A_{o,cm}}{2}\right) + \frac{R_2/R_1}{1+R_2/R_1}\left(A_{o,d} - \frac{A_{o,cm}}{2}\right)\right)\frac{1}{2M} \quad (3.8)$$

$$A_{CL,cm} = \left(\frac{R_4/R_3}{1+R_4/R_3}\left(A_{o,d} + \frac{A_{o,cm}}{2}\right) - \frac{R_2/R_1}{1+R_2/R_1}\left(A_{o,d} - \frac{A_{o,cm}}{2}\right)\right)\frac{1}{M} \quad (3.9)$$

The constraint is proposed that $R_4 / R_3 = R_2 / R_1$ must be met for the difference amplifier to be able to reject a large common-mode signal and to generate simultaneously an output that is exactly proportional to the difference between the two input signals. In the limits as $A_{o,d} \to \infty$ and $A_{o,cm} \to 0$, the differential-mode gain of $A_{CL,d}$ equals the ideal value R_2 / R_1 and the difference amplifier has zero common-mode gain.

$$V_{out} \approx \frac{R_2}{R_1} V_{in,d} \tag{3.10}$$

3.2 Balanced Isolated Floating Difference Amplifier (BIFDA)

As presented in Fig. 3.1, a floating signal module comprises an isolation amplifier and a pair of difference amplifiers that are connected in an indirect-floating cascaded form. The output voltages of the difference amplifiers in non-inverting and inverting configuration have the same magnitude but are anti-phase. The output swing across the load is therefore double the swing that would be produced by a single difference amplifier. Any nonlinearity become symmetrical, reducing the second harmonic distortion to less than that associated with a single difference amplifier. Another advantage is that the bridge configuration doubles the slew rate.

The isolation amplifier is used as the input stage and the bridge configurations of the difference amplifiers are the second, or amplifier power stage. The previous results reveal that the input signal V_{in} of the isolation amplifier may be separated by the common-mode and differential-mode input signals. Since the inverting input terminal of the isolation amplifier is grounded, the pair of differential output voltages of the isolation amplifier can be written in terms of the input voltage V_{in} as follows. All the derived function below can refer to the Fig. 3.2, which presents a path flow of signal process of balanced

isolated floating difference amplifier in indirect-floating cascaded topology.

$$V_{out,iso}^{+} = \frac{1}{2} A_{iso,d} V_{in} + \frac{1}{2} A_{iso,cm} V_{in} + V_b \tag{3.11}$$

and

$$V_{out,iso}^{-} = -\frac{1}{2} A_{iso,d} V_{in} + \frac{1}{2} A_{iso,cm} V_{in} + V_b \tag{3.12}$$

where $V_{out,iso}^{+}$ and $V_{out,iso}^{-}$ are positive and negative differential output voltages, respectively; $A_{iso,d}$ and $A_{iso,cm}$ are the differential-mode and common-mode gains of the isolation amplifier, respectively, and V_b is the ground potential. The second stage formed by the difference amplifiers subtracts the two output voltages of the isolation amplifier and cancels common-mode signals.

Substituting eqs. (3.11) and (3.12) into Eq. (3.7) yields the output voltage of the upper difference amplifier in the non-inverting configuration:

$$V_{out,p} = A_{iso,d} A_{cl,d,p} V_{in} + \frac{1}{2} A_{iso,cm} A_{cl,cm,p} V_{in} + V_b \tag{3.13}$$

An analogous analysis of the inverting configuration achieves similar results, producing the negative differential-mode output voltage and the same common–mode voltage when the two difference amplifiers are identical.

$$V_{out,n} = -A_{iso,d} A_{cl,d,n} V_{in} + \frac{1}{2} A_{iso,cm} A_{cl,cm,n} V_{in} + V_b \tag{3.14}$$

The subscripts after the comma, p and n, refer to the non-inverting and inverting configurations, respectively. The overall output of the floating signal module is,

$$\begin{aligned} V_{out} &= V_{out,p} - V_{out,n} \\ &= (A_{cl,d,p} + A_{cl,d,n}) A_{iso,d} V_{in} + \frac{1}{2} (A_{cl,cm,p} - A_{cl,cm,n}) A_{iso,cm} V_{in} \end{aligned} \tag{3.15}$$

The output signal is independent on the ground pin, which is the key to the

flexibility of the floating signal module. Therefore the circuit topology shown in Fig. 3.1 is named as floating signal module.

3.3 Multi-Level Balanced Isolated Floating Difference Amplifier (MBIFDA)

The multi-level balanced isolated floating difference amplifier, MBIFDA, in indirect-floating cascaded topology shown in Fig. 3.3 consists of familiar floating signal modules in a cascaded connection. And the block diagram of one level floating amplifier is shown in Fig. 3.2. The indirect-floating cascaded multi-level amplifier has distinct benefits because of compounding of the voltage levels. Each floating signal module is made from low-voltage devices and provides both positive and negative analogous voltage levels. The resulting connection yields a high voltage and good power quality through the load connection. In the following, the superscript i refers to the i^{th} level of a floating signal module. The isolated bipolar power sources are required to provide sufficient power to the floating signal module and to deliver a specified power to a load. Previous results indicate that each floating signal module yields two output voltages $V_{out,p}^{(i)}$ and $V_{out,n}^{(i)}$, which are equal in magnitude but anti-phase. As discussed in chapter 2 and referring therein, the non-inverting configuration output terminal of the $(i\text{-}1)^{th}$ level of the floating signal module is directly connected to the inverting configuration output terminal of the i^{th} level of the floating signal module:

$$V_{out,p}^{(i-1)} = V_{out,n}^{(i)} \tag{3.16}$$

Substituting Eqs. (3.13) and (3.14) into Eq. (3.16) and rearranging the terms yields the ground potential in the i^{th} level as

$$\begin{aligned} V_b^{(i)} = V_b^{(i-1)} &+ A_{iso,d}^{(i)} A_{cl,d,n}^{(i)} V_{in} + A_{iso,d}^{(i-1)} A_{cl,d,p}^{(i-1)} V_{in} \\ &- \frac{1}{2} A_{iso,cm}^{(i)} A_{cl,cm,n}^{(i)} V_{in} + \frac{1}{2} A_{iso,cm}^{(i-1)} A_{cl,cm,p}^{(i-1)} V_{in} \end{aligned} \tag{3.17}$$

The maximum output voltage between the non-inverting configuration output terminal of the i^{th} level and the inverting configuration output terminal of the first level of the floating signal module in the cascade form is

$$V_{out,p}^{(i)} - V_{out,n}^{(1)} = A_{iso,d}^{(i)} A_{cl,d,p}^{(i)} V_{in} + \frac{1}{2} A_{iso,cm}^{(i)} A_{cl,cm,p}^{(i)} V_{in} + V_b^{(i)} + A_{iso,d}^{(1)} A_{cl,d,n}^{(1)} V_{in} - \frac{1}{2} A_{iso,cm}^{(1)} A_{cl,cm,n}^{(1)} V_{in} - V_b^{(1)} \quad (3.18)$$

Solving the ground potential among each level circuit by recursively commutating from Eq. (3.17) enables Eq. (3.18) to be rewritten as

$$V_{out,p}^{(i)} - V_{out,n}^{(1)} = \sum_{k=1}^{i} (A_{cl,d,p}^{(k)} + A_{cl,d,n}^{(k)}) A_{iso,d}^{(k)} V_{in} + \frac{1}{2} \sum_{k=1}^{i} (A_{cl,cm,p}^{(k)} - A_{cl,cm,n}^{(k)}) A_{iso,cm}^{(k)} V_{in} \quad (3.19)$$

Clearly, when difference amplifiers in floating signal modules are identical, or match on each level, common-mode signals formed by the internal op-amp devices or tolerances among discrete resistors may appear almost constant at the non-inverting and inverting terminals. The final term in Eq. (3.19) is the net common-mode signal, and approaches zero. The differential-mode signal represented by the first term in Eq. (3.19) is double that which would be generated by the non-inverting or inverting configuration single output voltages. The synthesized voltage waveform may be specified as a sum of output voltages of floating signal modules. Any number of floating signal modules may have in general any number of levels.

A prototype amplifier with six floating signal modules is implemented and experimental results presented in chapter 4 will verify the results of multi-level floating amplifier which were analyzed above. This prototype offers high-precision, high slew rate, high power density and a wide, safe operating region. Voltage driver capability can be readily increased further as required by

the piezoelectric application. The multi-level amplifier provides high-fidelity performance levels that were previously offered by high-quality linear amplifiers.

3.4 Frequency Response Due to Capacitive Loads

As the above mentioned, the external/isolated resistor R_S plays an important role in the system response. Despite the analyses and discussions presented in this chapter only take the external/isolated resistor R_S into consideration, but the following experimental and simulated results will present the effects and differences caused by this parameter.

Capacitive loads commonly cause problems, in part because they can greatly reduce the output bandwidth and slew rate, but primarily because the phase lag generated in the feedback loop can cause the amplifier to oscillate. The frequency response of the difference amplifier in the output portion is initially studied to determine the stability of the multi-level amplifier with the capacitive loads. The open-loop output resistance, R_O, is the factor that most strongly influences the variation in output performance with capacitive load. Figure 3.4 presents the equivalent circuit of the difference amplifier. An external resistor R_S is placed between the output of the difference amplifier and the load. The resistor isolates the op-amp output and the feedback network from the capacitive load, potentially eliminating the oscillation or reducing ringing. The combination of the isolation resistor and the load capacitor introduces a pole to increase stability of the overall system. The equivalent circuit has a finite open-loop gain $A_{O,d}$ and a nonzero output resistance R_O. The open-loop input resistance between the two input terminals of the op-amp is assumed to be ideal, which approaches to infinite, and so in most cases is assumed to be very large. Rearranging terms in Kirchhoff's Current Law (KCL) equations in S-domain for

nodes a, b, c, d and e, yields

$$AX = Y \tag{3.20},$$

where

$$A = \begin{bmatrix} 1+R_1/R_2 & 0 & 0 & -R_1/R_2 & 0 \\ 0 & 1+R_3/R_4 & 0 & 0 & 0 \\ A_{o,cm}/2 - A_{o,d} & A_{o,cm}/2 + A_{o,d} & -1 & 0 & 0 \\ 1/R_2 & 0 & 1/R_o & -1/R_o - 1/R_2 - 1/(R_s + 1/SC_L) & 0 \\ 0 & 0 & 0 & 1/(SC_L R_s + 1) & -1 \end{bmatrix},$$

$$X = \begin{bmatrix} V_a & V_b & V_c & V_d & V_{out} \end{bmatrix}^T,$$

$$Y = \begin{bmatrix} V_{in}^+ & V_{in}^- & 0 & 0 & 0 \end{bmatrix}^T$$

Then the output voltage can be derived as

$$V_{out} = \left(\frac{R_4/R_3}{(1+R_4/R_3)} (A_{o,d} + \frac{A_{o,cm}}{2}) + \frac{R_2/R_1}{(1+R_2/R_1)} (A_{o,d} - \frac{A_{o,cm}}{2} - \frac{R_0}{R_2}) \right) \frac{V_{in,d}}{2M'} + \left(\frac{R_4/R_3}{(1+R_4/R_3)R_o} (A_{o,d} + \frac{A_{o,cm}}{2}) - \frac{R_2/R_1}{(1+R_2/R_1)} (A_{o,d} - \frac{A_{o,cm}}{2} - \frac{R_0}{R_2}) \right) \frac{V_{in,cm}}{M'} \tag{3.21}$$

where

$$M' = (1 + \frac{A_{o,d}}{1+R_2/R_1} - \frac{A_{o,cm}}{2(1+R_2/R_1)} + \frac{R_o}{R_1+R_2} + \frac{R_o}{R_s + 1/C_L s})(1 + R_s C_L s)$$

and s is Laplace operator.

3.5 Differential-Mode Gain in Single Level Amplifier

The open-loop common-mode gain $A_{o,cm}(s)$ is neglected because a linear op-amp can readily reject a common-mode signal. The two resistance ratios R_2/R_1 and R_4/R_3 must be exactly equal to enable the difference amplifier to reject a large common-mode signal and to generate simultaneously an output that is exactly proportional to the difference between the two input signals. Rearranging the factor M' appears in Eq. (3.21), then

$$\frac{1}{M'} = \frac{1}{R_o(1+R_sC_Ls)} \frac{R_o \| (R_1+R_2) \| (R_s+1/C_Ls)}{1+\frac{R_1A_{o,d}}{R_o(R_1+R_2)} R_o \| (R_1+R_2) \| (R_s+1/C_Ls)} \tag{3.22}$$

Therefore, the overall differential-mode gain expressed in the first portion of Eq. (3.21) is reduced to

$$\begin{aligned} A_{CL,d}(s) &= \frac{R_2A_{o,d}-R_o/2}{R_1+R_2}\frac{1}{M'} \approx \frac{R_2A_{o,d}}{R_1+R_2}\frac{1}{M'} \\ &= \frac{R_2}{R_1}\frac{1}{(1+R_sC_Ls)}\frac{R_o \| (R_1+R_2) \| (R_s+1/C_Ls)}{(R_o \| (R_1+R_2) \| (R_s+1/C_LS)+Z_{CL,o})} \end{aligned} \tag{3.23}$$

where the closed-loop output impedance $Z_{CL,o}$ of the difference amplifier, to a good approximation, is given by

$$Z_{CL,o}(s) \approx \frac{(1+R_2/R_1)R_o}{A_{o,d}(s)} \tag{3.24}$$

$R_1 + R_2$ is typically in the kilo-Ohm range, and the two resistances R_o and R_S are both of the order of 10 ohm. The effective resistance of combinations of R_o and R_S is smaller than $R_1 + R_2$. Therefore, Eq. (3.23) can be rewritten as

$$A_{CL,d}(s) \approx \frac{R_2}{R_1}\frac{1}{(1+R_sC_Ls)}\frac{R_o \| (R_s+1/C_Ls)}{((R_o \| (R_s+1/C_Ls))+Z_{CL,o})} \tag{3.25}$$

The frequency response of the open-loop differential-mode gain $A_{o,d}(s)$ for a linear op-amp device can be characterized by inserting a dominant pole, as follows.

$$A_{o,d}(s) = \frac{A_{o,d}(0)}{1+s/\omega_{o,d}} \tag{3.26},$$

where $A_{0,d}(0)$ is the low-frequency differential mode gain in open loop and $\omega_{o,d}$ is the corresponding dominant pole frequency. Substituting Eqs. (3.26) and (3.24) into Eq. (3.25), and rearranging terms yields

$$A_{CL,d}(s) = \frac{R_2}{R_1} \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{3.27},$$

where the natural frequency ω_n and the damping ratio ξ are defined by

$$\omega_n^2 = \frac{A_{o,d}(0)\omega_{o,d}}{(1 + R_2 / R_1)(R_o + R_s)C_L} \tag{3.28}$$

and

$$\xi = \frac{R_s}{2}\sqrt{\frac{C_L A_{o,d}(0)\omega_{o,d}}{(1 + R_2 / R_1)(R_o + R_s)}} + \frac{1 + (R_o + R_s)\omega_{o,d}C_L}{2}\sqrt{\frac{(1 + R_2 / R_1)}{(R_o + R_s)C_L A_{0d}(0)\omega_{o,d}}} \tag{3.29}$$

Since $A_{o,d}(0)$ typically greatly exceeds the value of $1 + R_2 / R_1$, negative feedback drives the closed-loop output impedance $Z_{CL,o}$ in Eq. (3.24) to some low value at low frequency. The third term on the right-side of Eq. (3.25), which is expressed in an impedance divider format approaches unity. The limiting low frequency of differential-mode gain, given by Eq. (3.25), is R_2 / R_1. As the frequency increases, the open-loop gain declines but $Z_{CL,o}$ increases. The factor of impedance divider in the differential-mode gain expression of Eq. (3.25) becomes less than one. And the other explicit pole introduced by the capacitive load C_L is important in the drop of the magnitude of differential-mode gain with increasing frequency. This pole may dominate the high frequency response when the amplifier is used to drive a heavy capacitive load. At high frequency, the impedance of C_L declines and acts as a shunt between the output and ground. The differential-mode gain tends toward zero. The expression for the transfer function of differential-mode gain is a second order, low-pass response, given by Eq. (3.27). The damping ratio in Eq. (3.29) characterizes the transient response of the two-pole amplifier. For a very low damping ratio, the response is oscillatory, while for a large damping ratio, the response does not oscillate. The

desired performance depends on the value of the isolation resistor; a larger isolation resistor corresponds to a more damped pulse response.

3.6 Differential-Mode Gain in Multi Level Amplifier

Equation (3.19) in the previous analysis reveals that the overall differential-mode gain is the sum of the individual levels of gain factors;

$$A_{tot,d}(s) = \sum_{k=1}^{i} (A_{cl,d,p}^{(k)}(s) + A_{cl,d,n}^{(k)}(s)) A_{iso,d}^{(k)}(s) \tag{3.30}$$

The pole introduced by the isolation amplifier is assumed to be a low-frequency dominant pole, such that the poles of the difference amplifiers are far apart, and the isolation amplifier dominates the corner frequency of the overall differential-mode gain. As the overall gain is increased by increasing the number of levels of floating signal modules, the bandwidth is kept constant and the gain-bandwidth product multiplied by the number of levels. Trade-offs must be made between gain and the bandwidth in the design of a floating single module. As the output swing of the difference amplifier increases, both the levels of the multi-level amplifier used to reach the desired output swing and the corner frequency drop. The multi-level amplifier can operate effectively with fewer levels when the floating single module provides a higher voltage gain. The two poles introduced by capacitive loading and the difference amplifier gain move toward the dominant pole of the isolation amplifier and reduce the bandwidth as the gain factor increases. Evaluating the overall bandwidth requirement and preserving signal integrity during amplification are critical to design. The benefit of reducing the level greatly outweighs the disadvantage of reducing the bandwidth.

Chapter 4 Directly Floating Cascaded Topology

4.1 Balanced Isolated Floating Difference Amplifier (BIFDA)

As discussed in section 2.2, the floating cascaded topology consists of two topologies, the direct-cascaded and indirect-cascaded. Two topologies are extremely similar to each other in response characteristics. The following discussions are presented due to the differences between these two topologies. In section 3.2, Eqs. (3.13) and (3.14) describe the non-inverting and inverting configuration output signals of BIFDA in indirect-floating cascaded topology individually. Referring to Fig. 2.4, the syn-phase and opposite-phase output signals of BIFDA in directly floating cascaded topology can similarly be derived as

$$V_{out,p} = A_{iso,d}A_{cl,d,p}V_{in} + \frac{1}{2}A_{iso,cm}A_{cl,cm,p}V_{in} + V_{b+} \quad (4.1),$$

and

$$V_{out,n} = -A_{iso,d}A_{cl,d,n}V_{in} + \frac{1}{2}A_{iso,cm}A_{cl,cm,n}V_{in} + V_{b-} \quad (4.2)$$

The overall output of the floating signal module is,

$$\begin{aligned} V_{out} &= V_{out,p} - V_{out,n} \\ &= (A_{cl,d,p} + A_{cl,d,n})A_{iso,d}V_{in} + \frac{1}{2}(A_{cl,cm,p} - A_{cl,cm,n})A_{iso,cm}V_{in} + V_{b+} - V_{b-} \end{aligned} \quad (4.3)$$

The output signal is not independent on the ground pin here, which is main difference to compare to the indirectly floating cascaded one.

4.2 Multi-Level Balanced Isolated Floating Difference Amplifier (MBIFDA)

The multi-level balanced isolated floating difference amplifier, MBIFDA, in direct-floating cascaded topology shown in Fig. 4.1 which consists of the similar floating signal modules in a cascaded connection. The instinctive

configurations for these two floating power suppliers are determined for the direct- and indirect-floating cascaded multi-level amplifiers. The number of power supplies is almost twice of the indirect-floating cascaded topology, and the number of isolated amplifier is also twice of the indirect-floating cascaded one. Each floating signal module is made from low-voltage devices and provides both positive and negative analogous voltage levels. The resulting connection yields a high voltage and good power quality through the load connection. Previous results indicate that each floating signal module yields two output voltages $V_{out,p}^{(i)}$ and $V_{out,n}^{(i)}$, which are equal in magnitude but anti-phase. As discussed in chapter 2 and referring therein, the non-inverting configuration output terminal of the $(i\text{-}1)^{th}$ level, $V_{out,p}^{(i-1)}$ is directly connected to the floating reference, $V_{b+}^{(i)}$, the inverting configuration difference amplifier in the i^{th} level of the floating signal module; and $V_{out,n}^{(i-1)}$ is directly connected to $V_{b-}^{(i)}$.

$$V_{b+}^{(i)} = V_{out,p}^{(i-1)} \tag{4.4}$$

$$V_{b-}^{(i)} = V_{out,n}^{(i-1)} \tag{4.5}$$

The output voltage between the non-inverting and the inverting configuration output terminal of the i^{th} level floating signal module in the cascade form is derived from Eq. (4.3):

$$\begin{aligned} V_{out}^{(i)} &= V_{out,p}^{(i)} - V_{out,n}^{(i)} \\ &= (A_{cl,d,p} + A_{cl,d,n})A_{iso,d}V_{in} + \frac{1}{2}(A_{cl,cm,p} - A_{cl,cm,n})A_{iso,cm}V_{in} + V_{b+}^{(i)} - V_{b-}^{(i)} \end{aligned} \tag{4.6}$$

And the total output by summarizing all levels of MBIFDA can be obtained by substituting Eqs. (4.4) and (4.5) into Eq. (4.6):

$$\begin{aligned} V_{out}^{(i)} &= V_{out,p}^{(i)} - V_{out,n}^{(i)} \\ &= \sum_{k=1}^{i}(A_{cl,d,p}^{(k)} + A_{cl,d,n}^{(k)})A_{iso,d}^{(k)}V_{in} + \frac{1}{2}\sum_{k=1}^{i}(A_{cl,cm,p}^{(k)} - A_{cl,cm,n}^{(k)})A_{iso,cm}^{(k)}V_{in} + V_{b+}^{(1)} - V_{b-}^{(1)} \end{aligned} \tag{4.7}$$

Figure 4.1 shows that the floating references of non-inverting and inverting configuration in the first level are identical and directly connect to the ground, so

$$V_{b+}^{(1)} = V_{b-}^{(1)} \tag{4.8}$$

Replacing Eq. (4.7) with Eq. (4.8), the real output of i^{th} level is

$$\begin{aligned} V_{out}^{(i)} &= V_{out,p}^{(i)} - V_{out,n}^{(i)} \\ &= \sum_{k=1}^{i} (A_{cl,d,p}^{(k)} + A_{cl,d,n}^{(k)}) A_{iso,d}^{(k)} V_{in} + \frac{1}{2} \sum_{k=1}^{i} (A_{cl,cm,p}^{(k)} - A_{cl,cm,n}^{(k)}) A_{iso,cm}^{(k)} V_{in} \end{aligned} \tag{4.9}$$

Comparing Eq. (4.9) with Eq. (3.19), despite that there is differences exist between two floating cascaded topologies, but eventually the output signals drained from indirect- and direct-floating cascaded present the identical results. The following experimental and simulated results in chapter 5 also show these two topologies, which mean the same thing basically. Also, the frequency response of floating difference amplifier derived through section 3.4 to 3.6 can be used in the direct-floating cascaded topology.

Chapter 5 Simulations and Experimental Results

The practicality and performance of the modular implementation concepts described above were confirmed experimentally using six floating signal modules, interconnected in a cascaded six-level amplifier. Here the designing rules are following the specifications which be specified in general purpose for driving piezoelectric loads or capacitive loads. Table 5.1 presents a detail specification data for the prototype amplifier. As mentioned in chapter 3 and 4, according to experimental and simulated results, except the difference in the system architecture, direct and indirect cascaded circuit topologies mean the same thing, and have the same response in both time and frequency domains. But the influence caused by external/isolated resistor R_s can not be neglected anyhow. So the following experimental results and simulations will present and compare the influences derived from the presence and absence of the external/isolated resistor.

5.1 Experimental Setup

Figure 5.1(a) and 5.1(b) display the photographs of the experimental setup of the direct-floating cascaded and indirect-floating cascaded circuit topologies respectively, which are interconnected in a cascaded six-level amplifier. HCPL-7800 [30] is a fixed gain IC with the value of 8, and its corner frequency is around 100 kHz. The isolation amplifier electrically isolates input and output signals. The maximum input signal is limited to within ±200 mv to reduce the nonlinear distortion of the output signal. In order to meet the isolated amplifier input constraint and the voltage level of an A/D card of ±2.5 V, so a 1/11 voltage divider exists prior to the isolated amplifier input in the direct-floating cascaded topology. But in the indirect-floating cascaded circuit topology, the voltage divider is absent here.

LM4700 [31] is a power amplifier that can deliver 30W of continuous power to a load, and is used in the output stage of the floating signal module. It provides a slew rate of 18V/μs and a pretty wide unit-gain bandwidth of 7.5MHz. The full power bandwidth associated with the slew rate is about 1.85 MHz. The maximum output current is approximately ±2.5A for power supply voltages of ±20 volts. The input signal of the power amplifier in the floating signal module is varied between +1.6V and -1.6V. From Eq. (3.13), the maximum possible output swing of the difference amplifier is a function of the resistor ratio R_2 / R_1 when the equal ratios R_4 / R_3 and R_2 / R_1 are determined. The output saturation that generates large distortion in linear applications must be prevented by adjusting the feedback gain using a resistor ratio R_2 / R_1 of 11. When the input voltage of the isolation amplifier is ±200 mv, the output swing of the six-level amplifier may reach 400V, which is the designed value. From the point of view for the input signal of the circuit system, the total differential gain of direct-floating cascaded topology derived from Eq. (4.9) is

$$G_{dir,f} = 2 \times G_{vol,div} \times G_{iso} \times G_{diff} \times 6 = 2 \times \frac{1}{11} \times 8 \times 11 \times 6 = 96 \quad [V/V] \text{ (5.1),}$$

and the total differential gain of the indirect-floating cascaded topology derived from Eq. (3.19) is

$$G_{indir,f} = 2 \times G_{iso} \times G_{diff} \times 6 = 2 \times 8 \times 11 \times 6 = 1056 \quad [V/V] \qquad (5.2)$$

Where $G_{vol,div}$ means the gain of voltage divider, G_{iso} is the gain of isolation amplifier, and G_{diff} is the gain of differential amplifier. The constant factor 2 means the balanced amplifier topology and 6 means the six levels of the MBIFDA.

5.2 Results of the Simulation and Experiment

Figure 5.2 plots the simulated results. The figure has two contour plots of

the damping ratio ξ and natural frequency ω_n as functions of two independent variables - capacitive load and isolation resistance. The following parameters are used; R_o = 6 Ω, R_2 / R_1 = 11 and $A_{o,d}(0)\omega_{o,d}$ = 1.85 MHz. The iso-lines correspond to constant damping ratios and natural frequencies given by Eqs. (3.28) and (3.29). The two contour plots indicate that the damping ratio increases with the capacitive load and the isolation resistance, but the natural frequency declines. When the load is driven by a sinusoidal signal, the energy stored in the capacitor during the first half of the cycle is returned to the amplifier during the second half of the cycle as heat. The isolation resistance may increase the dissipation of the reactive energy. An experimental test indicated that much of the energy travels backward to the amplifier when the output is connected directly to a capacitor with no series resistances or is under 5Ω for an input sinusoidal signal with a frequency of less than 1 kHz. The distortion of the waveform is considerable. The output signal will slightly attenuated in a manner determined by the ratio of the isolation resistance to the total output resistance. An 10Ω isolation resistor is used, following a trial-and-error examination of the variation of the output response with the various capacitive loads. The contour plot reveals that the damping ratio is approximately 0.4 at a capacitive load of 0.1 μF.

5.2.1 Time-Domain Response

Figure 5.3 shows the system of six output and one input signals on the individual levels of the direct/indirect-floating cascaded circuit topology with six levels, where the capacitive loading is absent and voltage divider appears prior to the isolation amplifier input. Referring to it, the frequency of waveform is 100 kHz, a phase lag almost 90 degree exists therein. Then Fig. 5.4 plots the time-domain response of the multi-level amplifier excited by a sinusoidal-wave signal of 20 kHz with a floating output of 400V across the 0.1 μF capacitive

load. The output current requirement is

$$I_{out} = 2\pi f_{\max} V C_L = 2\pi(20e3)(\pm 200)(0.1e-6) = \pm 2.51A \quad (5.3)$$

This figure reveals that the output peak-to-peak current in the experiment is approximately 5.3A, which is measured across a 1 Ohm resistor in front of capacitive loading. The maximum power dissipation requirement [32] is

$$P_{ave,\max} = 4V_s^2 f_{\max} C_L = 4(200)^2(20e3)(0.1e-6) = 326.6\,W \quad (5.4)$$

Figure 5.4(b) presents the simulation results of the power dissipation analysis. Solid, dashed and dotted curves represent the powers that are instantaneously delivered from the amplifier to the load, from the supply unit to the amplifier, and dissipated from the amplifier, respectively. The portion of reactive power flow that is associated with the pure capacitive load returns to the amplifier in each cycle. The reactive power averaged over a complete cycle of the AC waveform, is zero. The mean power dissipation requirement of an amplifier, which is the difference between the power delivered from the supply unit and that delivered to the load, is 326.6W. This 326.6W of dissipated power has nothing to do with mechanical work. It is merely wasted in the electronics as the heat.

Figure 5.5 plots a typical pulse response for various capacitive loads where the external/isolated resistor is presented. The curve marked "C_L = open" is the response when capacitive load C_L is neglected; the curve marked capacitive values plots the circuit response if the amplifier is adopted with a capacitive load connected to its output. Most power amplifiers cannot easily drive highly capacitive loads very effectively, and attempting the same normally causes oscillations or ringing on the square wave response. The $C_L \leq$ 0.1 μF curves exhibit slight peaking. This peaking is caused by a large input signal at a high frequency that exceeds the slew rate of the output amplifier. The time response characteristics are almost identical when the capacitive loads are less than 0.01

μF. Table 5.2 lists rise and fall times for various capacitive loads. These times are based on the current that the output stage can deliver or sink. The slew rates measured from 10% to 90% the full-scale voltage swing is controlled by the current available to charge and discharge a high-impedance node capacitor. The experimental results, Fig. 5.5(a), and IsSpice simulation, Fig. 5.5(b), yield closely matching results.

5.2.2 Frequency-Domain Response without External/Isolated Resistor

Figure 5.6 plots the frequency response of the floating signal module without external/isolated resistor in six levels where a voltage divider 1/11 exists in front of isolation amplifier; Fig. 5.6 (a) is determined from the Matlab® analysis. Fig. 5.6(b) shows the experimental results of outputs on individual level of MBIFDA based on the zero loading test. Fig. 5.6(c) is obtained experimentally with four capacitive load values assigned. The results show that the corner frequency is in the order of 100 kHz. As shown in Fig. 5.6(a) and (c), both the simulation and experimental results present that the response roll off at -40 dB/decade near 100 kHz, indicating that the response involves more than one pole as Eq. (3.28) reveals. And this pole induced from capacitive loading greatly influences the system bandwidth and the response when the capacitive loading increases. Moreover, a 1/11 voltage divider exists in front of isolation amplifier, so the system total gain is equal to 96 V/V (~39.6 dB). The modified afterthought version of the indirect-floating cascaded circuit topology adds an external/isolated resistor R_S, therefore the simulation and experimental results are discussed and shown in the following section.

5.2.3 Frequency-Domain Response with External/Isolated Resistor

Figure 5.7 plots the frequency responses of a floating signal module with external/isolated resistor. Fig. 5.7 (a) is determined by the IsSpice® analysis based on the difference capacitive loadings in one level. Fig. 5.7(b) shows the

experimental results based on the difference capacitive loadings in one level. Fig 5.7(c) is determined by the IsSpice® analysis on the individual level based on the no-loading test. Fig 5.7(d) shows the experimental results on individual level based on the no-loading test. Fig. 5.7(e) is determined by the IsSpice® analysis of the sixth level based on the difference capacitive loadings and Fig. 5.7(f) is obtained experimentally from the output of the sixth level based on the difference capacitive loadings.

The results of Fig. 5.7(a) and (b) show that the corner frequency is of the order of 100 kHz. The three curves for capacitive loads of 0.1 μF, 0.01 μF and open conditions are fairly close together, and roll off at -40 dB/decade, also indicating that the response involves more than one pole as mentioned in section 5.2.2. As the capacitive load increases to C_L=0.2 μF, the output impedance at high frequency declines; the corner frequency drastically declines and the slope becomes steeper than -40 dB/decade. Two dominant poles are present near the corner frequency of 100 kHz in the circuit. Therefore, the signals change from a flat response to an about -40 dB/decade drop in gain. The first pole is on the isolation amplifier and the second pole is on the difference amplifier. The corner frequency of the isolation amplifier presented in the data sheet is 100 kHz. The LM4700 op-amp with the gain-bandwidth product of 7.5 MHz is connected in the difference amplifier configuration with a low-frequency closed-loop gain of 11. The corner frequency given by the gain bandwidth product rule is about 681 kHz. The full power bandwidth (FPBW) is the maximum frequency over which the output can swing dynamically without significant distortion. At lower frequency, the FPBW is limited by the output swing of the amplifier; at higher frequency, the response is limited by the slew rate of the amplifier. The LM4700 slew rate is SR=18 $V/\mu s$ and the desired peak output voltage is V_{op}=17 V. The FPBW based on slew-rate limitation, is $SR/(2\pi V_{op})$= 168.52 kHz, which is

much smaller than the bandwidth under small-signal non-slew rate limiting conditions and is close to 100 kHz. The analysis compares favorably with the experimental results. When the capacitive load exceeds 0.1 μF, the bandwidth is no longer determined by the internal op-amp, but rather than by the external capacitive load. Additionally, the pole introduced by the capacitive load dominates the frequency response. The corner frequency obtained by the time constant associated with the isolation resistance and capacitive load is approximately 99 kHz, which exceeds the value presented in Fig. 5.7(a) and (b). The low frequency differential-mode gain calculated from the first term of Eq. (3.15) is about 44.9 dB, which agrees with experimental results.

Figure 5.7(c) and (d) display a Bode plot of the voltage gains of the multi-level amplifier, accounting for the stack levels. The capacitive load is 0.01 μF. These curves show that the overall gain increases with the floating signal modules. The multi-level amplifier has a fixed bandwidth that is close to 100 kHz. The slope of the roll off at high frequency is -40 dB/decade, which was predicted theoretically. The experimental result demonstrates that the low frequency gain is approximately 60 dB, which is slightly lower than the simulated result of 61 dB. The common mode effect or the parameter tolerances among discrete components may explain the above gain loss.

Figure 5.7(e) and (f) present a bode plot of the voltage gains of the six-level amplifier versus capacitive load. The amplifier provides a maximum peak-to-peak current of 5 A. When a capacitive load of 0.1 μF is driven and reasonable power maintained in each module, the maximum allowable frequency that corresponds to the maximum peak-to-peak current is about 20 kHz as the dash line indicated. As the capacitive load increases, more peaking is observed. These curves reveal that this capacitance would dominate the circuit response if a capacitor load of 0.1 μF or higher were connected to the output.

The simulation results demonstrate this hypothesis. Figure 5.8 presents both the line spectrum of input and output signals and the magnitude has been normalized as unit.

5.3 Isolated Power Supply Unit

The advantage of the multi-cell configuration is its capacity to divide total power dissipation among cells, because each cell-amplifier provides the same loading current. Six isolated supply units that feed the individual floating signal module cell are adopted in the prototype amplifier setup of indirect-floating cascaded topology. And twelve isolated supply unit are adopted in the direct-floating cascaded topology. An extra amount of leakage current caused by the primary-to-secondary capacitances of the isolated power units increases the power dissipated by individual amplifier cells. Line filter safety capacitors (or an AC interference suppression capacitor) which improve the reliability, safety and performance of the power supply unit are important in the multi-cell circuit. Type Y safety capacitors are typically adopted between the AC line and ground, between AC neutral and ground, and between the primary and secondary circuits. Y capacitors contribute directly to increasing the total leakage current in the ground lead. When the input signal is positive, output current flows from the non-inverting amplifier of the $(i\text{-}1)^{th}$ cell to the inverting amplifier of the i^{th} cell, as presented in Fig. 5.9. The ground potential of the i^{th} cell of the isolated power supply unit has a positive voltage of $V_{out,p}^{(i-1)} - V_{out,n}^{(i)}$ above the ground potential of the $(i\text{-}1)^{th}$ cell. The safety capacitor Y, with capacitance $C_Y^{(i)}$, is charged and discharged as a bipolar input signal is applied, adding to the output loads of the inverting configuration amplifier of the i^{th} cell and the non-inverting configuration amplifier of the $(i\text{-}1)^{th}$ cell. The leakage currents are proportional to the driving frequency and occur in the internal cells. The topmost non-inverting configuration amplifier in the n^{th} cell and the bottom most

inverting configuration amplifier in the first cell is unaffected because the output currents directly flow into the external load. The surplus power dissipated because of leakage currents increases the temperature of ICs. These leakage currents can be reduced by introducing a low capacitive input/output coupling or inserting a common-mode choke into the output of the switch mode power supply unit [15].

Chapter 6. Conclusions

Multi-cell amplifiers can be realized using low-voltage, high current and power MOSFET devices or costly IC power amplifiers, to achieve high output power. Multi-cell topology enables the output voltage of the piezoelectric amplifier to be increased while maintaining the module's output swing limits. The multi-cell portion divides the total power dissipation among all of the modules, such that the higher system output power of each module does not exceed its individual power dissipation capacity. As compared to the achievable technical specifications the realization effort and production cost are comparatively low. The drawback of the multi-cell circuit topology is that many isolated switching-mode power supply units are required to feed the individual cell of power. In spite of this topology needs a lot of power supply units, but all power supply unit applied here costs less than NT 1,000. The cost of merchant amplifying instrument is usually more than NT 100,000, so this topology provides a low cost solution.

In applications that involve driving capacitive loads, the peak output current of the amplifier limits the useful bandwidth of the amplifier. The maximum capacitive load depends on both the slew rate of the amplifier and the maximum output current. The isolation resistance increases the damping ratio and reduces the output ringing. The experimental data presented herein correspond to an adjustment for a capacitive load of 0.1 μF. The advantages of the multi-cell amplifier include the approximately constant corner frequency and high common mode rejection ratio (CMRR), which offer the accuracy and linearity required for piezoelectric applications. Strong electrical isolation keeps high voltages away from equipment and reduces the risk of electrical shock. The feasibility and reliability of the amplifier were demonstrated both experimentally and by simulation.

This circuit topology presents a high bandwidth, high output and quite precision result. However the fed power directly into the loading will substantially decrease the system bandwidth. The original idea of design for the multi-level circuit topology is that the system bandwidth and dominant pole are completely dominated by the isolation amplifier. After huge amount of the substantial analyses, simulations and experiments, we found that the effect of the dominant pole shall be replaced by the loading effect in system response. Although the multi-level amplifier topology does not perform perfectly in the role of playing a power supply dues to the output current limitation of power amplifier, this circuit topology owns many advantages as the dissertation mentioned above, that can be applied in many fields of driving, and its flexibility and expandability make it more applicable to other fields.

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31. LM4700 Datasheet, *National Semiconductor Corp.*, 2004.
32. "General Operating Considerarions", *APEX Application Note 1,pp.539-549*, 2001 (http://www.apexmicrotech.com)

Type	dimensions mm	max. stroke µm	el. capacitance nF	stiffness N/µm	resonance frequency kHz	max. force generation N	max. compr. load N
PSt 150/2x3/5	2x3xL = 5	**7**/5	70	45	120	300	300
PSt 150/2x3/7	2x3xL = 9	**15**/9	170	25	70	300	300
PSt 150/2x3/20	2x3xL = 18	**30**/20	340	12	35	300	300
PSt 150/3.5x3.5/7	3.5x3.5xL = 9	**15**/9	350	50	70	800	800
PSt 150/3.5x3.5/20	3.5x3.5xL = 18	**30**/20	800	25	35	800	800
PSt 150/5x5/7	5x5xL = 9	**15**/9	700	120	70	1800	2000
PSt 150/5x5/20	5x5xL = 18	**30**/20	1800	60	35	1800	2000
PSt 150/7x7/20	7x7xL = 18	**30**/20	3600	120	35	3500	4000
PSt 150/10x10/20	10x10xL = 18	**30**/20	7200	250	35	7000	8000
PSt 150/14x14/18	14x14xL = 20	**25**/18	10500	500	32	11000	16000

Table 1.1 Catalog of stack type piezo actuators [2]

Multi-level amplifier

Output voltage	: ±200 V
Maximum output current	: ±2.5 A
Capacitive load	: 0 ~ 0.1 uF
Number of levels	: 6
Isolated power supply voltage	: ± 24 V
Bandwidth	: 100 KHz
Input voltage (direct-floating cascaded)	: ± 2.5 V
Input voltage (indirect-floating cascaded)	: ± 200 mV
System Gain (direct-floating cascaded)	: 96 (Ideal)
System Gain (indirect-floating cascaded)	: 1056 (Ideal)

Isolated amplifier (IC: HCPL7800)

Input voltage swing	: ±200 mV
Gain	: 8
Bandwidth	: 100 KHz

Difference amplifier (IC: LM4700)

Maximum supply voltage	: ±33 V
Output dissipation	: 30 W
Maximum output current	: 2.9 A
Gain-bandwidth product	: 7.5 MHz
Open-loop gain	: 110 dB
Close-loop gain (resistor ratio)	: 11
Slew rate	: 18 V/μs

Table 5.1 Multi-level linear power amplifier specifications

C_L	Rise time	Fall time	Slew rate
0.20 μF	18.2 μs	18.5 μs	17.6 V/μs
0.15 μF	13.7 μs	13.6 μs	23.3 V/μs
0.10 μF	9.2 μs	9.1 μs	34.7 V/μs
0.01 μF	2.9 μs	2.8 μs	110 V/μs
open	2.8 μs	2.7 μs	115 V/μs

Table 5.2　Response estimates

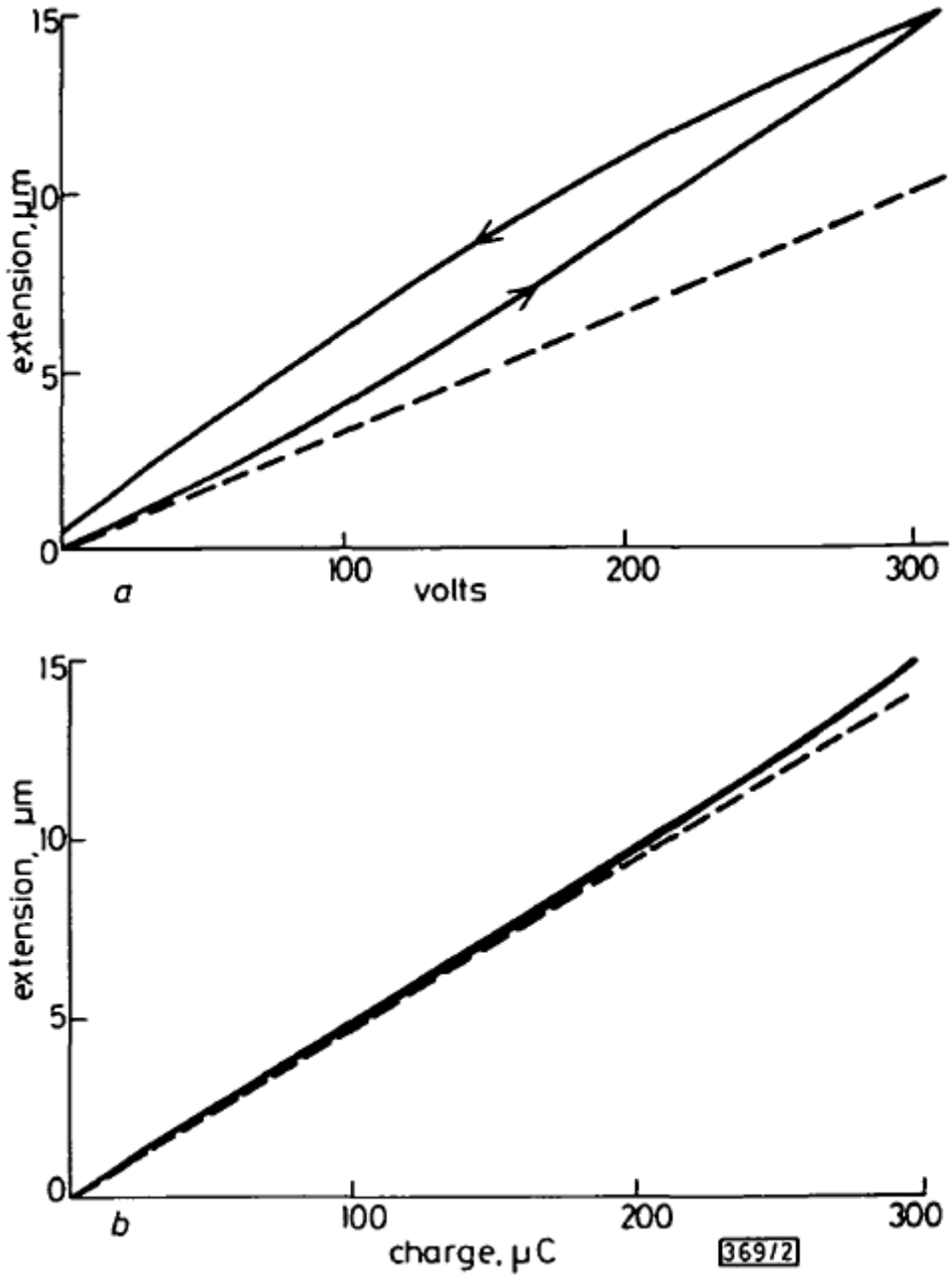


Figure 1.1 Measured extension of piezoelectric actuator (a) Against applied voltage, (b) Against applied charge [5].

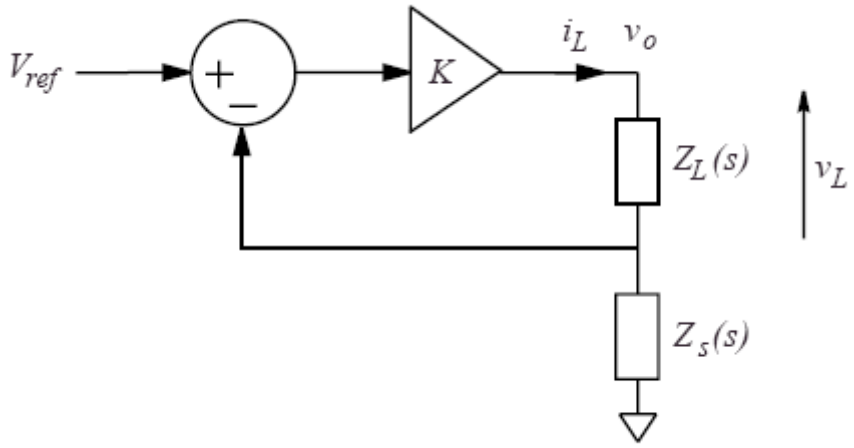


Figure 1.2 Generic current source [7].

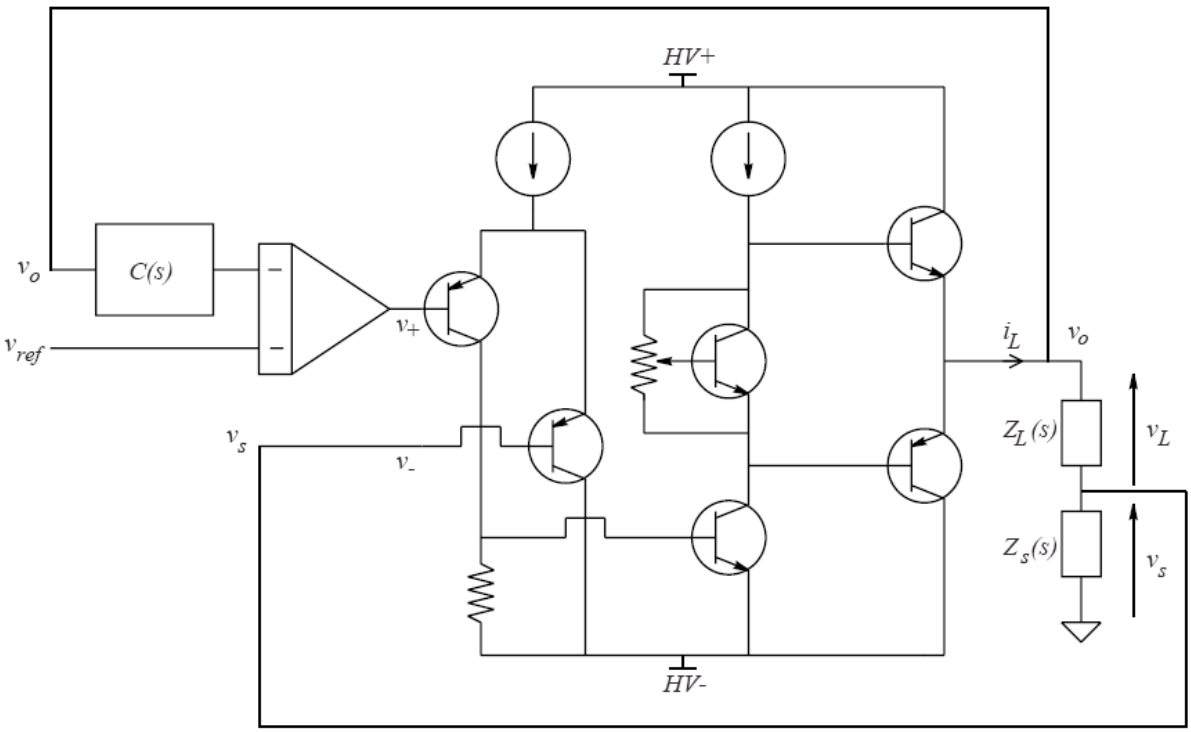


Figure 1.3 Simplified schematic of a compliance feedback current amplifier [7].

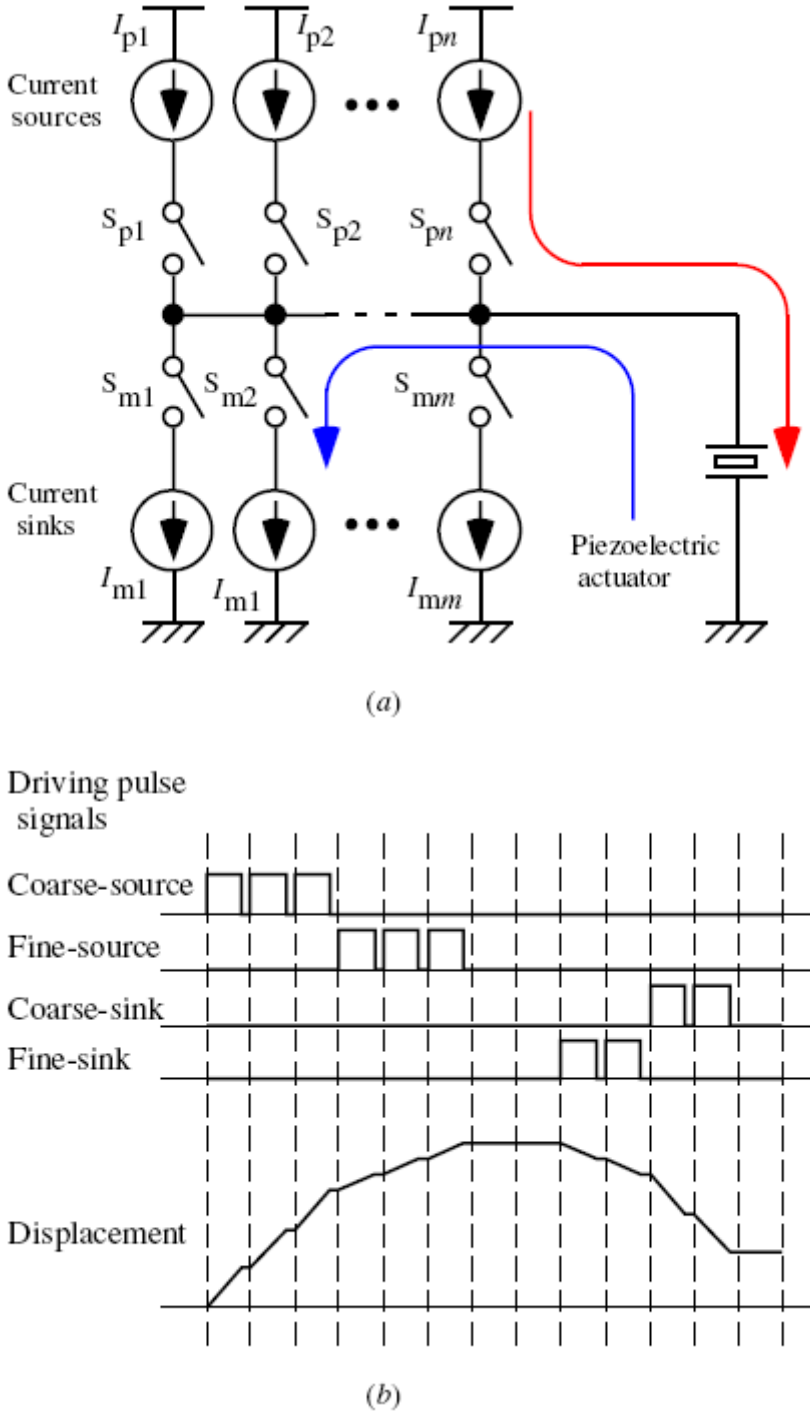
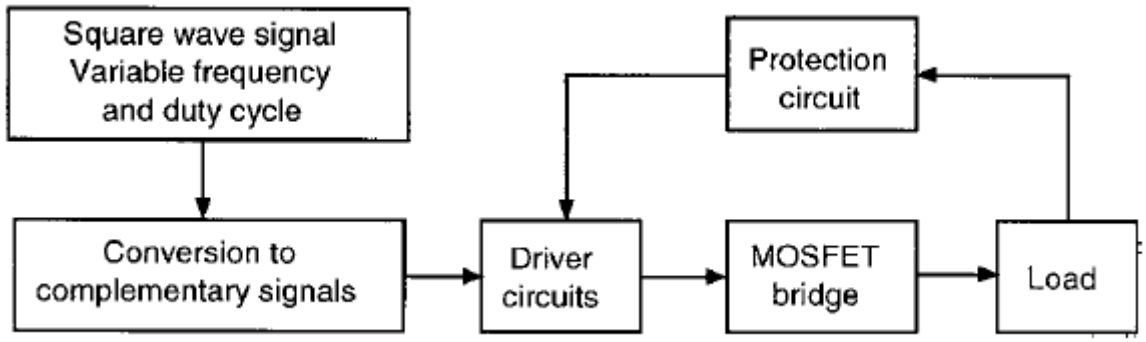
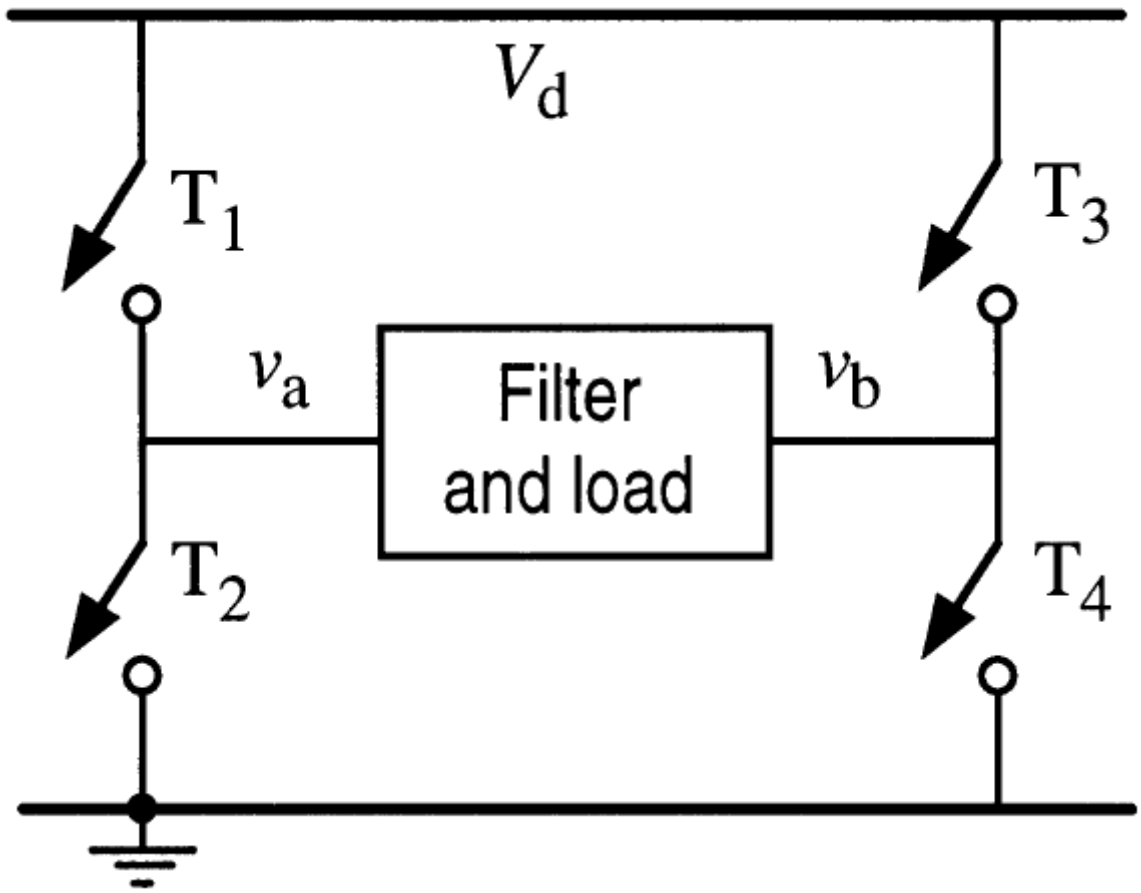


Figure 1.4 Principle of driving method by using current pulse (a) configuration of circuit (b)displacement [11].

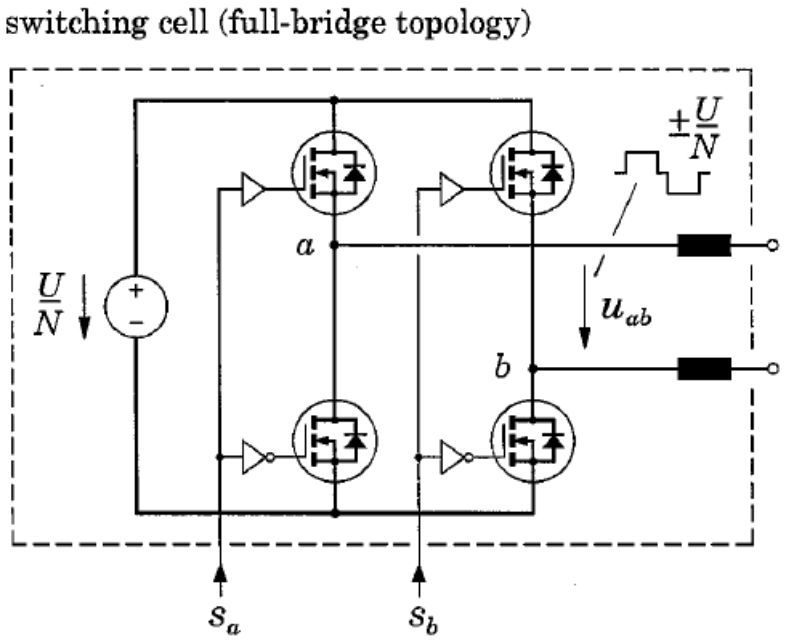


(a)

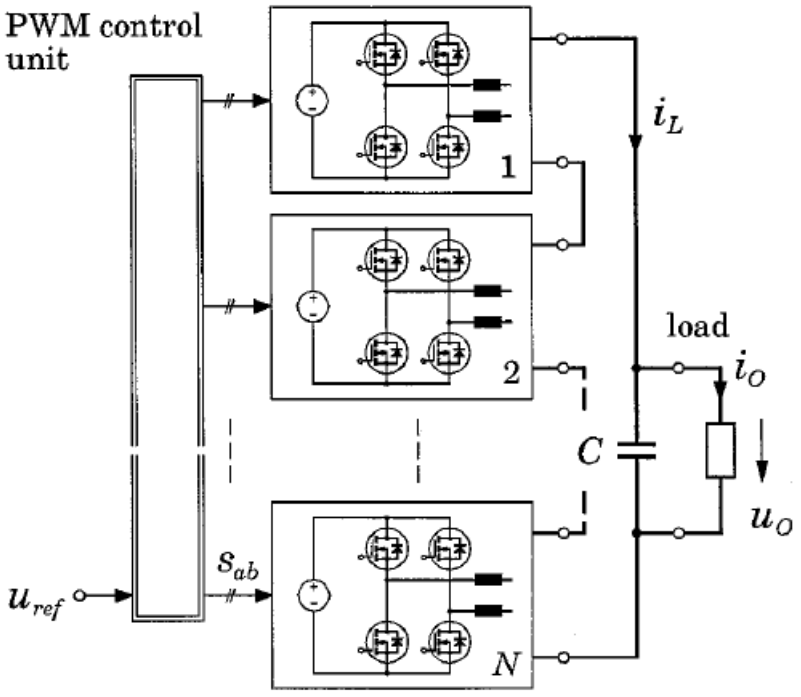


(b)

Figure 1.5 (a) Inverter block diagram, (b) Full-Bridge inverter [13].



(a)



(b)

Figure 1.6 Basic circuit topology of the multicell multilevel switch-mode power amplifier. (a) Single switch cell (full-bridge topology), (b) Total multistage amplifier system [15].

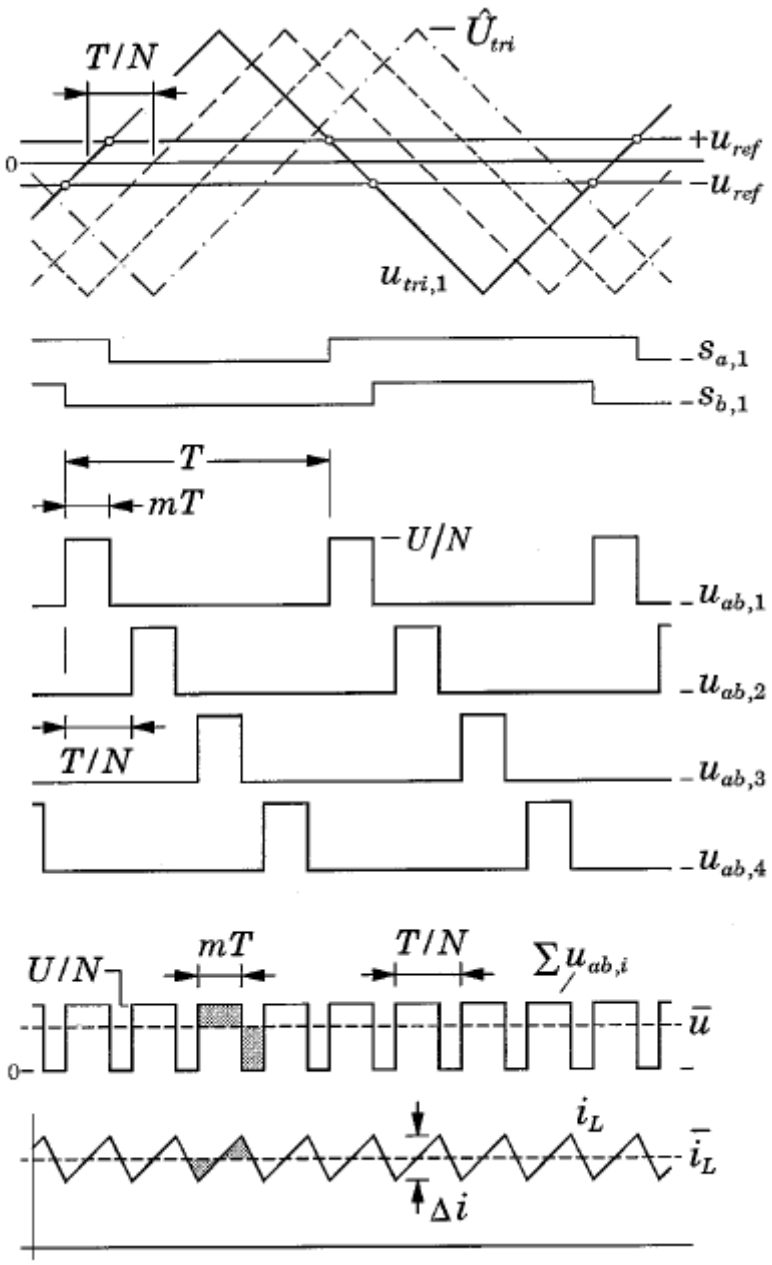


Figure 1.7 Wave shapes of interleaved triangular carrier signals for a multicell (N = 4) switched-mode amplifier [15].

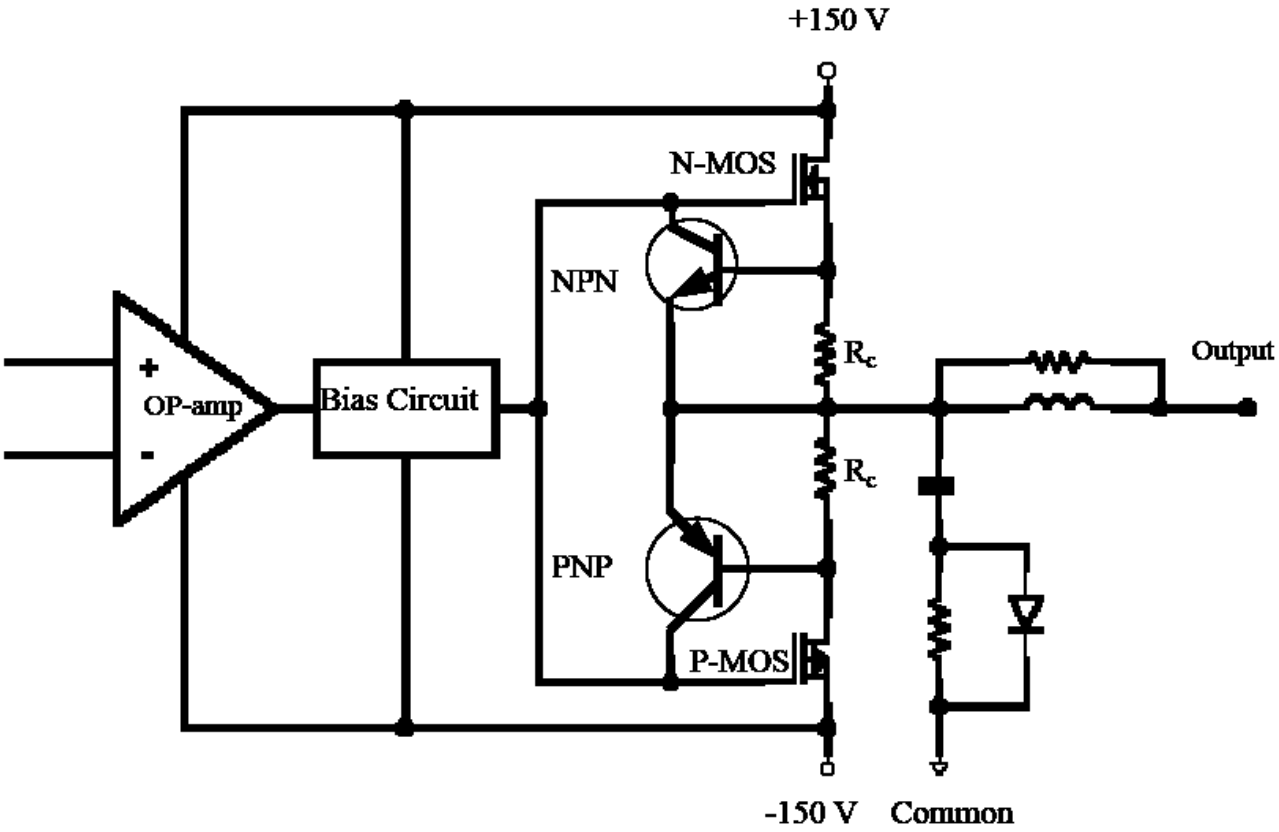


Figure 1.8 Basic circuit topology of linear amplifier with power stage [19].

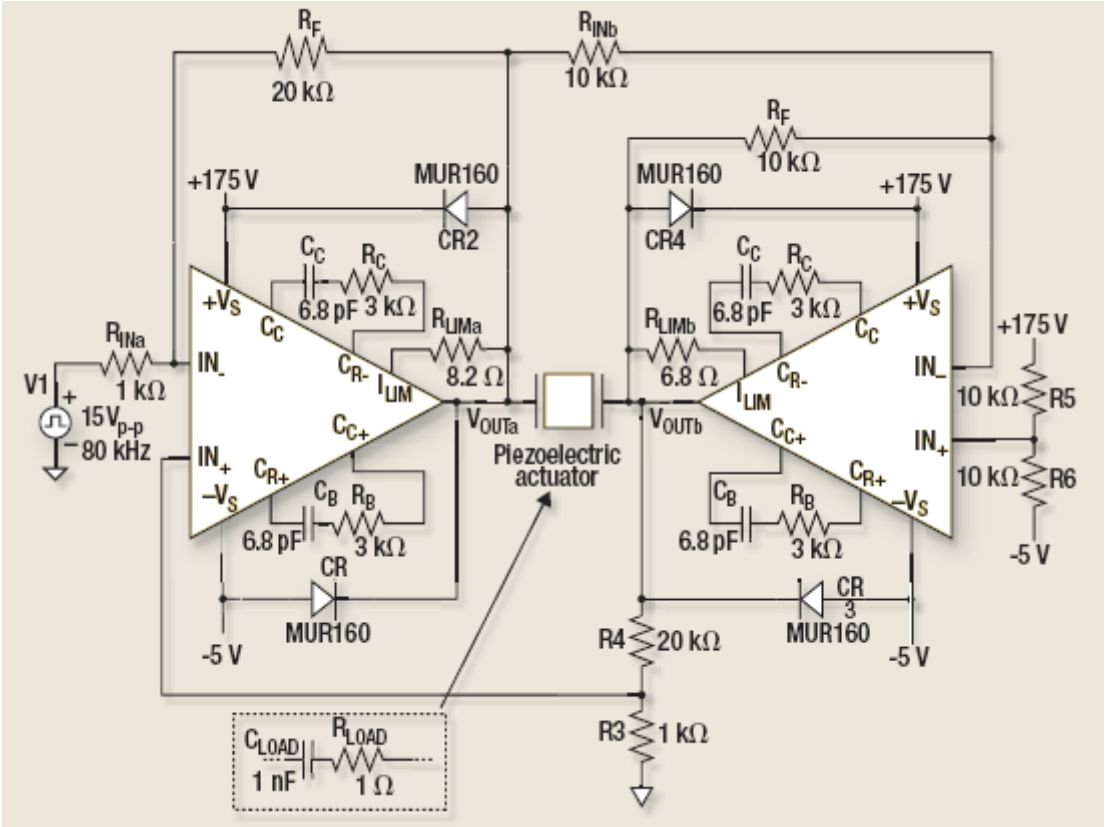


Figure 1.9 A pair of bridge-connected power op amps drive the piezoelectric actuator [20].

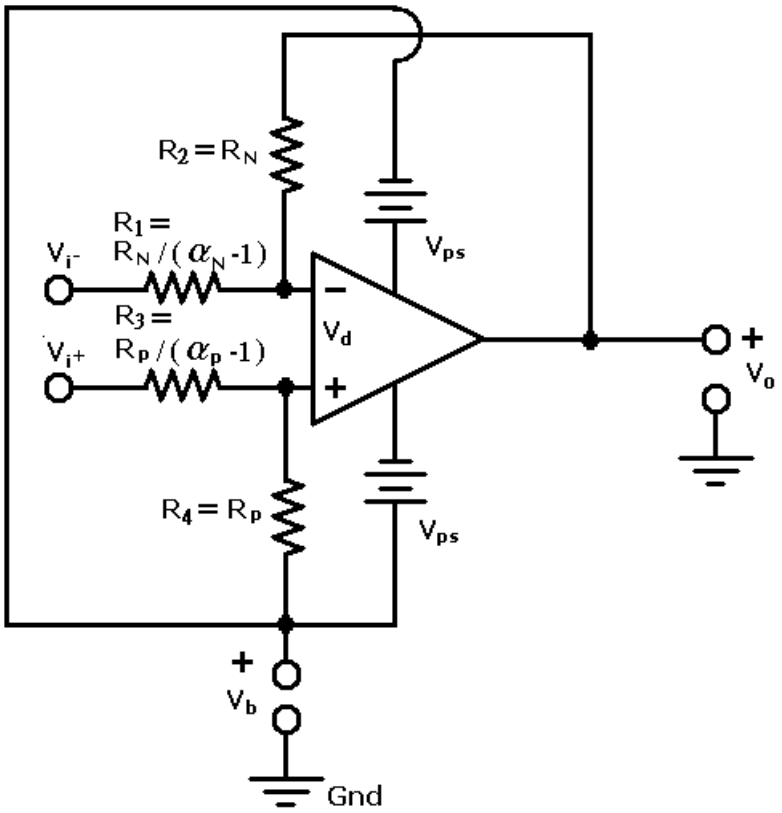


Figure 2.1 The difference amplifier

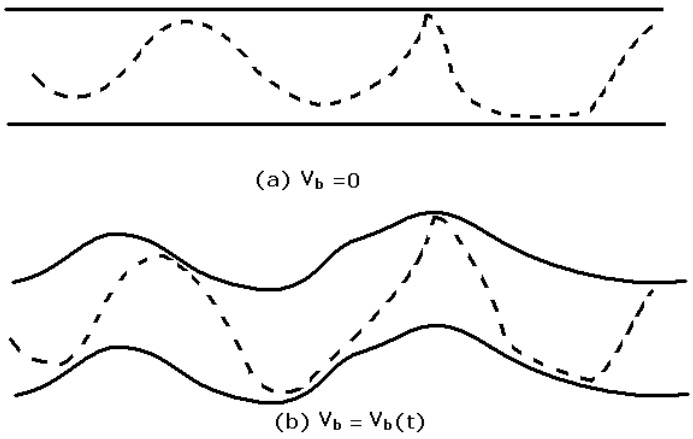


Figure 2.2 Output signals of difference amplifier of different power supply rail

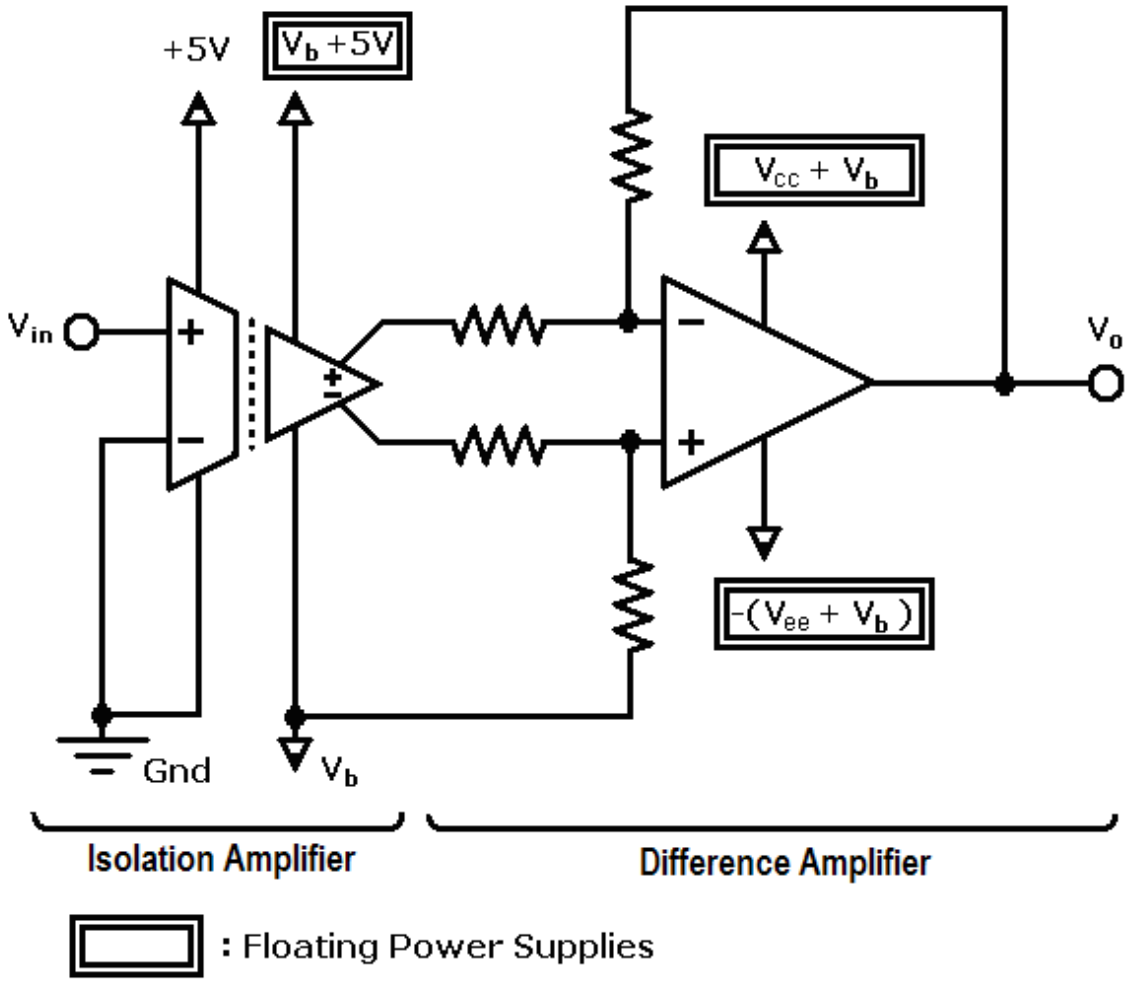


Figure 2.3 Isolated floating difference amplifier (IFDA)

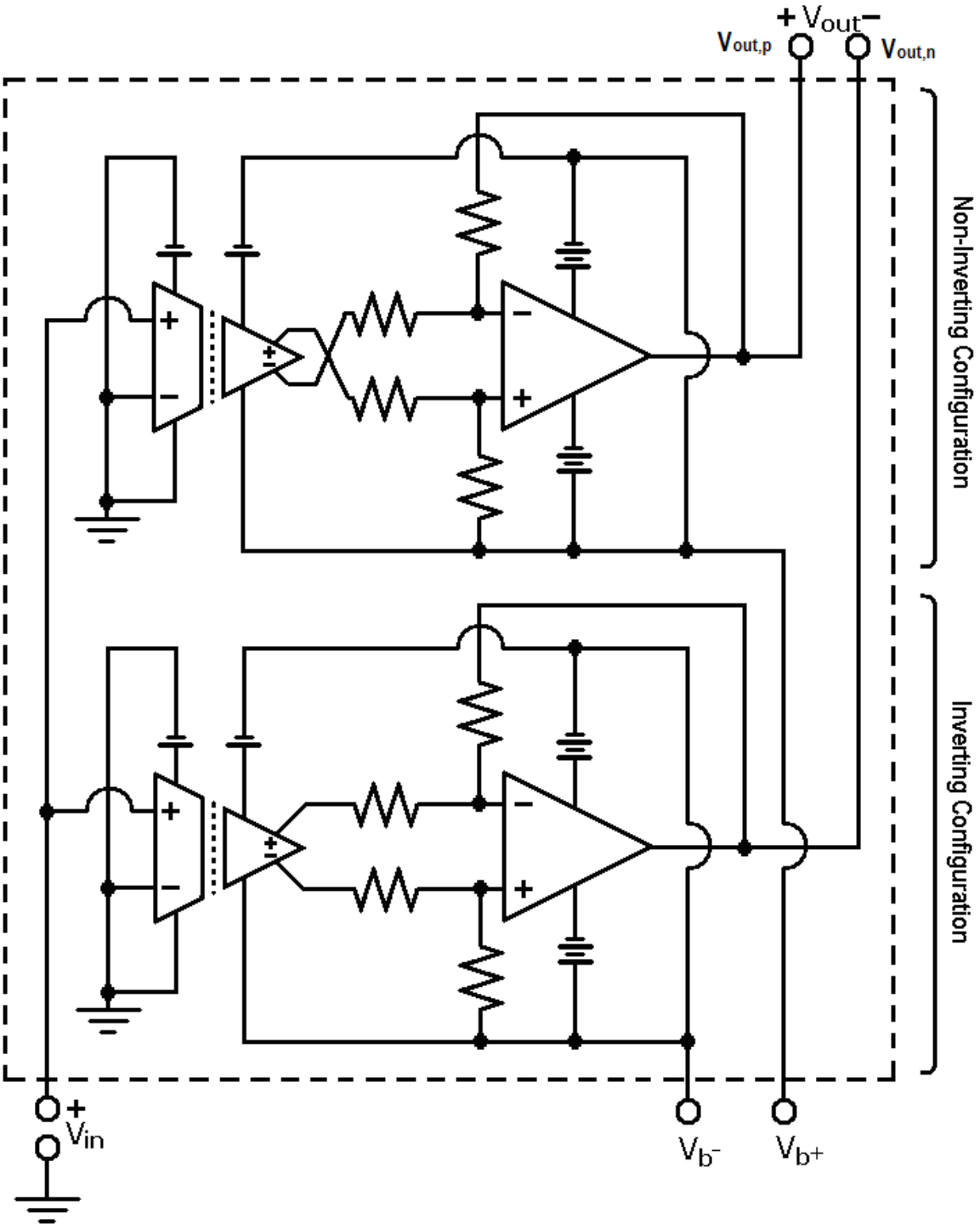
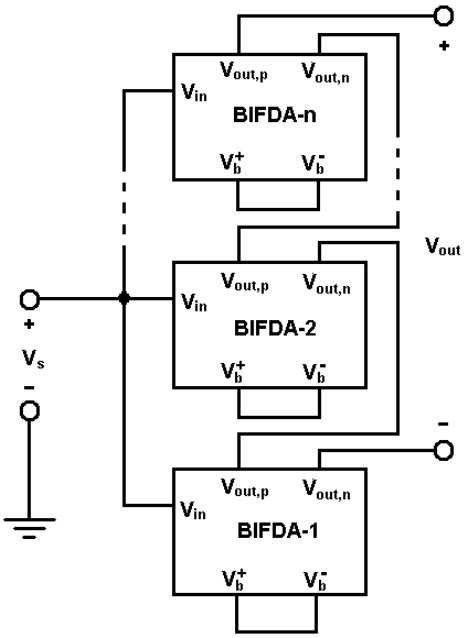
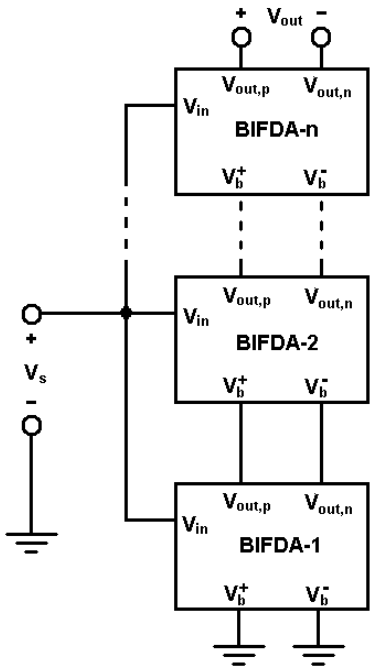


Figure 2.4 BIFDA in direct-floating cascaded topology

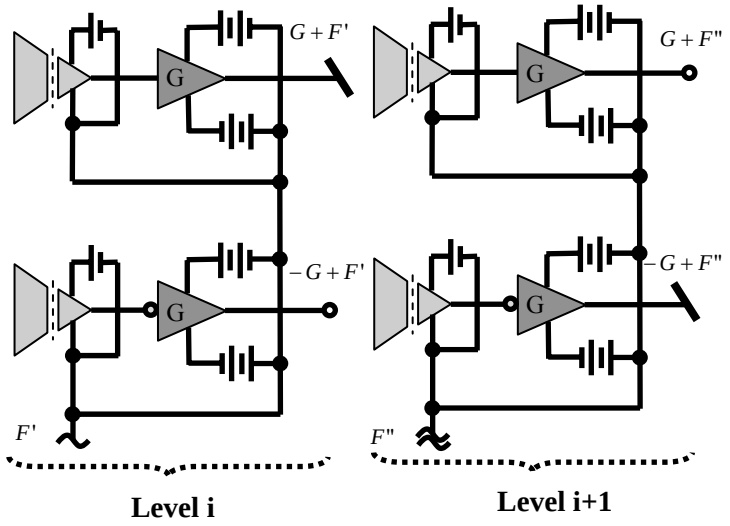


(a)

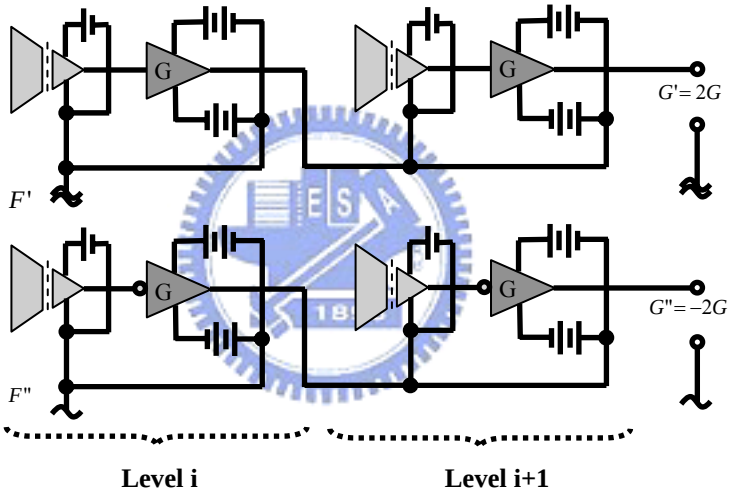


(b)

Figure 2.5 Multi-level floating amplifier (a) Indirect-floating cascaded topology (b) Direct-floating cascaded topology



(a)



(b)

Figure 2.6 Gain principle of multi-level floating amplifier (a) Indirect-floating cascaded topology (b) Direct-floating cascaded topology

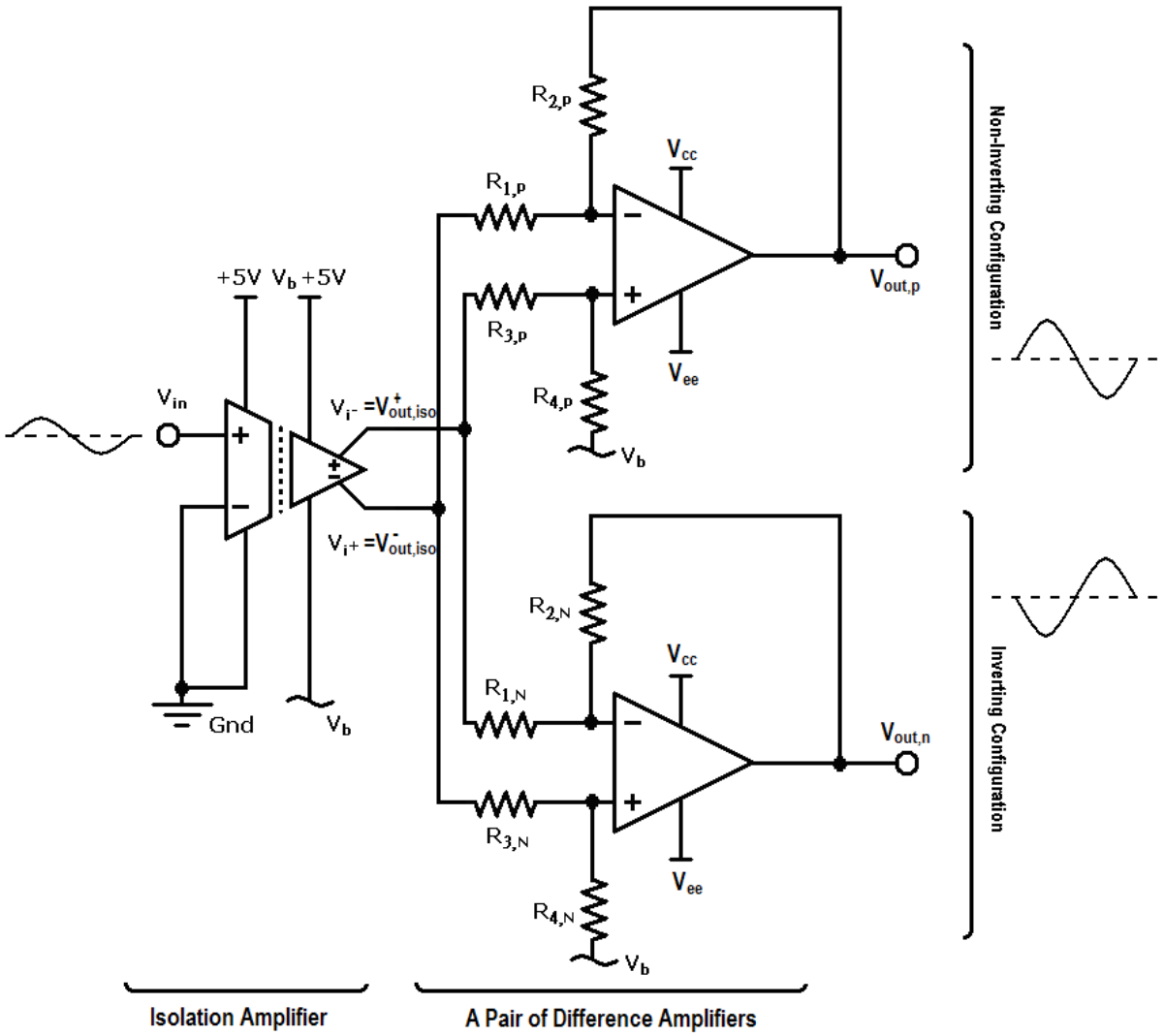


Figure 3.1 BIFDA module in indirect-floating cascaded topology

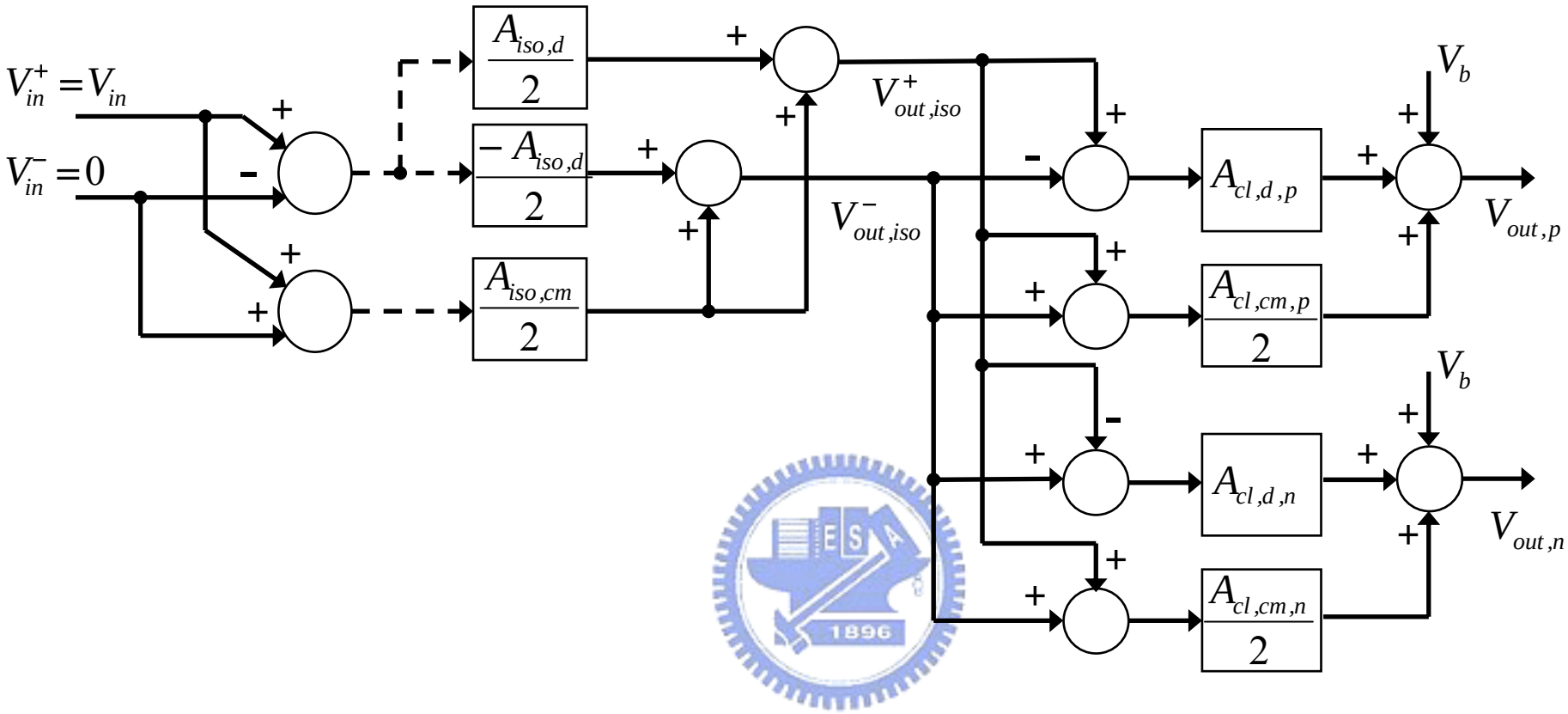


Figure 3.2 Flow path of multi-level floating amplifier in indirect-floating cascaded topology

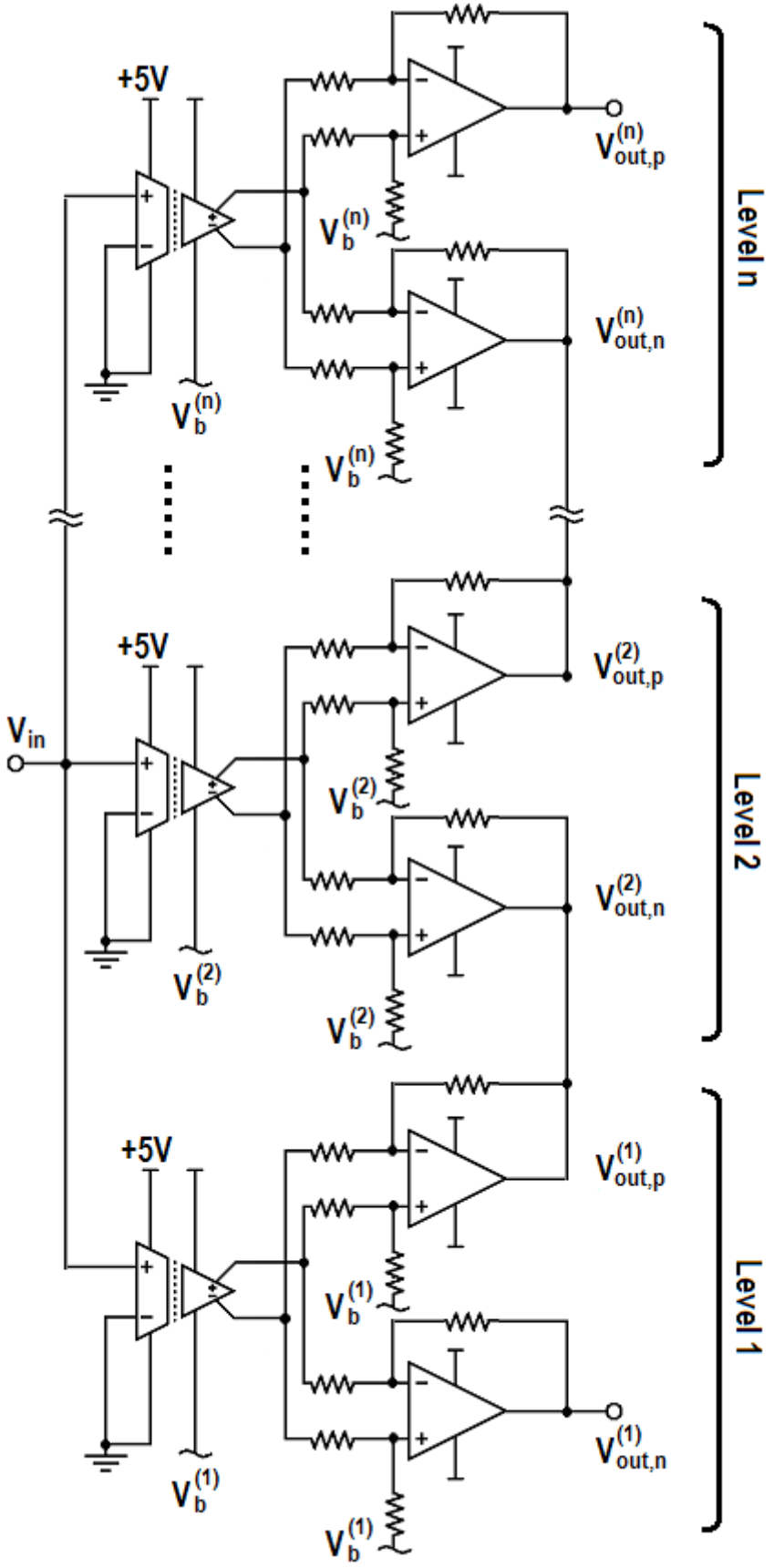


Figure 3.3 MBIFDA in indirect-floating cascaded topology

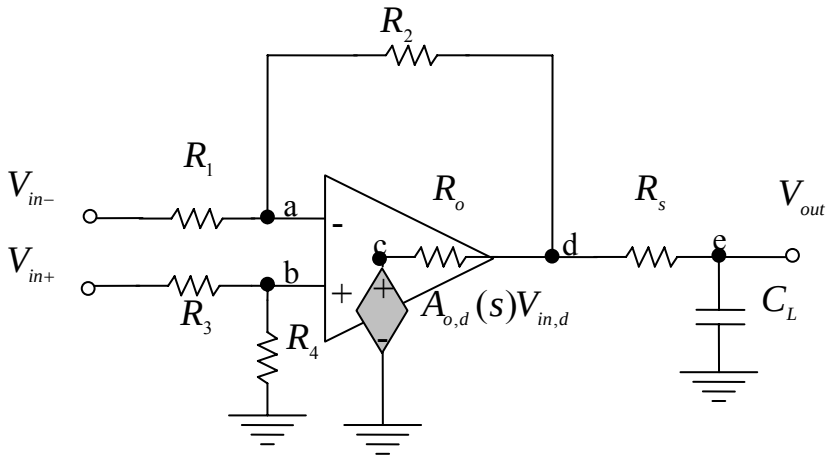


Figure 3.4 Equivalent circuit of the difference amplifier with nonzero output resistance and capacitive load.

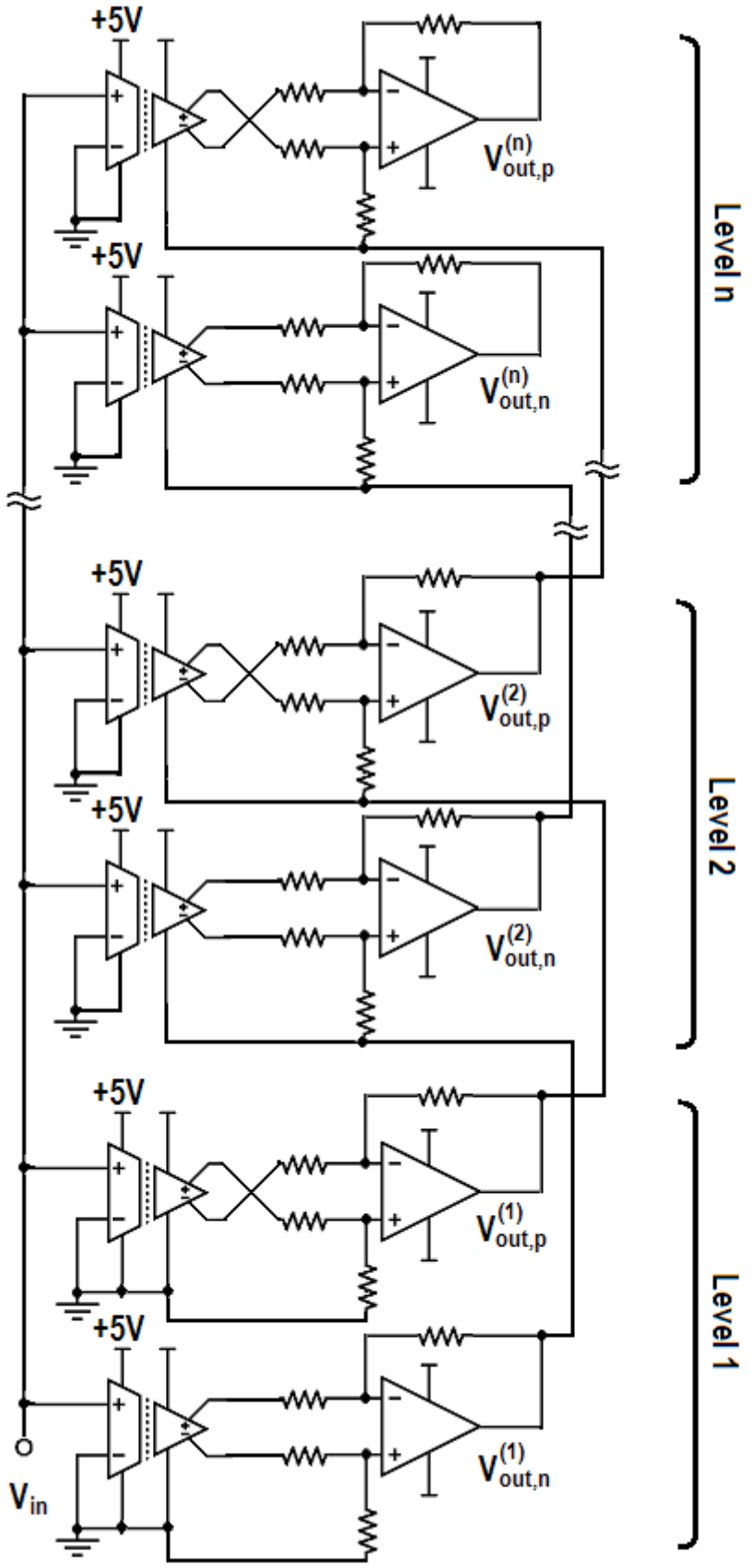


Figure 4.1 MBIFDA in direct-floating cascaded topology

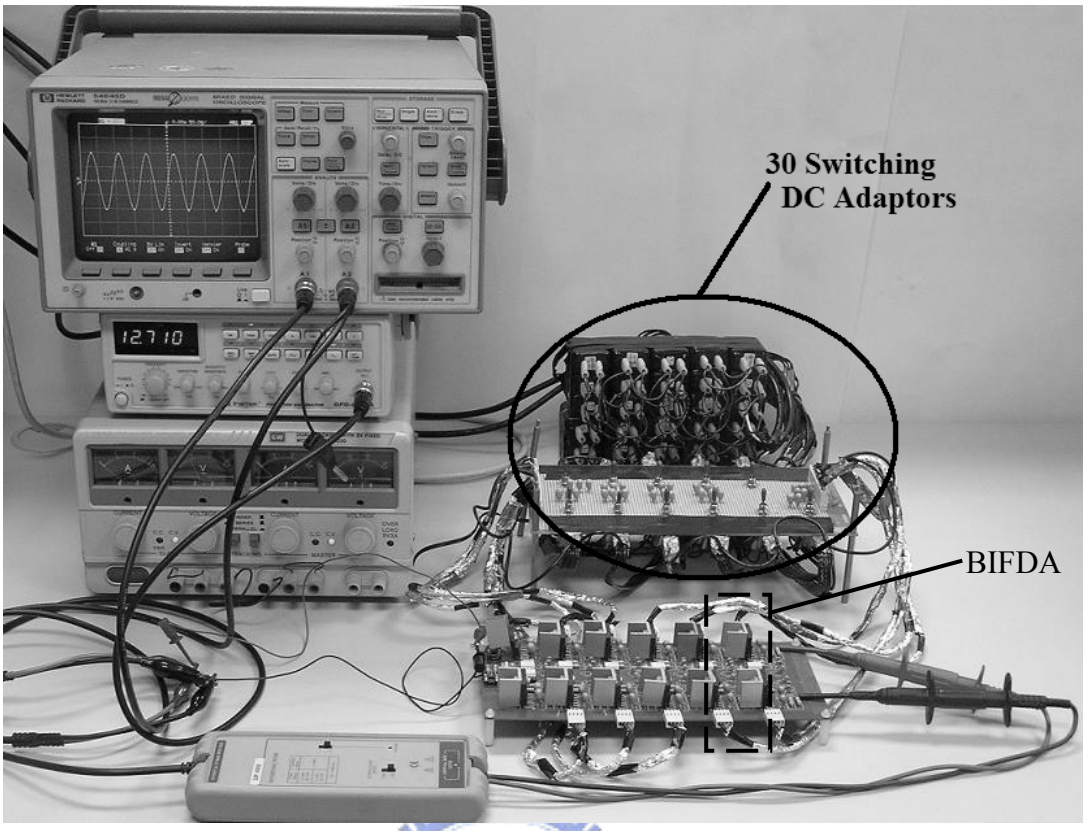


Figure 5.1(a) Experimental setup of direct-floating cascaded topology

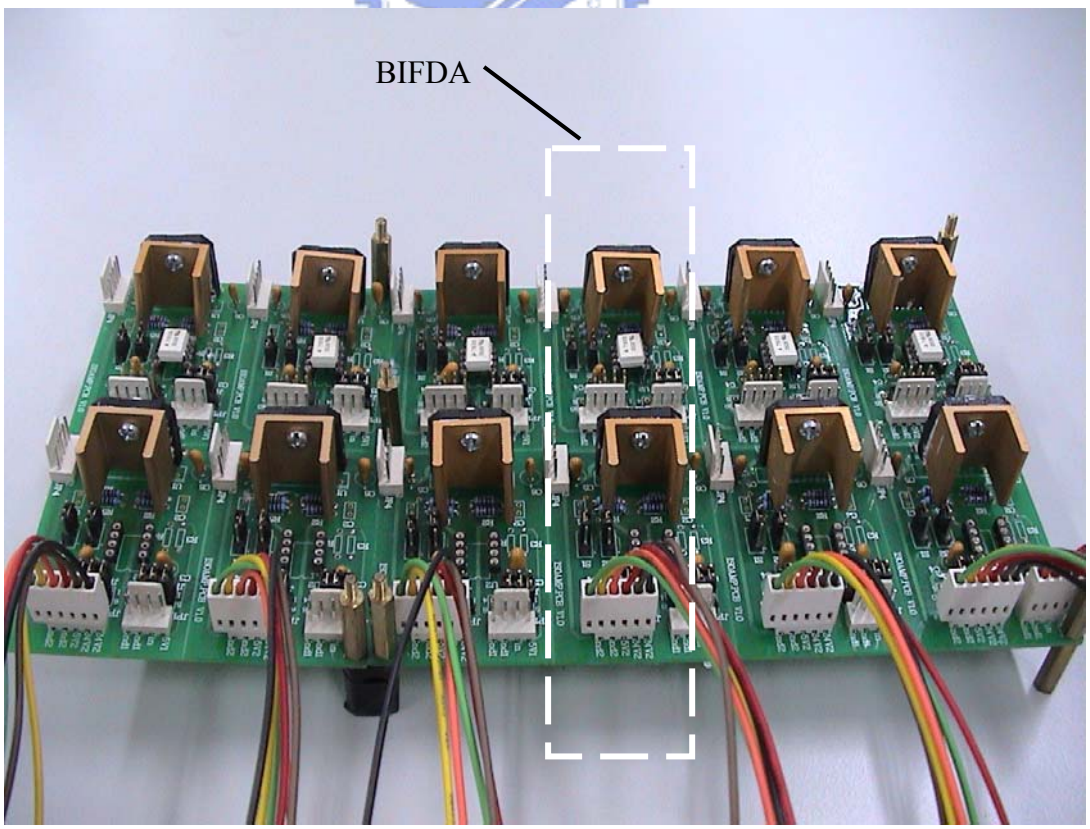


Figure 5.1(b) Experimental setup of indirect-cascaded topology

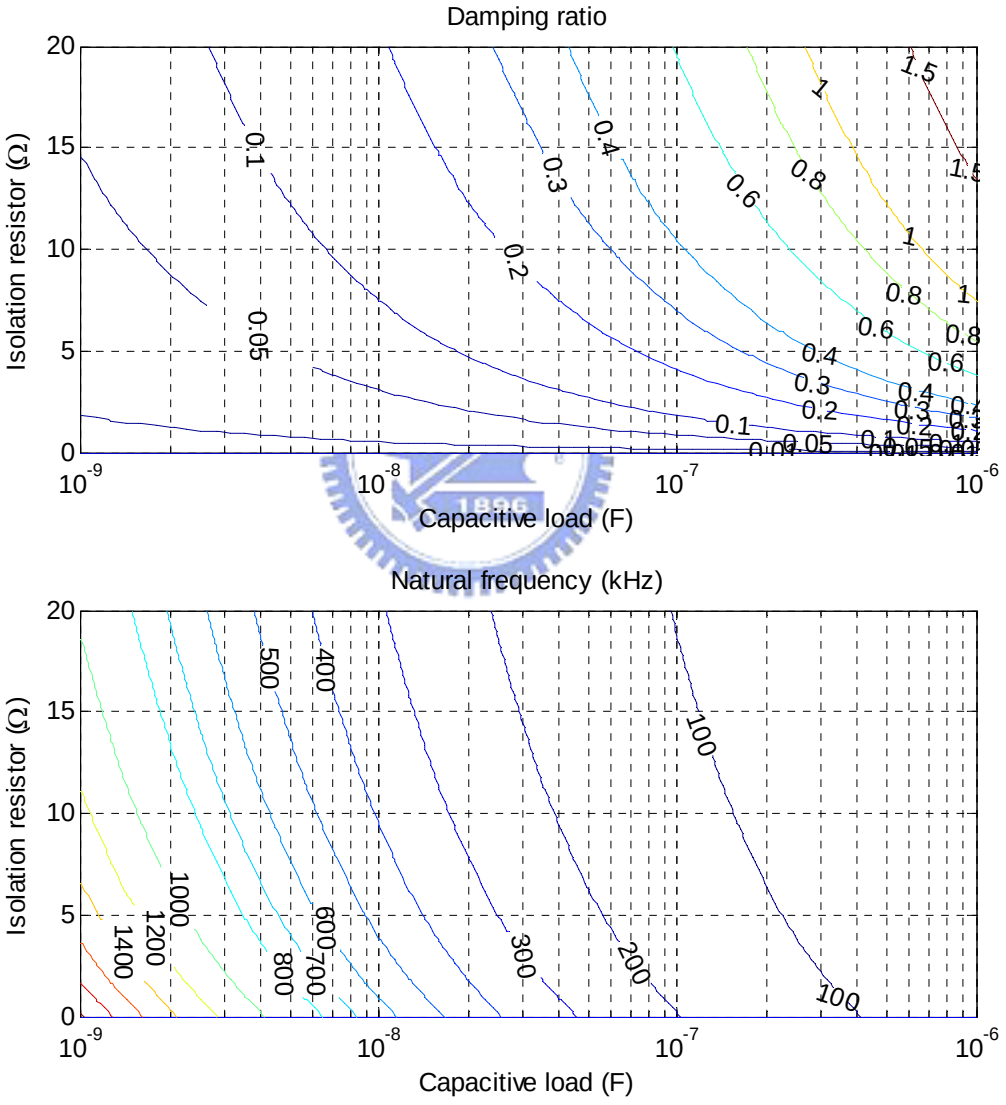


Figure 5.2 Contour plots of the damping ratio and nature frequency

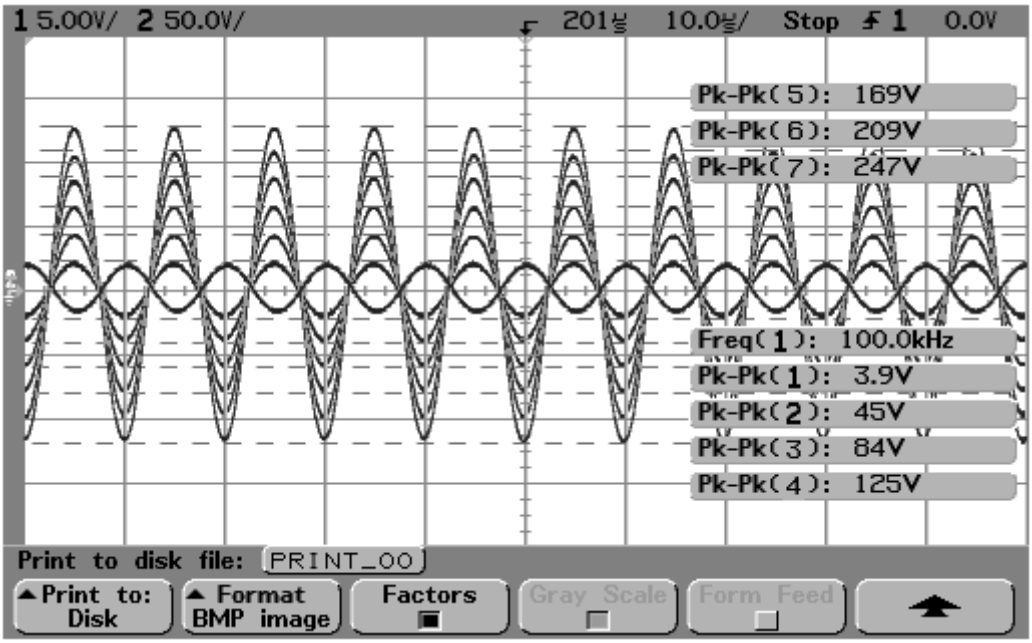
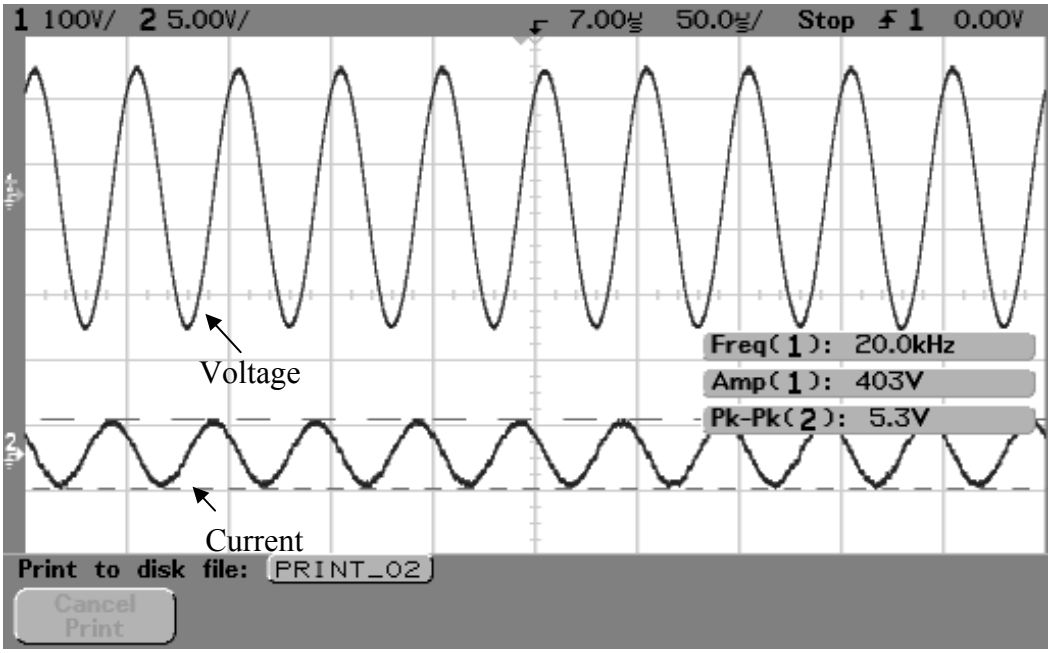
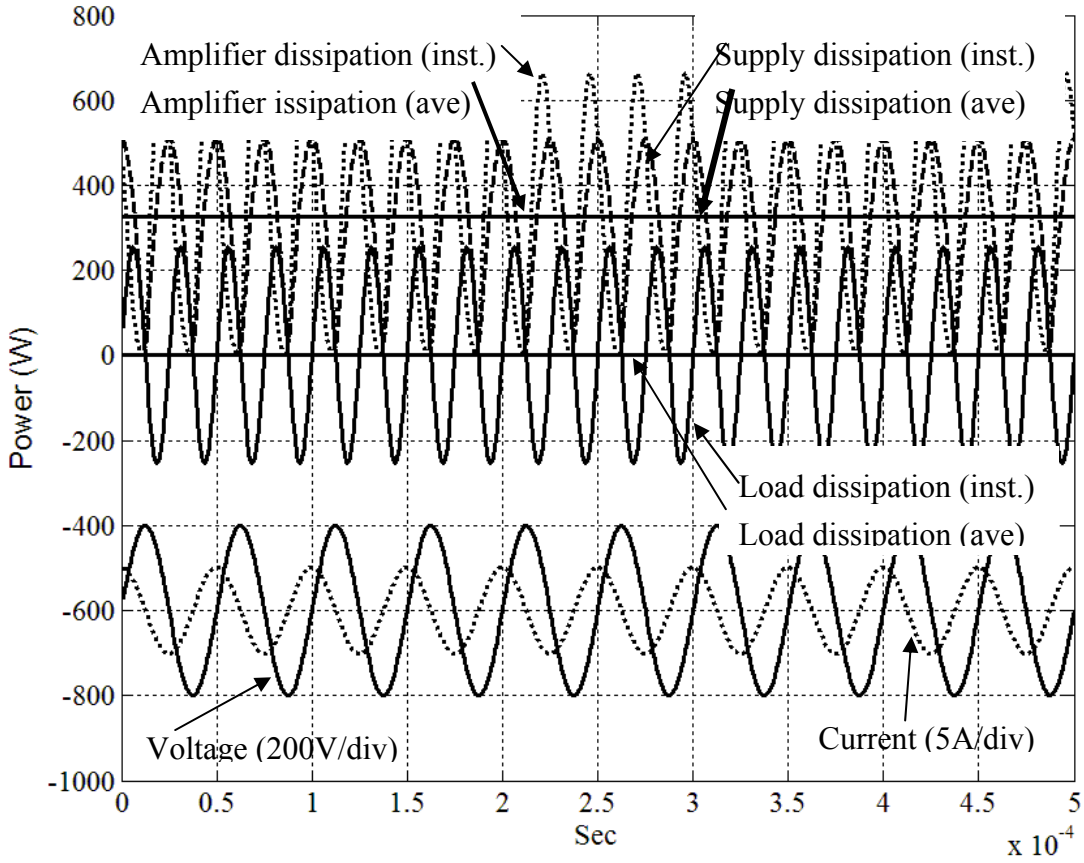


Figure 5.3 Input and output signals of each level in six-level amplifier

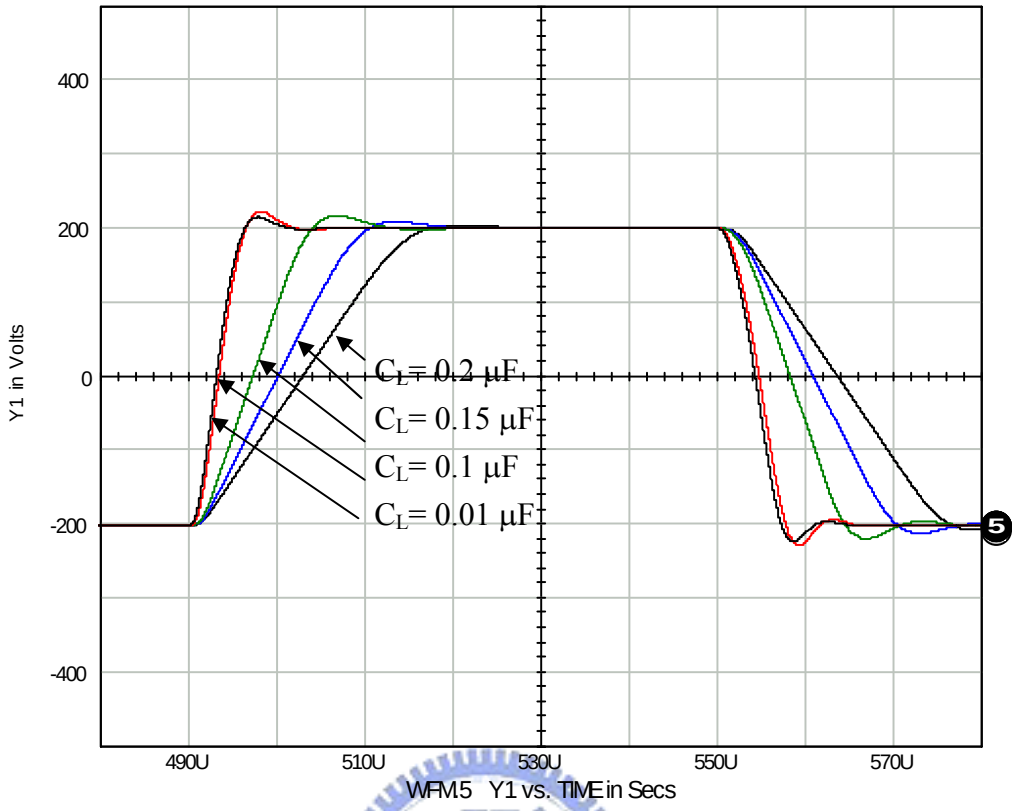


(a) Time response

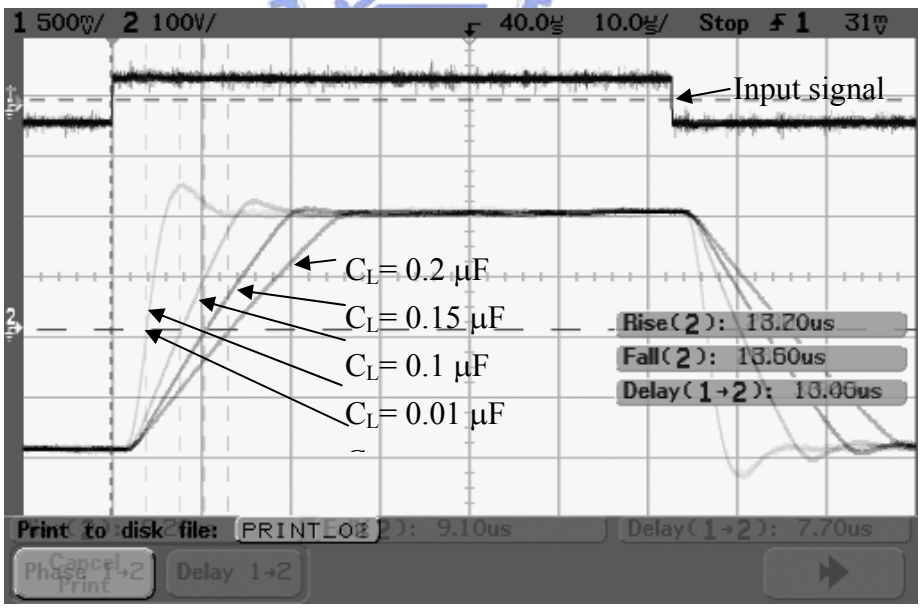


(b) Power dissipations

Figure 5.4 Six-cell amplifier based on the 20 KHz sinusoidal input signal

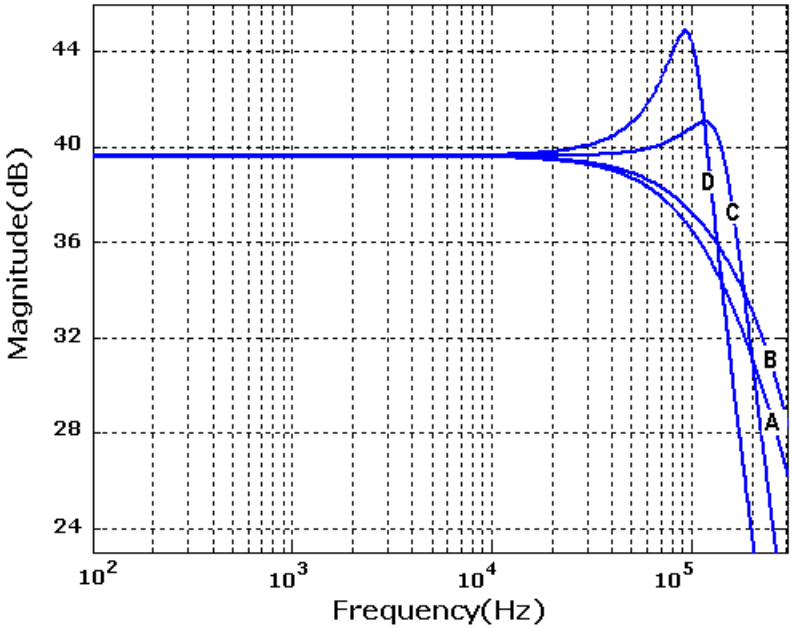


(a) IsSpice analysis results

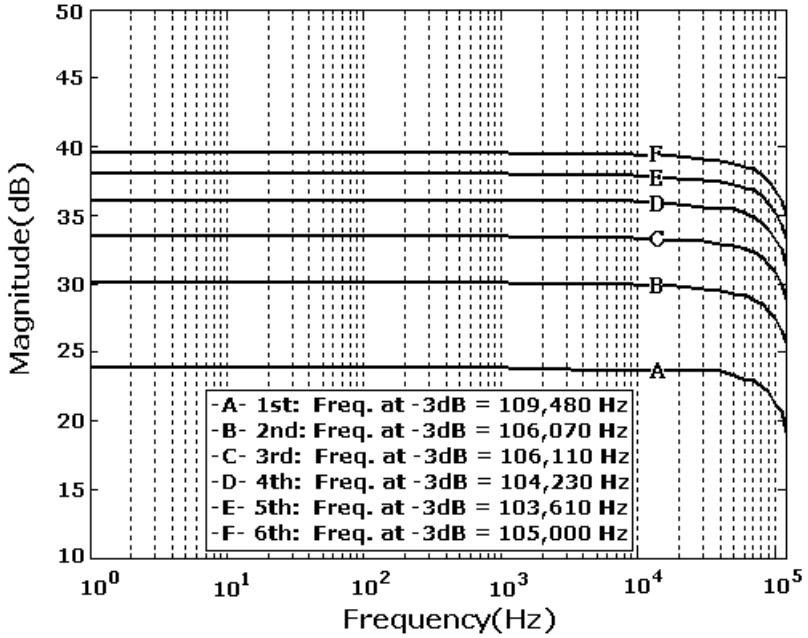


(b) Experimental results

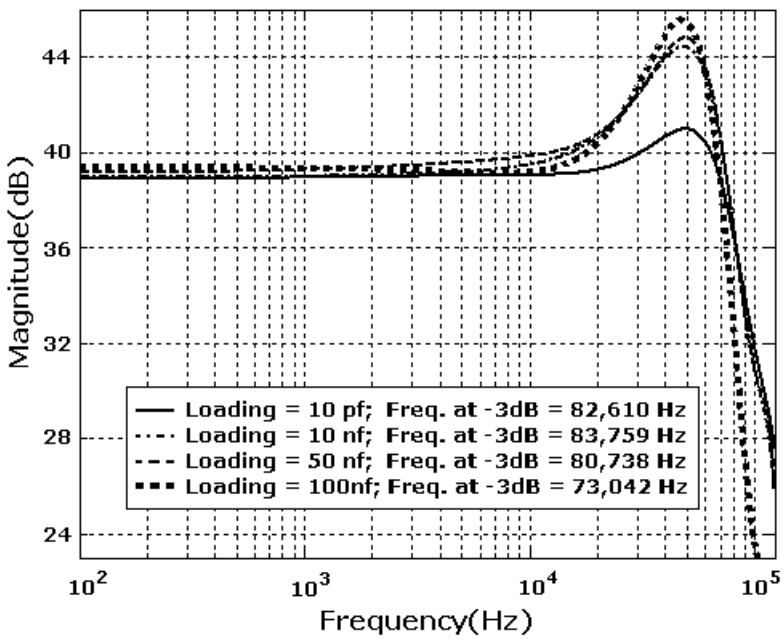
Figure 5.5 Rise and fall times of the six-level amplifier under various capacitive loads.



(a) Matlab® simulation (A) C_L = 10pF, (B) C_L = 10nF, (C) C_L = 50nF, and (D) $C_L = 10^2$nF

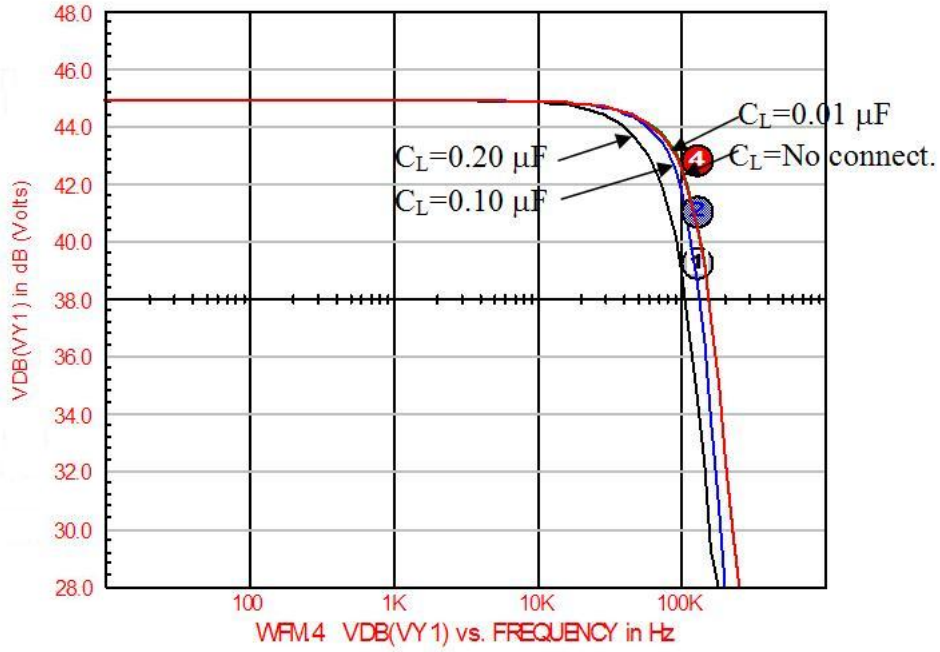


(b) Experimental results: outputs on individual levels of MBIFDA based on the zero loading test

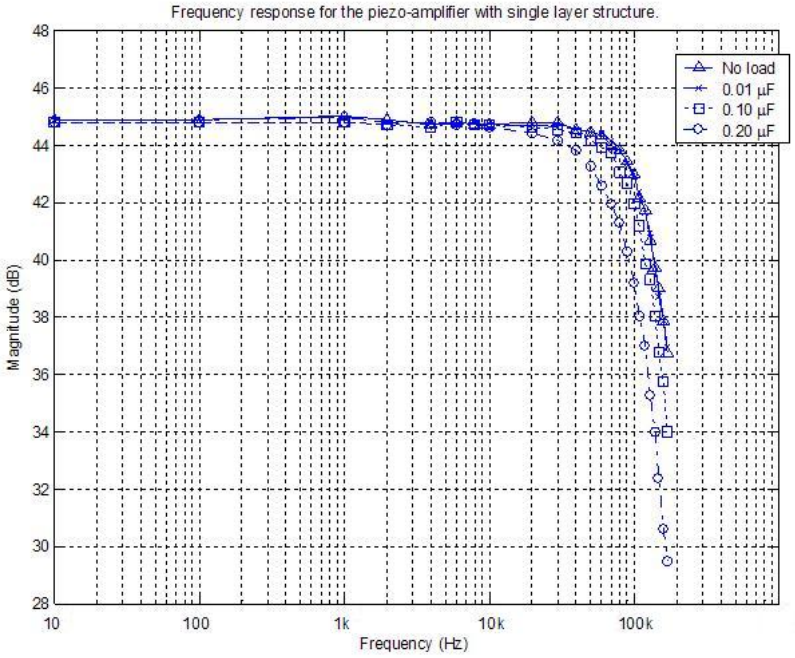


(c) Experimental Result: frequency responses based on difference capacitive loadings

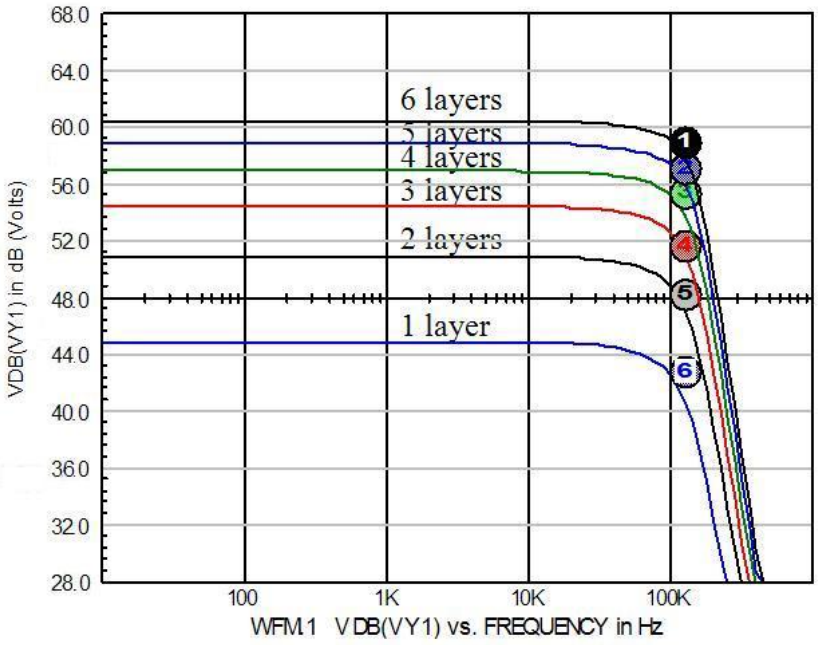
Figure 5.6 Frequency response of direct-floating cascaded circuit topology without external/isolated resistance in six levels.



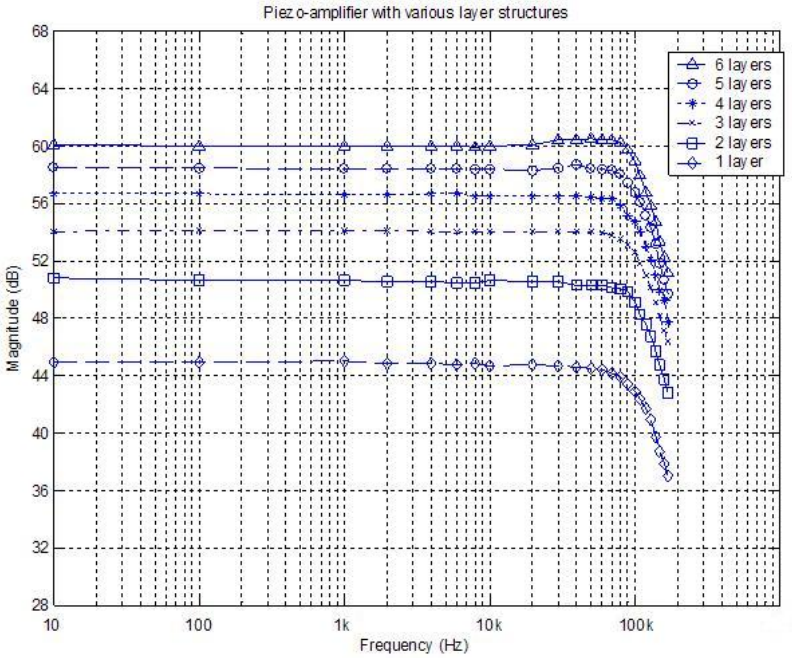
(a) IsSpice analysis results of one level based on difference capacitive loadings



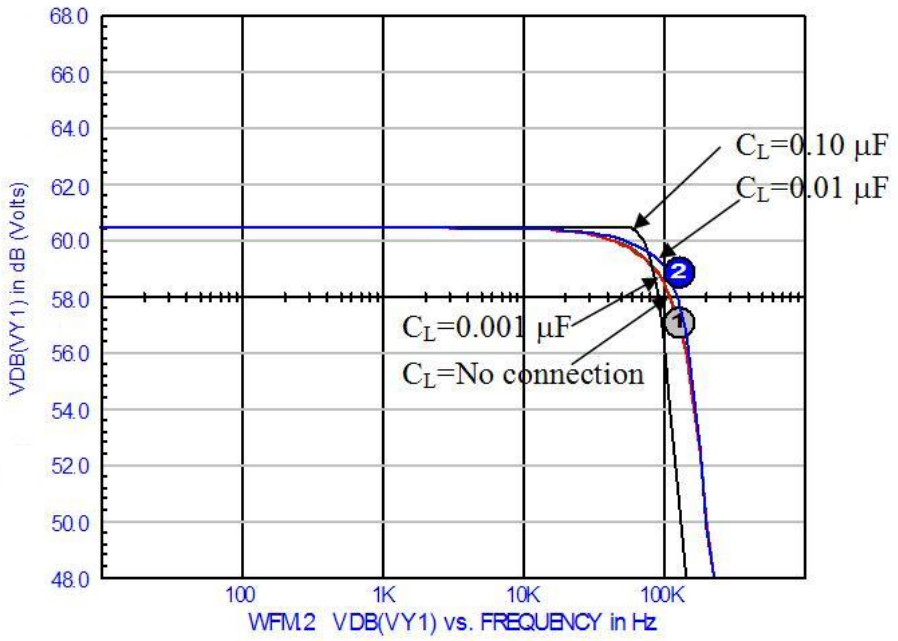
(b) Experimental results of one level based on difference capacitive loadings



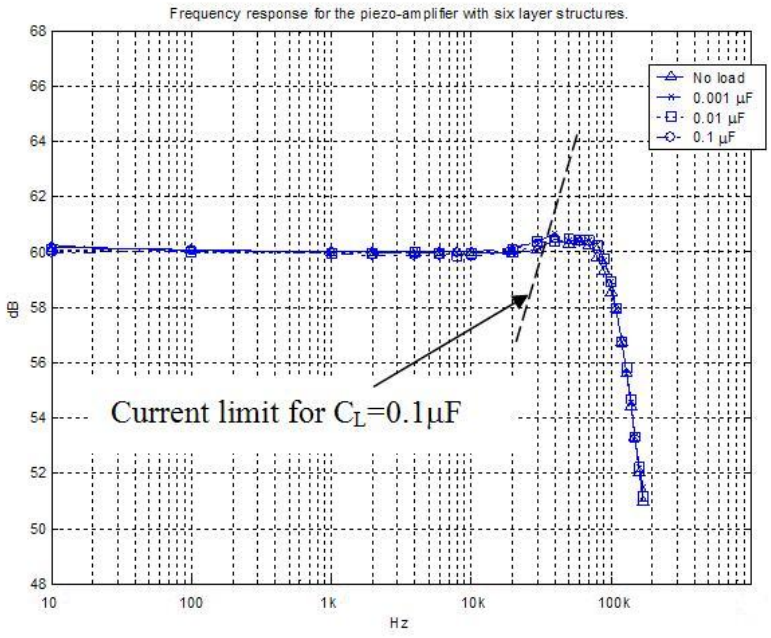
(c) IsSpice analysis results on individual level based on the zero loading test



(d) Experimental results on individual level based on zero loading test



(e) IsSpice analysis results of sixth level based on difference capacitive loadings



(f) Experimental results of sixth level based on difference capacitive loadings

Figure 5.7 Frequency response of indirect-floating cascaded circuit topology with external/isolated resistance

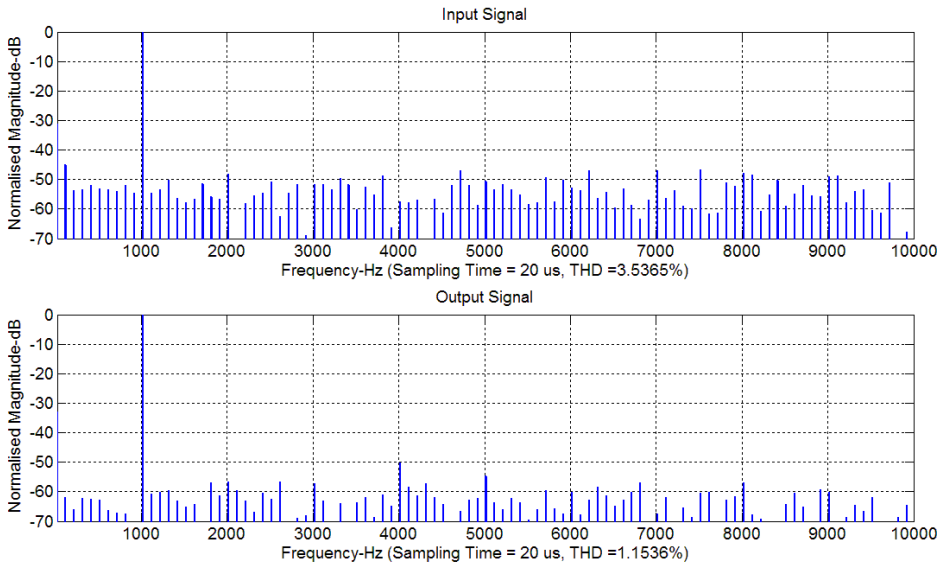


Figure 5.8 Line spectrum of input and output signals

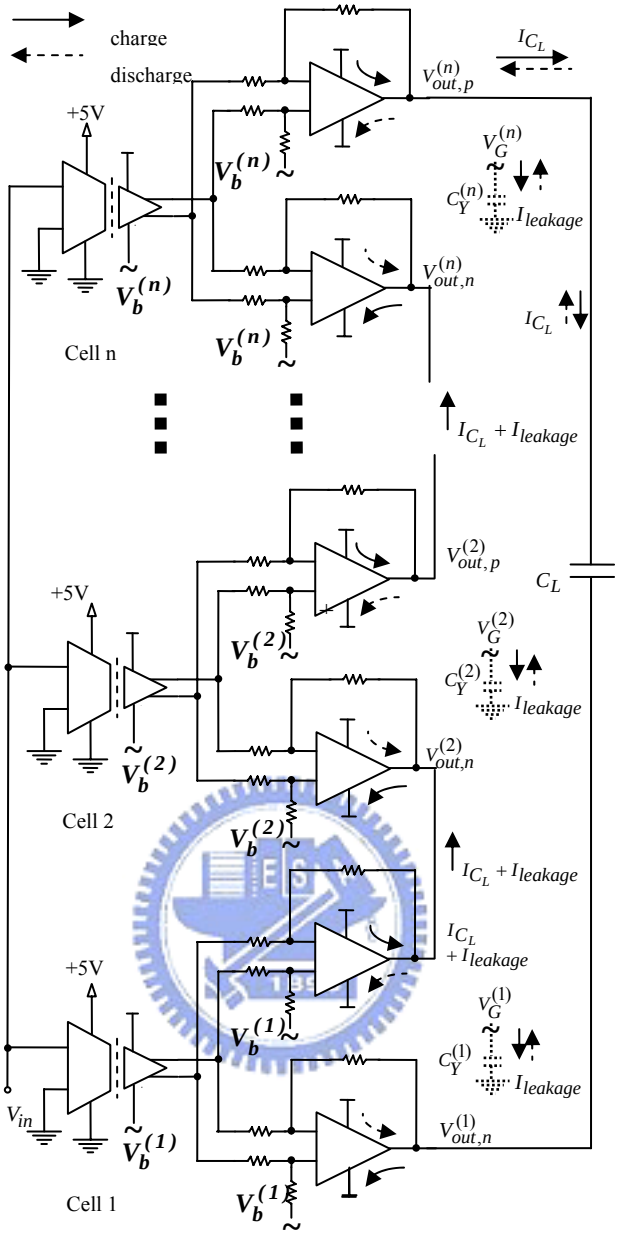


Figure 5.9 Leakage currents due to the primary-to-second capacitances of the isolated power supply units.

本論文作者已發表的著作

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1. Yung Cheng Tung, Wei-Hua Chieng and Shr Wai Ho, “The Controllable Ball Joint Mechanism,” *JSME International Journal, Series C,* Vol. 49, No.4, 2006. pp.1151-1158.

2. Yung-Cheng Tung, Shyr-Long Jeng and Wei-Hua Chieng, “Multi-level Balanced Isolated Floating Difference Amplifier,” *IEEE Transactions on Circuits and Systems I,* accepted in December 2007.

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1. 童永成，黃志方，陶吉文，成維華，”機載合成孔徑雷達支天線控制與運動補償”，第十三屆國防科技學術研討會，Oct. 14-15, 2004, pp. 365-376.

2. 鄭時龍，童永成，黃旭生，”WinCE 嵌入式系統於變頻式電動跑步機之開發”，*中國機械工程學會第二十二屆全國學術研討會*，B6-009，Nov. 25-26, 2005.