國立交通大學

電子物理系碩士班

碩士論文

氟氮離子摻雜應用於金屬閘極與高介電常數絕緣層之低溫多晶矽薄膜電晶體

Impact of Fluorine and Nitrogen Implantation on LTPS TFTs with Metal Gate and High-k Dielectric

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本校電子物理系 楊宗諭 君，學號 9421513

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口試委員： 陳振芳 簡昭欣

趙天生 林孝義

指導教授： 趙天生

系主任： 陳振芳 教授

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氟氮離子摻雜應用於金屬閘極與高介電常數絕緣層之低溫多晶矽薄膜電晶體

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摘要

在本論文中，我們利用低溫製程(< 600^{o}C)，在多晶矽中使用離子佈植引入氟(fluorine)，氮(nitrogen)離子，控制其濃度與能量的離子佈植，再搭配後閘極製程，覆蓋高介電常數閘極絕緣層二氧化鉿(HfO_2)與金屬閘極，成功的製作具有出色次臨界擺幅(sub-threshold swing)的低溫多晶矽薄膜電晶體(LTPS TFTs)的元件。我們首先使用正偏壓溫度不穩定(Positive Bias Temperature Instability)的量測方法，去找出最佳能量以及劑量的元件，期望在最佳缺陷覆蓋的情況下，與沒有經過離子佈植的元件做比較。

在找出最佳能量與劑量的元件後，我們使用熱載子(Hot Carrier Stress)量測方法，驗證了氟與氮在汲極端的接面缺陷覆蓋的能力，以及同時也發現了使用電子槍(e-gun)製作的二氧化鉿，在抵抗熱載子破壞時表現較差，在熱載子方法後的量測發現有閘極漏電，表示熱載子在二氧化鉿內形成嚴重的缺陷，促使電子有漏電路徑，而有氟的摻雜的元件閘極漏電較低，由於氟離子擴散進入二氧化鉿修補大部分缺陷，且同時熱載子也不易打斷有氟離子的鍵結，因此在缺陷捕捉相關的參數-臨界電壓變動，具有較小的變化量。

在熱載子效應後，接著進行正偏壓溫度不穩定的量測方法，從隨時間變動的臨界電壓(threshold voltage)以及次臨界擺幅，發現臨界電壓的變動趨勢與臨界擺幅變動趨勢不符合，表示二氧化鉿的原生缺陷補捉是造成臨界電壓變動的主因，而臨界擺幅的變動也可得知有氟，氮處理元件具有比較好的介面可靠度。之後，進行了升溫量測，由升溫後的轉換特性曲線也可以說明氟離子具有較好的汲極端缺陷控制能力，使得熱電子激發(thermionic emission)產生的漏電流較少，再從升溫前後的臨界電壓的表現可以得知，由於溫度使得捕捉電子更容易被釋放，因此推測有摻雜氟的元件其通道以及閘極絕緣層中間的介面氧化層較薄，使得捕捉電子容易在高溫的情況下逃脫。

Impact of Fluorine and Nitrogen Implantation on LTPS TFTs with Metal Gate and High-k Dielectric

Student: Tsung-Yu Yang **Advisor: Dr. Tien-Sheng Chao**
Department of Electrophysics
National Chiao Tung University

Abstract

In this thesis, fluorine and nitrogen ions with different dosage and energy were implanted into polycrystalline silicon of thin film transistor with the gate-last process in all low temperature process < 600°C. After deposition of HfO_2 high-k gate dielectric and metal gate, the Low-Temperature-Poly-Si Thin Film Transistors which have excellent sub-threshold swing were fabricated. In order to find out the best device with proper implant dosage and energy, we use the method of positive bias temperature instability, which could help us to find out the best defect-passivation condition.

After finding out the best implant dosage and energy conditions, hot carrier stress method was used to qualify the fluorine and nitrogen passivation ability in the drain-side junction. It is found that the gate dielectric HfO_2 which fabricated by the e-gun exhibited the worse performance to resist the hot carrier damage. After stress, transferred curves show serious gate leakage, which means hot carriers create damage inside the HfO_2, resulting in a path for electron to tunnel through gate dielectric. It is found that a lower gate leakage current was found in the F-implanted devices, which maybe due the passivation of defects by fluorine. On the other hand, strong Si-F bonds exhibit good resistance to hot carrier, causing less threshold voltage shift which is strongly defect-related.

After hot carrier stress, devices were evaluated by using positive bias temperature instability test. With different trends in the time evolution of threshold voltage shift and sub-threshold swing degradation, it is found that electron trapping in the HfO_2 is the major reason for the threshold voltage variation. Compared to control devices, devices with fluorine and nitrogen exhibit good passivation at the interface. Devices were measured at an elevated temperature. The transferred curves measured at higher temperature show that fluorine implantation reduces the thermionic emission current at the drain junction. Finally, from the shift of the threshold voltage, it is found that the electron trapping in the HfO_2 could easily be de-trapped at high temperature. This can be explained by that interfacial oxide layer between gate dielectric and channel can be suppressed with F-incorporation, so that trapping electrons could easily escape at high temperature for devices with F-incorporation.

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在此，把本論文獻給我的家人

楊宗諭

于新竹交大

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Table Captions

Figure Captions

Chapter 1 Introduction

1.1 Overview of Poly-Si Thin-Film Transistor (Poly-Si TFT)

Since the first Polycrystalline-Silicon Thin Film Transistor (Poly-Si TFT) was published by C.H.Fa et al.[1] in 1966, it attracted most of the scientists who work in the Panel Display. Therefore, many researches devoted themselves on how to improve the performance of TFT has been started at that time. TFTs also play lots of roles in the panel industry, like Active Matrix Liquid Crystal Display (AMLCD)[2, 3], Static Random Access Memory (SRAMs)[4, 5], Electrical Erasable Programming Read Only Memories (EEPROM)[6, 7], etc. And among theses applications, the application of active matrix liquid crystal display was the major driving force to promote the developments of Poly-Si TFTs technology.

For the skills in the prior art in TFTs, it is well know that amorphous silicon had been a popular material to be used to fabricated on TFTs in AMLCD, due to its compatibility with low processing temperature on large-area glass substrate. However, there existed a disadvantage with its low electron mobility (<1 cm^2/V$_s$), which hard to realize the integration of the switching pixels with the peripheral driver circuit on the same substrate to further reduce the prime cost. Recently, one solution have developed to over come the tough problem above described is to use polycrystalline silicon to be use as the channel film, due to its electron mobility higher than amorphous silicon. On the other hand, poly-Si TFTs plate also have higher panel resolution than amorphous-Si one, because it has larger aperture ratio in each pixel. Thus, how to improve the performance of poly-Si TFTs is the most important issue so as to realize the concept of System-On-Panel (SOP) [8].

With equal requirement of electrical characteristic to MOSFETs, TFTs also work hard to achieve high driving current, low leakage current, low threshold voltage and low sub-threshold swing.

To improve leakage current, there exist two ways to approach. First of all, we need to know various leakage mechanisms, like space-charge limited flow of hole from source to drain, thermal emission of carriers via grain boundary traps in the depletion regions, parasitic bipolar effect, impact ionization in the drain depletion region, band-to-band tunneling in the depletion region, and field emission via grain boundary traps[9]. Therefore, one of the problems is the large electric field across gate dielectric between gate and drain electrode when biasing gate voltage at leakage current region, and the other one is lots amount of defect states in grain boundary in the drain side junction.

Several novel device structures have been reported to reduce the leakage current with the approach of reduce the electric field between gate and drain electrode. Past lectures show these technologies that including Lightly Doped Drain (LDD) structure[10-12], source overlap and drain offset structure[13-15], Field Induce Drain (FID) structure[16], N-P-N gate structure[17], Floating Sub-Gate Structure with using photoresist reflow[18, 19], Air Cavity structure[20], High-k Spacer Offset-Gated structure[21], Vertical Bottom-Gate Structure[22], Gate Overlapped LDD (GOLDD) structure[23-25], Amorphous Silicon Buffer structure[26, 27], and T-gate Technology[28].

Except for using new structures, reducing defect states in grain boundary is also an important method. As we know, defect states in the grain boundary or in the interface between gate dielectric and channel serve as the trapping centers. Since free carrier be trapped in the trap sites, they will not contribute to the conduction current and will generate potential barriers to degrade the performance of the TFTs. In order to reduce the defects and defects related grain boundary, some effective treatment methods have been reported to enlarge grain size and passivate the defects. First, amorphous-silicon can be crystallizes to polycrystalline silicon typically via SPC(solid phase crystallization)[29], ELA(excimer laser annealing)[30, 31] and MILC(metal-induce lateral crystallization) [32]. Each of above method has its advantages and disadvantages. Besides, in order to passivate the defect states, introducing ions to bonding with defects have several technologies been reported, that including plasma treatment[33-40], solid phase diffusion[41], and ionic implantation[42-47], etc. As the trapping centers decrease, it will also help to increase the efficiency of free carriers contributed conducting current.

1.2 Recent High-k Dielectric

Furthermore, to improve the driving current and to have better sub-threshold swing, high-k gate dielectric is one of the solutions. There are many kinds of the candidate materials to alter the SiO_2, due to the trend of scaling down length of device, which accompany with thinner dielectric thickness. High-k insulator can be deposited physically thicker for the same equivalent electrical oxide thickness (EOT), thus offering significant gate leakage current reduction, as demonstrate by several groups [48].

In the past studies, several new high-k gate dielectric materials, like Al_2O_3 and Ta_2O_5, were suggested to increase gate capacitance density so as to improve the mobile carrier density in the channel region. However, the k value of Al_2O_3 is 9~10 and is not high enough, and the improvement of the device performance is not apparent[49]. On the other hand, it is necessary to use a thick Ta_2O_5 as the gate dielectric in TFTs to reduce the gate leakage current, due to its narrow band-gap[50] . Therefore, the increase of gate capacitance density is limited.

Consequently, Hafnium-oxide based materials, such as HfO_2, $HfSi_xO_y$, HfO_xN_y and $HfSi_xO_yN_z$, have been provided with some better characteristics, that including high-permittivity, wider band-gap, and superior thermodynamic stability on silicon[48]. Recent researches show that only replacing gate insulator may not sufficient for device scaling, because poly-depletion effect can not be ignore for the sub-2-nm evolution any more. Besides, temperature for the dopant activation in the poly-Si gate electrode is always higher than the melting point of the glass substrates, which is not suitable for the applications of panel industry. By the way, metal gate does not need dopant activation process, and therefore to combine metal gate with HfO_2 will have the greatest potential for the future CMOS technology[48].

These years, some reports had showed that high-k insulator used on poly-Si TFTs. Not only for using in peripheral integral circuits TFTs[51], but also using in the (Silicon-Oxide-Nitride-Oxide-Silicon) SONOS-Type memory of TFTs[52, 53]. As long as TFTs combine with high-k dielectric, some excellent device performances can be achieved, that including high driving current, low threshold voltage, and low sub-threshold swing.

1.3 Review of Introduce Fluorine and Nitrogen

For reducing trap states in the grain boundary or in the interface, plasma treatments could easily introduce some species, like hydrogen[36], oxygen[33, 34], deuterium[35] by gas H_2, D_2, O_2. And solid phase diffusion methods also reported to introduce fluorine into poly-Si by thermal diffusion[41]. For the past reports, fluorine and nitrogen have better performances than hydrogen, and states passivated by hydrogen could easily dehydrogenate undergo an Aluminum alloy process.

Since fluorine introduces into poly-Si can achieve higher driving current, lower leakage current, steeper sub-threshold slope, and higher field effect mobility[44-46, 54], it can help to realize the ideal of transfer characteristic of TFTs. On the other hand, fluorine also passivate the deep states in the band gap of poly-Si[47], which lead to enhance better reliability. And nitrogen also has its superiority in performance and reliability in TFTs[37-40, 42, 43].

1.4 Motivation

To conclude and combine the advantage above described, we seek for poly-Si TFTs with excellent performances with lower leakage current, higher driving current, lower threshold voltage, and lower sub-threshold swing. Therefore, we take fluorine or nitrogen and high-k insulator together into TFTs processes. And for the limited of melting point of glass substrates, we need low temperature processes to be processed. Gate last process would become our choice, and detail will be discussed in the chapter 2.

In addition, long-term reliability issues are always what we concerned in Thin Film Transistor. We use the methods of Positive Bias Temperature Instability (PBTI) and Hot Carrier Stress (HCS) stressing our device. The PBTI issue earlier major appears in n-channel device due to the “ high ” state in the inverter operation in CMOS circuit. To date, PBTI also play an important role in the TFTs in the panel, which used in switching elements or in the integral circuits. To deserve to be mentioned here, we also have the same reliability problems with high-k dielectric. There will have more completed situations to be discussed in this thesis.

1.5 Organization of Thesis

In this section, I will show our research efforts. This thesis is organized as follow:

In chapter 1, the overview of Poly-Si TFTs, recent High-k dielectric, review of introduces fluorine and nitrogen, and finally motivation are described in this section.

In chapter 2, experimental process flows, and electrical parameter extraction are shown.

In chapter 3, the best implant conditions of fluorine and nitrogen within our experiments were determined.

In chapter 4, since the best fluorine implant condition will be use to compare with control sample which does not introduce fluorine. To qualify how the fluorine can strength the reliability, Hot Carrier Stress and Positive Bias Temperature Instability would be use to be our methods. For the later half of this chapter, the same methods will be to play into practice in nitrogen.

In chapter 5, at the end of this thesis, we will make conclusions and future works.

Chapter 2 Experiment Method

2.1 Device Fabrication Flow

This section, we will talk about the whole device fabrication flows. First, 50 nm undoped amorphous-Si (α-Si) was deposited on thermally oxidized Si wafer by dissociation of SiH_4 gas at 550^{o}C in a low-pressure chemical vapor deposition (LPCVD) system. Subsequently, fluorine or nitrogen ionic was introduced into α-Si film with various energies and dosages by implantation, as list in Table 2-1 and Figure 2-1. Furthermore, control sample will have identical process except for the fluorine or nitrogen implantation. After special species implantation, α-Si was taken into furnace for re-crystallization, which so-called solid-phase crystallization (SPC), at 600^{o}C for 24 hours in N_2 ambient, as show in Figure 2-2. Then, 480 nm thick SiO_2 was deposited by plasma-enhanced chemical vapor deposition (PECVD) for field oxide isolation. Next, source and drain regions inside the active region was patterned for etching oxide and to proceed to implant with phosphorous (20k eV at 5 x 10^{15} cm^{-2}) ,and next, dopant activated at 600 °C for 24 hr annealing in a N_2 ambient, as show in Figure 2-3. After dopant activation, whole active region patterned for oxide etching. Followed by standard RCA, samples deposited 50 nm HfO_2 by electron-beam evaporation system. A 400 ^{o}C 30 min furnace O_2 treatment was applied to improve the gate oxide quality. And before the TaN deposition, photoresister was coating for the lift off method. After contact etching, devices was completed by 500 nm Aluminum deposited by thermal evaporation system and etching, alloying. The overview of device was show in Figure 2-5.

Energy (eV) **Dosage (cm^{-2})**	**11k**	**20k**	**30k**
1 x 10^{13}	1F1N, 1N1N	2F1N, 2N1N	3F1N, 3N1N
1 x 10^{14}	1F2N, 1N2N	2F2N, 2N2N	3F2N, 3N2N
5 x 10^{14}	1F3N, 1N3N	2F3N, 2N3N	3F3N, 3N3N

Table 2-1 Fluorine and nitrogen implant conditions

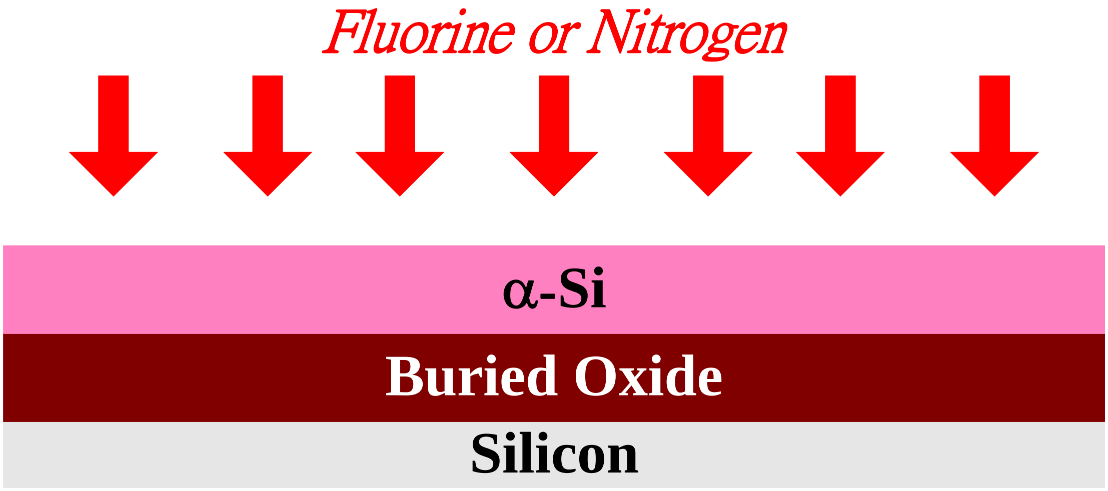

Figure 2-1 Process flow – blanket implantation with fluorine and nitrogen

Figure 2-2 Process flow – solid phase crystallization

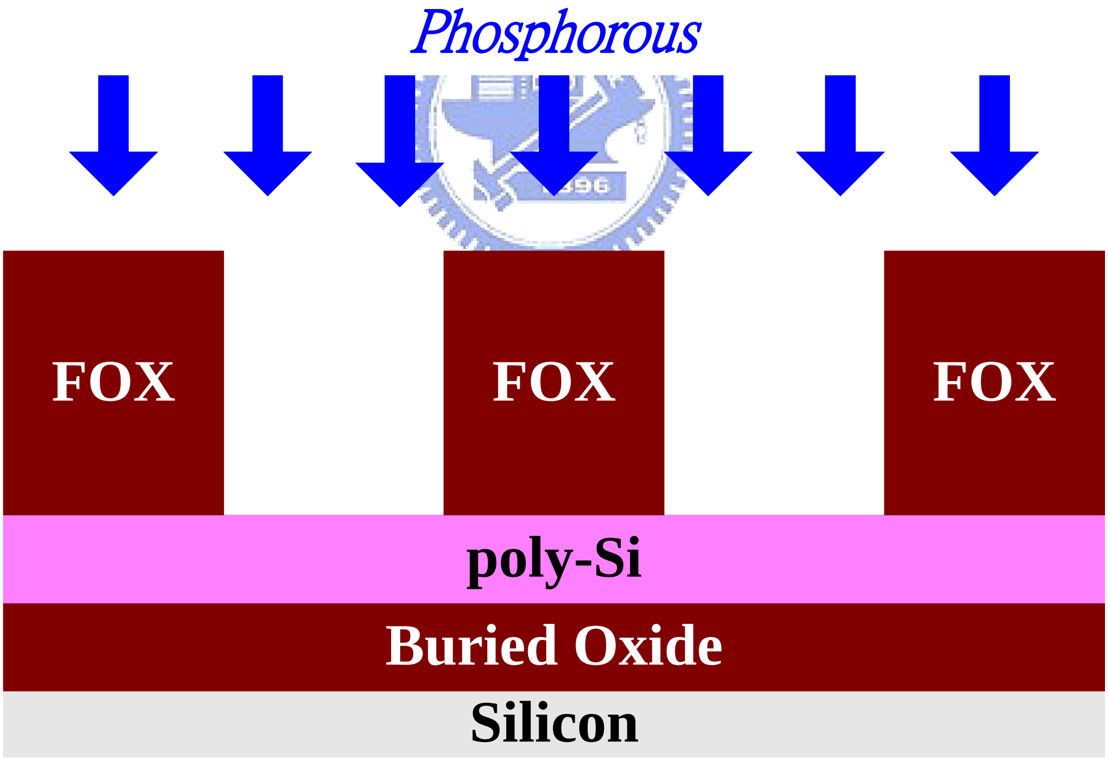

Figure 2-3 Process flow – source/drain phosphorous implantation

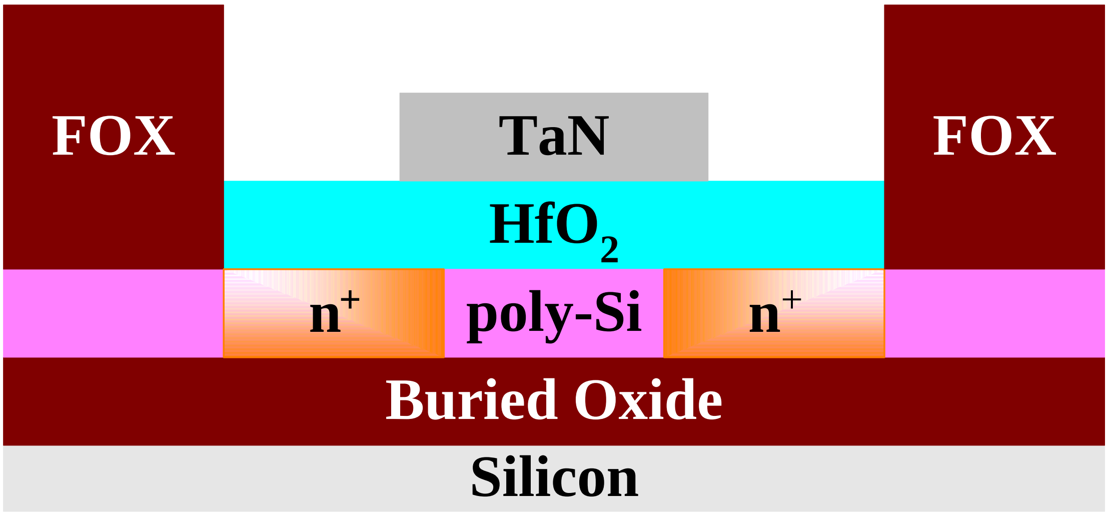

Figure 2-4 Process flow – deposited high-k and metal gate

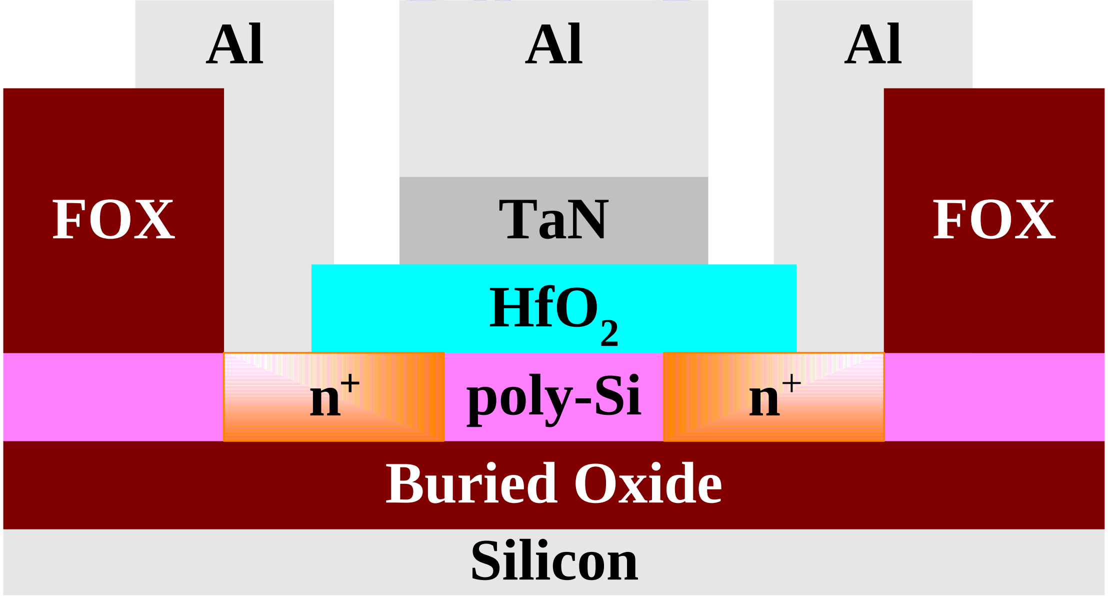

Figure 2-5 Process flow – device overview

2.2 Device Electrical Parameters Extraction

In this section, the electrical characteristics and the long-term tests for reliability of different conditions, were all measured by semiconductor characterization system - KEITHLEY 4200. Moreover, the methods of parameter extraction used in this study are described in this section. These parameters included threshold voltage (V_{th}), transconductance (G_m), sub-threshold swing (S.S.), ON current (I_{ON}), OFF current (I_{off}), ON/OFF current ratio (I_{on}/I_{off}).

2.2.1 Threshold Voltage

Threshold Voltage (V_{th}) is one of the most important parameters for us to determine whether the device is good or not. However, there are lots of ways to define the V_{th} for semiconductor devices, and most of them were extracted from I_{ds}-V_{gs} curves. One of the most common V_{th} measurement technique is the linear extrapolation method with the I_{ds}-V_{gs} curve at low drain voltage of 50 ~ 100 mV typically to ensure operation in the linear region[55]. In fact, curve of drain current is not zero when gate voltage is fairly low, but it can be approached to zero with intercept the curve of drain current to axis of gate voltage by the equation

$$V_{th} = V_{gsi} - \frac{V_{ds}}{2} \quad \text{(Eq 2-1)}$$

Equation 2-1 is only valid to extract V_{th} with negligible series resistance. And usually series resistance could be negligible when the drain voltage is low so as to keep the channel to be operated in the linear region. The I_{ds}-V_{gs} curve can be divided to two parts by the point of V_{th}: V_{gs} above V_{th} is usually due to series resistance and mobility, V_{gs} below V_{th} is contributed by sub-threshold current. It is practice to extract the V_{th} by find out the maximum slope of I_{ds}-V_{gs} first, so as to see maximum point of transconductance versus gate voltage is a simply way. And next, linear I_{ds}-V_{gs} curve can be use to extract V_{th} by fit a straight line to extrapolate to I_{ds}=0.

In this thesis, V_{th} is defined differ form above description and is defined by more simply way which called constant drain current method. This method can be found in almost the papers relate to poly-Si TFTs. The V_{th} obtained from this way is close to the one extracted from linear extrapolation method. Here, constant drain current is fixed to

$$I_{ds} = I_{dn} \times \frac{W}{L} \qquad \text{……………………………………………………(Eq 2-2)}$$

where I_{dn}=100 nA for n-channel at V_{ds}=0.1 and W, L are channel width and length respectively. In this thesis, devices were all measured by W=100 μm, L=10 μm. Thus, I_{ds} was fixed to 10^{-6} A in all our discussion.

2.2.2 Transconductance

Transconductance (G_m) is one guide for us to obtain the field effect mobility. Since transfer characteristics of poly-Si TFTs are similar to those of MOSFETs, first order of I_{ds}-V_{gs} relation in bulk Si MOSFETs can be applied to poly-Si TFTs. The drain current in linear region ($V_{ds} < V_{gs} - V_{th}$) can be approximated as the following equation:

$$I_{ds} = \mu_{FE} C_{ox} \left(\frac{W}{L}\right)\left[(V_{gs} - V_{th})V_{ds} - \frac{1}{2}{V_{ds}}^{2}\right] \qquad \text{…………………… (Eq 2-3)}$$

where W is the channel width, L is the channel length, V_{th} is the threshold voltage, C_{ox} is the gate oxide capacitance per unit area. Thus, G_m is given by

$$G_m = \frac{\partial I_{ds}}{\partial V_{gs}} = \mu_{FE} C_{ox} \left(\frac{W}{L}\right) V_{ds} \qquad \text{………………………………… (Eq 2-4)}$$

Here, transconductance of devices were all measured with W=100 μm, L=10 μm at V_{ds}=0.1 V.

2.2.3 Sub-threshold Swing and Interface State

Sub-threshold Swing (S.S.) is a typical parameter which reflects gate control ability and also the on/off speed of a device. Swing is related to the variation of the bending at the interface with the gate voltage[8]. The drain current in the saturation region ($V_{ds} > V_{gs} - V_{th}$) is expressed as the following equation:

$$I_{ds} = \frac{1}{2}\mu_{FE} C_{ox} \frac{W}{L}(V_{gs} - V_{th})^2 \quad \text{..................................} \quad \text{(Eq 2-5)}$$

It appears that the current abruptly vanishes while V_g is reduced to zero from the equation above. This current is due to the weak inversion happened in the channel between flat-band and threshold voltage, which leads to a diffuse current from source to drain electrode. However, sub-threshold swing in TFTs also present the fact of exist of interface states in the gate insulator/poly-Si surface. The sub-threshold swing has been reported to be closely related to the trap states located near the mid-gap (deep states), which originate from dangling bonds, while the mobility is more associated with the trap states located near the band edge (tail state)[56, 57]. To evaluate the traps original existed and the states created near the interface of gate insulator/poly-Si channel after long-time stress, there is a way. By neglecting the depletion capacitance in the active layer, Takashi Noguchi has report that effective interface-trap-state density (N_{it}) near the poly-Si/SiO_2 interface can be evaluated from the sub-threshold swing [58-60],

$$N_{it} = [(\frac{S.S.}{\ln 10})(\frac{q}{kT}) - 1](\frac{C_{ox}}{q}) \quad \text{..................................} \quad \text{(Eq 2-6)}$$

Roughly, sub-threshold swing can tell us whether the states occur in the interface or not. The sub-threshold swing is defined as the reciprocal of slope of the I_{ds}-V_{gs} curve in weak inversion region and as the amount of gate voltage required to increase/ decrease drain current by one order of magnitude. The formula of S.S were defined as

$$\mathrm{S.S.}=\left[\frac{\partial(\log I_{ds})}{\partial V_{gs}}\right]^{-1} \qquad \text{(Eq 2-7)}$$

In this thesis, the sub-threshold swing is defined as one-third of the gate voltage required decreasing the threshold current by three orders of magnitude. The threshold current is specified to be the drain current when the gate voltage is equal to threshold voltage.

2.2.4 On/Off Current Ratio

In common with conventional MOSFETs, on/off current ratio is also one important parameter to request in the transfer characteristic in TFTs. A high performance poly-Si TFT should not only exhibit large driving current, but also low off state current or called leakage current, is required. For a switching element, like pixel cell, the off state is frequently encountered in normal operation. Therefore, on/off current ratio is obviously a better evaluation parameter compared with on current alone. The leakage current mechanism in poly-Si TFTs in more complicate than bulk Si MOSFETs. Poly-Si exist lots of inherent defect states in the intra-grain and inter-grain site, and most of the density of states located inside the deep level of forbidden band-gap, and increase with the number of dangling bond increase. The values of activation energy in poly-Si is about 0.5~0.6eV, which really close to the mid-gap[57]. Thus, it is easy to generate leakage current via trap-assist-tunneling and band-to-band tunneling. Generally speaking, when low drain voltage biased, leakage current usually occur with thermal generation in the drain depletion region, and that was increase with the thicker active region layer. However, due to the existing numerous trap states in the poly-Si film and the large electric field locate near drain side, electron and hole emission from trap states become strongly increasing as functions of electric field. The tunneling rate depends upon the total electric field locate in the drain side, and consequently the leakage current is highest when the voltage between drain and gate electrode are large. In short, leakage current can affect by several mechanisms which described above and affect the on/off current ratio strictly.

In this thesis, the on current is defined with the method of constant overdrive current, which gate voltage apply 1V over than the threshold voltage and drain voltage fixed to 1V for n-channel TFTs. Since devices with different conditions in this thesis undergo stressing progresses, constant overdrive current method is one better choice even if the threshold voltage shift is serious. This is differ from the conventional on current extract method which grab the maximum current of sweep V_{gs} at high V_{ds}, due to the low V_{gs} sweeping range in virgin measurement, which does not want “stress” happened and this range is differ from the range after stress. Finally, off current is specified as the minimum current when drain voltage equals to 1V.

Chapter 3 Electrical Characteristic of LTPS High-k TFTs

3.1 Performance and Reliability with Fluorine Implantation

To investigate how fluorine affect the LTPS High-k TFTs, the best implant condition should be found before compare to the control sample, which does not implant with fluorine. To find out the best condition, not only original electric characteristic be discussed, but also the characteristic should be analyzed after stress. Therefore, we use the positive bias temperature stress to help us find out the best one. With stress condition as follow: bias gate stress voltage 5 V over than threshold voltage, both drain and source bias equal to 0 V, stress time equal to 1000 s, and temperature of measurement are all in the room temperature. All the device dimension we measure are gate width=100 μm and gate length=10 μm, so as to reduce the effect come from miss align gate pattern, which would lead to asymmetric of source and drain electrode.

The measurement of transfer characteristic apply gate bias sweep from -0.5 V to 6 V, with drain voltage fixed to 0.1 V, and between stressing interval, all the measurement are applied to linear region measurement, to prevent hot carrier which occur under saturation region measurement. Thus, gate bias instability would simply contribute to the variation of whole material.

Figure 3-1 show the transfer characteristic before and after 1000 s PBTI stress with V_g-V_{th}=5 V, V_d=V_s=0 V, at 25 ^{o}C, with different fluorine implant dosages. The off state current, I_{min}, reduce further with implant dosage increase under implant energy 11k eV, this could be thought as the drain side junction defect states would be passivate efficiency when the large number of fluorine be introduced. Since our implant dosage does not higher than the Si solid solubility, the fluorine we introduce into poly-Si will not segregate out which will not lead to passivate the trap states but generate the additional defects to degrade the electrical properties[45].

Figure 3-2 show the characteristics before and after 1000 s PBTI stress with V_g-V_{th}=5 V, V_d=V_s=0 V, at 25 ^{o}C, with different fluorine implant energies. The off state current increase with the increase of implant energy, but the larger implant energy of 30k eV perform the lowest off state current. The latter measurement of this sample serve serious gate leakage current, this may be due to the damage created in the interface which does not repair after 600 ^{o}C anneal from the higher implant energy, so that create a Flank-Pool tunneling path. Since the serious gate leakage current, we do not present the transfer characteristic of 30k eV here.

The Table 3-1, 3-2 list the characteristic before and after PBTI stress, and Table 3-3 list the degradation percentage under the same PBTI stress. The transconductance (G_m) increase with the implant dosages, this might due to the more fluorine ions passivate the tail states in the grain boundary, even after PBTI stress the dosage of 5e14 cm^{-2} still perform best. Although the better of G_m show in the condition of 20k eV, but it has the larger off state current, this is because of the drain side junction near the interface does not passivated, but the states in the grain boundary been passivated very well as show in G_m, which is due to larger implant energy accompany with deeper passivated positions.

Finally, the best condition of 11k eV, 5e14 cm^{-2} has been our choice, due to the lowest off state current, higher on/off current ratio, excellent sub-threshold swing, as show in the Table 3-1, 3-2, 3-3.

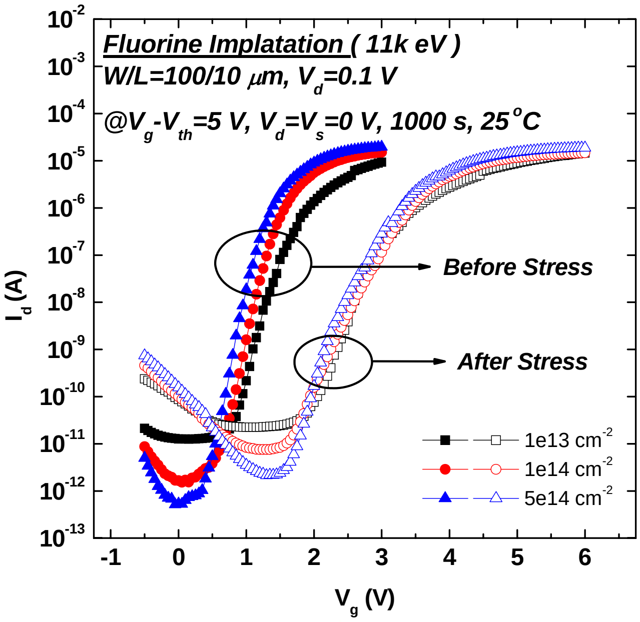

Figure 3-1 Transfer characteristic of LTPS High-k TFTs with various fluorine implant conditions under 1000 s PBTI stress at 25 ^{o}C with V_g-V_{th}=5 V, V_s=V_d=0 V

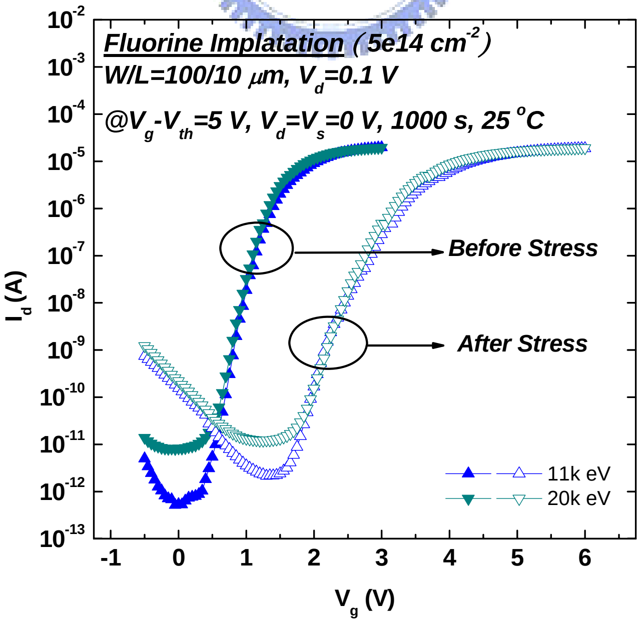

Figure 3-2 Transfer characteristic of LTPS High-k TFTs with various fluorine implant conditions under 1000 s PBTI stress at 25 ^{o}C with V_g-V_{th}=5 V, V_s=V_d=0 V

	Control	**11k eV 1e13 cm^{-2}**	**11k eV 1e14 cm^{-2}**	**11k eV 5e14 cm^{-2}**	**20k eV 5e14 cm^{-2}**	**30k eV 5e14 cm^{-2}**
$I_{on}(10^{-5}A)$	9.13	3.76	6.79	7.55	9.22	8.46
$I_{off}(10^{-10}A)$	1.28	1.44	0.42	0.30	1.00	0.19
$I_{on}/I_{off}(10^{5})$	7	2	15	24	9	43
S.S.(mV/dec)	135	191	155	158	150	133
$V_{th}(V)$	0.91	1.91	1.56	1.38	1.33	1.48
$G_m(\mu s)$	17.0	8.56	12.9	15.8	18.6	15.3

Table 3-1 Characteristics of LTPS High-k TFTs with various fluorine implant condition before 1000 s stress at 25 ^{o}C with V_g-V_{th}=5 V, V_s=V_d=0 V,

	Control	**11k eV 1e13 cm^{-2}**	**11k eV 1e14 cm^{-2}**	**11k eV 5e14 cm^{-2}**	**20k eV 5e14 cm^{-2}**	**30k eV 5e14 cm^{-2}**
$I_{on}(10^{-5}A)$	3.37	2.16	3.73	3.27	4.44	x
$I_{off}(10^{-10}A)$	1.77	2.08	0.79	0.45	1.28	x
$I_{on}/I_{off}(10^{5})$	1	1	4	7	3	x
S.S.(mV/dec)	320	278	342	250	258	x
$V_{th}(V)$	2.99	3.49	3.42	3.14	3.19	x
$G_m(\mu s)$	6.95	6.10	8.72	10.2	12.5	x

Table 3-2 Characteristics of LTPS High-k TFTs with various fluorine implant conditions after 1000 s stress at 25 ^{o}C with V_g-V_{th}=5 V, V_s=V_d=0 V,

	Control	**11k eV** **1e13 cm^{-2}**	**11k eV** **1e14 cm^{-2}**	**11k eV** **5e14 cm^{-2}**	**20k eV** **5e14 cm^{-2}**	**30k eV** **5e14 cm^{-2}**
ΔI_{on}(%)	-63	-57	-45	-55	-51	x
ΔI_{off}(%)	-37	44	85	49	27	x
ΔS.S.(%)	135	45	119	57	72	x
ΔV_{th}(V)	2.08	1.57	1.85	1.76	1.85	x
ΔG_m(%)	-59	-28	-32	-35	-32	x

Table 3-3 Characteristic degraded percentage of LTPS High-k TFTs with various fluorine implant conditions under 1000 s stress at 25 ^{o}C with V_g-V_{th}=5 V, V_s=V_d=0 V

3.2 Performance and Reliability with Nitrogen Implantation

To find out the best sample with introduce nitrogen by implantation, we also discuss the electrical characteristic before and after PBTI stress, with apply gate bias 5 V over than threshold voltage, and connect source and drain electrode to ground, with stress time 1000 s, at room temperature 25 ^{o}C.

Figure 3-3 show the transfer characteristic of various nitrogen implant energy, including 11k, 20k, 30k eV. And we could easily notice the sample with implant energy 30k eV has the steeper sub-threshold swing after PBTI stress, this is due to better interface recovery by nitrogen passivation.

And Figure 3-4 show the transfer characteristic with introduces different nitrogen implant dosages but the same energy. With has larger the dosage, 1e14 cm^{-2}, the upper sub-threshold region which almost near the threshold voltage became smoother than the dosage of 1e13 cm^{-2}. This is due to the exceed nitrogen create the tail states which original from the strain bonds in the interface. And the continuing increase the dosages, 5e14 cm^{-2}, the lower sub-threshold region become smoother, which is due to the deep state creation. This results come from the exceed nitrogen do not bond with Si, but generate dangling bonds in the interface, which do not repaired undergo 600 ^{o}C annealing.

Moreover, the characteristics before and after BPTI stress have been list in the Table 3-4, 3-5, and the degradation percentage is list in the Table 3-6. Since the excellent sub-threshold swing and large value of transconductance been performed, the condition 30k eV, 1e13 cm^{-2}, has been our choice. This condition perform excellent sub-threshold swing mean the interface states reduction, and also large value of transconductance could tell us the tail states in grain boundary also passivated very well.

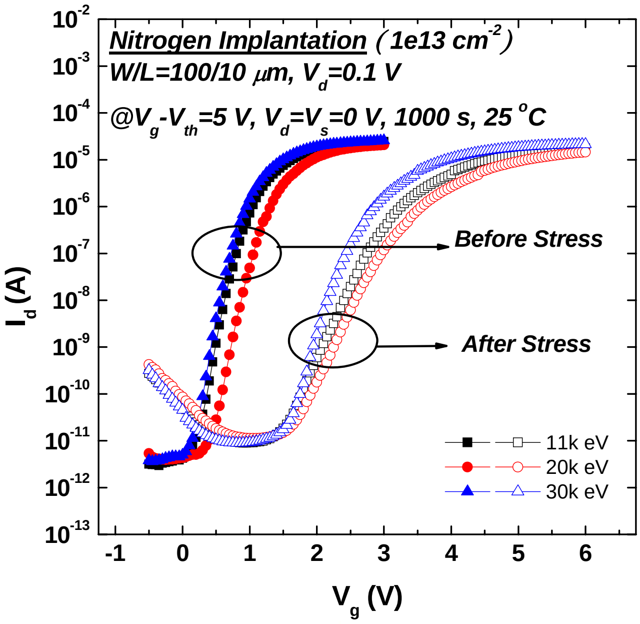

Figure 3-3 Transfer characteristic of LTPS High-k TFTs with various nitrogen implant conditions under 1000 s PBTI stress at 25 °C with V_g-V_{th}=5 V, V_s=V_d=0 V

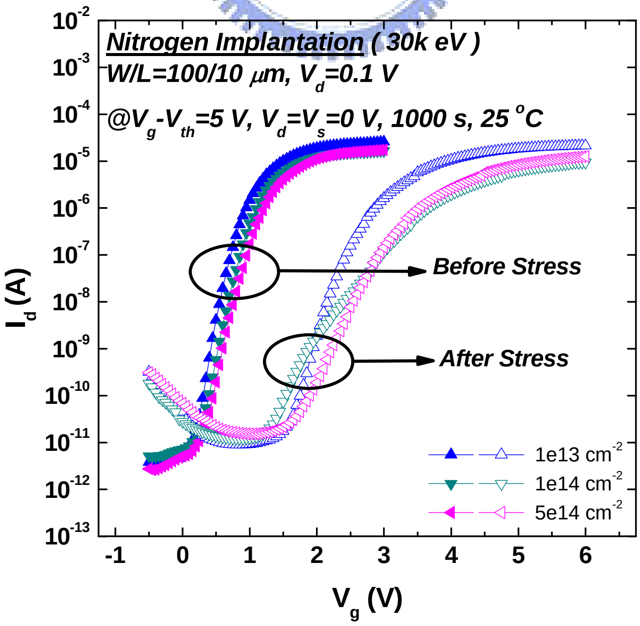

Figure 3-4 Transfer characteristic of LTPS High-k TFTs with various nitrogen implant conditions under 1000 s PBTI stress at 25 °C with V_g-V_{th}=5 V, V_s=V_d=0 V

	Control	**11k eV 1e13 cm^{-2}**	**20k eV 1e13 cm^{-2}**	**30k eV 1e13 cm^{-2}**	**30k eV 1e14 cm^{-2}**	**30k eV 5e14 cm^{-2}**
$I_{on}(10^{-5}A)$	8.92	8.68	8.88	9.80	7.35	7.80
$I_{off}(10^{-10}A)$	0.55	0.67	0.78	0.56	0.95	0.92
$I_{on}/I_{off}(10^{5})$	16	12	11	17	7	8
S.S.(mV/dec)	148	137	152	137	150	160
$V_{th}(V)$	0.85	1.05	1.31	0.98	1.12	1.21
$G_m(\mu s)$	16.6	19.8	18.3	21.0	15.0	15.4

Table 3-4 Characteristics of LTPS High-k TFT with various nitrogen implant conditions before 1000 s stress at 25 °C with V_g-V_{th}=5 V, V_s=V_d=0 V

	Control	**11k eV 1e13 cm^{-2}**	**20k eV 1e13 cm^{-2}**	**30k eV 1e13 cm^{-2}**	**30k eV 1e14 cm^{-2}**	**30k eV 5e14 cm^{-2}**
$I_{on}(10^{-5}A)$	2.55	2.85	2.40	4.26	1.95	2.30
$I_{off}(10^{-10}A)$	0.91	1.11	1.30	1.06	1.39	1.61
$I_{on}/I_{off}(10^{5})$	2	2	1	4	1	1
S.S.(mV/dec)	254	326	339	202	508	327
$V_{th}(V)$	2.62	3.25	3.56	2.85	3.65	3.51
$G_m(\mu s)$	5.97	7.93	6.86	10.1	4.27	5.73

Table 3-5 Characteristics of LTPS High-k TFT with various nitrogen implant conditions after 1000 s stress at 25 °C with V_g-V_{th}=5 V, V_s=V_d=0 V

	Control	**11k eV $1e13\ cm^{-2}$**	**11k eV $1e14\ cm^{-2}$**	**11k eV $5e14\ cm^{-2}$**	**20k eV $5e14\ cm^{-2}$**	**30k eV $5e14\ cm^{-2}$**
ΔI_{on}(%)	-71	-67	-72	-56	-73	-70
ΔI_{off}(%)	65	64	65	86	45	72
ΔS.S.(%)	72	136	122	46	238	104
ΔV_{th}(V)	1.76	2.19	2.24	1.87	2.53	2.30
ΔG_m(%)	-64	-60	-62	-51	-71	-63

Table 3-6 Characteristic degraded percentage of LTPS High-k TFT with various nitrogen implantation conditions under 1000 s stress at 25 ^oC with V_g-V_{th}=5 V V_s=V_d=0 V

Chapter 4 Reliability in LTPS High-k TFTs

4.1 Brief Reliability Review

Before we discuss the reliability of hot carrier stress (HCS) and positive bias temperature instability (PBTI), let us take a review of past studies in reliability in TFTs. Past years, most of the reliability studies focus on hot carrier stress and negative bias temperature instability. Among these studies, NBTI have been proposing some models about how the interface reactions affect the electrical characteristic. The classical model is show in Figure 4-1[61]. At high temperature, hydrogen in poly-Si would dissociate and diffuse into SiO_2, and react with SiO_2 to generate OH-groups bonded to Si atoms. Hence, defects would exist in interface or grain boundary due to dangling bonds, in the SiO_2 due to OH-groups, un-bonded positively Si atoms, and free electrons. Since free electron would be carry away to poly-Si by electric field and accelerate these reactions again. These years, new ideal have been proposed to improve the poly-Si reliability under NBT operation by fluorine incorporation in poly-Si. As show in Figure 4-2, strong Si-F bond does not broken easily and hence the diffuse mechanism would not happen[46]. Due to the positively Si exist in the SiO2, interface states would be easy generated by this hole trap recombination with injected electrons, which also reported in the hot carrier stress studies[62]. Hence the mechanism of NBTI will be more complicate than PBTI, because of hole traps will not easily happened in SiO_2. Therefore, PBTI mechanism will be simply only contributed by electron injection.

In order to clarify the mechanisms that degrade electrical characteristics, some parameters need to be extract to help analyzing. The sub-threshold swing depend mainly on intra-grain traps distributed uniformly inside the poly-Si film and also on the deep interface states[63-65], as show in Figure 4-3 number 1. The deep states existing in the grain boundary and oxide trap charges which do not de-trap have been demonstrated to affect mainly on threshold voltage[63, 66, 67], as show in Figure 4-3 number 2 and 5. Tail states in the interface and/or in grain boundary mainly contribute to the decrease of G_m maximum[63, 67], which the latest parameter to start with, as show in Figure 4-3 number 3 and 4. Therefore, it is obvious that depending on the nature of states generation after stress, electrical parameters can provide useful information to clarify poly-Si TFTs degraded mechanisms under HCS and PBTI in our device.

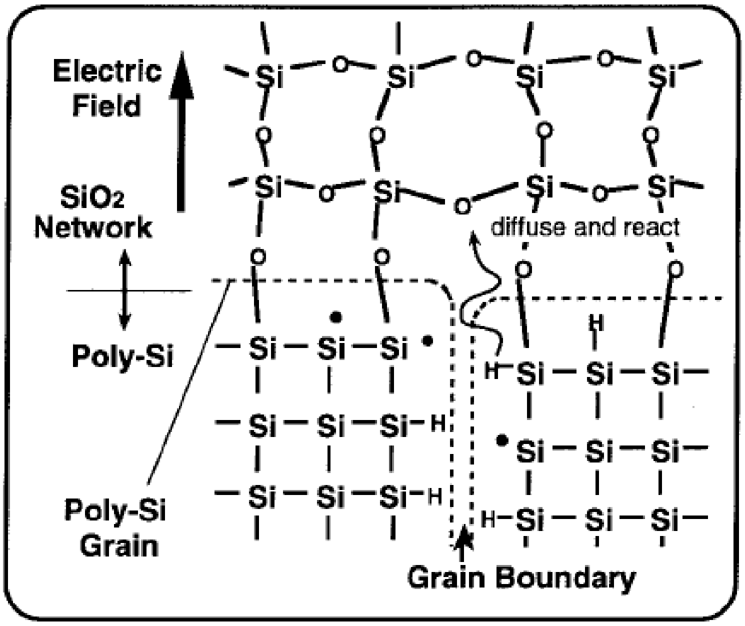

Figure 4-1 NBTI model of interaction between poly-Si and SiO_2[61]

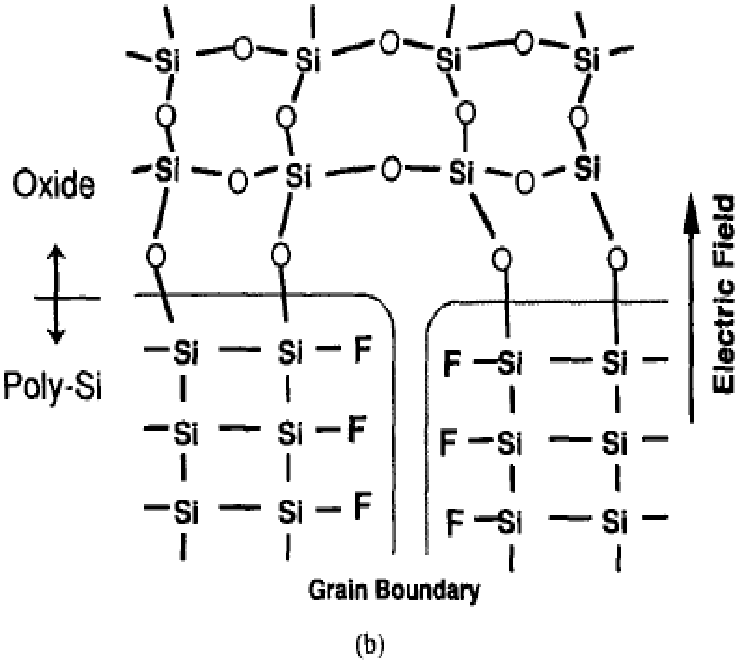

Figure 4-2 NBTI model show fluorine incorporation into poly-Si [46]

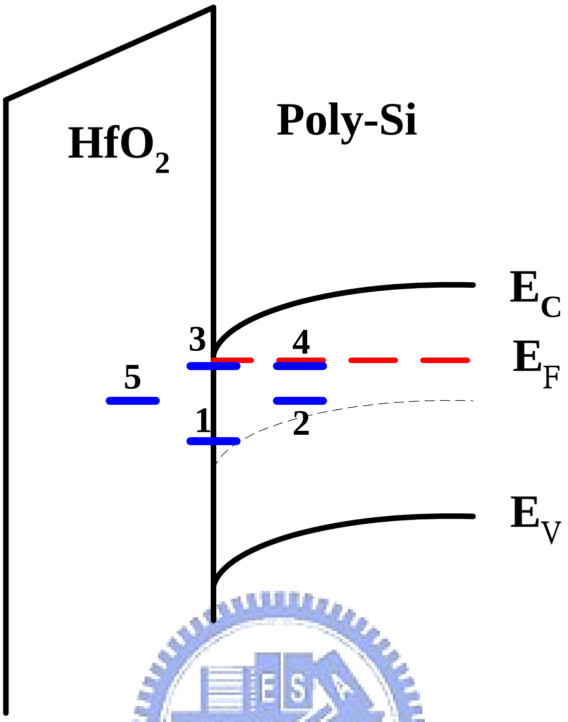

Figure 4-3 Defect sites in band diagram

4.2 Fluorine Implantation

4.2.1 Hot Carrier Stress

First reliability test method which we use is hot carrier stress, with stress condition by apply gate voltage 5 V over than threshold voltage, fixed drain voltage to 5 V, and connect source electrode to ground for 1000 s. Figure 4-4 show the transfer characteristic of control sample and fluorine implanted sample. It could be easily noticed the off state current segment in both the control and fluorine implanted sample been disappear after hot carrier stress. We suggest the damage does not happen in the channel, but in the gate dielectric. In order to examine our ideal, forward and reverse drain current were measured just like the method use in the two-bit operation memory. Figure 4-5 show the forward measurement setup, which drain voltage fixed to 0.1 V and source connect to ground. For the reverse measurement, source voltage fixed to 0.1 V and drain connect to ground. Figure 4-6 show the result that reverse measurement perform the off state current have the same order as the initial reverse measurement. It means that damage happened in the drain side gate dielectric, so that offer the frank-pool tunneling path for the current comes from gate, which the path marked by three start sign as show in Figure 4-5. As the gate voltage larger than drain voltage in Figure 4-4, the off state electron current will conduct upward, tile the inversion layer electron flow into drain larger than the gate current, and then curve again appear in the transfer characteristic. Figure 4-7 shows the transfer characteristic again but different with the current been take for absolute calculated, hence, the gate leakage current appeared as show in hallow sign. The fluorine implanted sample has the lower gate leakage current suggest that the damage happened in the drain side gate dielectric less than that in the control sample.

We speculate that the fluorine will diffuse into HfO_2 under the gate dielectric densify process and passivate the defect in the HfO_2. Although the hot electron inject into gate dielectric, the fluorine bond inside the HfO_2 will not easy be broken. Thus the defect created damages can be less than the control one, so that have lower gate leakage current. And the phenomenon of fluorine passivate the defects in HfO_2 also can be see in the threshold voltage shift which is fewer than control one. Figure 4-8 show the gate dielectric capacitance of control and fluorine implanted sample, and the fluorine implanted one have lower gate capacitance than control due to the fluorine indeed have diffuse into gate dielectric as report in [68]. And this could also be show at the initial G_m maximum, which has lower gate capacitance by fluorine as show in Figure 4-9. And after hot carrier stress, the fluorine implanted sample performs the higher G_m maximum than the control one, thanks to the strong Si-F has work in passivate the grain boundary tail states in the drain side as discussed in the Figure 4-3.

Now let us take a look at Figure 4-10 and 4-11 which show the time evolutions of sub-threshold swing degradation and threshold voltage shift, respectively. The time evolution sub-threshold swing degradation of fluorine implanted sample exhibit better than control, which contribute by strong Si-F bond passivate the interface deep states in the drain side. And Figure 4-11 also show the fluorine implanted sample has lowered threshold voltage shift than control, which due to the fluorine passivate the defect states in HfO_2, as discuss yet. Since sub-threshold swing region happened earlier than the threshold voltage, the threshold voltage shift should have the same trend with sub-threshold swing degradation, but it is not. It may be due to different mechanisms between these two parameters. In the past studies of prediction of threshold voltage shift, if it exhibit logarithm time dependent means that most of shift comes from bulk oxide charges, but for the power time dependent means that states created in poly-Si or HfO_2[59, 69, 70]. Hence, the threshold voltage shift for the control and fluorine implanted sample both have the same logarithm time dependent, which suggest that our HfO_2 perform the large amount of electron trapping even though fluorine have been passivate some of these defects. Table 4-1 and 4-2 list the characteristics before and after of control and fluorine implanted sample before and after hot carrier stress. We could easily see the fluorine implanted sample perform the better resist to hot carrier damage.

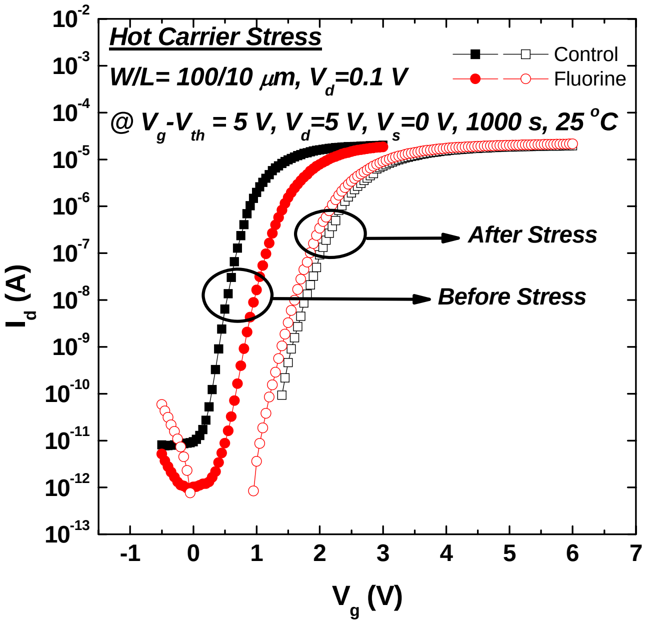

Figure 4-4 Transfer characteristic with and without fluorine implantation, before and after 1000 s hot carrier stress at 25 ^{o}C with V_g-V_{th}=5 V, V_d=5 V, V_s=0 V

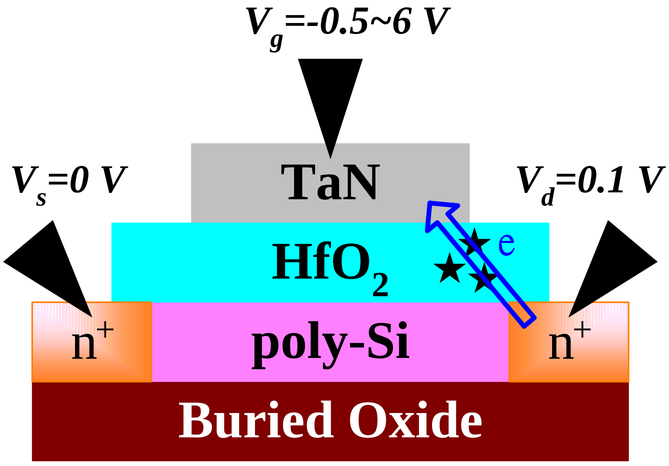

Figure 4-5 Forward measurement with sweep V_g=-0.5~6 V, V_s=0 V, V_d=0.1 V

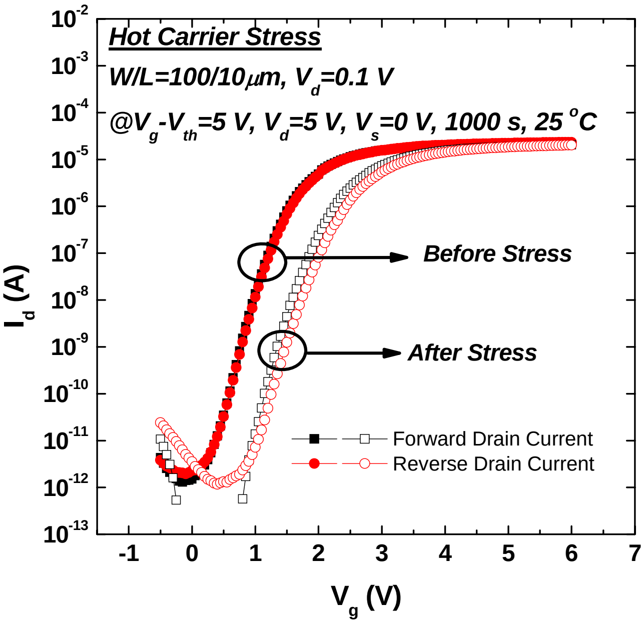

Figure 4-6 Forward and reverse transfer characteristic with fluorine implantation, before and after 1000 s hot carrier stress at 25 °C with V_g-V_{th}=5 V, V_d=5 V, V_s=0 V,

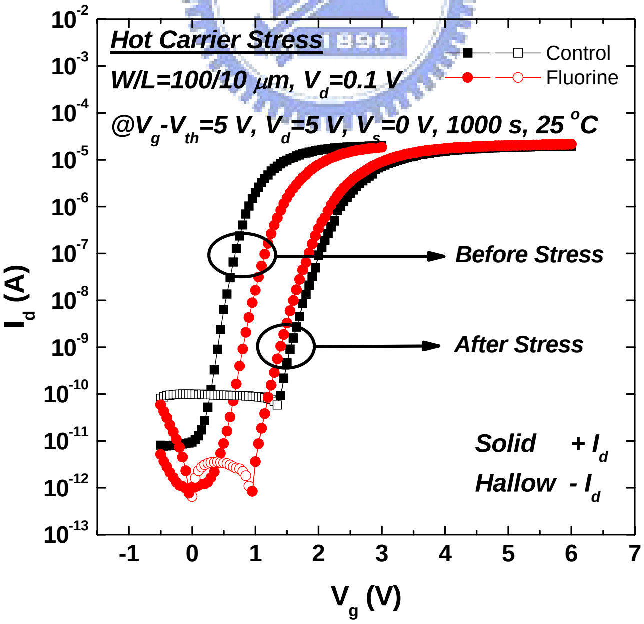

Figure 4-7 Transfer characteristic with and without the fluorine implantation, before and after 1000 s hot carrier stress at 25 °C with V_g-V_{th}=5 V, V_d=5 V, V_s=0 V, where solid line indicate the positive current, hallow line indicate the negative current

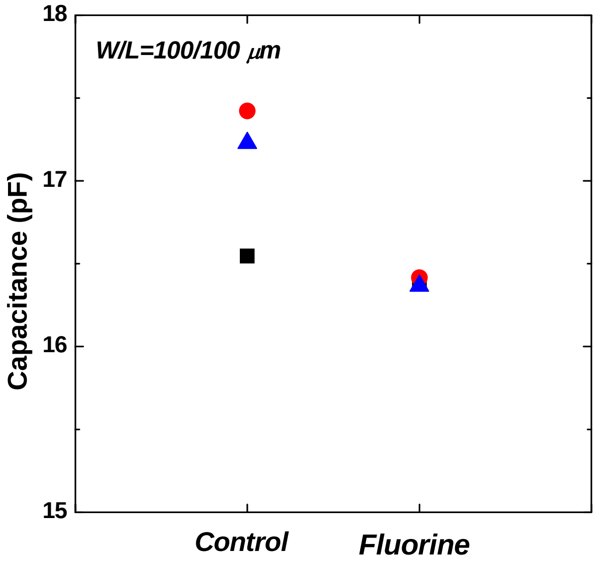

Figure 4-8 Gate dielectric capacitance with and without fluorine implantation

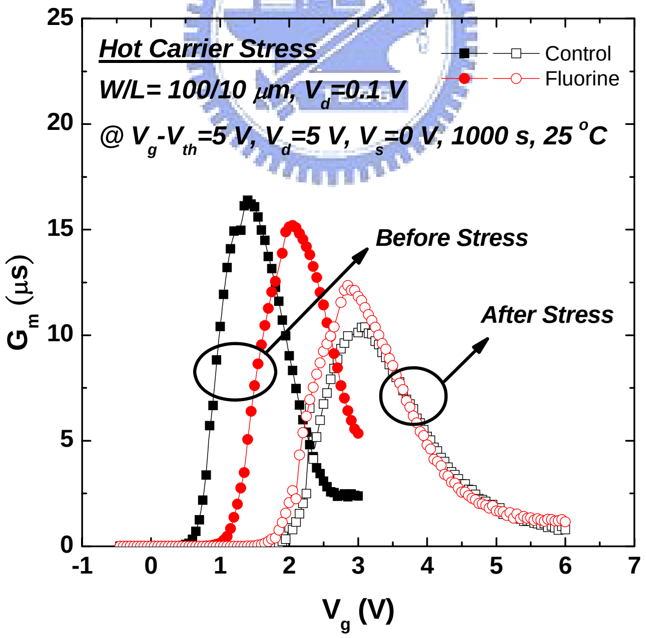

Figure 4-9 Transconductance with and without the fluorine implantation, before and after 1000 s hot carrier stress at 25 ^{o}C with V_g-V_{th}=5 V, V_d=5 V, V_s=0 V

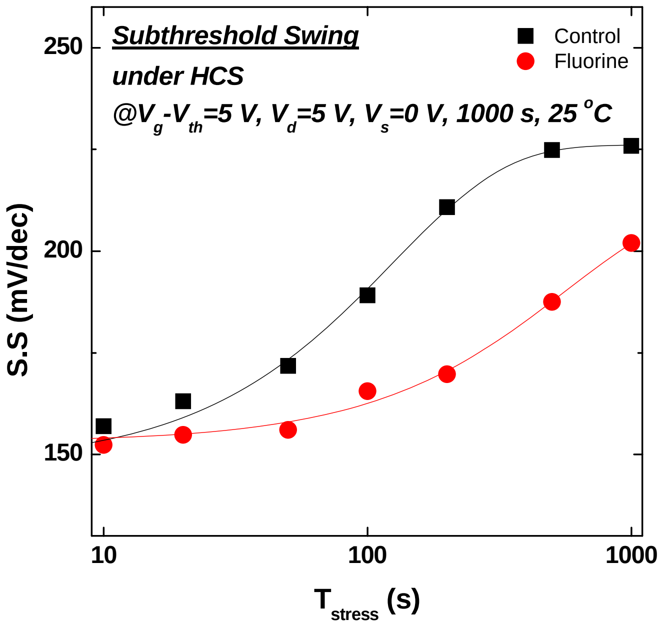

Figure 4-10 Time evolution of sub-threshold swing degradation under hot carrier stress with and without fluorine implantation

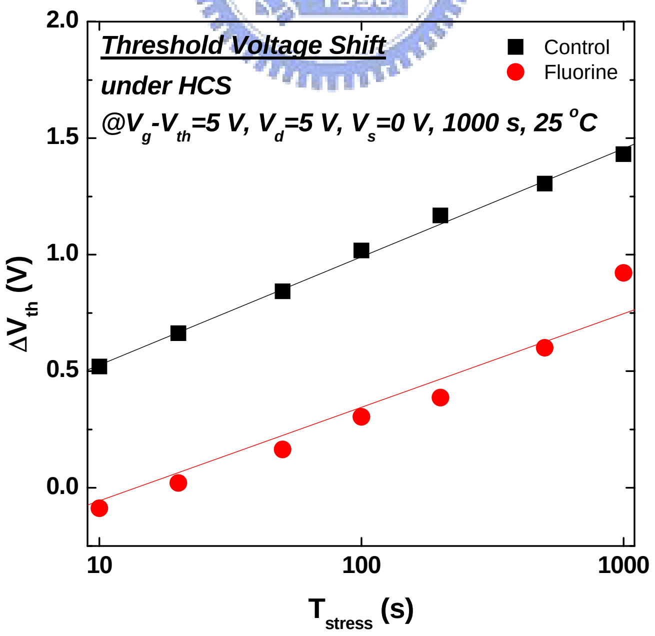

Figure 4-11 Time evolution of threshold voltage shift under hot carrier stress with and without fluorine implantation

	Control Before stress	**Control After stress**	**Fluorine Before stress**	**Fluorine After stress**
$I_{on}(10^{-5}A)$	8.51	6.37	7.80	6.61
$I_{off}(10^{-10}A)$	1.09	0.98	0.27	0.22
$I_{on}/I_{off}(10^{5})$	9	6	28	29
S.S.(mV/dec)	132	225	154	202
$V_{th}(V)$	0.91	2.34	1.42	2.18
$G_m(\mu s)$	16.4	10.3	15.1	12.3

Table 4-1 Characteristics of LTPS High-k TFTs with and without fluorine implantation before and after 1000 s hot carrier stress at 25 ^{o}C with V_g-V_{th}=5 V, V_d=5 V, V_s=0 V

	Control	**Fluorine**
$\Delta I_{on}(\%)$	-27	-15
$\Delta I_{off}(\%)$	-10	-18
ΔS.S.(%)	70	29
$\Delta V_{th}(V)$	1.43	0.76
$\Delta G_m(\%)$	-36	-18

Table 4-2 Characteristics degraded percentage of LTPS High-k TFTs with and without fluorine implantation under 1000 s hot carrier stress at 25 ^{o}C with V_g-V_{th}=5 V, V_d=5 V, V_s=0 V

4.2.2 Positive Bias Temperature Instability

After discuss the hot carrier stress which happened locally in the drain side, we look for the PBTI which qualify all the material degrade issue. Figure 4-12 show the transfer characteristic of control and fluorine implanted sample, before and after PBTI stress at 25 ^{o}C with V_g-V_{th}=5 V, V_d=V_s=0 V. One could easily see that both the drain current of control and fluorine in the upper region of sub-threshold segment become not steeped, and we suggest that was due to the donor like states created in the upper of band gap[71, 72]. Figure 4-13 and 4-14 show the process of defect generated which have the same ideal with defect pool model. Since Fermi level had been operating in the on state for n-channel device, the band bending curve would be show like Figure 4-13. The defect states have been generated at the time device operate in channel turn on, but the states still under Fermi level which will not contribute transfer curve. As the time our device measure after stress, the Fermi level will move downward, and the electron in the states will flow out and the defect states will lost the energy which electron carry away, followed by the defect energy level move download but still locate in the half of upper band gap. At the time we sweep the gate voltage again, Fermi level move upward and the electron would be trapped into the states created by stress, hence the hump in the transfer characteristic would be found. But we should notice that this phenomenon could not be see in the hot carrier stress, due to the drain bias in hot carrier operation will reduce the electric field upward in the drain side. Therefore, the donor like states would generate fewer in HCS than PBTI.

Figure 4-15 show the transconductance of control and fluorine implanted sample before and after PBTI stress. We could notice the larger G_m maximum degradation in control than fluorine implanted sample, which contribute to the strong Si-F bond exist in the grain boundary and reduce the tail states in the whole channel. And the larger the degradation percentage could also be seen in compare PBTI with HCS, the improvement in fluorine in HCS is 9.7 % better than control, but for the PBTI is 46.76 %. Thus the effect of material degraded will be expand under PBTI operation, which can help as much more easily see the passivated effect by fluorine incorporation.

Figure 4-16 and 4-17 show the time evolution of threshold voltage shift and sub-threshold swing degradation, respectively. We could see the same phenomenon with HCS in PBTI, the less threshold voltage shift contribute the defect in HfO_2 been passivate by the fluorine diffuse and resist the to the gate voltage stress damage. And here one could see the logarithm time dependent in the threshold voltage shift in both the control and fluorine implanted sample, which mean that electron trapping in HfO_2 still play the major role. For the better sub-threshold swing in fluorine implanted sample, which suggest that the better deep state reduction in the interface have been passivate by strong Si-F bond.

Figure 4-18 and 4-19 show the transfer characteristic of control and fluorine implanted sample with different temperature operation, respectively. The fluorine implanted performs better off state current than control one even after elevate temperature, means that the drain side junction defect really reduce by fluorine passivated. Since device operated at the higher temperature, the off state current dominated by the thermionic emission, still perform lower in fluorine implanted sample then in control.

Moreover, the time evolution of threshold voltage shift of control and fluorine implanted sample with different temperature operation also be show in Figure 4-20 and 4-21. One could easily see that the curve of 75 ^{o}C of threshold voltage shift lower than curve 25 ^{o}C in both control and fluorine implanted samples, which we suggest the trapping sites in those samples would be de-trap in the higher temperature, which believe that de-trapping rate is higher than the trapping rate[69]. But the much more de-trap could be found in the fluorine implanted sample, which we suggest that thinner interfacial oxide layer growth which due to fluorine like to grab the oxygen and prevent the oxygen reactive with Si[73]. The sketch map describe above as show in Figure 4-22.

Finally, Table 4-3 and 4-4 list the characteristics of control and fluorine implanted samples before and after PBTI stress. We could easily see that fluorine implanted sample still perform the better resist to PBTI.

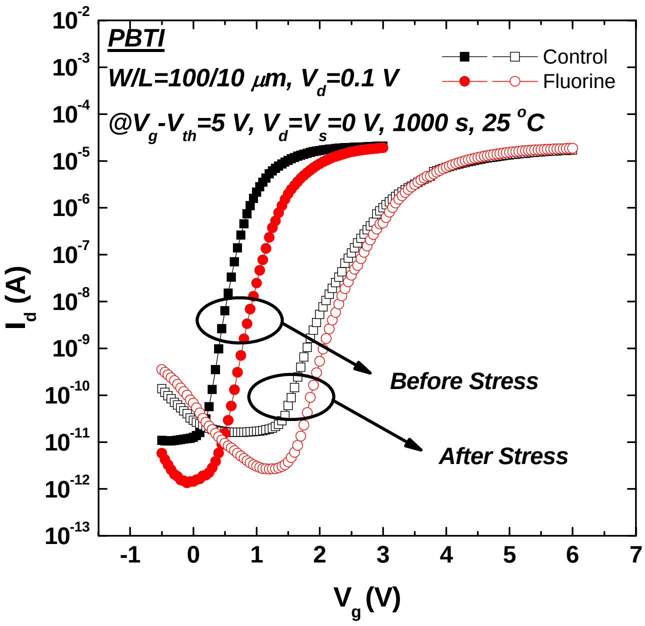

Figure 4-12 Transfer characteristic with and without the fluorine implantation, before and after 1000 s PBTI at 25 °C with V_g-V_{th}=5 V, V_d=V_s=0 V

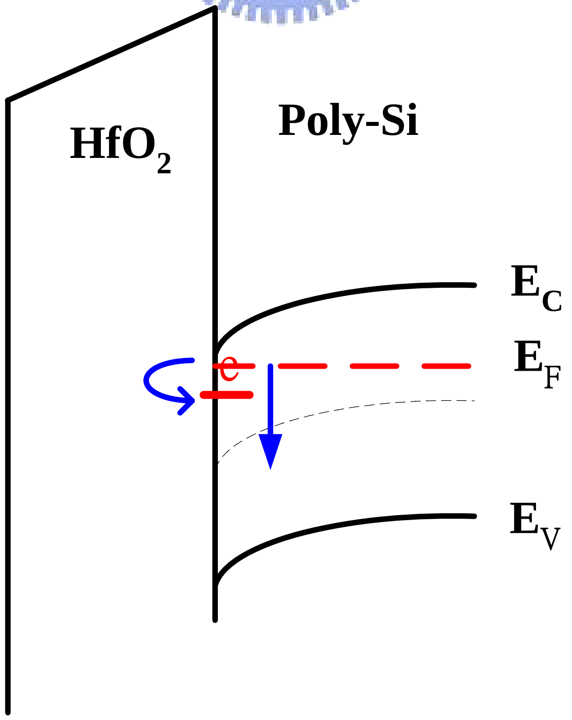

Figure 4-13 Defect pool model before states creation

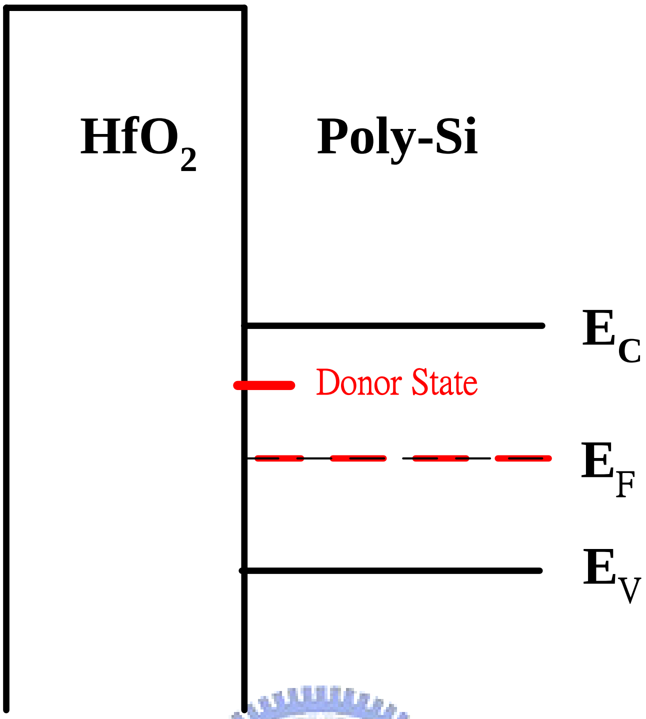

Figure 4-14 Defect pool model after states creation

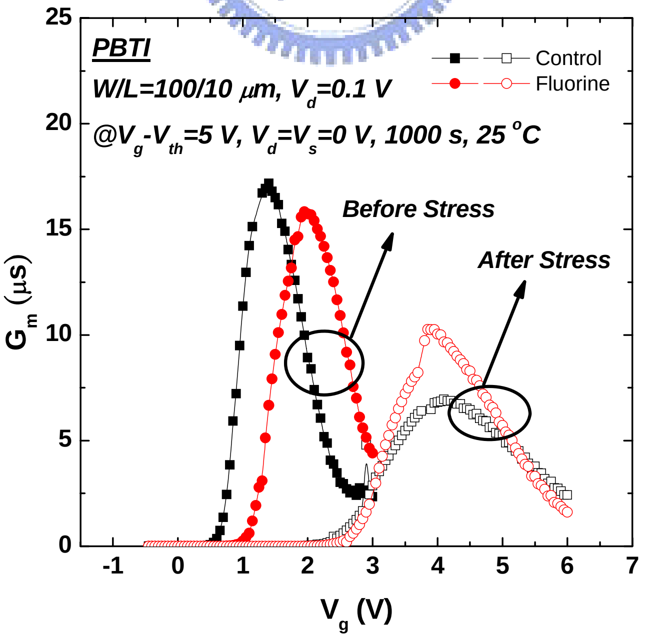

Figure 4-15 Transconductance with and without the fluorine implantation, before and after 1000 s PBTI at 25 °C with V_g-V_{th}=5 V, V_d=V_s=0 V

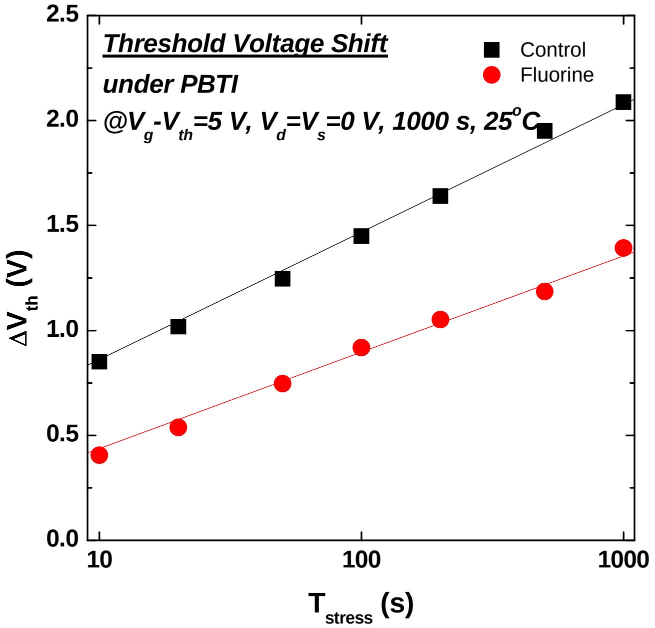

Figure 4-16 Time evolution of threshold voltage shift under PBTI with and without fluorine implantation

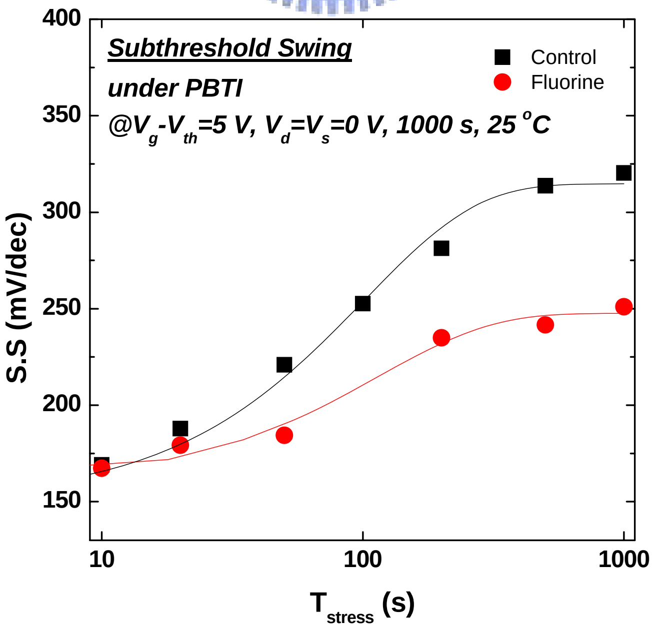

Figure 4-17 Time evolution of sub-threshold swing degradation under PBTI with and without fluorine implantation

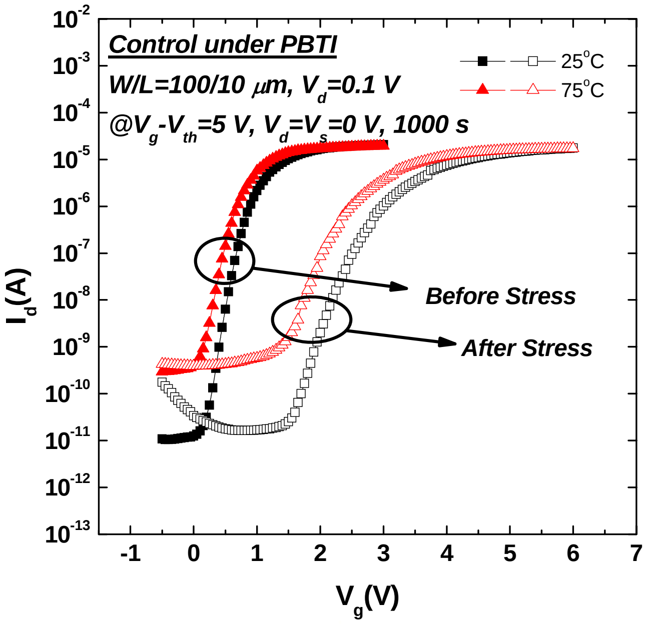

Figure 4-18 Transfer characteristic without fluorine implantation, before and after 1000 s PBTI at 25 °C and 75 °C with V_g-V_{th}=5 V, V_d=V_s=0 V

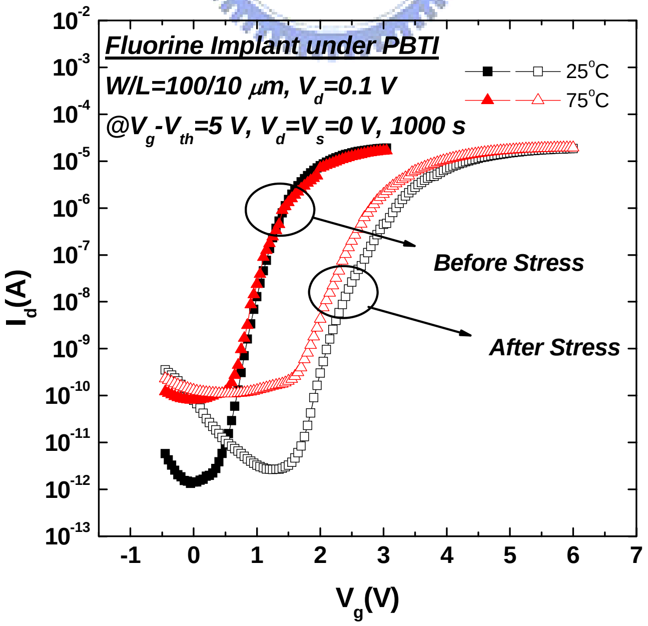

Figure 4-19 Transfer characteristic with fluorine implantation, before and after 1000 s PBTI at 25 °C and 75 °C with V_g-V_{th}=5 V, V_d=V_s=0 V

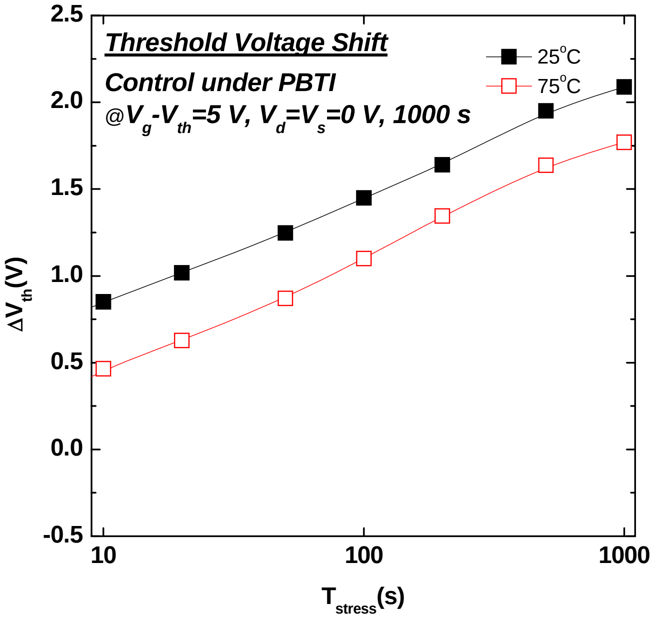

Figure 4-20 Time evolution of threshold voltage shift in control sample with temperature of 25 °C and 75 °C

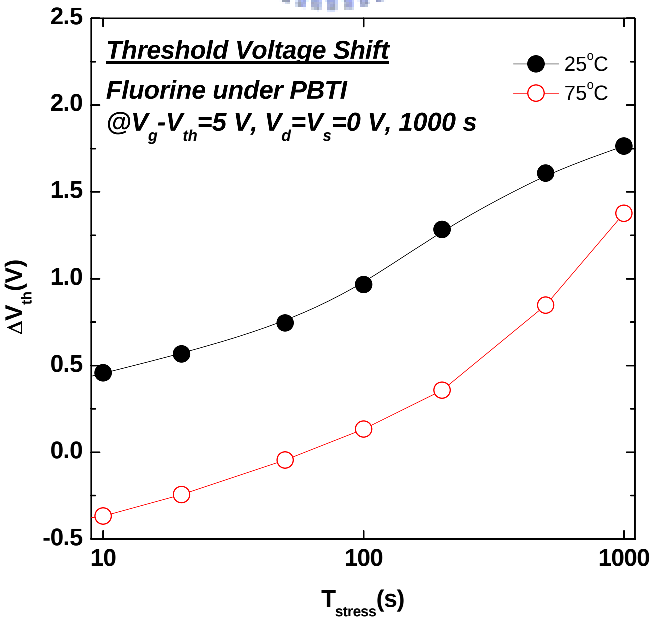

Figure 4-21 Time evolution of threshold voltage shift in fluorine implanted sample with temperature of 25 °C and 75 °C

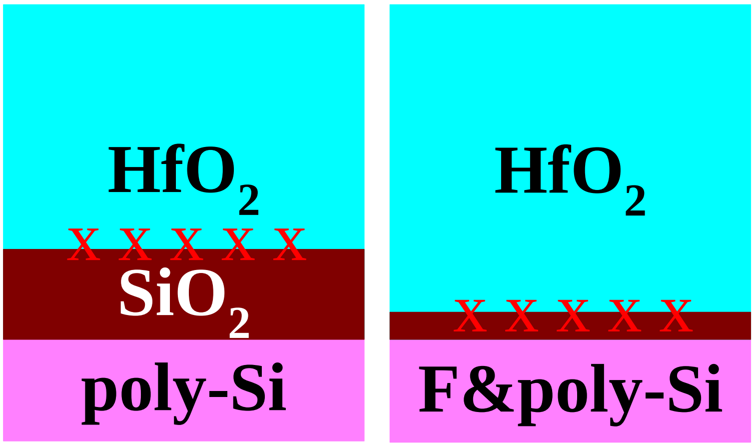

Figure 4-22 Interfacial oxide growth with and without fluorine implanted poly-Si

	Control Before stress	**Control After stress**	**Fluorine Before stress**	**Fluorine After stress**
$I_{on}(10^{-5}A)$	9.13	3.37	7.55	3.27
$I_{off}(10^{-10}A)$	1.28	1.77	0.30	0.45
$I_{on}/I_{off}(10^{5})$	7	1	24	7
S.S.(mV/dec)	135	320	158	250
$V_{th}(V)$	0.91	2.99	1.38	3.14
$G_m(\mu s)$	17.0	6.95	15.8	10.2

Table 4-3 Characteristics of LTPS High-k TFTs with and without fluorine implantation before and after 1000 s PBTI at 25 ^{o}C with V_g-V_{th}=5 V, V_d=V_s=0 V

	Control	**Fluorine**
ΔI_{on}(%)	-63	-55
ΔI_{off}(%)	37	49
ΔS.S.(%)	135	57
ΔV_{th}(V)	2.08	1.76
ΔG_m(%)	-59	-35

Table 4-4 Characteristics degraded percentage of LTPS High-k TFTs with and without fluorine implantation under 1000 s PBTI at 25 ^{o}C with V_g-V_{th}=5 V, V_d=V_s=0 V

4.3 Nitrogen Implantation

4.3.1 Hot Carrier Stress

Since we find out the best condition in chapter 3, the condition will be discuss here compare to control sample which without any nitrogen implantation. Figure 4-24 show the transconductance of control and nitrogen implanted sample before and after 1000 s HCS with the same stress voltage as described in section fluorine implantation. One should notices that initial G_m maximum of nitrogen curve is larger than that in control, which might be due to the gate dielectric capacitance increased. And this thought could be see in Figure 4-23, which describe the gate capacitance in nitrogen implanted samples are larger than control, which suggest that the nitrogen diffuse into HfO_2. After HCS, the G_m maximum of nitrogen implanted samples still performs better than that in control, but the improvement does not obvious. And this grain boundary states passivation effect might be see in PBTI, which would expand the effect that can not see in local HCS.

Figure 4-25 and 4-26 show the transfer characteristic and time evolution of threshold voltage shift. The off state current in the nitrogen exhibit higher than the control, which indicates that nitrogen in the HfO2 does not passivates and have less resist ability again to hot carrier injection. On the other hand, the larger time evolution threshold voltage shift perform in nitrogen might not only come from the defect less passivated, but also might be the larger driving current due to the larger gate capacitance in nitrogen implanted sample.

Figure 4-27 show the time evolution sub-threshold swing degradation of control and nitrogen implanted sample before and after HCS. Since the have lower sub-threshold swing expressed in the nitrogen implantation curve in whole hot carrier stress course, but the same trend both in control and nitrogen one. Here, we suggest the nitrogen passivated ability could not obvious in local stress, and the lower sub-threshold swing behave might be contribute to the higher gate capacitance which lead to better gate control ability.

Finally, Table 4-5 and 4-6 list the electrical parameters extracted from the transfer characteristic curves before and after HCS.

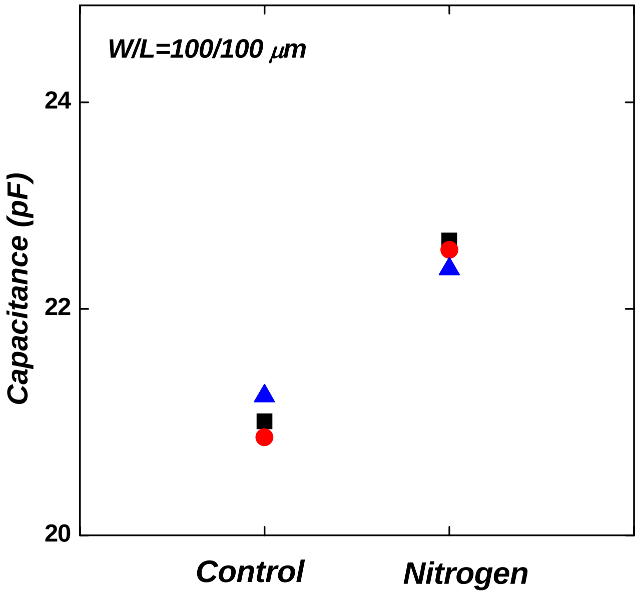

Figure 4-23 Gate dielectric capacitance with and without nitrogen implantation

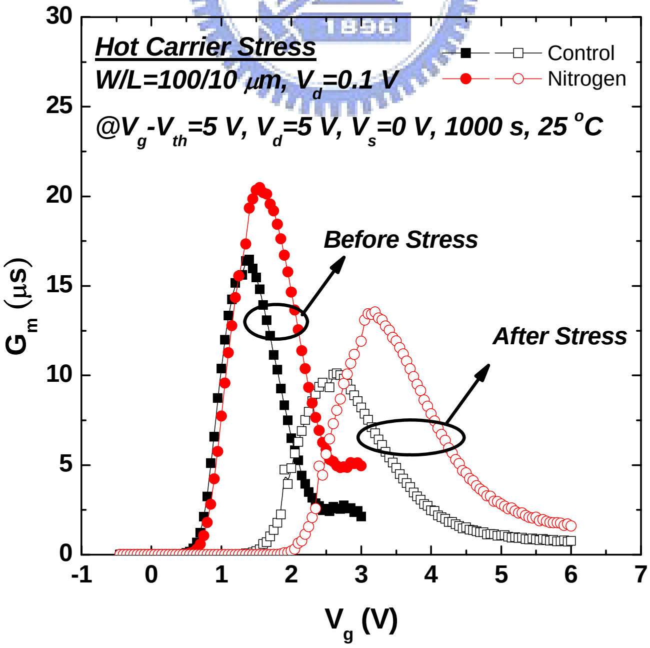

Figure 4-24 Transconductance with and without the nitrogen implantation, before and after 1000 s hot carrier stress at 25 ^{o}C with V_g-V_{th}=5 V, V_d=V_s=0 V

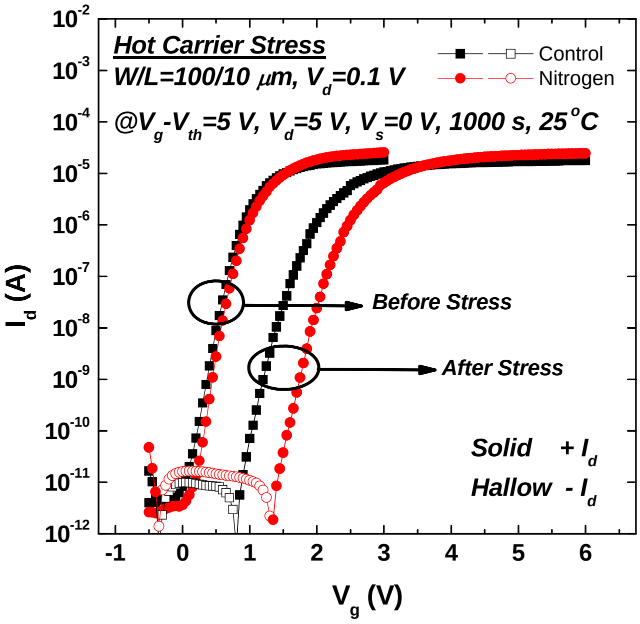

Figure 4-25 Transfer characteristic with and without the nitrogen implantation, before and after 1000 s hot carrier stress at 25 °C with V_g-V_{th}=5 V, V_d=V_s=0 V, where solid line indicate the positive current, hallow line indicate the negative current

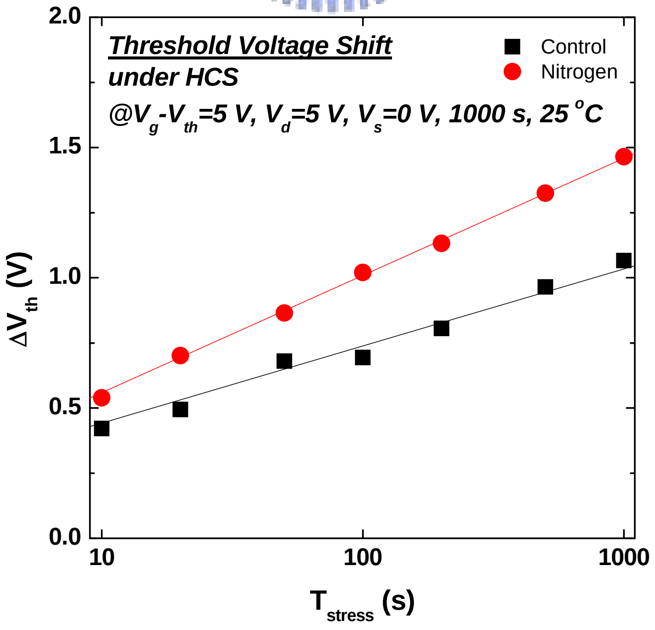

Figure 4-26 Time evolution of threshold voltage shift under hot carrier stress with and without nitrogen implantation

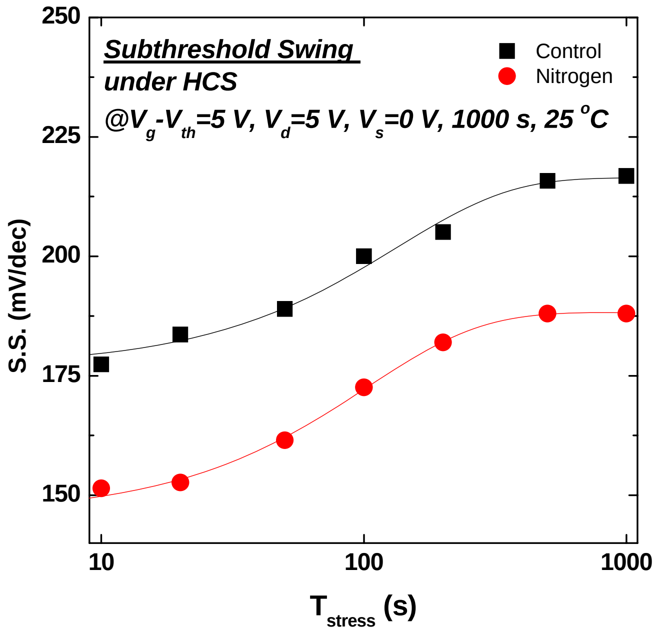

Figure 4-27 Time evolution of sub-threshold swing degradation under hot carrier stress with and without nitrogen implantation

	Control Before stress	Control After stress	Nitrogen Before stress	Nitrogen After stress
$I_{on}(10^{-5}A)$	8.97	6.55	9.61	7.06
$I_{off}(10^{-10}A)$	0.57	0.50	0.54	0.72
$I_{on}/I_{off}(10^5)$	15	12	17.6	9.71
S.S.(mV/dec)	152	216	144	188
$V_{th}(V)$	0.91	1.97	0.99	2.45
$G_m(\mu s)$	16.4	10.1	20.5	13.5

Table 4-5 Characteristics of LTPS High-k TFTs with and without nitrogen implantation before and after 1000 s hot carrier stress at 25 ^oC with V_g-V_{th}=5 V, V_d=V_s=0 V

	Control	**Nitrogen**
ΔI_{on}(%)	-26	-26
ΔI_{off}(%)	-12	33
ΔS.S.(%)	42	30
ΔV_{th}(V)	1.06	1.46
ΔG_m(%)	-38	-34

Table 4-6 Characteristics degraded percentage of LTPS High-k TFTs with and without nitrogen implantation under 1000 s hot carrier stress at 25 °C with V_g-V_{th}=5 V, V_d=V_s=0 V

4.3.2 Positive Bias Temperature Instability

Nitrogen species passivates the defect states could not easily be seen if device stressed in local side in HCS, hence we continue using PBTI to qualify the whole material. Figure 4-28 and 4-29 show the transfer characteristic and transconductance of control and nitrogen implanted samples before and after PBTI at 25°C. The transfer characteristic in nitrogen implanted one have better sub-threshold swing than control, which would be seen in the latter time evolution description. And now we see the transconductance compare nitrogen to control, the improve percentage after HCS is 34 % but is 69 % for PBTI. The larger improvement could be due to large stress region, and the little passivate effect could be expanded, so that the nitrogen still contribute to passivation by strong Si-N bond in the G_m maximum related grain boundary tail states.

Figure 4-30 and 4-31 show the time evolution threshold voltage shift and sub-threshold swing degradation under PBTI stress. The large threshold voltage shift in nitrogen implanted should have the same reason with HCS, which including nitrogen does not passivate the defect in the HfO_2 and the higher driving current make more the electron trapping opportunity. And for the logarithm time dependent threshold voltage shift in both control and nitrogen implanted sample, suggest that the cause of shift still major contribute from large amount of electron trapping. For the sub-threshold swing degradation, the nitrogen implantation curve exhibit a trend of saturation differ from the control one, which means that interface deep states do not degraded at the latter stress time. Hence, strong Si-N bonds still work on passivate the deep states in the interface. And we also notice that the transfer characteristic of nitrogen implanted sample have non-obvious donor like states creation which perform from the upper sub-threshold region degrade. Hence, strong Si-N bond still have its better passivated ability than strong Si-F bond.

Next, Figure 4-32 and 4-33 show the transfer characteristic of control and nitrogen implanted samples under PBTI stress at 25 ^{o}C and 75 ^{o}C. And we could compare the off state current with control and nitrogen before and after elevate temperature, which exhibit that the nitrogen implanted samples have large off state current. Hence, nitrogen does not passivate the drain side junction very well and would make more the current than control one at higher temperature. Thus the higher thermionic emission current could be seen in the nitrogen sample due to the traps assist tunneling happened.

Finally, the Table 4-7 and 4-8 list the parameters of control and nitrogen samples before and after PBTI stress.

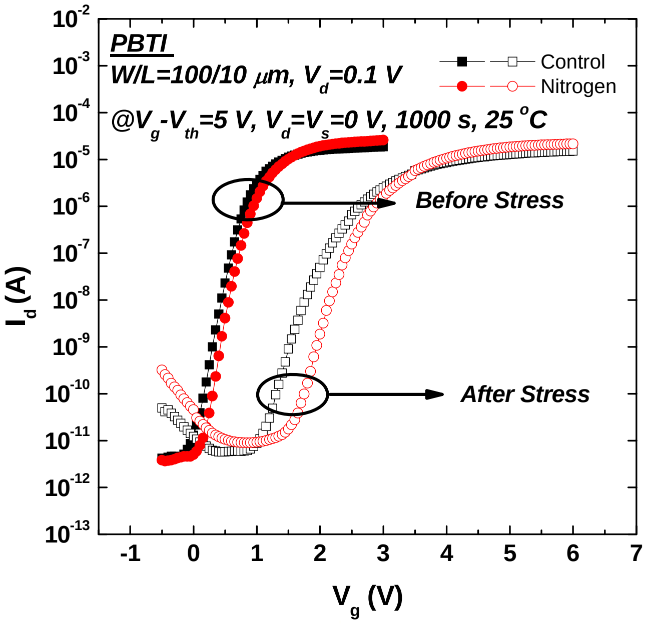

Figure 4-28 Transfer characteristic with and without the nitrogen implantation, before and after 1000 s PBTI at 25 ^{o}C with V_g-V_{th}=5 V, V_d=V_s=0 V

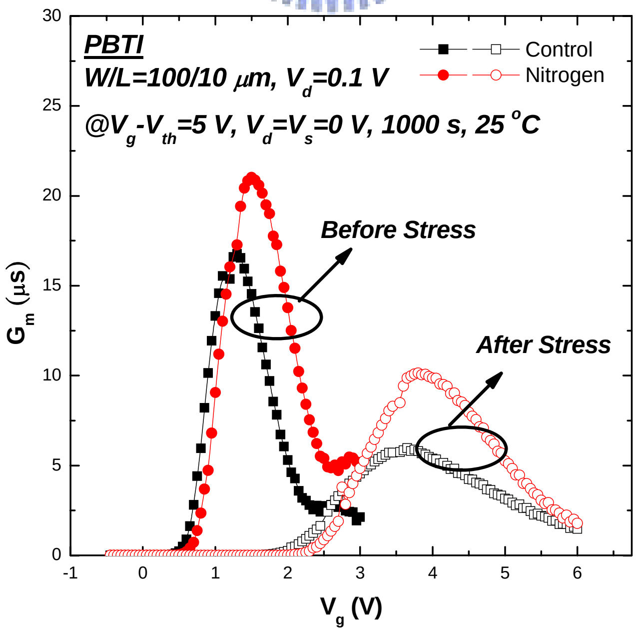

Figure 4-29 Transconductance with and without the nitrogen implantation, before and after 1000 s PBTI at 25 ^{o}C with V_g-V_{th}=5 V, V_d=V_s=0 V

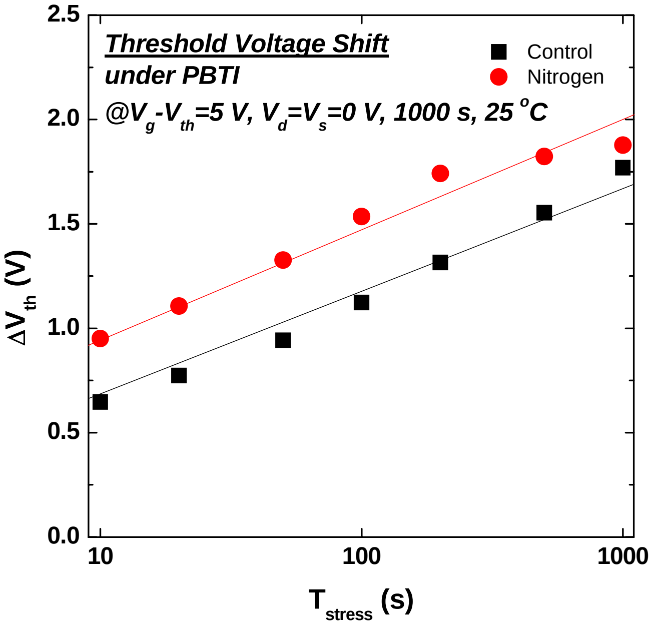

Figure 4-30 Time evolution of threshold voltage shift under PBTI with and without nitrogen implantation

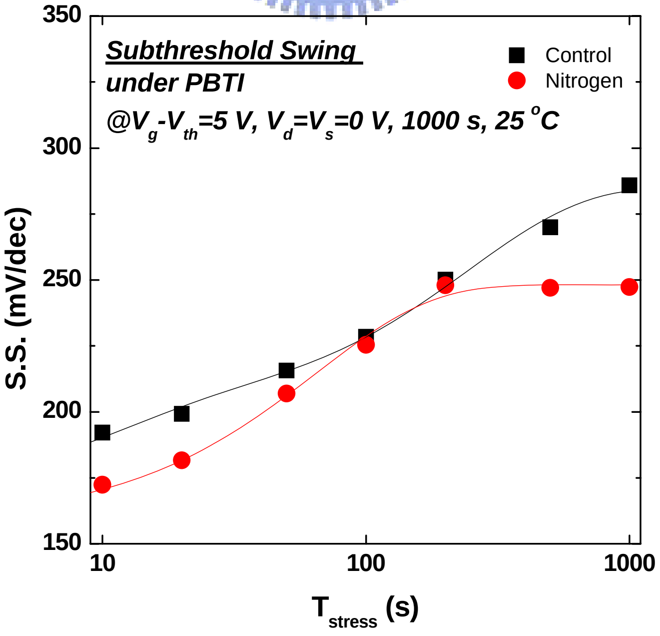

Figure 4-31 Time evolution of sub-threshold swing degradation under PBTI with and without nitrogen implantation

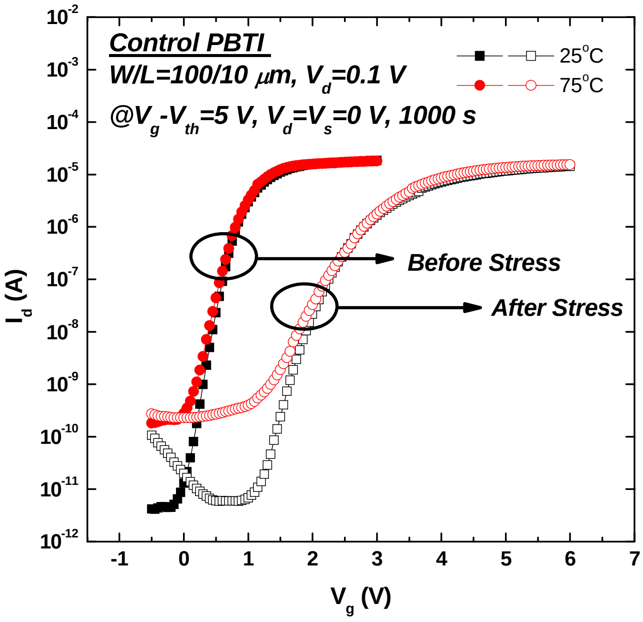

Figure 4-32 Transfer characteristic without nitrogen implantation, before and after 1000 s PBTI at 25 °C and 75 °C with V_g-V_{th}=5 V, V_d=V_s=0 V

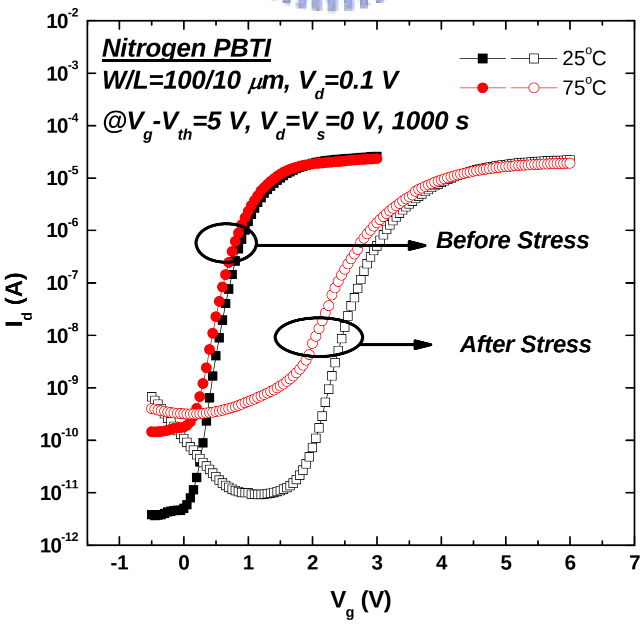

Figure 4-33 Transfer characteristic with nitrogen implantation, before and after 1000 s PBTI at 25 °C and 75 °C with V_g-V_{th}=5 V, V_d=V_s=0 V

	Control Before stress	**Control After stress**	**Nitrogen Before stress**	**Nitrogen After stress**
$I_{on}(10^{-5}A)$	8.92	2.55	9.80	4.26
$I_{off}(10^{-10}A)$	0.55	0.91	0.56	1.06
$I_{on}/I_{off}(10^{5})$	16	2	17	4
S.S.(mV/dec)	148	285	142	247
$V_{th}(V)$	0.85	2.62	0.98	2.85
$G_m(\mu s)$	16.6	5.97	21.0	10.1

Table 4-7 Characteristics of LTPS High-k TFTs with and without nitrogen implantation before and after 1000 s PBTI at 25 °C with V_g-V_{th}=5 V, V_d=V_s=0 V

	Control	**Nitrogen**
$\Delta I_{on}(\%)$	-71	-56
$\Delta I_{off}(\%)$	65	86
ΔS.S.(%)	93	73
$\Delta V_{th}(V)$	1.76	1.87
$\Delta G_m(\%)$	-64	-51

Table 4-8 Characteristics degraded percentage of LTPS High-k TFTs with and without nitrogen implantation under 1000 s PBTI at 25 °C with V_g-V_{th}=5 V, V_d=V_s=0 V

Chapter 5 Conclusion

5.1 Summary

In this thesis, the LTPS high-k TFT devices have been successfully fabricated by the gate-last process. Thanks to the high-k gate dielectric, all devices have the excellent sub-threshold swing which approximately in 135~150 mV/dec. and low threshold voltage about 1-V. Under HCS and PBTI stressing, we found that this gate dielectric, HfO_2, prepared by e-gun, is not good enough and easy to trap charges.

Compared with control devices, all the F-implanted samples under HCS and PBTI show a better electrical characteristic, in terms of less threshold voltage shift under HCS and BPTI stressing, low gate leakage current in HCS and the low gate dielectric capacitance. Based on these observations, we can conclude that the fluorines diffuse into gate dielectric and passivate the defect in it. Second, have better sub-threshold swing than control both in HCS and PBTI, suggesting that strong Si-F bonds can passivate the deep states at the interface. Third, less degradation of transconductance after both HCS and PBTI implies that tail states in grain boundary have been effectively passivated by strong Si-F bond. Finally, the off state current after PBTI under higher temperature of F-implanted TFTs is found better than control one, which means that drain side junction defects have been passivated due to fluorine implanted. From the above result, F-implant into TFT can significantly improve the performance of TFTs.

For the N-Implanted TFTs, the performance does not show the same improvement as those in F-implanted devices. However, it still exhibits better characteristic in the sub-threshold swing compared with control and F-implanted deices after PBTI. Our result show that fluorine does not passivate the donor like state after PBTI, but it does not see in the nitrogen after the same PBTI stress.

Hence, the LTPS high-k TFTs with F- and N-implantation have been investigated under HCS and PBTI stressing in this thesis. The F-implanted LTPS High-k TFTs have the better performance and reliability than N-implanted ones. Hence, the fluorine implantation seems to be a promising approach to obtain a high performance LTPS high-k TFTS.

Since high-k gate dielectric, HfO_2, deposited by e-gun, is not good enough in this study, how to improve the integrity of HfO_2 in the low temperature process is worthy for future study.

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Biography

I was born in September 1, 1983 in Tainan city of R. O. China. When I studied in my high school, Tainan Fist Senior High School, my teacher who teaches physics bring me into the interesting world. From then on, I was really love to find out the physical mechanism behind the phenomena. In 2005, I completed degree of Bachelor of Science in Applied Physics at National Chia-Yi University, R. O. China. I recommended myself into the Institute of Electrophysics at National Chiao-Tung University, R. O. China at the same year. Here, I was major in semiconductor device and process in T.S Chao's group. And my research was focus on how to improve the performance and reliability of TFTs. In this two year, I have been published the related results in several Letter and Conference. Now, I finished my research and received degree of master in physics at NCTU on June, 2007.