# 國　立　交　通　大　學

電子物理學系 電子物理研究所

碩士論文

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# 氮化矽層內嵌奈米矽晶體之SONOS型記憶體

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## 摘要

對廣泛使用的非揮發性記憶體 — 快閃記憶體而言，通常會遇到兩個問題：一是在元件尺寸繼續微縮下之瓶頸，由於尺寸微縮後穿隧氧化層(或閘極氧化層)之厚度亦隨之下降，如此雖可得到較快的讀寫速度，但電荷保存時間亦隨之下降，故須在兩者之間取得平衡點；二是在經過多次讀寫後在穿隧氧化層品質容易劣化而產生漏電路徑，一旦有一條漏電路徑產生，所有儲存在浮動閘極(Floating Gate)的電荷都會經由此漏電路徑而全部流失掉。為了克服上述兩個問題，主要有兩種改良的方法被提出，一是SONOS 非揮發性記憶體，另一種是奈米晶體(量子點)非揮發性記憶體。

在本文中，一個將前述兩種改良非揮發性記憶體結合之新記憶體被提出。利用半導體奈米點作為電荷儲存的單元。在元件的反覆操作下，即使穿隧氧化層產生缺陷或漏電路徑，所損失掉的儲存電子，僅是單一奈米點的電子漏失，對整體元件特性的影響並不明顯。因此，穿隧氧化層的厚度得以縮減，使得操作速度增快，元件積集度提升，元件可操作的次數(Endurance)以及保存時間(Retention)也同時得到改善。當電子儲存在奈米點時，由於庫倫阻絕(Coulomb Blockade)效應，儲存的電子會限制後續電子的注入。奈米點的庫倫阻絕效應使得記憶體元件的儲存及操作更加的穩健。當閘極偏壓使通道產生反轉層後，通道的電子藉由直接穿隧效應或是F-N穿隧效應通過穿隧氧化層，而讓奈米點捕獲，是為寫入動作。當閘極偏壓反向時，儲存的電子變經由穿隧氧化層回到通道，是為抹除動作。藉由電容-電壓(C-V)量測，當電子注入奈米點之後，元件之起始電壓會發生偏移，此偏移的量即($\triangle V_{FB}$=6.25V)定義為記憶體元件的記憶窗(Program Window)。

本研究提出利用氮化矽內嵌奈米矽晶體(Si-NCs)來取代SONOS非揮發性記憶體中的氮化矽($Si_3N_4$)薄膜，如此便完成了將兩種記憶體結合之新型記憶體。由於奈米矽晶體及內嵌奈米矽晶體之氮化矽皆可儲存電荷，故新型記憶體的記憶窗比單純只有氮化矽薄膜來得更大，電荷保存能力也較佳。在改變奈米矽晶體尺寸大小，其它條件不變之下，尺寸愈大的奈米矽晶體之記憶窗愈大，但記憶窗愈大之記憶體電荷保存能力沒有愈佳，因此本研究尋找適當大小的奈米矽晶體之新記憶體元件，使之更容易達到十年的電荷保存時間。

我們亦針對可靠度問題對我們的元件進行測試。我們分別在室溫、150℃以及250℃高溫進行資料保存能力測試。在室溫及150℃方面，單純只有氮化矽薄膜與新型記憶體均有好的資料儲存能力，推測十年後的電荷保存能力可維持在75%以上。在250℃高溫，由於穿隧氧化層之品質較差所以導致部份儲存電荷流失，但奈米矽晶體優異的資料儲存能力仍優於氮化矽薄膜。

# Embedded Si-NCs in $Si_3N_4$ for SONOS Memories

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## Abstract

For non-volatile memories (NVM) generally, there are two limitations encountered at the present time. (1) The limited potential for continued scaling of the device structure: this scaling limitation stems from the extreme requirements on the tunnel oxide layer. To balance between program/erase speed and retention time, there is a trade-off between speed and reliability for the optimal tunnel oxide thickness. (2) The quality and strength of tunnel oxide after plenty of program/erase cycles, once a leaky path has been created in tunnel oxide, all charges stored in the floating gate will be lost. Therefore, two approaches, the silicon-oxide-nitride-oxide-silicon (SONOS) and the nanocrystal non-volatile memory device, have investigated to overcome this oxide quality limit of the conventional floating gate non-volatile memories.

A combination of SONOS and nanocrystal non-volatile memory device is proposed in this study. To alleviate the scaling limitation of the conventional FG device while preserving the fundamental operating principle of the memory, we have studied the distributed charge storage approach such as the nanocrystal non-volatile memory. Each nanocrystal will typically store only a handful of electrons; collectively the charges stored in these dots control the channel conductivity of the memory device. Nanocrystal charge storage offers several advantages, the main one being the potential to use thinner tunnel oxide without sacrificing non-volatility. This is a quite attractive proposition since reducing the tunnel oxide thickness is a key to lowering operating voltages and/or increasing operating speeds. The improved scalability results not only from the distributed nature of the charge storage, which makes the storage more robust and fault-tolerant, but also from the beneficial effects of Coulomb

blockade. A local leaky path will not cause a fatal loss of information for the nanocrystal non-volatile memory device. Also, the nanocrystal memory device can maintain good retention characteristics and lower the power consumption.

A Si-NCs embedded in $Si_3N_4$ film is introduced to replace the nitride film in SONOS structure. Because there are two charge-storage node source, the nodes in Si-NCs in $Si_3N_4$ dielectric film, comparing to SONOS and Si-NCs memory, a large memory window and good retention characteristics can be obtained. Changing the Si-NCs size, size large memory window large, but memory window large which have not good retention characteristics. When a memory device has a proper Si-NCs size, it is easier to meet the requirement of 10-year retention. And, we hope this approach can improve the two limitation mentioned above.

We also discussed the data retention issues. We measured the data retention at room temperature, 150℃ and high temperature 250℃, respectively. At room temperature and 150℃, SONOS and Si-NCs memory show good capability of data retention. But at high temperature 250℃, bad tunnel oxide quality resulted in charge loss, but the data retention of Si-NCs SONOS memories is still superior to the SONOS.

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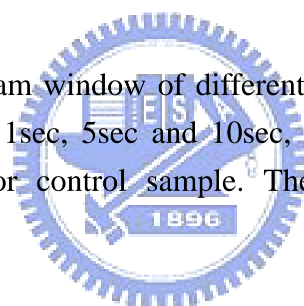

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**Fig. 3-15** Data retention characteristic of different sample for different tunnel oxide film when programming △Vt=2V at T=250℃. (a) control sample, (b) Si-NCs_2min sample and (c) Si-NCs_1m30s sample.

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**Fig. 3-21** Programming gate disturbance characteristic of different sample at $V_G$=7V. This gate length and width are 0.4 m and 10 m. The tunnel oxide is dry $O_2$ 2.5nm by vertical-furnace. The Vt shift of gate disturbance is lower than 0.4V for 1000s stress with $V_G$=7V.

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# *Chapter 1 Introduction*

## 1.1 Brief Introduction of SONOS Memory Cell

SONOS cell offers several advantages over conventional floating gate memory cells: higher density, simple processes, low-voltage operation, elimination of the drain-induced turn of effect, multi-bit operation, and no floating gate coupling effect [1-5]. For the SONOS cell, the endurance and data retention [6] are the two most important reliability issues. Scaled SONOS can be operated at a lower bias; however, data retention has been critical for the scaling of ONO layers [7-9] SONOS Flash memory cell which Fowler-Nordheim tunnel program by electron and direct tunnel erase by hole [10] has been proposed for years. As shown in Fig.1-1, the carriers are stored in the traps of the nitride layer between the top and the bottom oxides. Besides, its large cell size ($6F^2$, F=feature size) and slow program/erase speed limit its applications. Recently, SONOS cell has evolved into a 2-bits-per-cell storage architecture (NROM [11]) by utilizing the localized charge trapping effect of nitride. Localized trapping nitride trapping storage memory cell enables a memory cell to hold twice as much data as the standard memory cell. But, the quality and strength of tunnel oxide after plenty of program/erase cycles, once a leaky path has been created in tunnel oxide, some region charges stored in the nitride will be lost.

Eitan *et al*. [11] proposed a novel localized 2-bit nonvolatile memory cell named as NROM™. The two-bit operation is performed by charge storage on source-side and drain-side silicon nitride layer. NROM Flash memory cell structure is shown in Fig.1-2, and the operation principle is shown in Table 1-1. NROM programs its memory cell by channel hot electron injection as conventional NOR-type floating gate memory does, which is suitable for code storage applications. Erase is done by band-to-band tunneling induced hot-hole injection. A novel reverse read scheme [11] is introduced to realize physically 2-bits-per-cell

operation. Although NROM cell has many advantages over conventional floating gate memory cells, it can only be applied to code storage application due to its high power consumption and slow program speed in program operation. Previous works [12-13] reveal that reliability issues including read disturb, over erasure and cell retention after cycling are major challenges. Besides, 2-bit interaction effect resulted from the reverse read scheme also limits the device scalability [13].

To improve the device performance of the SONOS technology, the optimization of the ONO stack has been the main considerations currently. She *et al*.[14] demonstrated jet vapor deposited (JVD) silicon nitride as a tunnel dielectric for flash memory device application. Compared to conventional devices with $SiO_2$ tunnel dielectric, faster programming speed as well as better retention time is achieved with low programming voltage [15]. Resisinger *et al*. [16] proposed a SONOS structure with a $p^+$ doped silicon gate instead of the commonly used $n^+$ gate. In the erase mode, the $p^+$ gate prevents the Fowler-Nordheim tunneling of electrons from the conduction band of the gate into the silicon nitride film.

The consecutive scaling of the SONOS technology also drives the industry of flash memory approaching the high density, low power consumption, and improved data retention and endurance EEPROM's [17]. Differing from the storage element of silicon nitride of SONOS technology, King *et al*. proposed another charge storage element such as silicon rich oxide for dynamic or quasi-nonvolatile memory application [18]. Using the traps in the silicon rich oxide layer for charge storage, the symmetrical write/erase characteristics were achieved.

## 1.2 Introduction of Nanocrystal Nonvolatile Flash Memory

Non-volatile memory (NVM) devices based on localized charge storage have received much attention due to lower program/erase (P/E) voltage, better scalability and retention characteristics. For future charge trap NVM devices, one of the most important issues is to achieve both high P/E speed and long retention time [19].

Recently, Metal-oxide-semiconductor (MOS) memory structures based on silicon nanocrystals have attracted a great interest both for potential applications in future integrated circuit devices and for new physical phenomena. NVM devices with silicon nanocrystals (Si-NCs) have been investigated to improve retention characteristics [20-21]. Nanocrystal memories can achieve better reliability and higher bit density than conventional non-volatile memories and have thus been drawing much attention. Given a large number of nanocrystals, the cell is immune to local defects of the tunnel oxide. Furthermore, with hot-carrier programming, charge storage in each cell can be localized, enabling 2-bit/cell operation [20].

Nanocrystal nonvolatile flash memories, shown in Fig. 1-3, are one particular implementation of storing charges by dielectric-surrounded nanocrystals. In this kind of memory structures, silicon nanocrystals as floating gate are embedded in the nitride layer between the control gate and the source-drain conduction channel, and charges direct-tunneling through much thin oxide into and off the nanocrystals shift the device threshold [22]. For the application of non-volatile memory device, in a sense, a long charge retention time at room temperature is the most important [23-24].

As compared to conventional stacked gate NVM devices, nanocrystal charge storage offers several advantages, the main one being the potential to use thinner tunnel oxide without sacrificing nonvolatility. This is a quite attractive proposition since reducing the tunnel oxide thickness is a key to lowering operating voltages and/or increasing operating speeds. This claim of improved scalability results not only from the distributed nature of the charge storage, which makes the storage more robust and fault-tolerant, but also from the beneficial effects of Coulomb blockade [25]. One way to exploit this advantage is to use a higher drain bias during the read operation, thus improving memory access time. Of particular importance is the low capacitive coupling between the external control gate and the nanocrystal charge storage layer. This does not only results in higher operating voltages, thus offsetting the benefits of the thinner tunnel oxide, but also removes an important design parameter (the coupling ratio)

typically used to optimize the performance and reliability tradeoff. Unlike volume distributed charge traps (ex: nitride in SONOS NVM device, nanocrystals be deposited in a two-dimensional 2-D) layer at a fixed distance from the channel separated by a thin tunnel oxide. By limiting nanocrystals deposition to just one layer and adjusting the thickness of the top blocking dielectric, charge leakages to the control gate from the storage nodes can be effectively prevented.

## 1.3 Motivation

The Semiconductor Industry Association (SIA) International Technology Roadmap for Semiconductors (ITRS) indicates the difficult challenge, beyond the year 2005, for nonvolatile semiconductor memories is to achieve reliable, low-power, low-voltage performance [26]. For NVM, two limitations encountered at the present time are: (1) the limited potential for continued scaling of the device structure. This scaling limitation stems from the extreme requirements put on the tunnel oxide layer. In order to get balance between program/erase speed and retention time, there is a trade-off between speed and reliability to get the optimal tunnel oxide thickness. (2) the quality and strength of tunnel oxide (or tunnel dielectric) after plenty of program/erase cycles. Once a leaky path has been created in tunnel oxide, all the charges stored in the floating gate will be lost. Therefore, two suggestions, the SONOS and the nanocrystal non-volatile memory devices, are proposed to overcome this oxide quality limit of the conventional floating gate structure. These technologies replace the floating gate structure with a great number of charge storage nodes in the dielectric or in the nanocrystal. Unlike the floating gate, the local leaky path will not cause the fatal loss of information for the nanocrystal NVM device. This effectively prevents the leakage of all the stored charges out of the floating gate. In this thesis, a combination of SONOS and nanocrystal NVM devices is proposed. Embedded Si-NCs in $Si_3N_4$ film is introduced to replace the nitride film in SONOS structure. After thermal processes, thin amorphous silicon

nucleation in the $Si_3N_4$ film will assemble to form Si-NCs embedded in the $Si_3N_4$ film. Because there are two charge-storage node sources, the nodes in Si-NCs and in $Si_3N_4$ dielectric film, comparing to SONOS and Si-NCs NVM device, a deep trap can be obtained. It is easier to meet the requirement of retention of 10 years. And, hope to solve the two limitations mentioned above.

## 1.4 Organization of This Thesis

The organization of this thesis is separated into four chapters.

In Chapter 1, A brief introduction are introduced.

In Chapter 2, we introduced the capacitance fabrication, and experimental measurement.

In Chapter 3, we demonstrated a SONOS memory with Si-NCs trapping layer. We will show the basic characteristics of the Si-NCs SONOS memory and compare the capacitance performance with various tunnel oxide film thickness and quality, including program window, data retention. We will discuss the influence of different tunnel oxide.

In Chapter 4, the conclusion is given.

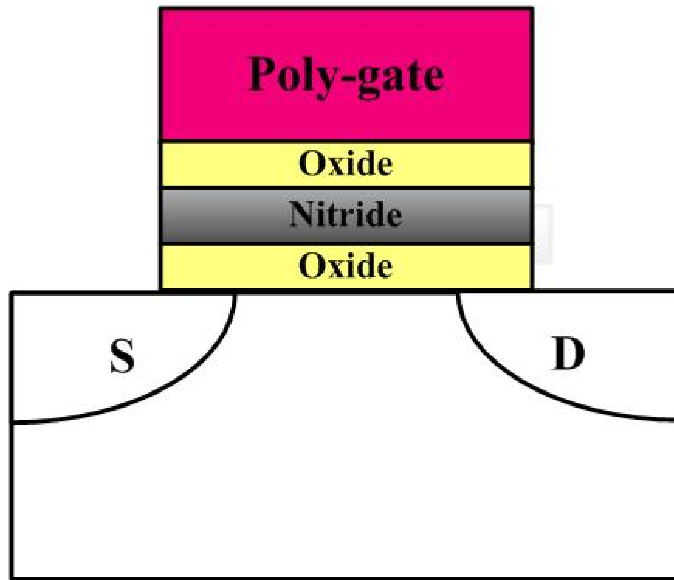



**Fig. 1-1** The cell structure of a nitride storage flash memory cell.

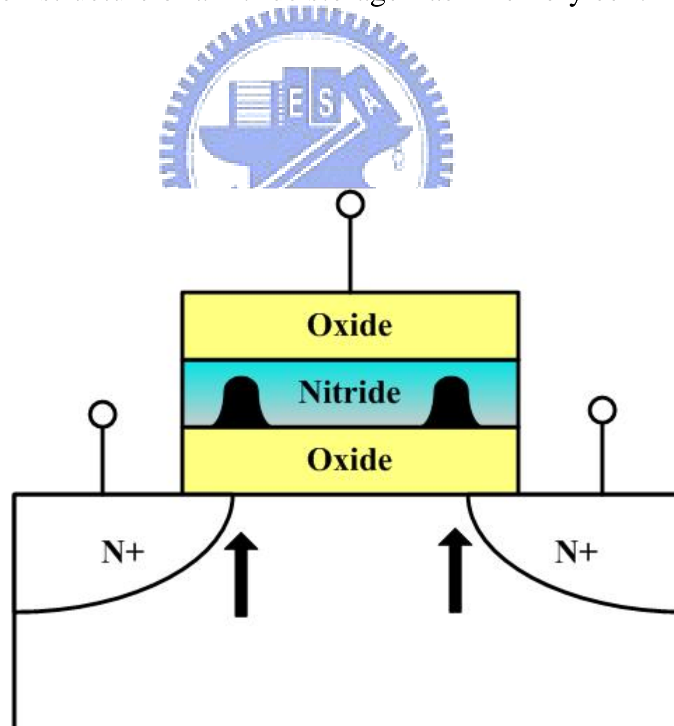



**Fig. 1-2** Schematic representation of a NROM cell with physically 2-bits storage. The shaded area in the nitride layer represents stored charges.

**Table 1-1** Operation bias conditions of a NROM cell.

| | | Program | Erase | Read |
|---|---|---|---|---|
| Bit 1 | $V_g$ | 11 V | -3 V | 2.5 V |
| | $V_d$ | 5 V | 8 V | 0 V |
| | $V_S$ | 0 V | 0 V | >1.5 V |
| Bit 2 | $V_g$ | 11 V | -3 V | 2.5 V |
| | $V_d$ | 5 V | 8 V | 0 V |
| | $V_S$ | 0 V | 0 V | >1.5 V |

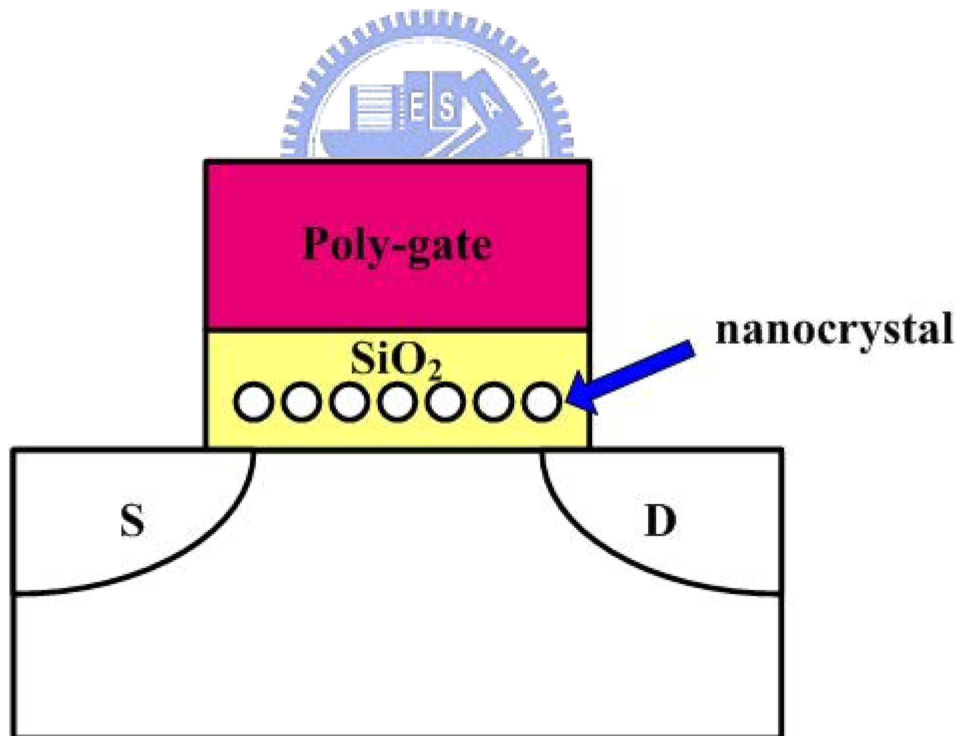



**Fig. 1-3** The device structure of nanocrystal non-volatile memory.

# *Chapter 2*

# *Experiment Procedures*

# *and Electric Characteristic of Capacitor*

## 2.1 Capacitor Fabrication

The schematic diagram of the fabrication process is illustrated in Fig.2-1.Three different types of tunnel oxide are grown on p-type (100) silicon substrates after RCA cleaning. (1) 3-nm thick $SiO_2$ film was thermally grown in dry $N_2O$ atmosphere by horizontal-furnace. (2) 2.5-nm thick $SiO_2$ film was thermally grown in dry $N_2O$ atmosphere by vertical-furnace. (3) 2.5-nm thick $SiO_2$ film was thermally grown in dry $O_2$ atmosphere by vertical-furnace. Then, a 3-nm thick silicon nitride films was deposited as the trapping layer in a LPCVD system using $SiH_2Cl_2$ and $NH_3$ as source for 30 and 130 sccm, respectively. Si-NCs were formed on the 3-nm thick silicon nitride films immediately by LPCVD for 2-min and 1-min and 30-sec. The deposition of amorphous silicon nucleation was kept at 550°C and the pressure was controlled at 100-mTorr. The flow rate of the reaction gas of $SiH_4$ was 85-sccm. Then, the silicon nitride capped on the Si-NCs was 4-nm. During this high temperature period, the previously deposited thin amorphous silicon nucleation was crystallized and then formed into poly-Si nanocrystals, which were embedded in silicon nitride films as show in Fig. 2-2. The formation of Si-NCs was confirmed by atomic force microscopy (AFM) as shown in Fig's.2-3 (a)-(c). We estimated size and density of Si-NCs_1m30s and Si-NCs_2min sample in Table 2-1. A blocking oxide about 20-nm was then deposited using high density plasma chemical vapor deposition (HDPCVD) oxide. A 200-nm thick poly-Si was deposited to serve as the gate electrode by LPCVD. Subsequently, the $n^+$ poly-Si gate was formed by phosphorous ion implanted at 40-keV to a dose of $5x10^{15}$ $cm^{-2}$. Also, the sample without Si-NCs was fabricated as a control sample.

After phosphorous implantation, activation was formed at 900°C for 30 minutes. Then, the poly-Si gate electrode and the Si-NCs trapping layer with blocking oxide were etched by poly-Si dry etcher (TCP- 9400) and the oxide dry etcher (TEL-5000). The capacitance with Si-NCs memory was made.

## 2.2 Typical Program Window Parameter Extraction

In this section, the methodology of extracting typical parameters, such as program window from device characteristics, are briefly introduced. Plenty ways are used to determinate the program window which is the most important parameter of memory devices. The method to determinate the program window in my thesis is the *constant capacitance method* that the voltage at a specific gate voltage $V_G$ is taken as the program window. This technique is easy and can give a program window close to that obtained by the capacitance-voltage hysteresis method. Typically, the program window $\triangle V_{FB} = V_{FB}'-V_{FB}$ where $V_{FB}$ is a normalized flat-band voltage. Here, $V_{FB}'$ is the flat-band voltage after program condition for all capacitance to extract the program window of Si-NCs memory.

## 2.3 Measurement Equipment Setup

The experimental setup of for the I-V and threshold voltage characteristics measurement of the SONOS is illustrated in Fig.2-4. As shown Fig.2-4, the characterization apparatus with semiconductor characterization system (KEITHLEY 4200), one channel pulse generator (Agilent 81110A), low leakage switch mainframe (KEITHLEY 708A), and a probe station provide an adequate capability for measuring the device I-V characteristics and executing the SONOS memory cell program/erase operation.

The KEITHLEY 4200 equipped with programmable source-monitor units (SMU) and provides a high current resolution to pico-ampere range facilitates the gate current measurement, subthreshold characteristics extraction, and the saturation drain current

measurement. The one channel Agilent 81110A with high timing resolution provides one pulse level for transient and P/E cycling endurance characterization. Another pulse level is provided by KEITHLEY 4200. The KEITHLEY 708A configured a 10-input×12-output switching matrix, switches the signals from the KEITHLEY 4200 and the Agilent 81110A to device under test in probe station, automatically. In addition, the $C^{++}$ is used as the program language to achieve the KEITHLEY 4200 control of these measurement instruments [27].

## 2.4 Characteristic of Program/Erase

### 2.4.1 Program Mechanism

Fowler-Nordheim tunneling is a field-assisted carrier tunneling mechanism [28], when a large positive voltage is applied across a poly-ONO-substrate structure, its band structure will be influenced as indicated in Fig.2-5. Due to high electrical field, electrons in the Si conduction band as triangular energy barrier with a width dependent on applied electric field. At sufficient high fields, the width of barrier becomes small enough to tunnel through the barrier from the Si conduction band into Si-NCs electron trap center or nitride trap layer.

Fig.2-6 shows program window characteristic of different samples. The program window of control, Si-NCs_1m30s and Si-NCs_2min are about 3.58-V, 6.25-V and 8.98-V, respectively. Summary for program window of different sample when program voltage $V_G$=25-V and 10-sec program time in Table 2-2. The program window of Si-NCs is larger for control sample. And the larger Si-NCs size has more trapping sites for large memory window. Fig's.2-7 (a)-(c) exhibit program window characteristic of different samples when program voltage was set at 15-V, 20-V and 25-V and stressed for 1-sec, 5-sec and 10-sec, respectively. The tunnel oxide is dry $N_2O$ 3-nm by horizontal-furnace. Fig's. 2-8 (a)-(c) show program window characteristic of different samples when program voltage was set at 15-V, 20-V and 25-V and stressed for 1-sec, 5-sec and 10-sec,

respectively. The tunnel oxide is dry $N_2O$ 2.5-nm by vertical-furnace. And Fig's. 2-9 (a)-(c) exhibit program window characteristic of different samples when program voltage was set at 15-V, 20-V and 25-V and stressed for 1-sec, 5-sec and 10-sec, respectively. The tunnel oxide is dry $O_2$ 2.5-nm by vertical-furnace. Summary for program window of different sample when program voltage 15-V, 20-V and 25-V and stress 1-sec, 5-sec and 10-sec, respectively. The program window of Si-NCs is larger for control sample. The tunnel oxide is dry $N_2O$ 3-nm by horizontal-furnace.

### 2.4.2 Erase Mechanism

Fig. 2-10 exhibit erase characteristic of different negative gate bias. The gate bias $V_G$= -15-V, t=10-sec,can be erased $\triangle V_{FB}$ shift about -0.5-V. But, when the gate bias increasing -20-V, t=1-sec, because gate injection effect be programmed $\triangle V_{FB}$ shift about 0.8-V. Fowler-Nordheim tunneling is a field-assisted carrier tunneling mechanism, when a large negative voltage is applied across a poly-ONO-substrate structure, its band structure will be influenced as indicated in Fig.2-11.

Because the capacitor can only be programmed/ erased by Fowler-Nordheim tunneling mechanism, the quality of blocking oxide is important for this high field stressing. We found that the quality of our blocking oxide is not so good, causing electron injection into oxide which makes the erasing not so easy. To look for some other material or better quality blocking oxides is necessary. Using high-k material ($Al_2O_3$, $HfO_2$ …etc) or HTO to replace already existed blocking oxide and using $p^+$ poly-Si gate or larger work function metal gate would to replace $n^+$ poly-Si gate be helpful[29-32].

## 2.5 Characteristic of Retention

### 2.5.1 Characteristic of Retention for Different Temperature

Data retention is an important reliability issue of SONOS memories. In general, retention capability of SONOS memories has to be checked by using accelerated test that

usually adopts high electric fields and high temperature [33]. In this section, we will discuss data retention of capactior after programming with different temperature. In general, the flash memory cells are required for a long 100,000 seconds. Timing is known to cause fairly uniform wear-out of cell performance due to the oxide damage.

Fig's. 2-12 (a)-(c) show retention characteristic of different temperature for $\triangle V_{FB}$=2-V. The tunnel oxide of 3-nm was grown in dry $N_2O$ by horizontal-furnace. Fig's. 2-13 (a)-(c) exhibit retention characteristic of different temperature for $\triangle V_{FB}$=2-V. The tunnel oxide of 2.5-nm was grown in dry $N_2O$ by vertical-furnace. Fig's. 2-14 (a)-(c) show retention characteristic of different temperature for $\triangle V_{FB}$=2-V. The tunnel oxide of 2.5-nm was grown in dry $O_2$ by vertical-furnace. We can clearly see that the memory window narrows to about 2-V after $10^4$ seconds for all samples.

### 2.5.2 Characteristic of Retention for Different Si-NCs Sizes

In this section, we will discuss data retention for capactior after programming with different Si-NCs sizes. In general, the flash memory cells are required to keep the charge for $10^4$ seconds. Timing is known to cause fairly uniform wear-out of cell performance due to the oxide damage.

Fig's. 2-15 (a)-(c) show retention characteristic of different Si-NCs sizes for $\triangle V_{FB}$=2-V. The tunnel oxide of 3-nm was grown in dry $N_2O$ by horizontal-furnace. Fig's. 2-16 (a)-(c) exhibit retention characteristic of different Si-NCs sizes for $\triangle V_{FB}$=2-V. The tunnel oxide of 2.5-nm was grown in dry $N_2O$ by vertical-furnace. Fig's. 2-17 (a)-(c) show retention characteristic of different Si-NCs sizes for $\triangle V_{FB}$=2-V. The tunnel oxide of 2.5-nm was grown dry $O_2$ by vertical-furnace. The memory window narrows to about 2-V after $10^4$ seconds for all samples. We can clearly see that the best data retention is Si-NCs_1-min and 30-s sample.

### 2.5.3 Characteristic of Retention for Different Tunnel Oxide

In this section, we will discuss data retention for capactior after programming with

different tunnel oxide. In general, the flash memory cells are required to keep the charge for $10^4$ seconds. Timing is known to cause fairly uniform wear-out of cell performance due to the oxide damage.

Fig's. 2-18 (a)-(c) show retention characteristic of different tunnel oxide thickness for $\triangle V_{FB}$=2-V at T=25°C. Fig's. 2-19 (a)-(c) exhibit retention characteristic of different tunnel oxide thickness for $\triangle V_{FB}$=2-V at T=85°C. Fig's. 2-20 (a)-(c) show retention characteristic of different tunnel oxide thickness for $\triangle V_{FB}$=2-V at T=150°C. The memory window narrows to about 2-V after $10^4$ seconds for all samples. It is clearly to see that the best data retention is tunnel oxide for dry $N_2O$ 3-nm by horizontal-furnace.

## 2.6 Summary

For the program window, Si-NCs has more trapping sites than SONOS memory. The program window of Si-NCs is larger for control sample. And the larger Si-NCs size has more trapping sites similar to floating gate for large memory window.

For the data retention, thermionic emission, direct tunneling and trap-to-trap tunneling, in relating to the data loss, are the three dominant leakage components [34-35]. The reduction of the programmed flat band voltage is due to trap generation in the oxide and also interface state generation between tunnel oxide and channel interface, which are usually called electron degradations. In our capacitor, the Si-NCs memory window still maintains quite about 2-V even through stressed for $10^4$ seconds.

At temperature T=25$^o$C and T=85$^o$C, all cases presented good retention characteristics but charge loss is serious for control sample than Si-NCs of capacitor sample at high temperature. This also shows that the trapping capability of Si-NCs trapping layer is very excellent. On the other hand, we observed larger charge loss percentage for ten years when using accelerated test at temperature T=150$^o$C. This charge loss is due to the poor quality of tunnel oxide which results in many leakage current paths.

For different tunnel oxides, all cases presented good retention characteristics but charge loss is serious for tunnel oxide by dry $O_2$ 2.5-nm than $N_2O$ 2.5-nm and 3-nm sample. This also shows that the quality of tunnel oxide of 3-nm grown by dry $N_2O$ is very excellent. On the other hand, we observed larger charge loss percentage for ten years when using accelerated test for tunnel oxide of 2.5-nm grown in dry $O_2$ sample. Based on the above result, we know the quality of dry $N_2O$ 3-nm by horizontal-furnace is better than that of dry $O_2$ 2.5-nm by vertical-furnace [36-37].

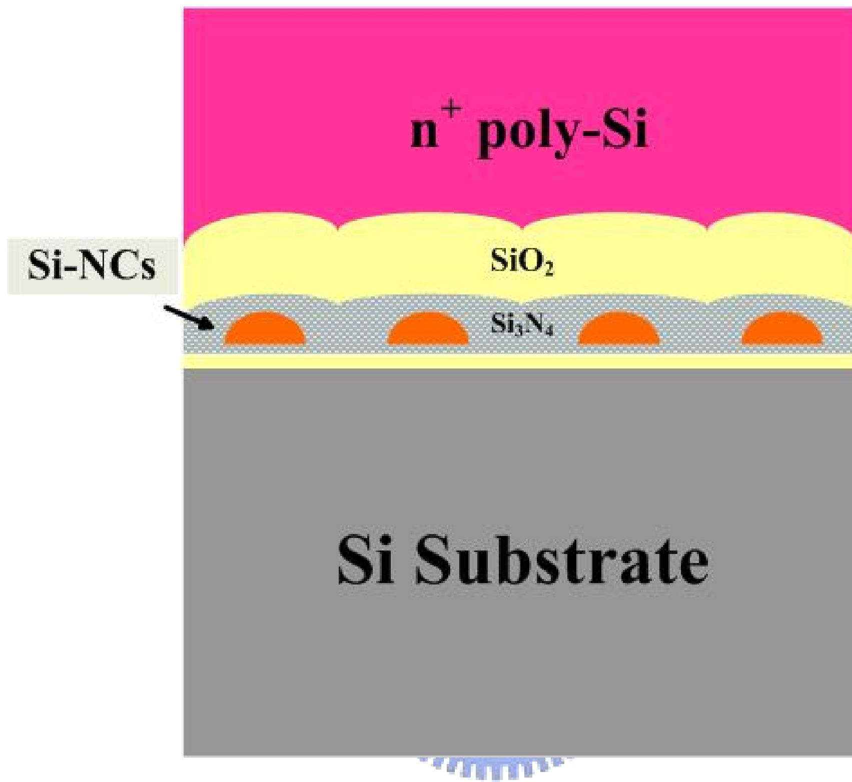
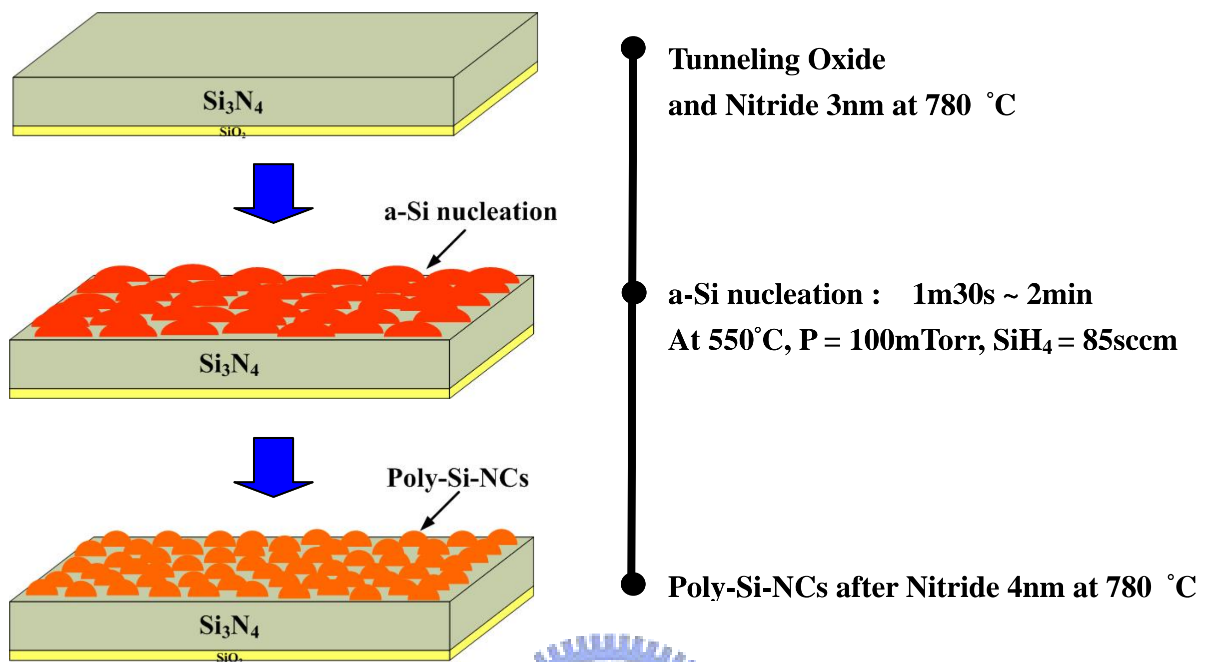



**Fig. 2-1** Structure of Si-NCs SONOS memory. During the nitride deposition step, the Si-NCs trapping layer was crystallized and Si-NCs embedded in $Si_3N_4$ were formed.



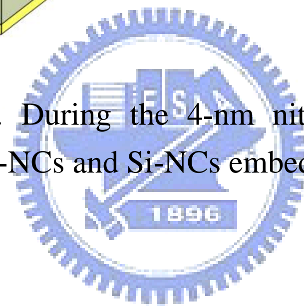
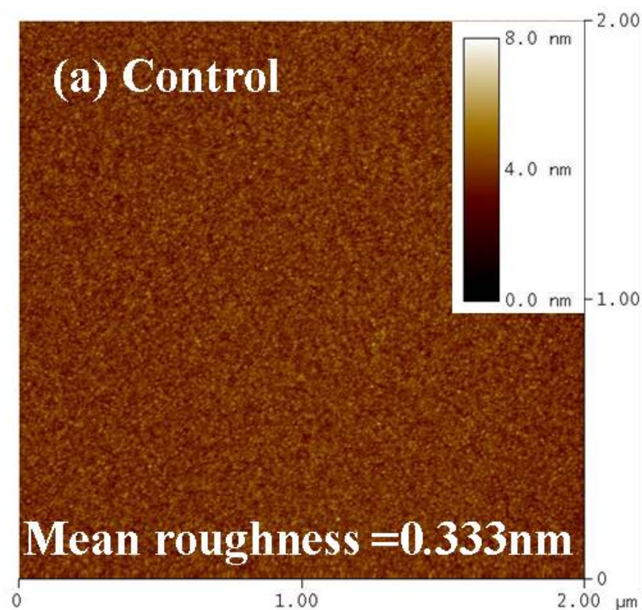
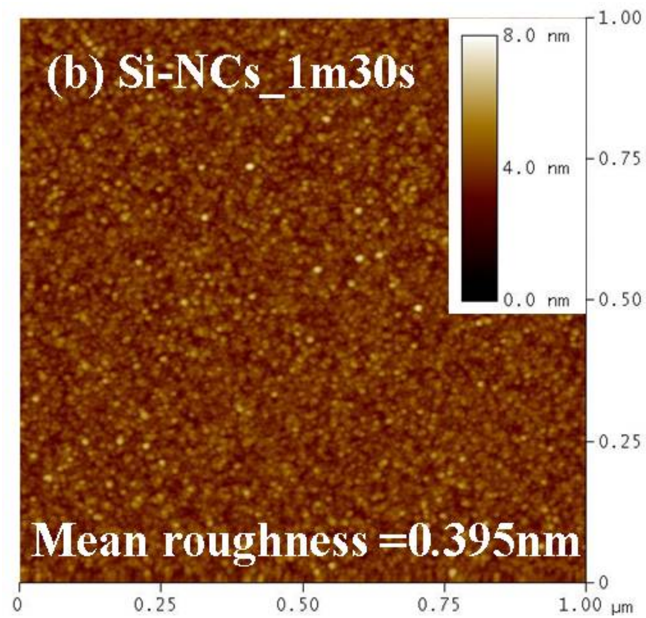




**Fig. 2-2** Si-NCs formation. During the 4-nm nitride deposition step, the a-Si nucleation convert to poly-Si-NCs and Si-NCs embedded in $Si_3N_4$ were formed.




(a)

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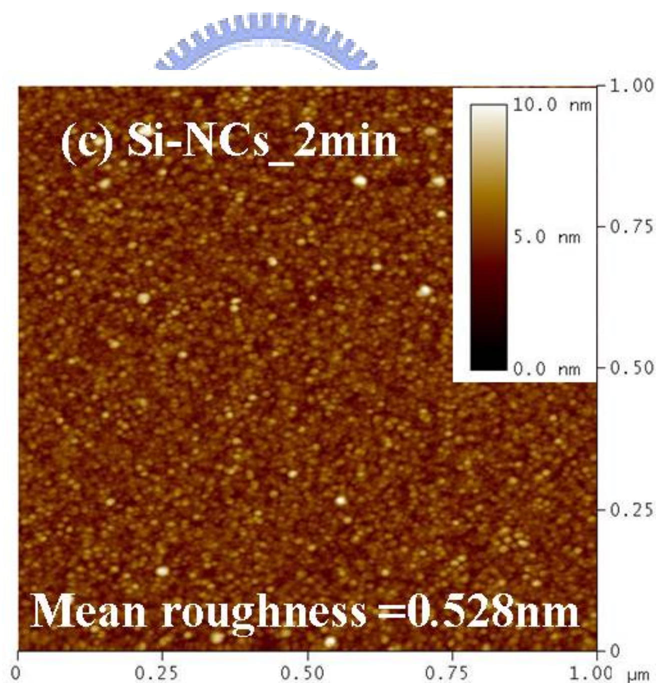



**(c)**

**Fig. 2-3** AFM pictures of Si nanocrystals deposited on $Si_3N_4$ (a) control sample (b) Si-NCs_1m30s sample and (c) Si-NCs_2min sample, with the same growth conditions. The densities are, respectively, 6.7x$10^{11}$ and 3x$10^{11}$ $cm^2$. The diameters are about, respectively, 8 and 10 nm.

**Table 2-1** Size and density of Si-NCs_1m30s and Si-NCs_2min sample.

| sample | Size( nm ) | Density( $1/cm^2$ ) |
|---|---|---|
| Si-NCs_1m30s | ~8 | $6x10^{11}$ |
| Si-NCs_2min | ~10 | $3x10^{11}$ |

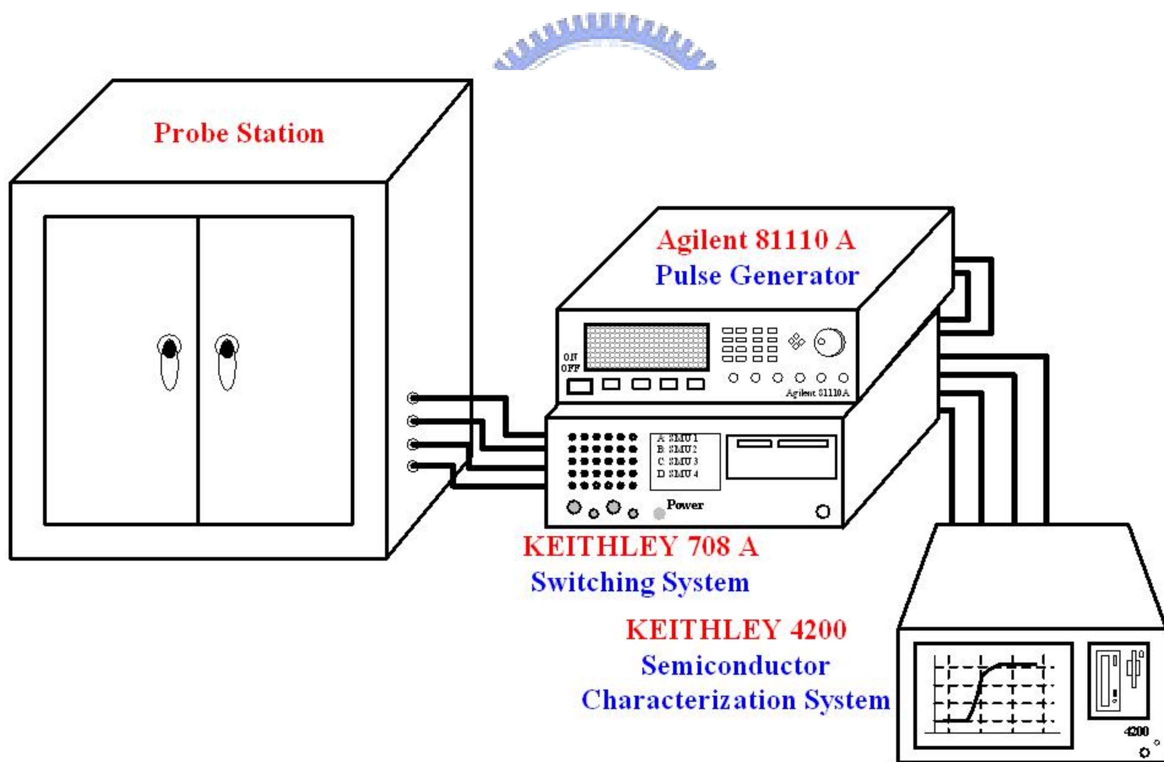



**Fig. 2-4** The experimental setup for the transfer characteristic and program/erase characteristic of SONOS with Si nanocrystals memory.

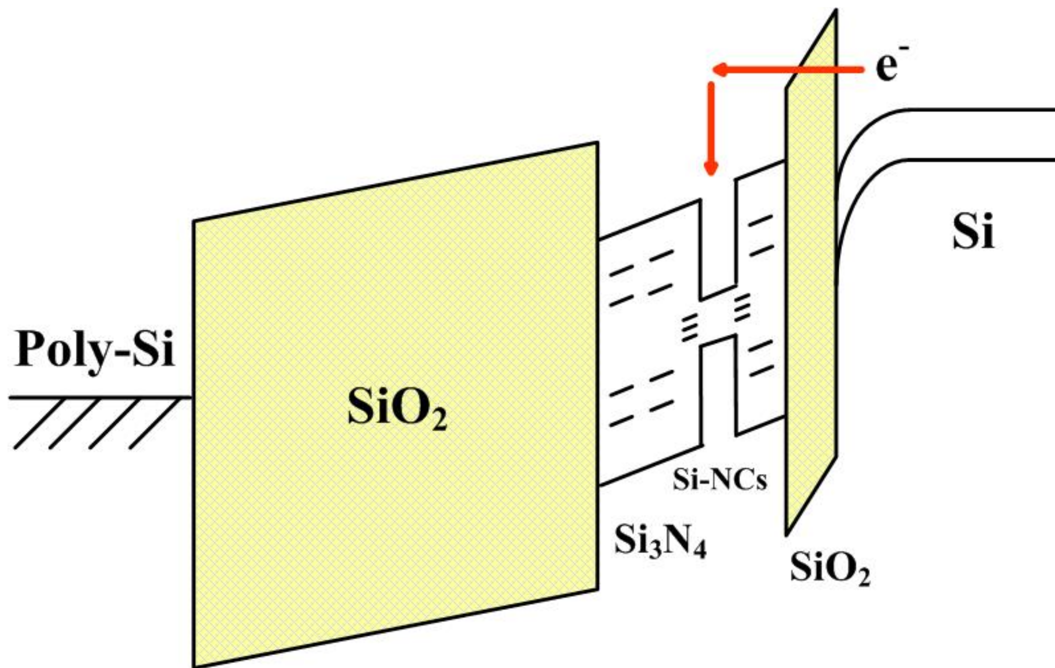



**Fig. 2-5** Positive gate voltage applied when use Fowler-Nordheim tunneling to program. Energy band representation of Fowler-Nordheim tunneling. Electron in Si conduction band tunnel through the triangular energy barrier.

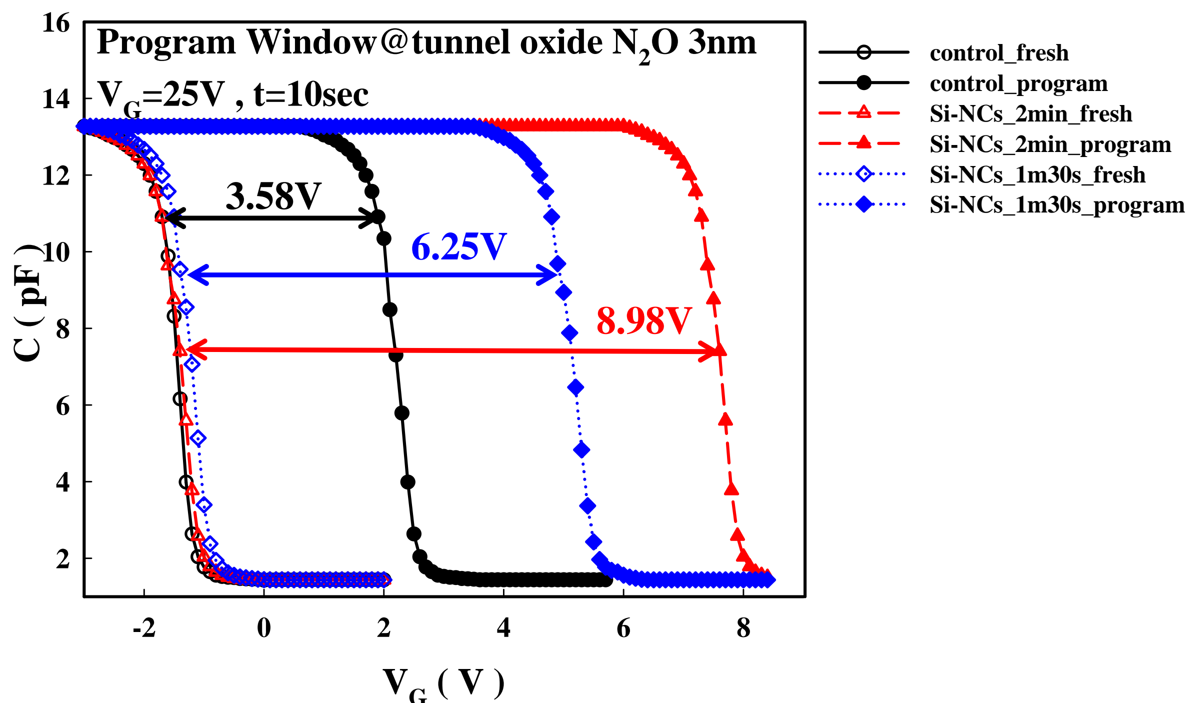
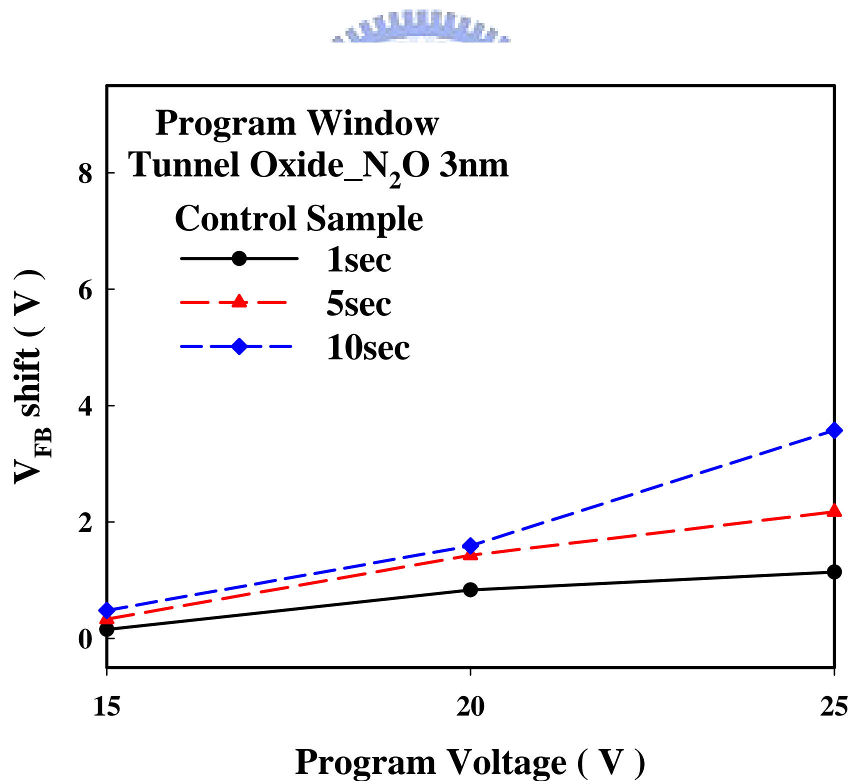


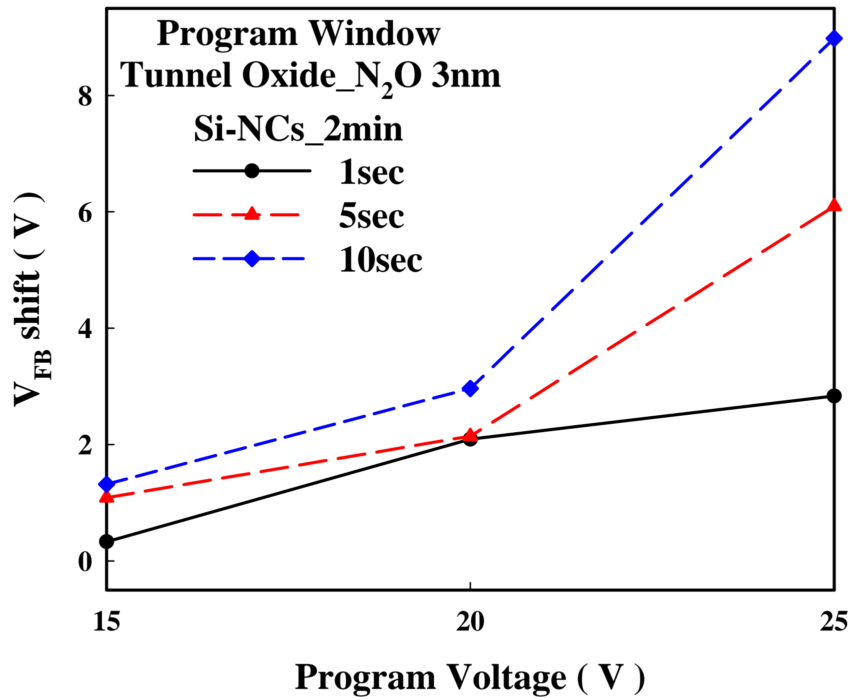

**Fig. 2-6** Program window characteristic of different sample. The program window of control, Si-NCs_1m30s and Si-NCs_2min sample are about 3.58V, 6.25V and 8.98V, respectively.

**Table 2-2** Summary for program window of different sample when program voltage $V_G$=25-V and program time 10-sec. The program window of Si-NCs is larger for control sample. And the larger Si-NCs size has more trapping sites for large memory window.

| sample | Control | Si-NCs_1m30s | Si-NCs_2min |
|---|---|---|---|
| **Program Window ( V )** | **3.58** | **6.25** | **8.98** |




(a)

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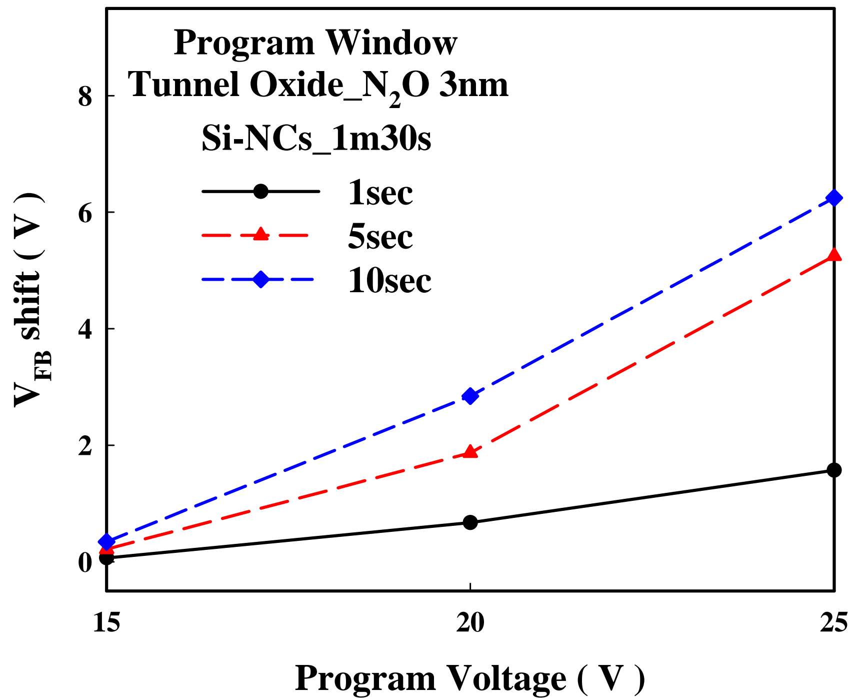
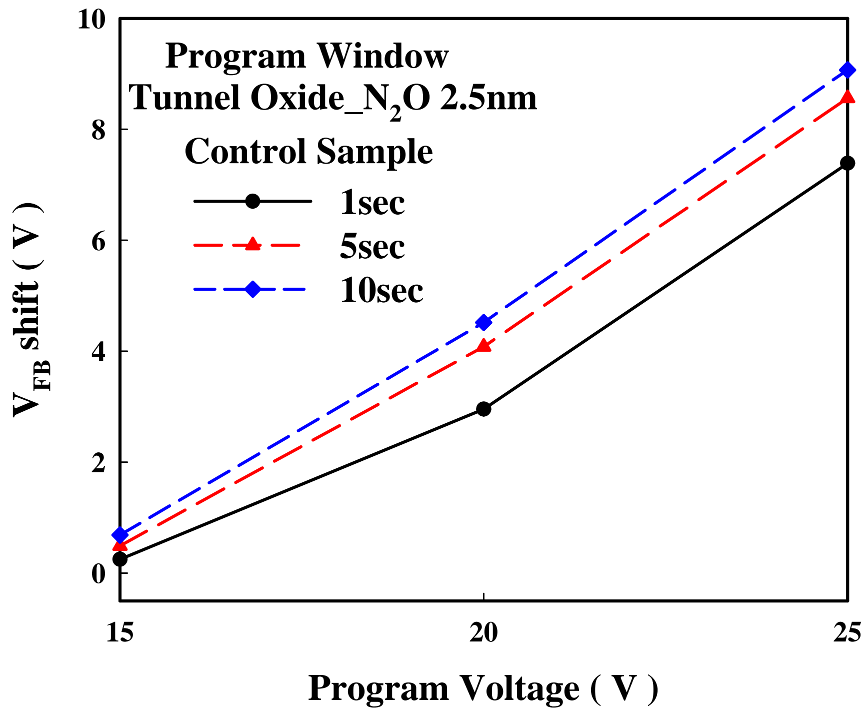
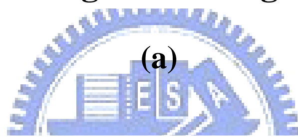


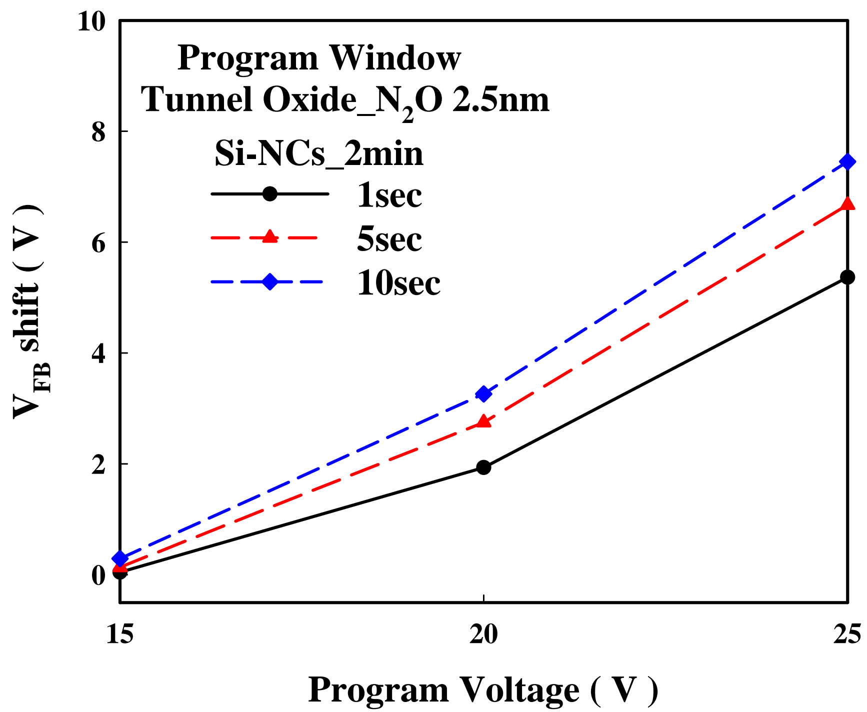

(c)

**Fig. 2-7** Program window characteristic of different sample when program voltage 15, 20 and 25V stress 1sec, 5sec and 10sec, respectively. (a) control sample, (b) Si-NCs_2min sample and (c) Si-NCs_1m30s sample. The tunnel oxide is dry $N_2O$ 3nm by horizontal-furnace.

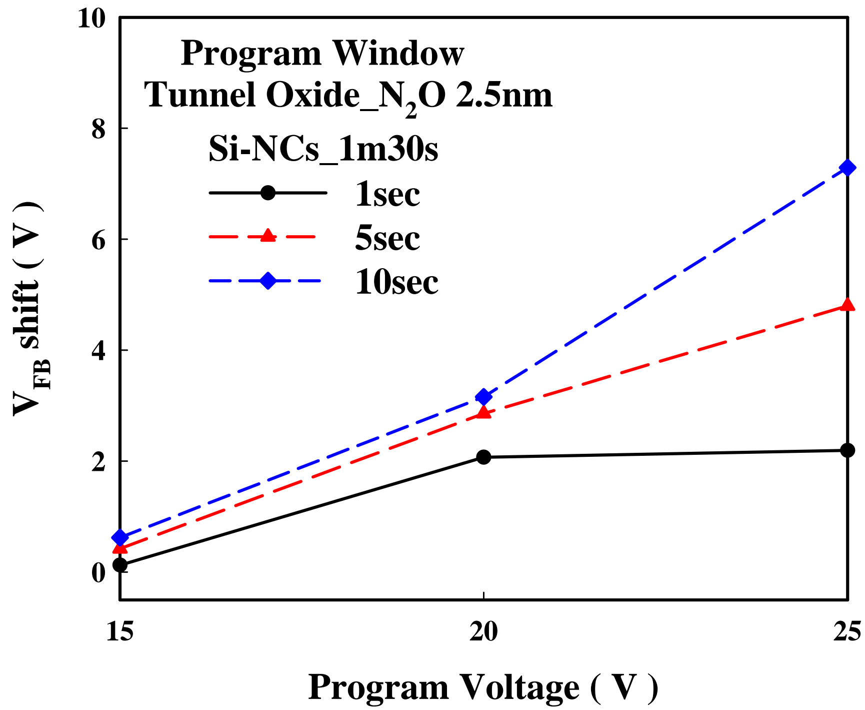



(a)



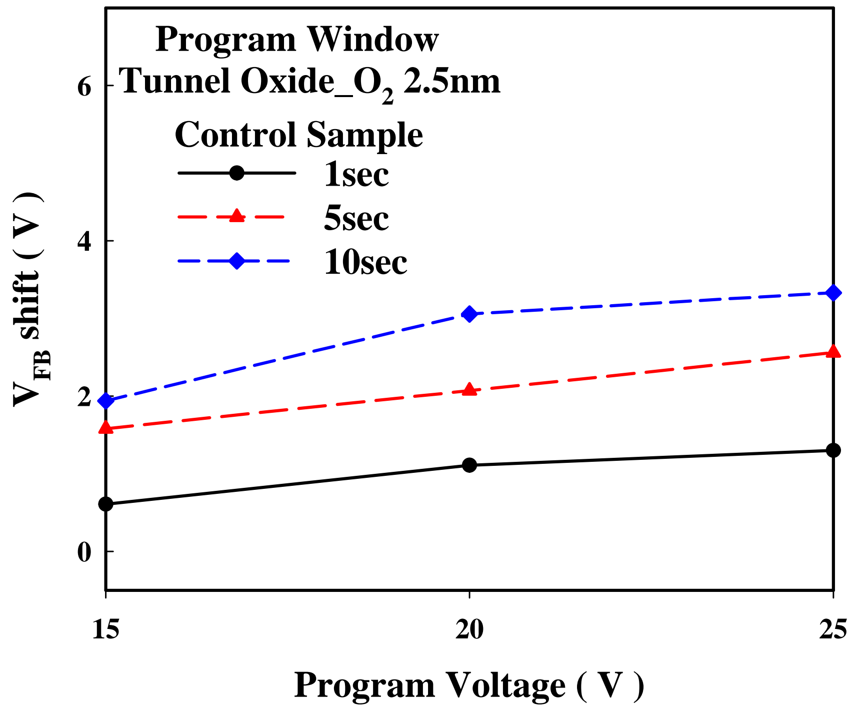



(b)

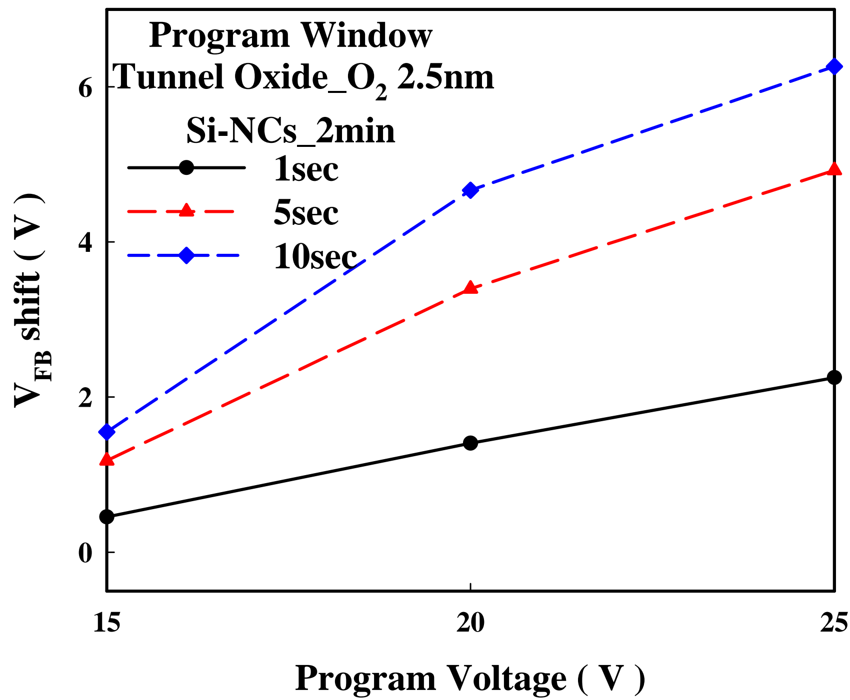



(c)

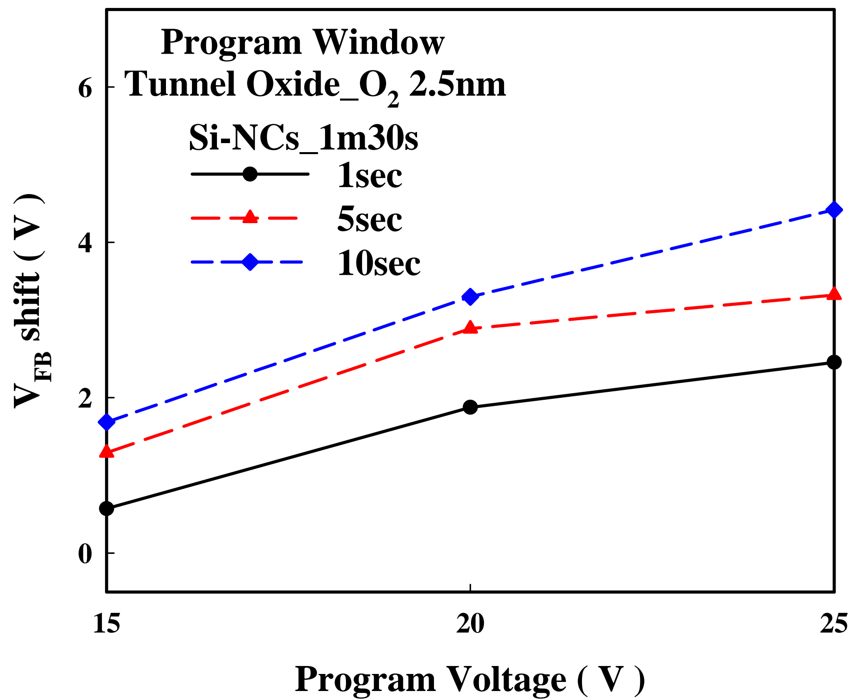
**Fig. 2-8** Program window characteristic of different sample when program voltage 15, 20 and 25V stress 1sec, 5sec and 10sec, respectively. (a) control sample, (b) Si-NCs_2min sample and (c) Si-NCs_11m30s sample. The tunnel oxide is dry $N_2O$ 2.5nm by vertical-furnace.




(a)




(b)




(c)

**Fig. 2-9** Program window characteristic of different sample when program voltage 15, 20 and 25V stress 1sec, 5sec and 10sec, respectively. (a) control sample, (b) Si-NCs_2min sample and (c) Si-NCs_1m30s sample. The tunnel oxide is dry $O_2$ 2.5nm by vertical-furnace.

**Table 2-3** Summary for program window of different sample when program voltage 15, 20 and 25V and stress 1sec, 5sec and 10sec, respectively. The program window of Si-NCs is larger for control sample. The tunnel oxide is dry $N_2O$ 3nm by horizontal-furnace.

| Program Window_$N_2O$ 3nm | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | $V_G$ = 15V | | | $V_G$ = 20V | | | $V_G$ = 25V | | |
| | t=1sec | t=5sec | t=10sec | t=1sec | t=5sec | t=10sec | t=1sec | t=5sec | t=10sec |
| control | 0.15 | 0.33 | 0.48 | 0.84 | 1.43 | 1.59 | 1.14 | 2.18 | 3.58 |
| Si-NCs_1m30s | 0.07 | 0.21 | 0.34 | 0.67 | 1.87 | 2.84 | 1.57 | 5.25 | 6.25 |
| Si-NCs_2min | 0.33 | 1.09 | 1.32 | 2.09 | 2.14 | 2.96 | 2.83 | 6.1 | 8.98 |

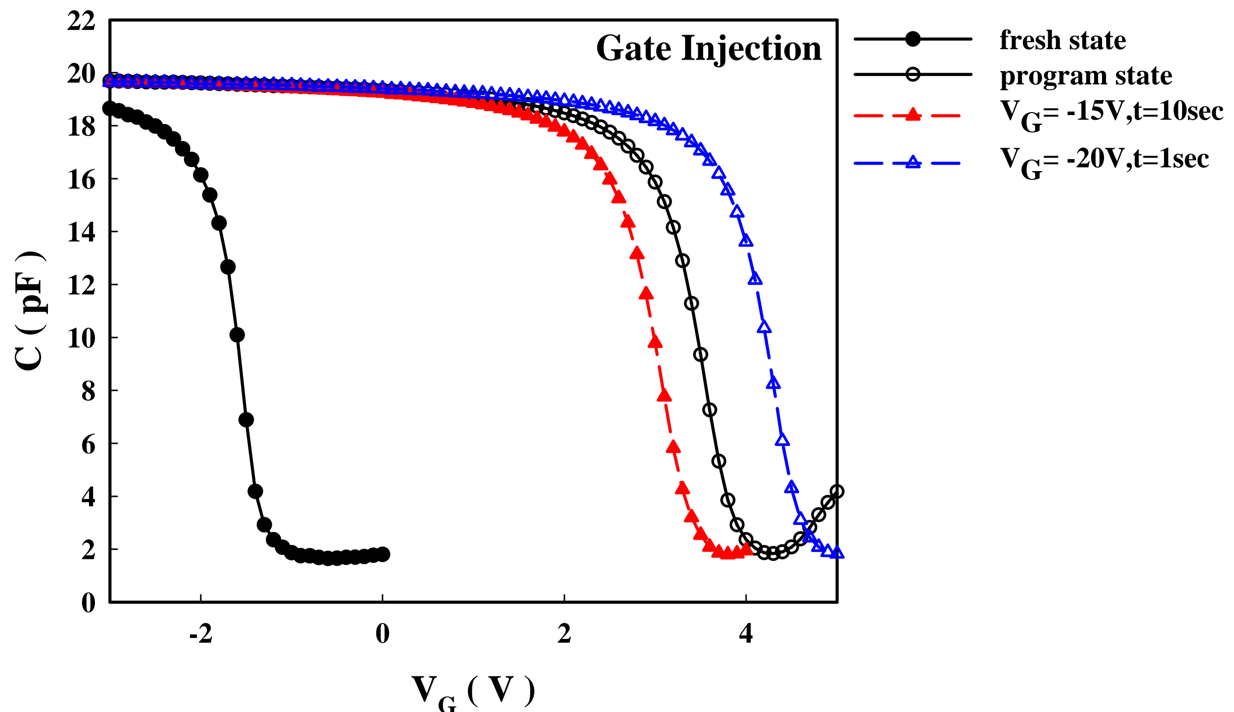



**Fig. 2-10** Erase characteristic of different negative gate bias. The gate bias $V_G$=-15V, t=10sec,can be erased △$V_{FB}$ shift about -0.5V. Because gate injection effect, when the gate bias $V_G$=-20V, t=1sec, be programmed △$V_{FB}$ shift about 0.8V.

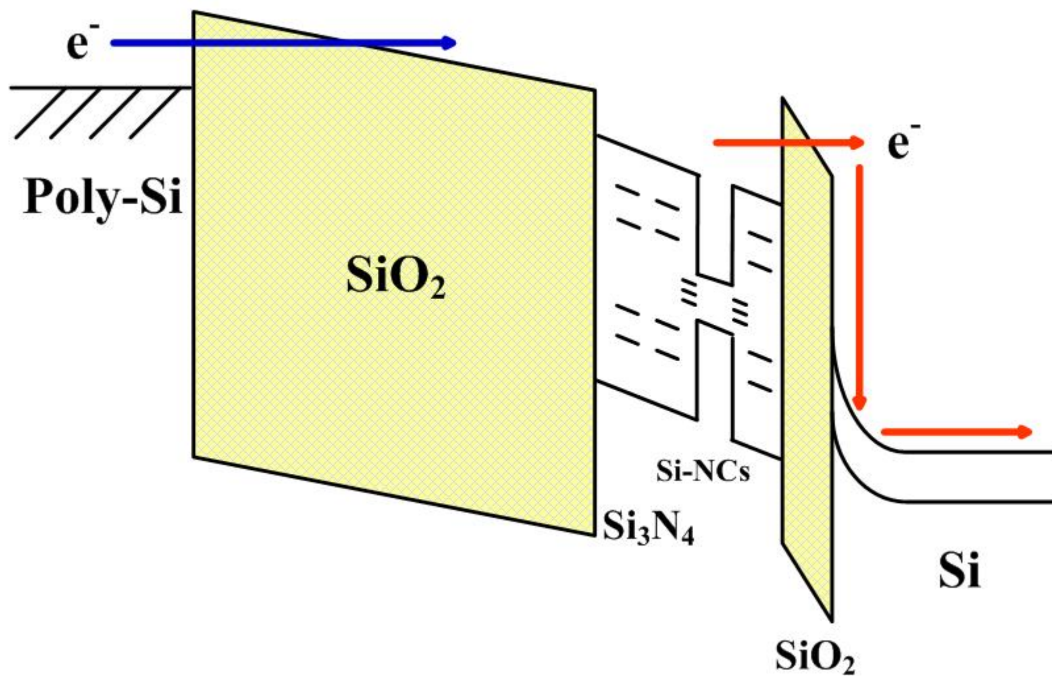
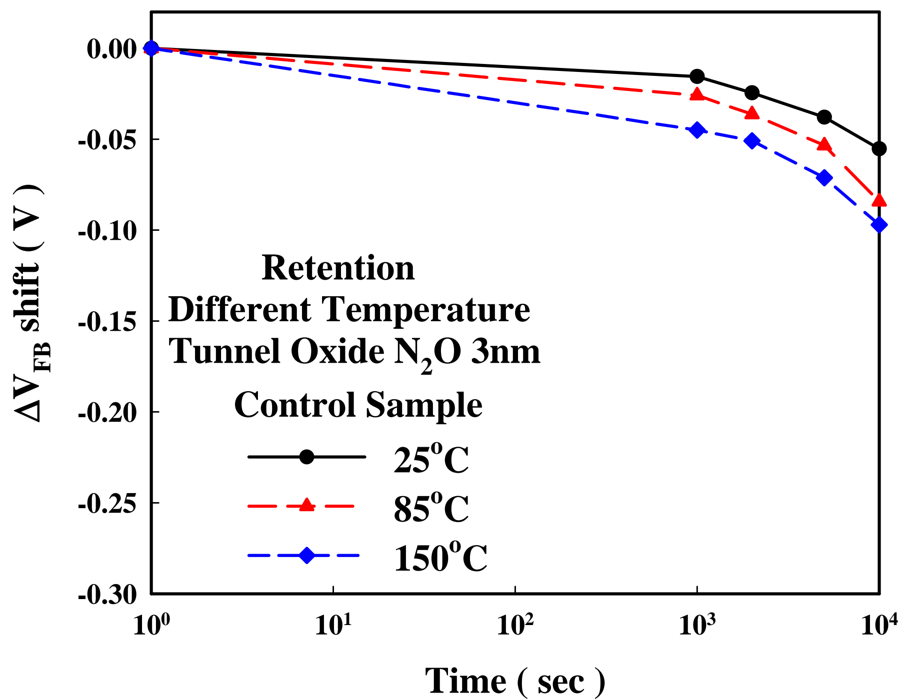
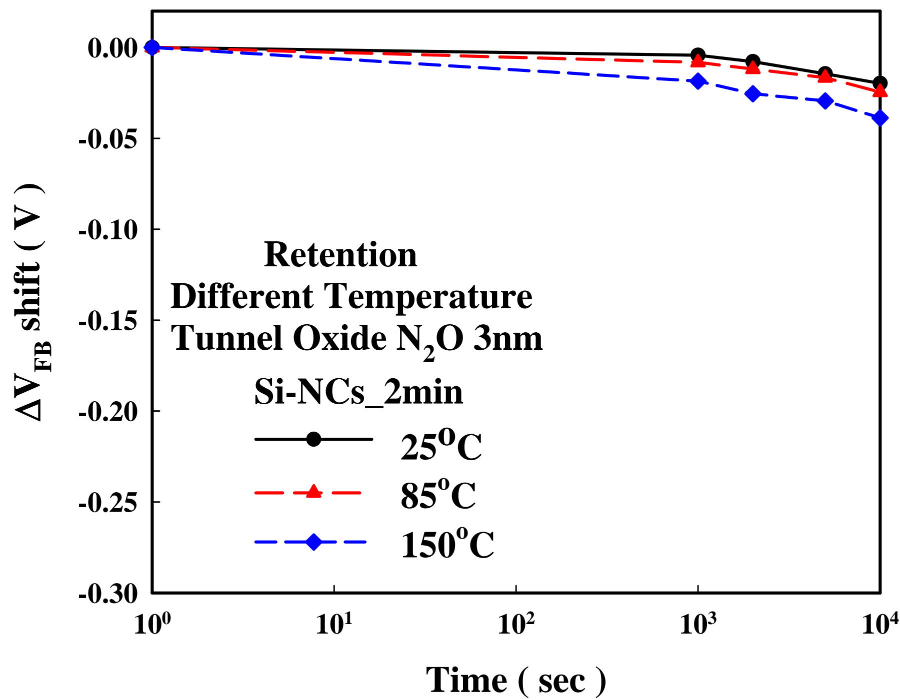


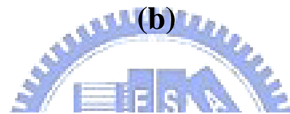

**Fig. 2-11** Negative gate voltage applied when use Fowler-Nordheim tunneling to erase. Energy band representation of Fowler-Nordheim tunneling. Electron in Si-NCs trapping layer and poly-Si gate are tunnel through the energy barrier.

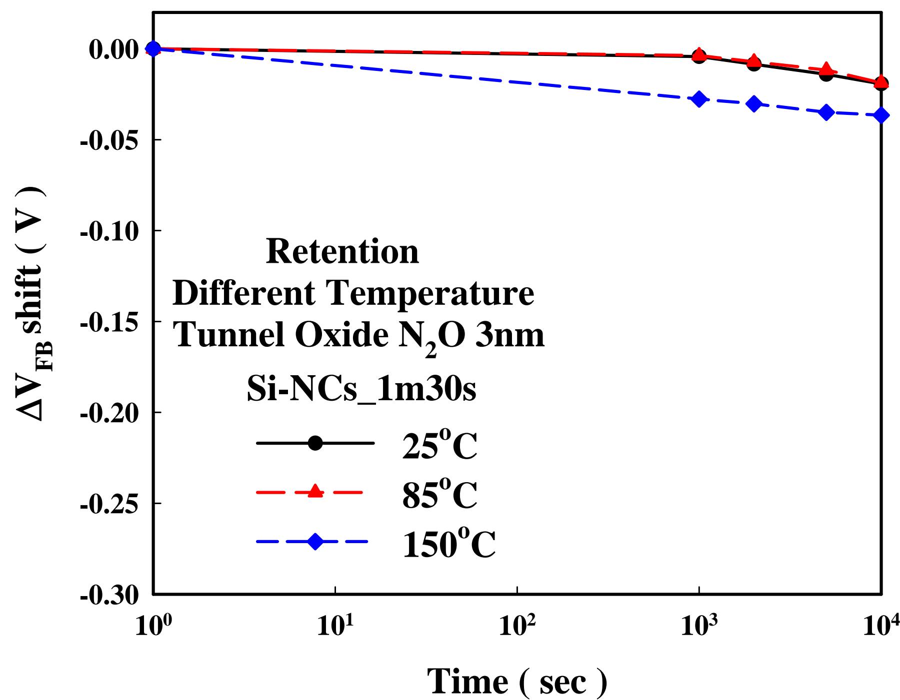



(a)



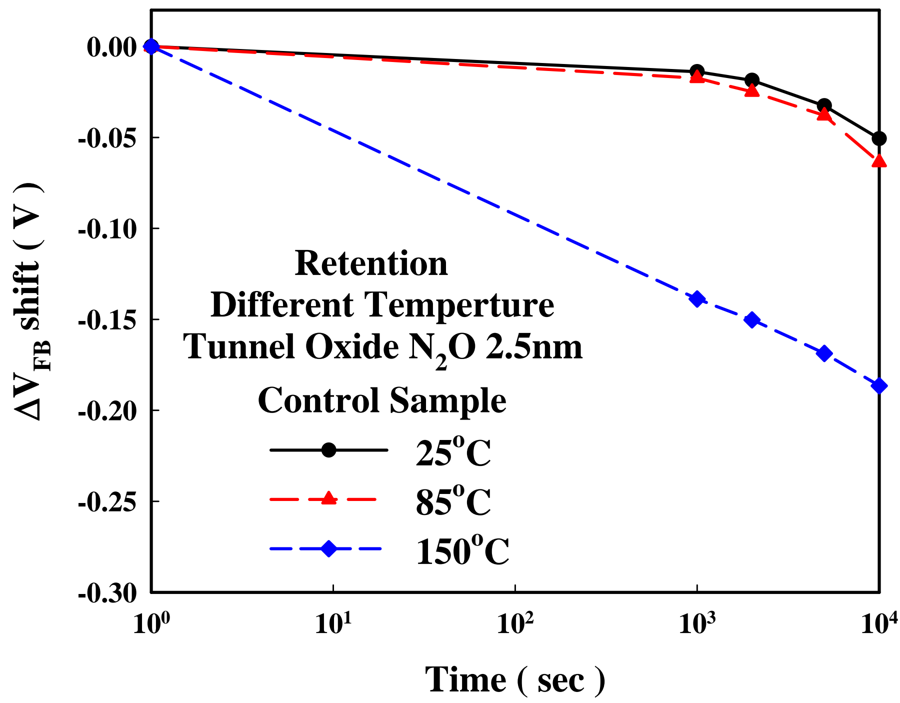

(b)

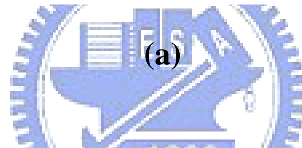




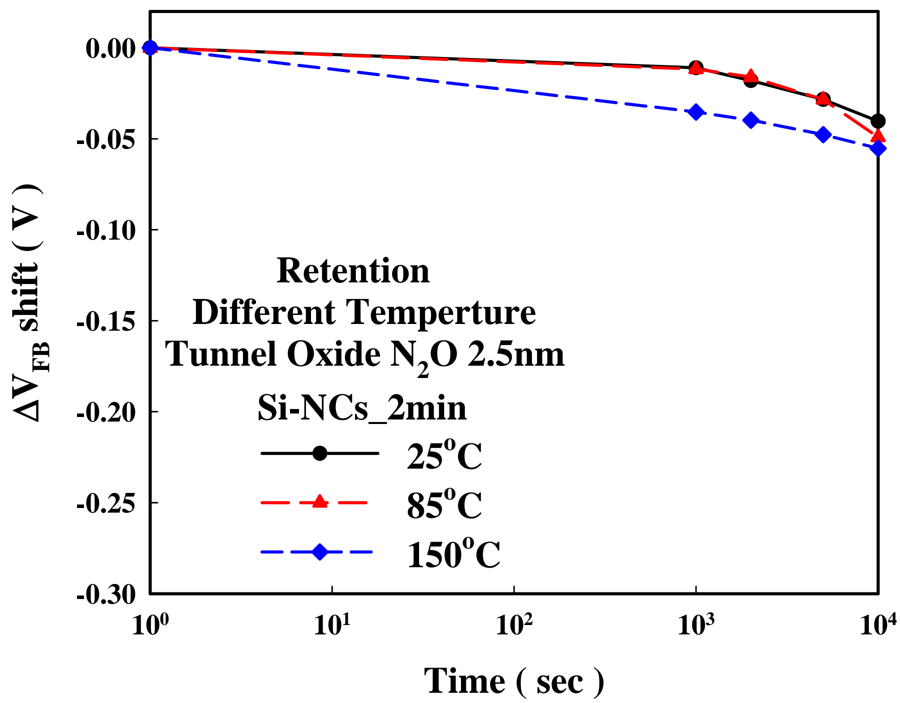

(c)

**Fig. 2-12** Data retention characteristic of different temperature for $\triangle V_{FB}$=2V. The tunnel oxide is dry $N_2O$ 3nm by horizontal-furnace. (a) control sample, (b) Si-NCs_2min sample and (c) Si-NCs_1m30s sample.

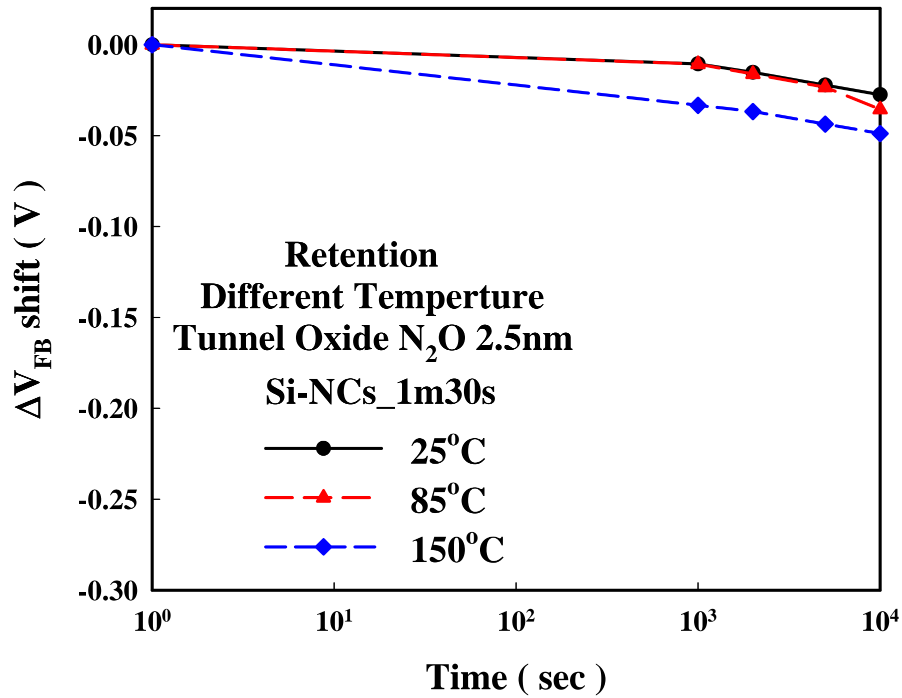


(a)

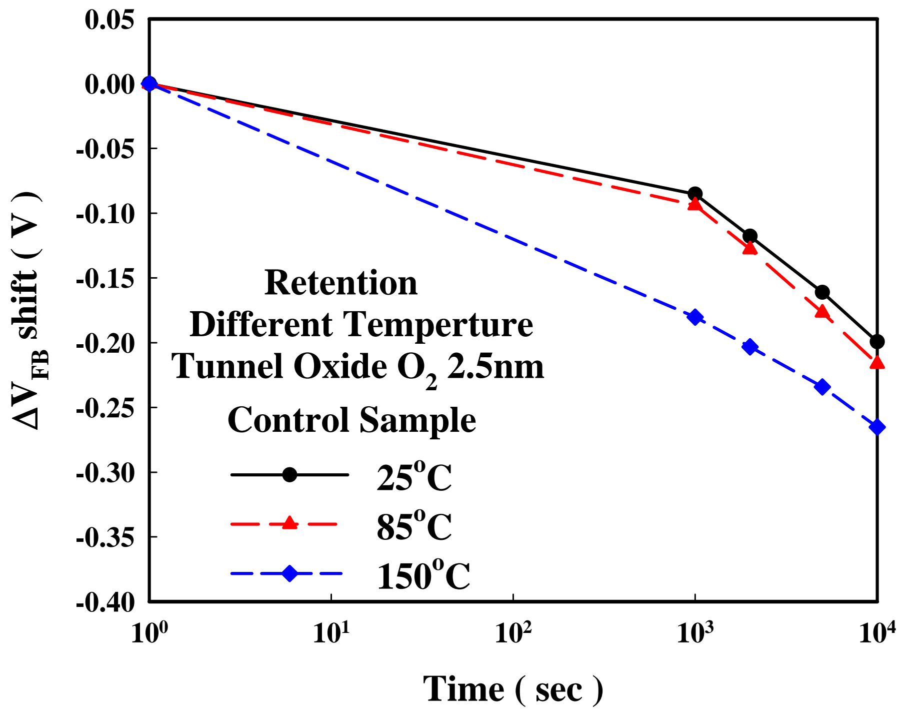



(b)

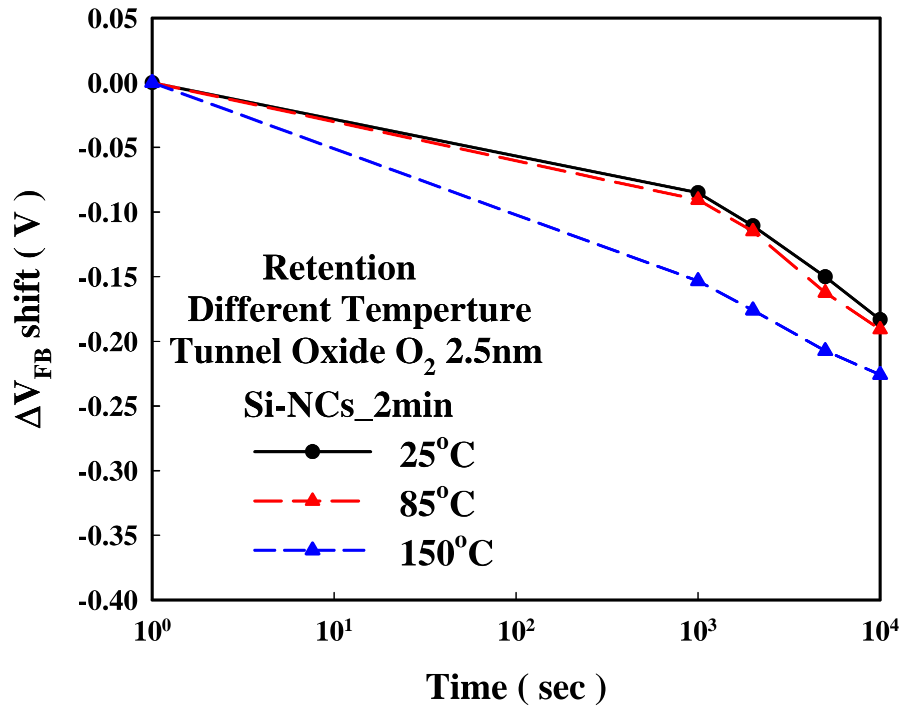



(c)

**Fig. 2-13** Data retention characteristic of different temperature for △$V_{FB}$=2V. The tunnel oxide is dry $N_2O$ 2.5nm by vertical-furnace. (a) control sample, (b) Si-NCs_2min sample and (c) Si-NCs_1m30s sample.




(a)

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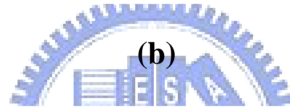
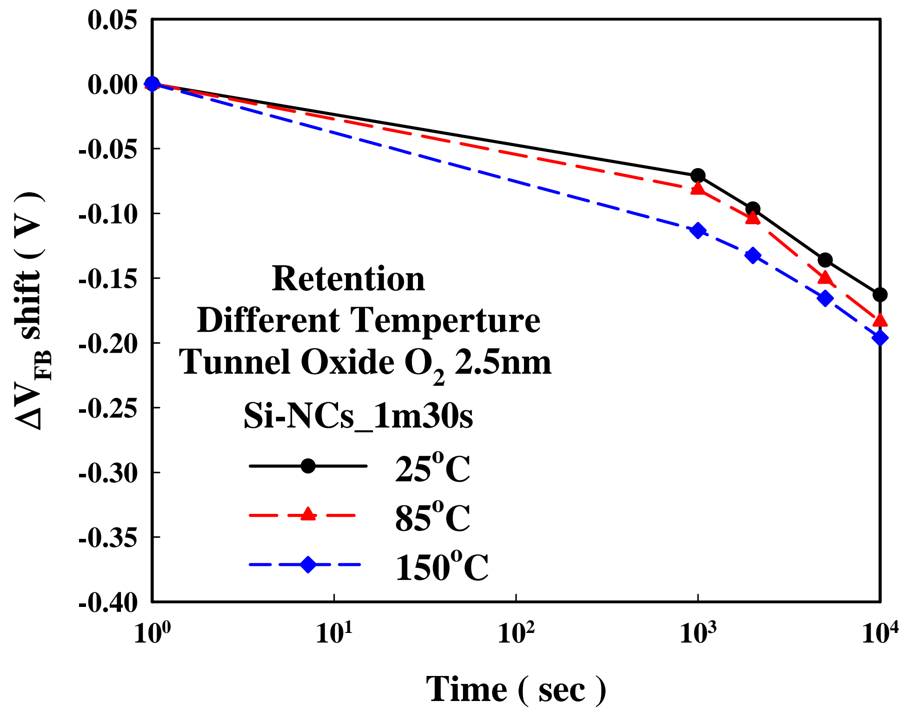
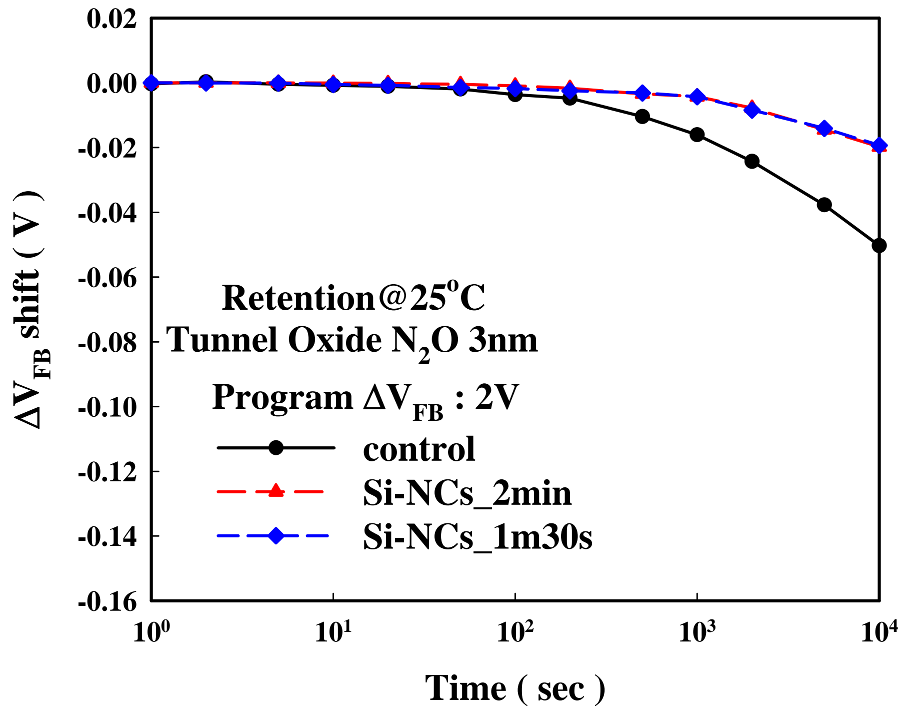
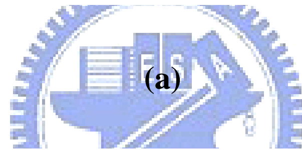




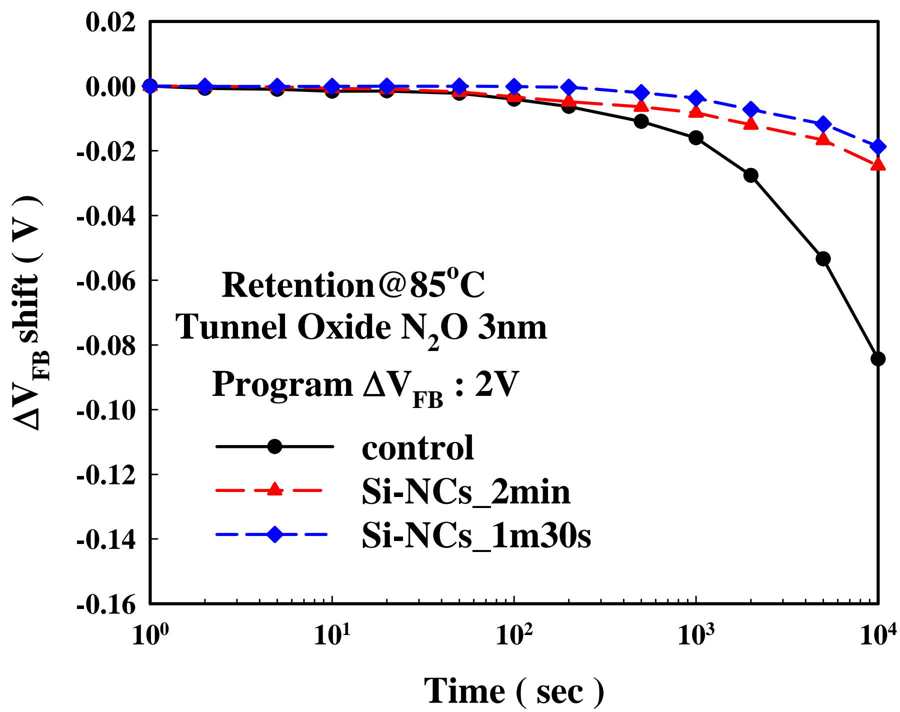

(c)

**Fig. 2-14** Data retention characteristic of different temperature for $\triangle V_{FB}$=2V. The tunnel oxide is dry $O_2$ 2.5nm by vertical-furnace. (a) control sample, (b) Si-NCs_2min sample and (c) Si-NCs_1m30s sample.



(a)

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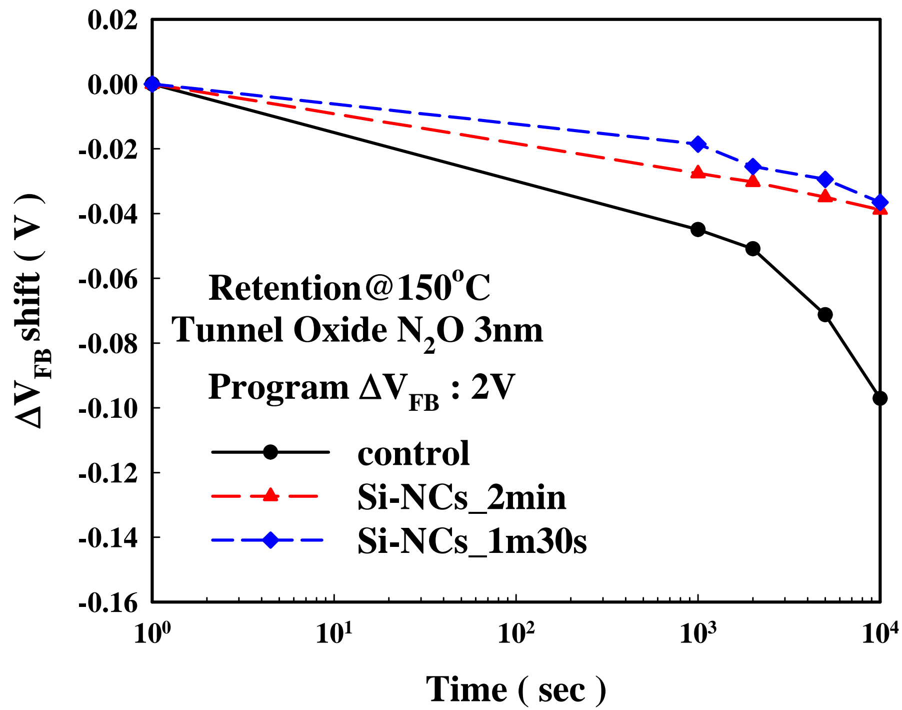
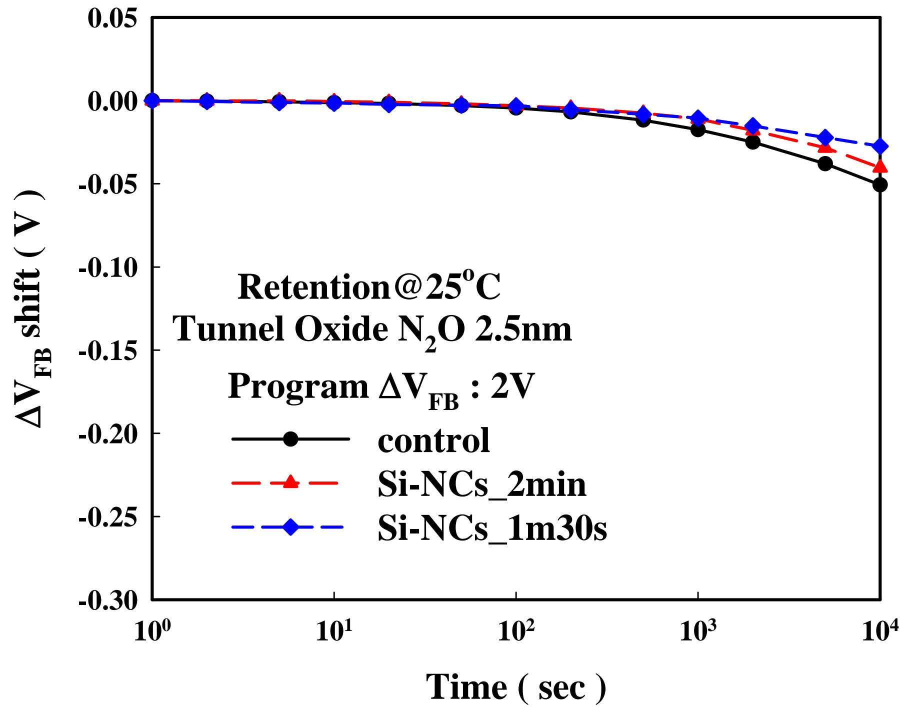
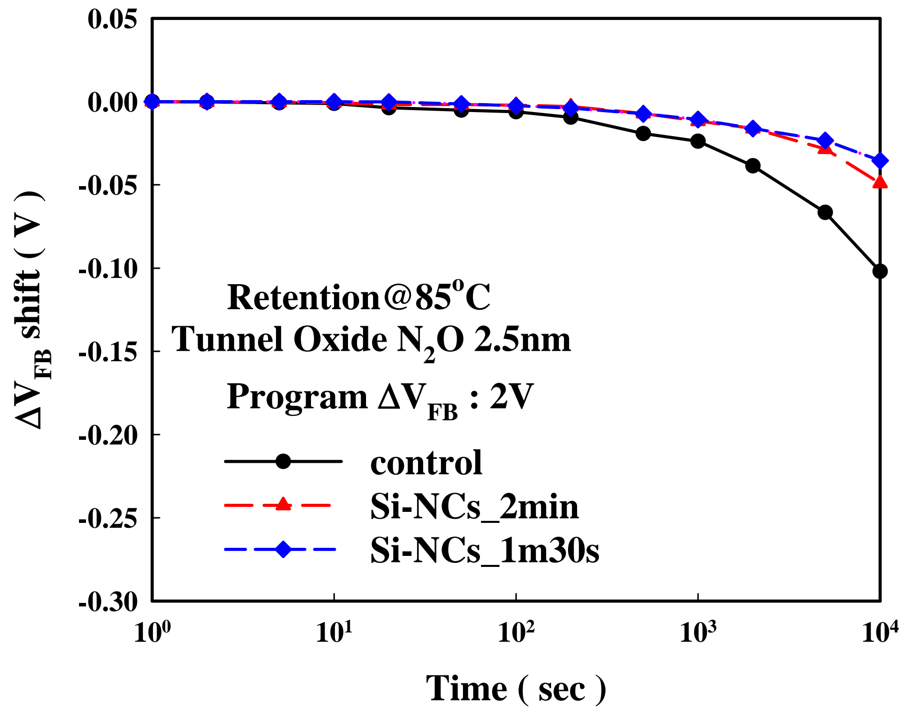


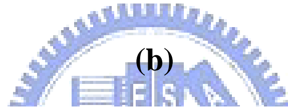

(c)

**Fig. 2-15** Data retention characteristic of different sample for △$V_{FB}$=2V. The tunnel oxide is dry $N_2O$ 3nm by horizontal-furnace. (a) At 25℃, (b) At 85℃ and (c) At 150℃.

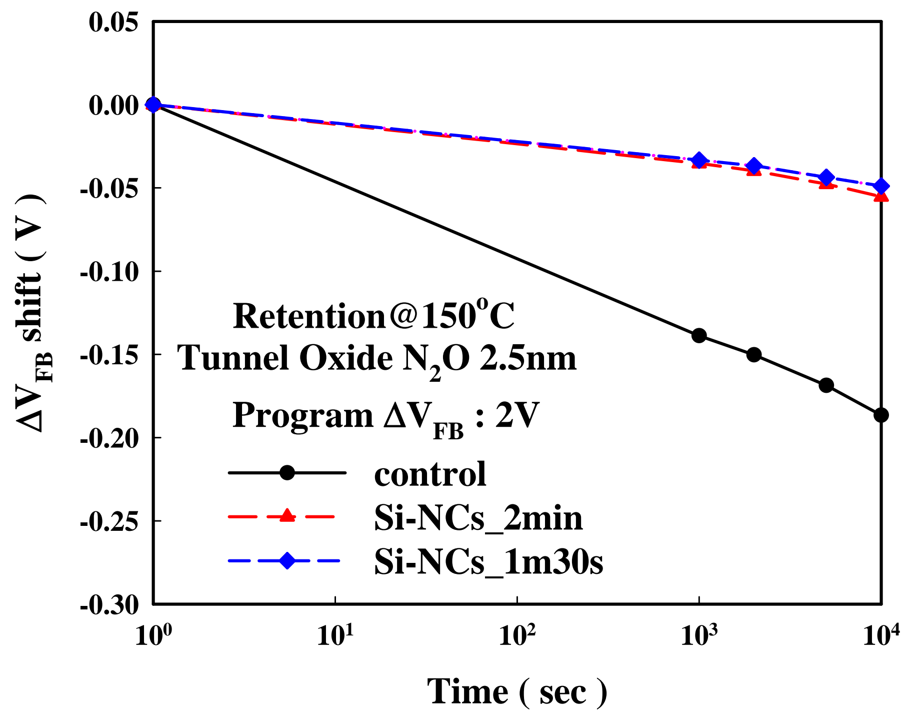



(a)



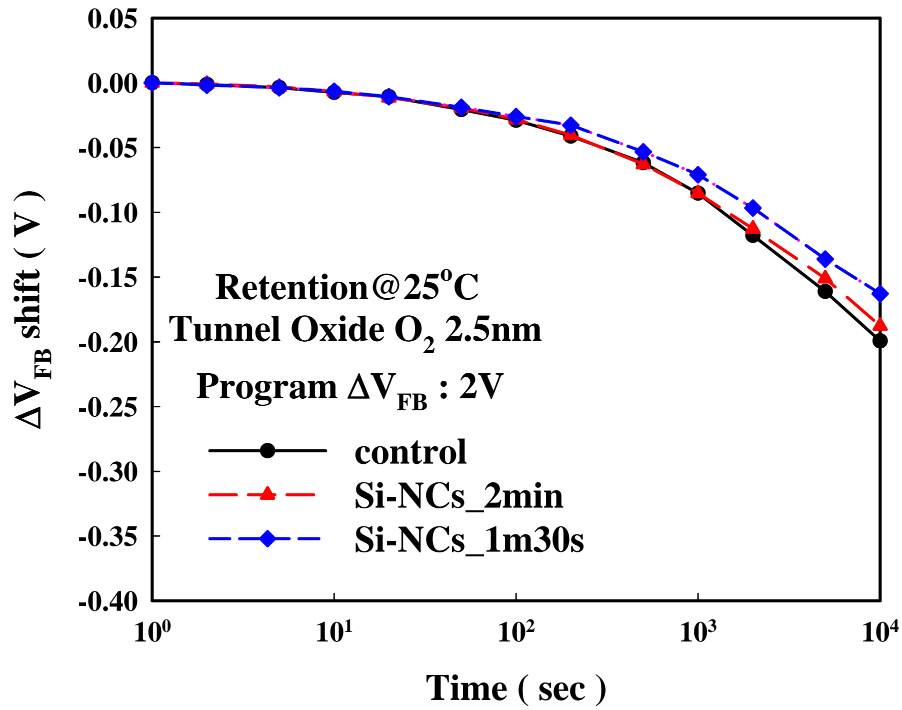



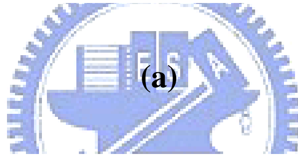
(b)



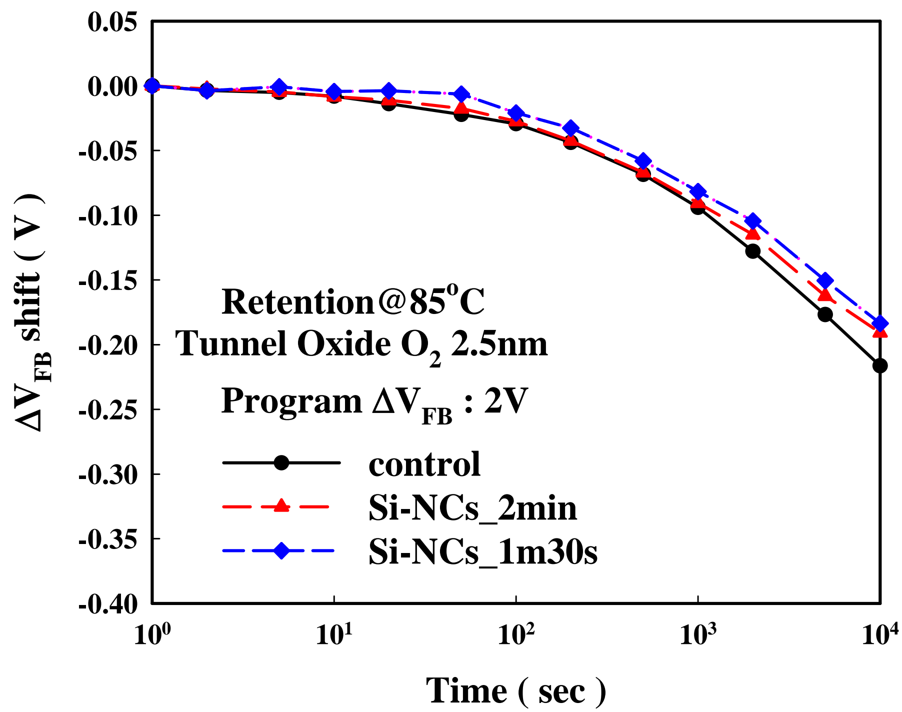

(c)

**Fig. 2-16** Data retention characteristic of different sample for $\triangle V_{FB}$=2V. The tunnel oxide is dry $N_2O$ 2.5nm by vertical-furnace. (a) At 25℃, (b) At 85℃ and (c) At 150℃.



(a)

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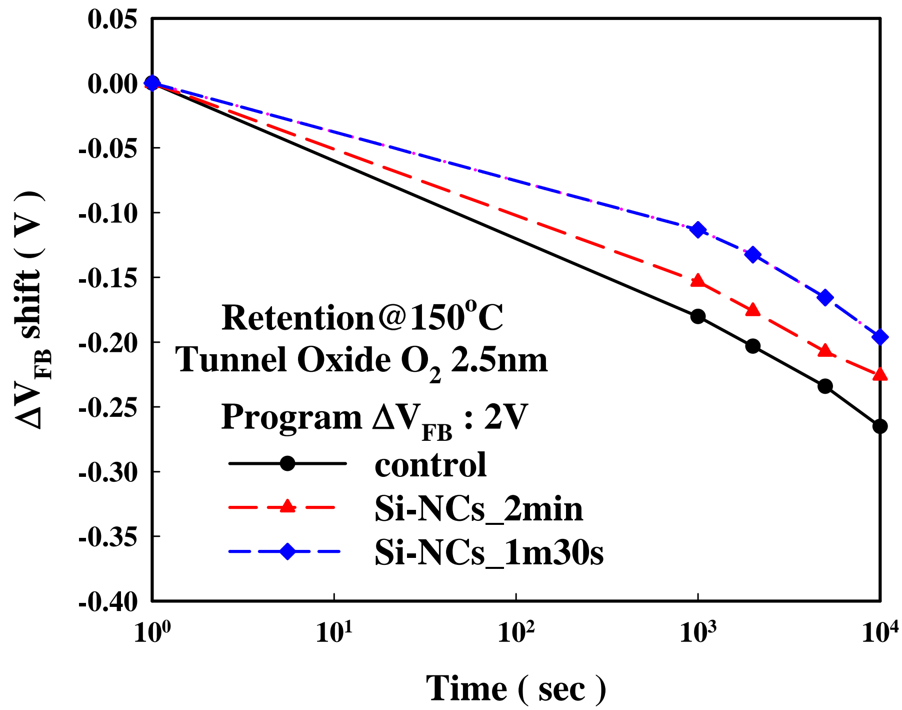
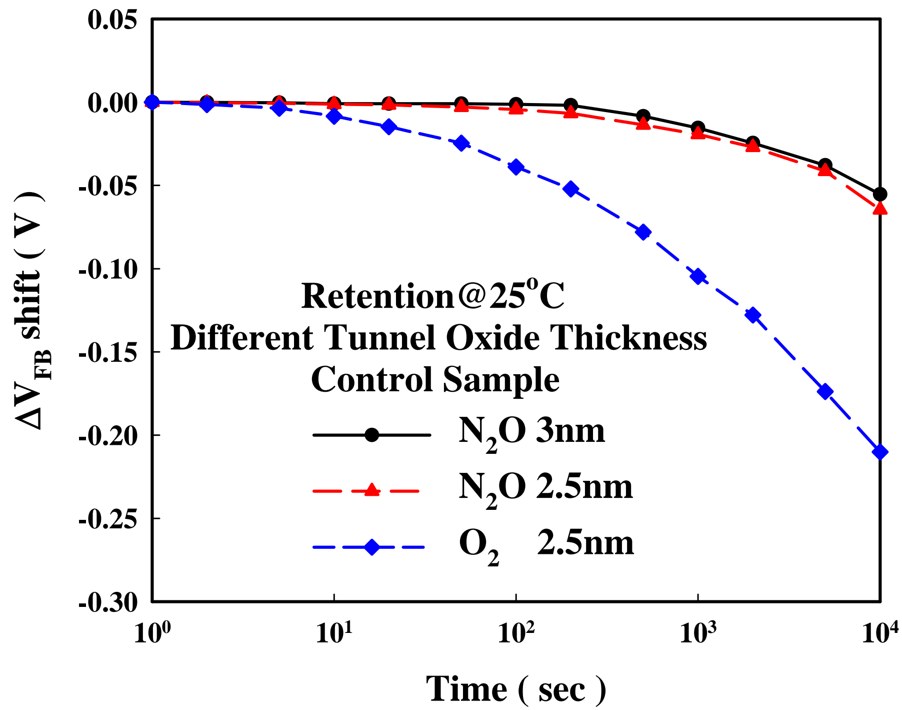
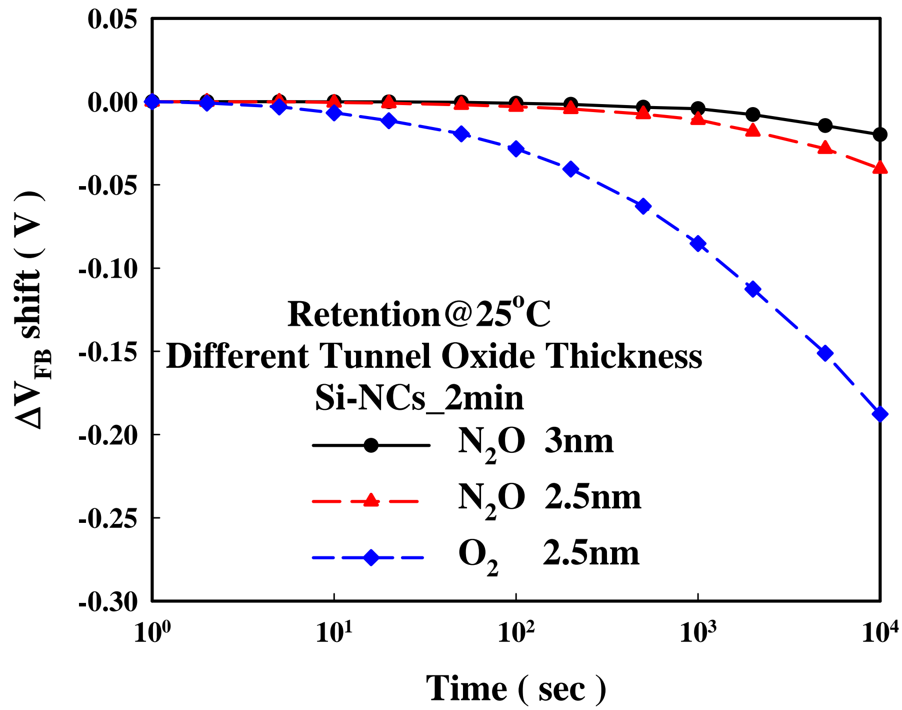



(c)

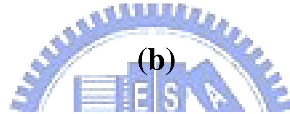
**Fig. 2-17** Data retention characteristic of different sample for $\triangle V_{FB}$=2V. The tunnel oxide is dry $O_2$ 2.5nm by vertical-furnace. (a) At 25℃, (b) At 85℃ and (c) At 150℃.

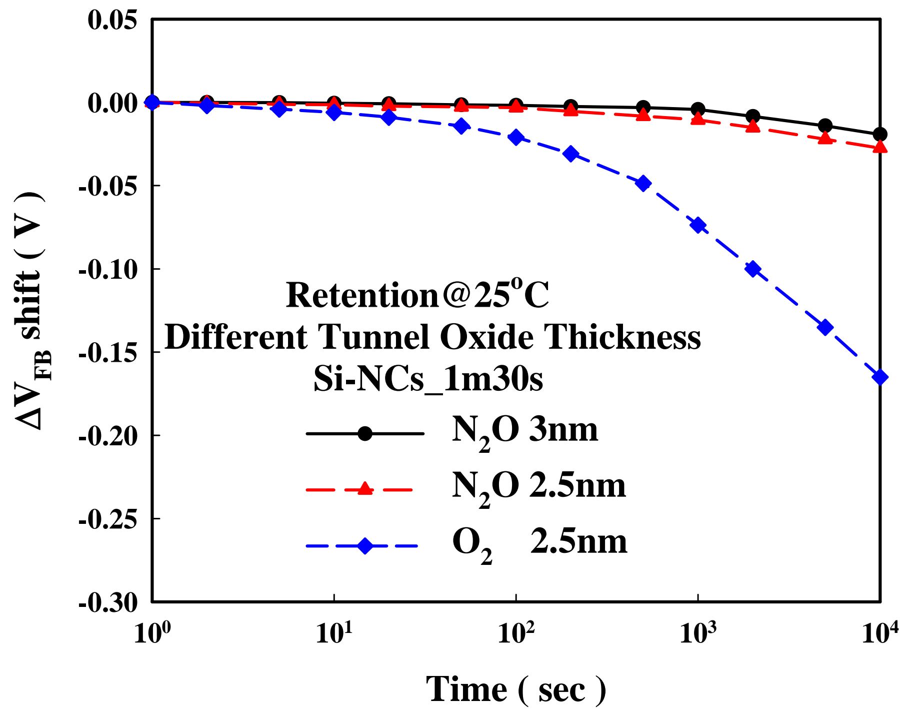



(a)



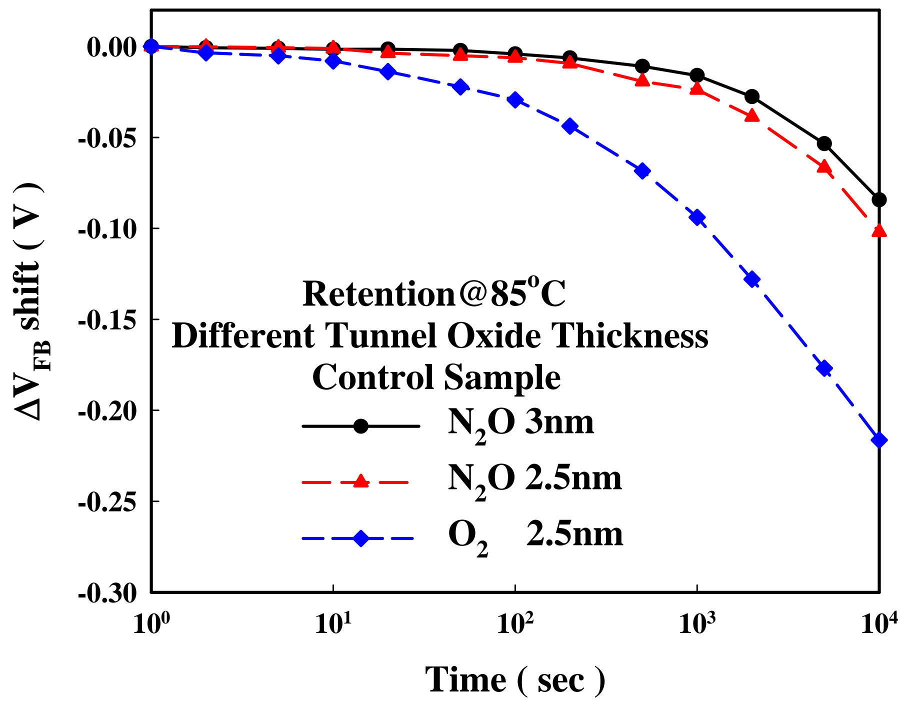

(b)

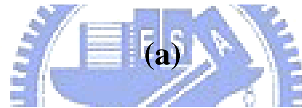




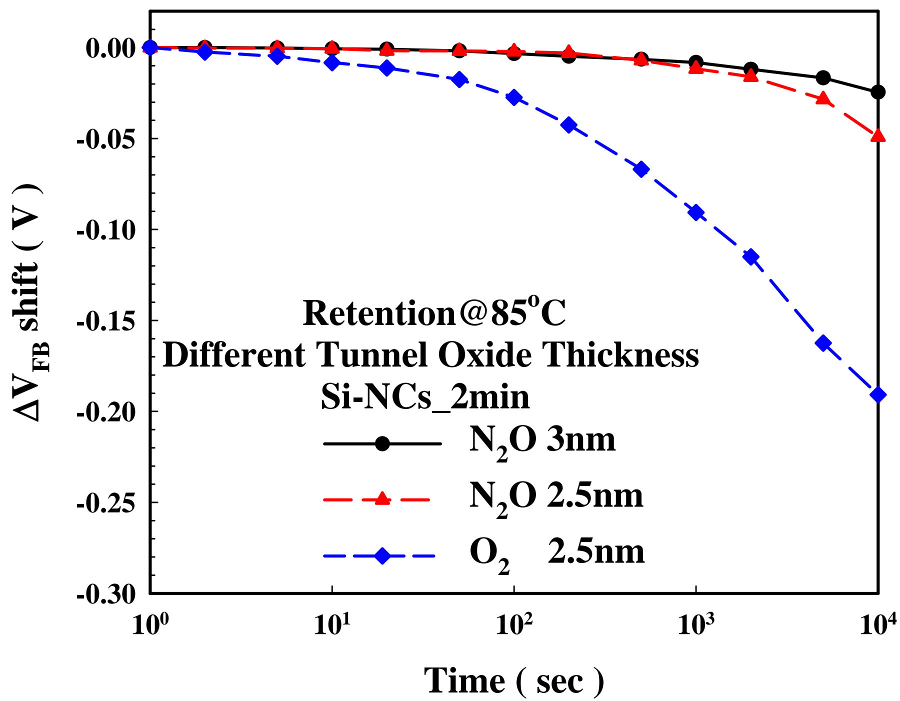

(c)

**Fig. 2-18** Data retention characteristic of different tunnel oxide film for $\triangle V_{FB}$=2V at T=25℃. (a) control sample, (b) Si-NCs_2min sample and (c) Si-NCs_1m30s sample.

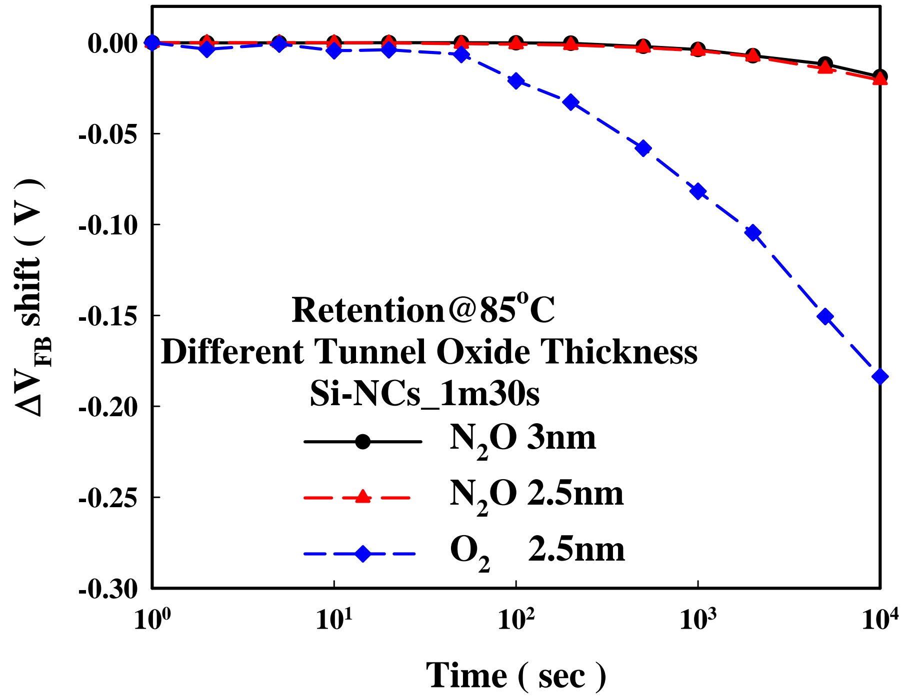


(a)

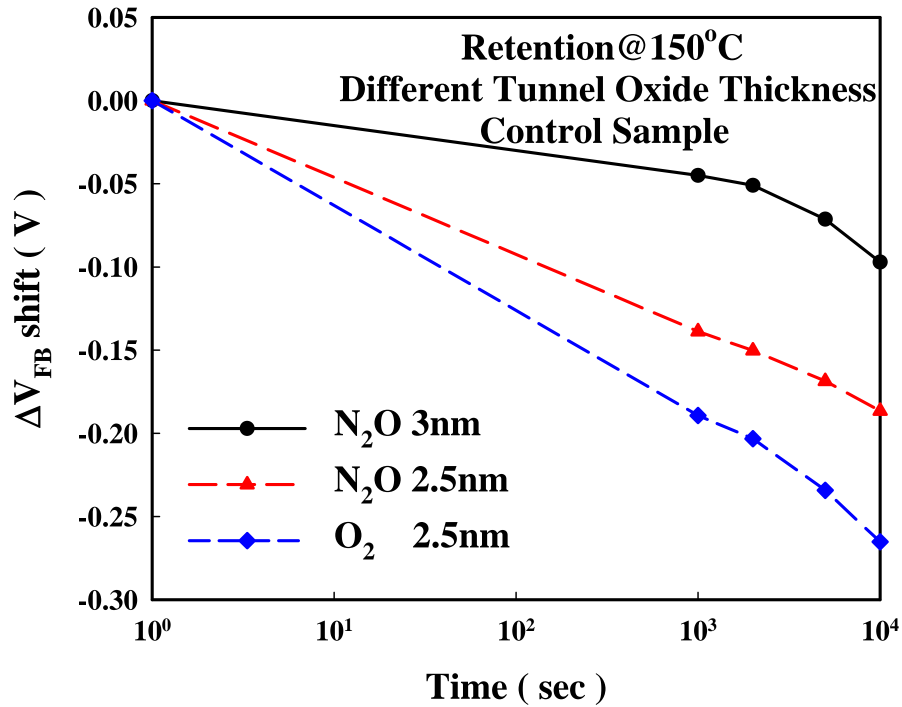



(b)

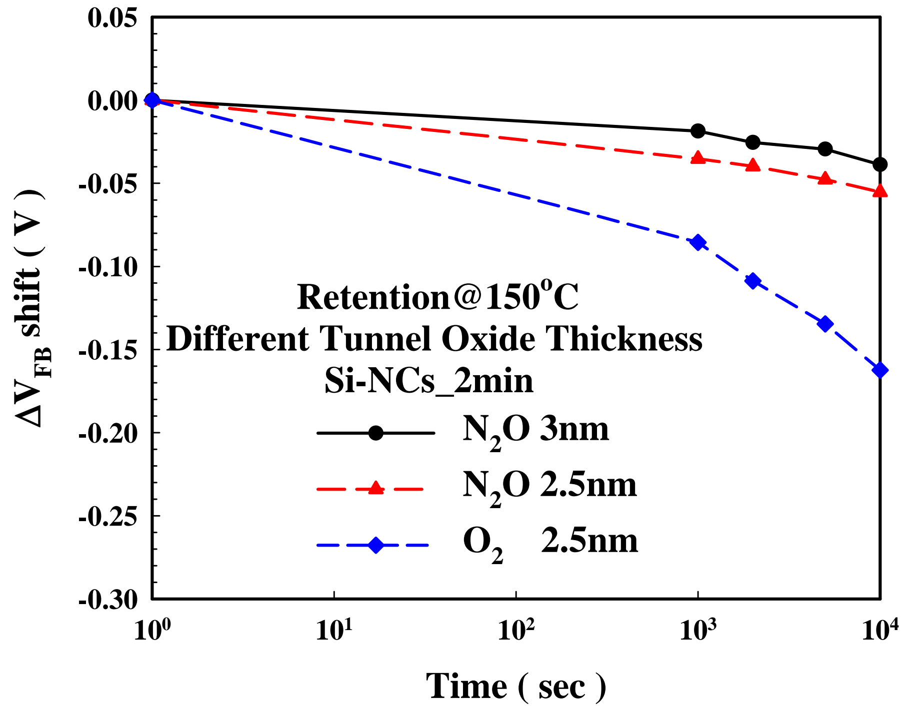



(c)

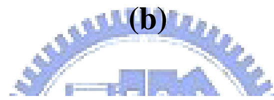
**Fig. 2-19** Data retention characteristic of different tunnel oxide film for $\triangle V_{FB}$=2V at T=85℃. (a) control sample, (b) Si-NCs_2min sample and (c) Si-NCs_1m30s sample.

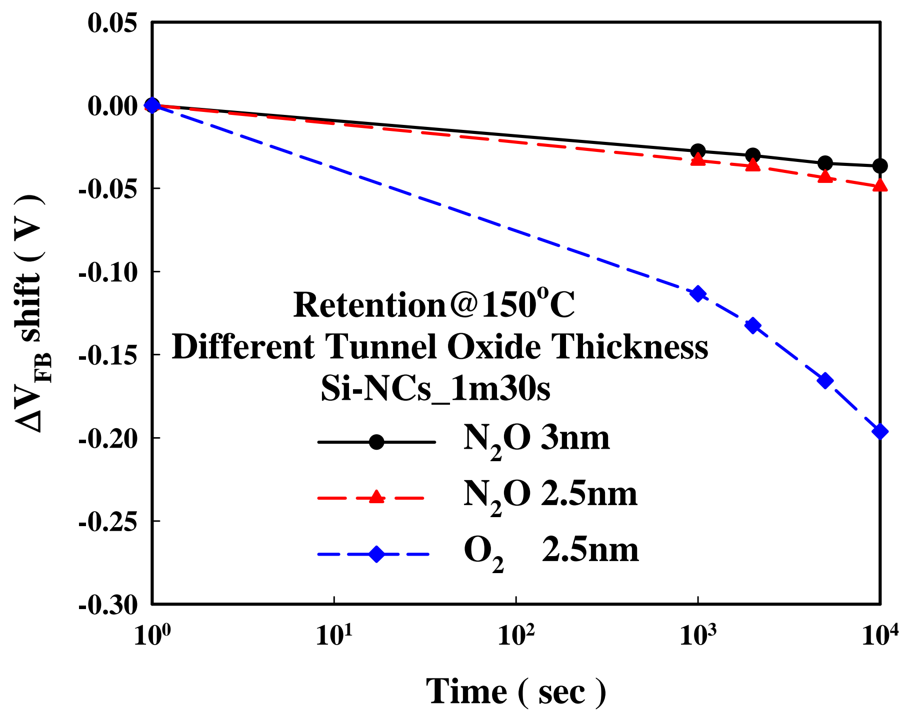



(a)




(b)






(c)

**Fig. 2-20** Data retention characteristic of different tunnel oxide film for $\triangle V_{FB}$=2V at T=150℃. (a) control sample, (b) Si-NCs_2min sample and (c) Si-NCs_1m30s sample.

# *Chapter 3*

# *Experiment Procedures*

# *and Electric Characteristic of Device*

## 3.1 Device Fabrication

The schematic diagram of the fabrication process is illustrated in Fig.3-1.Three different types of tunnel oxide are grown on p-type (100) silicon substrates after RCA cleaning. (1) 3-nm thick $SiO_2$ film was thermally grown in dry $N_2O$ atmosphere by horizontal-furnace. (2) 2.5-nm thick $SiO_2$ film was thermally grown in dry $N_2O$ atmosphere by vertical-furnace. (3) 2.5-nm thick $SiO_2$ film was thermally grown in dry $O_2$ atmosphere by vertical-furnace. Then, a 3-nm thick silicon nitride films was deposited as the trapping layer in a LPCVD system using $SiH_2Cl_2$ and $NH_3$ as source for 30 and 130 sccm, respectively. Si-NCs were formed on the silicon nitride films immediately by LPCVD for 2-min and 1-min and 30-sec. The deposition of amorphous silicon nucleation were kept at 550°C and the pressure was controlled at 100-mTorr. The flow rate of the reaction gas of $SiH_4$ was 85-sccm. Then, the silicon nitride capped on the amorphous silicon nucleation was 4-nm. During this high temperature period, the previously deposited amorphous silicon nucleation was crystallized and then formed into poly-Si nanocrystals,, which were embedded in silicon nitride films. A blocking oxide about 20-nm was then deposited using high density plasma chemical vapor deposition (HDPCVD) oxide. A 200-nm thick poly-Si was deposited to serve as the gate electrode by LPCVD. Subsequently, the $n^+$ poly-Si gate was formed by ion implantation of phosphorous at 40-keV to a dose of $5x10^{15}$ $cm^{-2}$. The sample without Si-NCs was fabricated as a control sample.

Then, the poly-Si gate electrode and the Si-NCs trapping layer with blocking oxide were

etched by poly-Si dry etcher (TCP- 9400) and the oxide dry etcher (TEL-5000). The wafers were ion implanted by arsenic. The energy and the dose of implantation were 15-keV to dose $5\times10^{15}$ $cm^{-2}$ for source and drain.

Substrate etching and substrate implantation were executed continuously. Rapid thermal annealing (RTA) was formed at 1000°C for 5 seconds. The passivation layer was employed by TEOS at 600°C for 400-nm. After contact etching, four-level metallization (Ti / TiN / Al / TiN) were carried out in PVD system. The SONOS with Si-NCs memory was made.

## 3.2 Typical Threshold Voltage Parameter Extraction

In this section, the methodology of extracting typical parameters, such as threshold voltage from device characteristics, are briefly introduced. Plenty ways are used to determinate the threshold voltage which is the most important parameter of semiconductor devices. The method to determinate the threshold voltage in my thesis is the *constant drain current method* that the voltage at a specific drain current $I_{ON}$ is taken as the threshold voltage. This technique is easy and can give a threshold voltage close to that obtained by the complex linear extrapolation method. Typically, the threshold current $I_{ON} = I_{DN} / (W / L)$ where $I_{DN}$ is a normalized drain current. Here, $I_{DN}$ is 100 nA and the same for all devices to extract the threshold voltage of SONOS memory.

## 3.3 Characteristic of Program/Erase

In this section, we will discuss the program/erase injection mechanism. In this thesis, the programming scheme is executed by using Fowler-Nordheim tunneling and channel hot electron to injection charge into the Si-NCs trapping layer. On the other hand, the erasing scheme is executed by using Band-to-Band hot holes injection [38] to combine negative charge in the trapping layer. The injection components and efficiency for different gate or drain bias and program time conditions on different size Si-NCs trapping layer device will be

discussed.

### 3.3.1 Program Speed

The Fowler-Nordheim tunneling hot electrons injection was employed for programming mode. Fig. 3-2 shows the transfer characteristic of fresh state and program state for Si-NCs_1m30s sample. We clearly observed that memory window is quite large. Applying $V_G$=20-V, a memory window about 2-V can be easily achieved for Si-NCs_1m30s sample, when program time is 1sec.The leakage current of Si-NCs_1m30s sample is low about $10^{-12}$A.

Fig's. 3-3 (a)-(b) exhibits program speed characteristic for different samples, when we applying gate voltage bias at 20-V. We can see that the programming time when time reaching 0.1s if the windows margin is set about 1.5-V for two cases of control sample and Si-NCs_1m30s sample. The tunnel oxide of 3-nm was grown in dry $N_2O$ by horizontal-furnace. For the same gate voltage bias, that different tunnel oxide film is increased does obviously improve program speed. Summary for program window of different tunnel oxide film when $V_G$=20-V and stress 1-sec. The program window of Si-NCs_1m30s is larger for control sample in Table 3-1.

The channel hot electron injection was employed for programming mode. Fig's. 3-4 (a)-(c) exhibits program speed characteristic for different programming conditions. We changed drain voltage bias and gate voltage bias with 5-V, 6-V and 7-V to measure program speed. We can see that the programming time can be as short as 10-μs if the windows margin is set about 1-V with $V_G$=6-V, $V_D$=6-V. For all cases, we use three kind of drain voltage bias for strong and weak drain avalanche. It can be clearly seen that larger drain bias induced strong drain avalanche makes faster program speed. On the other hand, we use three kind of the gate bias for strong and weak vertical field to hot electrons for injected into the trapping layer so the influence of increased gate voltage is conspicuous. According to all of the above, we can clearly observe that channel hot electron injection can improve injection efficiency and get faster program speed.

### 3.3.2 Erase Speed

Fig's. 3-5 (a)-(c) shows erase speed characteristic for different erasing conditions. We changed gate voltage bias with -8-V, -9-V and -10V to measure erase speed for fixed 7-V drain voltage bias. We can see that erasing time can be as short as μs in order to combine negative charge in the trapping layer. The increased gate bias does not obviously accelerate erase speed. The erase speed of different gate bias is almost the same. Fig's. 3-6 (a)-(c) exhibits erase speed characteristic when we changed drain voltage bias with 6-V, 7-V and 8-V to measure erase speed for fixed -9-V gate voltage bias.

In conclusion, show summary for erase Vt shift of 1s erase time, and compared at fixed $V_G$=-9-V for all cases of different $V_D$. The gate bias supplies only a vertical field to collect hot holes for combined negative charge in the trapping layer so the influence of increased gate voltage is not obvious. On the other hand, for all cases, we use three kind of drain voltage bias for strong and weak impact ionization at depletion of drain-side. It can be clearly seen that larger drain bias induced strong impact ionization makes faster erase speed. According to all of the above, we can clearly observe that SONOS memory with Si-NCs trapping layer has very higher hot holes injection efficiency and faster erase speed.

## 3.4 Characteristic of Retention

### 3.4.1 Characteristic of Retention for Different Temperature

Data retention is an important reliability issue of SONOS memories. In general, retention device of SONOS memories has to be checked by using accelerated test that usually adopts high electric fields and high temperature [33]. In this section, we will discuss data retention for device after programming with different temperature. The flash memory cells are required the charge for 100,000 seconds to be kept. Timing is known to cause fairly uniform wear-out of cell performance due to the oxide damage.

Fig's. 3-7 (a)-(c) show retention characteristic of different temperature for $\triangle V_t$=2-V.

The tunnel oxide of 3-nm was grown in dry $N_2O$ by horizontal-furnace. Fig's. 3-8 (a)-(c) exhibit retention characteristic of different temperature for $\triangle V_t$=2-V. The tunnel oxide of 2.5-nm was grown in dry $N_2O$ by vertical-furnace. And Fig's. 3-9 (a)-(c) show retention characteristic of different temperature for $\triangle V_t$=2-V. The tunnel oxide of 2.5-nm was grown in dry $O_2$ by vertical-furnace. We can clearly see that the memory window narrows to about 1.8-V after $10^4$ seconds for all samples. But there is worse retention at the high temperature.

### 3.4.2 Characteristic of Retention for Different Si-NCs Sizes

In this section, we will discuss data retention for device after programming with different Si-NCs sizes. In general, the flash memory cells are required to keep the charge for 100,000 seconds. Timing is known to cause fairly uniform wear-out of cell performance due to the oxide damage.

Fig's. 3-10 (a)-(c) show retention characteristic of different Si-NCs sizes for $\triangle V_t$=2-V at different temperature. The tunnel oxide of 3-nm was grown in dry $N_2O$ by horizontal-furnace. Fig's. 3-11 (a)-(c) exhibit retention characteristic of different Si-NCs sizes for $\triangle V_t$=2-V at different temperature. The tunnel oxide of 2.5-nm was grown in dry $N_2O$ by vertical-furnace. And Fig's. 3-12 (a)-(c) show retention characteristic of different Si-NCs sizes for $\triangle V_t$=2-V at different temperature. The tunnel oxide of 2.5-nm was grown dry $O_2$ by vertical-furnace. The memory window narrows to about 2-V after $10^4$ seconds for all samples. We can clearly see that the best data retention is Si-NCs_1-min and 30-s sample at each temperature.

### 3.4.3 Characteristic of Retention for Different Tunnel Oxide

In this section, we will discuss data retention for device after programming with different tunnel oxide. In general, the flash memory cells are required to keep the charge for 100,000 seconds. Timing is known to cause fairly uniform wear-out of cell performance due to the oxide damage.

Fig's. 3-13 (a)-(c) show retention characteristic of different tunnel oxide thickness for

△$V_t$=2-V at T=25°C. Fig's. 3-14 (a)-(c) exhibit retention characteristic of different tunnel oxide thickness for △$V_t$=2-V at T=150°C. And Fig's. 3-15 (a)-(c) show retention characteristic of different tunnel oxide thickness for △$V_t$=2-V at T=250°C. The memory window narrows to about 2-V after $10^4$ seconds for all samples. We can clearly see that the best data retention is tunnel oxide of 3-nm in dry $N_2O$ by horizontal-furnace. This charge loss is due to the poor quality of tunnel oxide which results in many leakage current path.

### 3.4.4 Characteristic of Retention for Different Program Window

In this section, we will discuss data retention for device after programming with different program window. The flash memory cells are required the charge for 100,000 seconds to be kept. Timing is known to cause fairly uniform wear-out of cell performance due to the oxide damage.

Fig's. 3-16 (a)-(c) show retention characteristic of different program window at T=25°C. The tunnel oxide of 3-nm was grown in dry $N_2O$ by horizontal-furnace. Fig's. 3-17(a)-(c) exhibit retention characteristic of different program window at T=150°C. The tunnel oxide of 3-nm was grown in dry $N_2O$ by horizontal-furnace. And Fig's. 3-18 (a)-(c) show retention characteristic of different program window at T=250°C. The tunnel oxide of 3-nm was grown in dry $N_2O$ by horizontal-furnace. The memory window narrows to about △$V_t$=1.5-V after ten years for all samples. We observed larger charge loss percentage for ten years when using accelerated test at the high state.

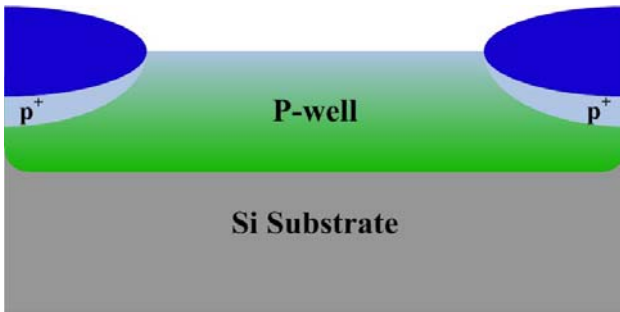
## 3.5 Characteristics of Disturbance

The first failure phenomenon, called program disturbance, often takes place under the electric stress applied to those neighboring un-programmed cells during programming a specific cell in the array. Two types of program disturbance, gate (word-line) disturbance and drain (bit-line) disturbance need be considered. The schematic circuitry of the memory array is shown in Fig. 3-19. During programming cell A, gate disturbance occurs in the cell B and

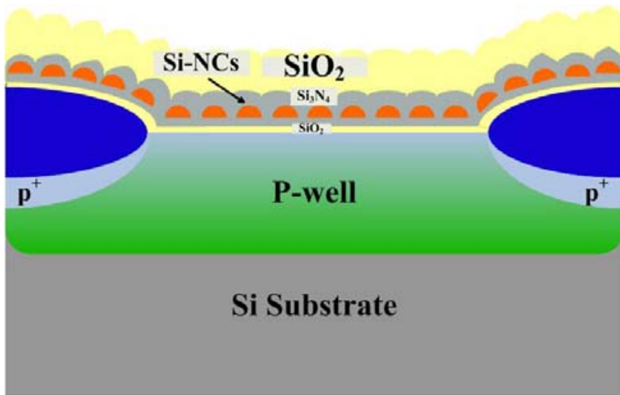
the same for those cells connected with the same with word-line because the gate stress is applied to the same word-line. This is called gate disturbance. During programming cell A, drain disturbance occurs in the cell C and the same for those cells connected with the same with bit-line because the drain stress is applied to the same bit-line. This is called drain disturbance. For the cell reading, the unwanted electron injection would happen while the word-line voltage and bit-line voltage are under read operation. This phenomenon would result in a significant threshold voltage of the selected cell. This is called read disturbance [39].

Fig. 3-20 shows programming gate disturbance characteristic of device with $V_G$=6-V for control, Si-NCs_1m30s and Si-NCs_2min, respectively. The $V_t$ shift of gate disturbance is lower than 0.1-V for 1000s stress with $V_G$=6-V. And Fig. 3-21 exhibits programming gate disturbance characteristic of device with $V_G$=8-V for control, Si-NCs_1m30s and Si-NCs_2min, respectively. The $V_t$ shift of gate disturbance can also be controlled lower than 0.4V for 1000s stress with $V_G$=8-V. After gate electrical stress applied for a long time, it resulted in threshold voltage arising. We proposed due to bad quality of blocking oxide result in the electrons gate injection.

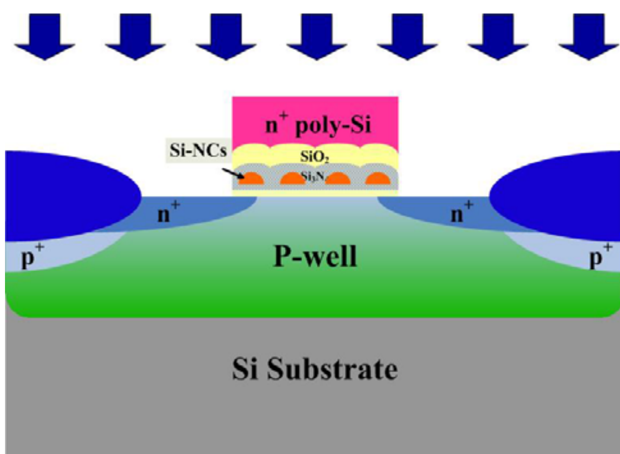
And Fig. 3-22 shows drain disturbance characteristic of device with $V_D$=6-V for control, Si-NCs_1m30s and Si-NCs_2min, respectively. The Vt shift of drain disturbance is lower than 0.04-V at the worse condition of 1000sec stress. Fig. 3-23 exhibits drain disturbance characteristic of device with $V_D$=7-V for control, Si-NCs_1m30s and Si-NCs_2min, respectively. The Vt shift of drain disturbance is lower than 0.1-V at the worse condition of 1000sec stress. After drain electrical stress applied a long time, it resulted in a increase of threshold voltage. It might be due to two factors: The first is due to poor quality of blocking and tunnel oxide result in the gate injection. The other is due to that drain electrical stress applied along long time resulted in the traps and interface states generated at drain-side, and sub-threshold swing became larger.




- P-Well Formation
- LOCOS Formation




- Gate Oxide Formation
  1. Dry $N_2O$ Oxide 3nm by Horizontal-Furnace
  2. Dry Oxide 2.5nm by Vertical Furnace
     a.$N_2O$
     b.$O_2$
- Trapping Layer Formation:
  1. Nitride: 3nm at 780˚C
  2. a-Si: 2min / 1m30s at 550˚C
  3. Nitride : 4nm at 780˚C
- HDPCVD Oxide 20nm as Blocking Oxide




- Deposited Poly-Si 200nm as Gate Layer and n+ implantation
- Gate Pattern Defined
- Source/Drain was implanted As and Dopant Activation

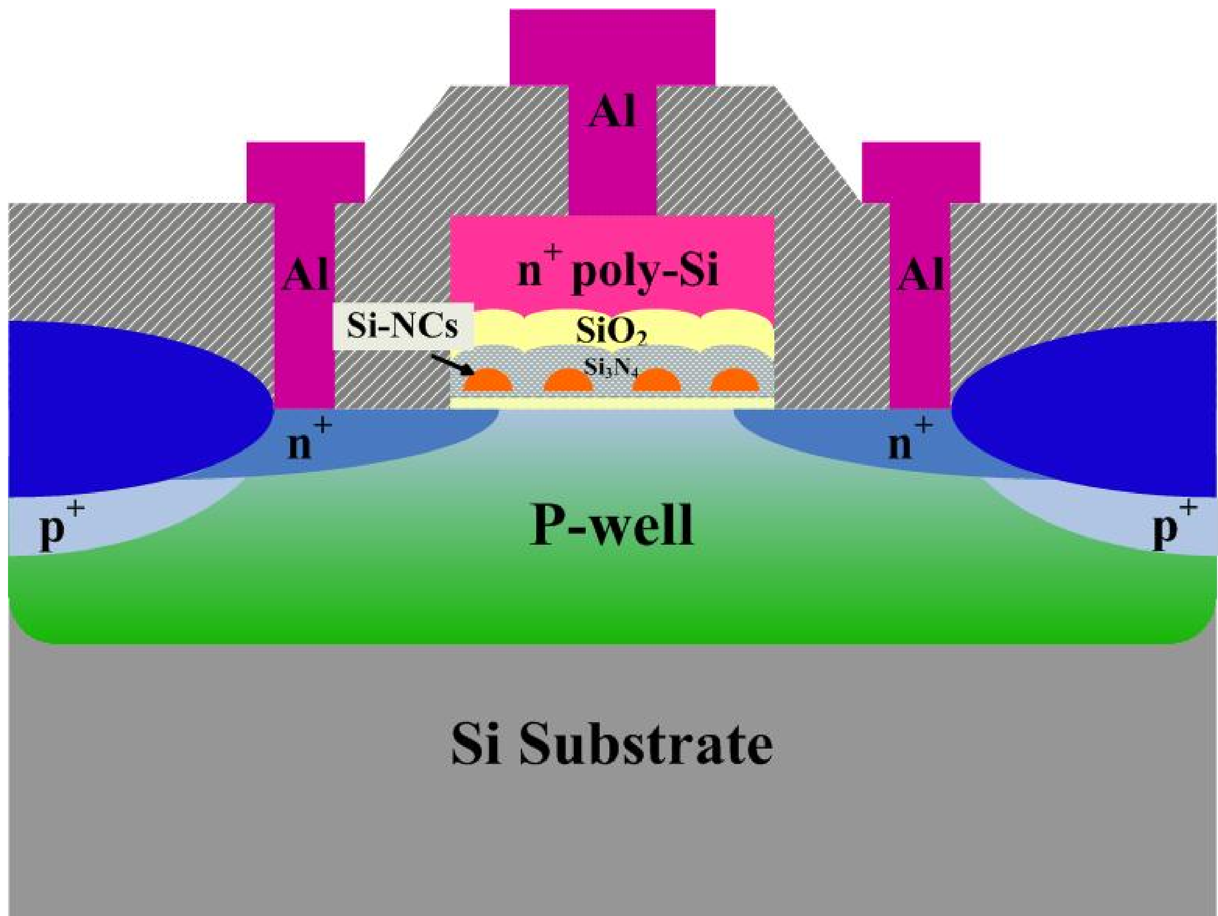



**Fig. 3-1** Process flows of Si-NCs SONOS memory. After dopant activation, deposited 400nm passivation oxide, and metallization, we had finished device fabrication. During the nitride deposition step, the Si-NCs trapping layer was crystallized and Si-NCs embedded in $Si_3N_4$ were formed.

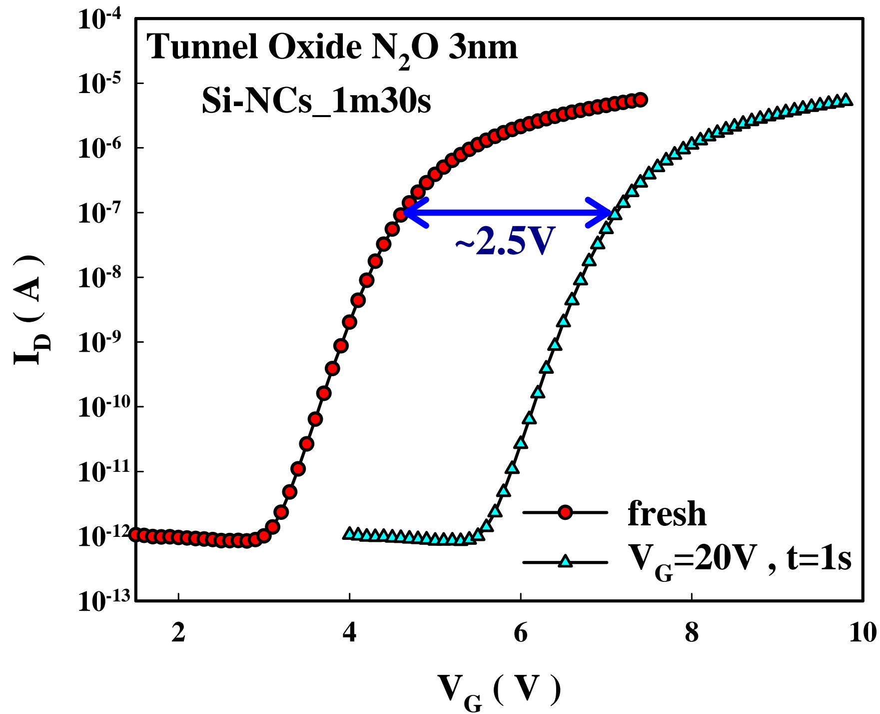
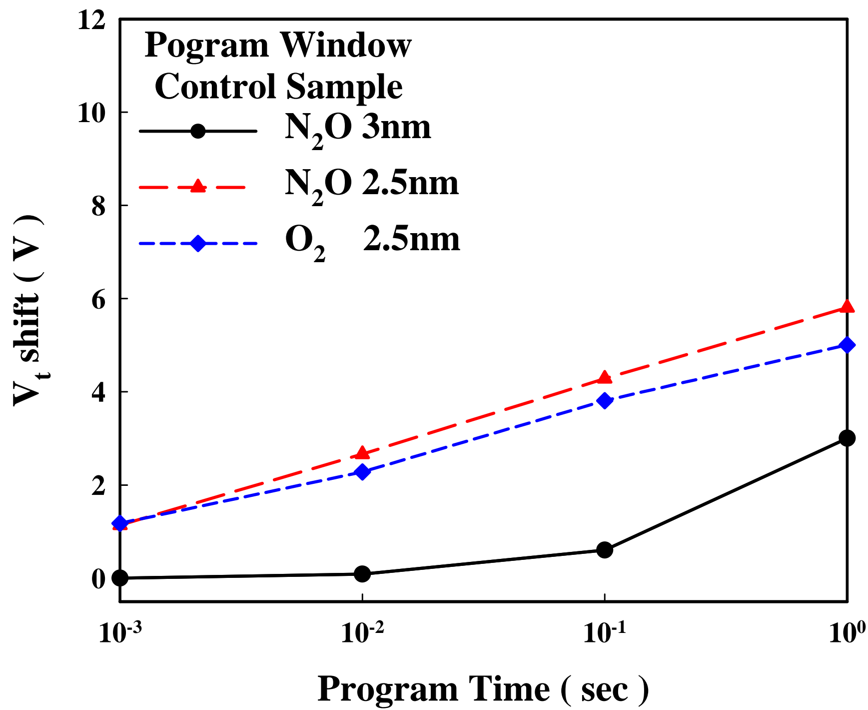
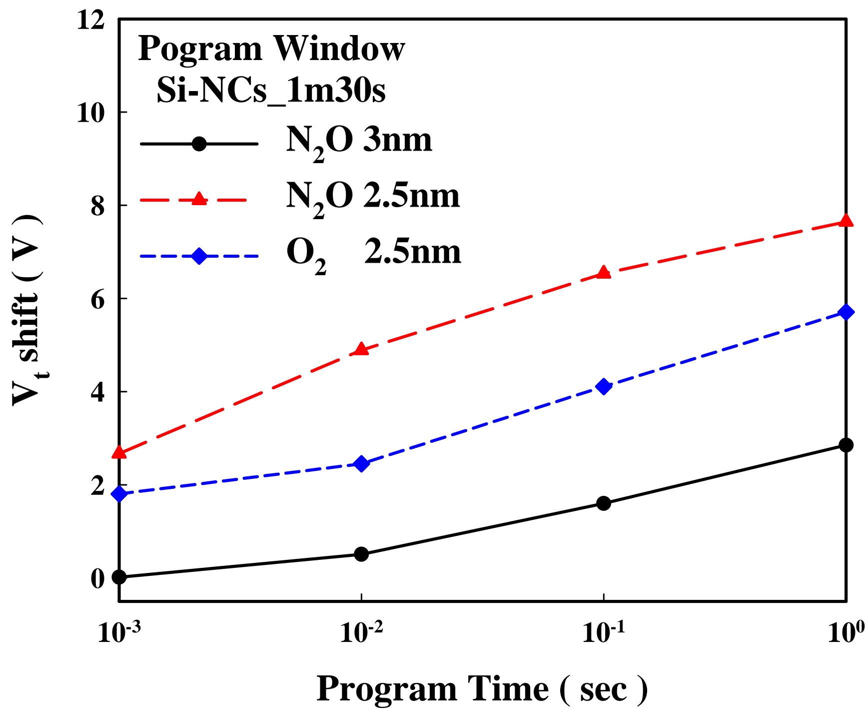



**Fig. 3-2** Transfer characteristic of fresh state and program state for Si-NCs_1m30s sample. A memory window about 2.5V can be easily achieved, when program time is 1sec. The leakage current of Si-NCs_1m30s sample is about $10^{-12}$A.




(a)

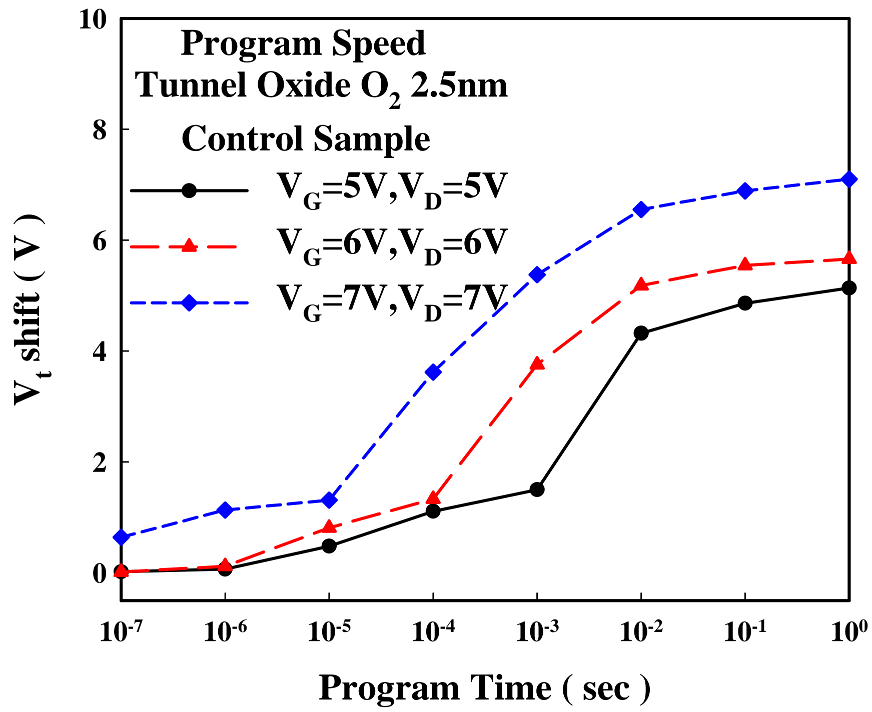


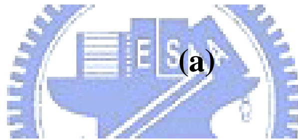

(b)

**Fig. 3-3** Program speed characteristic for different sample. This gate voltage bias is 20V and tunnel oxide by dry $N_2O$ 3nm horizontal-furnace. The programming time be 1s if the windows margin is set about 3V with $V_G$=20V for control sample.(a) control sample and (b) Si-NCs_1m30s sample.

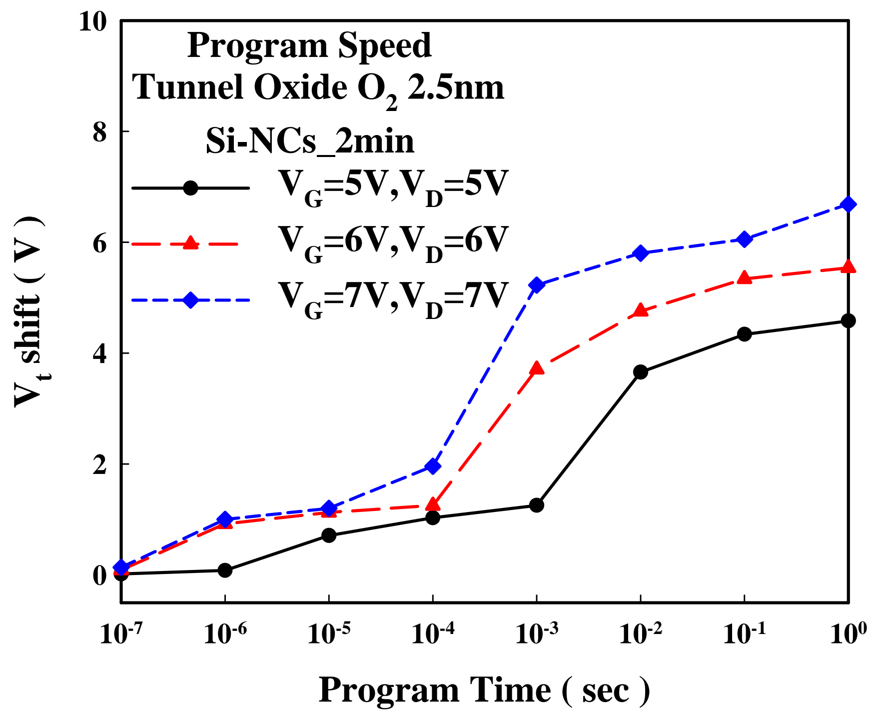
**Table 3-1** Summary for program window of different tunnel oxide film when $V_G$=20V and stress 1sec. The program window of Si-NCs_1m30s is larger for control sample.

| **Program Window for 1s at $V_G$=20V** | | | | | | |
|---|---|---|---|---|---|---|
| | **$N_2O$ 3nm** | | **$N_2O$ 2.5nm** | | **$O_2$ 2.5nm** | |
| | **Control** | **Si-NCs_1m30s** | **Control** | **Si-NCs_1m30s** | **Control** | **Si-NCs_1m30s** |
| Program Window | **3** | **2.85** | **5.8** | **7.64** | **5** | **5.7** |

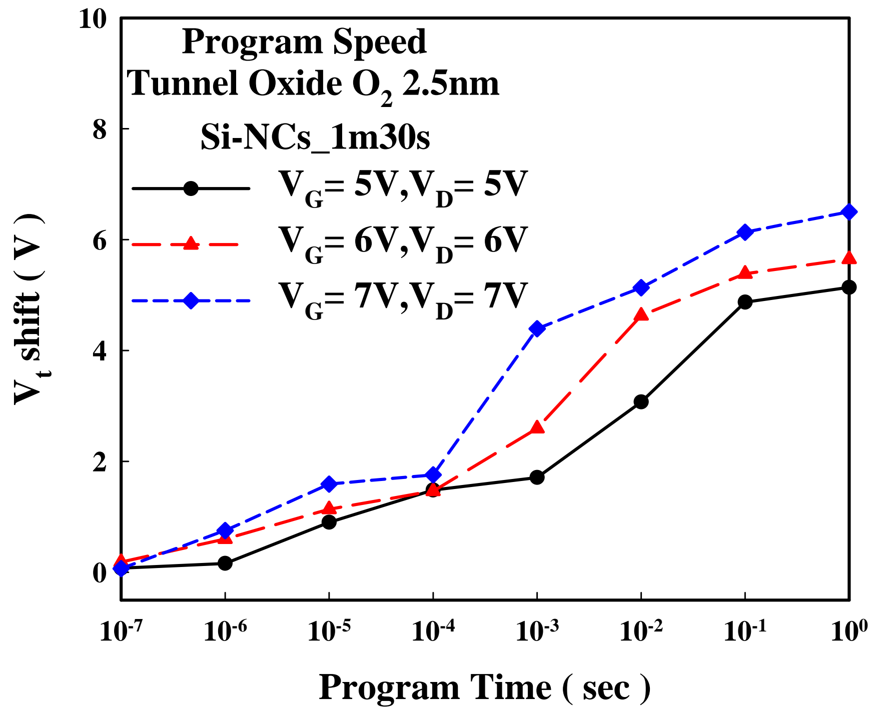


(a)

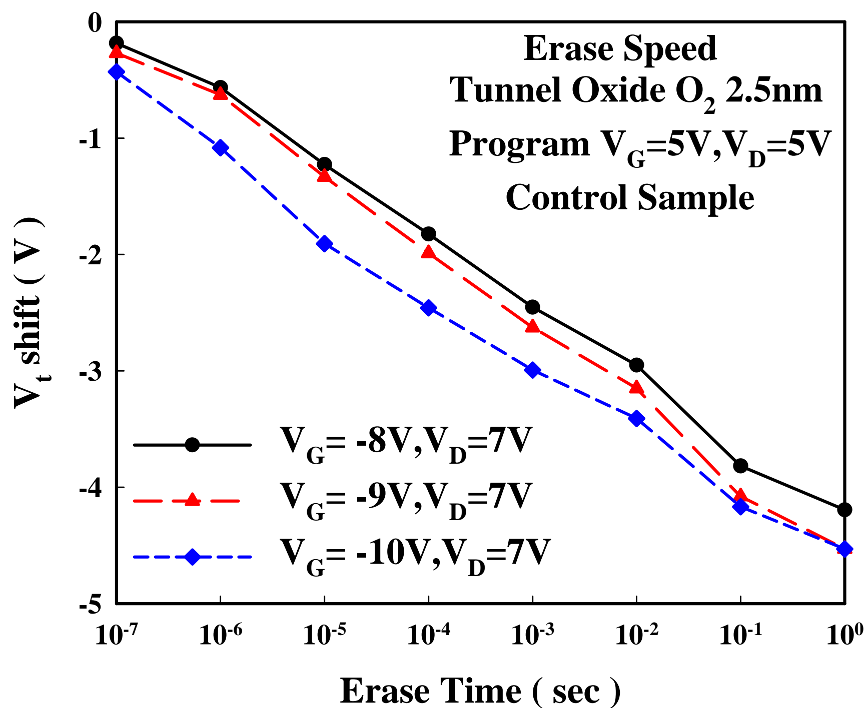



(b)

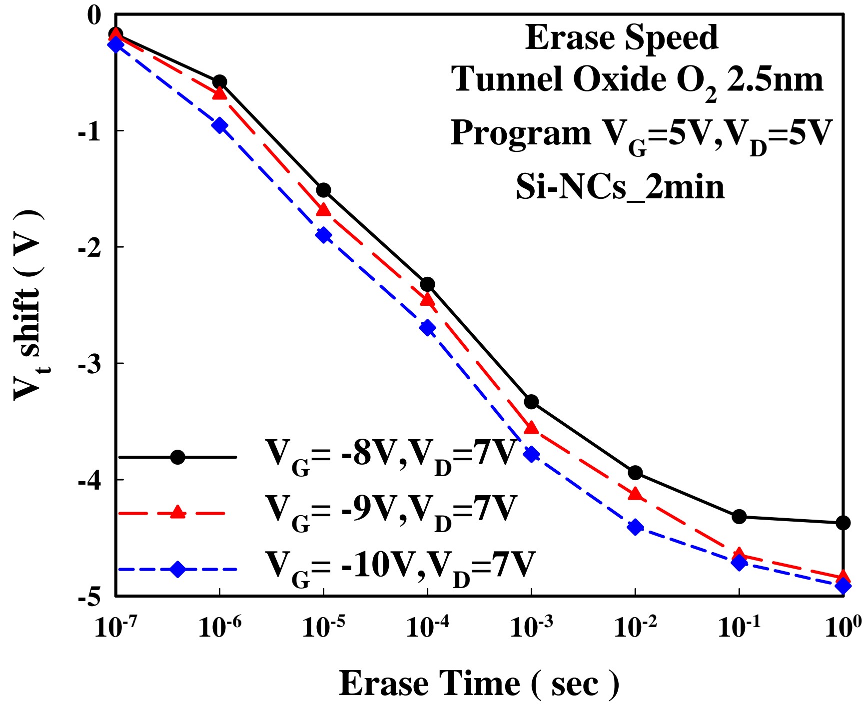



(c)

**Fig. 3-4** Program speed characteristic for different programming conditions at different $V_G$ and $V_D$. The programming time can be as short as 10μs if the windows margin is set about 1V with $V_G$=6V, $V_D$=6V. This tunnel oxide is dry $O_2$ 2.5nm vertical-furnace. (a) control sample, (b) Si-NCs_2min sample and (c) Si-NCs_1m30s sample.




(a)

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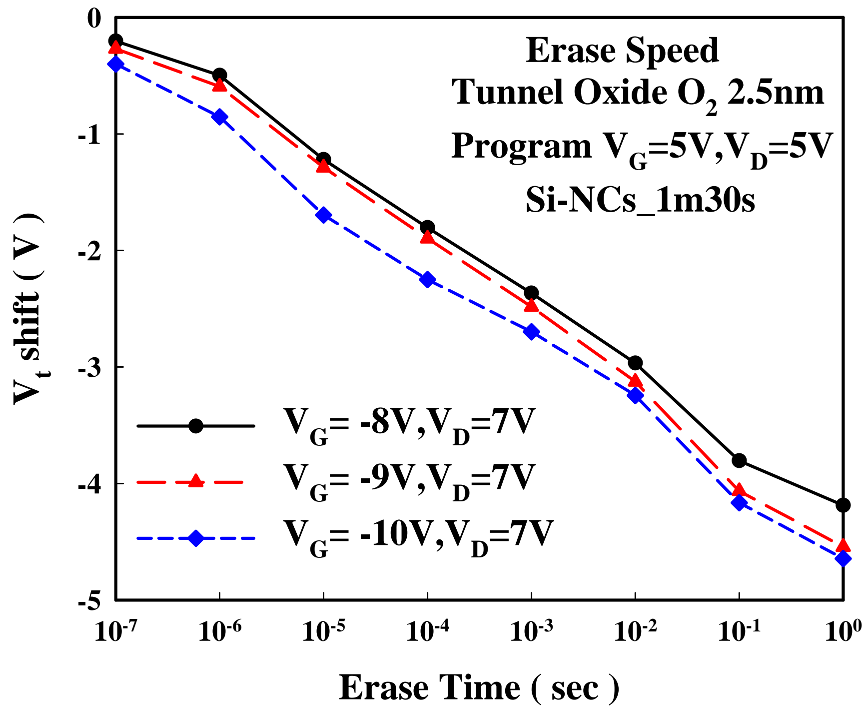
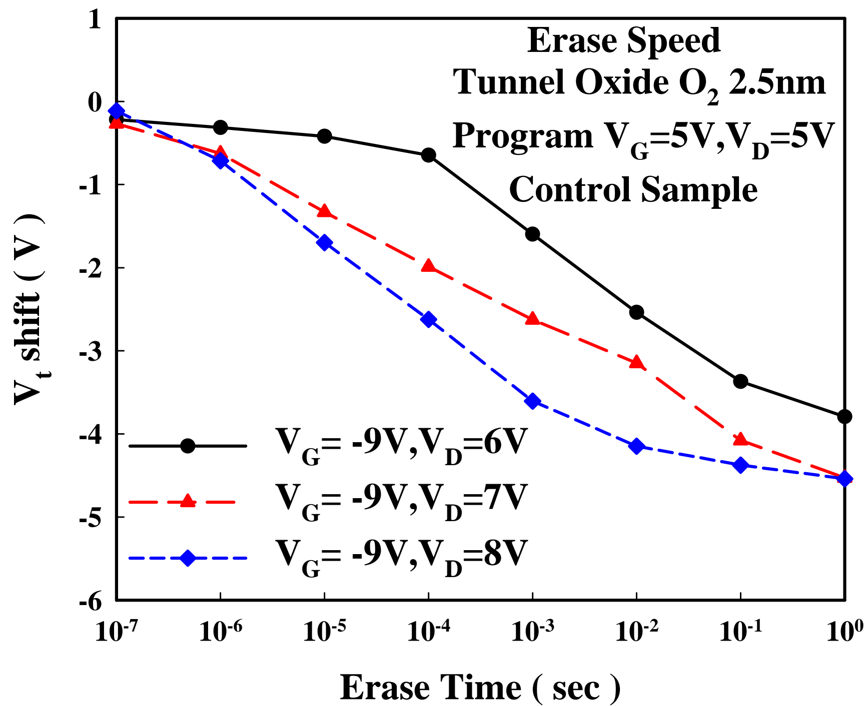
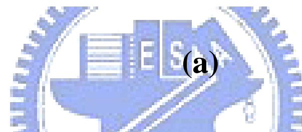


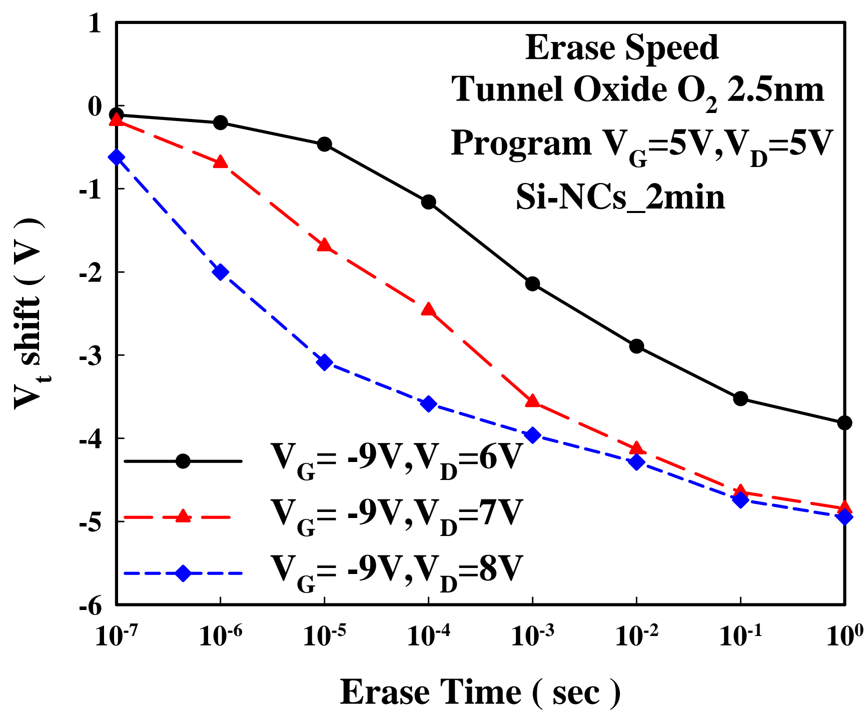

(c)

**Fig. 3-5** Erase speed characteristic for different erasing conditions at $V_D$=7V and different $V_G$. The erasing time can be as short as μs order. This tunnel oxide is dry $O_2$ 2.5nm vertical-furnace. (a) control sample, (b) Si-NCs_2min sample and (c) Si-NCs_1m30s sample.



(a)

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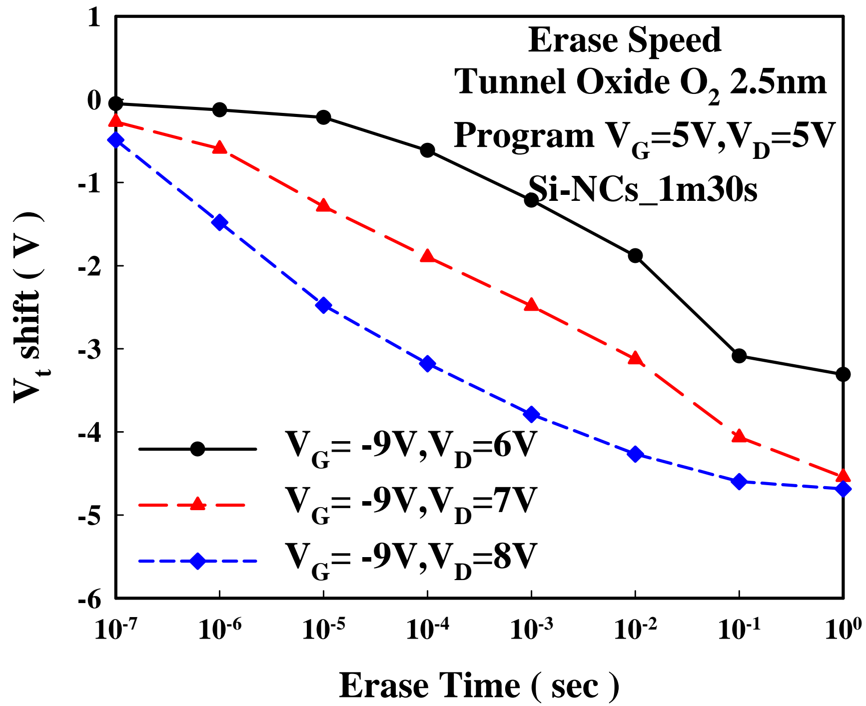
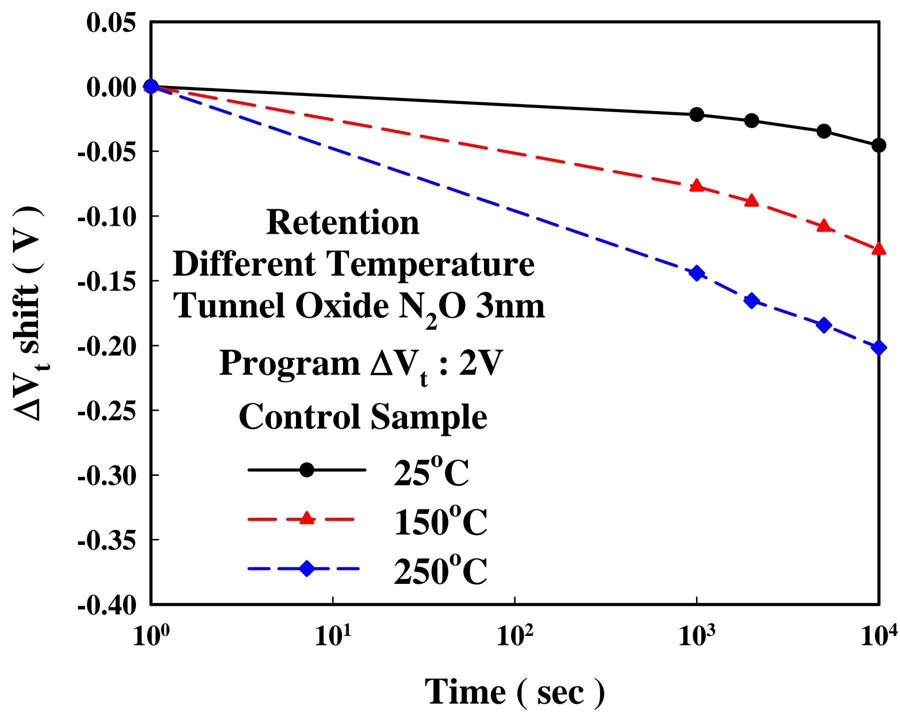
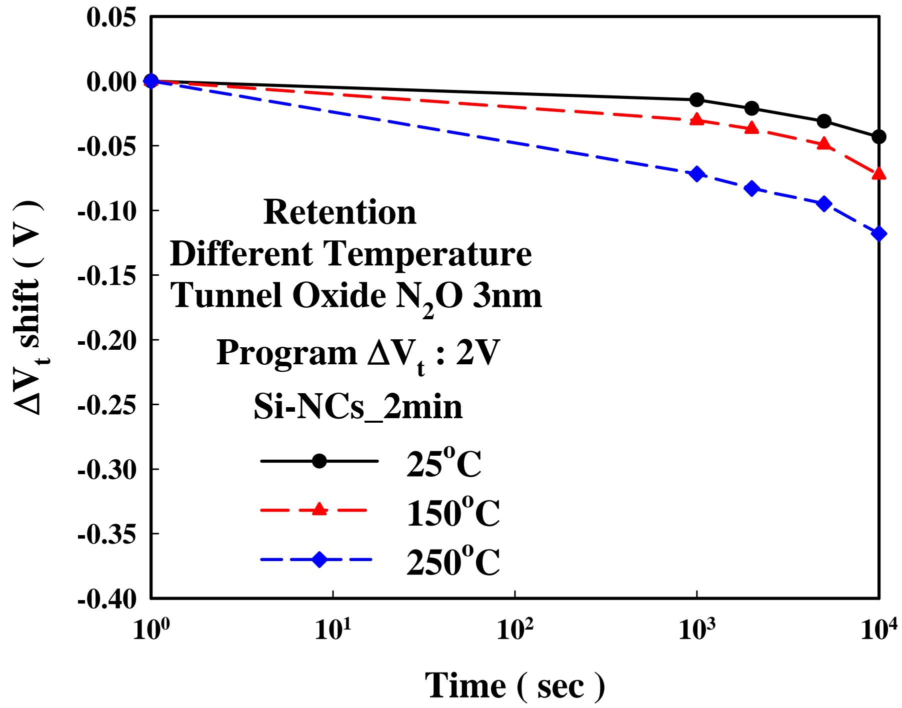



(c)

**Fig. 3-6** Erase speed characteristic for different erasing conditions at $V_G$=-9V and different $V_D$. The erasing time can be as short as μs order. This tunnel oxide is dry $O_2$ 2.5nm vertical-furnace. (a) control sample, (b) Si-NCs_2min sample and (c) Si-NCs_1m30s sample.




(a)

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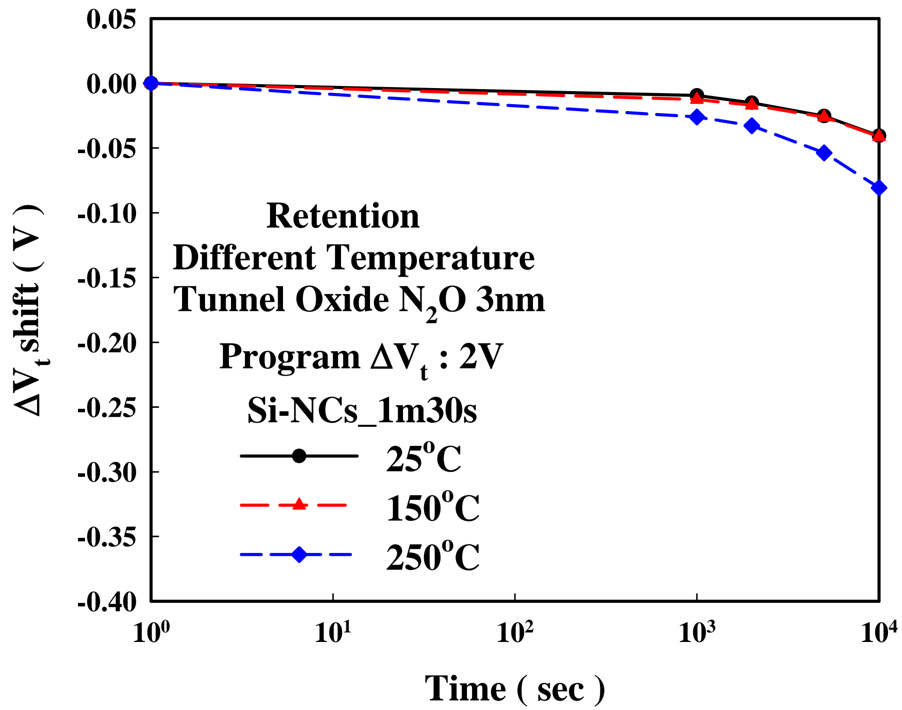
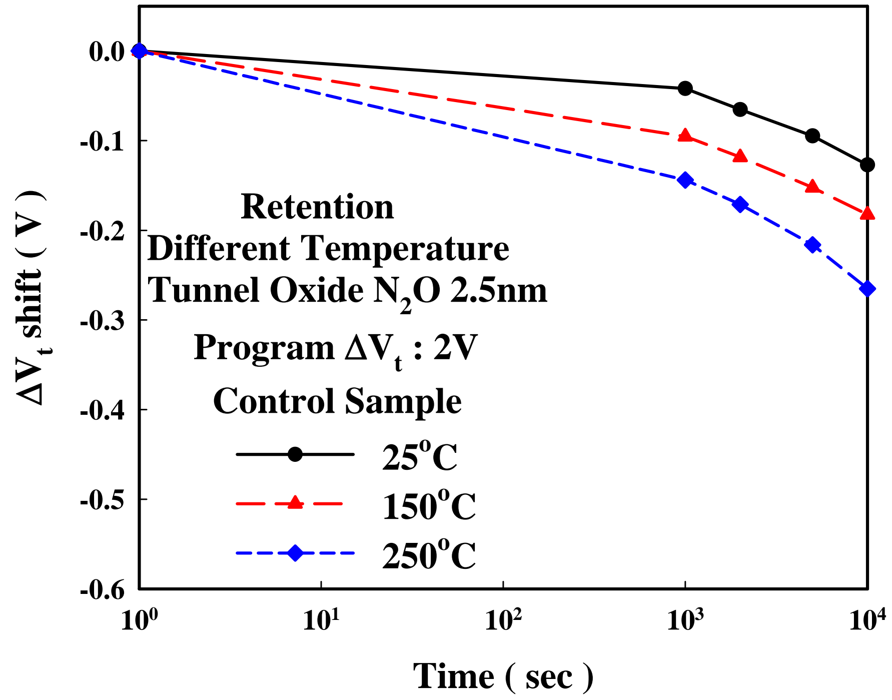
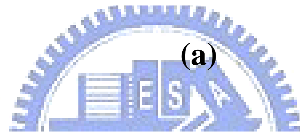


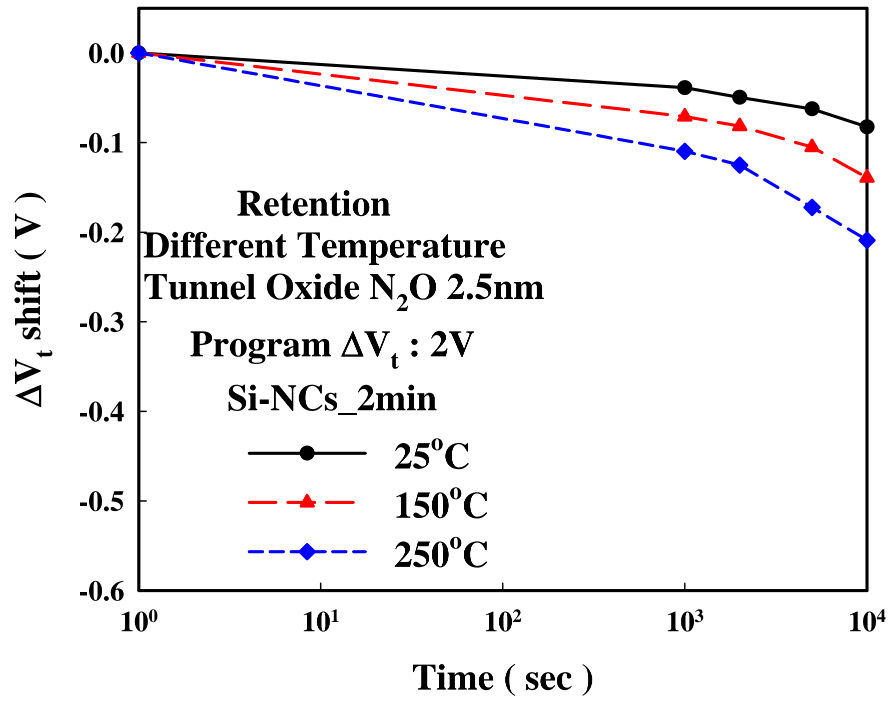

(c)

**Fig. 3-7** Data retention characteristic of different sample for $\triangle V_t$=2V. (a) control sample, (b) Si-NCs_2min sample and (c) Si-NCs_1m30s sample. The tunnel oxide is dry $N_2O$ 3nm by horizontal-furnace.




(a)



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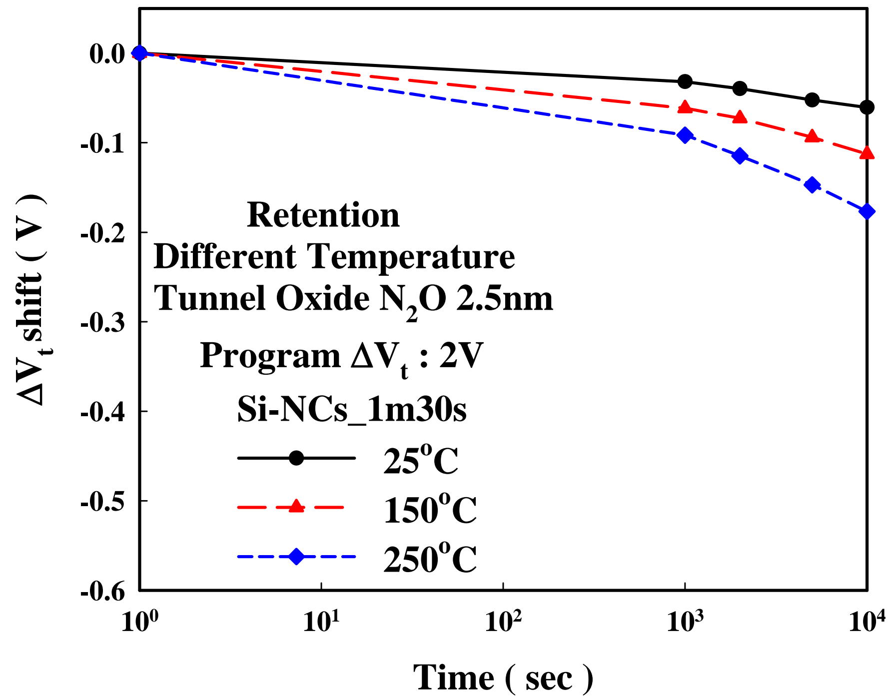
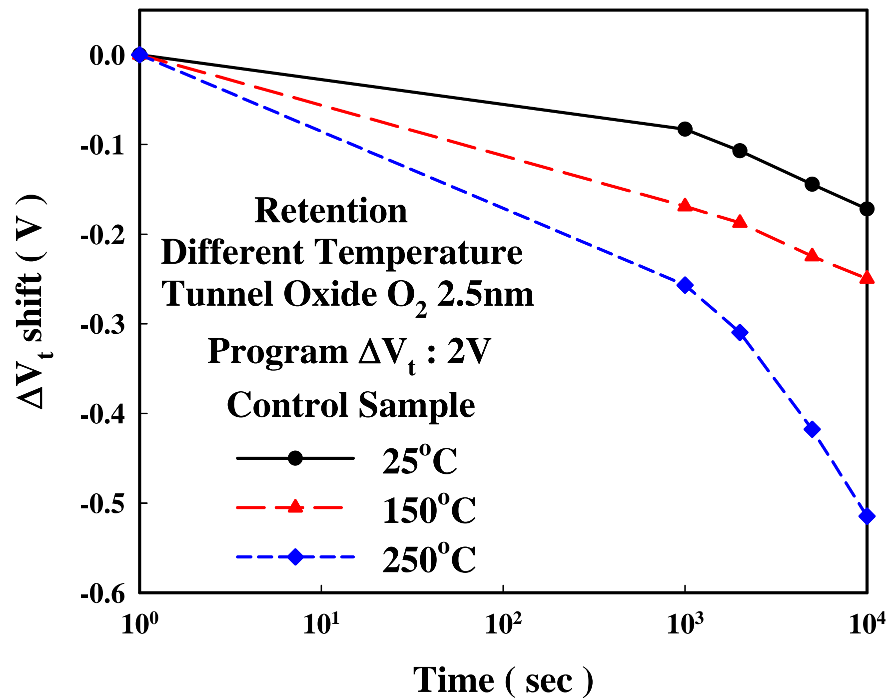
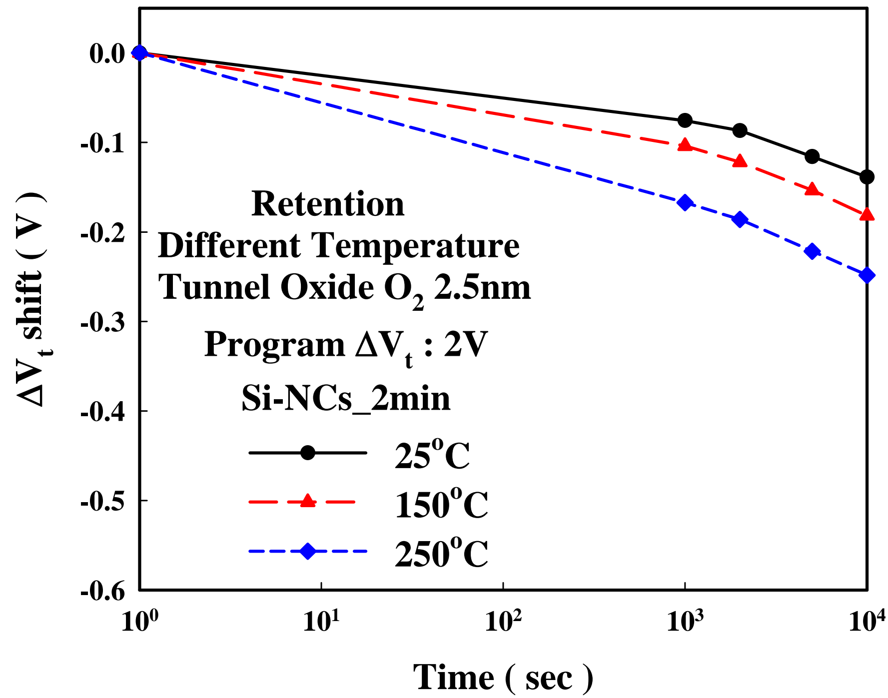



(c)

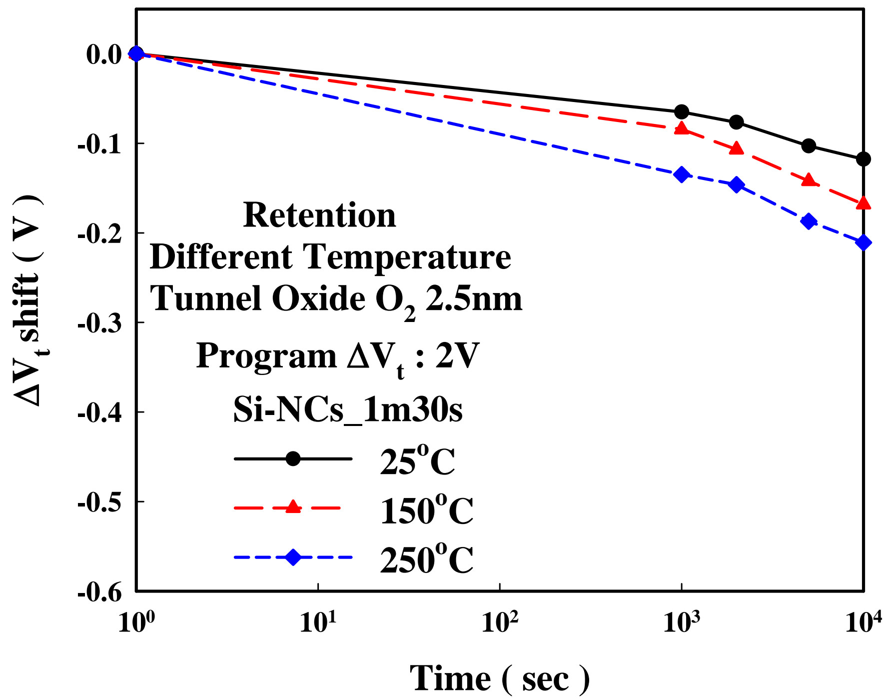
**Fig. 3-8** Data retention characteristic of different sample for $\triangle V_t$=2V. (a) control sample, (b) Si-NCs_2min sample and (c) Si-NCs_1m30s sample. The tunnel oxide is dry $N_2O$ 2.5nm by vertical-furnace.




(a)

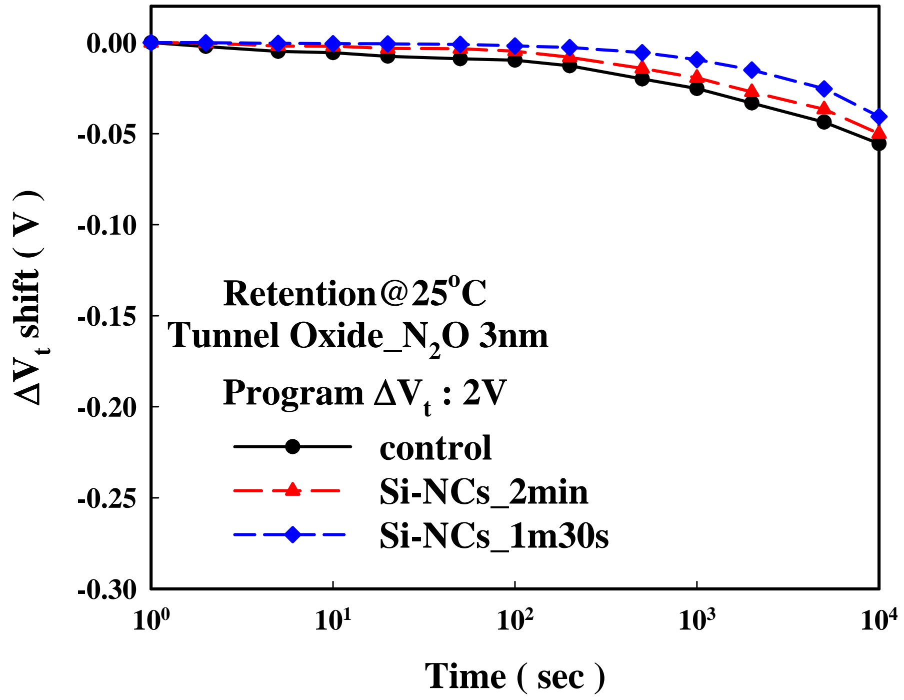


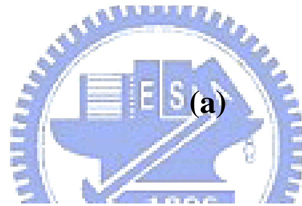
(b)



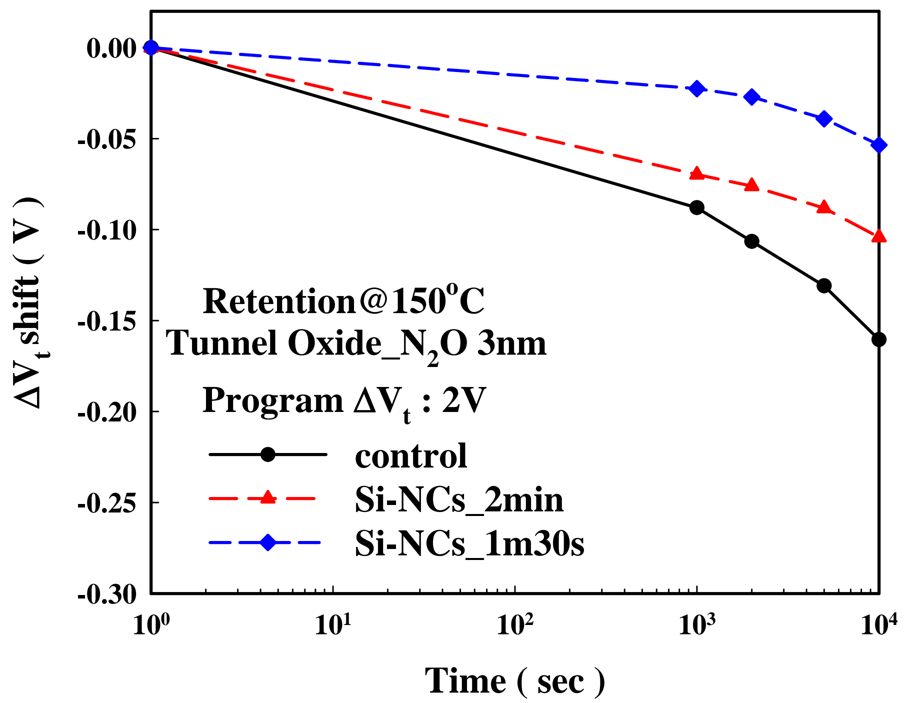

(c)

**Fig. 3-9** Data retention characteristic of different sample for $\triangle V_t$=2V. (a) control sample, (b) Si-NCs_2min sample and (c) Si-NCs_1m30s sample. The tunnel oxide is dry $O_2$ 2.5nm by vertical-furnace.



(a)

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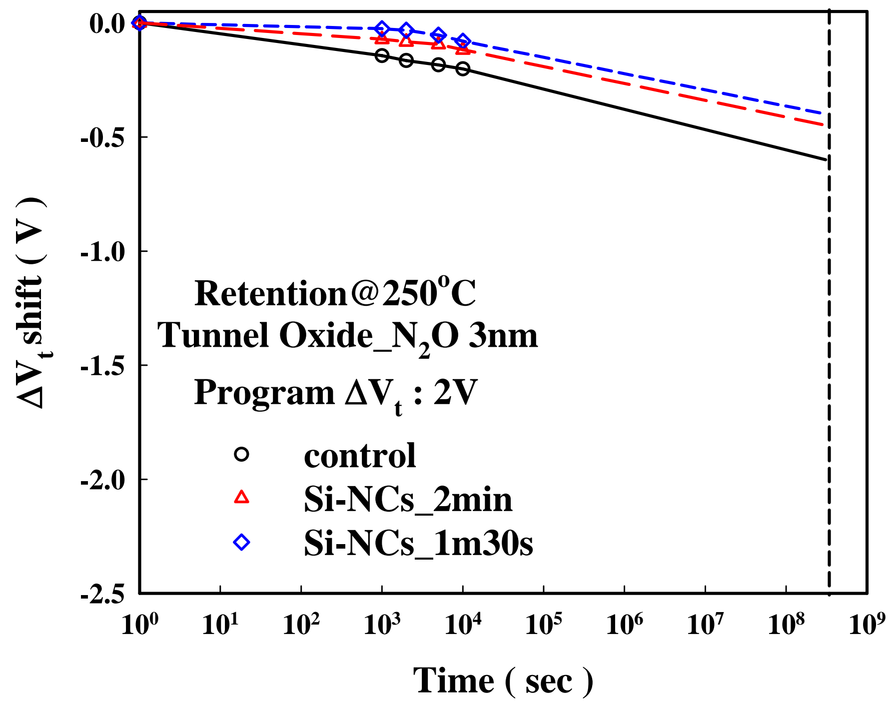
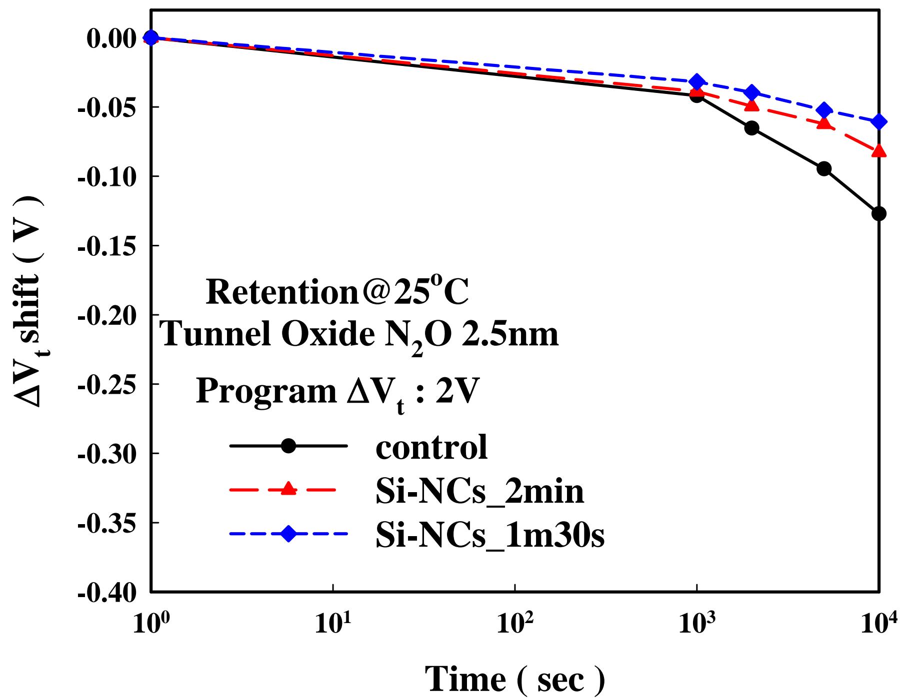
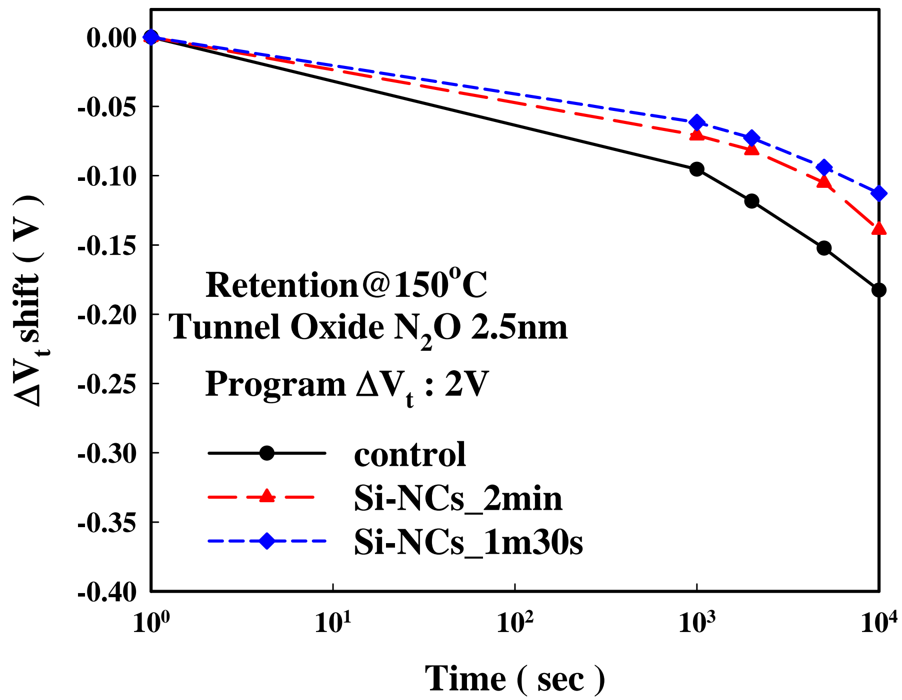



(c)

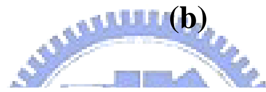
**Fig. 3-10** Data retention characteristic of different temperature for dry $N_2O$ 3nm by horizontal-furnace when programming △Vt=2V. (a) At T=25℃, (b) At T=150℃ and (c) At T=250℃.

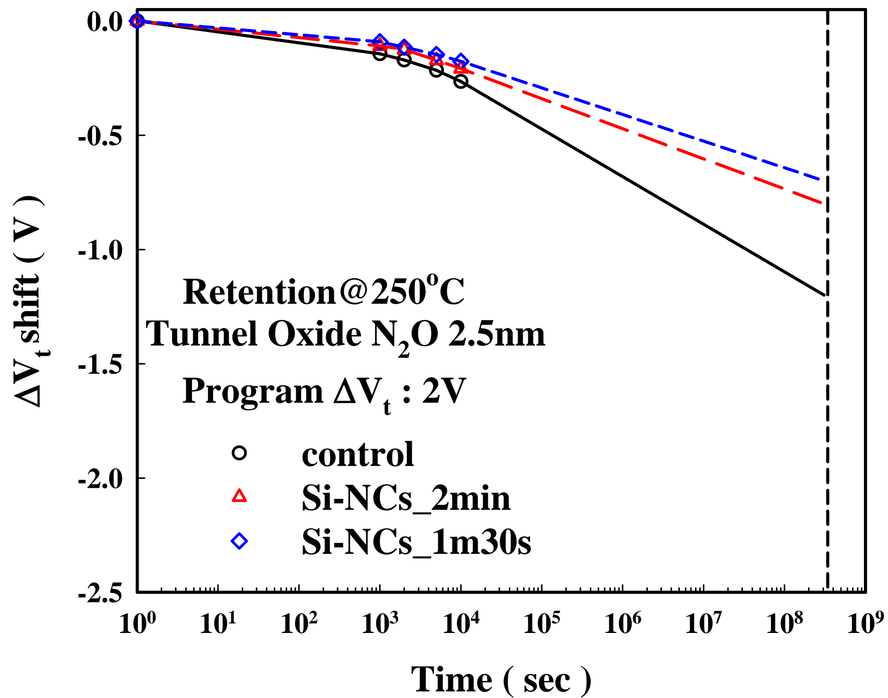



(a)



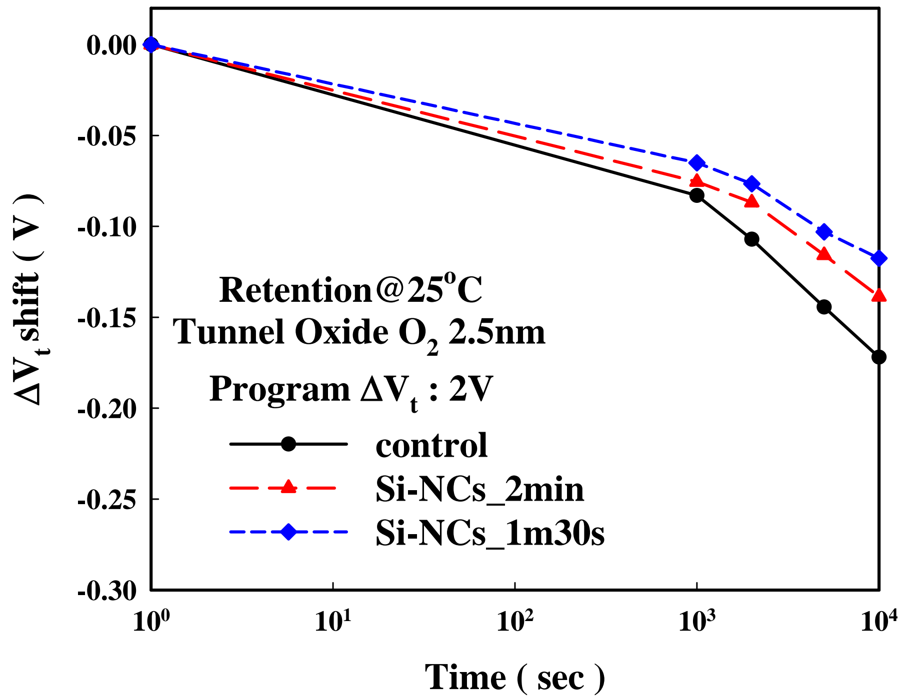

(b)

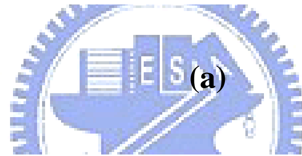




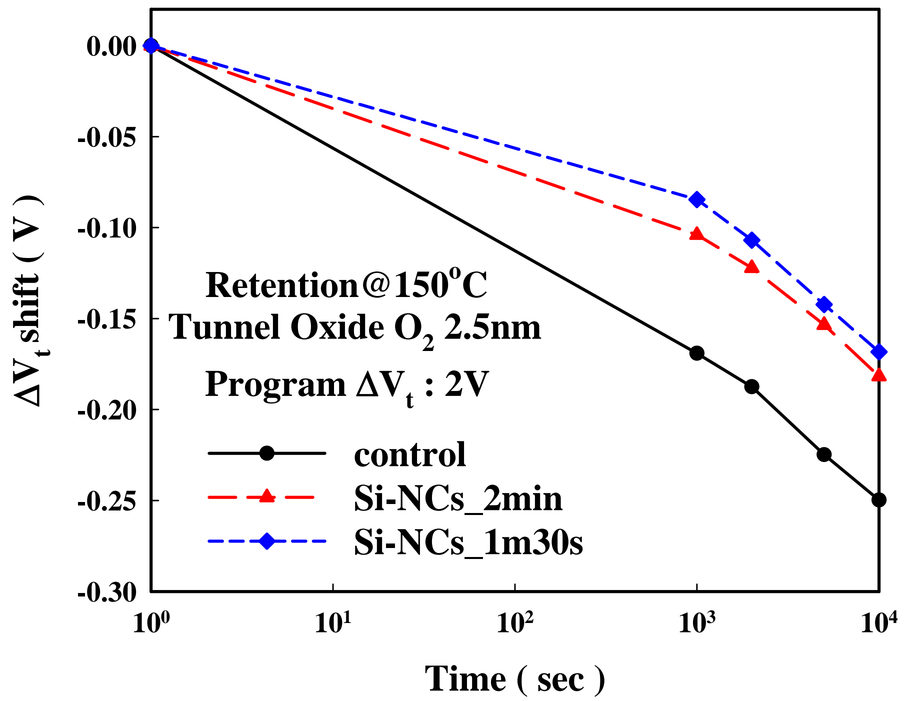

(c)

**Fig. 3-11** Data retention characteristic of different temperature for dry $N_2O$ 2.5nm by vertical-furnace when programming △Vt=2V. (a) At T=25℃, (b) At T=150℃ and (c) At T=250℃.



(a)

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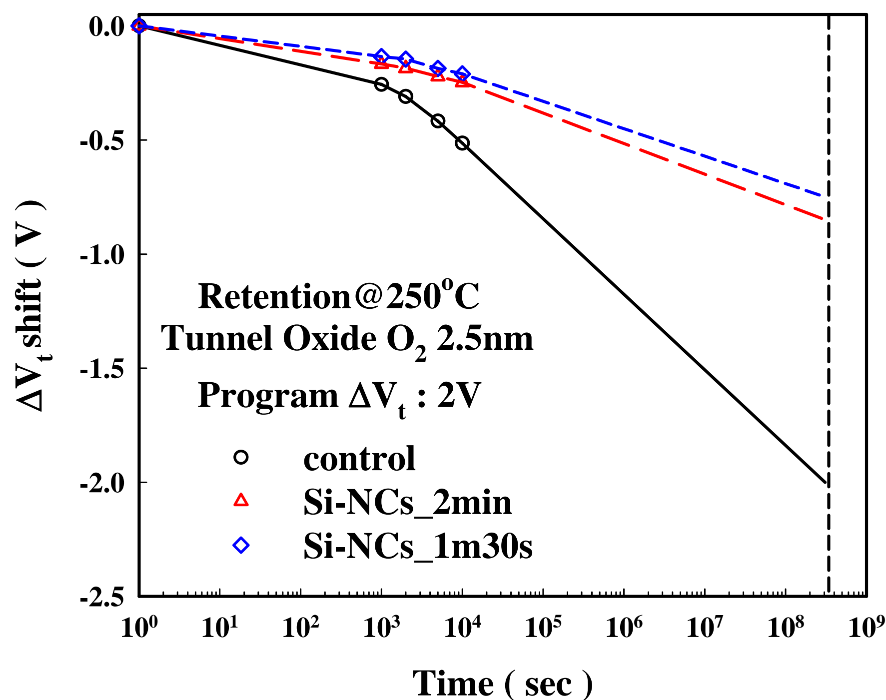
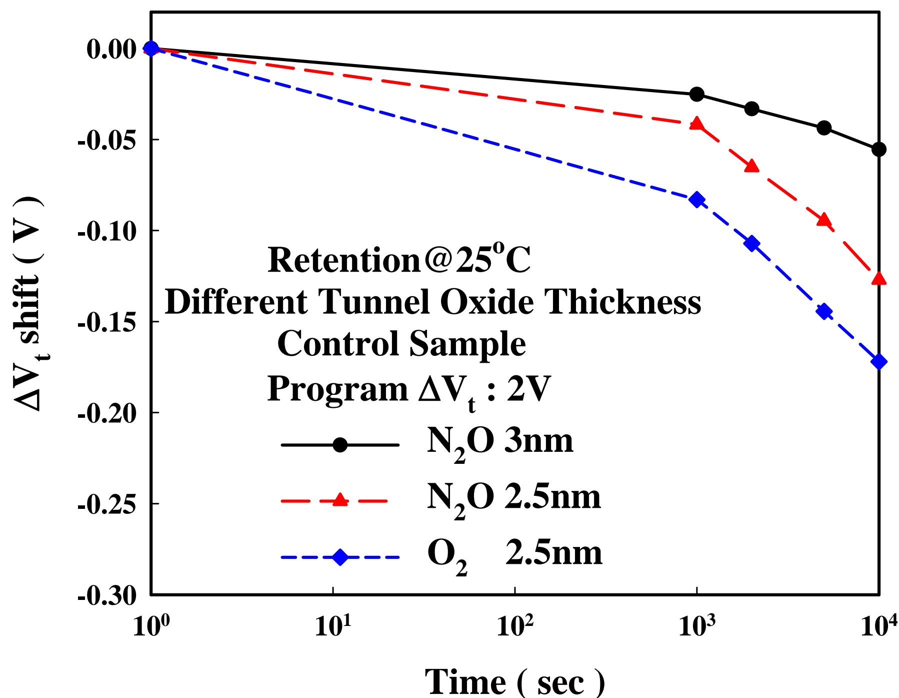
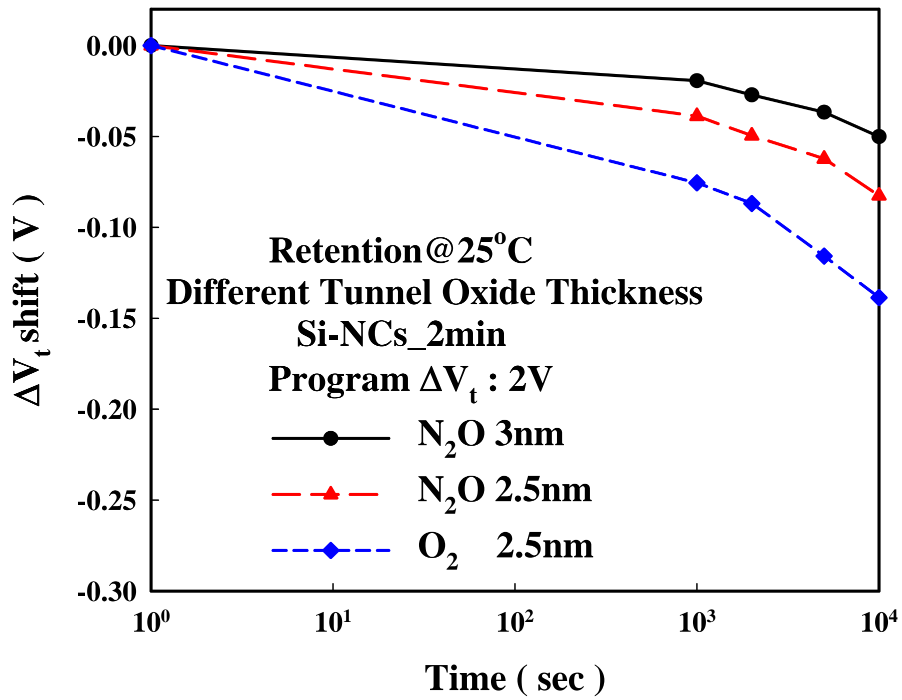



(c)

**Fig. 3-12** Data retention characteristic of different temperature for dry $O_2$ 2.5nm by vertical-furnace when programming △Vt=2V. (a) At T=25℃, (b) At T=150℃ and (c) At T=250℃.




(a)

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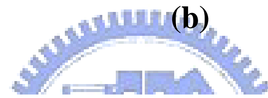
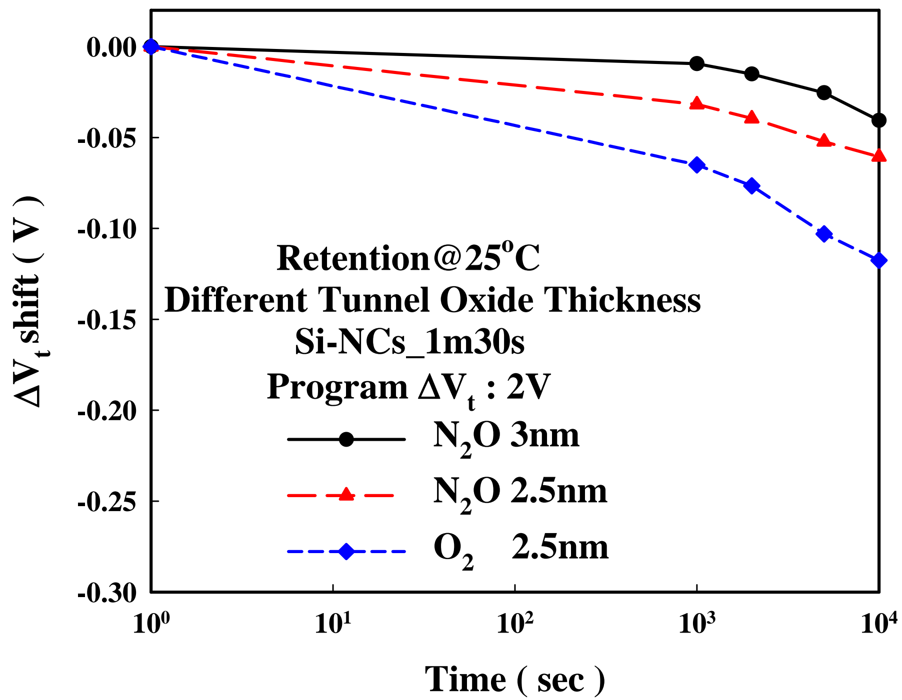
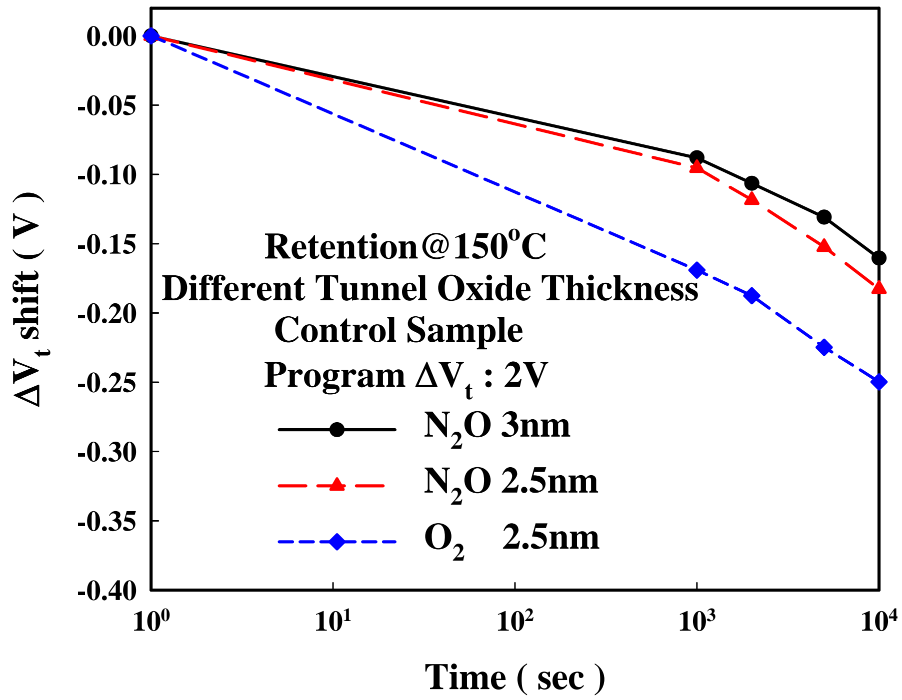
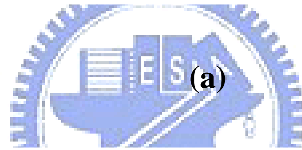




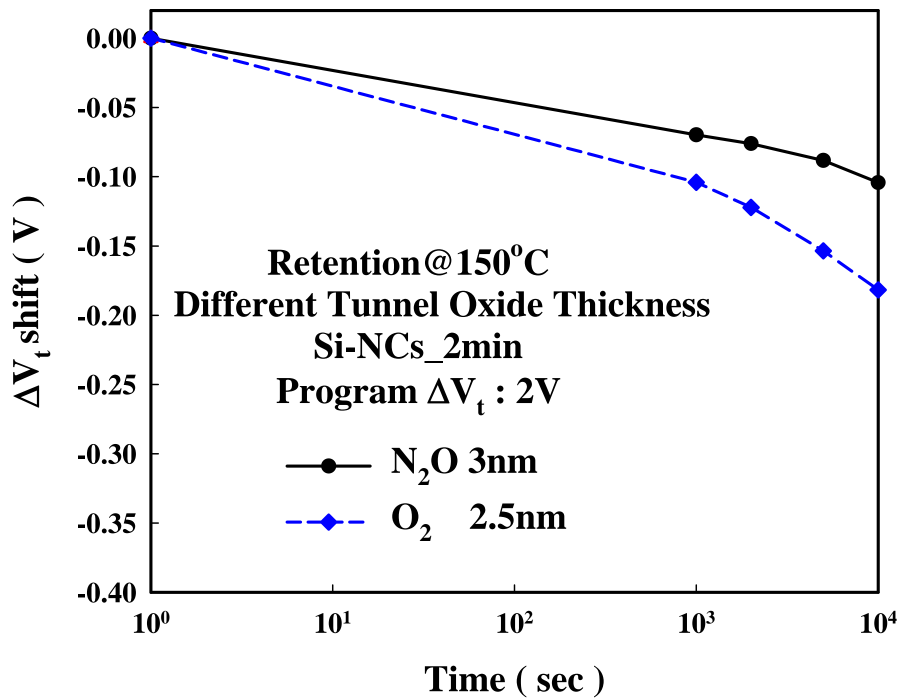

(c)

**Fig. 3-13** Data retention characteristic of different sample for different tunnel oxide film when programming △Vt=2V at T=25℃. (a) control sample, (b) Si-NCs_2min sample and (c) Si-NCs_1m30s sample.



(a)

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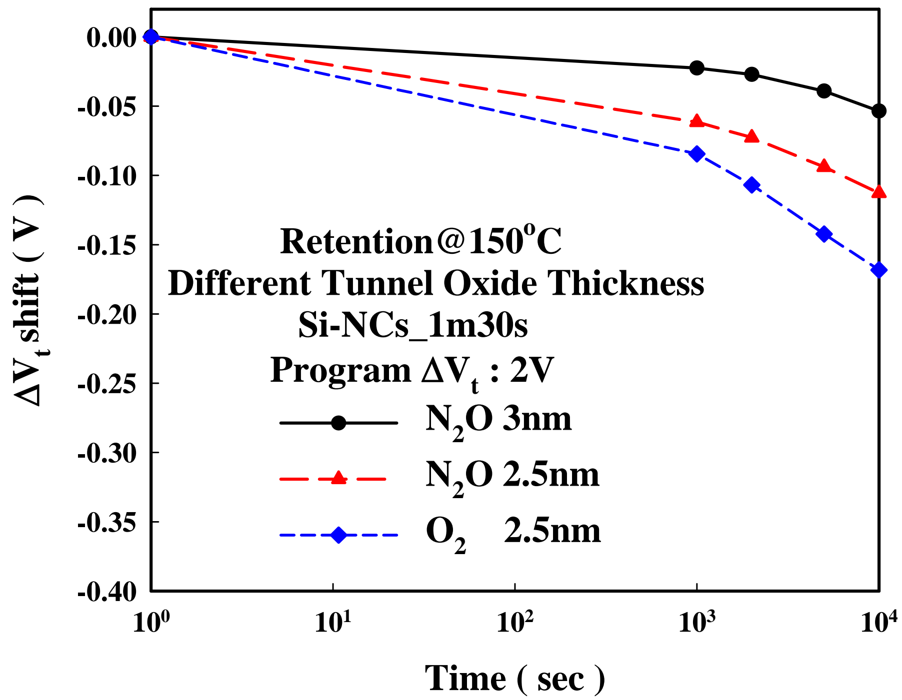
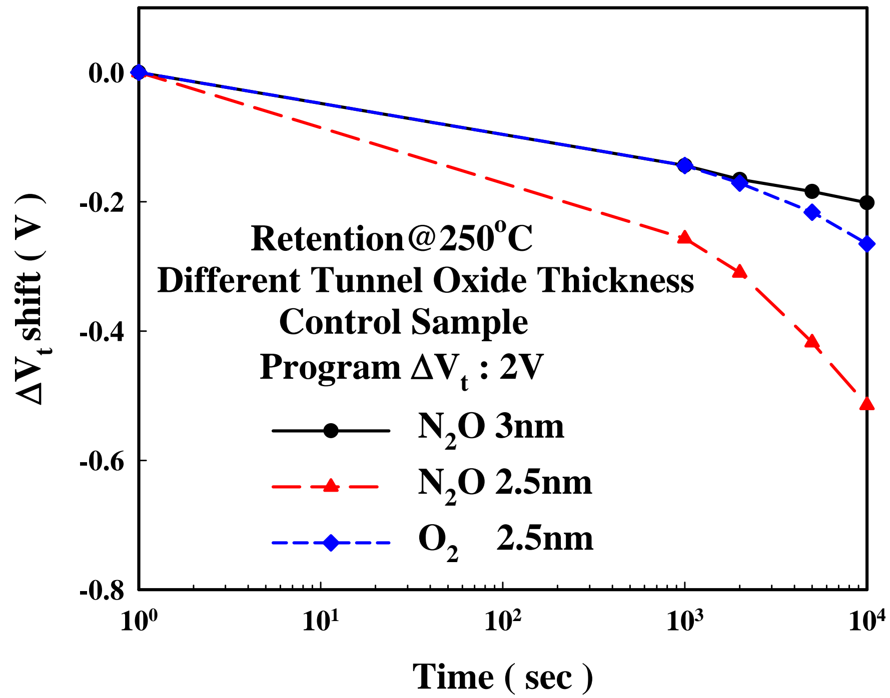
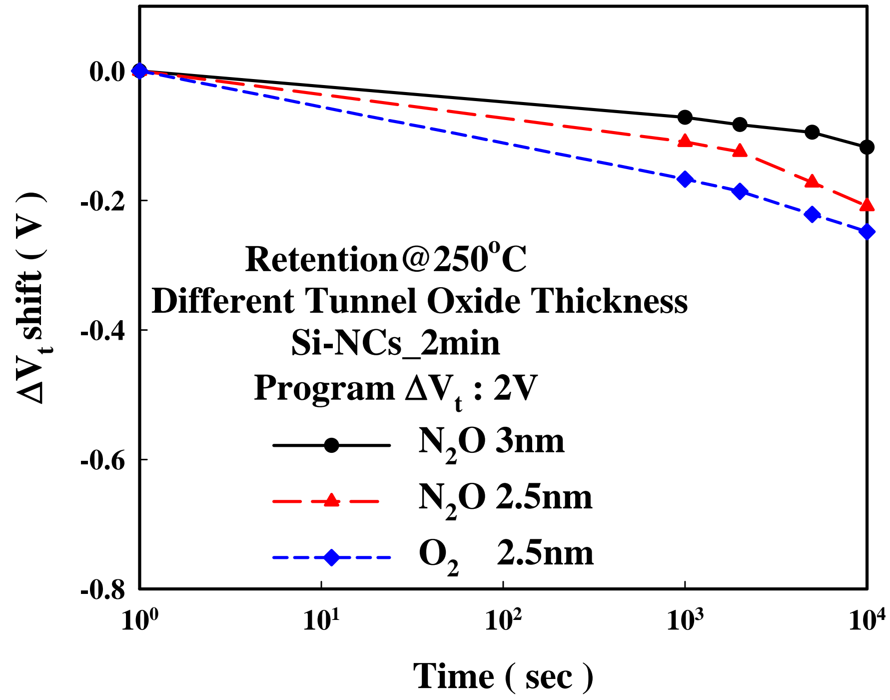



(c)

**Fig. 3-14** Data retention characteristic of different sample for different tunnel oxide film when programming △Vt=2V at T=150℃. (a) control sample, (b) Si-NCs_2min sample and (c) Si-NCs_1m30s sample.




(a)



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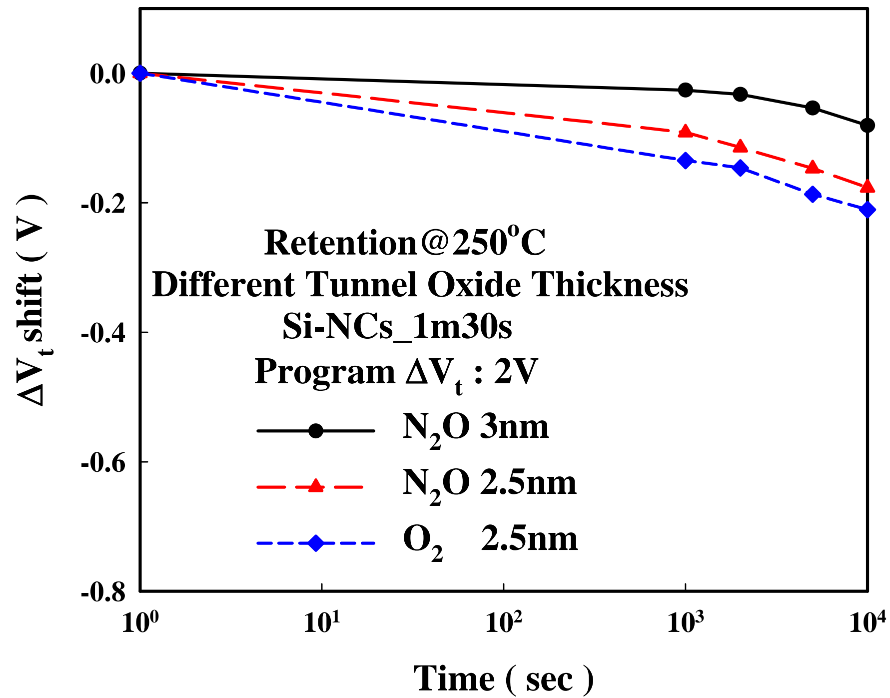
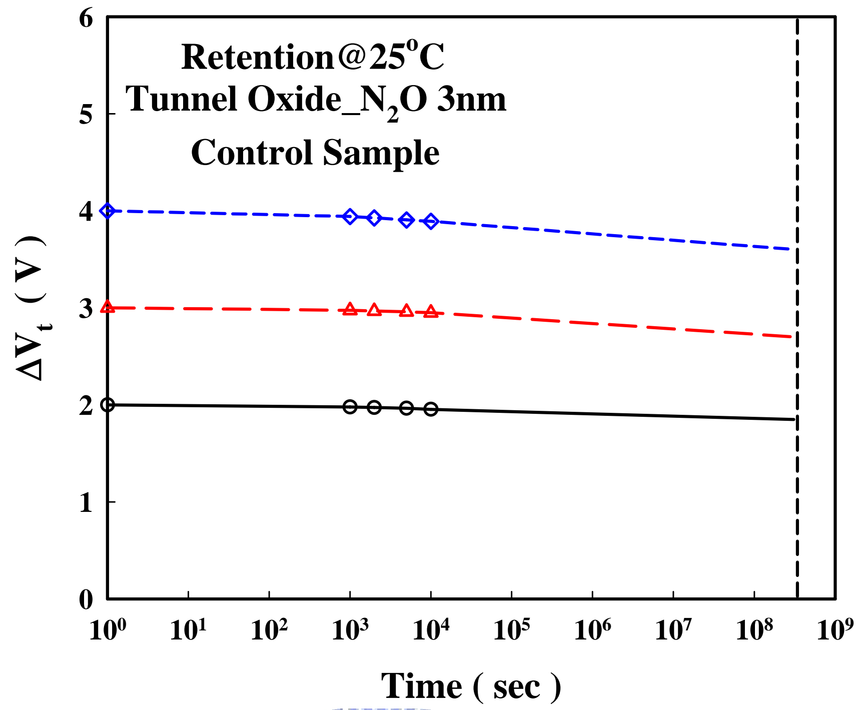



(c)

**Fig. 3-15** Data retention characteristic of different sample for different tunnel oxide film when programming △Vt=2V at T=250℃. (a) control sample, (b) Si-NCs_2min sample and (c) Si-NCs_1m30s sample.

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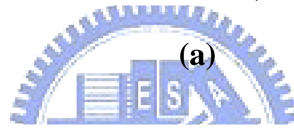

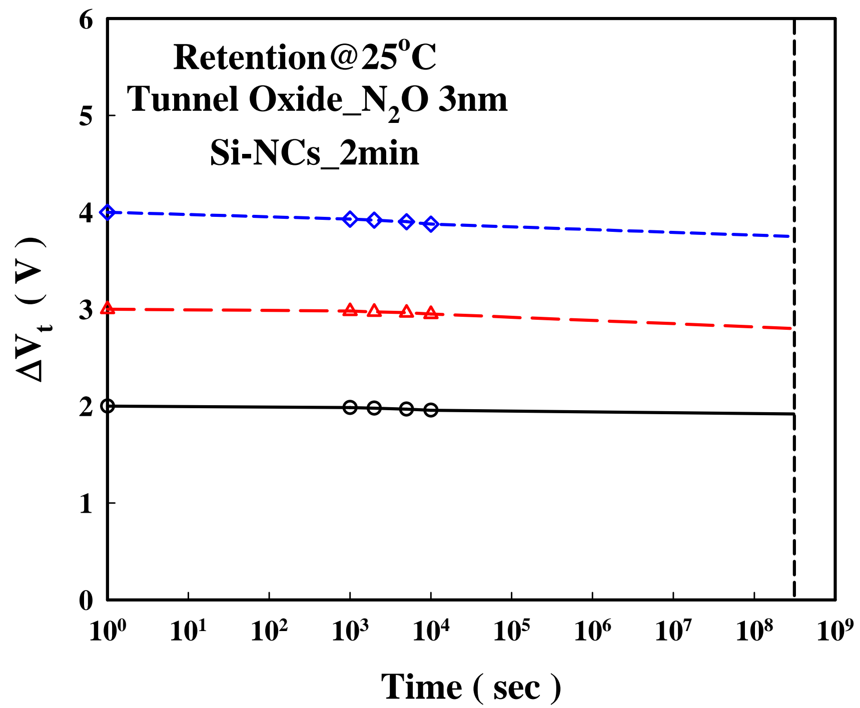


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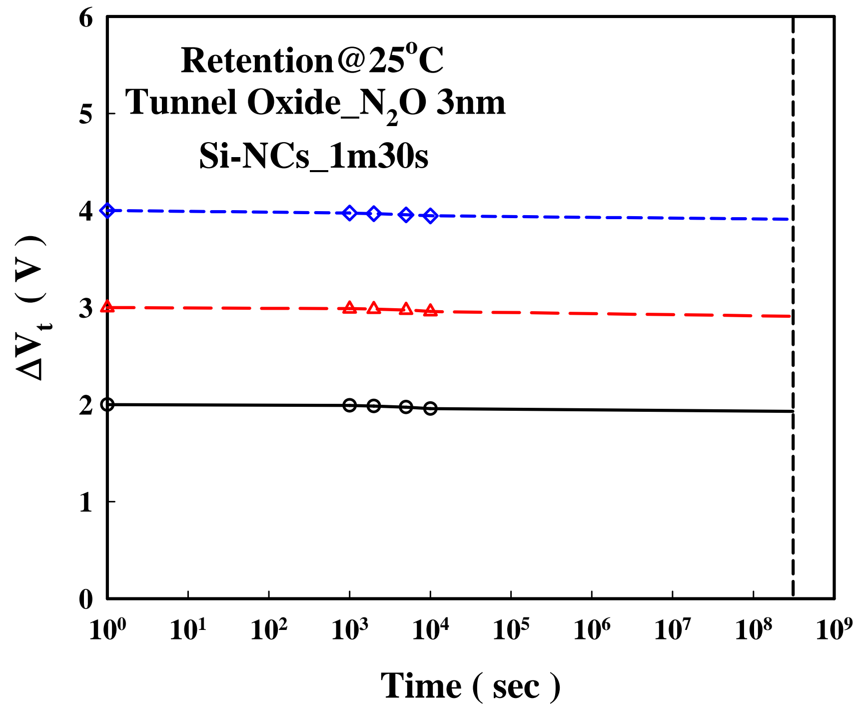
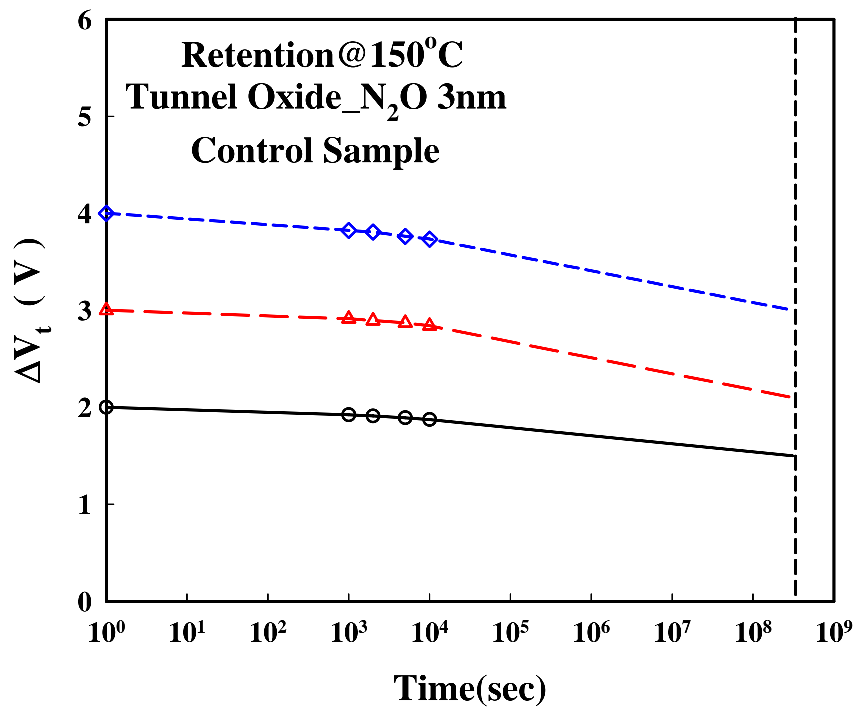
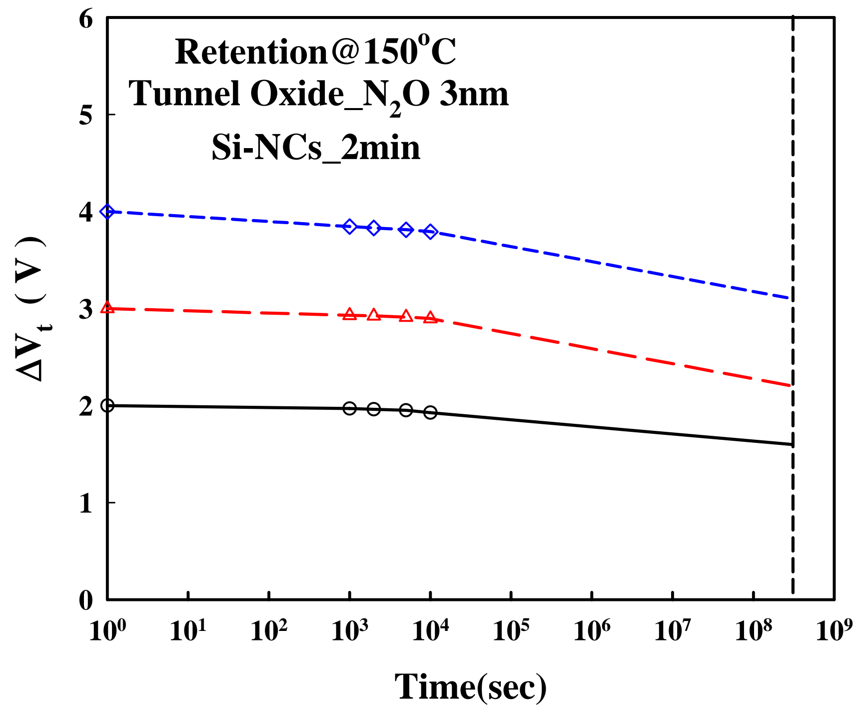


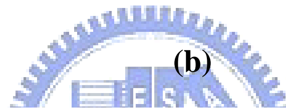

(c)

**Fig. 3-16** Data retention characteristic of high state and low state for dry $N_2O$ 3nm by horizontal-furnace at T=25℃. (a) control sample, (b) Si-NCs_2min sample and (c) Si-NCs_1m30s sample.

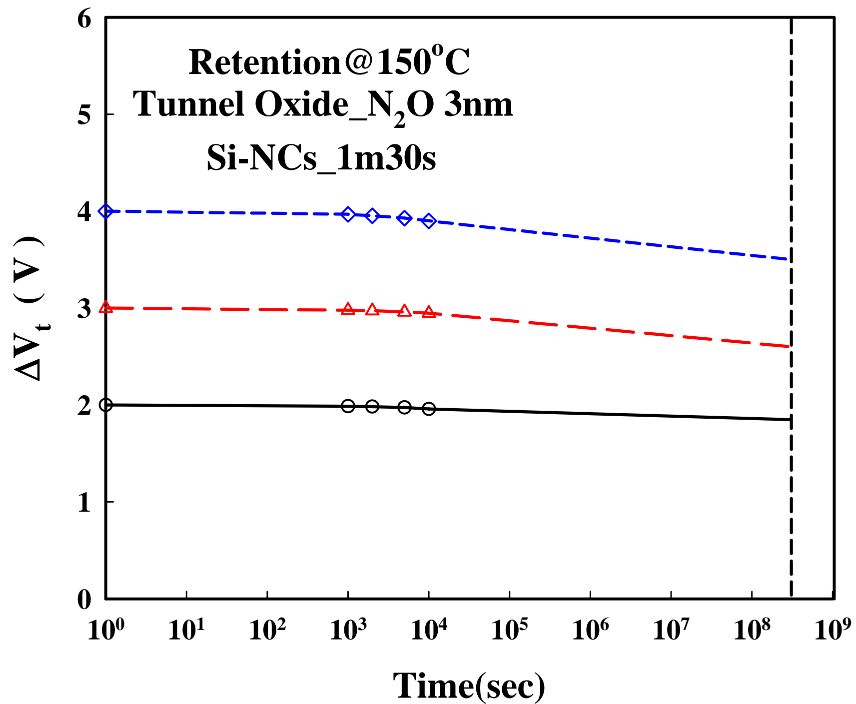



(a)



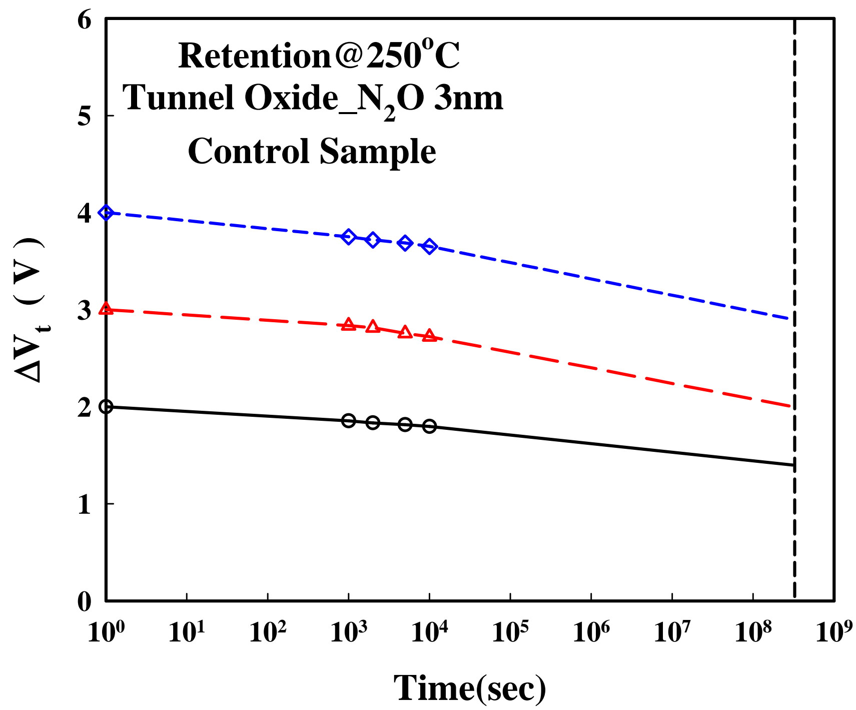



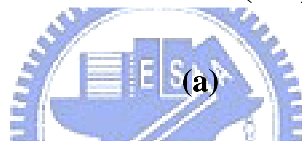
(b)




(c)

**Fig. 3-17** Data retention characteristic of high state and low state for dry $N_2O$ 3nm by horizontal-furnace at T=150℃. (a) control sample, (b) Si-NCs_2min sample and (c) Si-NCs_1m30s sample.



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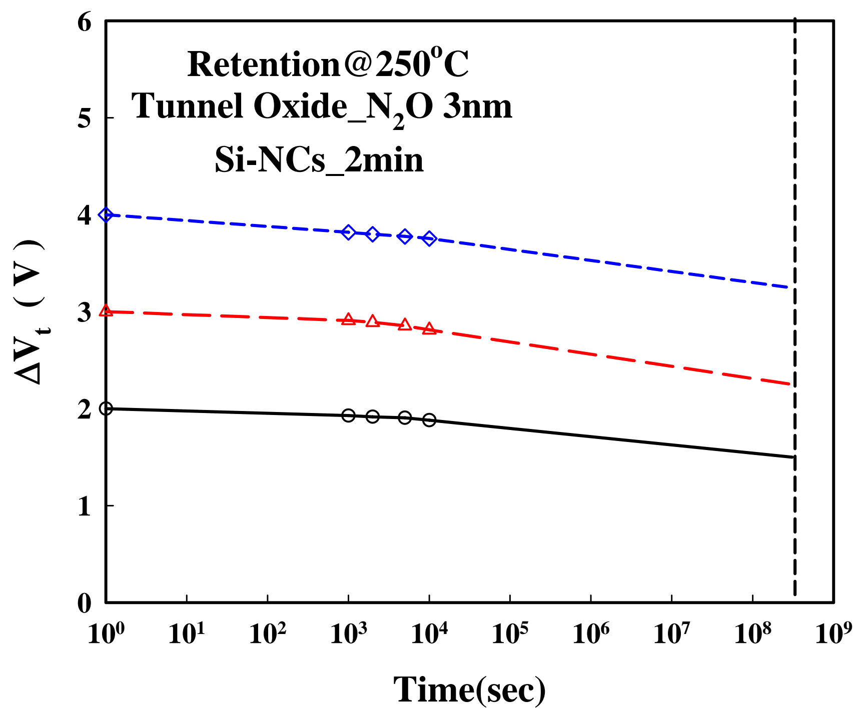


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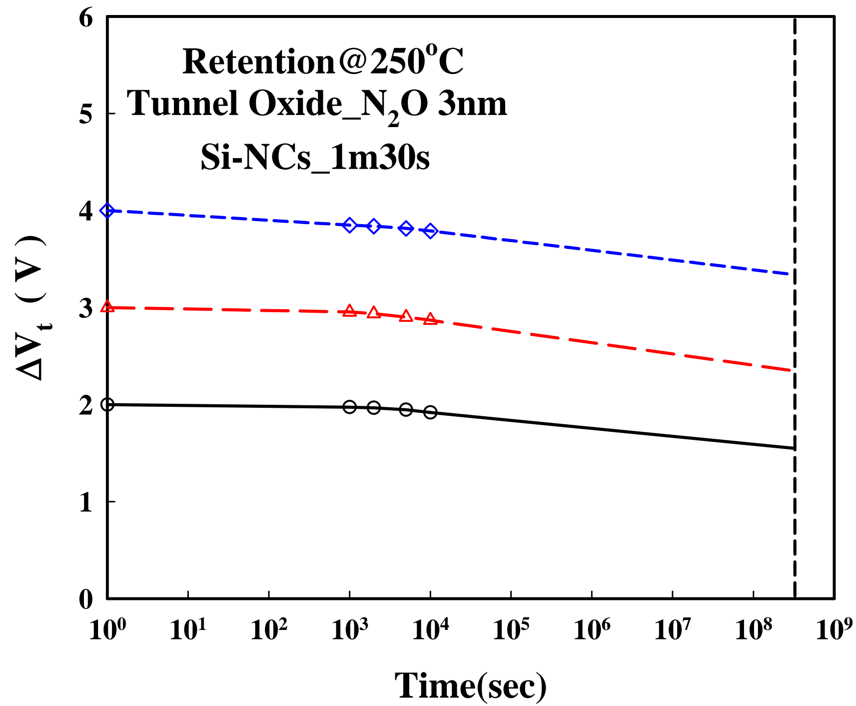


(c)

**Fig. 3-18** Data retention characteristic of high state and low state for dry $N_2O$ 3nm by horizontal-furnace at T=250℃. (a) control sample, (b) Si-NCs_2min sample and (c) Si-NCs_1m30s sample.

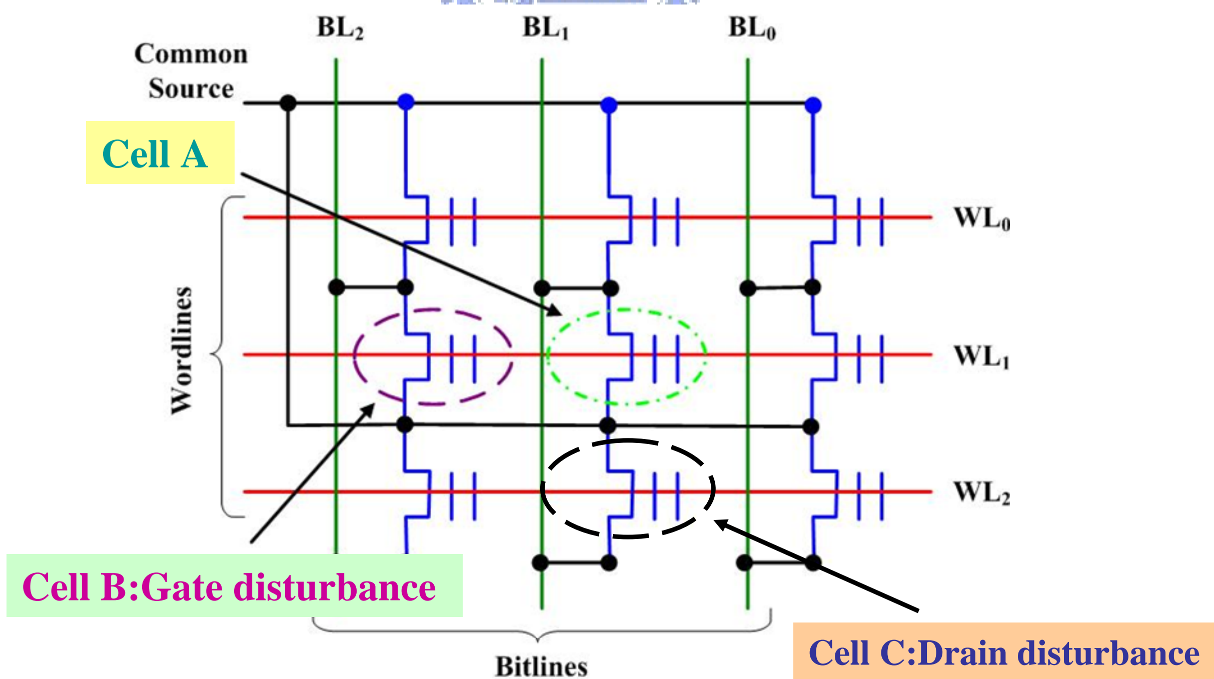


**Fig. 3-19** During Cell A is programmed, the gate disturbance takes place in Cell B and the drain disturbance takes place in Cell C.

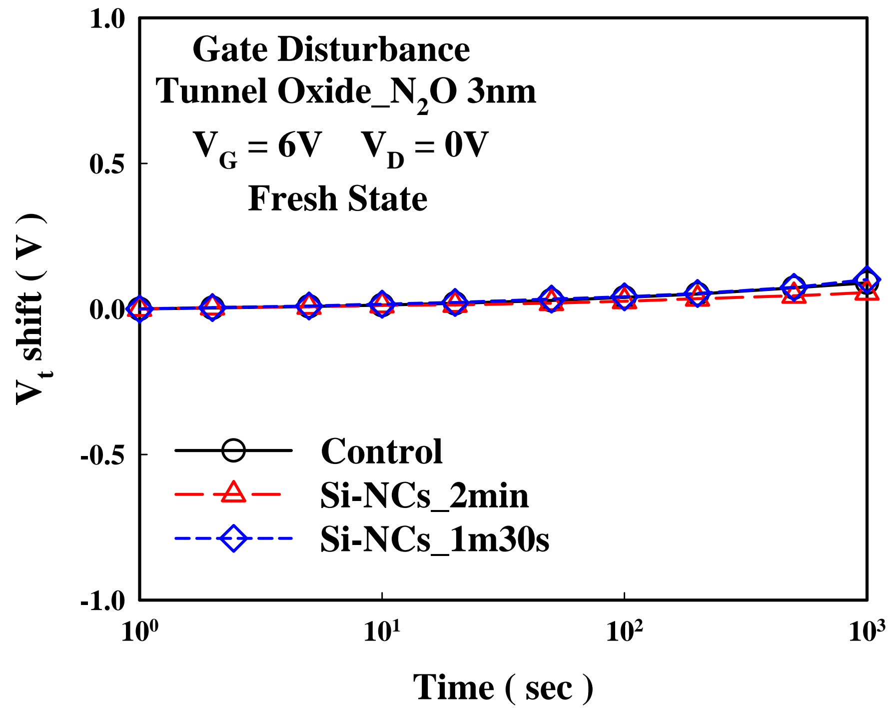


**Fig. 3-20** Programming gate disturbance characteristic of different sample at $V_G$=6V. This gate length and width are 0.4µm and 10µm. The tunnel oxide is dry $O_2$ 2.5nm by vertical-furnace. The Vt shift of gate disturbance is lower than 0.1V for 1000s stress with $V_G$=6V.

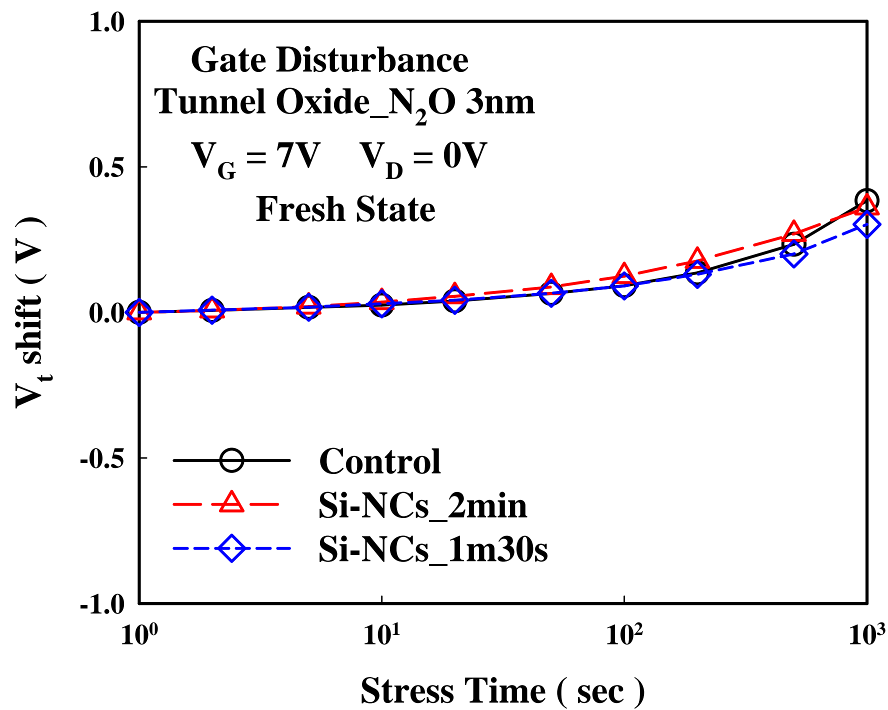


**Fig. 3-21** Programming gate disturbance characteristic of different sample at $V_G$=7V. This gate length and width are 0.4µm and 10µm. The tunnel oxide is dry $O_2$ 2.5nm by vertical-furnace. The Vt shift of gate disturbance is lower than 0.4V for 1000s stress with $V_G$=7V.

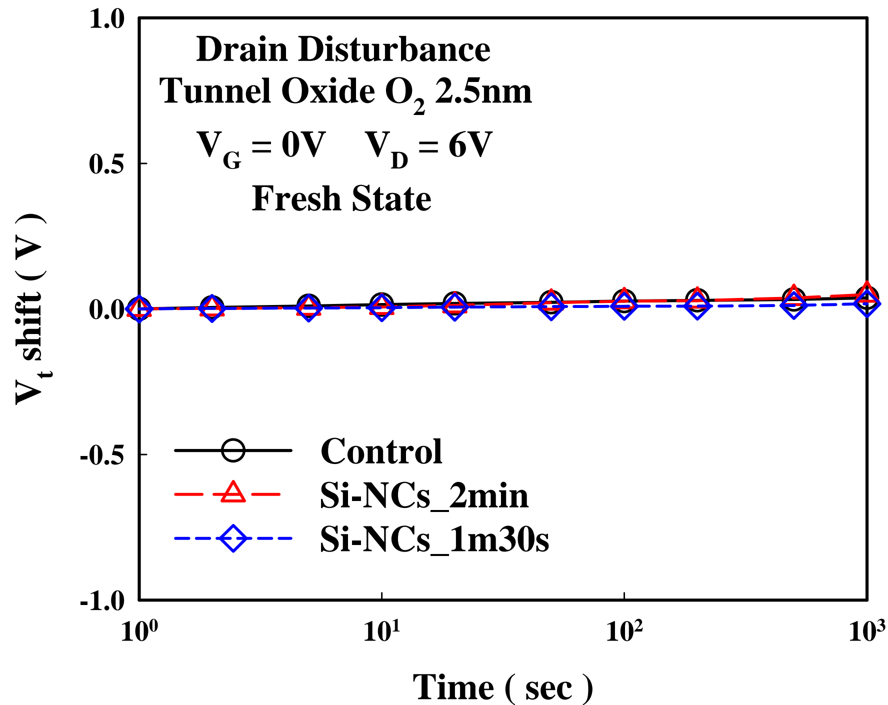


**Fig. 3-22** Drain disturbance characteristic of different sample at $V_D$=6V. This gate length and width are 0.4μm and 10μm. The tunnel oxide is dry $O_2$ 2.5nm by vertical-furnace. The Vt shift of drain disturbance is lower than 0.04V at the worse condition of 1000sec stress.

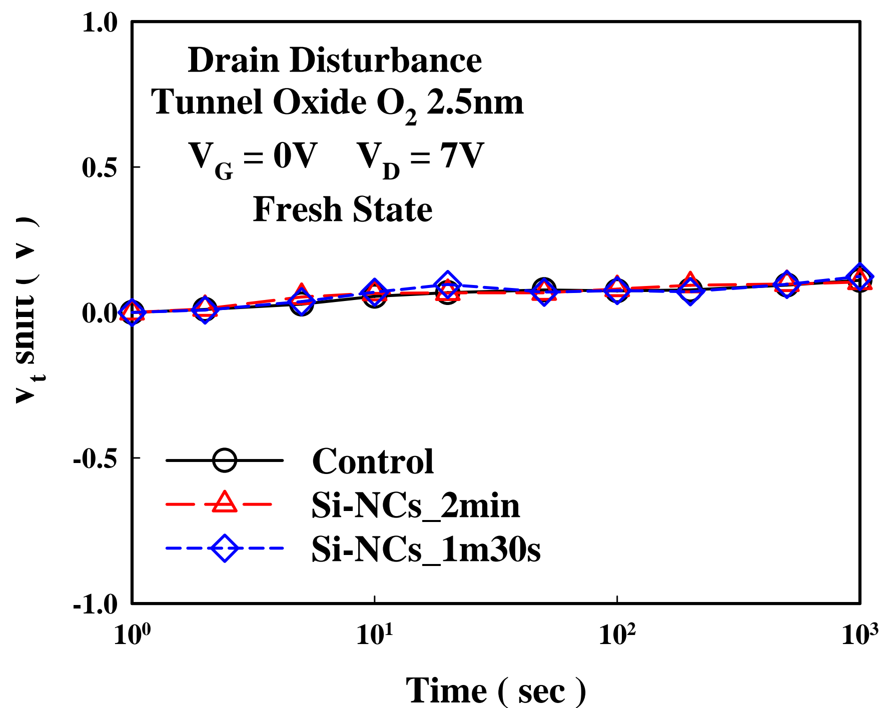


**Fig. 3-23** Drain disturbance characteristic of different sample at $V_D$=7V. This gate length and width are 0.4μm and 10μm. The tunnel oxide is dry $O_2$ 2.5nm by vertical-furnace. The Vt shift of drain disturbance is lower than 0.1V at the worse condition of 1000sec stress.

# *Chapter 4*

# *Conclusions*

In this thesis, we have studied embedded Si-NCs in $Si_3N_4$ of SONOS memories device application. We have successfully demonstrated the feasibility of fabricating embedded Si-NCs in $Si_3N_4$ of SONOS memories with excellent characteristics. The size of Si-NCs can be easily controlled by deposition time.

For the program window, Si-NCs SONOS memories has more trapping sites than conventional SONOS memory. The program window of Si-NCs is larger for control sample. And the larger Si-NCs size has larger trapping sites size similar to floating gate, so the memory window of Si-NCs_2min is larger than Si-NCs_1m30s memory window. For the different tunnel oxide film, dry $N_2O$ 2.5-nm by vertical-furnace and dry $O_2$ 2.5-nm by vertical-furnace of memory have thinner thickness than dry $N_2O$ 3-nm by horizontal-furnace of memory. The program window of thinner tunneling oxide is larger for tunneling oxide of dry $N_2O$ 3-nm by horizontal-furnace.

For the data retention, thermionic emission, direct tunneling and trap-to-trap tunneling, in relating to the data loss, are the three dominant leakage components. The reduction of the programmed flat band voltage is due to trap generation in the oxide and also interface state generation between tunnel oxide and channel interface, which are usually called electron degradations. In our device, the Si-NCs memory window still maintains quite about 2-V even through stressed for $10^4$ seconds.

At temperature T=25$^{o}$C, T=85$^{o}$C and T=150$^{o}$C, all cases presented good retention characteristics but charge loss is serious for control sample than Si-NCs of capacitor sample at high temperature. Program windows can maintain 1.9-V at 25℃. We can find that will make our data retention drop at high temperature. Due to thermionic tunneling is violent at high temperature. So program window has been reduced to 1.5-V. This also shows that the

trapping capability of Si-NCs trapping layer is very excellent. On the other hand, we observed larger charge loss percentage for ten years when using accelerated test at temperature T=250$^{o}$C. This charge loss is due to the poor quality of tunnel oxide which results in many leakage current paths.

For different tunnel oxides, all cases presented good retention characteristics but charge loss is serious for tunnel oxide by dry $O_2$ 2.5-nm than $N_2O$ 2.5-nm and 3-nm sample. This also shows that the quality of tunnel oxide of 3-nm grown by dry $N_2O$ is very excellent. On the other hand, we observed larger charge loss percentage for ten years when using accelerated test for tunnel oxide of 2.5-nm grown in dry $O_2$ sample. Based on the all above result, we know the quality of dry $N_2O$ 3-nm by horizontal-furnace is better than that of dry $O_2$ 2.5-nm by vertical-furnace. We find tunnel oxide that utilizing dry $N_2O$ 3-nm by horizontal-furnace will be performance of reliability. Because the thickness that horizontal-furnace grows is thicker. And the quality that horizontal-furnace grows is better.

In conclusion, according to our research we have demonstrated that embedded Si-NCs in nitride for SONOS memories have faster program and erase speed, lower operation voltage for scaled device, and multi-level per one memory cell. If we can improve the quality of blocking oxide in order to promote the erase speed and reliability, we believed this embedded Si-NCs in nitride for SONOS memories are very promising for the future flash memory application.

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論文題目：

**氮化矽層內嵌奈米矽晶體之 SONOS 型記憶體**

**Embedded Si-NCs in $Si_3N_4$ for SONOS Memories**

指導教授：趙 天 生 博士