不同高介電常數與傳統低溫介電層應用於低溫

複晶矽薄膜電晶體之比較

學生: 呂宜憲 指導教授: 趙 天 生 博士

簡 昭 欣 博士

國立交通大學



本論文中,擁有高效能P型通道薄膜電晶體以不同的高介電係數 介電層材料(包括二氧化铪(HfO₂)、鉿矽酸鹽(Hf-silicate)被提出, 以金屬-有機汽相沉積的高介電係數介電層與傳統二氧化矽 (TEOS-Oxide)介電層在低溫環境中被製作出來,以相同物理厚度比較 作為我們的主軸,並且研究其效應與可靠度。我們發現高介電常數在 電性的表現上有著普遍性的增長:包括了較低的臨界電壓、較好的次 臨界特性、較高的驅動電流;最主要原因在於高介電常數介電層有較 高的電容密度,使得多晶矽結晶邊界的載子缺陷能快速被填滿,因而多 晶矽電晶體存在的暫態時間較為縮短。然而二氧化鉿介電層的場效遷 移率卻是較低的,並且在關閉狀態下的漏電流增加較快,原因在於其 跟複晶矽通道間的介面特性較為曲折,以及由於高介電常數所造成的 在汲極端有較大的電場有關。

不同介電層的複晶矽薄膜電晶體,在不同溫度的加壓測試下都會 隨著測試時間的改變而裂化,其中鉿矽酸鹽在目前的測試中展現了較 佳的可靠度,主要在於其有較高的結晶溫度、較好的薄膜品質與較少 的介面狀態密度。



Comparison of Low Temperature Thin Film Transistor with Different High-k Dielectric Layers and Conventional TEOS Silicon Dioxide Layers

Student: Yi-Hsien Lu

Advisor: Dr. Tien-Sheng Chao Dr. Chao-Hsin Chien



In thesis, high-performance p-channel poly-Si thin-film transisitors (TFTs) are demonstrated using the different high-k dielectric with hafnium dioxide (HfO₂), hafnium silicate (HfSiO_x) layer are demonstrated by metal-organic chemical vapor deposition system with low-temperature processing. We compare with tetra-ethyl-oxy-silicate silicon dioxide (TEOS-SiO₂) layer with the same physics thickness for

our main shaft. Furthermore, the effect and reliability are also studied. It is found both the electric characteristic of high-k dielectric TFTs that improve obviously: including the lower threshold voltage, the better subthreshold swing, the higher on current. The main reason is imputed to the high capacitance density of high-k dielectric layers such that the grain boundary traps of poly-Si could be full faster and decrease the transition time exist in the poly-Si TFTs. However, the field effective mobility of HfO₂ dielectric TFTs is lower due to the roughness interface between HfO₂ layer and poly-Si channel and larger leakage current in the off state due to the high field near drain.

Devices characteristics of different dielectric layers degrade with stress time and stress conditions. We found the HfSiO dielectrics TFTs have the better reliability due to it has the better interface ,higher crystalline temperature and lower density of states.

誌謝

在踏上另一段人生旅程之前,僅一此論文感謝這兩年來一起成長、切磋 砥礪的各位。

感謝我的指導教授<u>趙天生</u>老師,由於老師的接納讓我有機會進入半導體的領 域從事相關的研究。並且在學術上或學術外皆樹立了好的模範,適時的給予建議 更是讓人獲益良多。<u>簡昭欣</u>老師總不吝嗇的給予學術上的建議與指導,感謝他兩 年來的殷勤教誨,讓我對於學術上與自我要求的態度有另一番新的體認與期許。 <u>楊明瑞</u>學長則在製程與數據分析上給予很多的協助,並感謝他總是耐著性子與我 們一起分析問題所在,他的好個性與積極的態度將一直是我學習的榜樣。

再者,感謝<u>馬鳴汶</u>學長在實驗技巧的傳授與指導,讓我省卻的許多摸索的時間;<u>吳偉成</u>學長管理實驗室的用心與風範、<u>郭柏儀</u>學長在量測時的協助以及<u>林育</u> 賢學長、陳建豪學長、羅文政學長、<u>楊紹明</u>學長、<u>陳世璋</u>學長、<u>鄭兆欽</u>學長、<u>摩</u> <u>耀仁</u>學長,各位學長的指導與寶貴的經驗皆令我獲益良多。

特別的是,感謝一路陪伴的實驗室夥伴:妍心、國興、德馨、宗諭、峻丞、 競之、治國、豐綺以及家豪、久騰、明宏、美君;畢業的學長姐:竣祥、彦學、 武欽、佩珊、棟煥以及學弟們,那些一起舌槍論戰的日子讓這兩年增色不少。

最後,感謝一路支持與鼓勵我的父親<u>呂水壬</u>先生、<u>郭環里</u>女士以及妹妹蕙 宇,讓我在求學過程能無後顧之憂;在此,再一次感謝所有幫助過我的人,

我將永遠感懷在心,謝謝。

Contents

摘要 (中文)	I
Abstract(English)	
誌謝	V
Table & Figure Captions	VIII

Contents

Chaprer1 Introduction1
1.1 Overview of Poly-Si Thin-Film Transistor1
1.2 Motivation
1.2.1 The thin oxide issue
1.2.2 Why do we use high-k dielectric ?4
1.3 Thesis Organization
Chaprer2 Experiment Method
2.1 Fabrication Process
2.2 Device Electrical Parameters Extraction7
2.2.1 Threshold Voltage7
2.2.2 Mobility
2.2.3 Sub-threshold Swing
2.3 Result and Discussion
2.3.1 Electrical Properties
2.3.2 Off-State Leakage Current Mechanism
Chaprer3 Reliability of the p-Channel with TEOS and High-k TFTs32
3.1 Introduction
3.1.1 Threshold Voltage Shift
3.1.2 Transconductance and Drive Current Degradation
3.2 Experimental Procedures

3.3 Result and Discussion	34
3.3.1 Negative Gate Bias Stress Instability	34
3.3.2 Negative Bias Temperature Instability	
Chaprer4 Conclusion and Summary	65
4.1 Conclusion	65
4.1.1 Electrical Properties	65
4.2 Reliability	66
Reference:	67



Table Caption

Table 2-1 Summary of V_{TH} , S.S. and ON/OFF current ratio characteristics of High-k TFTs and	
conventional TFTs with W/L=2µm/2µm2	5
Table 2-2 The crystallization structure of HfO2 dielectric film depicts the additional coulomb	
scattering that result in the mobility degradation2	6
Table 2-3 The trap-assisted-tunneling (TAT) enhance gate-induced-leakage-current (GIDL) at	
lower gate bias2	7
Table 2-4 The Frenkel-Poole emission illustration2	8
Table 3-1 The measurement setup illustration. 2	8



Figure Captions

Figure 2-1 Device Fabrication Process Flow
Figure 2-2 The cross-sectional transmission electron microscopy (TEM) images of the HfO ₂ ,
HfSiO _x and deposited-SiO ₂ films with a physical thickness of 57, 53, and 61 nm, respectively.
Eigner 2.2 The interfacial layor between HfCiOr and Paly Si shannel with a physical thickness of
20 mm
2.9 mm
Figure 2-4 The x-ray diffraction spectroscopy (XRD) of HO_2 and $HISIO_X$ films, respectively. 22
Figure 2-5 Capacitance capability of high-k dielectric and TEOS oxide
Figure 2-6 Breakdown field of high-k dielectric and TEOS oxide, HfSiO _x has smaller leakage
current and larger breakdown field than HfO ₂ 23
Figure 2-7 Transfer characteristics of TFTs with conventional TEOS and TFTs with HfO ₂
comparison at gate dimension with W/L=2µm/2µm24
Figure 2-8 Transfer characteristics of TFTs with conventional TEOS and TFTs with $\mathrm{HfSiO}_{\mathrm{X}}$
comparison at gate dimension with W/L=2µm/2µm24
Figure 2-9 Transfer characteristics of TFTs with HfO2 and TFTs with HfSiOx comparison at gate
dimension with W/L=2µm/2µm
Figure 2-10 Density of states extracted from transfer characteristics (V _{ds} = -0.1V) of poly-Si TFTs
using different gate dielectrics
Figure 2-11 Activation energy of channel obtained from temperature dependence of transfer
characteristics (V _{ds} = -0.1V) using different gate dielectrics
Figure 2-12 Threshold voltage roll-off of different dielectrics comparison, from W/L=10µm/10µm
scale down to W/L=1µm/1µm
Figure 2-13 Subthreshold swing characteristics of different dielectrics comparison, from
$W/L=10\mu m/10\mu m$ scale down to $W/L=1\mu m/1\mu m$
Figure 2-14 On/Off ratio characteristics of different dielectrics comparison, from
$W/I = 10 \mu m/10 \mu m scale down to W/I = 1 \mu m/1 \mu m 30$
Figure 2.15 On current and off current characteristics of different dielectrics comparison from
Figure 2-15 On current and on current characteristics of unrefent detectrics comparison, from $W/I = 10 \text{ mm}/10 \text{ mm}$ 20
Figure 2.16 Mahility shows the visiting comparison of different dislocating comparison from
Figure 2-16 Mobility characteristics comparison of different dielectrics comparison, from
$W/L=10\mu m/10\mu m$ scale down to $W/L=1\mu m/1\mu m$
Figure 3-1 The transfer characteristics of the LTPS TF is under NB11 stress with different stress
time, respectively
Figure 3-2 The transfer characteristics of the LTPS TFTs under NBI stress with initial state and
10000sec., respectively
Figure 3-3 Mobility degradation with different stress time
Figure 3-4 The transfer characteristics of the LTPS TFTs under NBTI stress with different stress

time, respectively. The stress was performed at 75°C40
Figure 3-5 The transfer characteristics of the LTPS TFTs under NBTI stress with initial state and
10000sec., respectively. The stress was performed at 75°C41
Figure 3-6 Mobility degradation with different stress time. The stress was performed at 75°C41
Figure 3-7 The transfer characteristics of the LTPS TFTs under NBTI stress with different stress
time, respectively. The stress was performed at 100°C42
Figure 3-8 The transfer characteristics of the LTPS TFTs under NBTI stress with initial state and
10000sec., respectively. The stress was performed at 100°C43
Figure 3-9 Mobility degradation with different stress time. The stress was performed at 100°C43
Figure 3-10 The transfer characteristics of the LTPS TFTs under NBTI stress with different
stress time, respectively44
Figure 3-11 The transfer characteristics of the LTPS TFTs under NBI stress with initial state and
10000sec., respectively45
Figure 3-12 Mobility degradation with different stress time
Figure 3-13 The transfer characteristics of the LTPS TFTs under NBTI stress with different
stress time, respectively. The stress was performed at 75°C46
Figure 3-14 The transfer characteristics of the LTPS TFTs under NBTI stress with initial state
and 10000sec., respectively. The stress was performed at 75°C47
Figure 3-15 Mobility degradation with different stress time. The stress was performed at 75°C47
Figure 3-16 The transfer characteristics of the LTPS TFTs under NBTI stress with different
stress time, respectively. The stress was performed at 100°C48
stress time, respectively. The stress was performed at 100°C
stress time, respectively. The stress was performed at 100°C
stress time, respectively. The stress was performed at 100°C
stress time, respectively. The stress was performed at 100°C
stress time, respectively. The stress was performed at 100°C
stress time, respectively. The stress was performed at 100°C
stress time, respectively. The stress was performed at 100°C
stress time, respectively. The stress was performed at 100°C
stress time, respectively. The stress was performed at 100°C
stress time, respectively. The stress was performed at 100°C
stress time, respectively. The stress was performed at 100°C
stress time, respectively. The stress was performed at 100°C
stress time, respectively. The stress was performed at 100°C
stress time, respectively. The stress was performed at 100°C
stress time, respectively. The stress was performed at 100°C
stress time, respectively. The stress was performed at 100°C

and 10000sec., respectively. The stress was performed at 100°C54 Figure 3-27 Mobility degradation with different stress time. The stress was performed at 100°C Figure 3-29 Dependence of the threshold-voltage shift on the stress time at 75°C......56 Figure 3-30 Dependence of the threshold-voltage shift on the stress time at 100°C......57 Figure 3-31 Dependence of the field-effective mobility degradation on the stress time at 25°C....58 Figure 3-32 Dependence of the field-effective mobility degradation on the stress time at 75°C....58 Figure 3-33Dependence of the field-effective mobility degradation on the stress time at 100°C...59 Figure 3-35 Dependence of the off current degradation on the stress time at 75°C......60 Figure 3-37 Dependence of the on current degradation on the stress time at 75°C......61 Figure 3-42 Dependence of the current ratio degradation on the stress time at 100°C64

