Chaprer1 Introduction

1.1 Overview of Poly-Si Thin-Film Transistor

The first report of TFTs, by Weimer, appeared in 1961[1][2]. TFTs have a history almost as long as that of metal-oxide-semiconductor field-effect transistors (MOSFETs). In the early 1980s, strong interest in TFTs revived due to new major application that include active-matrix addressed flat-panel displays[3] and static random-access memories (SRAMs)[4]. Various semiconductor materials have been studied for use in TFTs including: CdS, CdSb, PbTe, Se, Ge, SiC, C(diamond), SiGe, and Si. Amorphous Si thin films and polycrystalline silicon thin films are only two types of TFTs that use Si for active region.

It is known that the pixel switching device of AMLCDs rely on α-Si:H TFTs. The advantages of α-Si:H TFTs are their compatibility with low processing temperature on large-area glass substrates and high off-stated impedance which result in low leakage current. However, it is hard to realize the integration of the switching pixels with the peripheral driver circuits in one signal substrate to further reduce the production cost of AMLCDs due to their low electron mobility ($\leq$1 cm^2/Vs). Recently, poly-Si TFTs have attracted much attention, because the field effect mobility in poly-Si is significantly higher than that in α-Si, thus higher driving current

can be achieved in poly-Si[5]. The high driving current of poly-Si TFTs makes the integration of switching pixels and driver circuits possible. Furthermore, the aperture ratio and the panel brightness can be also greatly promoted due to small device size needed using poly-Si TFTs. So, the performance of display can be significantly improved. As a result, poly-Si TFTs have a great potential to realize high performance large area AMLCDs applications, and further to accomplish System-on-Panel (SOP).

But it is important to note that traps states of carries at the poly-Si grain boundary cause the degradation of TFTs performance. For example, in the off states, the boundary traps assist the carrier generation in the depletion layer that have larger leakage current compared with α-Si:H TFTs, therefore how to obtain a good quality polycrystalline Si film with higher carrier mobility, lower threshold voltage, lower leakage current at high operate voltage with excellent reliability has become a major concern for the poly-Si thin film transistors fabrication. According the reports, several methods have been proposed to improve the device performance by enlarging the grain size of poly-Si films[6] and reducing the trap states in grain boundaries, i.e. high quality poly-Si films . It has been reported that the α-Si films can be crystallized by several techniques, such as solid phase crystallization (SPC)[7], laser annealing crystallization[8] , metal induced crystallization (MIC)[9], and metal-induced lateral crystallization (MILC)[10] to obtain a large grain size of poly-Si to improve the field

effect mobility. In the other hands, there are other methods such as H_2, NH_3, N_2O and O_2 plasmas[11]-[14] plasma treatments to passivate the defects in the channel or narrowing the channel width to reduce the trap state density have been intensely investigated to accomplish this goal.

Finally, novel structure design is another approach to fabricate high-performance poly-Si TFTs. This technique focuses on the reduction of the electric field near the drain junction, and thus suppresses the device's off-state leakage current. Many structures including multiple channel structures[15], offset drain/source[16,17], lightly doped drain (LDD)[18], gate-overlapped LDD[19], field induced drain[20] and vertical channel[21] have been proposed and investigated intensively[22].

1.2 Motivation

1.2.1 The thin oxide issue

The most stable and useful dielectrics for semiconductor devices are silicon dioxide and silicon nitride，which have been successfully used in ULSI for over forty years. In the first transistor, the thickness of the SiO_2 gate oxide was a few hundred nanometers. Until very recently, the gate dielectric scaling down trended torward of the physic limitation(~2nm for SiO_2) . It extend a number of fundamental problems such high leakage current、low oxide breakdown voltage and low mobility…etc[23].

For TFTs, the key parameters of the LTPS TFTs are：(1)High mobility, (2)Low threshold voltage, and (3) High driving current and Low leakage current at high operate voltage. These are for demand of that to realize system-on-panel (SOP) 、integrating driving ICs on the glass substrate and drive the liquid crystal. Using a thin dielectric can improve the driving current of TFTs. Similar to MOSFETs, however, the conventional gate dielectric(i.e. SiO_2 、Si_3N_4) for small dimension TFTs also need to decrease the thickness. Although thinning down the gate oxide can increase the drive current of TFTs, however, the quality of low-temperature silicon oxide is not good enough, it results in higher gate leakage current

1.2.2 Why do we use high-k dielectric ?

In order to preserve the physical dielectric thickness while increasing the gate capacitance, several new high-κ materials, including Al_2O_3, Ta_2O_5 were proposed [24]-[25]. Among them, Al_2O_3 TFTs improvement is not sufficient due to the k value is not high enough.On the other hand, the Ta_2O_5 TFTs induce higher gate leakage current due to its narrow band-gap.

In thesis, we fabricated the LTPS TFTs with two kind of High-k gate dielectric deposited by MOCVD (Metal) , including HfO_2 and $HfSiO_X$. Conventional TEOS gate dielectric for compare. Mainly, in addition to show the lower threshold voltage，we want to discuss the influence of the different plasma treatment time, and

reliability between high-k and TEOS dielectric for p-channel Poly-Si TFTs as well. Moreover, we hope to increase the driving current, decrease the threshold voltage of high-k device and have high gate capacitance capability compared with conventional devices. Therefore, we found the better high-k dielectric for LTPS TFTs that will show higher mobility, alleviated V_{th} roll-off, improved subthreshold swing, and increased ON/OFF current ratio for p-channel Poly-Si TFTs.

1.3 Thesis Organization

In chapter 1, the overview of Poly-Si TFTs, the brief introduction of High-k dielectric, and motivation in this thesis are described.

In chapter 2, experimental process flows, and for p-channel Poly-Si TFTs, we will show High-k dielectric have the smaller EOT with almost same physics thickness that to obtain the better performances of device. Moreover, the performances of LTPS-TFTs with hafnium oxide and hafnium-silicate dielectrc are compared with the conventional TFTs.

In chapter 3, the reliability of different dielectric layers will be comparison.

In chapter 4, at the end of this thesis, we will make conclusions.

Chaprer2 Experiment Method

2.1 Fabrication Process

In this first draft, poly-Si TFTs were fabricated on both 6-inch thermally oxidized (100) p-type silicon. First, the thermal oxide growth on silicon about 550nm to simulate the glass substrate. Then, a 100nm-thick amorphous silicon (α-Si) active region layer was deposited at 550^{o}C by the dissociation of SiH_4 gas in a low-pressure chemical vapor deposition (LPCVD) system, and then wafer receive a furnace-annealed at 600^{o}C for 24 hours in N_2 ambient (SPC) to recrystallize the α-Si films. After defined the active device islands region, a 50nm dielectric then further split to three materials, one is hafnium based dielectrics, ex. Hafnium oxide and Hafnium-silicate (HfO_2 and $HfSiO_x$) layers that was deposited by Metal-Organic Chemical Vapor Deposition (MOCVD), the other one is low temperature tetraethylorthosilicate silicon dioxide (TEOS-SiO_2) layer was deposited. Another 300nm-thick amorphous silicon film was deposited at 550^{o}C in a LPCVD system, and patterned to form the gate of the transistor. A self-aligned BF_2 ion implantation at 40 Kev with a dose of 5×10^{15} cm^{-2} was used to dope the drain, source, and gate simultaneously. Prior to the passivation layer deposited by PECVD system, dopant activation is to carry out by furnace 24h at 600^{o}C in N_2 ambient. After passivation layer, contact holes and Al pad contacts were finished. After

sintering at 300^{o}C, the process was completed.

2.2 Device Electrical Parameters Extraction

In this section, all the electrical characteristics of proposed poly-Si TFTs were measured by HP 4156B-Precision Semiconductor Parameter Analyzer. Moreover, the methods of parameter extraction used in this study are described. These parameters include threshold voltage (V_{TH}), field-effect mobility (μ_{FE}), subthreshold swing (S.S.), parasitic resistance (R_P), ON current (I_{ON}), OFF current (I_{OFF}), ON/OFF current ratio (I_{ON}/I_{OFF}).

2.2.1 Threshold Voltage

The threshold voltage V_{TH} is an important parameter required for the channel length-width and series resistance measurements. However, V_{TH} is not unique defined. Various definitions exist and the reason for this can be found in the I_D-V_G curves. One of the most common threshold voltage measurement technique is the linear extrapolation method with the drain current measured as a function of gate voltage at a low drain voltage of 50~100 mV typically to ensure operation in the linear MOSFET region .

However, in our p-channel TFTs, the threshold voltage is defined at a low drain voltage of -0.1V, and a fixed drain current $I_D=I_{DN}\times(W/L)$ where I_{DN} is a normalized

drain current. Here, I_{DN} is 10nA for p-channel.

2.2.2 Mobility

Usually, field effect mobility (μ_{FE}) is determined from the maximum value of transconductance (g_m) at low drain bias. The transfer characteristics of poly-Si TFTs are similar to those of conventional MOSFETs, so that the first order of I-V relation in the bulk Si MOSFETs can be applied to poly-Si TFTs. The drain current in linear region ($V_{DS} < V_{GS} - V_{TH}$) can be approximated as the following equation:

$$I_{DS} = \mu_{FE} C_{OX} (\frac{W}{L})[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^{2}] \quad \textbf{..... (Eq.2.1)}$$

where W is the channel width, L is the channel length, V_{TH} is the threshold voltage, C_{ox} is the gate oxide capacitance per unit area. Thus, g_m is given by

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \mu_{FE} C_{OX} (\frac{W}{L}) V_{DS} \quad \textbf{..... (Eq.2.2)}$$

Therefore, the field-effect mobility is

$$\mu_{FE} = \frac{L}{C_{OX} W V_{DS}} g_{m(\max)} \quad \text{..... (Eq.2.3)}$$

2.2.3 Sub-threshold Swing

The drain current in the saturation region ($V_{DS} > V_{GS} - V_{TH}$) is expressed as the following equation:

$$I_{DS} = \frac{1}{2}\mu_{FE} C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2 \quad \text{..... (Eq.2.4)}$$

It appears that the current abruptly vanishes while V_G is reduced to zero from the

equation. In reality, there is still some drain conduction current below threshold, and this is known as the subthreshold conduction. This current is due to the weak inversion in the channel between flat-band and threshold, which leads to a diffusion current from source to drain. The subthreshold swing (S.S.) is defined as the reciprocal of slope of the I_D-V_G curve in weak inversion region. It is the amount of gate voltage required to increase/ decrease drain current by one order of magnitude. It is a typical parameter to describe the control ability of gate toward channel.

In this thesis, the subthreshold swing is defined as one-third of the gate voltage required decreasing the threshold current by three orders of magnitude. The threshold current is specified to be the drain current when the gate voltage is equal to threshold voltage.

2.3 Result and Discussion

In this section, we will show electrical characteristics as well as discuss physical meaning for p-channel TFTs. At first, the transmission electron microscopy (TEM) photograph for cross-section of the HfO_2, $HfSiO_x$ and deposited-SiO_2 films with a physical thickness of 57, 53, and 61 nm is shown in Fig.2-2 to Fig.2-3, respectively.

After the low-temperature process(below 600^{o}C), we can observe that the different crystalline temperature of the $HfSiO_x$ and HfO_2. The $HfSiO_x$ film keeps amorphous structure, and the polycrystalline structure can be seen in HfO_2 film (Fig.2-2 (a)), which is conducive to a smoother surface at both the top and bottom interfaces. This

result is consistent with our x-ray diffraction spectroscopy (XRD) data in Fig.2-4.

2.3.1 Electrical Properties

Figure 2-5 show the capacitance density of the HfO_2, $HfSiO_x$ and deposited-SiO_2 films, according to the capacitance density and physics thickness extraction, we can know the dielectric constant of the HfO_2, $HfSiO_x$ and deposited-SiO_2 films are about 15, 8 and 5, respectively. On the other hand, we measure the breakdown field that show in Figure 2-6, the result exhibit the leakage of the $HfSiO_x$ is smallest and the breakdown field of the $HfSiO_x$ film is increase of 3MV/cm than the HfO_2 film.

Fig.2-7 to Fig.2-9 show the I_D-V_G transfer characteristics shows transfer characteristics of TFTs with high-k dielectric and SiO_2 at V_{ds} = -0.1 and -2 V at gate width and length are both equal to 2μm. Obviously, TFTs with $HfSiO_X$ have better subthreshold swing, and higher ON/OFF current ratio in Figure 2-7. Particularly, off-state leakage current of $HfSiO_X$ at the low V_{DS} (=-0.1V) is like to TEOS TFTs, but off-state leakage current increase more rapidly at the high V_{DS}(=-2V) operate show in Fig.2-7. The explanation of the off-state leakage current will discuss in section 2.3.2.

The much better performance of TFTs with $HfSiO_X$ due to the better gate dielectrics/poly-Si interface quality[24], and the lower V_{TH} and significant improved S.S. could be explained that the thinner equivalent oxide thickness (EOT) with the

same physical thickness[25,26]. As discuss the further reason, the V_{TH} and S.S. factor sensitive to the density of deep states near the mid-gap has been report through the literature[27], Figure 2-10 shows the plots of density of states versus $E-E_{fb}$ of poly-Si TFTs with different gate dielectrics, we can observe that the density of states values of high-k dielectrics was lower than TEOS dielectric.

In Figure 2-8, obviously, TFTs with HfO_2 also depict much better performance than TFTs with conventional deposited-SiO_2 except for the OFF-state leakage current, additionally, we can observe the off-state leakage at the low V_{DS} (=-0.1V) of HfO_2 raise faster more than that of $HfSiO_x$ in Figure2-9. The extracted values of V_{TH}, field effective mobility, S.S., and ON/OFF current ratio will be shown in Table 3-1.

In Figure 2-9 to Figure 2-13, we compare the parameters of different dielectrics with different dimension (form W/L=10μm/10μm to W/L=1μm/1μm**).**

In the Figure 2-9, we can observe the V_{TH} of high-k dielectric TFTs are more stable than TEOS TFTs, this is due to the high capacitance density and lower density of states with high-k dielectrics such that TFTs transient time is shorter than TEOS TFTs. Additionally, for poly-Si TFTs, the threshold-voltage roll-off is dominated by the decreasing of number of grain boundary as the devices scale down. The grain boundary fill of charge is faster due to high capacitance density of high-k dielectrics, so the effect of grain boundary is less than TEOS TFTs.

In the Figure 2-11, we can observe the on/off ratio of TEOS and High-k dielectric TFTs both raise as the devices scale down. This phenomenon is explained by the grain boundary in the channel and grain boundary trap is less than large dimension. So on current increase and off current decrease in Figure 2-12

In the Fig.2-13, we could observe the mobility increase as device dimension decrease. However, the mobility of $HfSiO_X$ and TEOS at W/L=1μm/1μm is decrease, The reason mat be due to the S/D overlap such that effective length decrease and lateral field decrease.

Even though the S.S. of TFTs with $HfSiO_x$ are slightly worse than those of TFTs with HfO_2, we still believe that $HfSiO_x$ is still more suitable than HfO_2 for the gate dielectric of future poly-Si TFTs. The reasons are as follows: First, $HfSiO_x$ has smaller leakage current and larger breakdown field than HfO_2 due to the amorphous nature of $HfSiO_x$ after processing. Second, TFTs with $HfSiO_x$ show 2.4 times improvement in hole mobility over the conventional TFTs using deposited-SiO_2 dielectric, rather than degraded for the case of TFTs with HfO_2. According to the previous reports[28], we speculated that the degraded mobility of TFTs with HfO_2 dielectric was due to the additional Coulomb scattering caused by the plentiful charges exsited in the HfO_2 dielectric.

2.3.2 Off-State Leakage Current Mechanism

In order to further clarify the mechanism of OFF-state leakage current, at first, we calculated the dependence of activation energies on V_{GS} with V_{DS}=-0.1V of the three dielectric that we used in Figure 2-11. We can observe that the minimum leakage current of TFTs with HfO_2 due to the highest activation energy. But as increasing the $|V_{gs}|$ to across the highest point into OFF-state regime, the activation energy of TFTs with HfO_2 decrease fastest causes the OFF-state causes current to increase rapidly. Furthermore, the trap-assisted-tunneling (TAT) will enhance the GIDL phenomenon that cause the OFF-state leakage current more serious[29]. On the other hand, according to the leakage mechanism of poly-Si TFTs in previously literature [30]-[33], the Frenkel-Poole emission is dependent on the peak electric field (Epk) at the drain junction and dominated by the vertical field at the interface that expressed as follows:

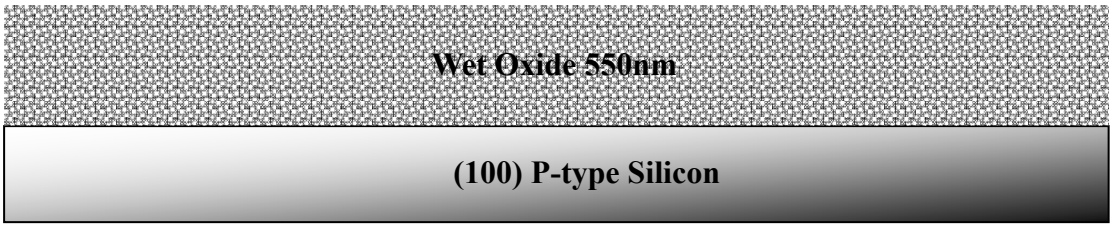
$$I_{FE} \propto \exp\left(\sqrt{E_{pk}}\right)$$

$$E_{pk} = \frac{(V_{gs} - V_{ds} - V_{fb})\varepsilon_{\text{gate dielectric}}}{(T_{\text{gate dielectric}}\varepsilon_{Si})},$$

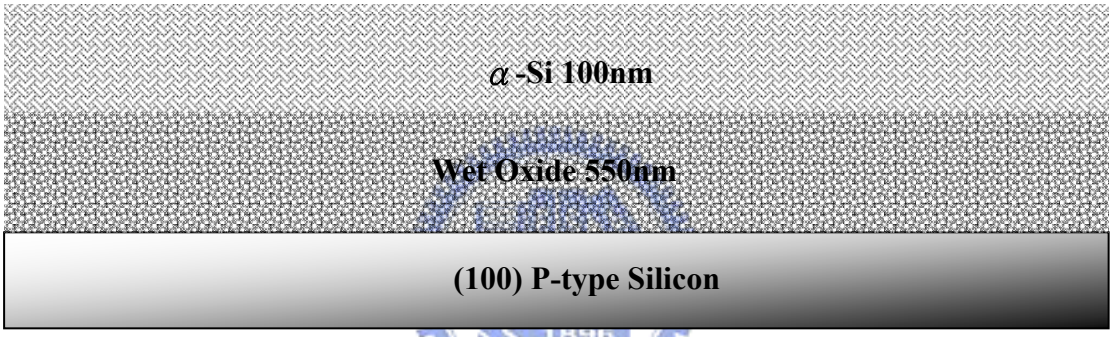
where the εSi and the εgate dielectric are the permittivities of Si and gate dielectric, respectively, V_{fb} is the flatband voltage, and $T_{\text{gate dielectric}}$ is the physical thickness of the gate dielectric. Poly-Si TFTs using high dielectric constant gate dielectric will exhibit higher peak electric filed, causing a rapidly increasing OFF-state current. The

Frenkel-Poole emission illustration is show at Table 2-4.

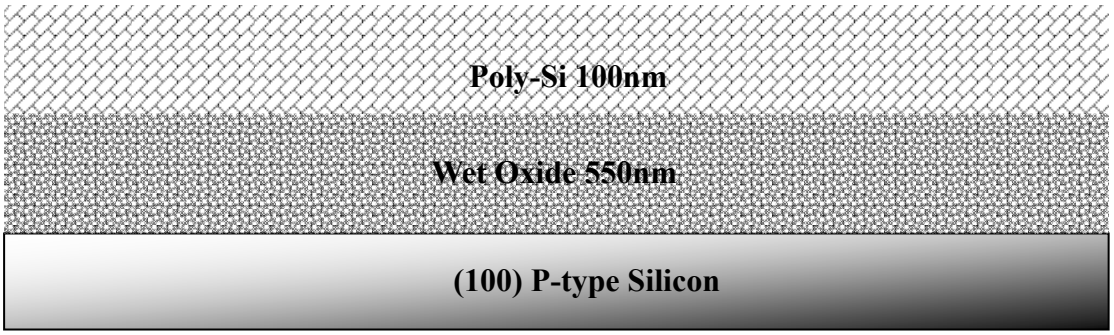
Figure 2-1 Device Fabrication Process Flow



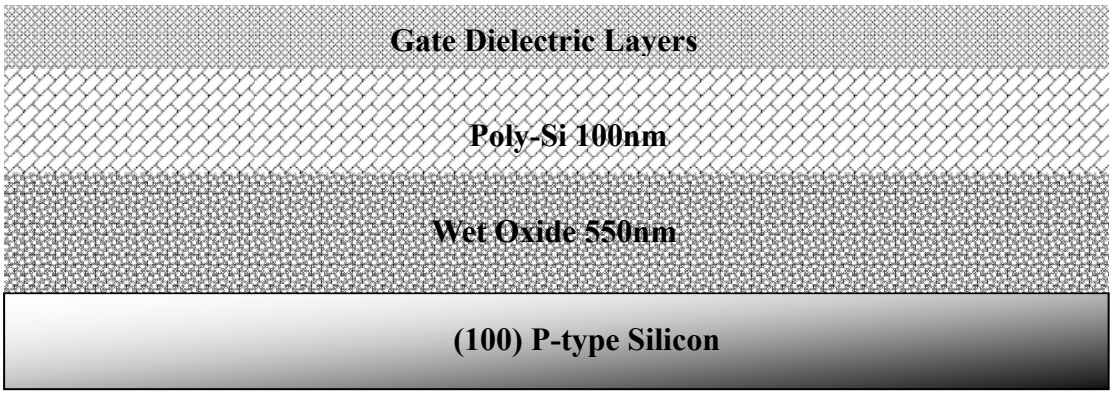
First, the thermal oxide growth on silicon about 550nm to simulate the Glass substrate.



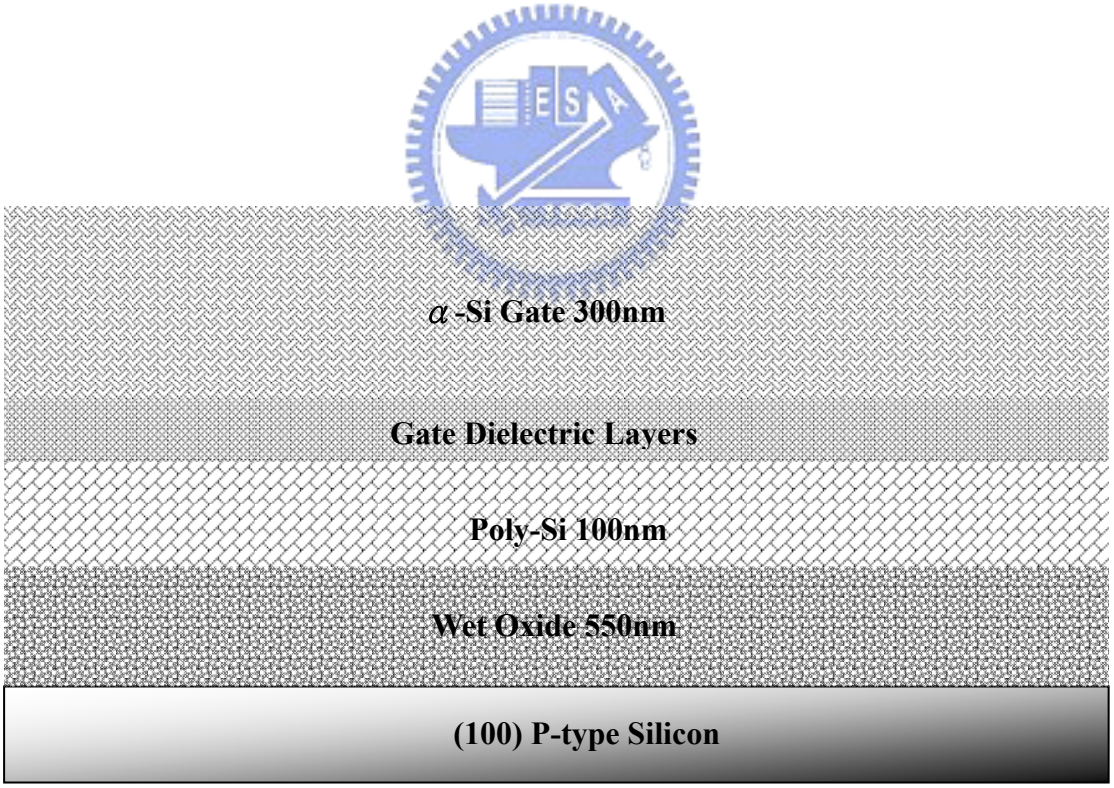
A 100nm-thick amorphous silicon (α-Si) was deposited at 550^{o}C by low-pressure chemical vapor deposition (LPCVD) system.



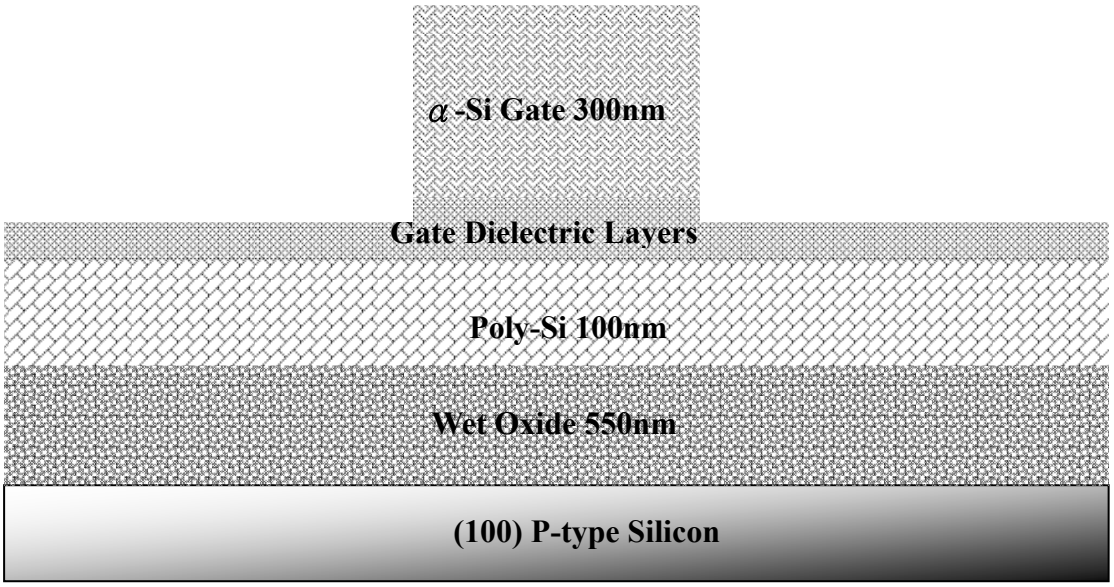
Wafer receive a furnace-annealed at 600^{o}C for 24 hours in N_2 ambient (SPC) to recrystallize the α-Si films and defined the active device islands region



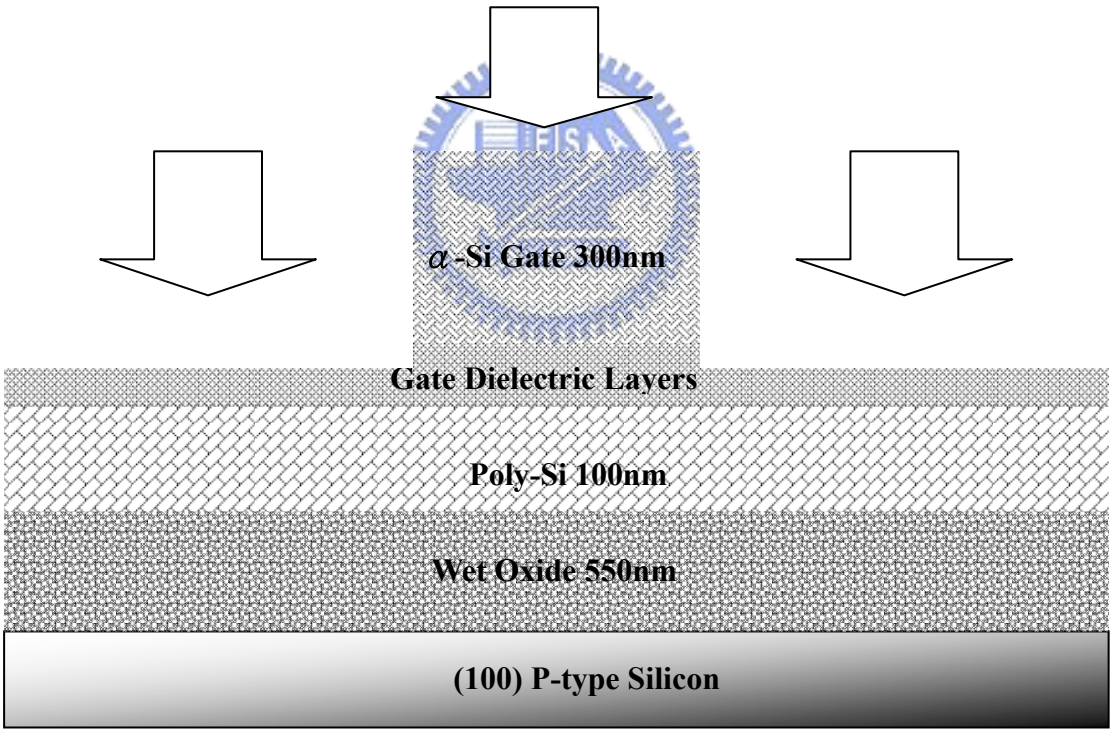
50nm dielectric then further split to three materials, HfO_2 and $HfSiO_x$ layers that was deposited by Metal-Organic Chemical Vapor Deposition (MOCVD)
Low temperature tetraethylorthosilicate silicon dioxide (TEOS-SiO_2) layer.



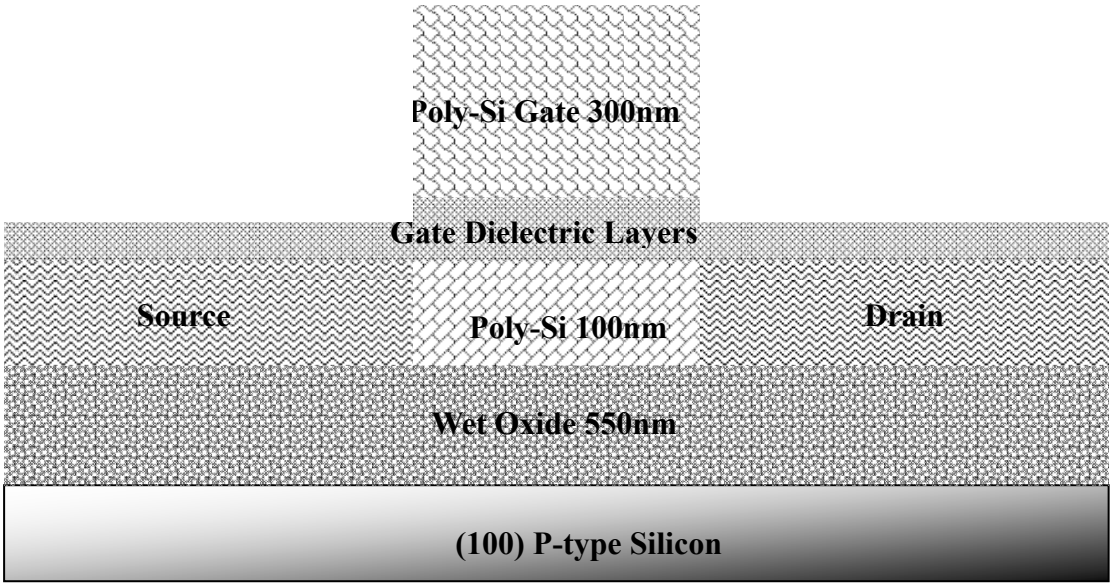
300nm-thick amorphous silicon film was deposited at 550^{o}C in a LPCVD system



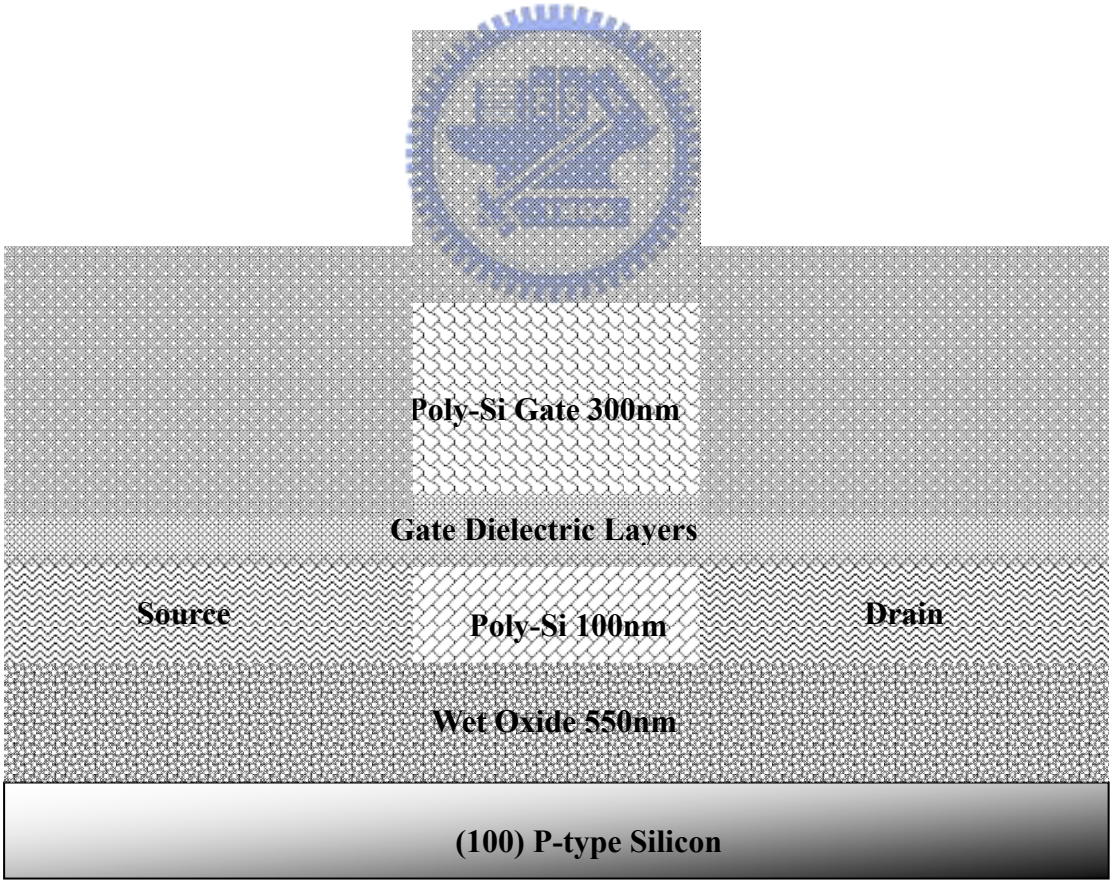
Patterned to form the gate of the transistor.



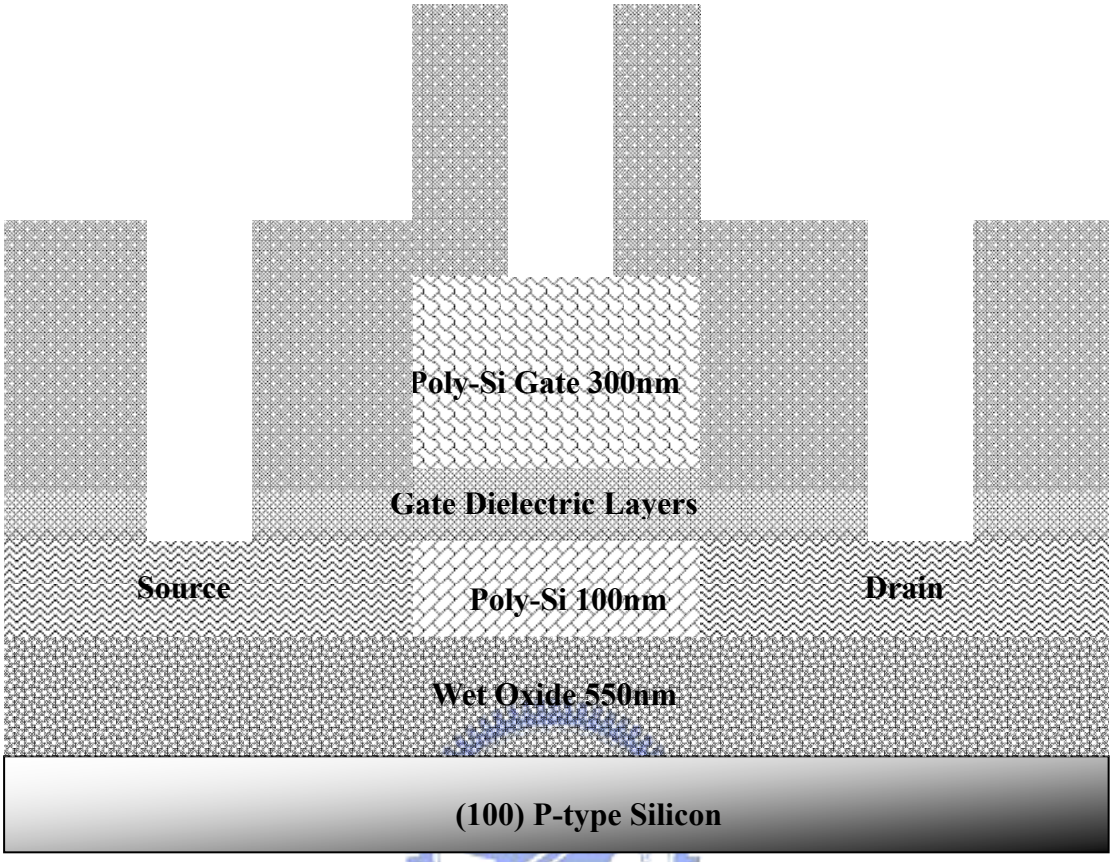
A self-aligned BF_2 ion implantation at 40 Kev with a dose of 5×10^{15} cm^{-2} was used to dope the drain, source, and gate simultaneously



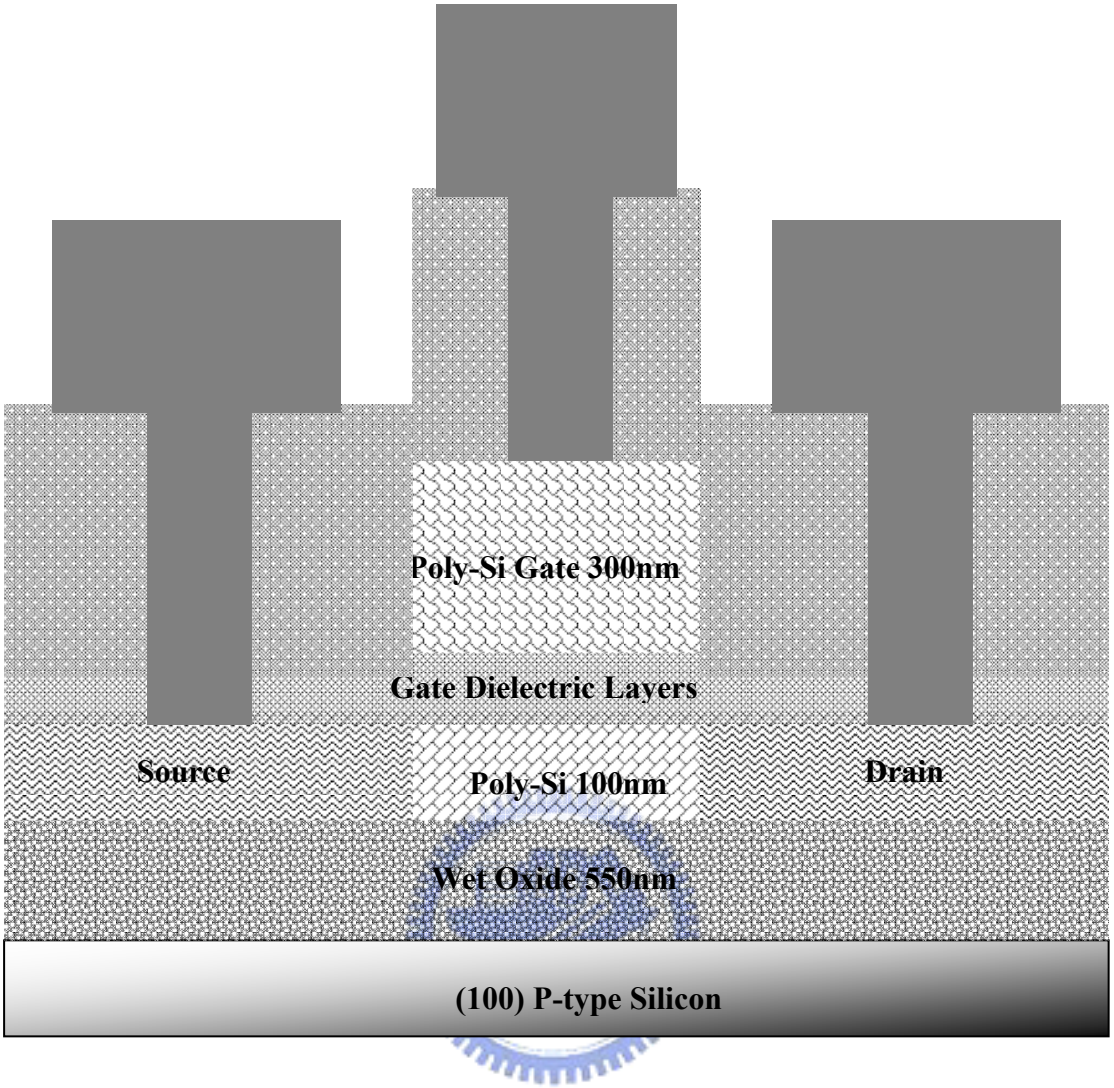
Dopant activation is to carry out by furnace 24h at 600^{o}C in N_2 ambient.



Passivation layer 550nm



Contact hole define and etching.



Al pad contacts were finished. After sintering at 300^{o}C, the process was completed.

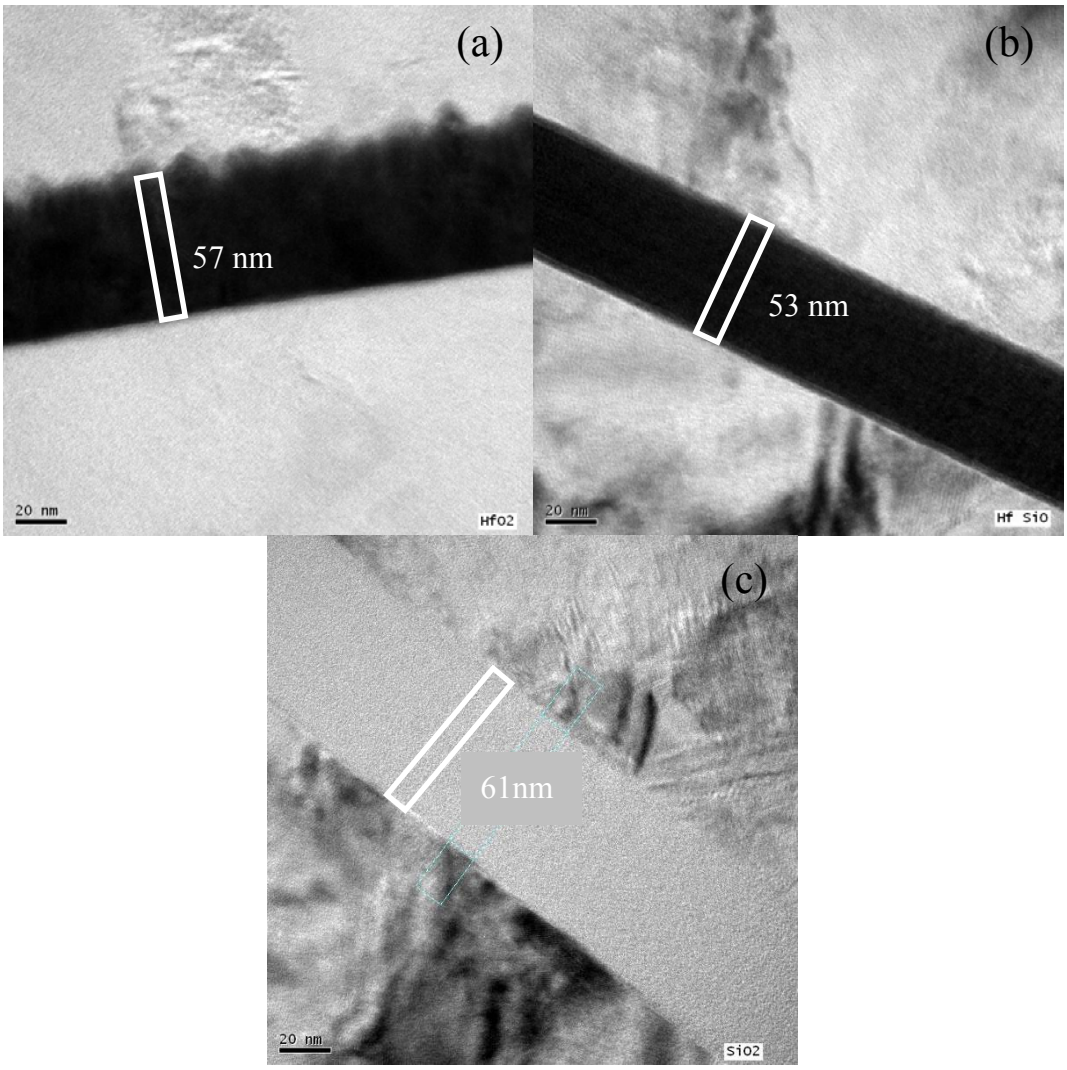


Figure 2-2 The cross-sectional transmission electron microscopy (TEM) images of the HfO_2, $HfSiO_x$ and deposited-SiO_2 films with a physical thickness of 57, 53, and 61 nm, respectively.

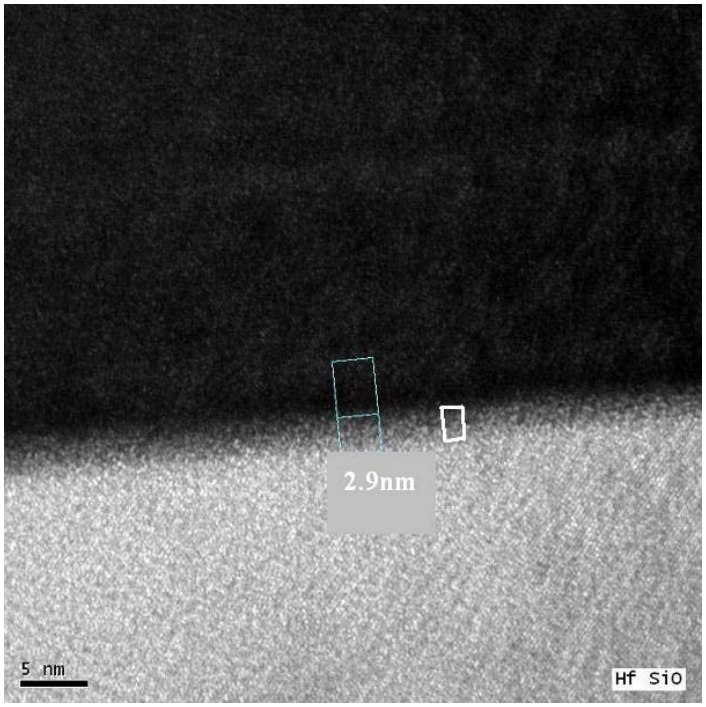


Figure 2-3 The interfacial layer between HfSiOx and Poly-Si channel with a physical thickness of 2.9 nm

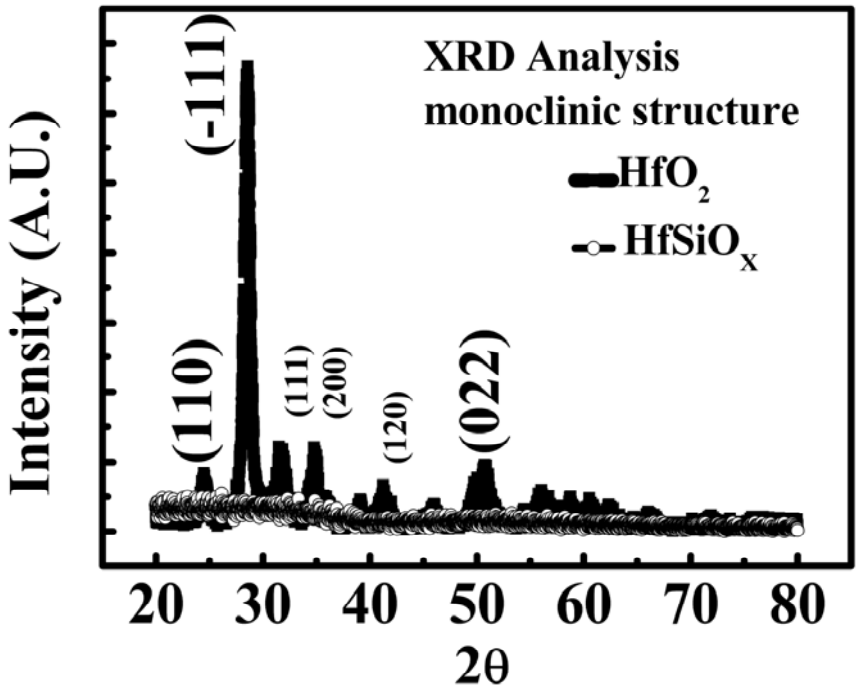


Figure 2-4 The x-ray diffraction spectroscopy (XRD) of HfO_2 and $HfSiO_X$ films, respectively.

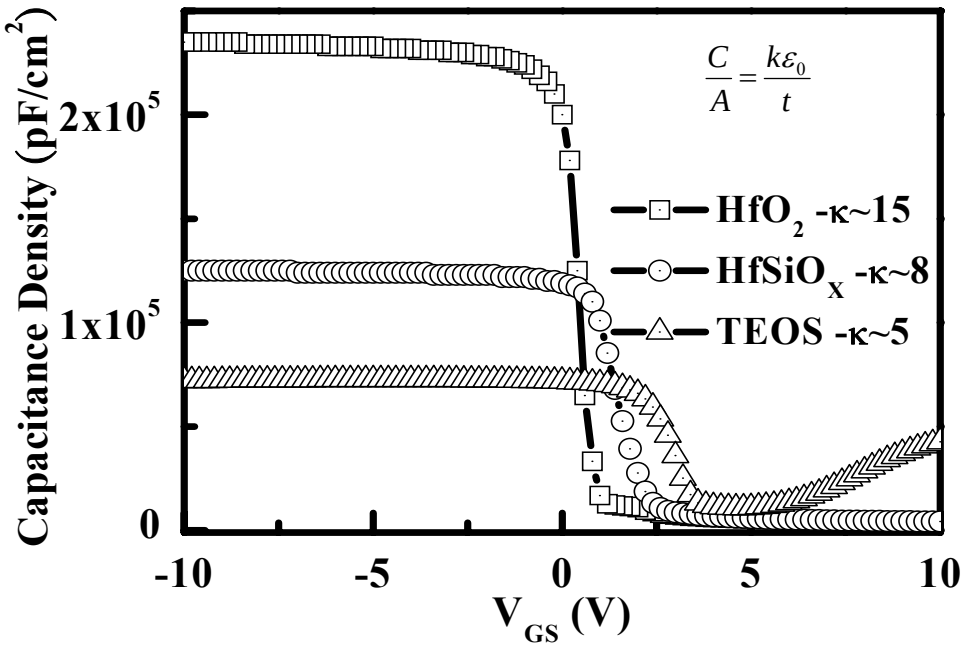


Figure 2-5 Capacitance capability of high-k dielectric and TEOS oxide.

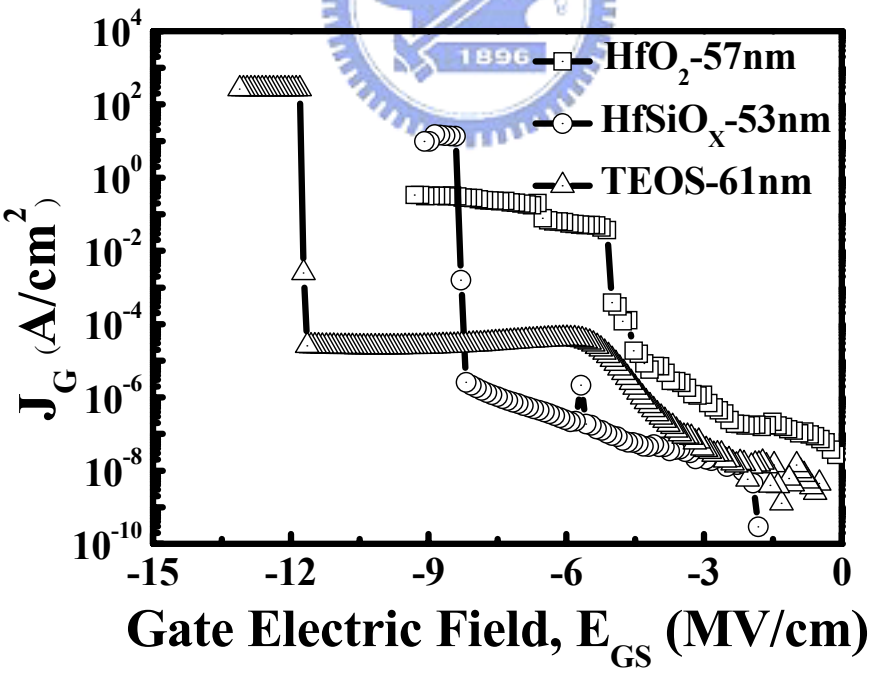


Figure 2-6 Breakdown field of high-k dielectric and TEOS oxide, $HfSiO_x$ has smaller leakage current and larger breakdown field than HfO_2

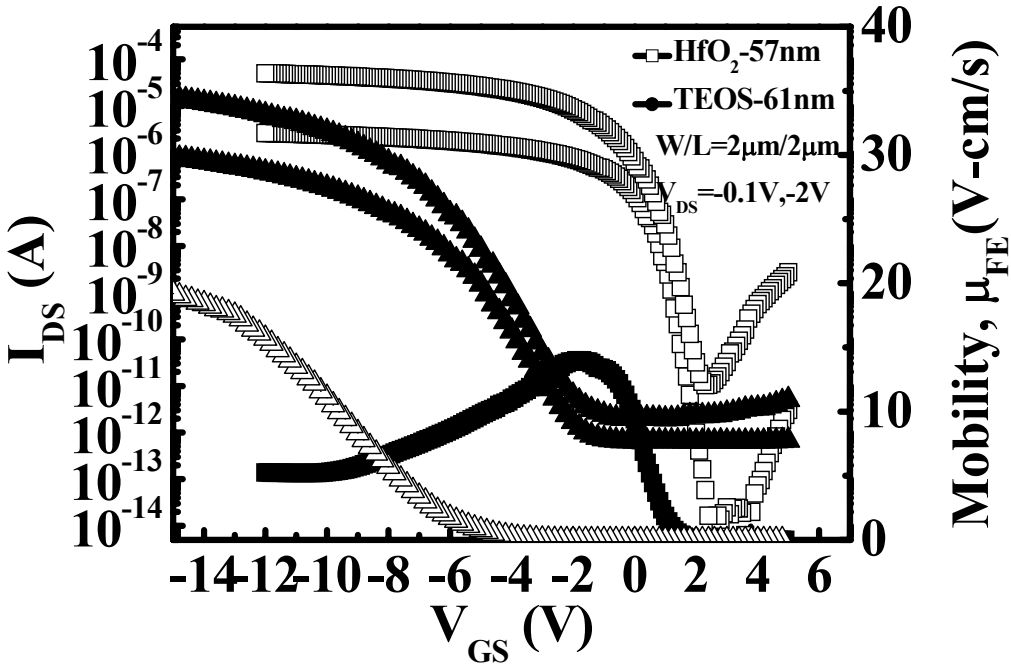


Figure 2-7 Transfer characteristics of TFTs with conventional TEOS and TFTs with HfO_2 comparison at gate dimension with W/L=2μm/2μm.

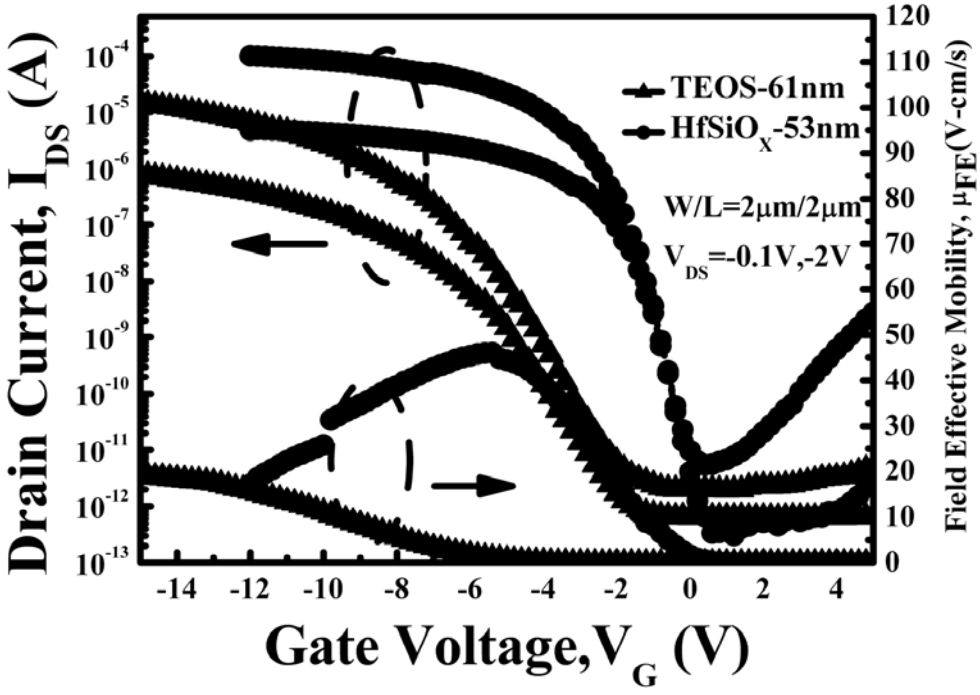


Figure 2-8 Transfer characteristics of TFTs with conventional TEOS and TFTs with $HfSiO_X$ comparison at gate dimension with W/L=2μm/2μm.

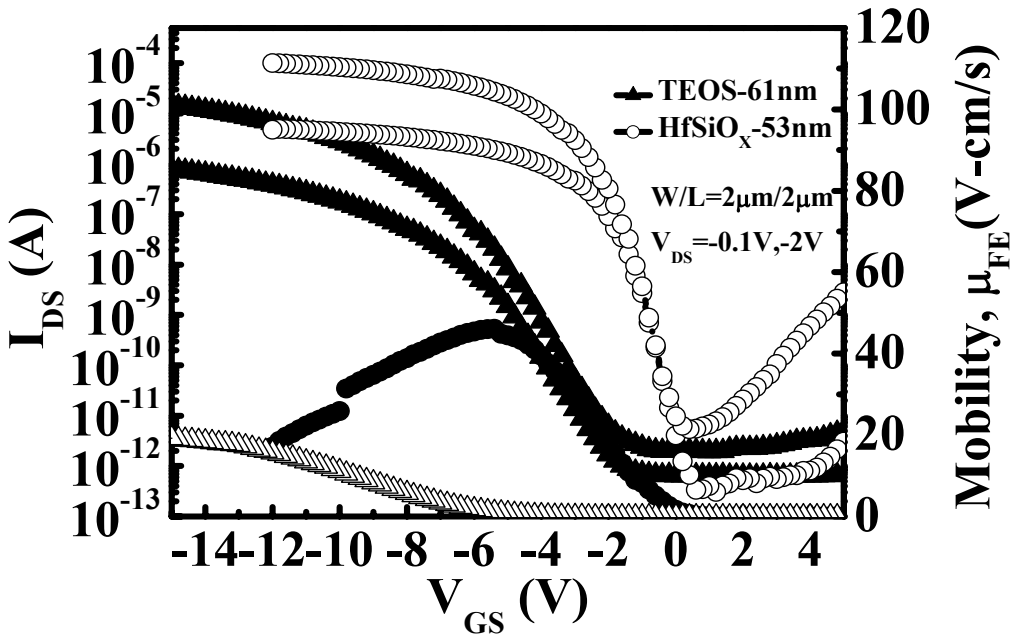
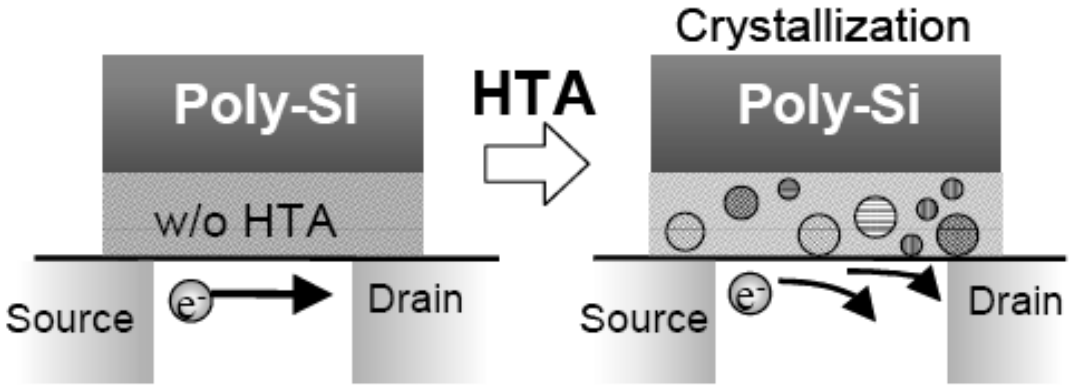


Figure 2-9 Transfer characteristics of TFTs with HfO_2 and TFTs with $HfSiO_X$ comparison at gate dimension with W/L=2μm/2μm.

Table 2-1 Summary of V_{TH}, S.S. and ON/OFF current ratio characteristics of High-k TFTs and conventional TFTs with W/L=2μm/2μm.

	V_{TH}(V)	μ_{EF} (cm^2/V-s)	S.S. (mv/dec)	I_{ON}/I_{OFF} (@V_{DS}=-2V)
HfO2 57nm	0.822	14	277.9	8.36E+06
HfSiO 53nm	-1.45	46	372.1	1.85E+07
TEOS 61nm	-6.27	19.2	1048	3.32E+06

Table 2-2 The crystallization structure of HfO2 dielectric film depicts the additional coulomb scattering that result in the mobility degradation.



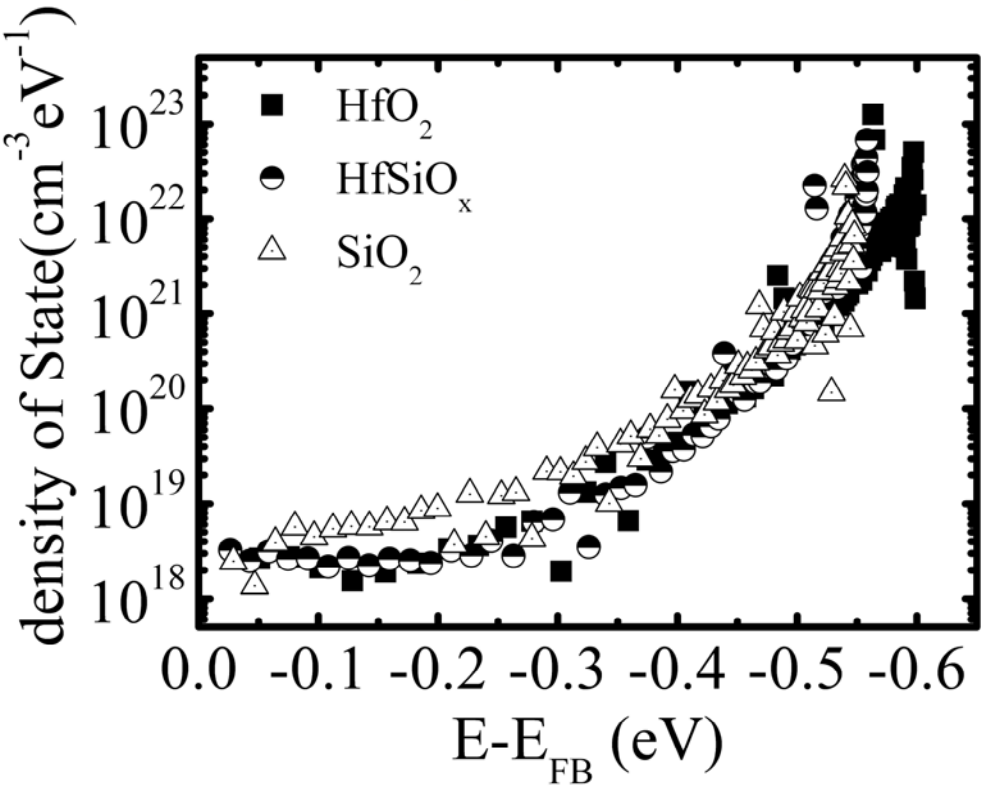


Figure 2-10 Density of states extracted from transfer characteristics (V_{ds}= -0.1V) of poly-Si TFTs using different gate dielectrics.

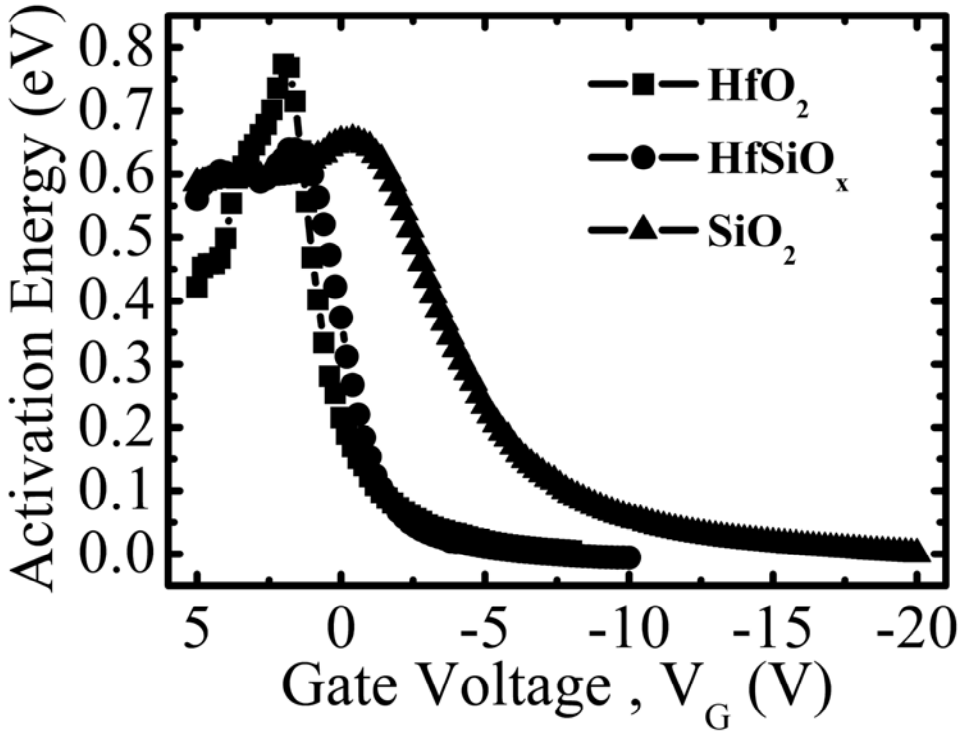


Figure 2-11 Activation energy of channel obtained from temperature dependence of transfer characteristics (V_{ds}= -0.1V) using different gate dielectrics.

Table 2-3 The trap-assisted-tunneling (TAT) enhance gate-induced-leakage-current (GIDL) at lower gate bias.

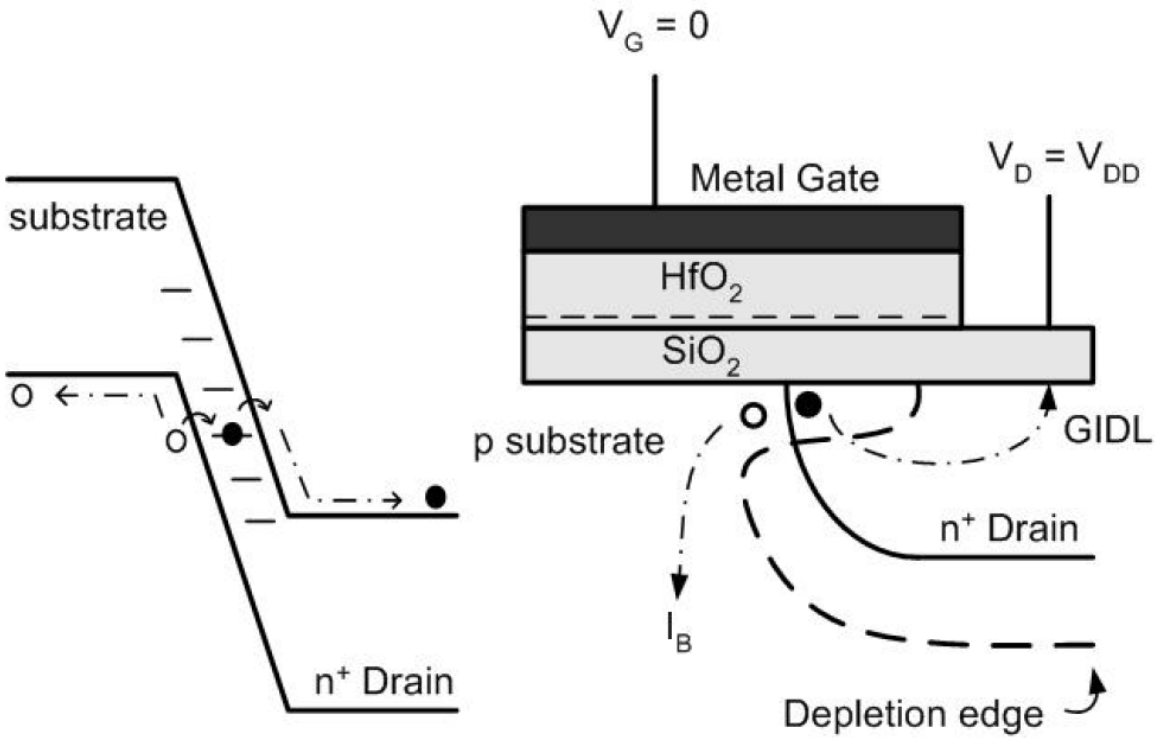
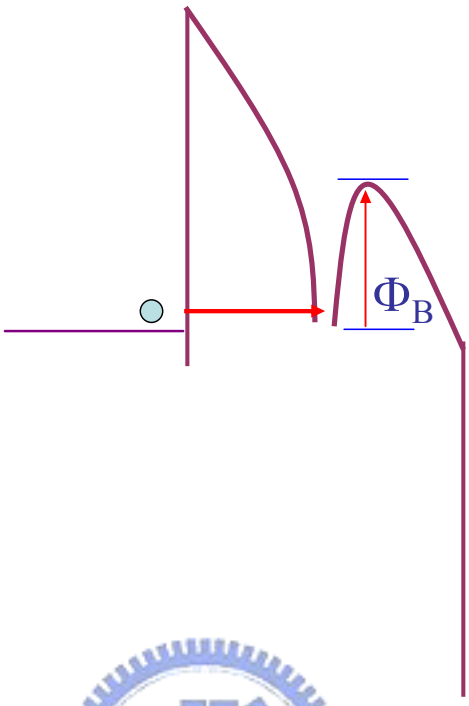


Table 2-4 The Frenkel-Poole emission illustration.



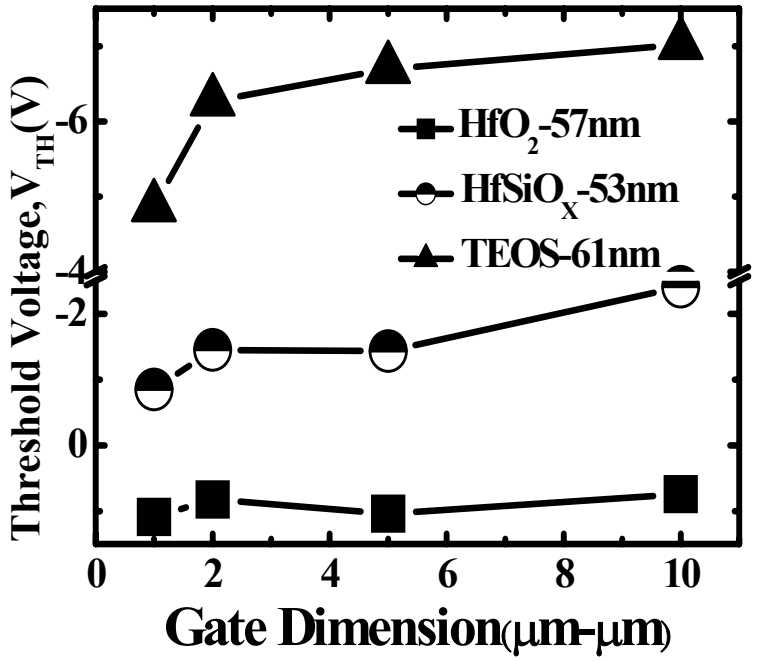


Figure 2-12 Threshold voltage roll-off of different dielectrics comparison, from W/L=10μm/10μm scale down to W/L=1μm/1μm

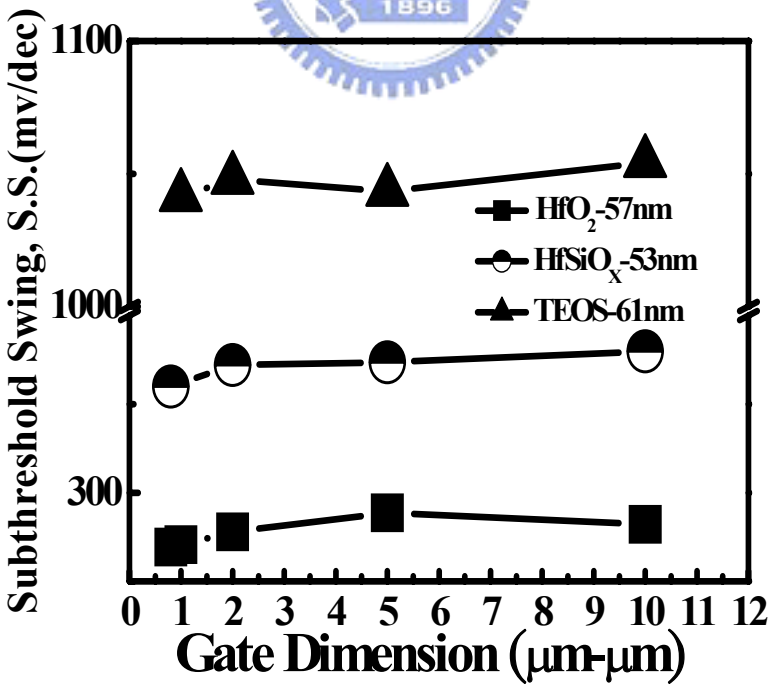


Figure 2-13 Subthreshold swing characteristics of different dielectrics comparison, from W/L=10μm/10μm scale down to W/L=1μm/1μm.

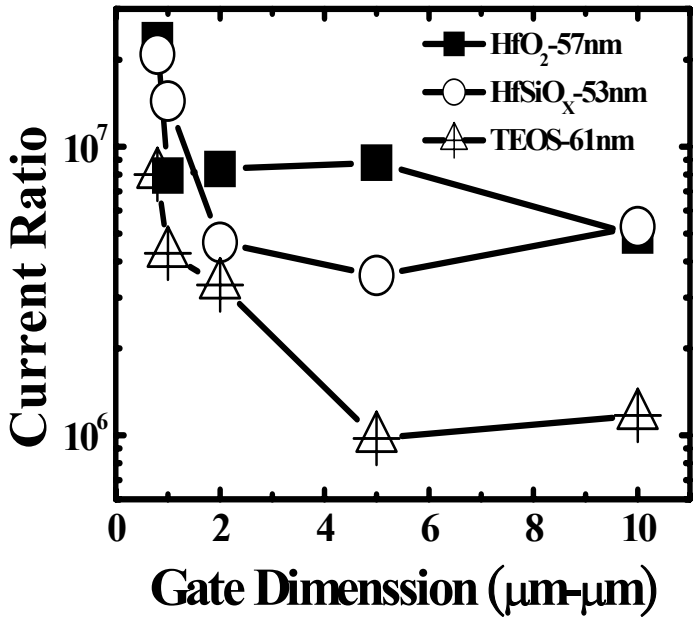


Figure 2-14 On/Off ratio characteristics of different dielectrics comparison, from W/L=10μm/10μm scale down to W/L=1μm/1μm.

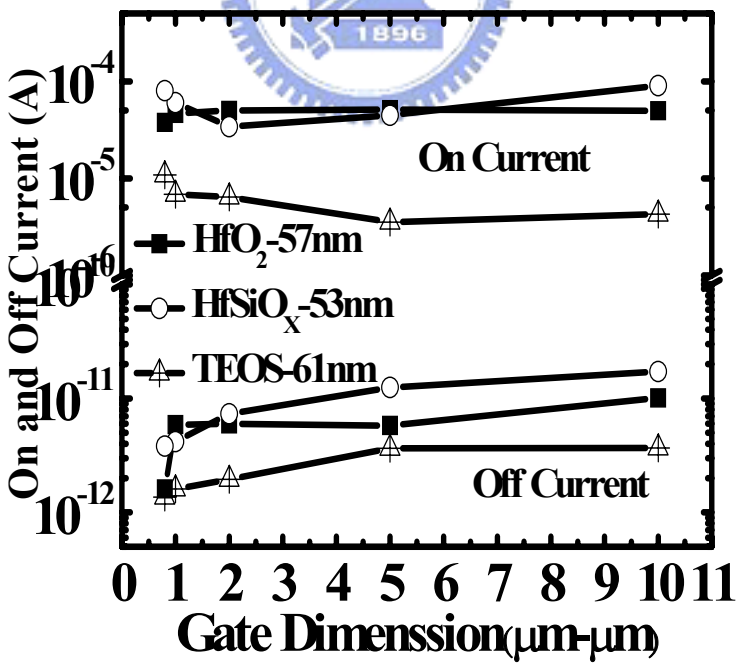


Figure 2-15 On current and off current characteristics of different dielectrics comparison, from W/L=10μm/10μm scale down to W/L=1μm/1μm

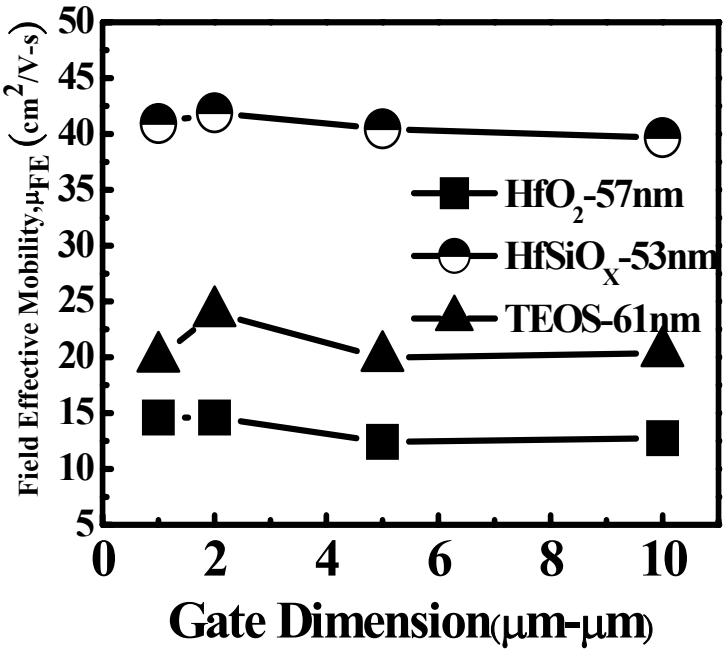


Figure 2-16 Mobility characteristics comparison of different dielectrics comparison, from W/L=10μm/10μm scale down to W/L=1μm/1μm

Chaprer3 Reliability of the p-Channel with TEOS and High-k TFTs

3.1 Introduction

The device performance of poly-Si TFTs is always limited by defect state exisiting in the bulk, at grain boundries, or at the poly –Si/ dielectric interface[34,35].

It is well known that various plasma treatments, including N_2, N_2/H_2 mixture, O_2, O_2/H_2, and F_2 were investigated to improve the performance of poly-Si TFTs by lowering the grain boundry potential barriers[36,37] (e.x. hydrogen plasma treatment) or improve the plasma passivation effects.

In this thesis, the non-treatment performance of high-k dielectrics TFTs were improved obviously. Therefore, various gate biases were used to observe the reliability of non-plasma treatment high-k dielectric TFTs. Additionally; we also used the gate bias stress to compare the reliability of non-plasma treatment TEOS TFTs.

3.1.1 Threshold Voltage Shift

In poly-Si TFTs, the threshold voltage depend mainly on dangling bond trap states located near the midgap, in addition to the generation of dangling bond midgap states, charge trapped within the gate dielectric resulting in a strong V_{TH} shift[38].

Several articles report higher NBTI degradation for higher initial interface trap density[39]. In additionally, the bulk trap of high-k dielectrics will enhance the faster V_{TH} shift during the shorter stress time.

3.1.2 Transconductance and Drive Current Degradation

We extracted the field-effective mobility degradation from the maximum transconductance with I_D-V_G measurement, in additionally, the on, off, and current ratio were extracted by the fixed V_{GS}. The HfO_2 and $HfSiO_X$ at the -8V and at the -17V with TEOS. During the NBI and NBTI stress, strain-bond tail-state will generate and cause the current and maximum transconductance Gm degradation. The trapped holes increase the vertical field near the drain junction of the transistor operated in the off-state regime. Thus, in addition to the strain-bond tail states generated during the gate bias stress, the increased electric field results in a faster degradation of current and Gm.

3.2 Experimental Procedures

The detail fabrication process of polycrystalline silicon TFTs is described in Chapter 2. Keithley 4200 semiconductor parameter analyze was used to generate gate bias stress and extract the parameters degradation after the long time stress. For p-channel devices, we focus on Negative bias on room temperature and we will

continue to focusing on the high temperature (e.x. 100^{o}C) that is called NBTI Stress in the future. The characterization involved the -0.1V and -2V were applied to the drain contact. Particularly, the gate voltage was swept from 5V to -8V in high-k dielectrics TFTs and 5V to -17V in TEOS TFTs. For this reason is that we went to extract the Field Effective mobility from the maximum transconductance at high-k dielectrics TFTs. However, we can not observe the maximum transconductance of TEOS TFTs. The measurement setup illustration is show in Table 3-1.

3.3 Result and Discussion

3.3.1 Negative Gate Bias Stress Instability

In this chapter, we will show dielectric reliability of TEOS TFTs, $HfSiO_X$ TFTs, and HfO_2 TFTs at room temperature. In Figure 3-1 to Figure 3-3, Figure 3-10 to Figure 3-12 and Figure 3-19 to Figure 3-21, we show the different Id-Vg characteristics of different dielectric that before and after stress. After 10000sec negative gate bias stress, we can observe the threshold voltage shift toward the negative direction after the NBI stress. In addition, the NBI stress also leads to the device degradation in the field-effect mobility, drive current and off-state leakage current. In particularly, the subthreshold swing degradation was not obvious to see

after the 10000 second stress.

The threshold voltage shift of TFTs with TEOS after stress that increase more and more fast than TFTs with high-k dielectric. At this case, the reliability of TFTs with $HfSiO_X$ dielectric is better than HfO_2 and TEOS. This can be explained as fallows: first, according to the density of states with different dielectrics from chapter2, the deep states near the mid-gap of TFTs with TEOS was more than TFTs with high-k dielectrics, therefore, the threshold voltage shift is more than the TFTs with high-k dielectrics. Second, the quality of TEOS layers is poorer than HfSiOX or HfO2 layers such that the TEOS TFTs depicts faster V_{TH} shift. On the other hand, the slope of the log-log plot means the interface state creation number, so we can estimate the $HfSiO_X$ TFTs depicts the best interface quality and the TEOS TFTs depicts the poorest interface quality.

In particularly, the high-k TFTs depict faster V_{TH} shift during the just beginning stress time and then in turn shift slowly. The jump can be explained by the general and initial bulk trap in the high-k dielectrics.

The mobility degradation of TFTs with different gate dielectrics at room temperature is show in Figure 3-31, we can observe the mobility of TFTs with TEOS degradation more and more faster between 1000 sec. and 10000 sec. The same degradation tendence of on current can be observe in Figure 3-34, This can be

explained by faster threshold voltage shift and mobility degradation. The off current degradation of TFTs with HfO_2 is more serious than other two materials, this can be explained by high gate capacitance density enhance the electron trap in the off-state regime such that increase the electrical field near the drain junction of TFTs. Therefore, the off current degradation of TFTs with HfO_2 is most serious and we can observe the HfO_2 and TEOS TFTs depict more serious on/off current ratio degradation.

3.3.2 Negative Bias Temperature Instability

After the constant gate bias stress, we add the temperature test and observe the same degradation tendence of TFTs with different dielectrics we using. In Figure 3-29 and Figure 3-30 is for threshold shift at the 75^{o}C and 100^{o}C, in Figure 3-32 and Figure 3-33 is for mobilities degradation and then is the current degradation. According to the results, we suggest the threshold voltage shift of TFTs with high-k dielectrics is due to the oxide trap. Because of that the subthreshold swing degradation is not obviously during stress time. On the other hand, the threshold voltage shift of TFTs with TEOS-oxide is due to the initial deep state near the mid-gap is more than TFTs with high-k dielectrics. This is result in the holes tunnel to the deep trap state easier than other two materials. Therefore, the on current and mobility of TFTs with

TEOS-oxide is degradation more serious as we extracted the parameter at the constant voltage.

Table 3-1 The measurement setup illustration.

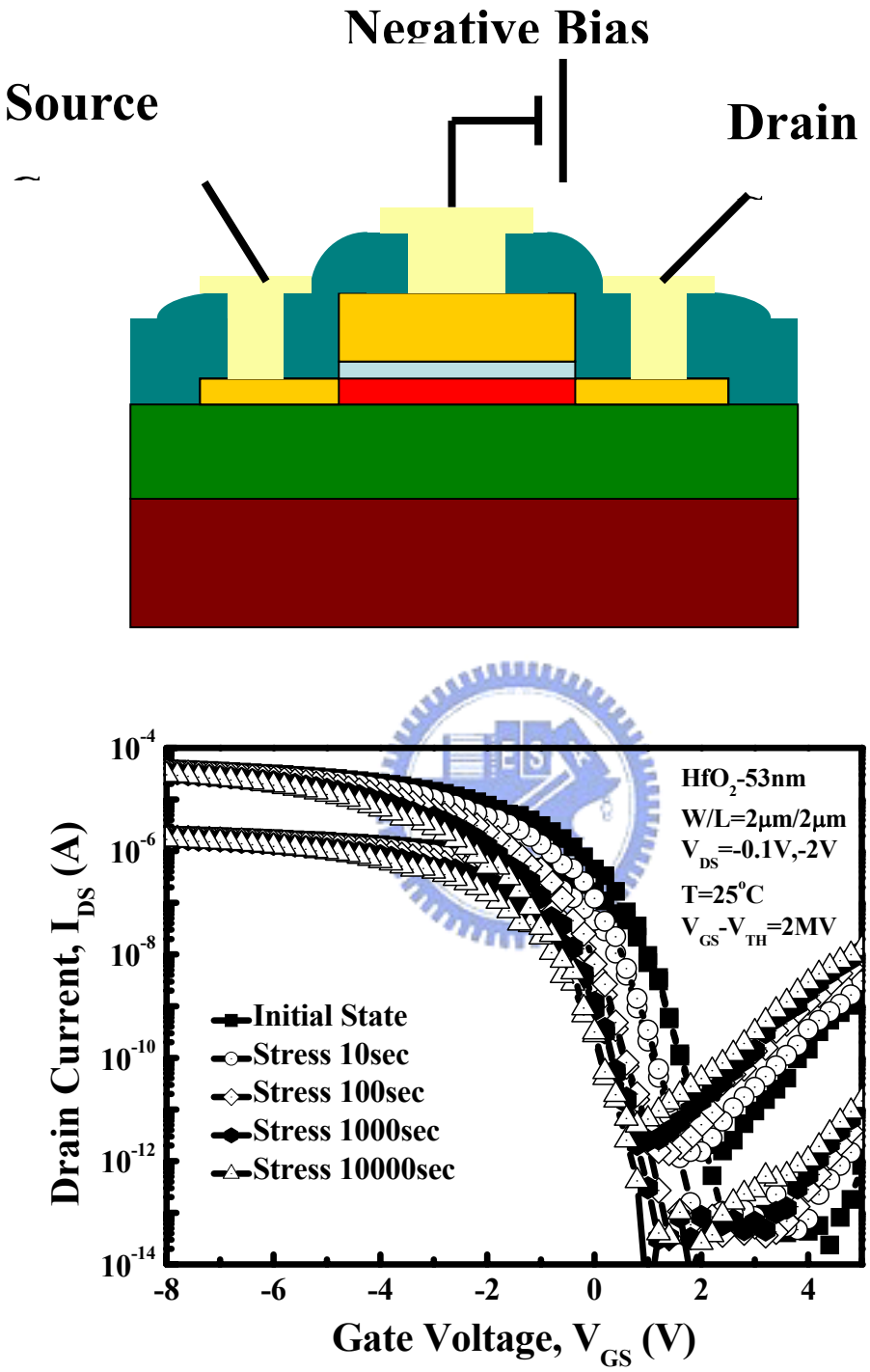


Figure 3-1 The transfer characteristics of the LTPS TFTs under NBTI stress with different stress time, respectively.

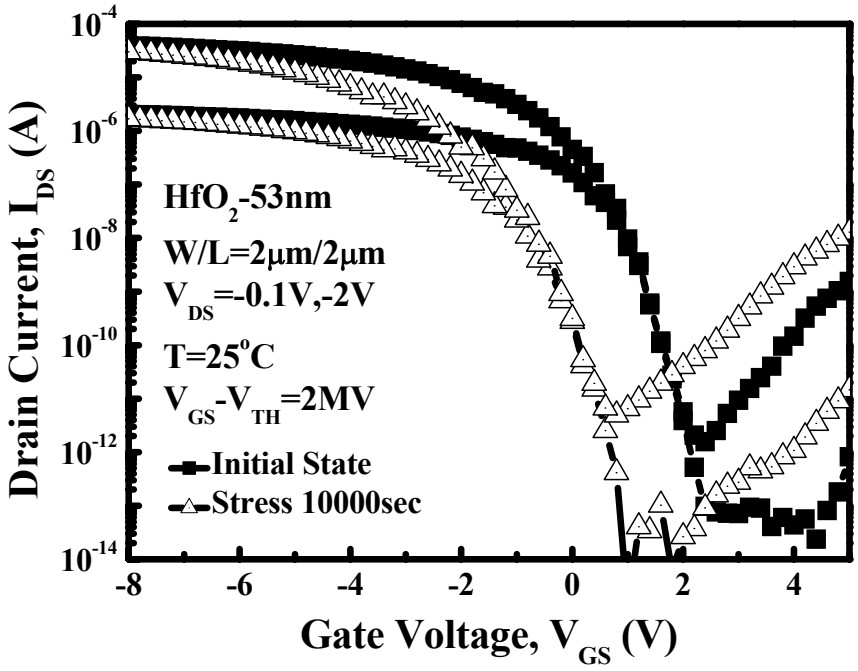


Figure 3-2 The transfer characteristics of the LTPS TFTs under NBI stress with initial state and 10000sec., respectively.

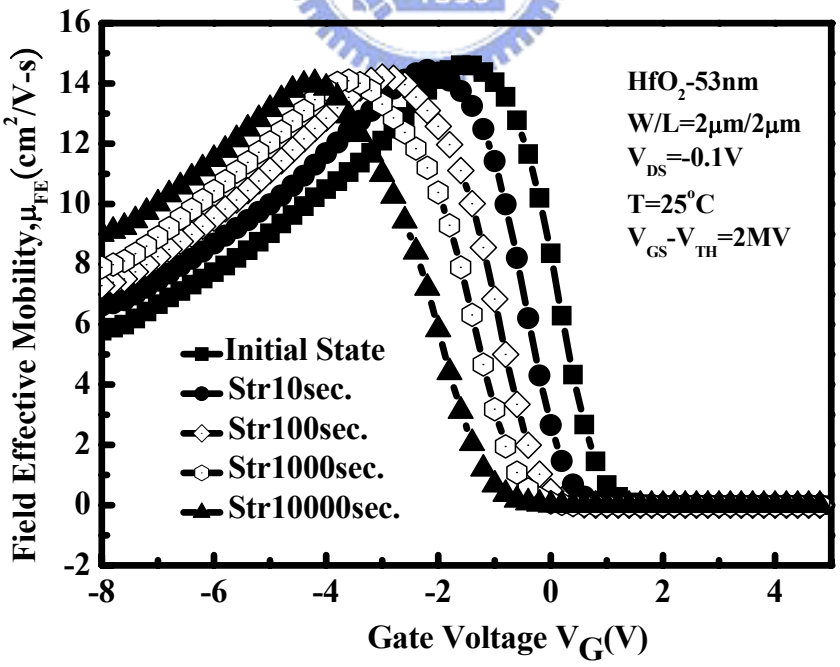


Figure 3-3 Mobility degradation with different stress time.

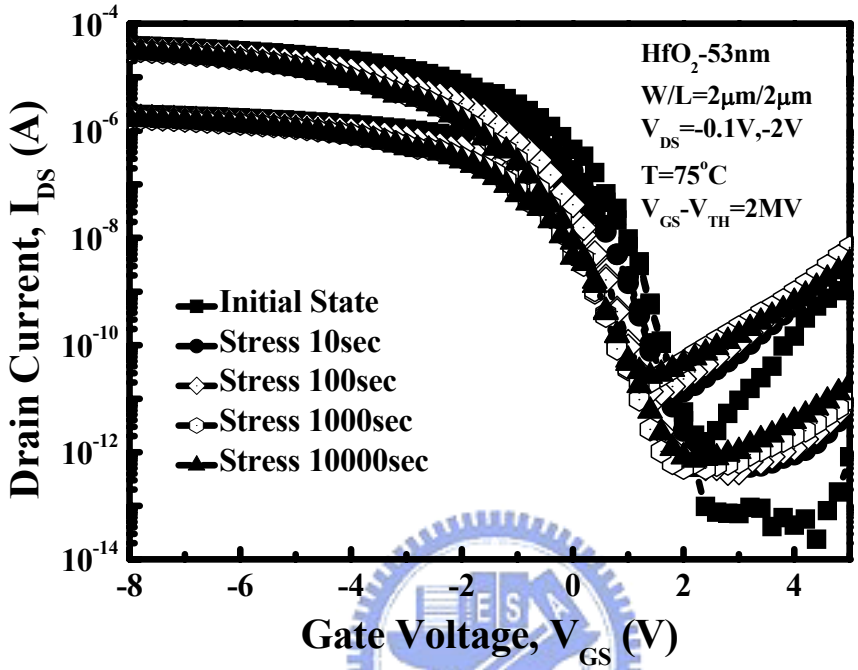


Figure 3-4 The transfer characteristics of the LTPS TFTs under NBTI stress with different stress time, respectively. The stress was performed at 75°C

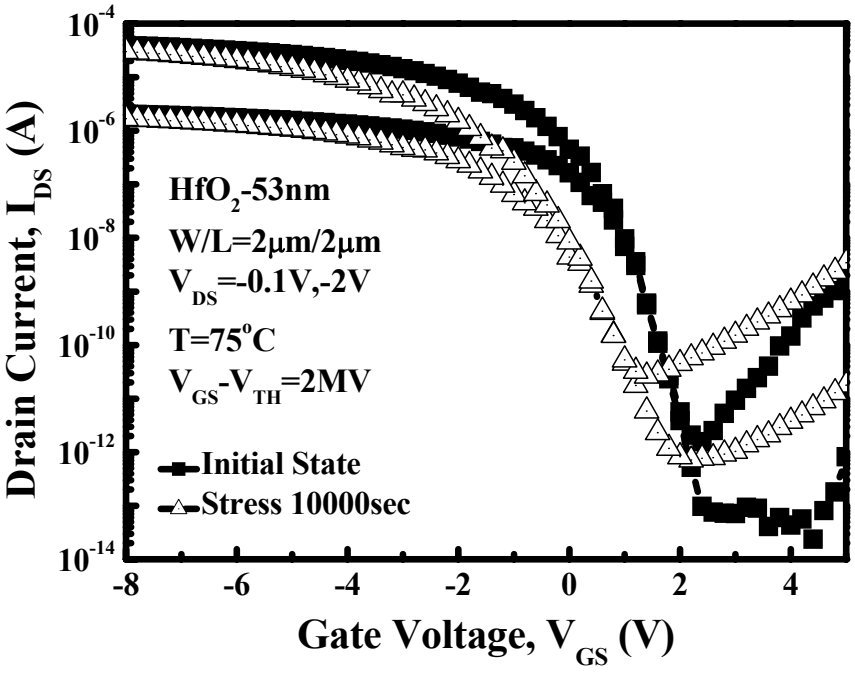


Figure 3-5 The transfer characteristics of the LTPS TFTs under NBTI stress with initial state and 10000sec., respectively. The stress was performed at 75°C

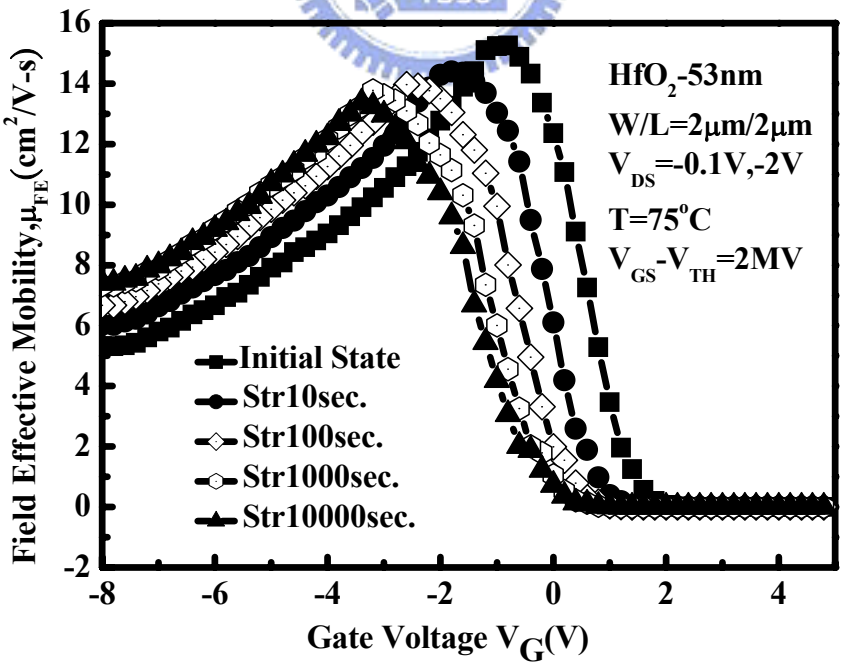


Figure 3-6 Mobility degradation with different stress time. The stress was performed at 75°C

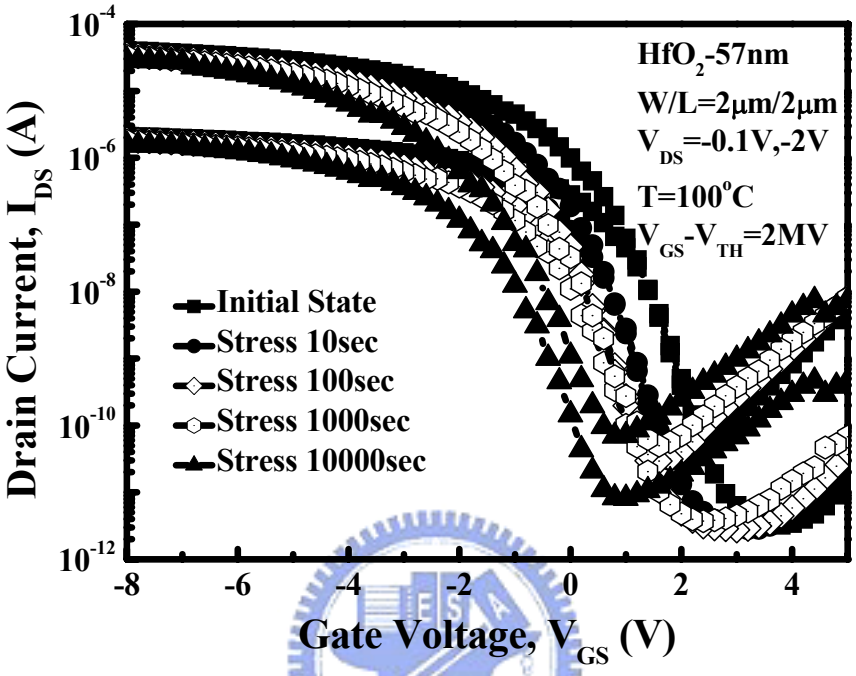


Figure 3-7 The transfer characteristics of the LTPS TFTs under NBTI stress with different stress time, respectively. The stress was performed at 100°C

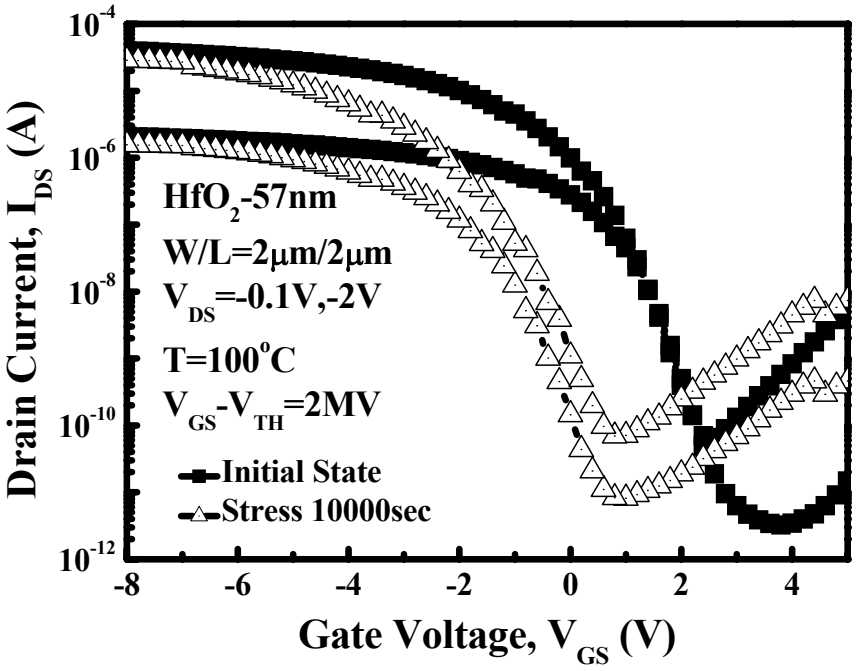


Figure 3-8 The transfer characteristics of the LTPS TFTs under NBTI stress with initial state and 10000sec., respectively. The stress was performed at 100°C

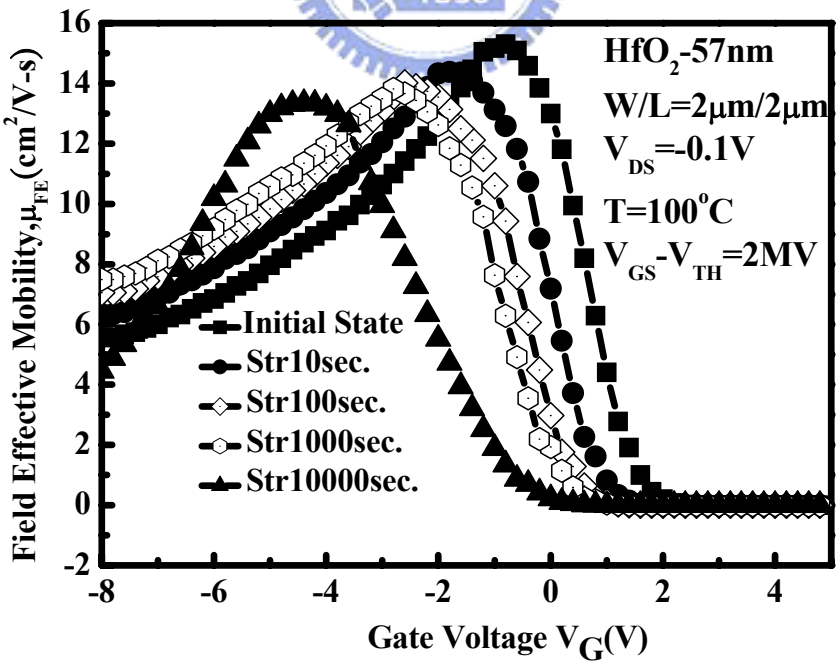


Figure 3-9 Mobility degradation with different stress time. The stress was performed at 100°C

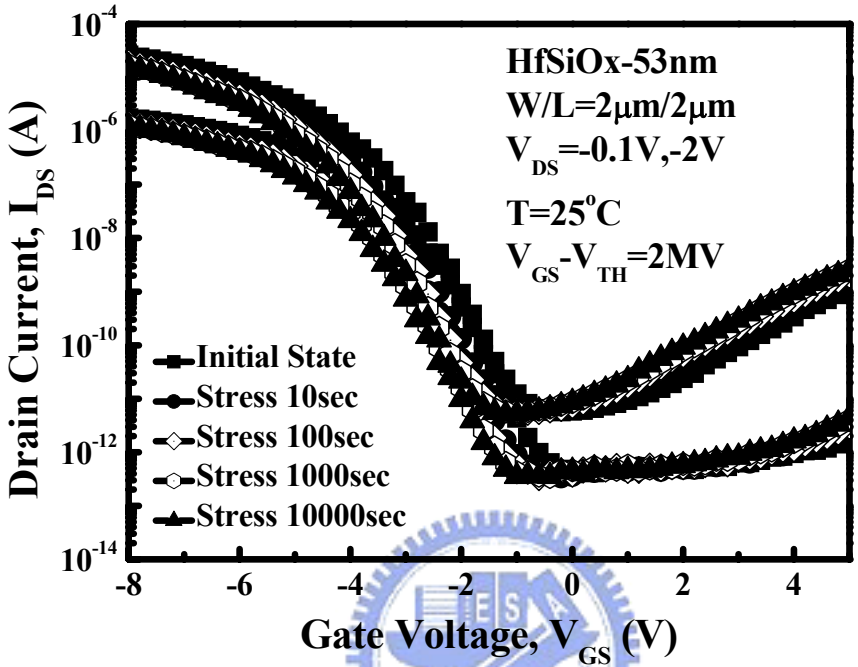


Figure 3-10 The transfer characteristics of the LTPS TFTs under NBTI stress with different stress time, respectively.

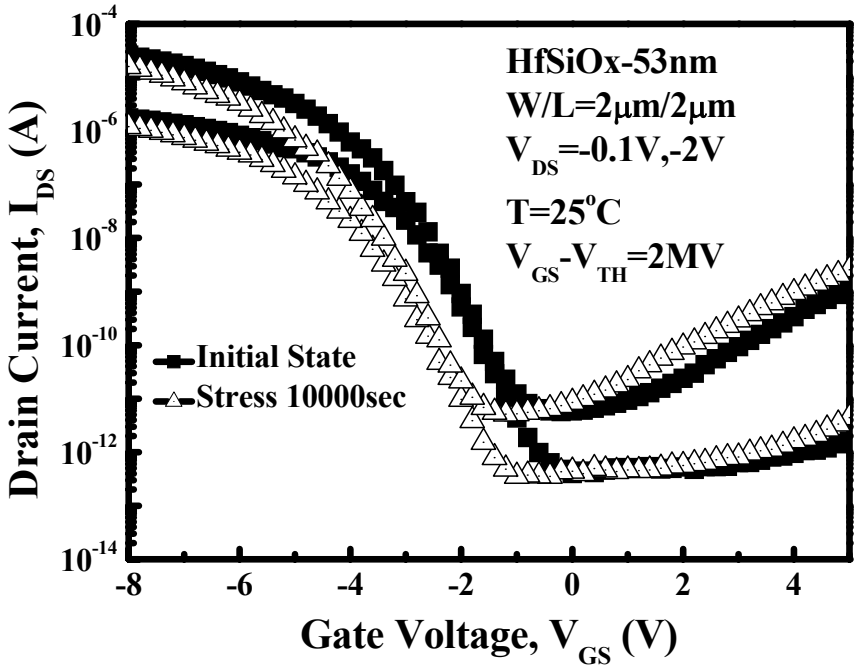


Figure 3-11 The transfer characteristics of the LTPS TFTs under NBI stress with initial state and 10000sec., respectively.

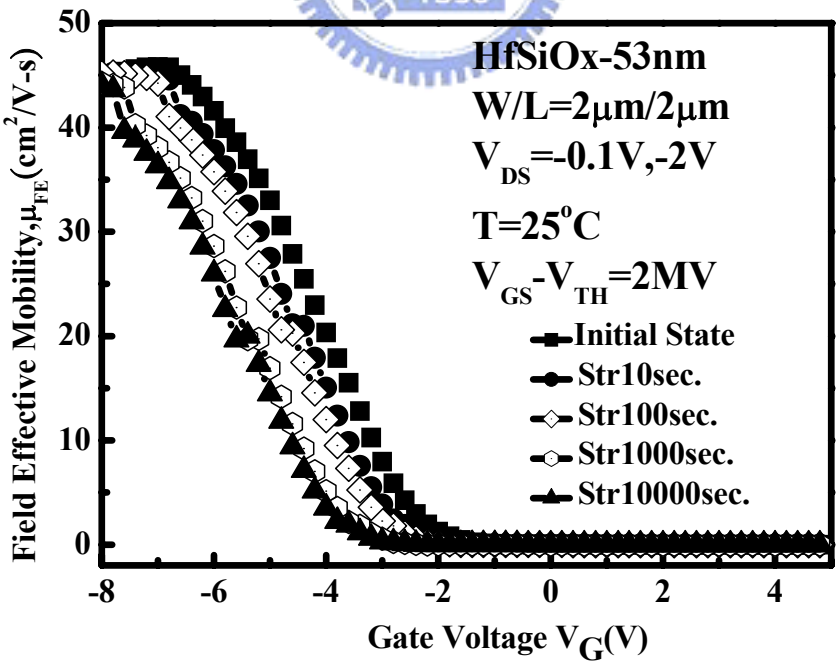


Figure 3-12 Mobility degradation with different stress time.

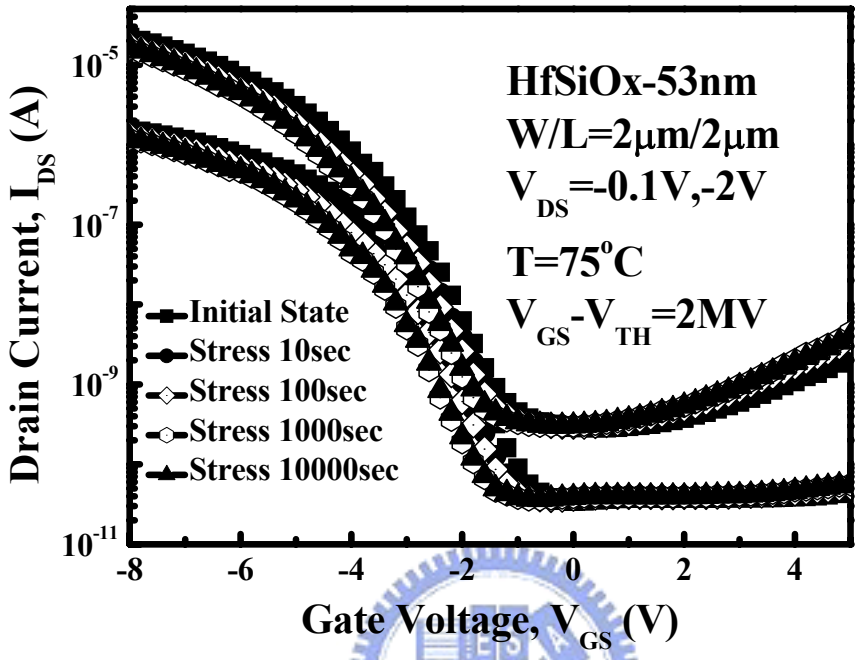


Figure 3-13 The transfer characteristics of the LTPS TFTs under NBTI stress with different stress time, respectively. The stress was performed at 75°C

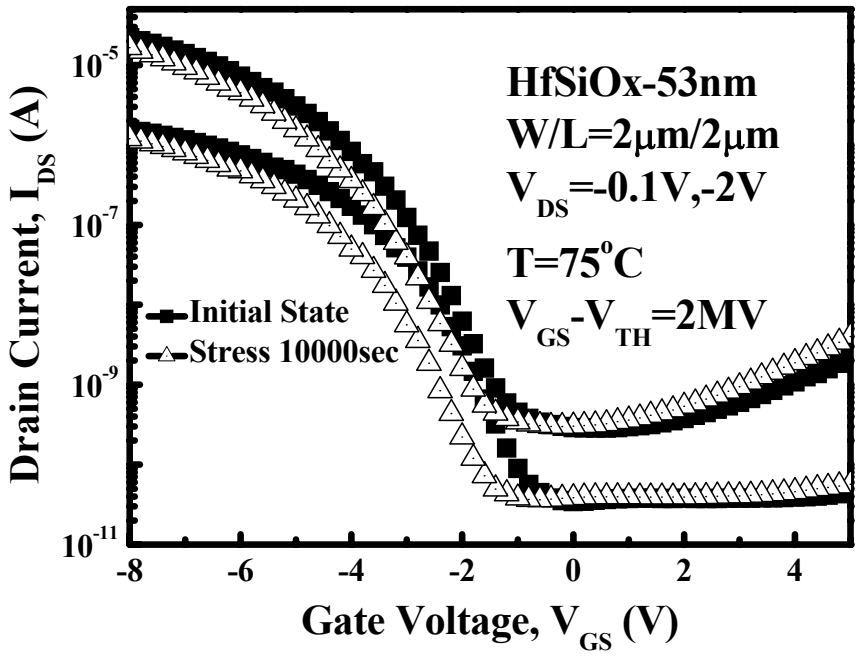


Figure 3-14 The transfer characteristics of the LTPS TFTs under NBTI stress with initial state and 10000sec., respectively. The stress was performed at 75°C

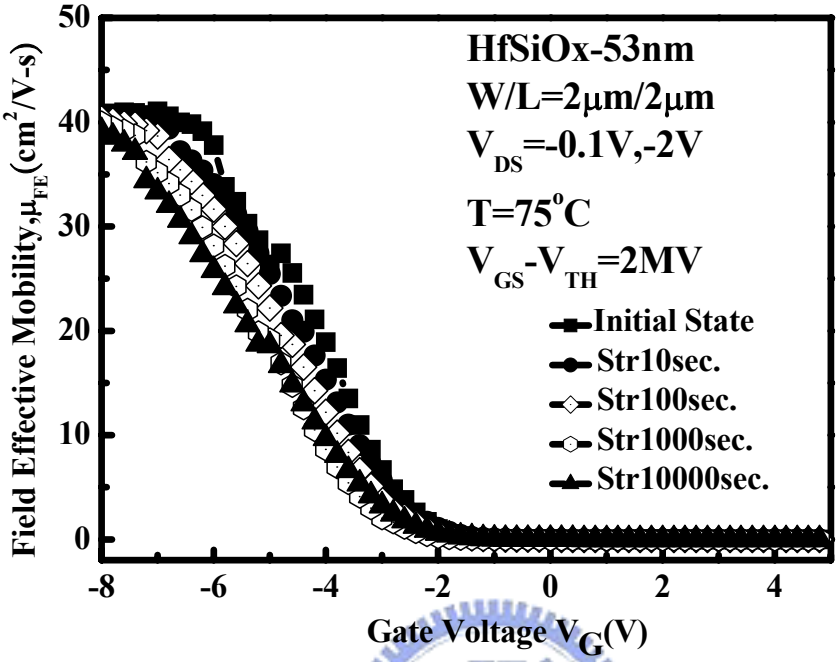


Figure 3-15 Mobility degradation with different stress time. The stress was performed at 75°C

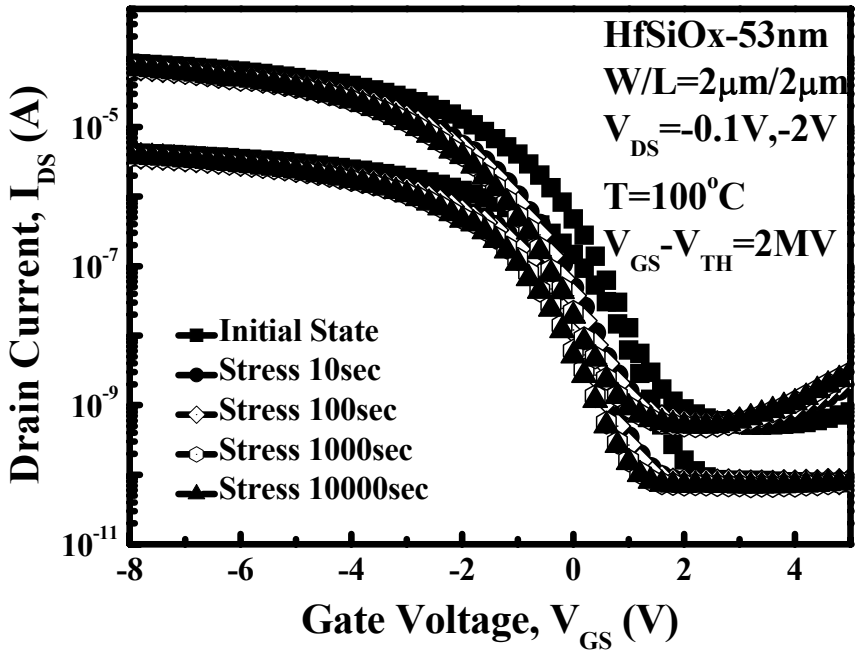


Figure 3-16 The transfer characteristics of the LTPS TFTs under NBTI stress with different stress time, respectively. The stress was performed at 100°C

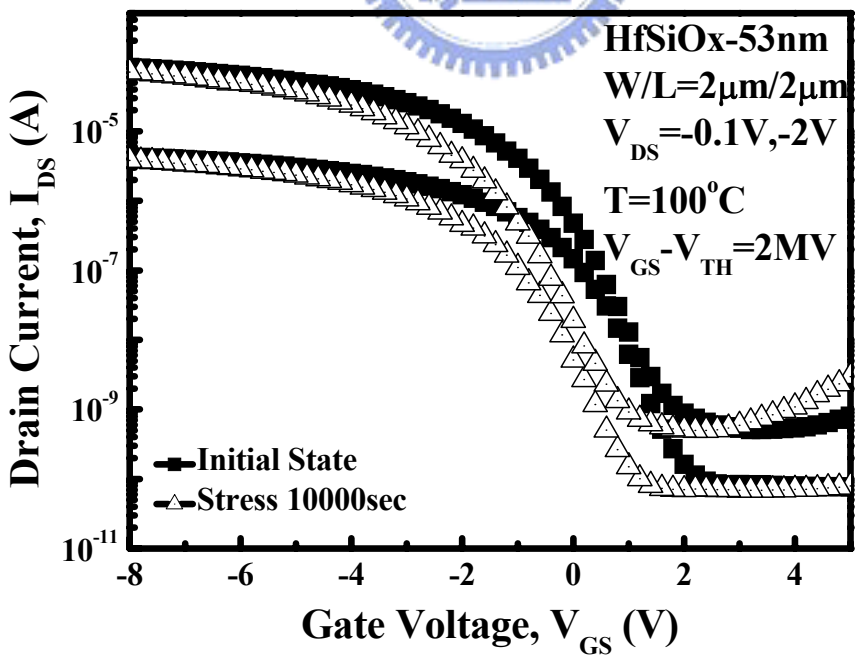


Figure 3-17 The transfer characteristics of the LTPS TFTs under NBTI stress with initial state and 10000sec., respectively. The stress was performed at 100°C

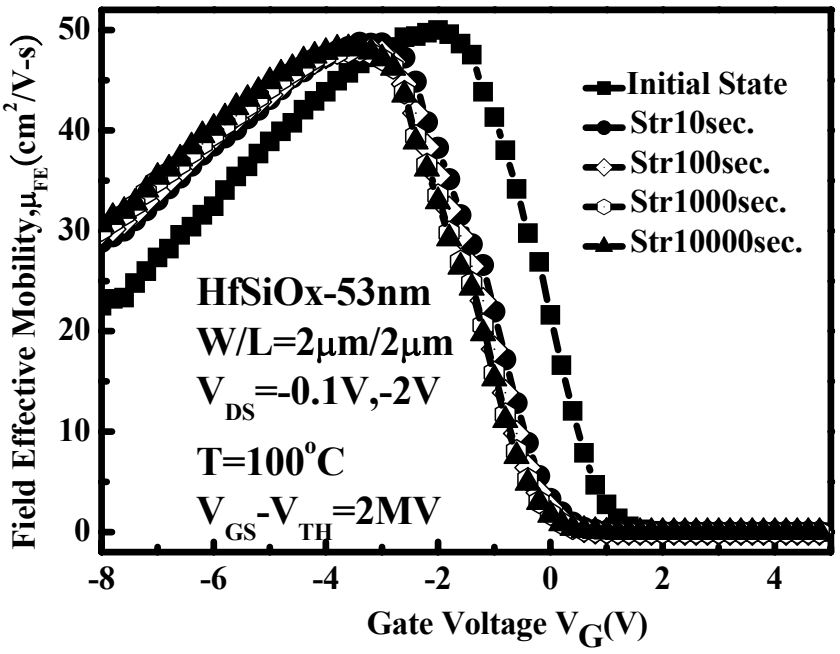


Figure 3-18 Mobility degradation with different stress time. The stress was performed at 100°C

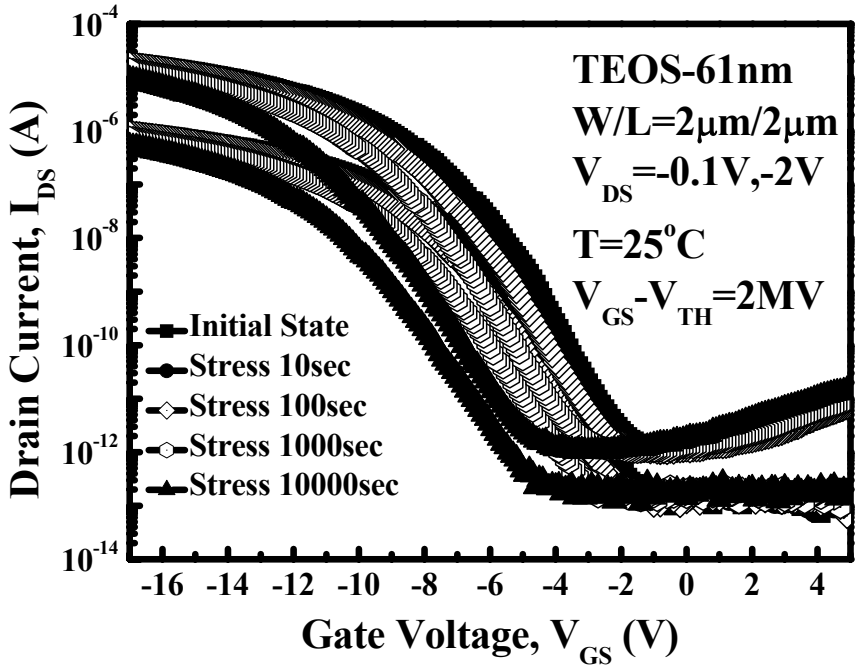


Figure 3-19 The transfer characteristics of the LTPS TFTs under NBTI stress with different stress time, respectively. The stress was performed at 25°C

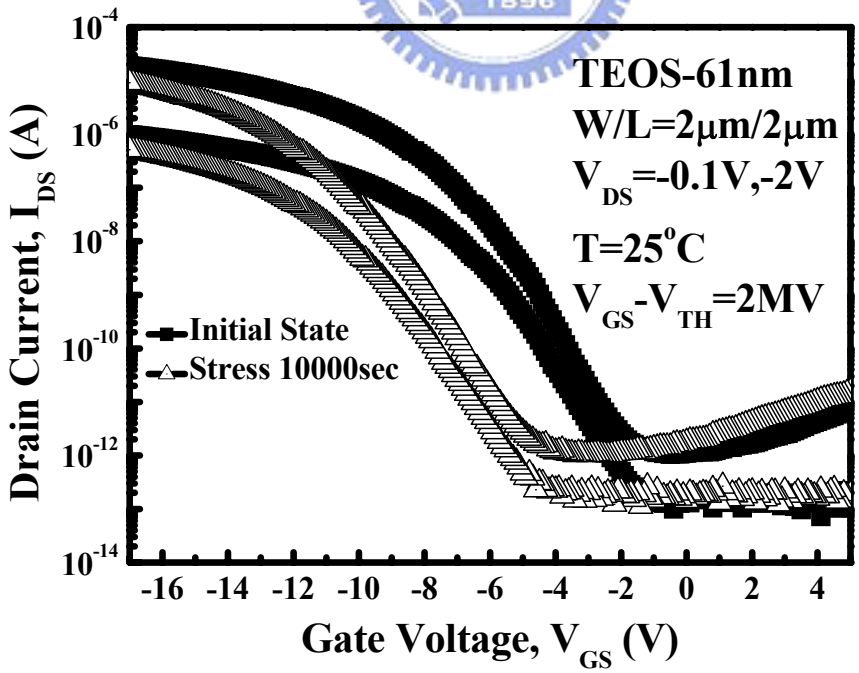


Figure 3-20 **The transfer characteristics of the LTPS TFTs under NBTI stress with initial state and 10000sec., respectively. The stress was performed at 25°C**

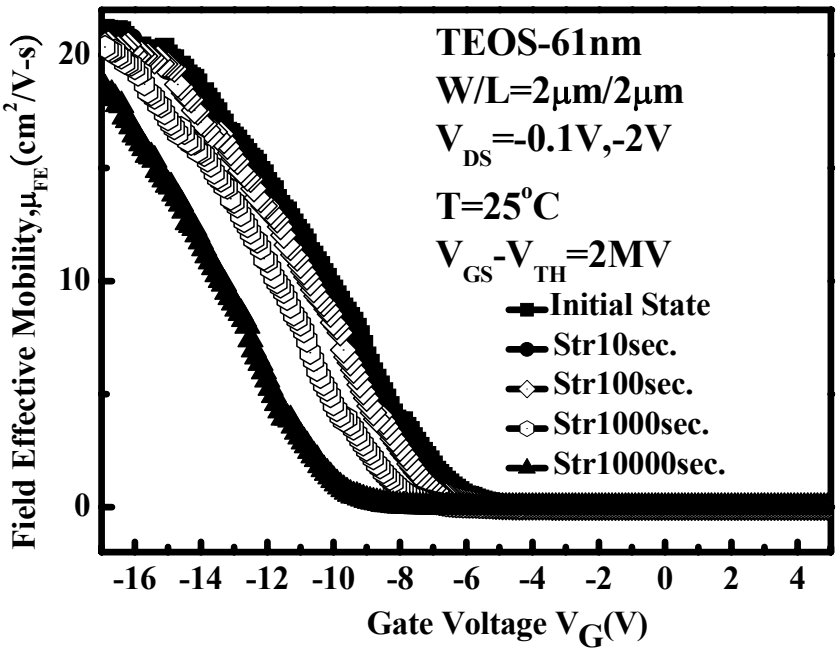


Figure 3-21 Mobility degradation with different stress time. The stress was performed at 25°C

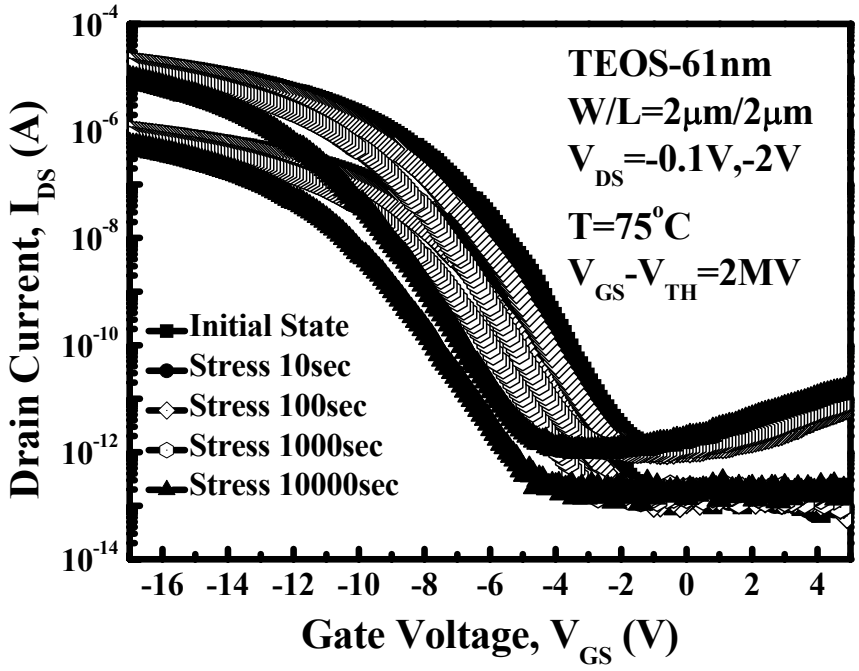


Figure 3-22 The transfer characteristics of the LTPS TFTs under NBTI stress with different stress time, respectively. The stress was performed at 75°C

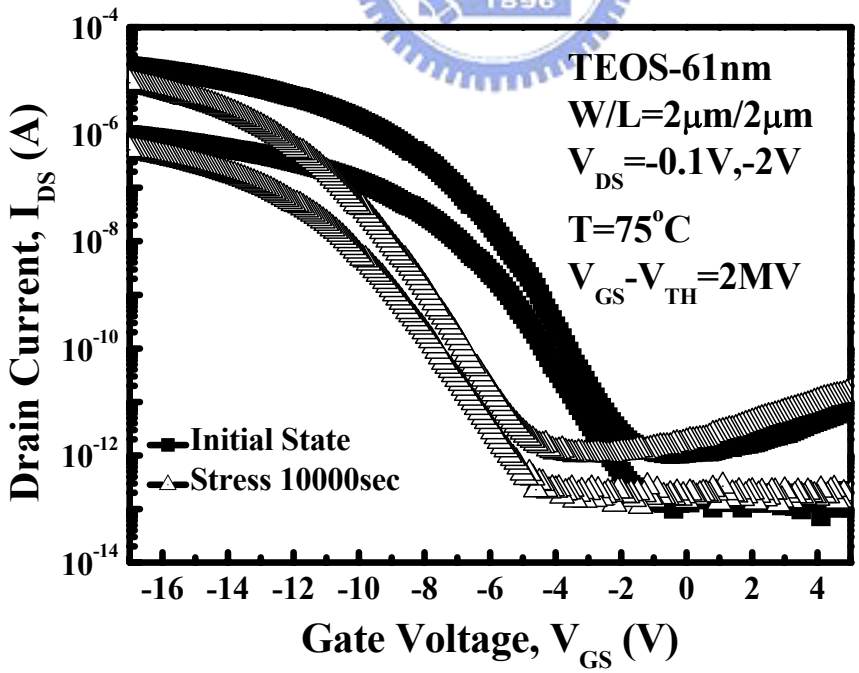


Figure 3-23 The transfer characteristics of the LTPS TFTs under NBTI stress with initial state and 10000sec., respectively. The stress was performed at 75°C

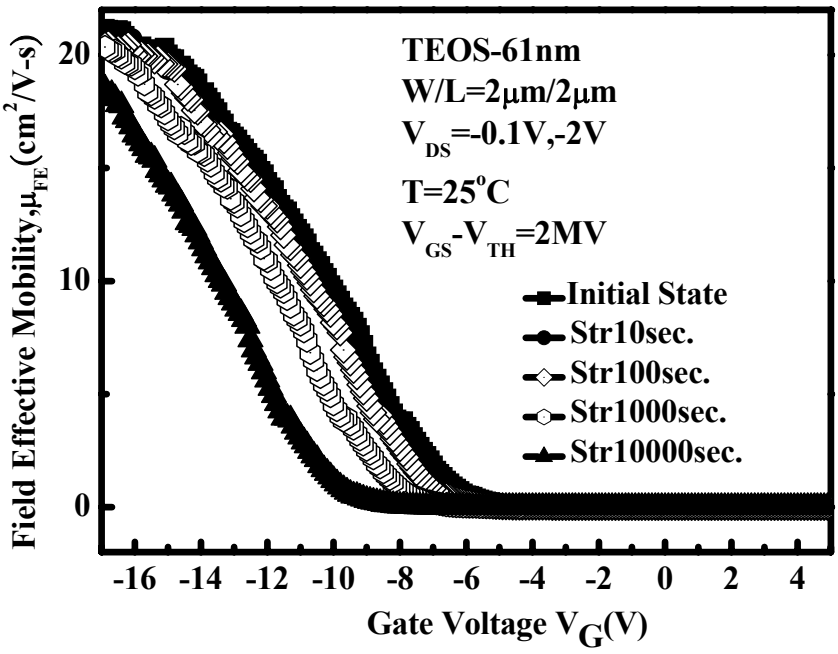


Figure 3-24 Mobility degradation with different stress time. The stress was performed at 75°C

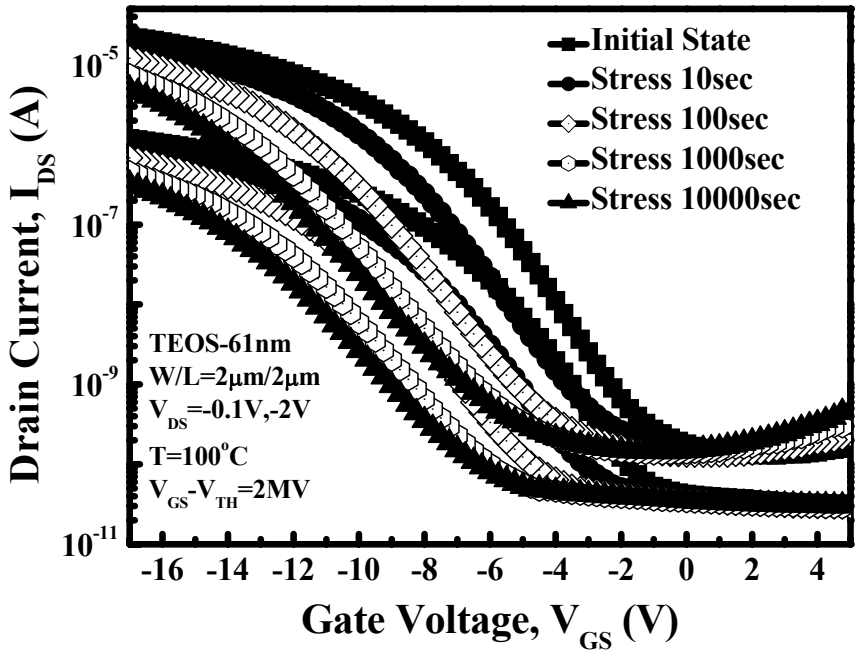


Figure 3-25 The transfer characteristics of the LTPS TFTs under NBTI stress with different stress time, respectively. The stress was performed at 100°C

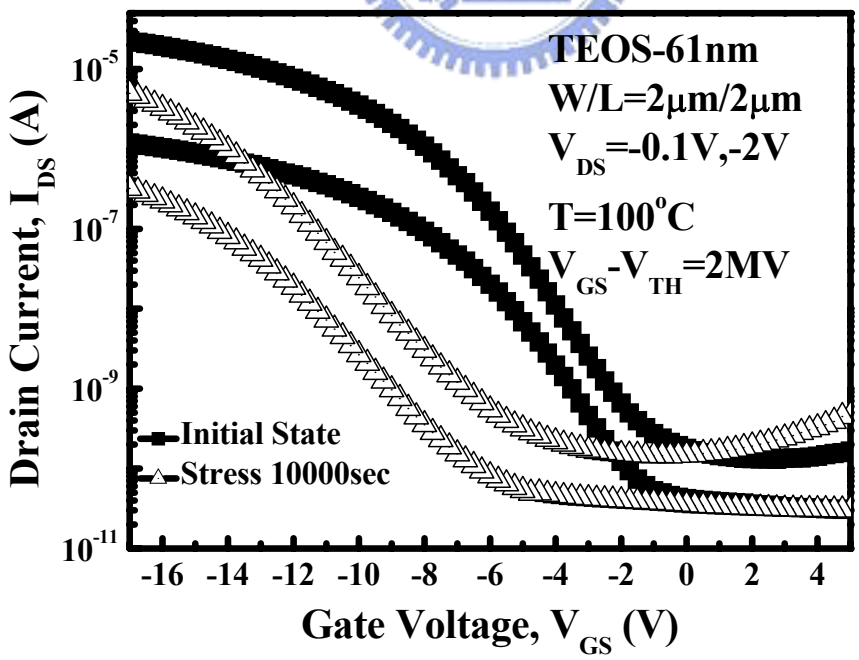


Figure 3-26 The transfer characteristics of the LTPS TFTs under NBTI stress with initial state and 10000sec., respectively. The stress was performed at 100°C

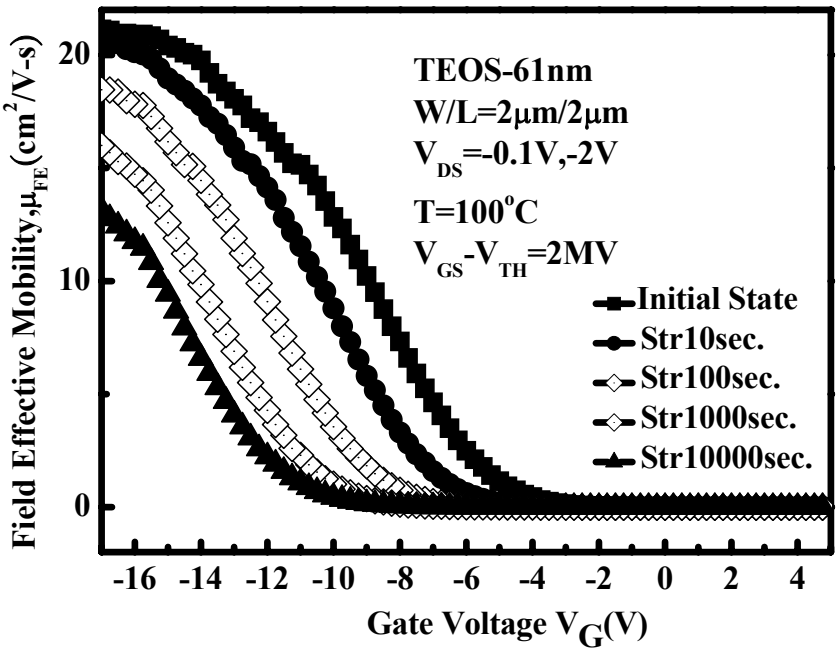


Figure 3-27 Mobility degradation with different stress time. The stress was performed at 100°C

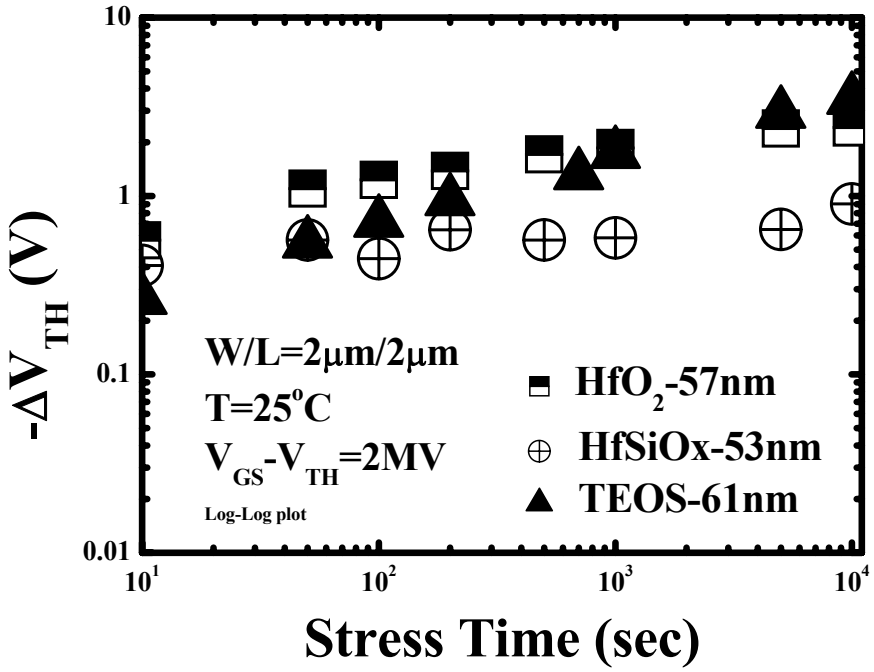


Figure 3-28 Dependence of the threshold-voltage shift on the stress time at 25°C.

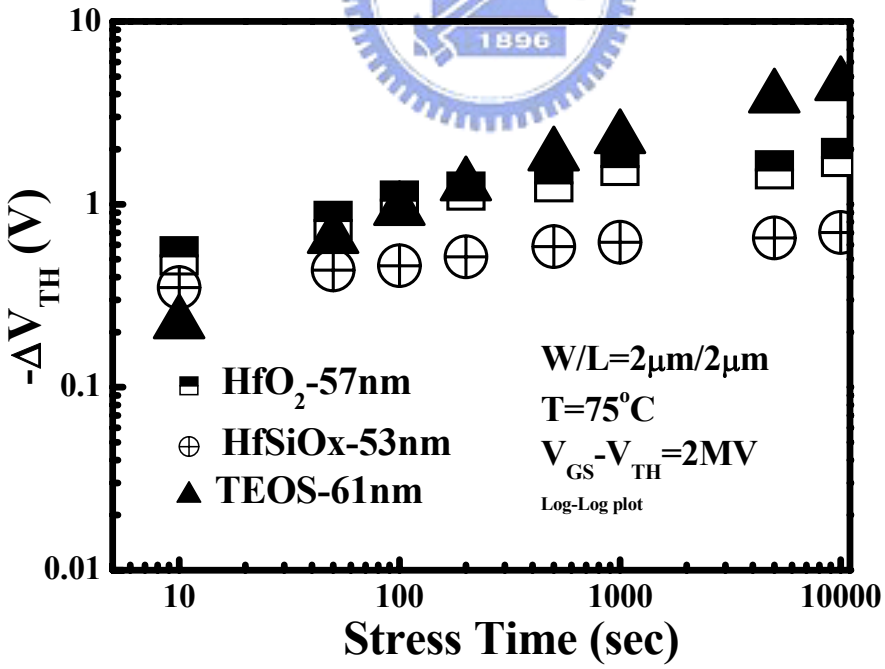


Figure 3-29 Dependence of the threshold-voltage shift on the stress time at 75°C.

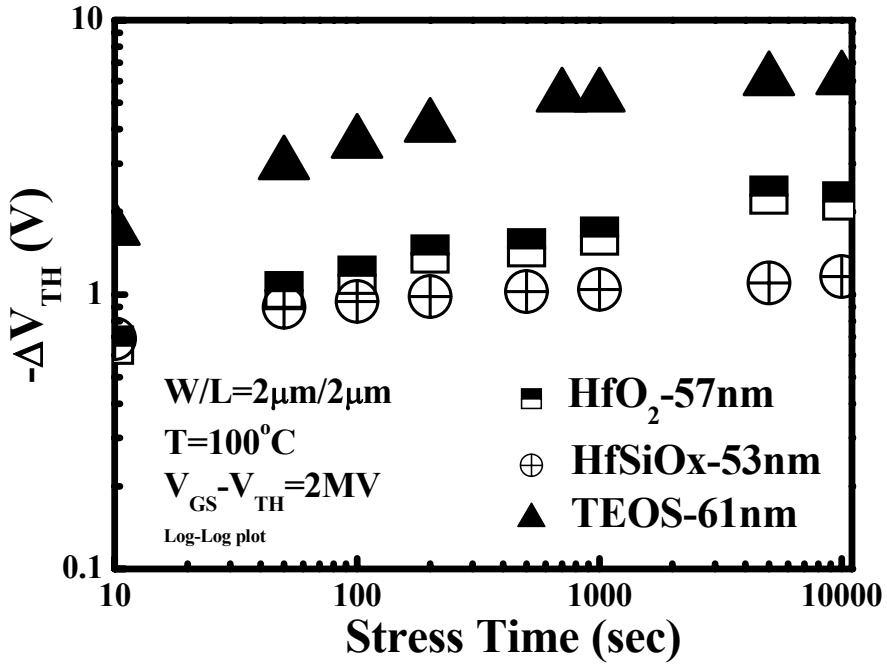


Figure 3-30 Dependence of the threshold-voltage shift on the stress time at 100°C.

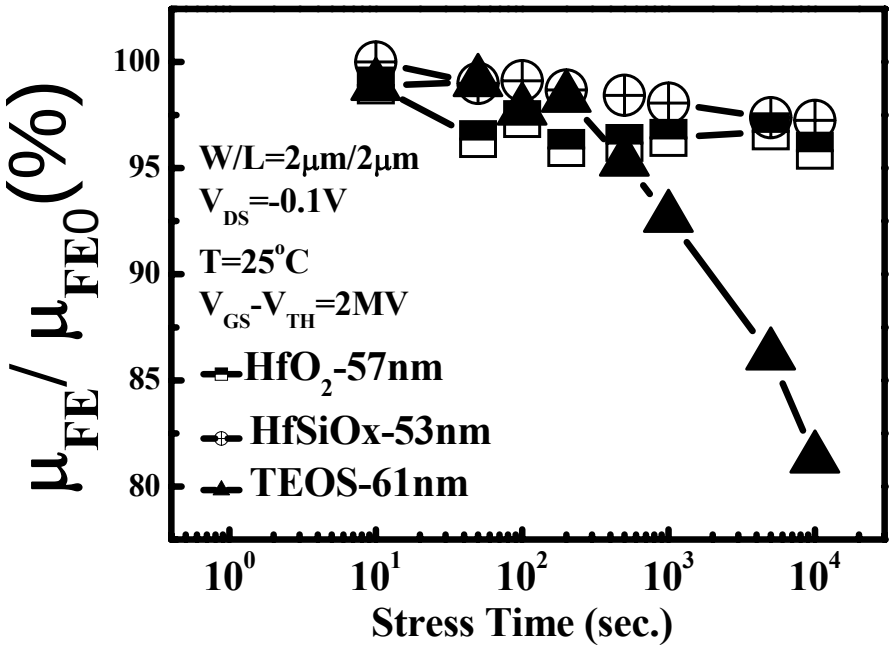


Figure 3-31 Dependence of the field-effective mobility degradation on the stress time at 25°C.

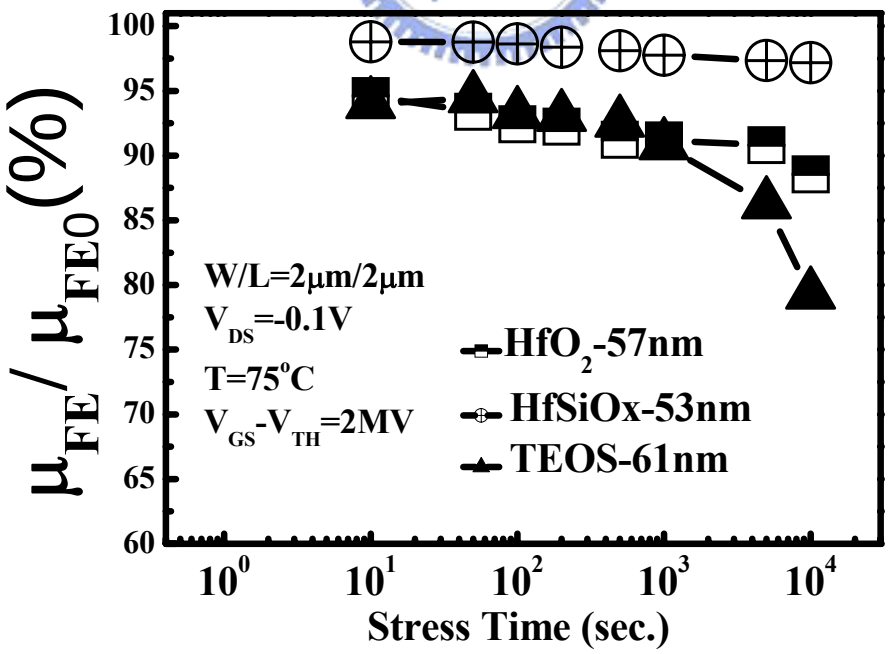


Figure 3-32 Dependence of the field-effective mobility degradation on the stress time at 75°C.

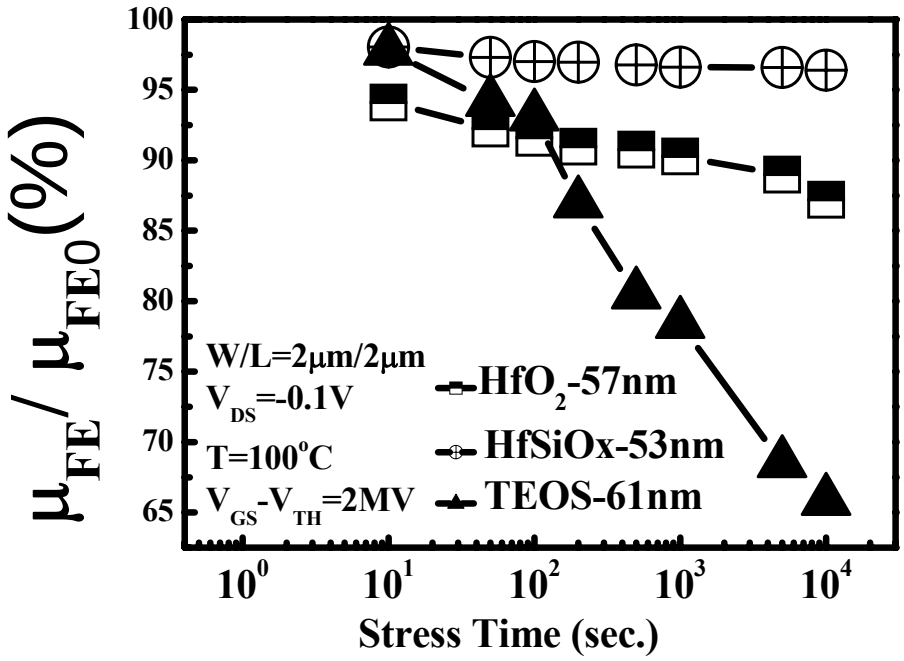


Figure 3-33Dependence of the field-effective mobility degradation on the stress time at 100°C.

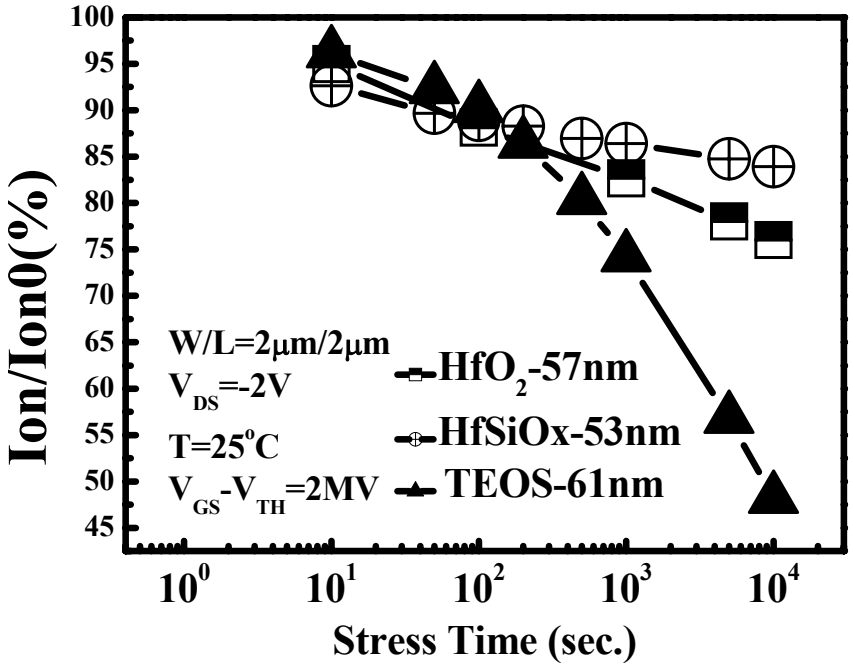


Figure 3-34 Dependence of the on current degradation on the stress time at 25°C.

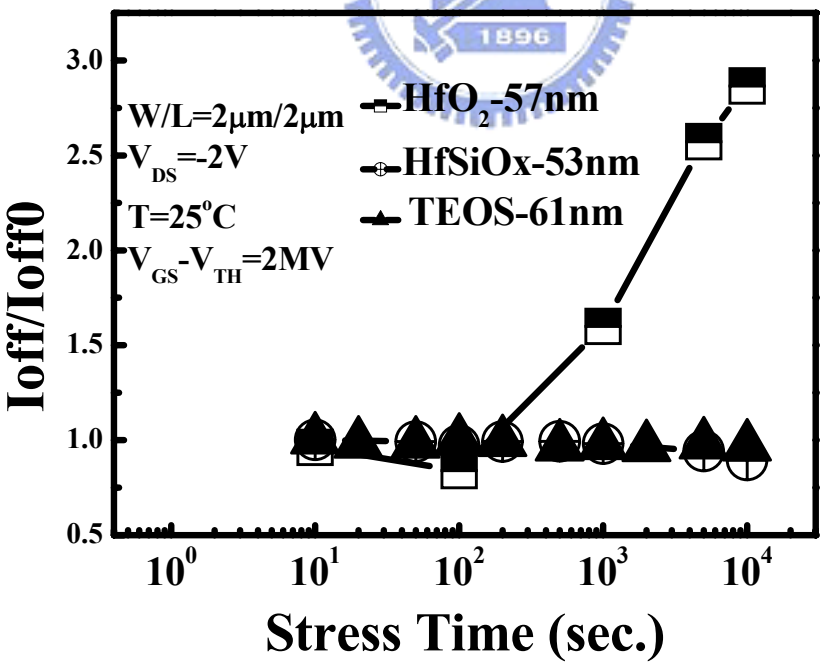


Figure 3-35 Dependence of the off current degradation on the stress time at 75°C

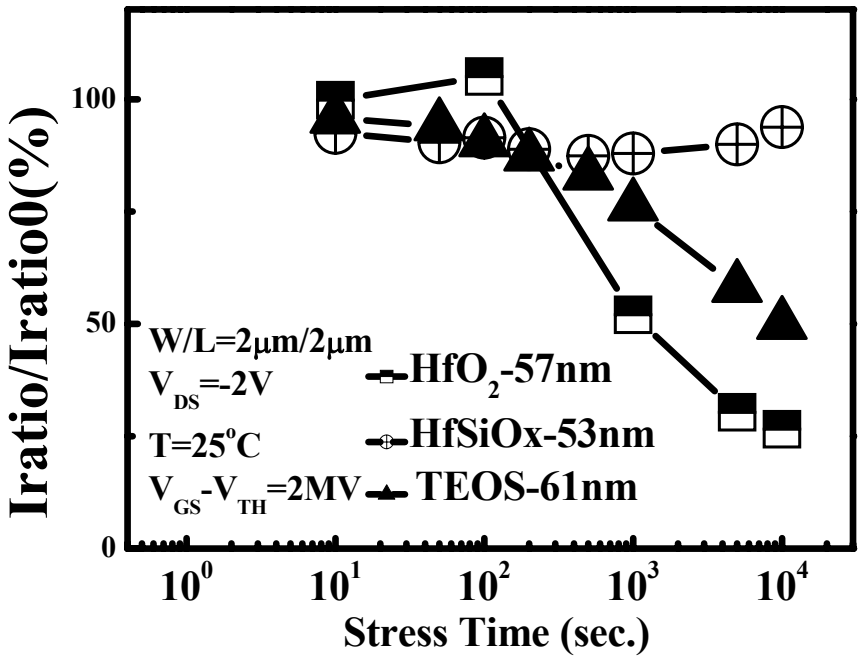


Figure 3-36 Dependence of the current ratio degradation on the stress time at 25°C

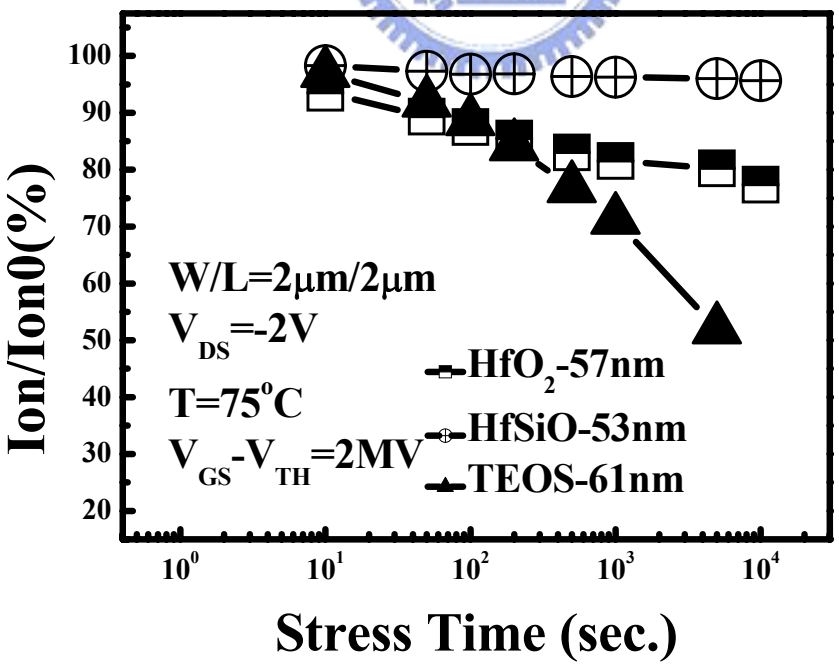


Figure 3-37 Dependence of the on current degradation on the stress time at 75°C.

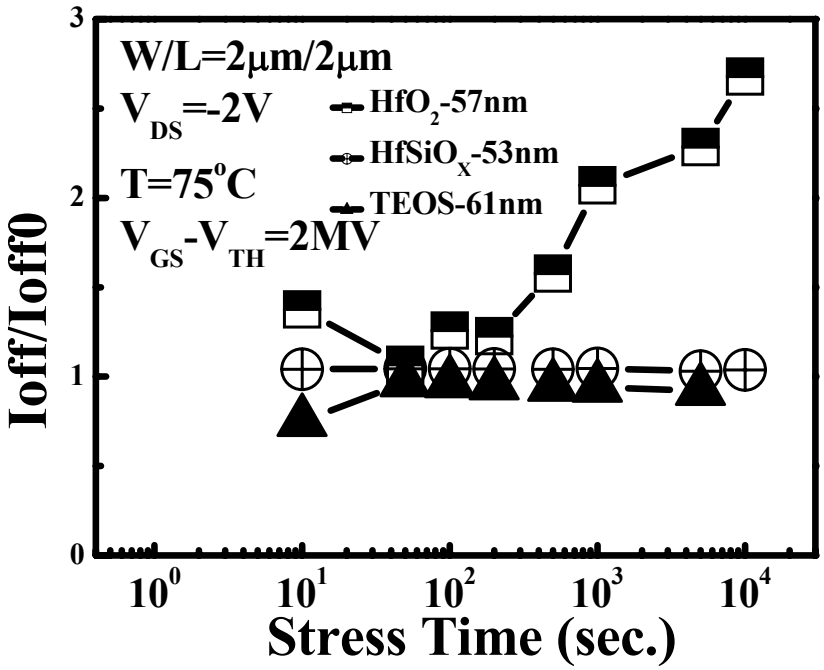


Figure 3-38 Dependence of the off current degradation on the stress time at 75°C

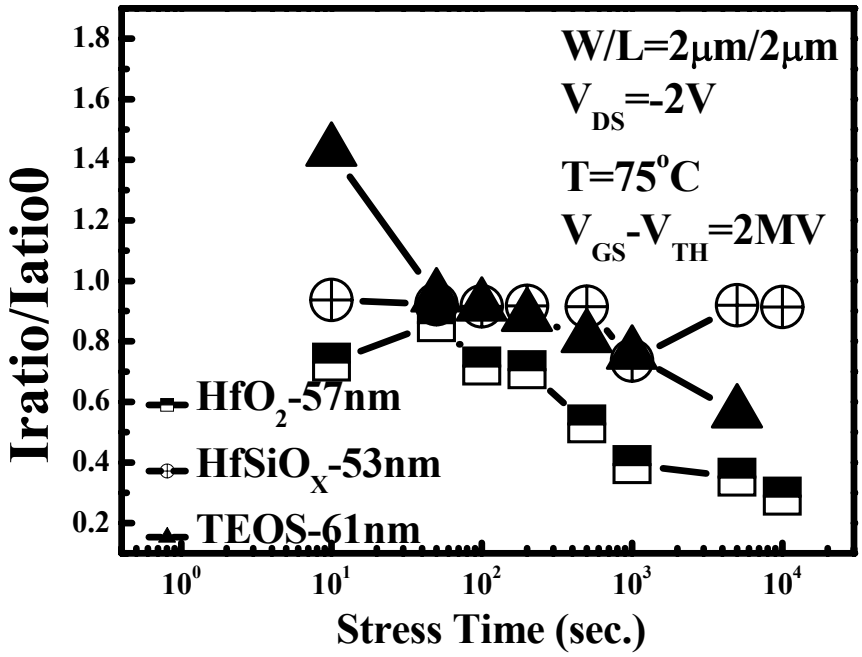


Figure 3-39 Dependence of the current ratio degradation on the stress time at 75°C

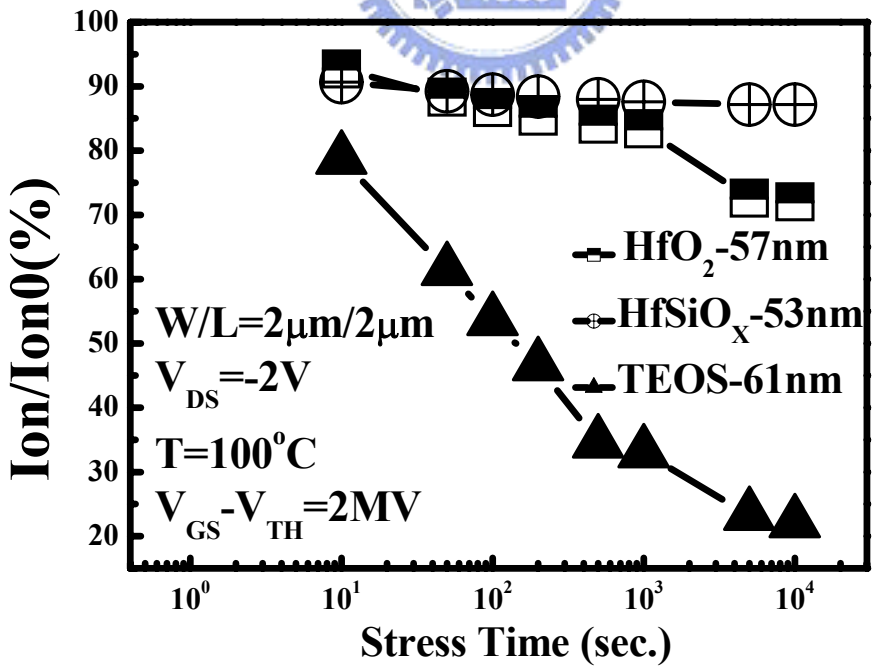


Figure 3-40 Dependence of the on current degradation on the stress time at 100°C.

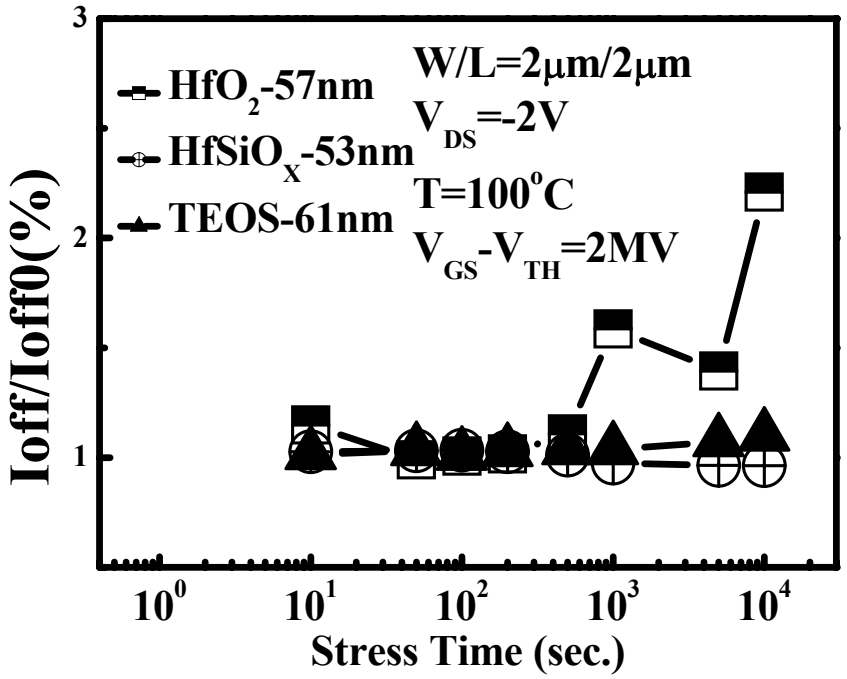


Figure 3-41 Dependence of the off current degradation on the stress time at 100°C.

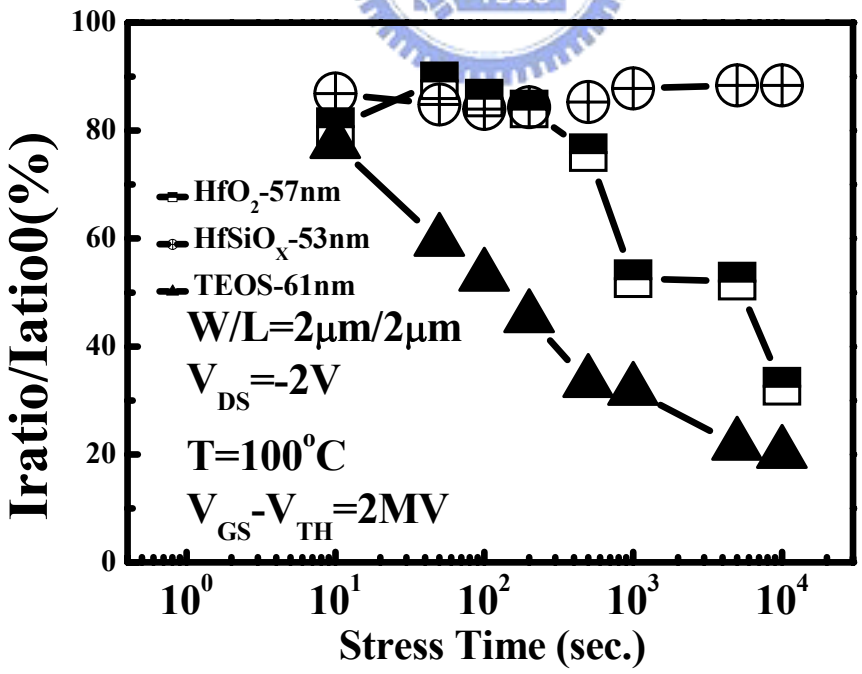


Figure 3-42 Dependence of the current ratio degradation on the stress time at 100°C

Chaprer4 Conclusion and Summary

4.1 Conclusion

High performance p-channel poly-Si TFTs using hafnium base high-k dielectric including hafnium oxide (HfO_2) and hafnium silicate ($HfSiO_X$) are demonstrated using low-temperature processing. The conventional oxide was prepared by LPCVD with tetra-ethyl-oxy-silane (TEOS) precursor at 700°C to serve as the control samples. The result and discussion are concluded and summarized as follows.

4.1.1 Electrical Properties

Higher I_{on}/I_{off} current ratio, smaller subthreshold swing, lower threshold voltage and higher mobility than those with conventional deposited-SiO_2 gate dielectric are achieved.

It can be seen that the crystalline temperature of $HfSiO_x$ film is higher than HfO_2 and which is conducive to a smoother surface at both the top and bottom interfaces.

Due to the lower density of states in the Poly-Si channel and the higher capacitance density, the High-k dielectric TFTs exhibit the lower threshold voltage, lower subthreshold swing and less threshold voltage roll-off than TEOS oxide TFTs.

The off-state current of HfO_2 TFTs increase more rapidly in small drain voltage (VDS=-0.1V) that is due to the activation energy decrease fastest, TAT enhance drain leakage current and FP emission due to higher field near the drain side.

However, the field-effective mobility of HfO_2 TFTs is lowest due to the additional Coulomb scattering caused by the plentiful charges exsited in the HfO_2 dielectric.

4.2 Reliability

For negative bias stress and negative bias temperature instability, the $HfSiO_X$ TFTs depicts the best stability due to its lower density of state, better film quality of low temperature and the better gate dielectrics/poly-Si interface quality. Our results suggest that $HfSiO_x$ is a potential candidate for the gate-dielectric material of future high-performance poly-Si TFTs.

Reference:

[1] O. K. Weimer. in IRE-AIEE Solid State Device Research Conference: Stanford University, 1961.

[2] O. K. Weimer, *Proc. IRE 50*, pp. 1462, 1962.

[3] T. Yamanaka, T. Hashimoto, N. Hasegawa, T. Tanaka, N. Hashimoto, A. Shimizu, N. Ohki, K. Ishibashi, K. Sasaki, T. Nishida, T. Mine, E. Takeda and T. Nagano, " Advanced TFT SRAM cell technology using a phase-shift lithography," *IEEE Trans. Electron Devices*, vol. 42, no. 7, pp. 1305-1313, 1995.

[4] T. P. Brody, "The thin film transistor-A late flowering bloom," *Electron Devices, IEEE Transactions on*, vol. 31, pp. 1614-1628, 1984.

[5] W. G. Hawkins, "Polycrystalline-silicon device technology for large-area electronics," *IEEE Trans. Electron Devices*, vol. 33, pp. 477-481, 1986.

[6] H. Kuriyama *et al.*, "Enlargement of poly-Si film grain size by excimer laser annealing and its application to high-performance poly-Si thin film transistor," *Jpn. J. Appl. Phys.*, vol. 30, pp. 3700-3703, 1991.

[7] A. Nakamura, F. Emoto, E. Fujii and A. Tamamoto, "A high-reliability, low-operation-voltage monolithic active-matrix LCD by using advanced solid-phase growth technique," in *IEDM Tech. Dig.*, pp.847, 1990.

[8] G. K. Guist, and T. W. Sigmon, "High-performance laser-processed polysilicon thin-film transistors," *IEEE Electron Device Letters*, vol. 20, no. 2, pp. 77-79, 1999.

[9] S. Y. Yoon, K. Hyung, C. O. Kim, J. Y. Oh and J. Jang, "Low temperature

metal induce crystallization of amorphous silicon using a Ni solution," *J. Appl. Phys.*, vol. 82, pp. 5865-5867, 1997.

[10] S. W. Lee and S. K. Joo, "Low temperature poly-Si thin-film transistor fabrication by metal-induced lateral crystallization," *IEEE Electron Device Letters*, vol. 17, pp. 160-162, 1996.

[11] A. Yin, and S. J. Fonash, "High-performance p-channel poly-Si TFT's using electron cyclotron resonance hydrogen plasma passivation," *IEEE Electron Device Letters*, vol. 15, no. 12, pp. 502-503, 1994.

[12] C. K. Yang, T. F. Lei, C. L. Lee, "The combined effects of low pressure NH3 annealing and H2 plasma hydrogenation on polysilicon thin-film-transistors," *IEEE Electron Device Letters*, vol. 15, pp. 389-390, 1994.

[13] J. W. Lee, N. I. Lee, J. I. Kan, C. H. Han, "Characteristics of polysilicon thin-film transistor with thin-gate dielectric grown by electron cyclotron resonance nitrous oxide plasma," *IEEE Electron Device Letters*, vol. 18, pp. 172-174, 1997.

[14] K. C. Moon, J. H. Lee, M. K. Han, "Improvement of polycrystalline silicon thin film transistor using oxygen plasma pretreatment before laser crystallization," *IEEE Trans. Electron Devices*, vol. 49, pp. 1319-1322, 2002.

[15] T. Unagami and O. Kogure, "Large on/off current ratio and low leakage current poly-Si TFTs with multichannel structure," *IEEE Trans. Electron Devices*, vol. 35, no. 11, pp. 1986-1989, 1988.

[16] B. H. Min, C. M. Park and M. K. Han, "A novel offset gated polysilicon thin film transistor without an additional offset mask," *IEEE Electron Device Letters*, vol. 16, no. 5, pp. 161-163, 1995.

[17] Z. Xiong, H. Liu, C. Zhu and Sin, J.K.O., "Characteristics of high-K spacer offset-gated polysilicon TFTs," *IEEE Trans. Electron Devices*, vol. 51, no. 8,

pp. 1304-1308, 2004.

[18] P. S. Shih, C. Y. Chang, T. C. Chang, T. Y. Huang, D. Z. Peng and C. F. Yeh, "A novel lightly doped drain polysilicon thin-film transistor with oxide sidewall spacer formed by one-step selective liquid phase deposition," *IEEE Electron Device Letters*, vol. 20, no. 8, pp. 421-423, 1999.

[19] K. Y. Choi and M. K. Han, "A novel gate-overlapped LDD poly-Si thin-film transistor," *IEEE Electron Device Letters*, vol. 17, no. 12, pp. 566-568, 1996.

[20] H. C. Lin, C.-M Yu, C.-Y. Lin, K.-L.Yeh, T. Y. Huang and T. F. Lei, "A novel thin-film transistor with self-aligned field induced drain," *IEEE Electron Device Letters*, vol. 22, no. 1, pp. 26-28, 2001.

[21] C. S. Lai, C. L. Lee, T. F. Lei and H. N. Chern, "A novel vertical bottom-gate polysilicon thin film transistor with self-aligned offset," *IEEE Electron Device Letters*, vol. 17, no. 5, pp. 199-201, 1996.

[22] Shen-De Wang, "Study on Fluorine Passivation Techniques and the Reliability for Low Temperature Polycrystalline Silicon Thin-Film Transistors" NCTU 博士論文 , September 2005.

[23] E. P. Gusev, V. Narayanan, M. M. Frank, "Advanced high-k dielectric stacks with poly-Si and metal gates: Recent progress and current challenges." IBM, 2006.

[24] Z. Jin, H. S. Kwok, and M. Wong, "High-performance polycrystalline SiGe thin-film transistors using Al_2O_3 gate insulators," *Electron Device Letters, IEEE*, vol. 19, pp. 502-504, 1998.

[25] B. F. Hung, K. C. Chiang, C. C. Huang, A. Chin, and S. P. McAlister, "High-performance poly-silicon TFTs incorporating $LaAlO_3$ as the gate dielectric," *Electron Device Letters, IEEE*, vol. 26, pp. 384-386, 2005.

[26] K. H. Lee, J. K. Park, and J. Jang, "A high-performance polycrystalline silicon thin film transistor with a silicon nitride gate insulator," *Electron Devices, IEEE Transactions on*, vol. 45, pp. 2548-2551, 1998.

[27] I.-W. Wu, T.-Y. Huang, W. B. Jackson, A. G. Lewis, and A. Chiang, "Passivation kinetics of two types of defects in polysilicon TFT by plasma hydrogenation," *Electron Device Letters, IEEE*, vol. 12, pp. 181-183, 1991.

[28] T. Yamaguchi, R. Iijima, T. Ino, A. Nishiyama, H. Satake, and N. Fukushima, "Additional scattering effects for mobility degradation in Hf-silicate gate MISFETs," presented at Electron Devices Meeting, 2002. IEDM '02. Digest. International, 2002.

[29] M. Gurfinkel, J. S. Suehle, J. B. Bernstein, and Yoram. Shapira, "Enhance Gate Induced Drain Leakage Current in HfO_2 MOSFETs due to Remote Interface Trap-Assisted Tunneling ", presented at Electron Devices Meeting, 2006. IEDM '06. Digest. International, 2006.

[30] C. F. Yeh, S. S. Lin, T. Z. Yang, C. L. Chen, and Y. C. Yang, "Performance and Off-State Current Mechanisms of Low-Temperature Processed Polysilicon Thin-Film Transistors with Liquid Phase Deposited SiO_2 Gate Insulator", *IEEE Trans. on Electron Devices*, vol. 41, no. 2, pp. 173–179, February 1994.

[31] C. T. Angelis, C. A. Dimitriadis, I. Samaras, J. Brini and G. Kamarinos, V. K. Gueorguiev, and Tz. E. Ivanov, "Study of leakage current in n-channel and –channel polycrystalline silicon thin-film transistors by conduction and low frequency noise measurements", *J. Appl. Phys.*, 82(8), 15 October 1997.

[32] M. Hack, I-W. Wu, T. J. King and A. G. Lewis, "Analysis of Leakage Currents in Poly-Silicon Thin Film Transistors", *IEDM Technical Digest*, pp.385, 1993.

[33] M. Yazaki, S. Takenaka, and H. Ohshima, "Conduction Mechanism of Leakage

Current Observed in Metal-Oxide-Semiconductor Transistors and Poly-Si Thin-Film Transistors", *Jpn. J. Appl. Phys.*, vol. 31, no. 2A, pp. 206-209, February 1992.

[34] Shunji Seki, Osamu Kogure, and Bunjiro Tsujiyama, "Effect of crystallization on trap state densities at grain boundaries in polycrystalline silicon", *Electron Device Letters, IEEE*, vol. 8, no. 8, pp. 368-370, August 1987.

[35] T. J. King, M. G. Hack, and I-Wei Wu, "Effective density-of-states distributions for accurate modeling of polycrystalline silicon thin-film transistors", *J. Appl. Phys.*, vol. 75, no. 2, pp. 908-913, January 1994.

[36] B. A. Khan, R. Pandya, "Activation-energy of source-drain current in hydrogenated and unhydrogenated polycrystalline thin-film transistors", *IEEE Trans. on Electron Devices.*, vol. 37, pp. 1727-1734, 1990.

[37] I. W. Wu, T. Y. Huang, W. B. Jackson, A. G. Lewis and A. C. Chiang, "Passivation kinetics of two types of defects in polycrystalline thin-film transistors by plasma hydrogenation ", *Electron Device Letters, IEEE*, vol. 12, pp. 181-183, 1991.

[38] N. A. Hastas, C. A. Dimitriadis, and G. Kamarions, "Effect of interface roughness on gate bias instability of polycrystalline silicon thin-film transistors", *J. Appl. Phys.*, vol. 92, no. 8, pp. 4741-4745, October 2002.

[39] Dieter K. Schroder, Jeff A. Babcock, "Applied Physics Reviews-Focused Review;Negative bias temperature instability: Road to cross in deep submicron silicon semiconductor manufacturing", *J. Appl. Phys.*, vol. 94, no. 1, pp. 1-18, July 2003.