Chapter 4

Flip-Chip Light-Emitting-Diodes with Textured Micro Pillar Arrays (MPAFC-LEDs)

4-1 Fabrication of MPAFC-LEDs

4-1.1 Process procedure

The GaN LED structure with dominant wavelength at 460 nm used in this study is grown by metal-organic chemical vapor deposition (MOCVD) on c-plane sapphire substrates. The LED structure consists of a 2-µm-thick undoped GaN layer, a 2-µm-thick highly conductive n-type GaN layer, a 0.2-µm-thick InGaN/GaN MQW, a 0.2-µm-thick p-type GaN layer and n InGaN/GaN short period super-lattice (SPS) tunneling contact layers for indium-tin-oxide (ITO).

Figure 4-1 shows the fabrication steps of flip-chip GaN LEDs with micro-pillar-arrays. Top-emitting LEDs with a size of 1000 μ m × 1000 μ m are fabricated using standard photolithography and BCl₃/Cl₂ inductively coupled plasma (ICP) etching for current isolation purposes. The p-GaN and active layers are partially etched by an ICP etcher to expose an n-GaN layer for electrode formation. A indium-tin-oxide of 250 nm is deposited on p-GaN layer as the transparent conductive layer. The samples are then annealed at 500°C for 10 minutes in air. The Cr/Pt/Au (50 nm/50 nm/2500 nm) metals are deposited for the p-and n-contact pads. After completing the conventional face-up LED structure, the sapphire is ground to let sapphire thickness become 100 μ m. The Ni metal of 500 nm is deposited onto the bottom side of sapphire substrate as the dry etching mask layer. The sample is then subjected to the ICP process using Cl₂/BCl₃ (10 sccm/30 sccm) plasma with an

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ICP power of 850 W and RF power of 400 W to form the micro pillar arrays for light extraction purpose. The ICP etching rate for the sapphire is approximately 800 Å/min. The processed LED wafer is subjected to the laser scribed and broken into 1000 μ m × 1000 μ m chips.

As for the silicon sub-mount preparation, the Ti/Al (500 Å /2000 Å) metals are deposited onto the silicon sub-mount as a mirror. Secondly, the SiO₂ film of 800 Å is deposited onto it as a passivation. The Au metal of 2 μ m is deposited for n and p bonding pad. The silicon sub-mount is subjected to stud bump process. Figure 4-2 (a) and (b) show the top view and side view images of the silicon sub-mount before flip-chip bonding. Finally, the chips are flip-chip bonded on silicon sub-mount using Panasonic ultra sonic flip chip bonder for electrical and optical measurement as shown in figure 4-3.

4-1.2 SEM images of micro pillar arrays

The surface morphology of a FC-LED with micro pillar-array sapphire surface is examined by scanning electron microscope as shown in figure 4-4. The periodic distance for pillar-array is about 5.5 μ m with the depth of the pillar between ~1.1 μ m and 3.2 μ m. Furthermore, the bevel angle of pillar is changed from 8° to 35° with increasing dry etching time. In attempt to verify the effect of micro pillar array surface on light extraction efficiency, the various depths and bevel angle of pillar is formed for further comparison. Figure 4-4 (a)~(b) show the rather smooth top surface and side wall and the inset is the cross view of one micro pillar. With the increase of the dry etching time, the surface of micro pillar becomes rougher and the bigger bevel angle is obtained as shown in figure 4-4 (c). Even the pineapple like textured pillar surface is obtained as shown in figure 4-4 (d). The results may be ascribed to the

uniformity of Ni hard mask, which results in partial over etching and the uneven pillar surface.

4-2 Characteristics of MPAFC-LEDs

4-2.1 L-I-V measurement and efficiency enhancement

The LED chips are packaged into TO can without epoxy resin for the subsequent measurement. The light-current-voltage (L-I-V) characteristics are measured using a high current measure unit (KEITHLEY 240). The light output power of the flip-chip LEDs are measured using an integrated sphere with a calibrated power meter. The corresponding I-V characteristics of flat surface FC-LEDs and micro-pillar-array FC-LEDs (MPAFC-LEDs) are also measured respectively as shown in figure 4-5. It is found that the I-V curve of MPAFC-LEDs present a normal p-n diode behavior with a forward voltage (@ 350 mA) of 3.4 V, indicating that there is no heating and charging damages for the fabrication process of micro-pillar-array during ICP etching process.

The light output power-current characteristics of the flat FC-LEDs and MPAFC-LEDs are shown in figure 4-6. We clearly observed that the output powers of the MPAFC-LEDs are larger than those of the flat FC-LEDs. At an injection current of 350 mA, it is found that the MQW emission peaks of those devices are located at about 460nm, and the light output powers of the flat FC-LEDs, 1.1 µm, 1.8 µm, 2.7 µm and 3.2 µm depth of the MPAFC-LEDs are about 151, 165, 179, 227 and 252mW, respectively. Figure 4-7 shows the light extraction efficiency enhancement of MPAFC-LEDs with various depth of pillar is 10%~68% at 350 mA current injection compared to a conventional flat surface FC-LED. It is indicated that the textured sapphire surface reduces the total internal reflection and improves the probability of photons escaping from

semiconductor to air. Furthermore, with the increase of pillar depth (1.1 μ m~3.2 μ m) and bevel angle (8°- 35°), the light output power of 3.2 μ m MPAFC-LED [figure 4-4 (d)] is increased by 55% compared to the 1.1 μ m MPAFC-LED [figure 4-4 (a)] under 350mA current injection. These results can be attributed to the increase of the effective surface areas by increasing the depth and bevel angle of micro disk.

Figure 4-8 (a) and (b) shows the images of conventional flat surface FC-LED and MPAFC-LED under 350 mA current injection. Intensity distributions are also shown. The EL intensities observed from the MPAFC-LED clearly exceeded those from the conventional flat FC-LED under the same current injection, especially on the FC-LED top surface. The improved light extraction efficiency can be further supported by the beam view analysis results.

Obviously, the results indicate that the sapphire substrate with micro-pillar-array surface reduces the internal light reflection and increases the light extraction efficiency. The probability of light escaping from the sapphire to air is increased due to the increase of escape cone by micro-pillar-array structure [23]. Such an enhancement can be attributed to the top surface roughness and the fact which photons are more likely to be emitted from the surface-roughed device, resulting in an increase of the light output power of the MPAFC-LED.

4-2.2 Monte-Carlo ray-tracing calculations

In order to investigate the fundamental of enhancement of light output with different etching time of MPAFC-LEDs, we used the commercial ray-tracing software employing the Monte-Carlo algorithm to obtain trajectory of

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ray-tracing, enhancement efficiency and spatial intensity distributions of radiometric and photometric data.

The simulated structure and properties of FC-LEDs are shown in figure 4-9 and table 4-1, respectively. Table 4-1 (a) shows the material variable of the models, and table 4-1 (b) shows the surface variable of the models. The wavelength and temperature in this simulation are 460 nm and 300 K, respectively. Figure 4-9 (a) shows the structure of the simulated models, and figure 4-9 (b) shows the models in the TracePro software. The epitaxial layer is not clear in the figure 4-9 (b). Figure 4-9 (c) is a sketch of the pattern on the backside surface of the sapphire substrate. The circles in the figure 4-9 (c) represent micro-pillar-array in these models. The distance of the center of the micro-pillar-array is about 5.5 µm and the simulated models which are similar to the geometric pattern of micro pillar structure as shown in figure 4-4 (a)~(d) are designed.

The solid model is built up with combing the simple solid objects and each semiconductor layers adjoin to the others. Light rays are generated in the active layer with a uniform random distribution. Monochromatic radiation with the peak wavelength of the measured spectral emission (460 nm) is used in the simulation.

Figure 4-10 (a) and (b) shows the irradiance maps of conventional flat FC-LEDs and 3.2 μ m MPAFC-LEDs, respectively. The intensity of 3.2 μ m MPAFC-LEDs clearly exceeds that of conventional flat FC-LEDs conforming to figure 4-8 (a) and (b).

The output power versus different depth of micro-pillar-array simulating with TracePro software can be obtained from the irradiance maps. Therefore, the enhancement efficiency can be calculated and it is found that the efficiency

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is increased by larger heights of micro-pillar-array as shown in figure 4-11. The simulated results are similar to experiment performance except 3.2 um point because the simulated model doesn't consider the further enhancement due to nano roughness of micro-pillar-array sidewalls. Consequently, the improved light extraction efficiency can be further supported by the simulation data as shown in figure 4-11.





Figure 4-1 Schematic of fabrication steps of GaN LEDs with micro-pillar-arrays



Figure 4-2 Scanning electron micrographs (SEM) images of Si sub-mount before flip chip bonding. (a) Top view and (b) Side view.



Figure 4-3 SEM image of a chip bonding on the Si sub-mount.





Figure 4-4 SEM images of micro-pillar-array surface of sapphire backside with various depth and bevel angle. (a) 1.1 μ m MPA, (b) 1.8 μ m MPA, (c) 2.7 μ m MPA, and (d) 3.2 μ m MPA.



Figure 4-5 The current-voltage (I-V) characteristics of flat surface FC-LEDs



Figure 4-6 The light output power-current (L-I) curves of flat surface FC-LEDs and MPAFC-LEDs.



Figure 4-7 Light extraction enhancement of experimental results versus different depth of MPA.



Figure 4-8 Photons of (a) conventional flat surface FC-LED and (b) micro pillar-array FC-LED at a dc injection current of 350 mA.

(a)

	thickness	index
sapphire	100 µm	1.7
n-GaN	4 µm	2.45
MQW	0.2 µm	2.65
p-GaN	0.2 µm	2.45
ITO	0.2 μm	2



(b)

	reflectance	transmission	absorptance
Al mirror	90%	0%	10%
p-pad	50%	0%	50%
n-pad	50%	0%	50%

Table 4-1 (a) shows the material variable of the models and (b) shows the surface variable of the models.

(a)



(b)





(C)

Figure 4-9 (a) shows the structure of the simulated models, (b) shows the models in the TracePro software, and (c) is a sketch of the pattern on the backside surface of the sapphire substrate.

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(a)

(b)



Figure 4-10 The simulation results by Monte-Carlo ray-tracing. (a) and (b) show the irradiance maps of conventional flat FC-LEDs and 3.2 μ m MPAFC-LEDs, respectively.



Figure 4-11 Light extraction enhancement comparison of experimental and simulation results versus different depth of MDA.