Chapter 1

Introduction

1.1 General Background

In 1967, D. Kahng and S. M. Sze invented the floating-gate (FG) nonvolatile semiconductor memory (or flash memory) at Bell Labs [1.1]. The stacked-gate FG device structure is shown in Figure1-1. Flash memory cells provide single-cell electrical program and fast simultaneous block electrical erase. The operation principal of conventional Flash memory is using the polycrystalline silicon as floating gate to be the charge stored units. After electrons which injected from the channel stored in floating gate, the threshold voltage of devices will be changed. The logical "0" and "1" definition of nonvolatile memory devices are used for the difference between threshold voltages. The invention of flash memory creates a huge industry of portable electronic devices such as digital cameras, MP3 players, personal digital assistants (PDA), mobile phones, and external data storage devices for personal computers, USB Flash personal disc ,etc., and play an important role in the market. Although a huge commercial success, conventional FG devices have their limitations. Two of the most prominent limitations are: (1) the limited potential for continued scaling of the device structure. This scaling limitation stems from the extreme requirements put on the tunnel oxide layer. The tunnel oxide has to allow quick and efficient charge transfer to and from the FG. On the other hand, the tunnel oxide needs to provide superior isolation under retention, endurance, and disturbed conditions in order to maintain information integrity over periods of up to a decade. When the tunnel oxide is thinner for the first consideration, the retention

characteristics may be degraded. And when the tunnel oxide is made thicker to take the isolation into account, the speed of the operation will be slower. Therefore, for mass production, there is a trade-off between speed and reliability for the optimal tunnel oxide thickness. (2) the quality and strength of tunnel oxide (or tunnel dielectric) after plenty of program/erase cycles. Once a leaky path has been created in tunnel oxide, all the charges stored in the floating gate will be lost. Therefore, two suggestions, SONOS [1.2-1.4] and nanocrystal nonvolatile memory devices [1.5-1.7], are proposed to overcome this oxide quality limit of the conventional FG structure. These technologies replace the floating gate structure with a great number of charge-storage nodes in the dielectric or in the nanocrystal. Unlike the floating gate, stored charges in isolated nodes cannot easily redistribute amongst themselves and the local leaky path will not cause the fatal loss of information for the nanocrystal nonvolatile memory device. This effectively prevents the leakage of all the stored charges out of the floating gate.

1.2 SONOS Nonvolatile Memory Devices

Nitride-based memories can be further broadly classified into charge-storage memories, such as SONOS (silicon-oxide-silicon-oxide-silicon), and localized charge-storage memories, such as those popularized by NROM [1.8]. Figure1-2 illustrates the progression of device cross section, which has led to the present SONOS device structure. The program/erase mechanism is shown in Fig. 1-3. During programming, the control gate is biased positively so that electrons from the channel can tunnel across the SiO_2 into the nitride layer. Some electrons will continue to move through the nitride layer then across the control oxide finally into the control gate. The remaining trapped charges in the nitride layer provide the electrostatic screening of the channel from the control gate. Therefore, there is a threshold voltage (V_T) shift

resulting from trapped charges in nitride and because of that SONOS can be used as a memory device just like conventional floating gate devices.The optimization of nitride and oxide films has been the main focus in recent years. Initial device structures in the early 1970s were p-channel metal-nitride-oxide-silicon (MNOS) structures with aluminum gate electrodes and thick (45 nm) silicon nitride charge storage layers. Write/erase voltages were typically 25-30 V. In the late 1970s and early 1980s, scaling moved to n-channel SNOS devices with write/erase voltages of 14-18 V. In the late 1980s and early 1990s, n- and p-channel SONOS devices emerged with write/erase voltages of 5-12 V. The dielectric consisting of oxide-nitride-oxide layers was considered for both gate insulator and storage node in nonvolatile memories (NVM). Advancements in ultra-thin tunnel oxides during the 1990s have opened the path to improved performance and reliability for NVM based on SONOS technology. The triple-dielectric SONOS structure is an attractive candidate for the compatibility with high-density scaled CMOS technology, better scaling capabilities compared to standard FG-based Flash memories and as a replacement for high-density dynamic random access memories (DRAM's). Figure1-4 illustrates SONOS device structures. The storage region for the floating-gate structure is the conducting polysilicon floating-gate electrode, while the SONOS uses a thin silicon-nitride film. The stored charge in the SONOS memory device lies in isolated sites within the silicon nitride dielectric. An advantage of the SONOS device over the floating-gate device is its improved endurance, since a single defect will not cause the discharge of the memory. A typical trap has a density of the order 10^{18}-10^{19} cm^{-3} according to Yang et al [1.9] and stores both electrons and holes (positive charges) injected from the channel.To improve the device performance of the SONOS technology, the optimization of the ONO stack has been the main considerations currently. She *et al.* demonstrated jet vapor deposited (JVD) silicon

nitride as a tunnel dielectric for flash memory device application. Compared to conventional devices with SiO_2 tunnel dielectric, faster programming speed as well as better retention time are achieved with low programming voltage [1.10]. Reisinger *et al.* [1.11] proposed a SONOS structure with a p^+ doped silicon gate instead of the commonly used n^+ gate. In the erase mode, the p^+ gate prevents the Fowler Nordheim tunneling of electrons from the conduction band of the gate into the silicon nitride film. Eitan *et al.* [1.12] proposed a novel localized 2-bit nonvolatile memory cell named as NROM^{TM}. The two-bit operation is performed by charge storage on source- and drain-side silicon nitride layer. Programming is performed by channel hot electron injection and erased by tunneling enhanced hot hole injection. Their read methodology is very sensitive to the location of trapped charge above the source and the single device cell has a two physical bit storage capability. Currently, the 2-bit-per-cell device has become a significant impact for the nonvolatile memory industry. The consecutive scaling of the SONOS technology also drives the industry of flash memory approaching the high density, low power consumption, and improved data retention and endurance [1.13]. Low-voltage (5-10 V) SONOS NVSMs may be scaled in cell size to $6F^2$ (F=feature size) [1.14] and perhaps even smaller in the years to come. The simplified ONO gate stack in SONOS memory transistors lends itself to the economics of scaled CMOS circuits

1.3 Nanocrystal Nonvolatile Memory Devices

Nanocrystal nonvolatile memories, shown in Fig. 1-5, are one particular implementation of storing charges by dielectric-surrounded nanodots, and were first introduced in the early 1990s by IBM researchers. They first proposed flash memory with a granular floating gate made out of silicon nanocrystals [1.15]. In a nanocrystal NVSM (nonvolatile semiconductor memory) device, charge is not stored on a

continuous FG poly-Si layer and not stored on a volume distributed charge traps like SONOS, but instead on a layer of discrete, mutually isolated, crystalline nanocrystals or dots. Each dot will typically store only a handful of electrons; collectively the charges stored in these dots control the channel conductivity of the memory transistor. As compared to conventional stacked gate NVSM devices, nanocrystal charge storage offers several advantages, the main one being the potential to use thinner tunnel oxide without sacrificing nonvolatility. This is a quite attractive proposition since reducing the tunnel oxide thickness is a key to lowering operating voltages and/or increasing operating speeds. This claim of improved scalability results not only from the distributed nature of the charge storage, which makes the storage more robust and fault-tolerant. There still keep the other important advantages. First, the fabrication of the nanocrystal memories is more simplified and lower cost process as compared to conventional stacked-gate Flash memories. Second, due to the less drain to FG coupling, nanocrystal memories suffer less from drain induced barrier lowering (DIBL), so they have intrinsically better punch through characteristics. One way to exploit this advantage is to use a higher drain bias during the read operation, thus improving memory access time. Third, nanocrystal memories are characterized by excellent immunity to stress induced leakage current (SILC) and oxide defects due to the isolated charge storage in the nanocrystal layer. Of particular importance is the low capacitive coupling between the external control gate and the nanocrystal charge storage layer. This does not only results in higher operating voltages, thus offsetting the benefits of the thinner tunnel oxide, but also removes an important design parameter (the coupling ratio) typically used to optimize the performance and reliability tradeoff. As for the fabrication processes, a first requirement is the aerial density of the nanocrystal dots. A typical target is a density of at least 10^{12} cm^{-2}. This is equivalent to approximately 100 particles controlling the channel of a memory FET

with 100×100 nm^2 active area, and requires particle size of 5-6 nm and below. Second, the fabrication process should result in a planar nanocrystal layer, i.e., the thickness of the dielectric layer separating the nanocrystal and the substrate should be well controlled. Poor control of the tunnel oxide thickness will result in wider threshold voltage distributions and will increase the number erratic bits. More generally, good process control is needed with regards to such nanocrystal features as: size and size distribution, inter-crystal interaction (lateral isolation), uniformity of aerial crystal density, and crystal doping (type and level).In optimizing NVM devices, the ideal goal is to achieve the fast write/erase and the long retention time. For this purpose we need to create an asymmetry in charge transport through the gate dielectric to maximize the {Ig, $_{write/erase}$/ Ig, retention} ratio. Three different approaches for achieving this goal are illustrated in Figure1-6[1.16]. By replacing the rectangular barrier with a parabolic or triangular barrier, the barrier height can be modulated by the electric field in the tunnel oxide [1.17]. Therefore, a higher tunnel–barrier is present during retention [low electric field, solid lines in Figure1-6] while a lower barrier is present during write/erase operations [high electric field induced by external bias, dashed lines in Figure1-6], thus increasing the {Ig, $_{write/erase}$/ Ig, retention} ratio. In practice, the parabolic or triangular barrier can be simulated by stacking multiple layers of dielectrics. Another approach is to use double-stacked storage nodes, preferably self-aligned with smaller dots at the lower stack [1.18]. In such devices, fast write/erase can still be achieved, if sufficiently thin tunnel oxides are used below and between the two stacks. However, the retention time can be significantly improved due to the Coulomb blockade effect at the lower stack, which prevents electrons in the top stack storage nodes from tunneling back into the substrate. The third approach, which is the focus of this paper, is to engineer the depth of the potential well at the storage nodes, thus creating an asymmetrical barrier between the

substrate and the storage nodes, i.e., a small barrier for writing and a large barrier for retention. This can be achieved if the storage nodes are made of metal nanocrystals. The major advantages of metal nanocrystals over their semiconductor counterparts include higher density of states around the Fermi level, stronger coupling with the conduction channel, a wide range of available work functions, and smaller energy perturbation due to carrier confinement. Nanocrystal memories have been presented in the mid-nineties as a possible alternative to conventional FG NVMs devices, by allowing a further decrease in the tunnel oxide thickness. In particular, nanocrystal memories promise to enable a further scaling of the tunnel oxide, by relying on Coulomb blockade effects in small semiconductor geometries and on the enhanced robustness and fault-tolerance of distributed charge storage. Research in this area has focused on the development of nanocrystal materials and fabrication processes, and on the integration of nanocrystal-based storage layers in actual memory devices. Promising device results have been presented, demonstrating low-voltage operation for comparable threshold voltage windows and operating speeds, and thin tunnel oxide retention behavior that suggests meeting long-term nonvolatility requirements. In spite of these promising results, it is unclear whether nanocrystal memories will ever see commercialization. In order for that to happen, the uniformity of the nanocrystals needs to be improved, and the claimed benefits need to be more unambiguously substantiated. Unlike volume distributed charge traps (ex: nitride in SONOS NVM), nanocrystals be deposited in a two-dimensional 2-D) layer at a fixed distance from the channel separated by a thin tunnel oxide (Fig. 2). By limiting nanocrystals deposition to just one layer and adjusting the thickness of the top blocking dielectric, charge leakages to the control gate from the storage nodes can be effectively prevented.

1.4 Organization of This Thesis

In chapter 1, general background of flash nonvolatile memory, SONOS nonvolatile memory and nanocrystal nonvolatile memory devices is introduced.

In chapter 2, basics of program and erase operation are introduced.

In chapter 3, sample structure, experimental methods and experimental process flow are stated.

In chapter 4, discuss the memory electric characteristics,

Finally, the conclusion is presented **in chapter 5**

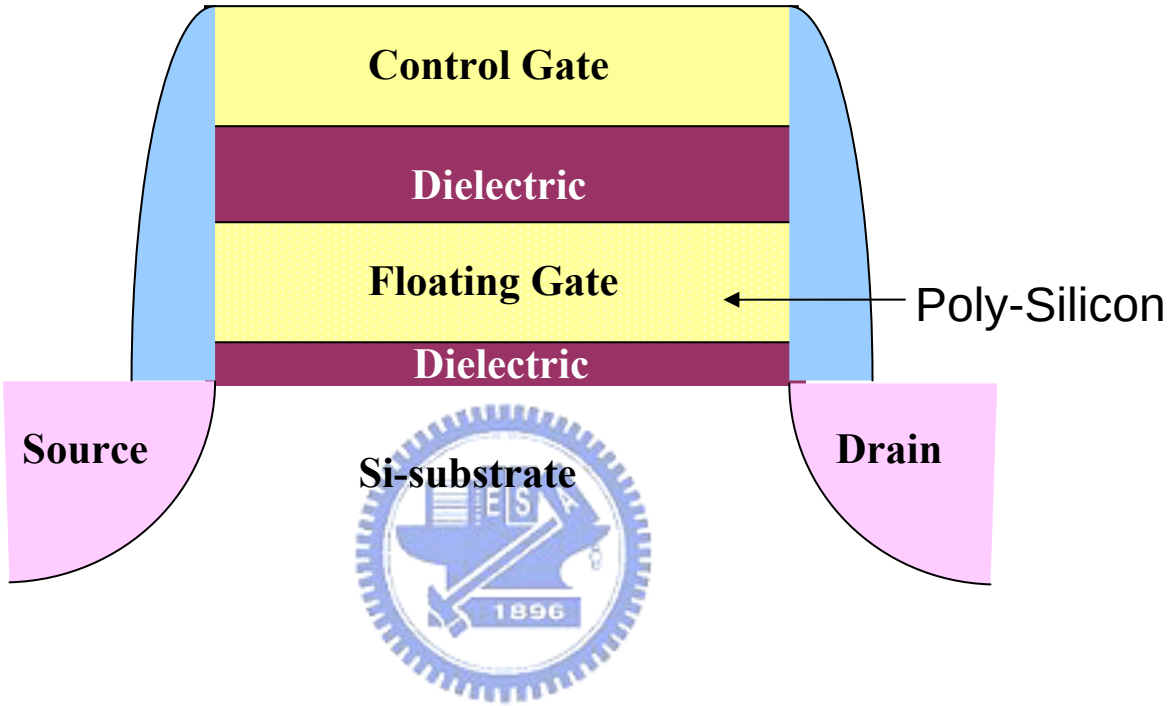


Figure 1-1 The structure of the conventional floating gate nonvolatile memory device. Continuous poly-Si floating gate is used as the charge storage element.

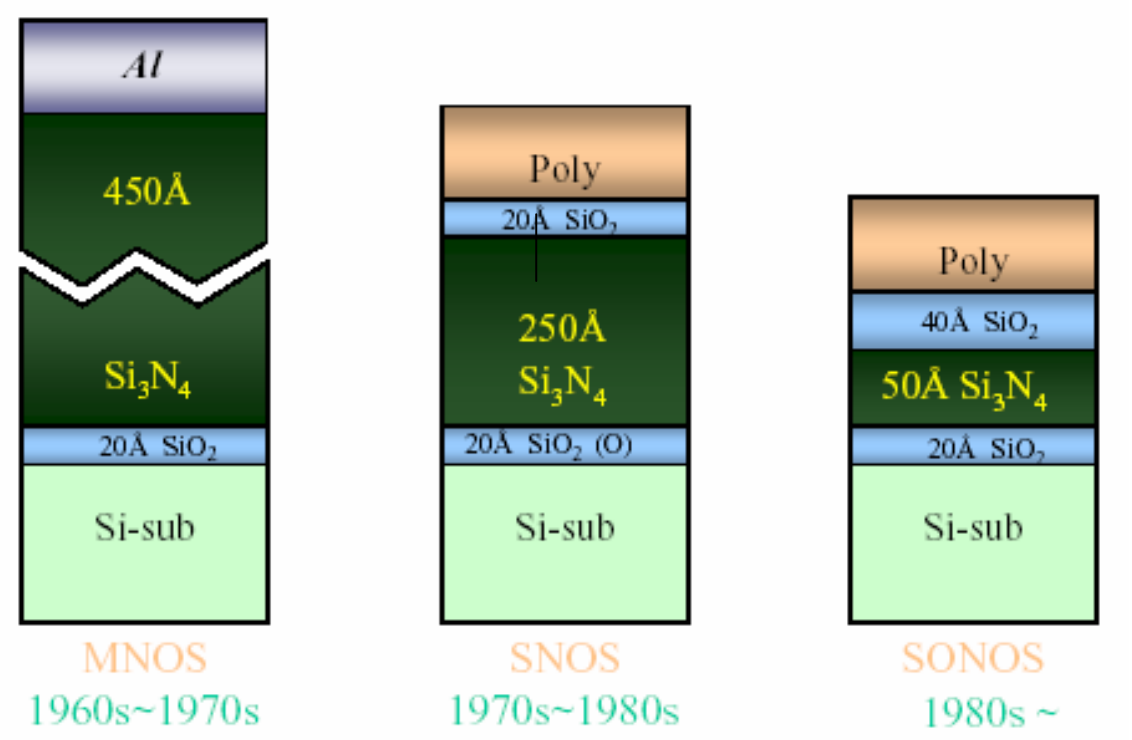


Figure 1-2 The development of the gate stack of SONOS EEPROM memory devices. The optimization of nitride and oxide films has been the main focus in recent years.

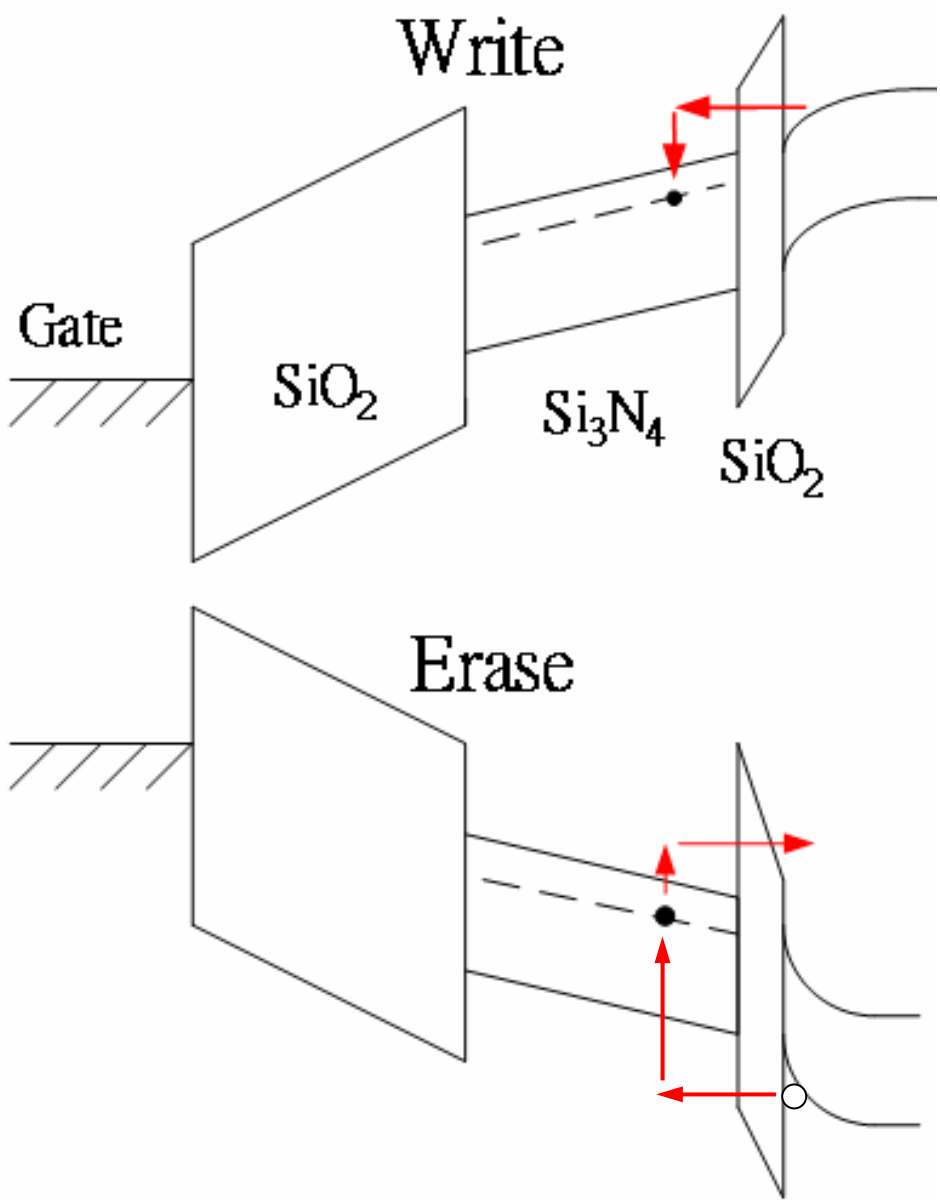


Figure 1-3 The energy band diagrams of the write/erase operation for a SONOS device.

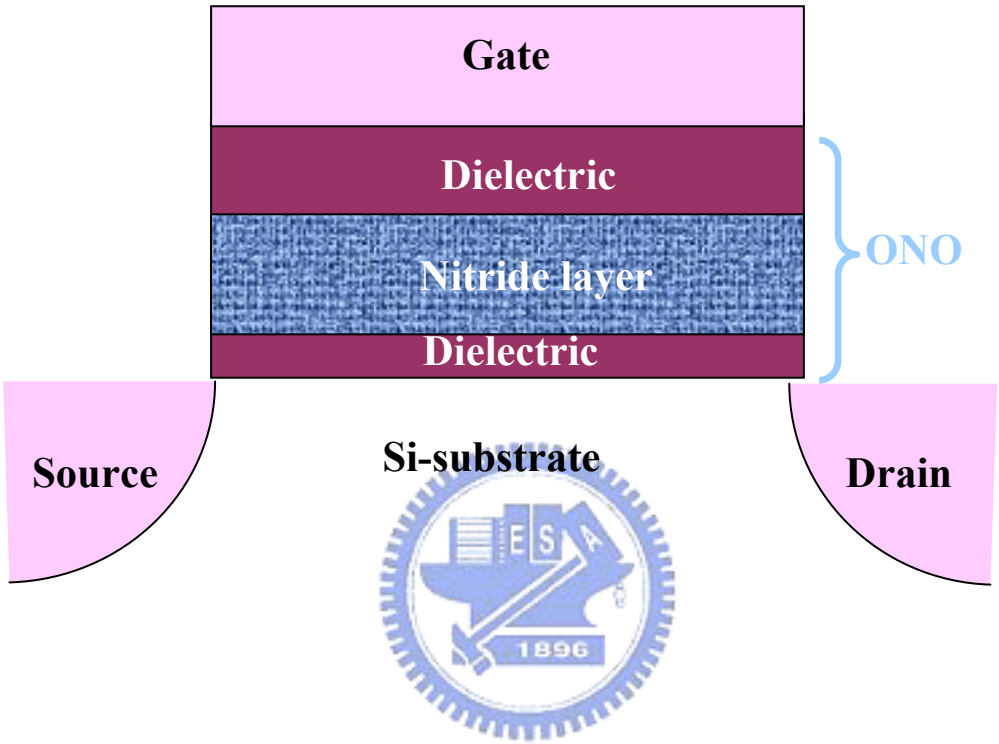


Figure 1-4 The structure of the SONOS nonvolatile memory device. The nitride layer is used as the charge-trapping element.

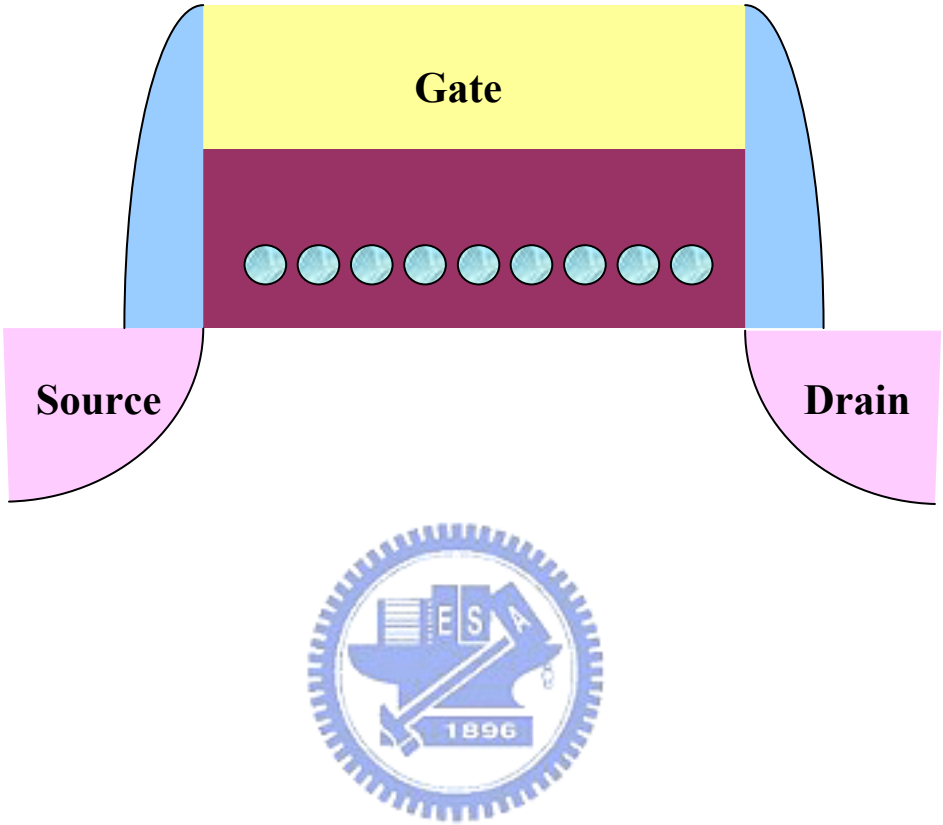


Figure 1-5 The structure of the nanocrystal nonvolatile memory device. The semiconductor nanocrystals or metal nano-dots are used as the charge storage element instead of the continuous poly-Si floating gate.

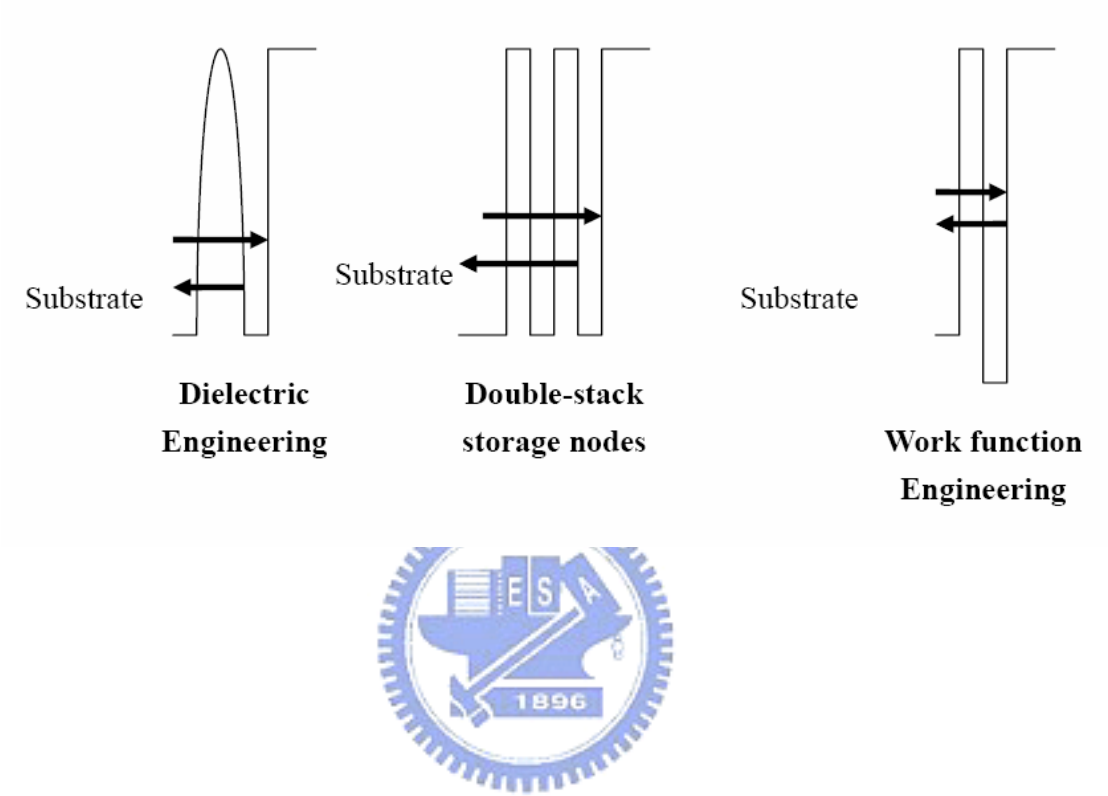


Figure 1-6 band diagram illustration of different approaches for improving the Ig, $_{write/erase}$/ Ig, retention ratio.

Chapter 2

Basics principle of nonvolatile memory

2.1 Introduction

Most of operations on novel nonvolatile memories, such as nanocrystal and SONOS memories are base on the concept of Flash memory. For SONOS NVSM, the basics operating principle of ONO structure is that electrons injected from the channel are trapped in the forbidden gap of the silicon nitride film during the program operation. On the other hand, during the erase operation, holes are injected from the substrate into silicon nitride film. If there are charges ($\overline{Q}$) stored in the silicon nitride film, the threshold voltage shift of a Flash transistor can be written as [2.1][2.2]:

$$\Delta V_T = -\frac{\overline{Q}}{C_{FC}}$$

where $\overline{Q}$ is the charge weighted with respect to its position in the gate oxide. The capacitances between the floating gate and control gate. The threshold voltage of the memory cell can be altered by changing the amount of charge present between the gate and the channel, corresponding to the two states of the memory cell, i.e., the binary values (“1” and “0”) of the stored bit. Figure 2-1 shows the threshold voltage shift between two states in a Flash memory. To a nonvolatile memory, it can be

"written" into either state "1" or "0" by either "programming" or "erasing" methods, which are decided by the definition of memory cell itself. There are many solutions to achieve "programming" or "erasing".

The energy band diagrams for the SONOS structure for positive (write) and negative gate bias (erase), and the main conduction mechanisms, are illustrated in Figure 2-2(a) (b), respectively. Under positive gate bias electron injection from the semiconductor to the nitride (J1) will dominate. In the nitride electrons are trapped and drift toward the top oxide by the Poole–Frenkel conduction [2.3] (J2). The electrons reaching the top oxide may tunnel through it to be collected by the gate (J3). Hole injection from the gate (J4) is negligible for two reasons: First, the top oxide is thicker than the bottom oxide. Second, in oxide the potential barrier for holes ($q\psi_B$=3.1 eV) is higher than for electrons ($q\psi_{Bh}$=3.8 eV). Under negative gate bias either holes are injected from the semiconductor into the nitride (J5) or the electrons previously injected by a write-pulse back-tunnel into the substrate (J6). Electrons are easily injected from the gate (J7) due to the lower potential barrier. The electrons and holes may recombine in the nitride (J8).

The write and erase processes for an n-channel semiconductor nanocrystal memory device are illustrated schematically in Figure2-3. During the write process, a positive gate voltage is applied to inject channel inversion-layer electrons into the nanocrystals. During the erase process, a reverse gate bias is applied to cause the

electrons to tunnel back into the channel and the accumulation layer holes to tunnel into the nanocrystal from the channel [2.4].

The relation between bias and energy band bending is a key to understand basics program and erase mechanisms. Figure 2-4 shows energy band diagram of SONOS. The barrier of SiO_2 is about 3.1ev for electrons in the conduction band of silicon, and 4.78ev for holes in valance band. The barrier of Si_3N_4 is about 1.05ev for electrons in the conduction band of nitride, and 2.85ev for holes in valance band, the gap for electron between conduction band and trapping level is 0.7ev, and, for hole between valance band and trapping level is 0.95ev[2.5].

In this chapter, we will discuss program/erase mechanisms from the relation between bias and energy band bending. Fowler-Nordheim Tunneling, hot electron injection, band to band assisted hole injection, channel hole injection will be discussed briefly. The reliability of nonvolatile memory and physical characteristic of nanocrystal NVM will be also discussed.

2.2 Basic Program/Erase Mechanisms

2.2.1 Tunneling Injection

Tunneling is a quantum mechanical process akin to throwing as ball against a wall often enough that the ball goes through the wall without damaging the wall or the ball. It also loses no energy during the tunnel event. Electron tunneling through the oxide can be attributed to different carrier-injection mechanisms. Which process applies depends on the oxide thickness and the applied gate field or voltage. Direct tunneling (DT), Fowler-Nordheim tunneling (FN), modified Fowler-Nordheim

tunneling (MFN) and trap assistant tunneling (TAT) are the main programming mechanisms employed in memory [2.6-2.8] as shown in Figure 2-5.

Direct Tunneling

Direct Tunneling is the flow of electrons through the full oxide thickness illustrated in Figure 2-6. For nanocrystal memories, the control-gate coupling ratio of nanocrystal memory devices is inherently small [2.9]. As a result, F-N tunneling cannot serve as an efficient write/erase mechanism when a relatively thick tunnel oxide is used, because the strong electric field cannot be confined in one oxide layer. The direct tunneling is employed in nanocrystal memories instead. In the direct-tunneling regime, a thin oxide with thickness less than 3 nm is used to separate the nanocrystals from the channel. During write/erase operations, electrons/holes can pass through the oxide by direct tunneling, which gives the advantages of fast write/erase and low operation voltage. In the other hand, the direct tunneling is more sensitive to the barrier width than barrier height, two to four orders of magnitude reduction in leakage current can still be achieved if large work function metals, such as Au or Pt [2.10].

Fowler–Nordheim Tunneling

Fowler-Nordheim tunneling is a field-assisted carrier tunneling mechanism [2.11], when a strong electric field (in the range of 8–10 MV/cm) applied across a metal-ONO-substrate structure, its band stricture will be influenced as indicated in Figure 2-7. Due to high electrical field, electrons in the poly-Si conduction band as triangular energy barrier with a width dependent on applied electric field. At sufficient high fields, the width of barrier becomes small enough to tunnel through the

barrier from the poly-Si conduction band into nitride electron trap layer.

Using a free-electron gas model for the metal and the WKB approximation for the tunneling probability [2.12], one obtains the following expression for current density [2.13]:

$$J = \frac{q^3 F^2}{16\pi^2 h^2 \Phi_B} \exp\left[\frac{-4(2m_{OX}^*)^{1/2}\Phi_B^{3/2}}{3\eta qF}\right] \quad (18)$$

Where Φ_B is the barrier height, m_{OX}^* is the effective mass of the electron in the forbidden gap of the dielectric, h is the Planck's constant, q is the electronic charge, and F is the electric field through the oxide. The exponential dependence of tunnel current on the oxide-electric field causes some critical problems of process control because, for example, a very small variation of oxide thickness among the cells in a memory array produces a great difference in programming or erasing currents, thus spreading the threshold voltage distribution in both logical states.

Modified Fowler–Nordheim Tunneling

Modified Fowler–Nordheim tunneling (MFN) is similar to the traditional FN tunneling mechanism, yet the carriers enter the nitride at a distance further from the tunnel oxide-nitride interface. MFN mechanism is frequently observed in SONOS memories. The SONOS memory is designed for low-voltage operation (<10 V, depending on the Equivalent oxide thickness), a relatively weak electrical field couldn't inject charges by DT or FN mechanism.

Trap Assistant Tunneling

The charge storage mediums with many traps may cause another tunneling mechanism. For example, the charges tunnel through a thin oxide and arrive to the

traps of nitride layer at very low electrical field in SONOS systems. During trap assisted injection the traps are emptied with a smaller time constant then they are filled. The charge carriers are thus injected at the same distance into the nitride as for MFN injection. Because of the sufficient injection current, trap assistant tunneling may influence in retention [2.14].

2.2.2 Hot-Electron Injection & Hot hole injection

The physical mechanism of HEI is relatively simple to understand qualitatively. An electron traveling from the source to the drain gains energy from the lateral electric field and loses energy to the lattice vibrations (acoustic and optical phonons). At low fields, this is a dynamic equilibrium condition, which holds until the field strength reaches approximately 100 kV/cm [2.15] At large drain bias, the minority carriers that flow in the channel are heated by the large electric fields occurred at the drain side of the channel and their energy distribution is shifted higher. This phenomenon gives rise to impact ionization at the drain, by which both minority and majority carriers are generated. The highly energetic majority carriers are normally collected at the substrate contact and from the so-called substrate current. The minority carriers heating occurs when some of the minority carriers gain enough energy to allow them to surmount the SiO_2 energy barrier. If the oxide field favors injection, these carriers injected over the barrier into the gate insulator and give rise to the so-called hot-carrier injection gate current [2.15-2.16]. Figure 2-8 shows the phenomenon of hot electron injection. This mechanism is schematically represented for the case of an n-channel nonvolatile memory.

In MOS devices, the drain voltage should increase beyond the saturation voltage Vdsat (Vd > Vdsat), the mode can named hot carrier effect. To distinguish from Fowler-Nordheim tunneling, the definition of hot carrier injection in this study is the

only condition that the drain is applied bias.

The mechanism of hot hole injection in P-channel is like to hot electron injection. Figure 2-9 shows the phenomenon of hot hole injection. It's reported that hole injection is a erase operation in P-channel device [2.17].

2.2.3 Band to Band Assisted Hole Injection

In N-channel, when a negative gate voltage and a positive drain voltage are applied to the cell, electron-hole pairs are generated by BTBT in the drain region [2.18-2.19]. The holes are accelerated by a lateral electric field toward the channel region and some of them obtain high energy. The injection of such hot holes [2.20] into nitride through the tunnel oxide is used for a new erase operation in N-channel.

2.3 Basic Reliability of Nonvolatile Memory

For a nonvolatile memory, the important to concern is distinguishing the state in cell. However, in many times operation and charges storage for a long term, the state is not obvious with charges loss. Endurance and retention experiments are performed to investigate Flash-cell reliability.

2.3.1 Retention

Retention describes the ability to the NVM to store and recover information after a number of program cycles at a specified temperature. In any nonvolatile memory technology, it is essential to retain data for over ten years. This means the loss of charge stored in the storage medium must be as minimal as possible. For example, in modern Flash cells, FG capacitance is approximately 1 fF. A loss of only 1 fC can cause a 1V threshold voltage shift. If we consider the constraints on data retention in ten years, this means that a loss of less than five electrons per day can be tolerated [2.21]. Possible causes of charge loss are: 1) by tunneling or thermionic emission

mechanisms; 2) defects in the tunnel oxide; and 3) detrapping of charge from insulating layers surrounding the storage medium.

2.3.2 Endurance

Endurance is the number of erase/write operations that the memory will complete and continue to operate as specified in the data sheet. In a conventional Flash memory the maximum number of erase/program cycles that the device must sustain is 10^5. Many researchers have observed excellent endurance behavior on nanocrystal memories, showing only limited threshold voltage window closure after more than 10^5 write/erase cycles [2.22-2.24].

2.4 Basic Physical Characteristic of Nanocrystal NVM

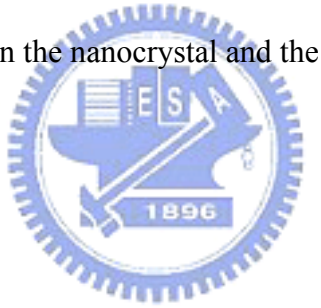
2.4.1 Quantum Confinement Effect

The quantum confinement energy dependence on nanocrystal size has been studied both experimentally and theoretically with the tight-binding model [2.23]. The quantum confinement effect becomes significant when the nanocrystal size shrinks to the nanometer range, which causes the conduction band in the nanocrystal to shift to higher energy compared with bulk material [2.25]. The quantum confinement energy dependence on nanocrystal size has been studied both experimentally and theoretically with the tight-binding model [2.26]. Compared with bulk Ge, a 3nm Ge nanocrystal can have a conduction band shift of 0.5eV, which is significant enough to affect the electrical performance of the nanocrystal memory cell.

2.4.2 Coulomb Blockade Effect

The stored electron charge will raise the nanocrystal potential energy and reduce the electric field across the tunnel oxide, resulting in reduction of the tunneling current density during the write process. It is more dominant at low programming

voltages (<3V). In a flash memory array, device cells often encounter disturbances with low gate voltage soft-programming. The Coulomb blockade effect can effectively inhibit the electron tunneling at low gate voltage and improve the flash memory array immunity to disturbance. However, the Coulomb blockade effect should be reduced by employing large nanocrystals if large tunneling current and fast programming speed are desired. The Coulomb blockade effect has a detrimental effect on the retention time, since the electrons in the nanocrystal have large tendency to tunnel back into the channel if the nanocrystal potential energy is high in retention mode. In the energy band diagram shown in Figure 2-2, the Coulomb blockade charging energy only raises the electrostatic potential of the nanocrystal; the quantum confinement energy shifts the nanocrystal conduction band edge upward so that the conduction band offset between the nanocrystal and the surrounding oxide is reduced.



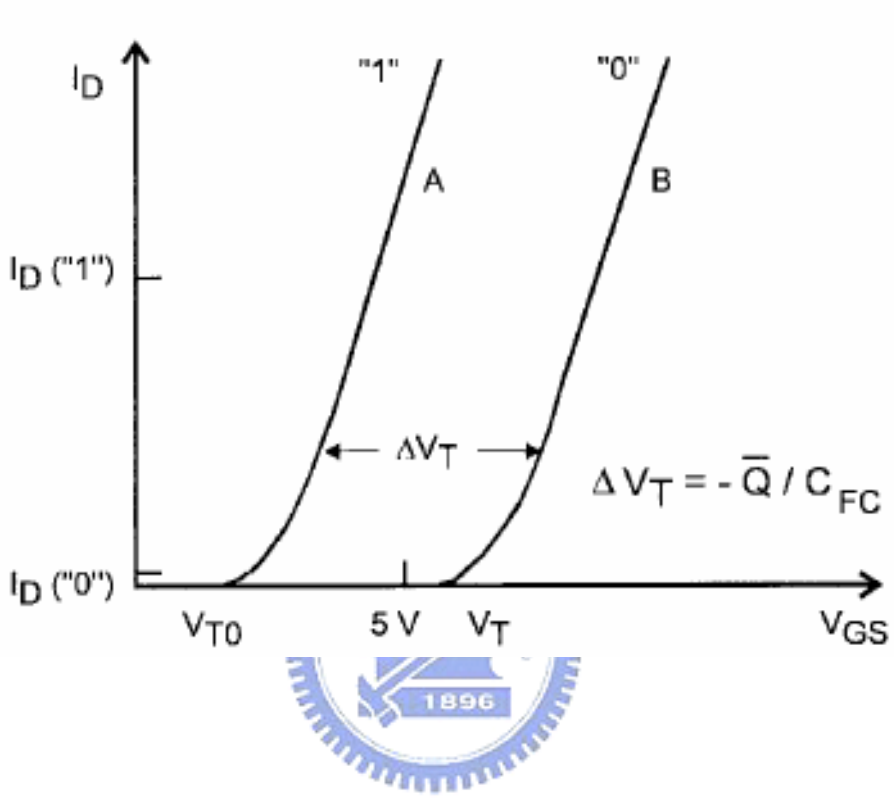


Figure 2-1 I–V curves of an FG device when there is no charge stored in the FG (curve A) and when a negative charge $\bar{Q}$ is stored in the FG (curve B).

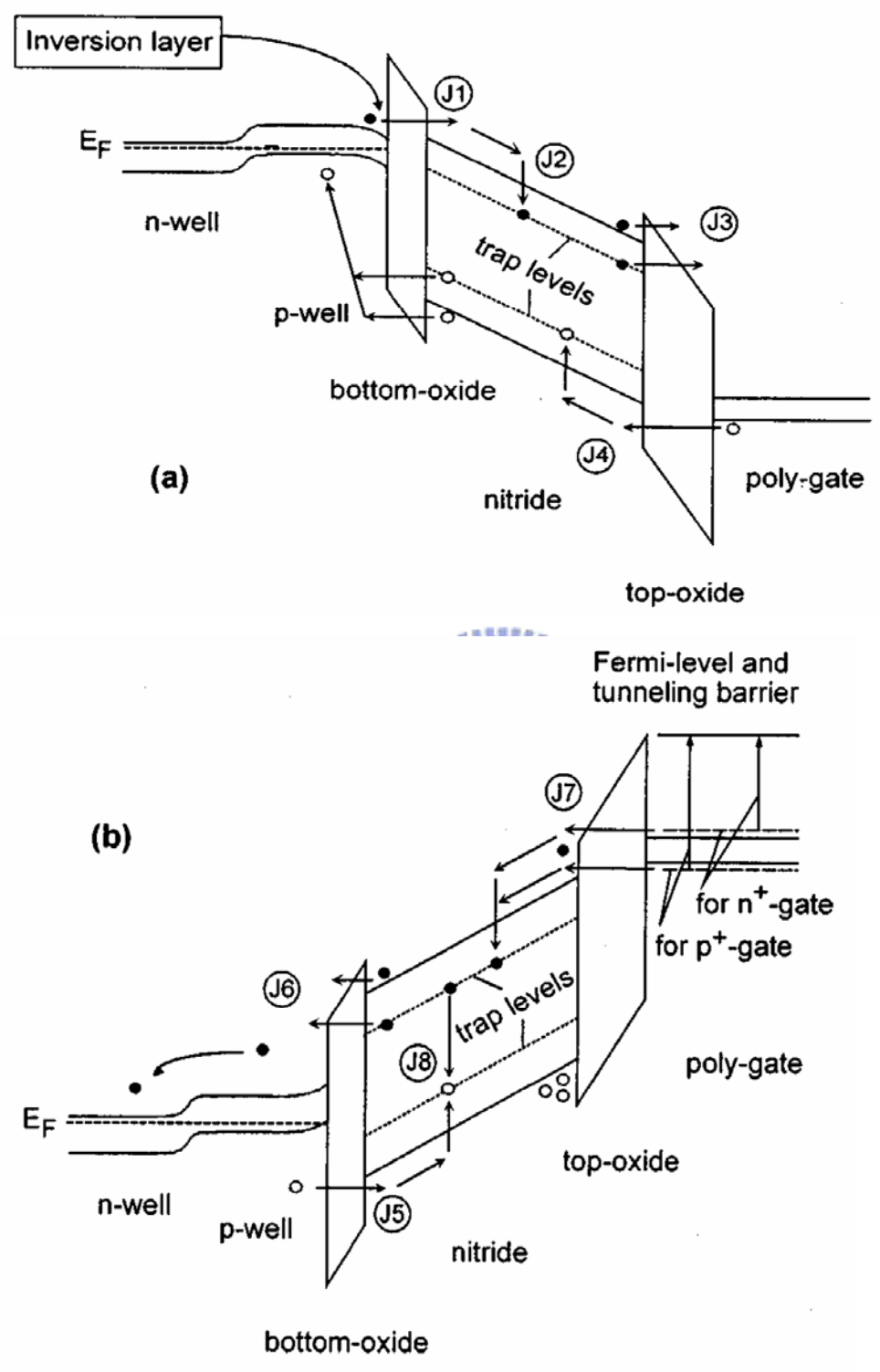


Figure 2-2 Energy band diagrams of a dual-channel SONOS transistor under (a) positive and (b) negative gate bias.● electrons, ○ holes.

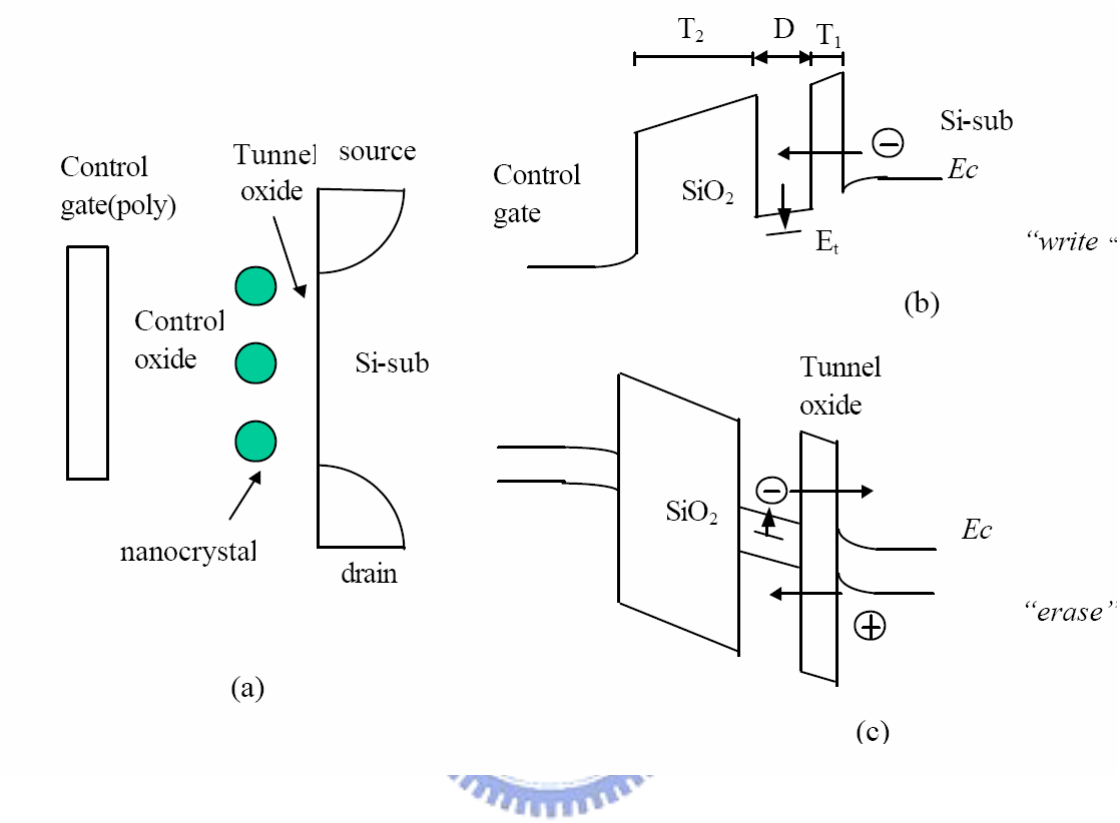


Figure 2-3 (a) Schematic cross-section of nanocrystal memory device structure; (b) illustration of write process: inversion-layer electron tunnels into the nanocrystal; (c) illustration of erase process: accumulation layer hole tunnels into the nanocrystal, electron in nanocrystal can tunnel back to the channel.

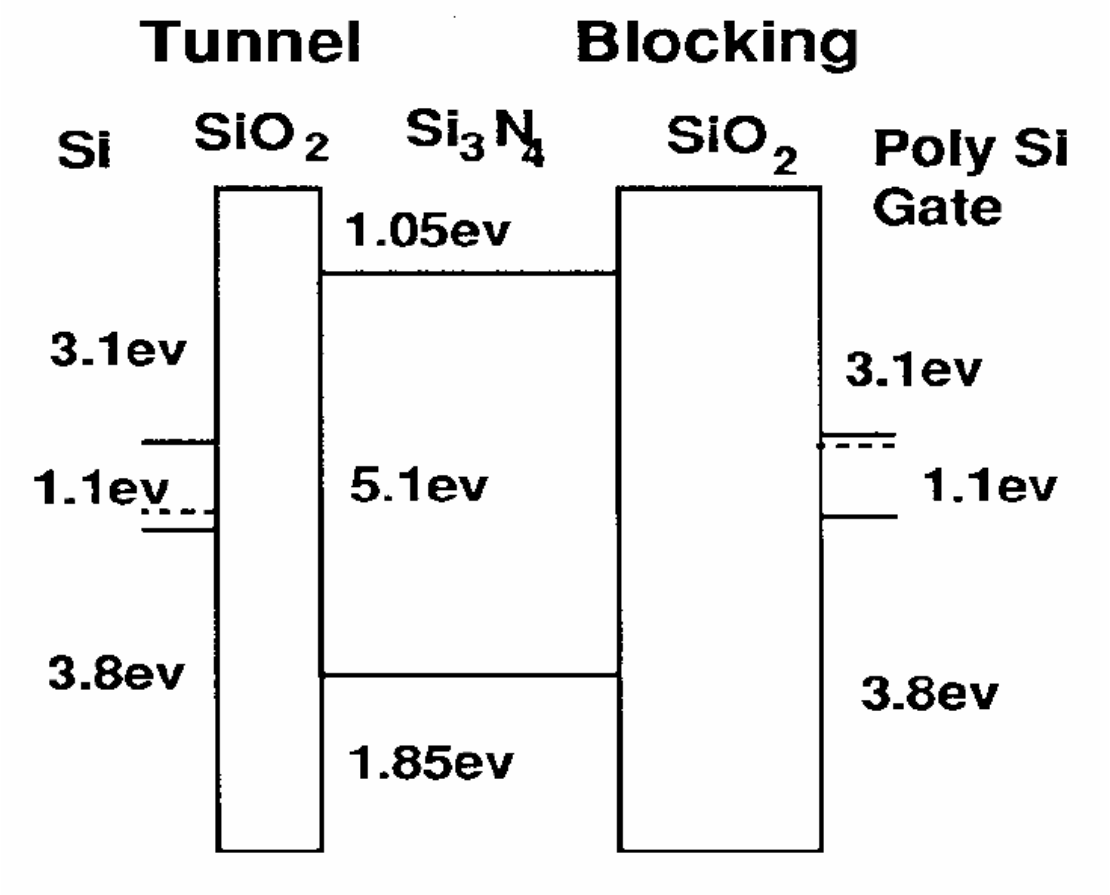
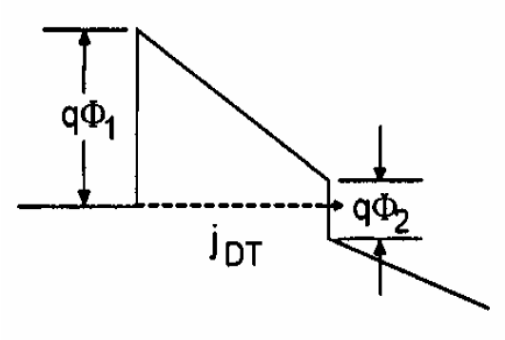
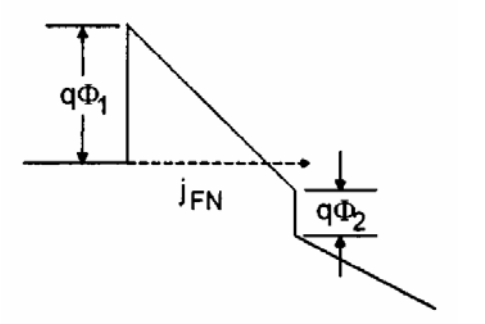


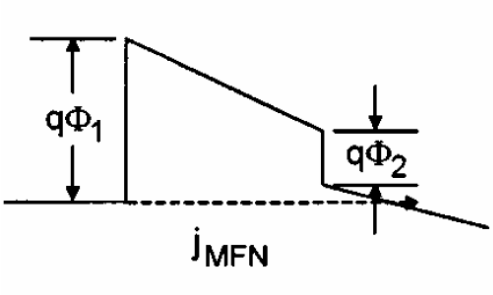
Figure 2-4 SONOS ideal energy band diagram.



DT occur when $\frac{\phi_1}{X_{OT}} > |E_{OT}| > \frac{\phi_1 - \phi_2}{X_{OT}}$

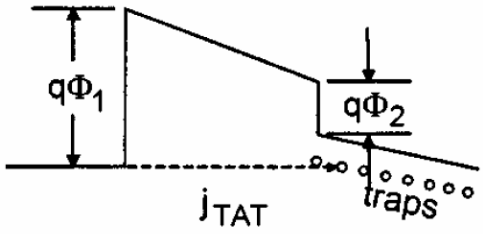


FN occur when $|E_{OT}| > \frac{\phi_1}{X_{OT}}$



MFN occur when

$$\frac{\phi_1 - \phi_2}{X_{OT}} > |E_{OT}| > \frac{\phi_1 - \phi_2}{X_{OT} + \left(\varepsilon_{OX} / \varepsilon_N\right) X_N}$$



TAT occur when

$$\frac{\phi_3}{X_{OT}} > |E_{OT}| > \frac{\phi_3}{X_{OT} + \left(\varepsilon_{OX} / \varepsilon_N\right) X_N}$$

$$\phi_3 = \phi_1 - \phi_2 - \phi_t$$

Figure 2-5 Fourth approaches to programming methods, described by Hu and White.

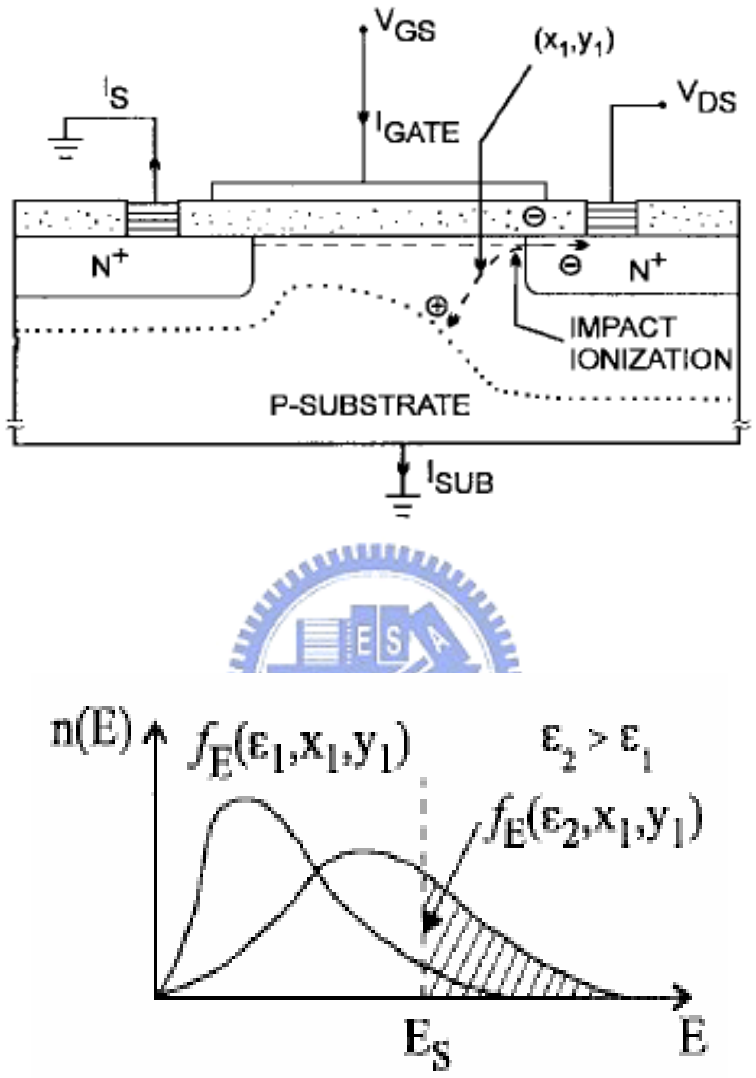


Figure 2-6 Schematic cross section of MOSFET. The energy-distribution function at point (X_1,Y_1) is also shown.

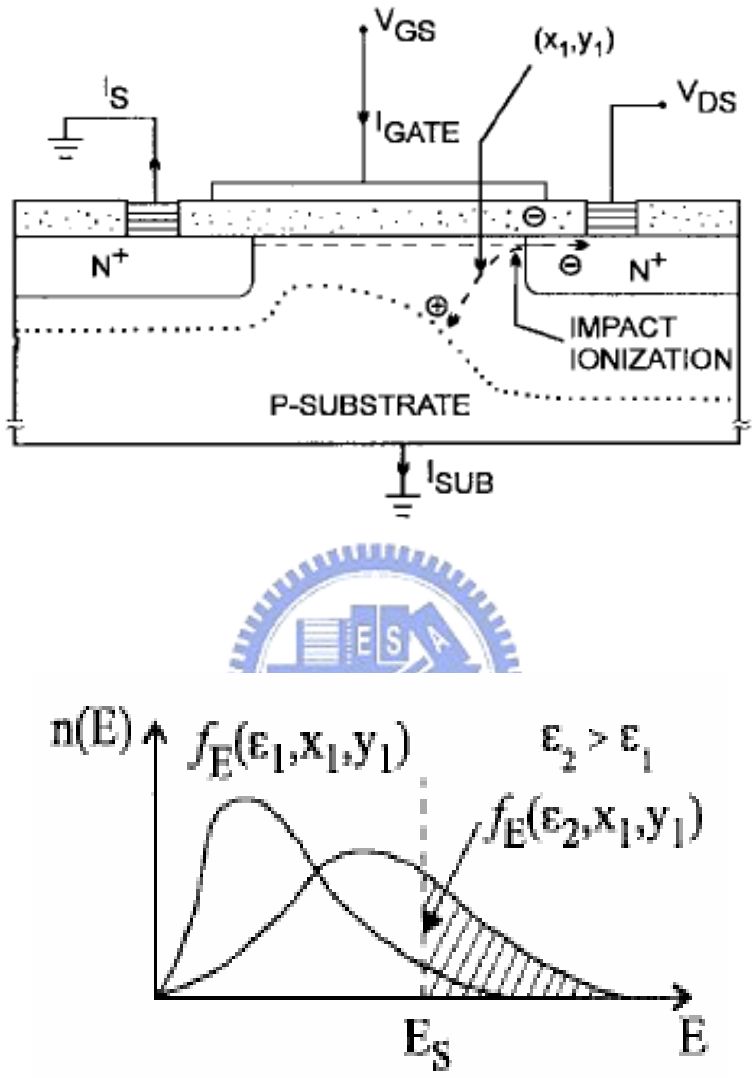
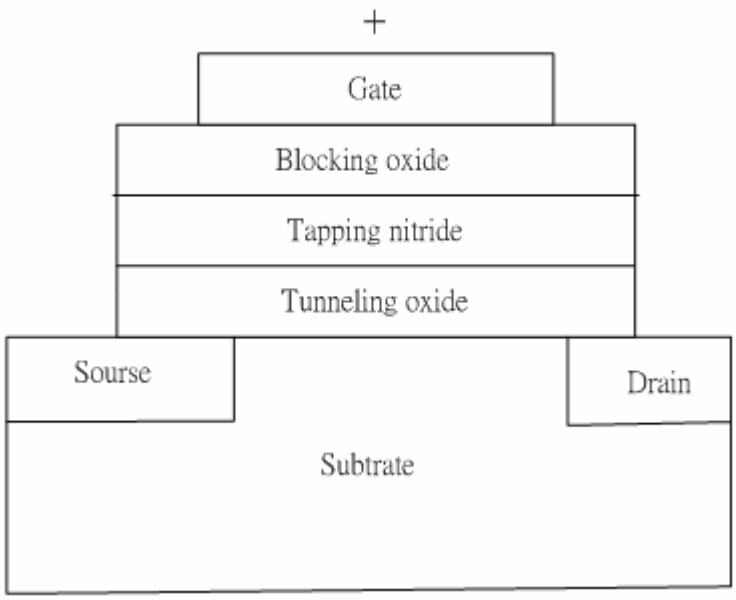
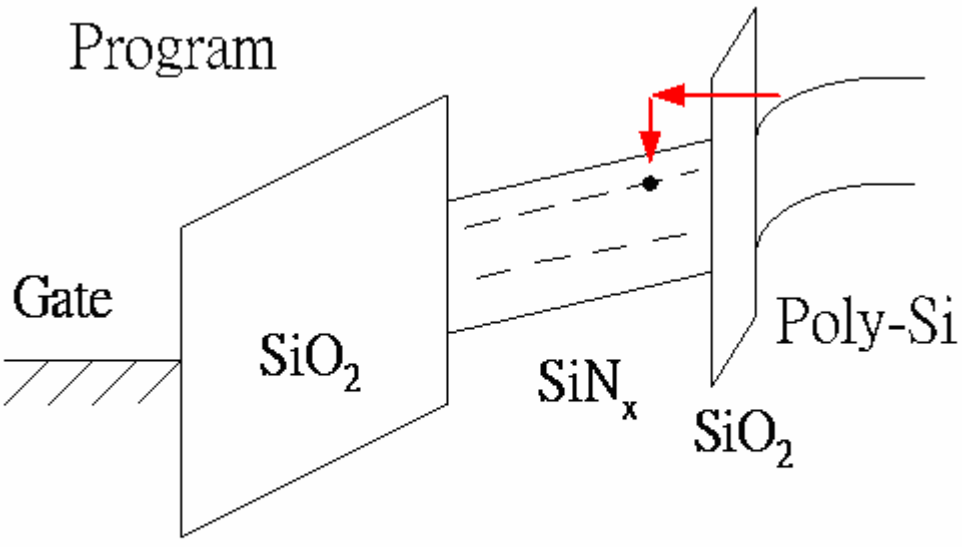


Figure 2-6 Schematic cross section of MOSFET. The energy-distribution function at point (X_1,Y_1) is also shown.



(a)



(b)

Figure 2-7 (a) Positive gate voltage applied when use Fowler-Nordheim tunneling to program (b) Energy band representation of Fowler-Nordheim tunneling. Electron in poly-Si conduction band tunnel through the triangular energy barrier.

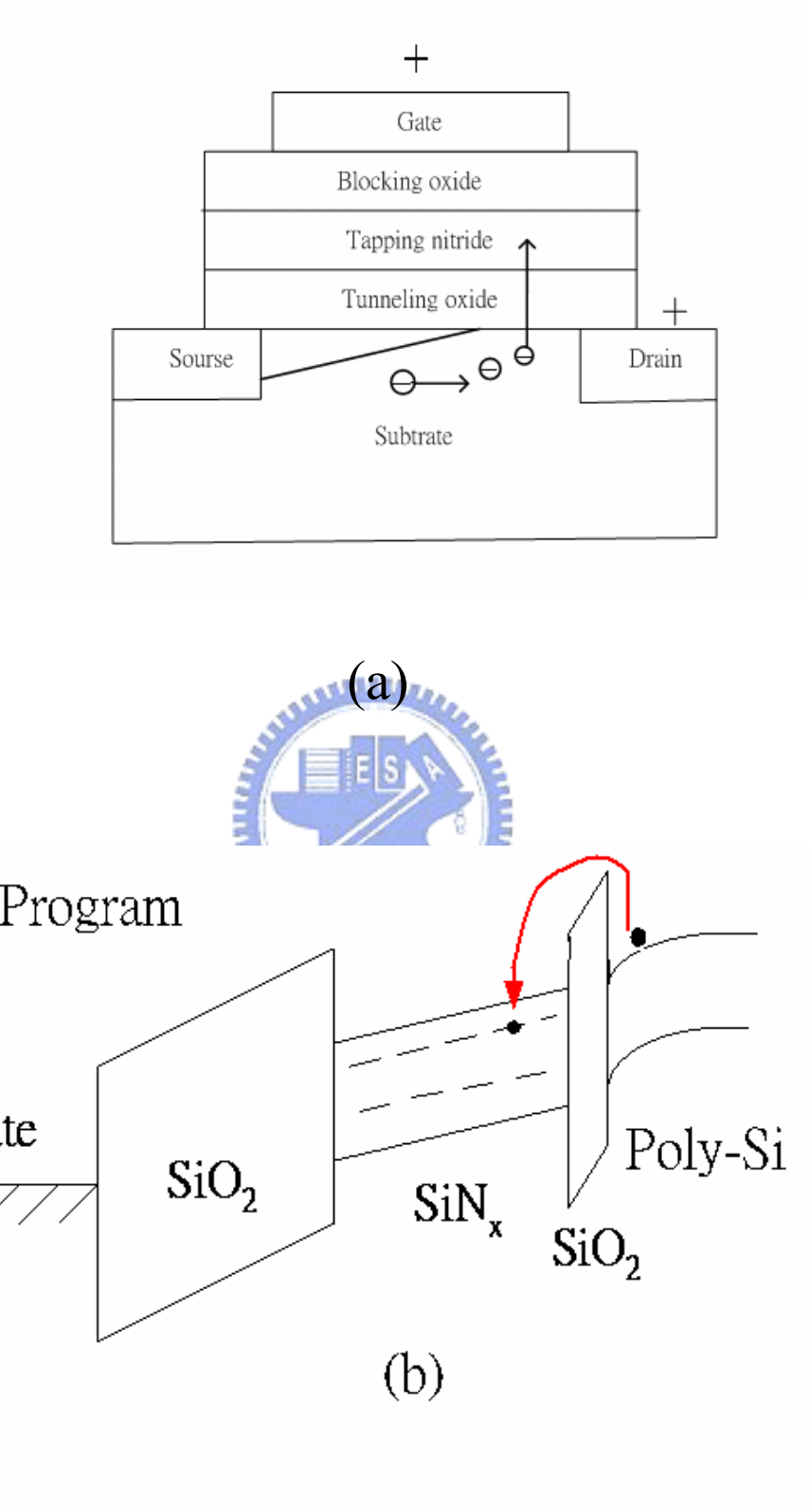


Figure 2-8 (a) Positive gate voltage and Positive drain voltage applied when use hot carrier injection to program (b) Energy band representation of hot carrier injection

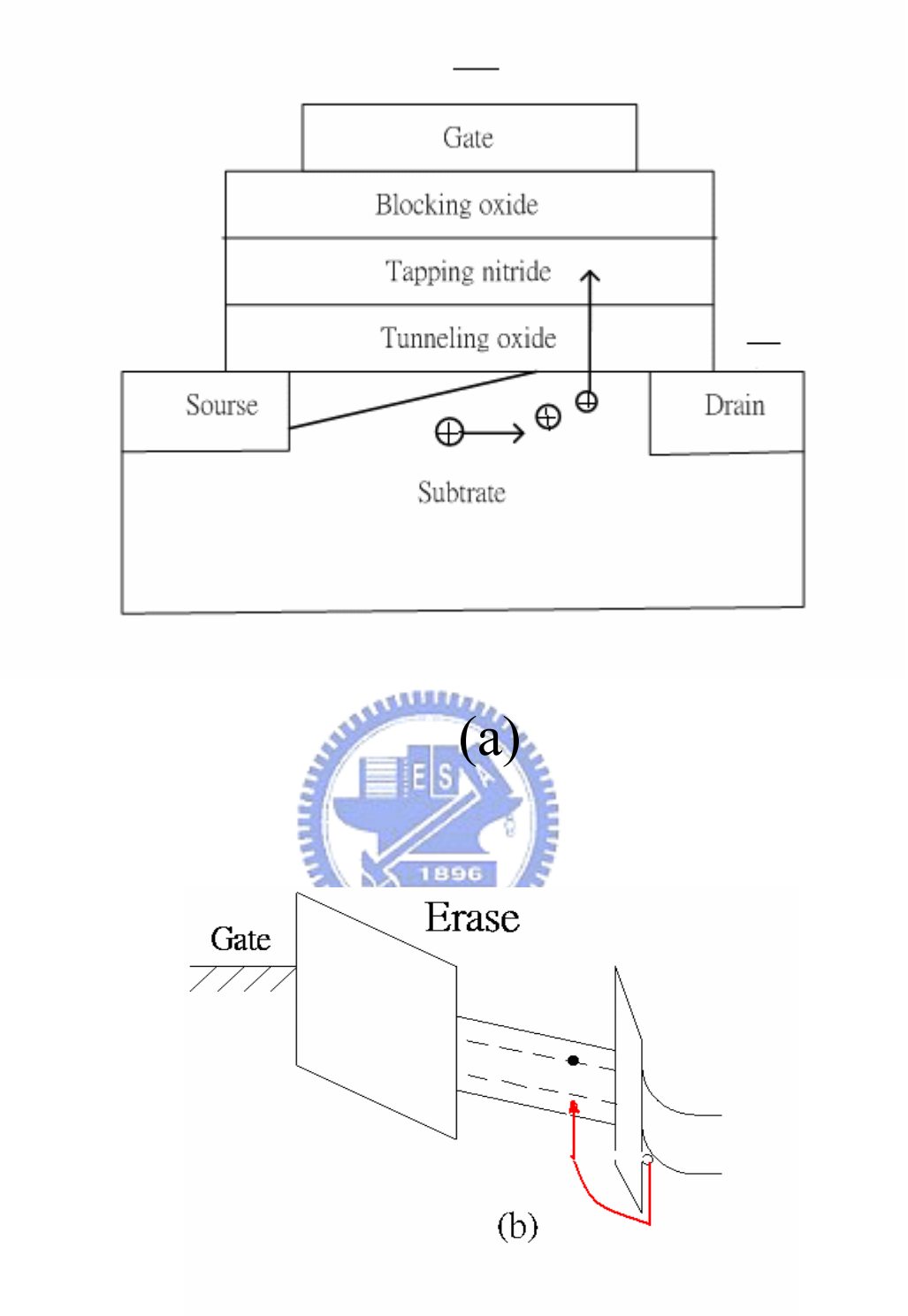


Figure 2-9 (a) Negative gate voltage and negative drain voltage applied when use hot hole injection to erase. (b) Energy band representation of hot hole injection to erase.

Chapter 3

Nonvolatile Zr-Germaniumlicide Memory

3.1 Motivation

Recently, the memories are required by high density, fast operation speed and good reliability. Memory-cell structures employing discrete traps as the charge storage media have been attracted large of the researches as the promising candidates to replace conventional DRAM or Flash memories. The advantages of metal nanocrystals over the semiconductor counterparts include lower power consumption, higher density of states, stronger coupling with the channel, and better size scalability. In addition, the design freedom of engineering the work functions is also considered to optimize device characteristics [3-1].

In this study, the ZrGe alloy nanocrystal was investigated for the application of nonvolatile memory. The obvious memory effects were observed after thermal treatment for the proposed structures in this study. In addition, the thermal treatment conditions were also discussed for proposed structures.

3.2 Sample Structure & Thermal process

Figure 3-1 (a) and (b) show the two different pre-thermal samples, labeled as structure 1 and structure 2 respectively. First, a 5-nm-thick thermal oxide was grown on p-type Si substrate by dry oxidation in an atmospheric pressure chemical vapor deposition (APCVD) furnace as a tunnel oxide in both samples. The doubled layers, 50-nm-thick Ge layer and 30-nm-thick Zr layer, were deposited on tunnel oxide by

sputter system. Also, this stacked structure is labeled as structure 1. However, structure 1 with following 10-nm-thick SiO2 layer deposition using plasma-enhanced chemical vapor deposition (PECVD) system is labeled as structure 2. Figure 3.1(a) and (b) indicate the structures for structure 1 and structure 2, respectively.

The deposition condition of the PECVD SiO_2 was kept at 300 ℃ in a low pressure of 6 mTorr. The precursor gases were SiH_4 : Ar : N_2O :N_2 = 69 sccm : 6 sccm : 120 sccm : 500 sccm. In addition, the RF power is kept at 50 W. The N_2 gas was served as the carrier gas to adjust the chamber pressure and make the process gas can easily transport into the process chamber. The low pressure of 6mTorr during deposition increases the mean free path of electrons and radicals to improve the uniformity of the thin film [3.2]. Then, the thermal treatments were performed in the rapid temperature annealing (RTA) system in nitrogen and oxygen ambient, respectively. Also, the blocking oxide formation was utilized by PECVD system. Finally Al gate was patterned and sintered to form a metal/oxide/Zirconium-Germaniumcide/oxide/ oxide/silicon (MONOS) structure. Figure 3-2 and Figure 3-3 indicate the thermal process flow for structure 1 and structure 2, respectively. In addition, the thermal treated Zr-Ge cosputtered layer as charge storage layer was also discussed in this thesis. Two groups of samples, with/ without PECVD SiO2 deposition first before thermal treatment, are also fabricated. Figure 3-4 (a) and (b) show the proposed structure with cosputtered Zr-Ge layer on tunnel oxide for with/without PECVD SiO2 deposition first, respectively. structure 3 is named as the stacked structure without PECVD SiO2 deposition before thermal treatment. The deposition condition for cosputtered Zr-Ge layer was kept at the 100W and 80W for Ge target and Zr target, respectively. Also, the same as the above discussion, structure 4 were thermal treated after 10-nm-thick SiO2 deposition by

PECVD system.

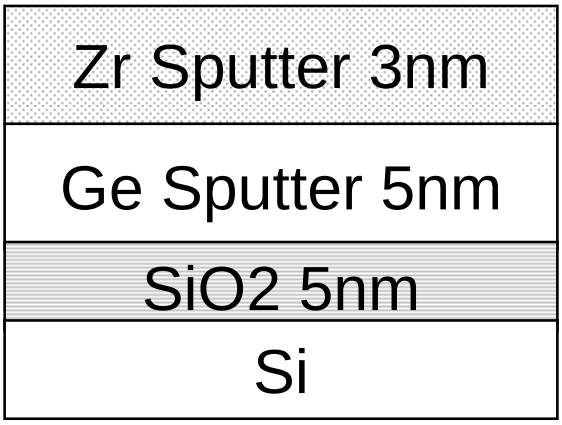
The deposition condition of the PECVD SiO_2 was the same as structure 2. Then, the samples were annealed in rapid temperature annealing (RTA). Then, 50-nm-thick blocking oxide was deposited by PECVD system. Finally, the Al gate was patterned and sintered to form a metal/oxide/Zirconium-Germaniumlicide/oxide/silicon (MONOS) structure. The process flow for structure 3 and structure 4 are as shown in Figure 3-5 and Figure 3-6, respectively.

And we fabricated two groups of structures only Ge and only Zr as a charge storage layer to compare above samples. Only Ge the process was like above structure. We also have two samples with/ without PECVD SiO2 deposition first before thermal treatment. Without PECVD SiO2 before thermal treatment was named structure 5 and with SiO2 was structure 6.Only Zr process like only Ge, just use Zr to replace Ge. So we also have two different samples, structure 7 was without SiO2 and structure 8 was with SiO2 before thermal treatment.

These MOS capacitance structure has prepared for material and electrical analyses.

Then, the micro-structures of samples were analyzed by transmission electron microscope (TEM). The capacitance-voltage characteristics were measured at frequency 100 kHz by HP4284 Precision LCR Meter. The capacitance-voltage measurement analyzed the electrical characteristics, such as memory effect of nanocrystal memories. The current-voltage (I-V) characteristics were measured by HP4156C Precision Semiconductor Parameter Analyzer.

Structure 1



(a)

Structure 2

(b)

Figure 3-1 (a) Sample structure of structure 1 (b) Sample structure of structure 2.

Structure 1

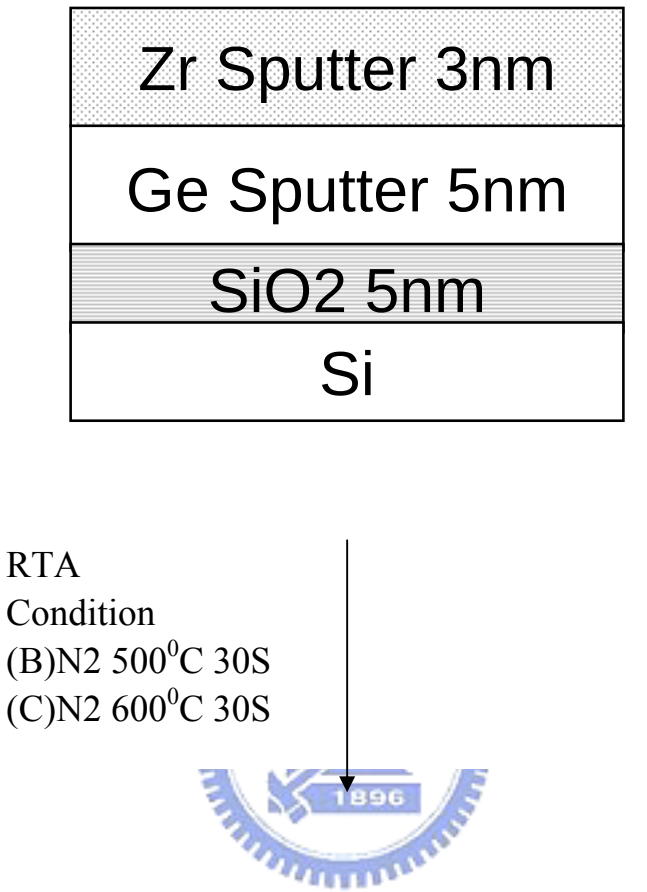


Figure 3-2 The thermal process flow of structure 1

Structure 2

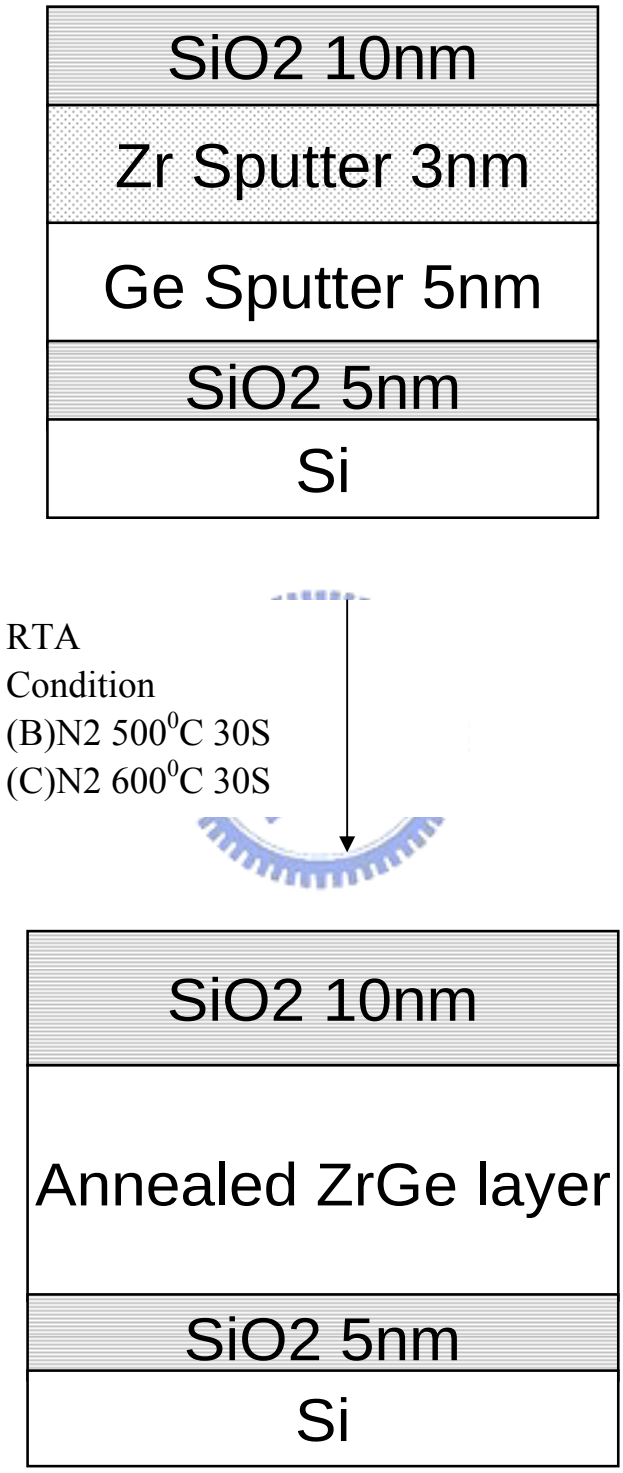
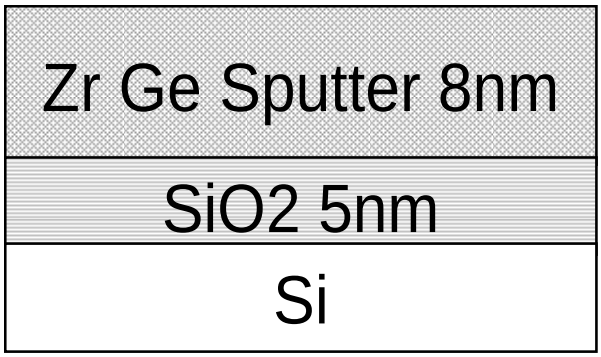


Figure 3-3 The thermal process flow of structure 2

Structure 3



(a)

Structure 4

(b)

Figure 3-4 (a) Sample structure of structure 3 (b) Sample structure of structure 4.

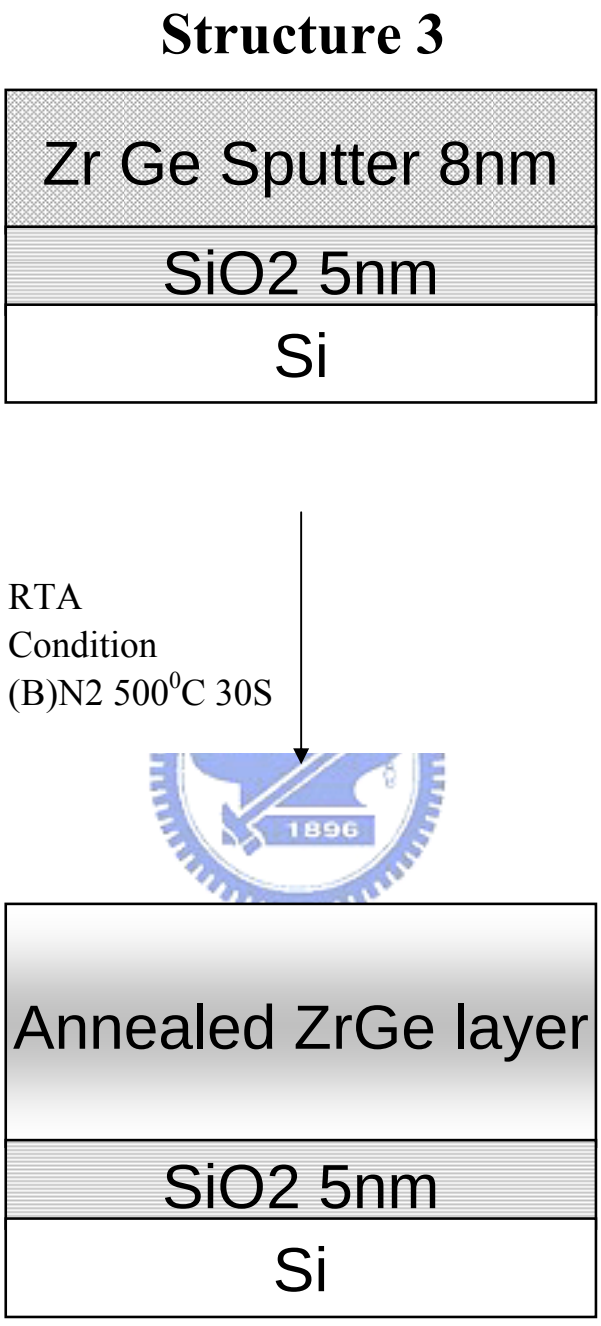


Figure 3-5 The thermal process flow of structure 3

Structure 4

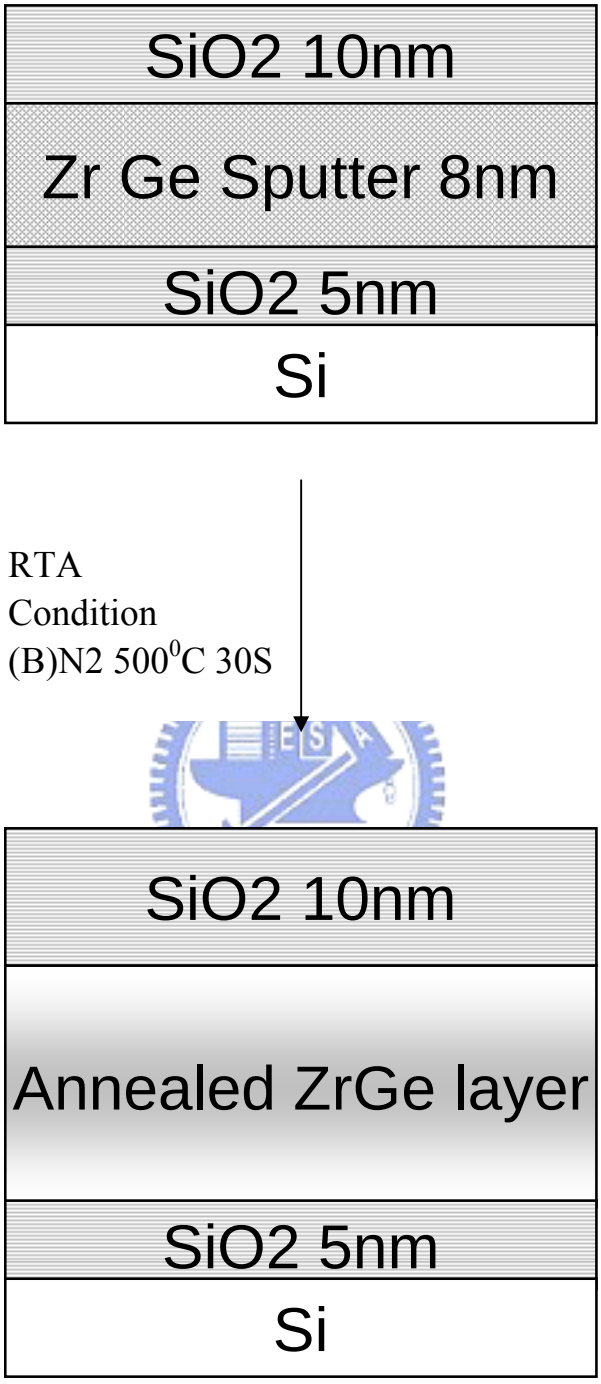
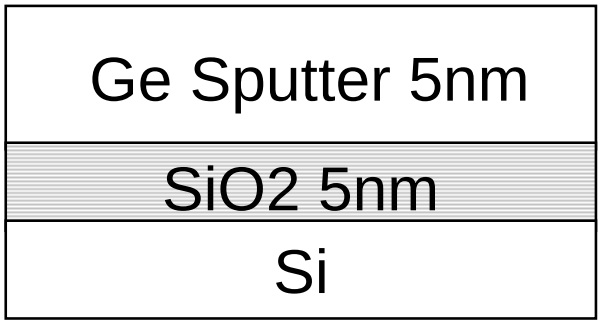


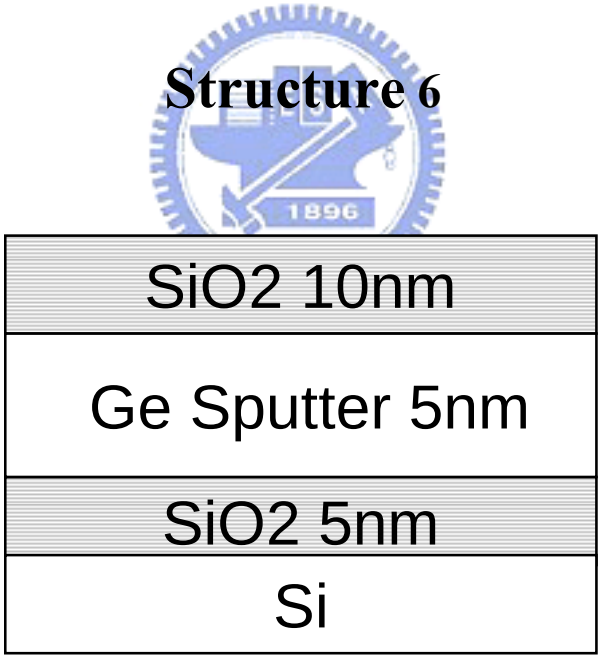
Figure 3-6 The thermal process flow of structure 4

Structure 5



(a)

Structure 6



(b)

Figure 3-7 (a) Sample structure of structure 5 (b) Sample structure of structure 6

Structure 5

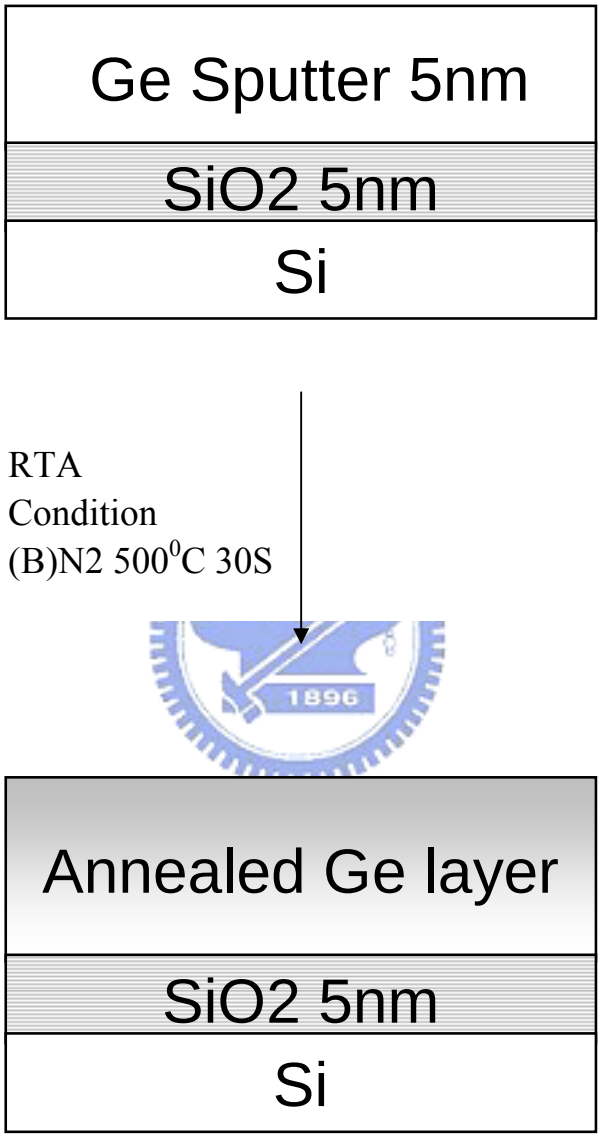


Figure 3-8 The thermal process flow of structure 5

Structure 6

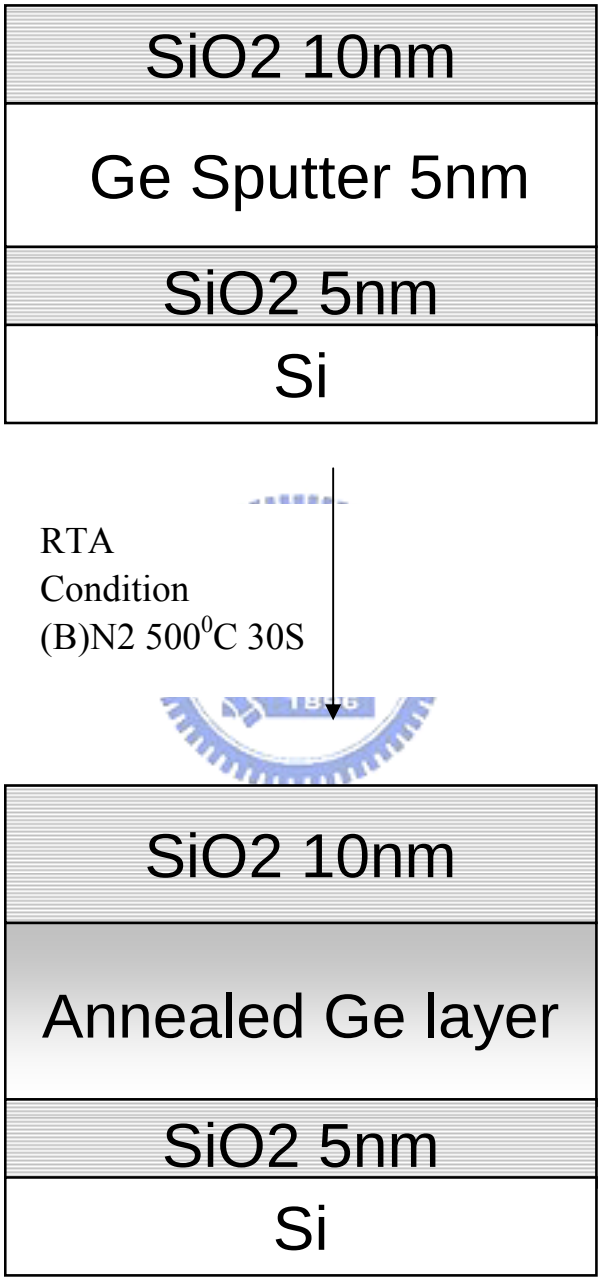
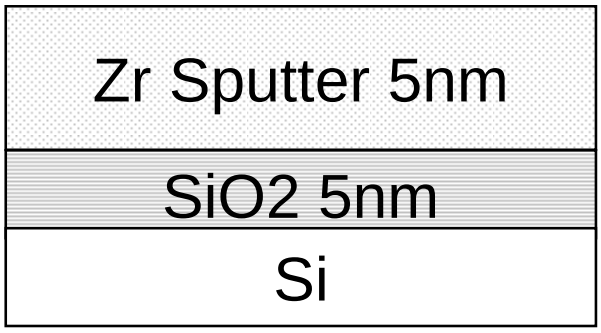


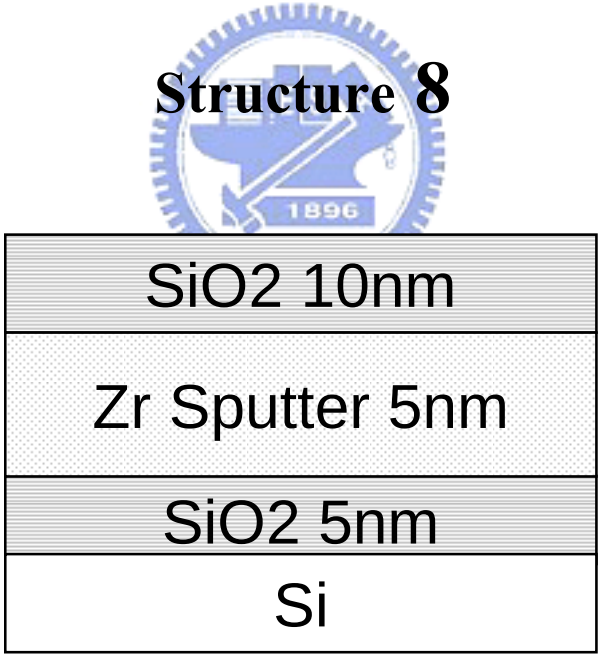
Figure 3-9 The thermal process flow of structure 6

Structure 7



(a)

Structure 8



(b)

Figure 3-10 (a) Sample structure of structure 7 (b) Sample structure of structure 8

Structure 7

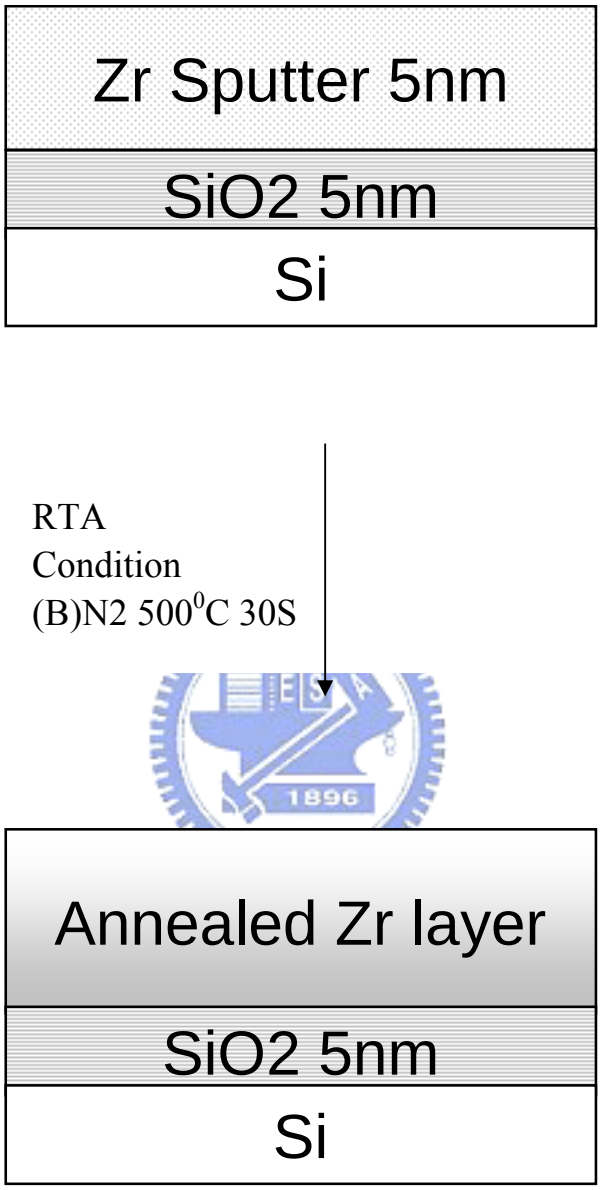


Figure 3-11 The thermal process flow of structure 7

Structure 8

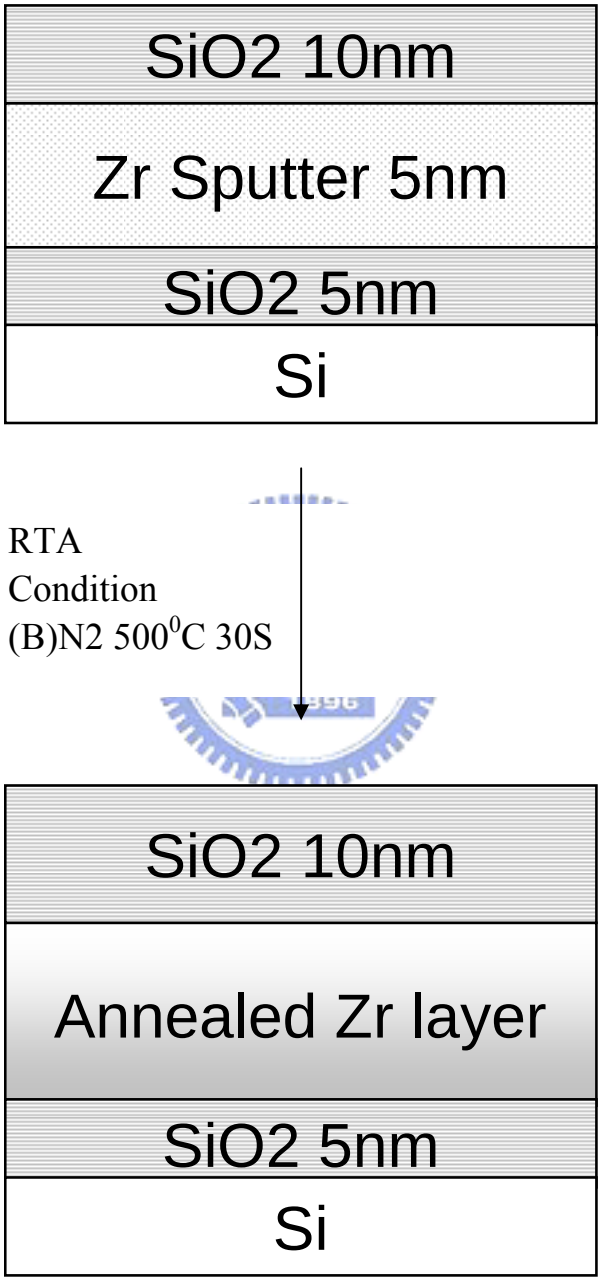


Figure 3-12 The thermal process flow of structure 8

Chapter 4

Experiment Results and Discussion

4.1 Introduction

The bidirectional *C-V* sweeps were performed from deep inversion to deep accumulation and in reverse, which exhibited an electron charging effect. The nanocrystals (the charge storage layer) embedded in SiO_2 layer of a MONOS memory device is utilized to capture the injected carriers from the channel, which cause a variation in the threshold voltage of the memory device. When the device is programmed, the electrons directly tunnel from the Si substrate through the tunnel oxide by Fowler-Nordheim (F-N) tunneling and they are trapped in the charge storage layer. For the erase, the holes may tunnel from the valence band of the Si substrate and recombine with the electrons trapped in the charge storage layer, or the electrons tunnel back to the Si substrate from the charge storage layer. The control oxide is utilized to prevent the carriers injecting into the charge-trapping layer by Fowler-Nordheim (F-N) tunneling from gate electrode. In several oxidation conditions, the electrons and holes injections into the nanocrystals layer are easier from the gate than from the Si substrate. If the thermal budget such as oxidation temperature and time are well controlled, the memory effect will be improved.

4.2 Ge/Zr double layer structure

4.2.1 Electrical Characteristics

The capacitance-voltage (C-V) hysteresis of standard **structure 1** with is shown in Figure 4-1. There is no obvious memory effect after bidirectional voltage sweep. The standard Ge/Zr doubled layer without any thermal treatment exhibits no charge

storage ability. However, the C-V characteristics for Ge/Zr doubled layer structure after RTA treatment at the condition, 500C for 30sec in nitrogen ambient is as shown in Figure 4-2. There is 3 V memory windows after 10 V bidirectional voltage sweep. However, the C-V characteristic of **structure 2** after the same thermal treatment condition is as shown Figure 4-3. Under 10 V bidirectional voltage sweep, the memory effect is not clear as shown in Fig. 4-3. Figure 4-4 exhibits the C-V characteristics for the sample 2 after RTA treatment at 600C, 30sec in nitrogen ambient. The memory effect is occurred as the thermal treatment temperature increasing (from 500C to 600C). It is considered that thermal budget is affected by capping SiO2 during thermal treatment. The capped SiO2 Zr/Ge stacked structure needs more thermal budget to form ZrGe alloy which can support trapping centers for injection charge storage.

In addition, the electrical reliability characteristics, such as retention time and endurance, were also investigated in this study. The retention and the leakage current characteristics of structure 1 after RTA treatment at 500C, 30sec in nitrogen ambient are as shown in Figure 4-5, and 4-6, respectively. Hence, the charges can not store in the charge storage center for long duration for the obvious leakage current was measured in the structure 1 for standard. Figure 4-7 and 4-8 exhibit the retention time and leakage current characteristics for structure 2 after RTA treatment at 600C, 30sec in nitrogen ambient. The superior retention characteristics were obtained due to the lower leakage current than structure 1 for standard. The quality of capped oxide on Zr/Ge double layer structure after thermal treatment must be improved. Hence, the stronger oxide can resist the storage charge leak to gate.

The endurance characteristics of structure 2 after RTA treatment at 600C, 30sec in nitrogen ambient for program/erase operation are as shown in Figure 4-9.The

obvious memory widow can be kept after 10^6 program/erase cycles. However, the threshold voltages for program and erase operation both shift to positive voltage, even if the memory window can be distinguished. It is considered that the negative oxide trapped causes the positive voltage shift.

4.2.2 Material analysis

The transmission electron microscope (TEM) diagrams of standard structure 1 and structure 1 after thermal treatment is shown in Figure 4-10 and 4-11, respectively. The tunneling oxide is about 5-nm-thick and the trapping layer is about 10-nm-thick. It is think that the standard Zr/Ge double layers can be distinguished two layers Ge layer and Zr layer.The Ge layer and Zr layer are about 6-nm-thick and 4-nm-thick, respectively. However, the Zr/Ge double layers after RTA treatment (at the condition 500C for 30sec in nitrogen ambient) becomes a well mixed layer. It can be evidenced from the X-ray photoelectron spectroscopy (XPS) analysis as shown in Figure 4-12 and Figure 4-13[4.1] [4.2].It indicates that the Zr/Ge double layer before thermal treatment is only with Ge-Ge and Zr-Zr bond. However, the Zr-Ge bond is formed after thermal treatment, including partial Ge-Ge and Ge-O2 signals which are believed contributed from un-acted Ge component and native oxide of Ge surface.

4.3 Ge-Zr cosputtering layer structure

4.3.1 Electrical Characteristics

The Zr-Ge mixed layer was prepared by sputtering Zr target and Ge target in vacuum. The capacitance-voltage (C-V) hysteresis of **structure 3** for standard and treat by RTA 500C, 30sec in nitrogen ambient are shown in Figure. 4-14 and 4-15**.** It is found that the memory window is 8V under ±10V C-V sweeping for the **structure 3** before any thermal treatment. Unlike Zr/Ge double layer structure, cosputtering Zr-Ge structure can desire memory effect without thermal treatment. It is considered

that the as-deposited Zr-Ge mixed layer may be partial alloy which get more charge storage centers. As shown in Figure 4-15, the 9V memory window under ±10V C-V sweeping of **structure 3** after RTA treatment at the condition, 500C for 30sec in nitrogen ambient. The enhanced memory effect was found for **structure 3** after theraml treatment, due to the Zr-Ge alloy can be formed. It is believed that the mixed Zr-Ge layer is more easily to form Zr-Ge alloy than Zr/Ge double layer.

However, the capped oxide effect was also discussed. Figure 4-16 shows the C-V hysteresis of Zr-Ge cosputtering layer as charge trapping layer after thermal treatment (RTA 500C N2 30sec). Under ±10V bidirectional voltage sweep, the 11V memory window is obtained. The more obvious memory window was desired than structure 3 and **structure 3** after thermal treatment (RTA 500C N2 30sec). However, the memory effect is a little affected by capped oxide on cosputtering Zr-Ge layer after thermal annealing.

Also, the retention and leakage current were also discussed for **structure 3**, **structure 3** after thermal treatment(RTA 500C N2 30sec), and **structure 4** after thermal treatment (RTA 500C N2 30sec)as shown in Figure 4-17, 4-18, 4-19, 4-20, 4-21, and 4-22, respectively. The proposed structures with cosputtering Zr-Ge layer as charge trapping layer get more superior retention characteristics and leakage current. The obvious memory effect must be from the contribution of lower leakage current.

In addition, the endurance characteristics of structure 3, structure 3 after thermal treatment (RTA 500C N2 30sec) ,and structure 4 (after RTA treatment at 500C, 30sec in nitrogen ambient) for program/erase operations are as shown in Figure 4-23, 4-24 and 4-25, respectively. The obvious memory widow can be kept after 10^6 program/erase cycles. Even if the threshold voltages for program and erase operation also both shift to positive voltage, the memory window can be distinguished.

4.3.2 Material analysis

The transmission electron microscope (TEM) diagrams of structure 3 before thermal treatment and after thermal treatment are shown in Figure 4-26 and 4-27.Tunneling oxide is about 5nm and trapping layer is about 8nm.It is considered that the Zr-Ge cosputtered layer was a more well mixed layer compared to Zr/Ge double layer structure which need a thermal treatment let Zr and Ge to mix. The X-ray photoelectron spectroscopy (XPS) analysis of structure 3 before thermal treatment and after thermal treatment for Ge 3d spectra and Zr 3d spectra are shown in Figure 4-28, and Figure 29, respectively [4.1] [4.2]. It is found that structure 3 desired obvious Zr-Ge bonds for as-deposited and after thermal treatment. The XPS analysis of structure 3 for as-deposited Zr-Ge cosputtered layer still are contributed from partially Ge-Ge bonds and Ge-O2 bonds.

4.4 Ge single layer

4.4.1 Electrical Characteristics

The C-V hysteresis of **structure 5** (Ge single layer) without thermal treatment is as shown in Figure 4-30. The memory window is about 0.5V under ±10V bidirectional voltage sweeping. However, the memory effect is eliminated for **structure 5** after RTA treatment at the condition, 500C for 30sec in nitrogen ambient is as shown in Figure 4-31. Figure 4-32 exhibits the C-V characteristics for the **structure 6** (Ge single layer) after RTA treatment at 500C, 30sec in nitrogen ambient. The memory effect is occurred as we capped a PECVD SiO2 before thermal treatment. The memory window is 5V under ±10V C-V sweeping. When a Ge-Ge structure sample without capping anything annealed in 500C 30sec in nitrogen ambient, Ge will be out diffusion. Hence, it is found that **structure 5** after RTA treatment at the condition, 500C for 30sec in nitrogen ambient exhibits no charge storage ability for

the Ge layer out diffusion in the thermal ambient. On the contrary, the **structure 6 (Ge layer capped oxide)** after RTA treatment at the condition, 500C for 30sec in nitrogen ambient with capping oxide before thermal treatment so the SiO2 can prevent Ge out diffusion. Hence, there is a little memory window in **structure 6** treated by RTA 500C N2 30sec. In Figure 4-30, the standard **structure 5** also desired a little memory window for the low temperature capped oxide can prevent the Ge out diffusion.

4.4.2 Material analysis

The transmission electron microscope (TEM) diagrams of structure 6 after thermal treatment are shown in Figure 4-33. The tunneling oxide and trapping oxide are about 5nm.It is considered that a part of Ge aggregated during thermal treatment. The X-ray photoelectron spectroscopy (XPS) analyses of structure 5 for as-deposited and after thermal treatment are shown in Figure 4-34[4.1] [4.2]. It is found that Ge-Ge bonds and Ge-O_2 bonds are existed in structure5 before thermal treatment. The Ge and Ge surface native oxide are also main components in the analyzed samples. However, the only Ge-O2 bonds exists after thermal treatment. It is reported that the Ge atoms outgas to the ambient in the oxygen-existed ambient [4.3]. Hence, it is believed that the Ge-O2 signal is the contribution from the surface oxide of the existed Ge layer.

4.5 Zr single layer

4.5.1 Electrical Characteristics

The capacitance-voltage (C-V) hysteresis of **structure 7** (Zr single layer) for standard and after RTA treatment at the condition, 500C for 30sec in nitrogen ambient are shown in Figure 4-35 and 4-36, respectively. Also, the C-V characteristics of **structure 8** after RTA treatment at the condition, 500C for 30sec in nitrogen ambient

is shown in Figure 4-37. The memory windows are ~0V in the above thermal treatment conditions on **structure 7**.

4.5.2 Material analysis

It is considered that Zr layer is still conductor after thermal annealing in nitrogen ambient. Hence, no expected memory effects were observed in the proposed **structure 7**.

The X-ray photoelectron spectroscopy (XPS) analyses of structure 7 for as-deposited and thermal treatment are shown in Figure 4-38[4.1] [4.2]. It is found that the Zr-Zr bonds in structure 7 in both conditions.

4.6 Summery

The Ge and Zr single layer structures can not obtain the obvious memory effects. However, the Zr-Ge mixed layer and Zr/Ge double layer contribute the memory windows. It is considered that the contributions of memory effects are from the Zr-Ge alloy. Also, the capped oxide on the proposed structure affect the alloy formation in this study. ZrGe on nonvolatile memory had been fabricated with appropriate control of the process temperature and annealing time. Capping a oxide before annealing to improve electric characteristic is useful. Cosputtering structure can gain a bigger memory window than layer by layer structure.

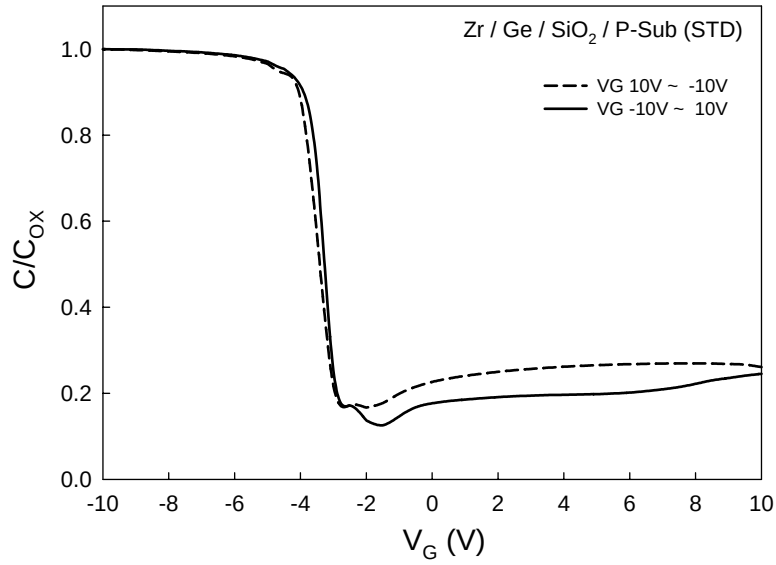


Figure 4-1 The capacitance voltage (C-V) hysteresis of structure 1 for standard under ±10V bidirectional voltage sweeping.

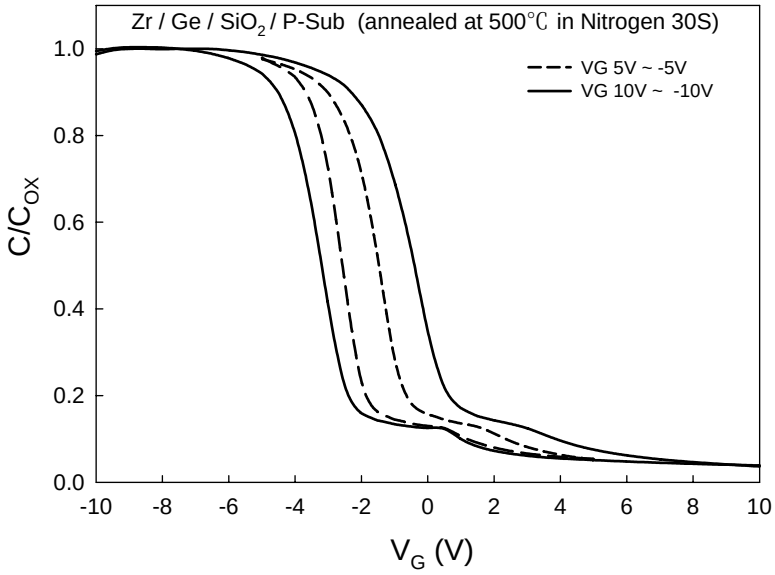


Figure 4-2 The capacitance voltage (C-V) hysteresis of structure 1 after thermal treatment (RTA 500C N2 30S) under ±5V and ±10V bidirectional voltage sweeping.

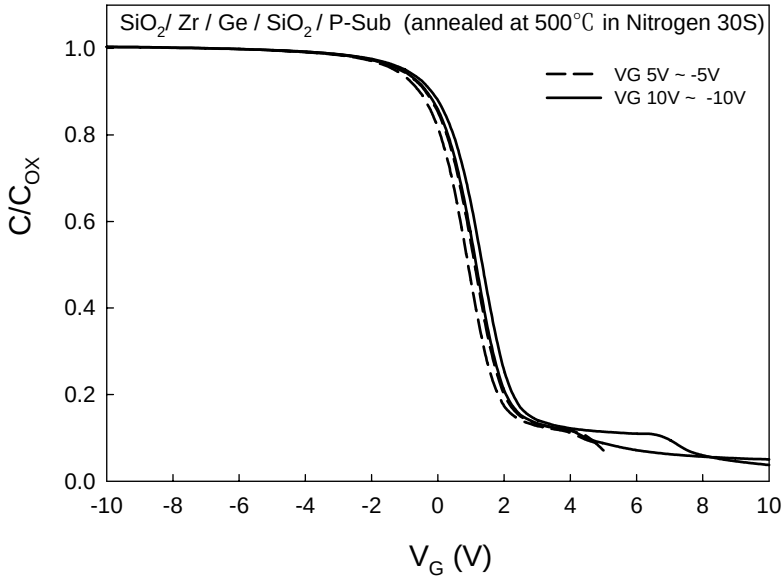


Figure 4-3 The capacitance voltage (C-V) hysteresis of structure 2 after thermal treatment (RTA 500C N2 30S) under ±5V and ±10V bidirectional voltage sweeping.

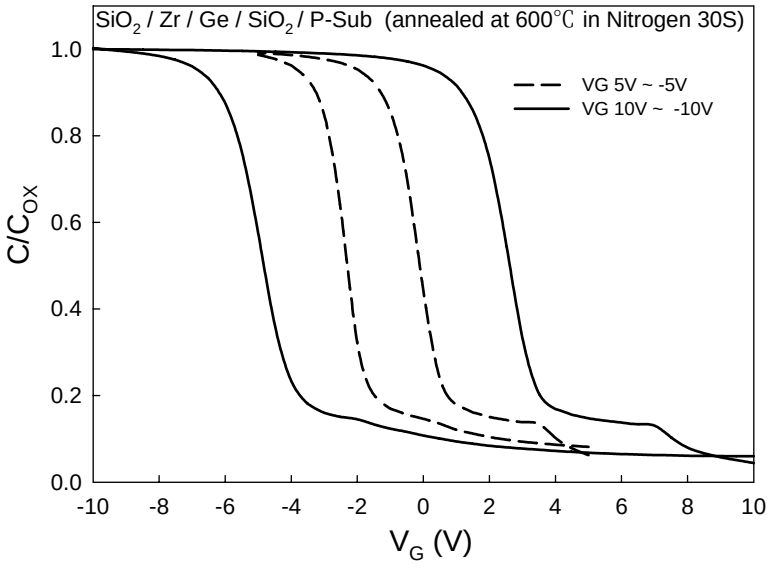


Figure 4-4 The capacitance voltage (C-V) hysteresis of structure 2 after thermal treatment (RTA 600C N2 30S) under ±5V and ±10V bidirectional voltage sweeping.

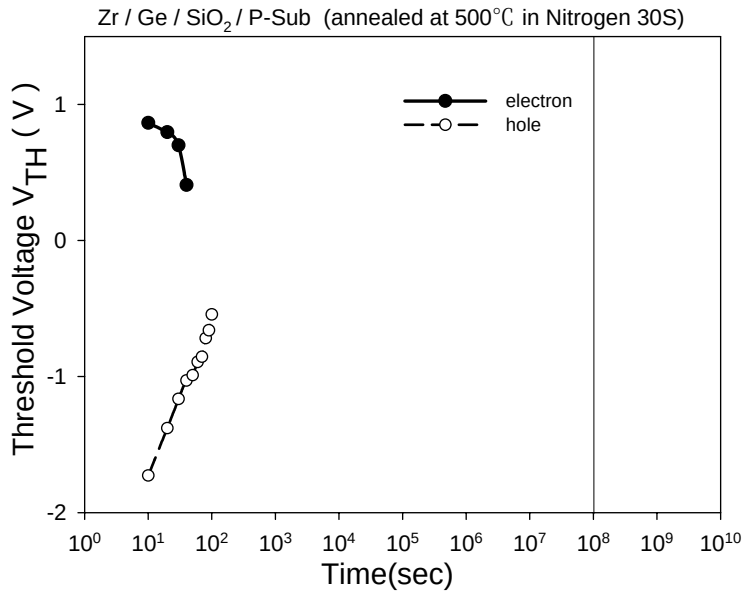


Figure 4-5 The retention hysteresis of structure 1 after thermal treatment (RTA 500C N2 30S)

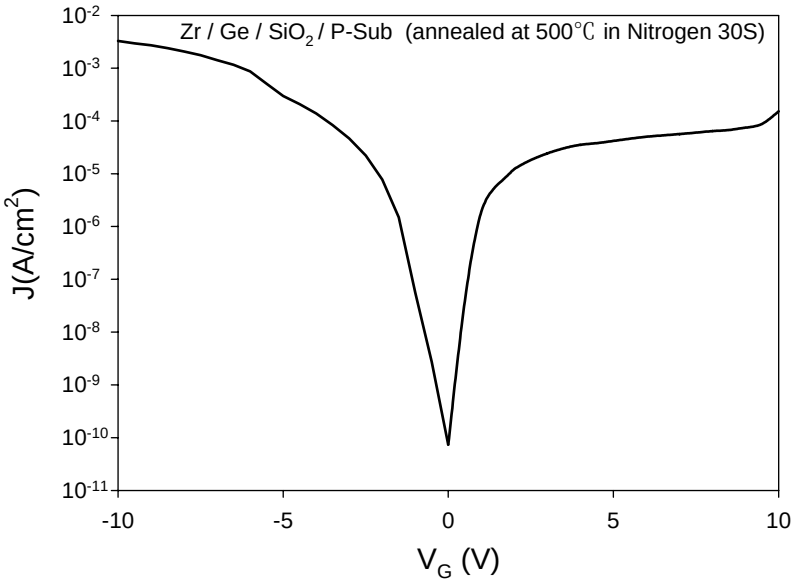


Figure 4-6 The leakage current character of structure 1 after thermal treatment (RTA 500C N2 30S)

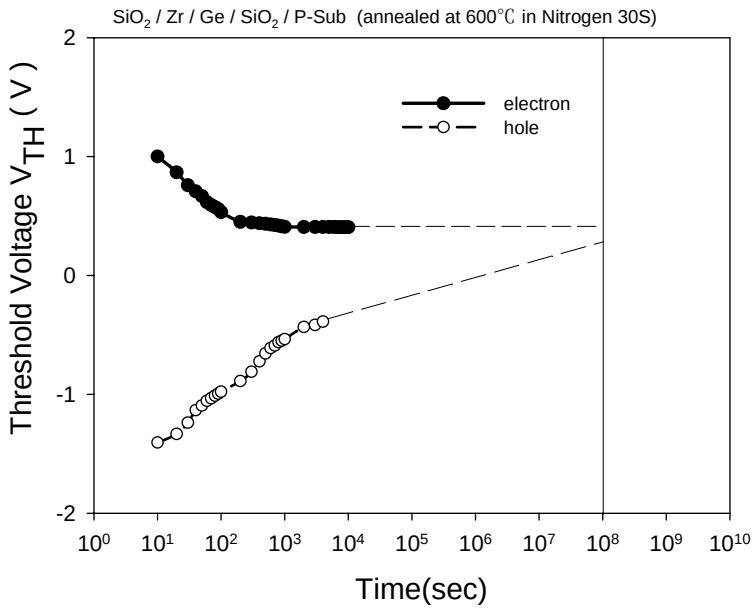


Figure 4-7 The retention hysteresis of structure 2 after thermal treatment (RTA 600C N2 30S)

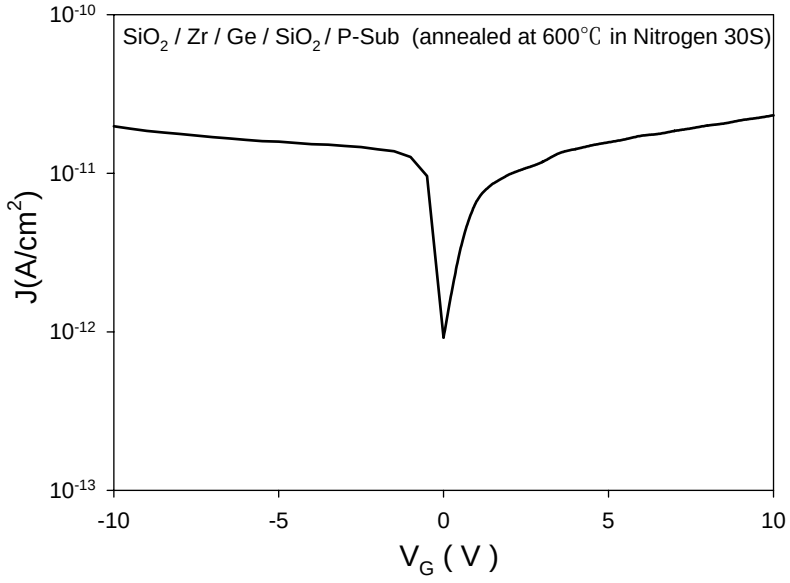


Figure 4-8 The leakage current character of structure 2 after thermal treatment (RTA 600C N2 30S)

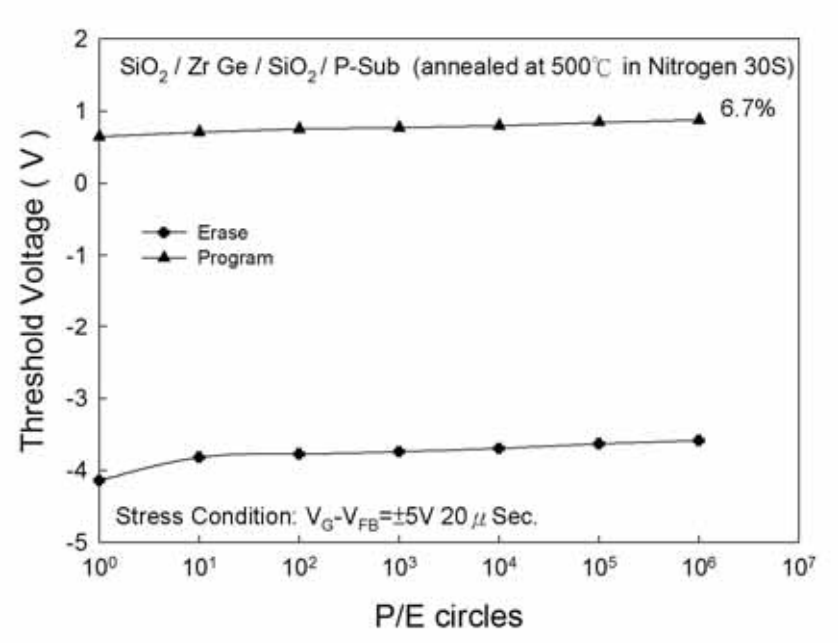


Figure 4-9 The endurance character of structure 2 after thermal treatment (RTA 600C N2 30S)

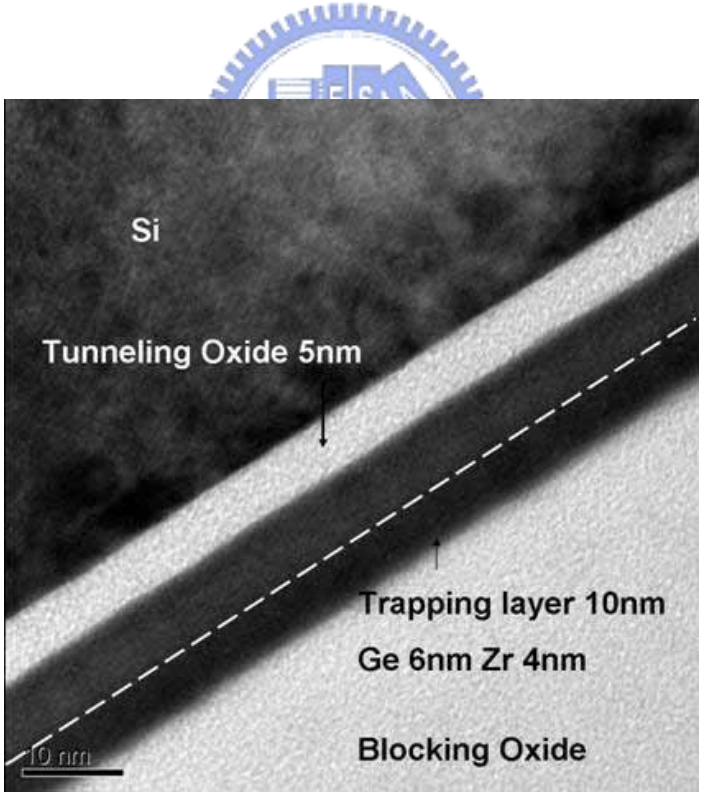


Figure 4-10 The transmission electron microscope (TEM) diagrams of standard structure 1

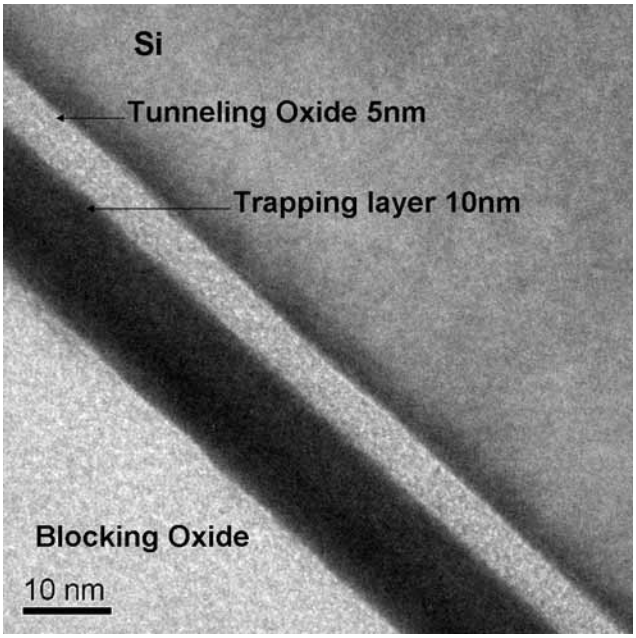


Figure 4-11 The transmission electron microscope (TEM) diagrams of structure 1 after thermal treatment after thermal treatment (RTA 500C N2 30S)

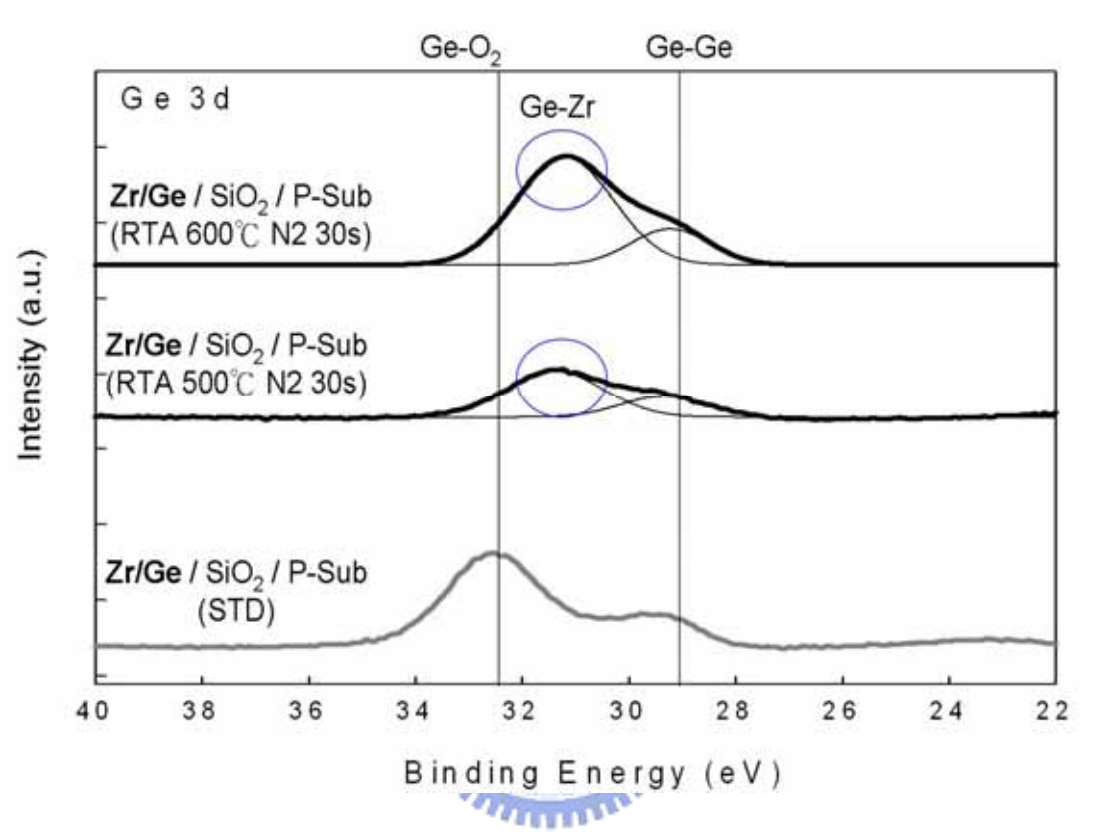


Figure 4-12 The X-ray photoelectron spectroscopy (XPS) analysis of structure1 for standard, after RTA treatment at the condition 500C for 30sec in nitrogen ambient and structure 2 after RTA treatment at the condition 600C for 30sec in nitrogen ambient for Ge 3d spectra.

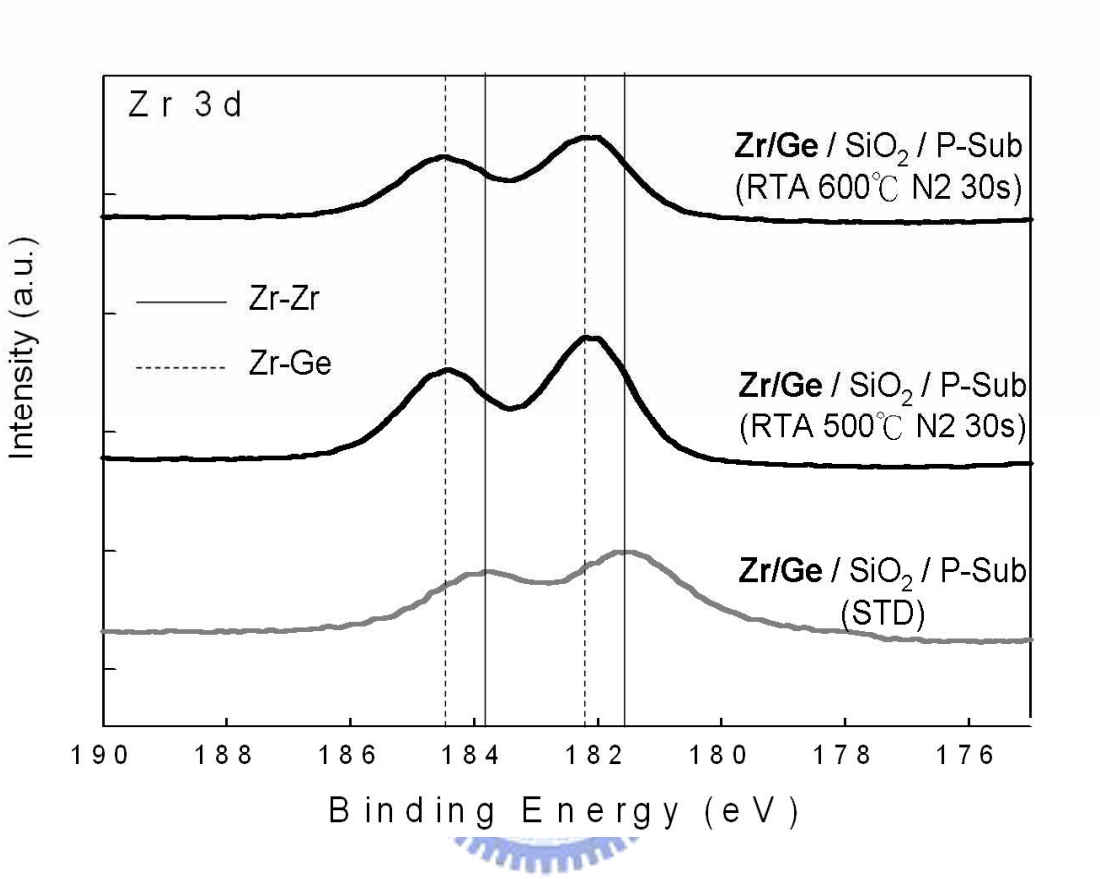


Figure 4-13 The X-ray photoelectron spectroscopy (XPS) analysis of structure1 for standard, after RTA treatment at the condition 500C for 30sec in nitrogen ambient and structure 2 after RTA treatment at the condition 600C for 30sec in nitrogen ambient for Zr 3d spectra.

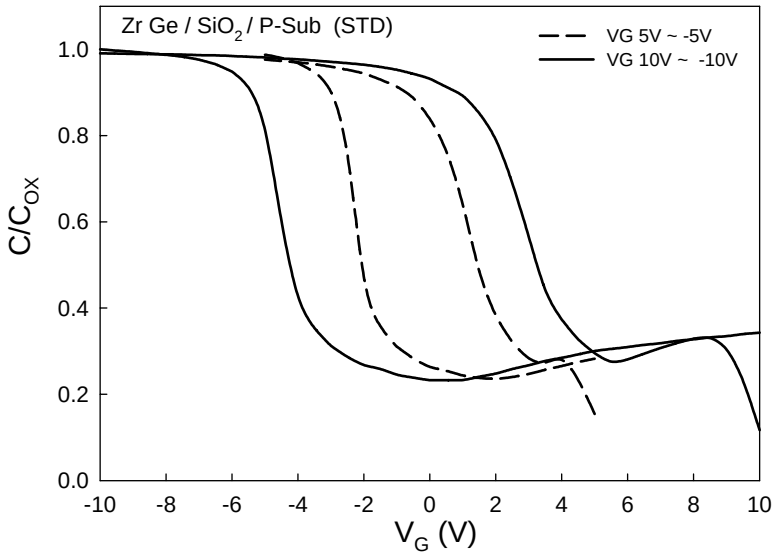


Figure 4-14 The capacitance voltage (C-V) hysteresis of structure 3 for standard under ±5V and ±10V bidirectional voltage sweeping.

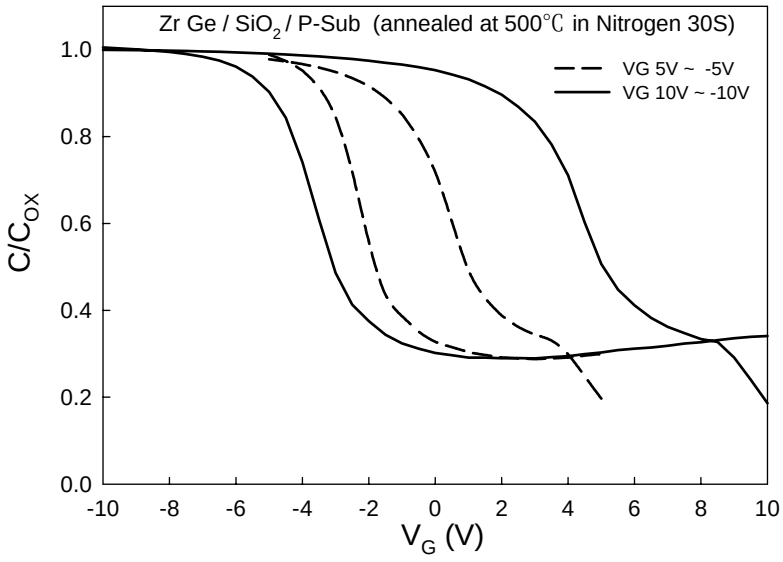


Figure 4-15 The capacitance voltage (C-V) hysteresis of structure 3 after thermal treatment (RTA 500C N2 30S) under ±5V and ±10V bidirectional voltage sweeping.

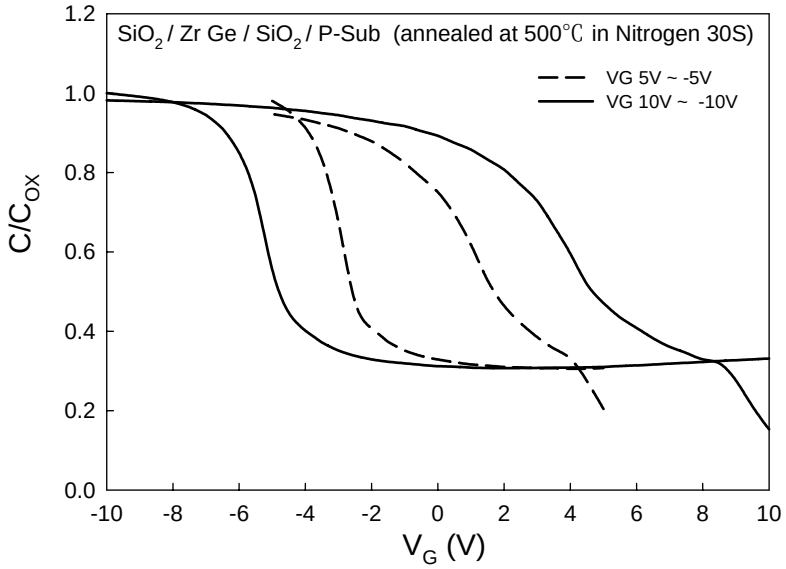


Figure 4-16 The capacitance voltage (C-V) hysteresis of structure 4 after thermal treatment (RTA 500C N2 30S) under ±5V and ±10V bidirectional voltage sweeping.

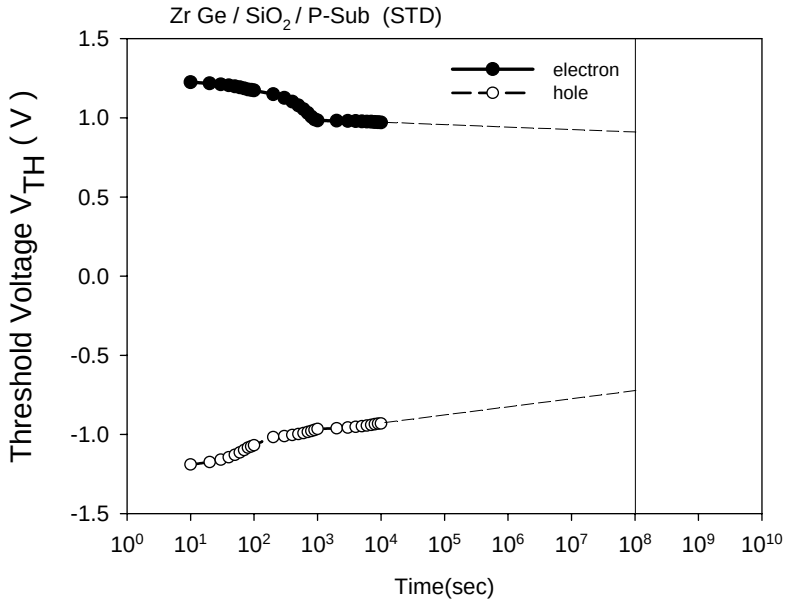


Figure 4-17 The retention hysteresis of structure 3 for standard

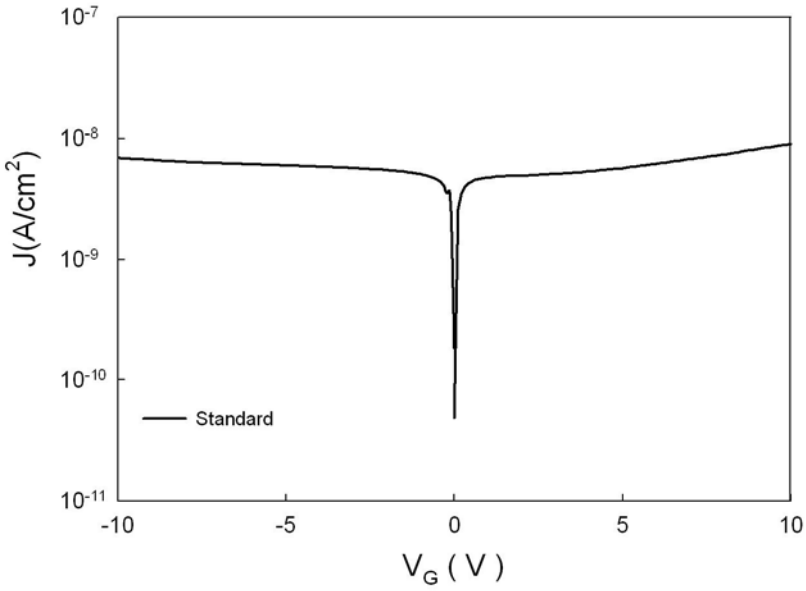


Figure 4-18 The leakage current character of structure 3 for standard

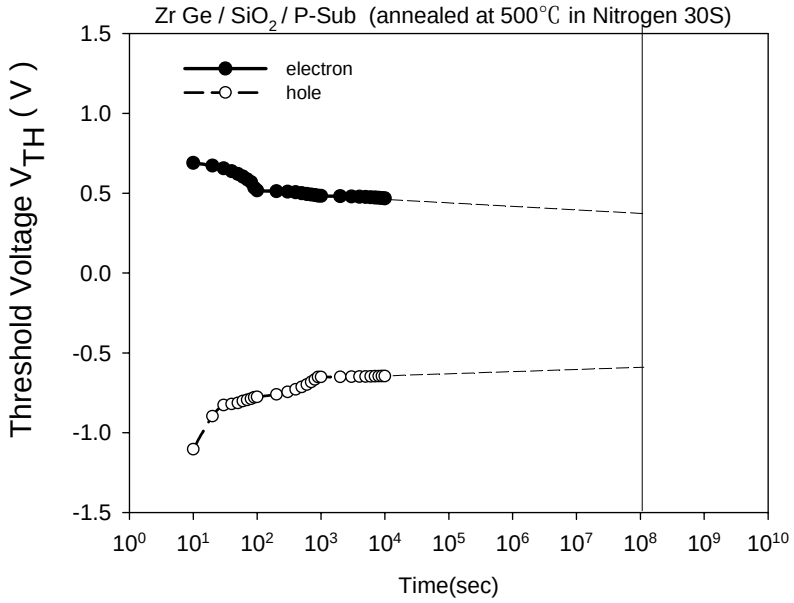


Figure 4-19 The retention hysteresis of structure 3 with after thermal treatment (RTA 500C N2 30S)

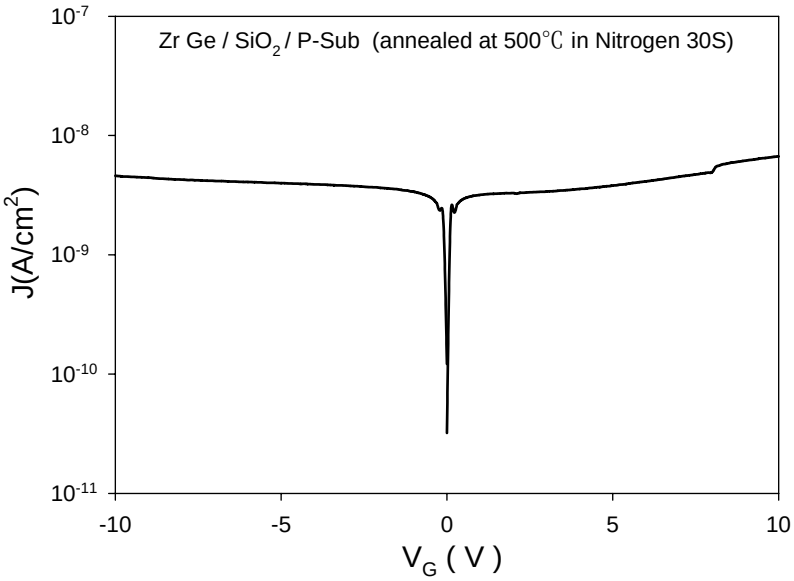


Figure 4-20 The leakage current character of structure 3 after thermal treatment (RTA 500C N2 30S)

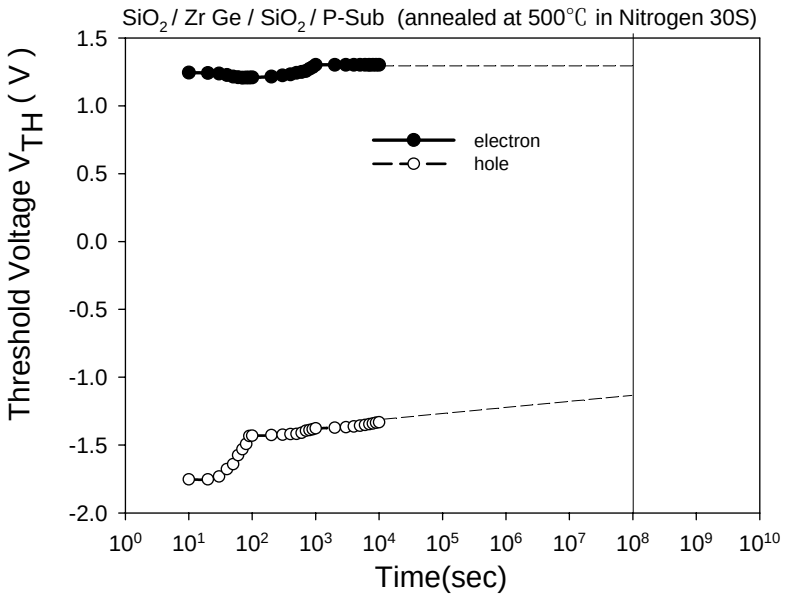


Figure 4-21 The retention hysteresis of structure 4 after thermal treatment (RTA 500C N2 30S)

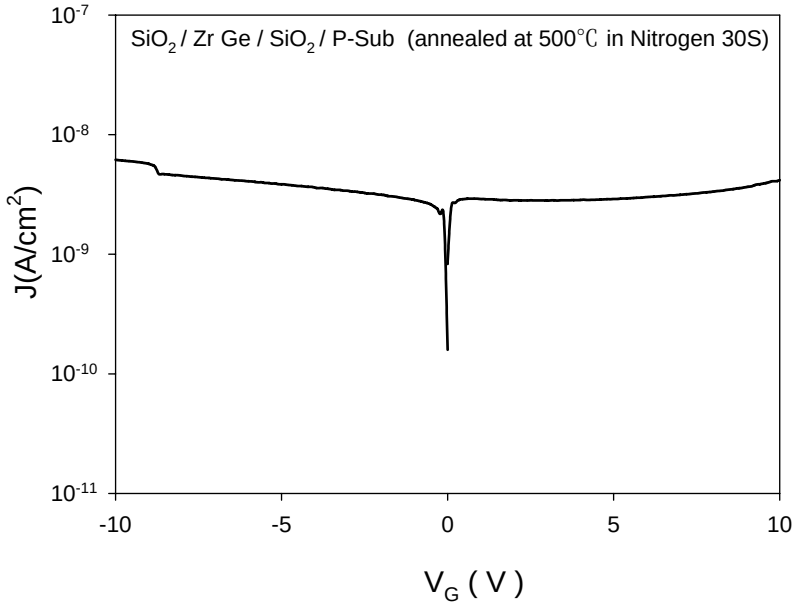


Figure4-22 The leakage current character of structure 4 after thermal treatment (RTA 500C N2 30S)

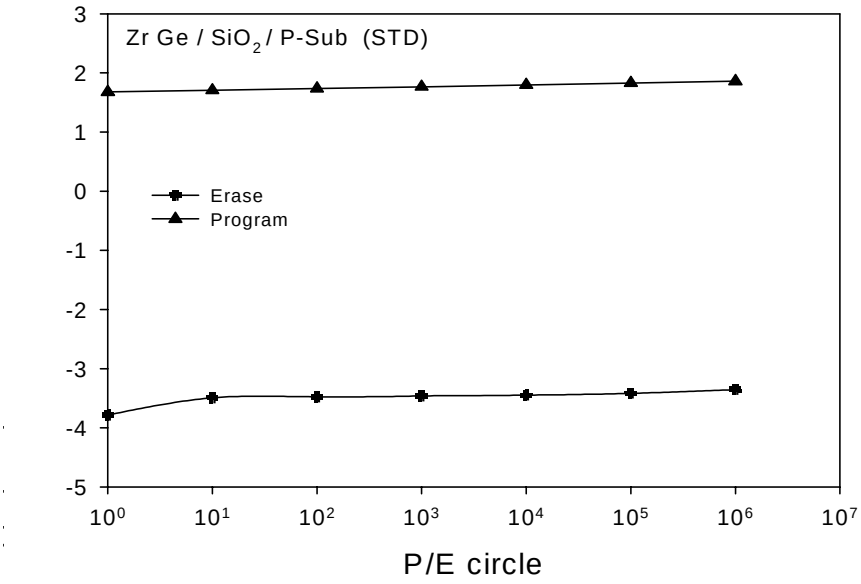


Figure4-23 The endurance character of structure 3 for standard

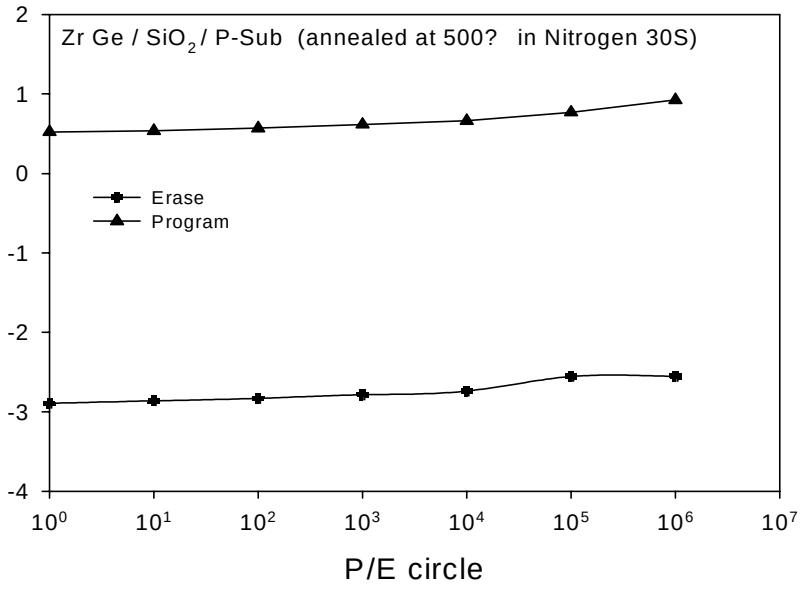


Figure4-24 The endurance character of structure 3 after thermal treatment (RTA 500C N2 30S)

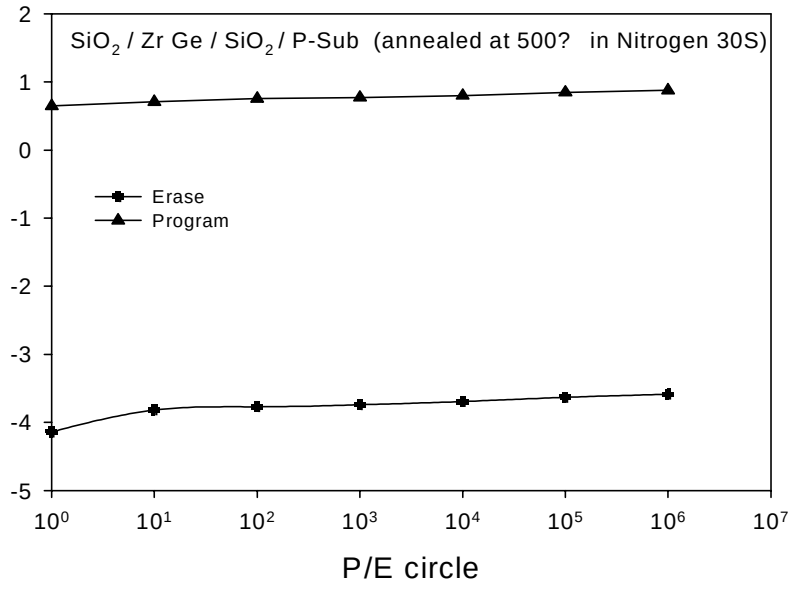


Figure4-25 The endurance character of structure 4 after thermal treatment (RTA 500C N2 30S)

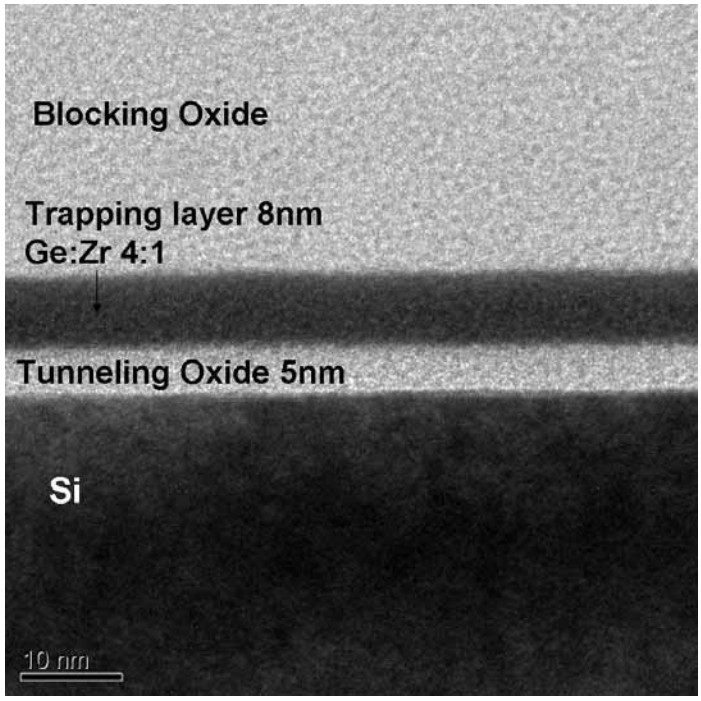


Figure4-26 The transmission electron microscope (TEM) diagrams of structure 3 for standard

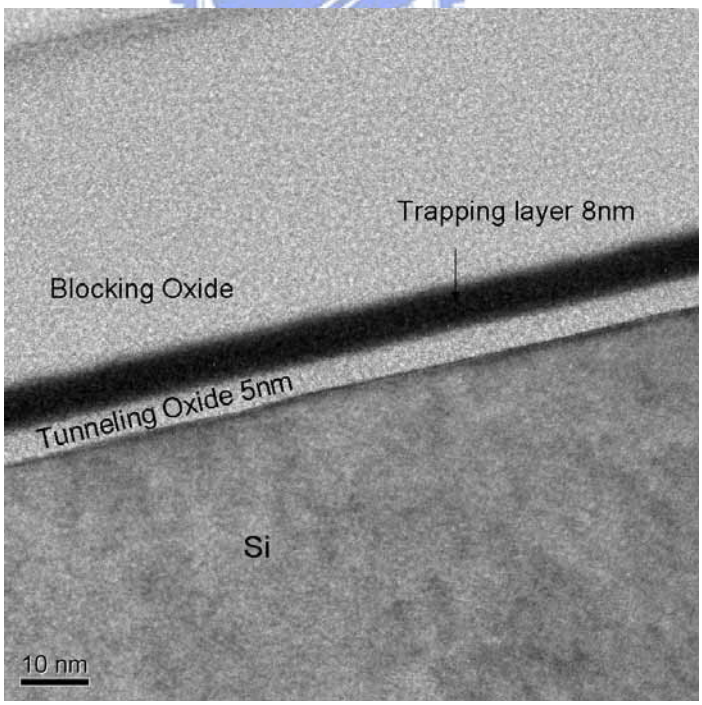


Figure4-27 The transmission electron microscope (TEM) diagrams of structure 3 after thermal treatment (RTA 500C N2 30S)

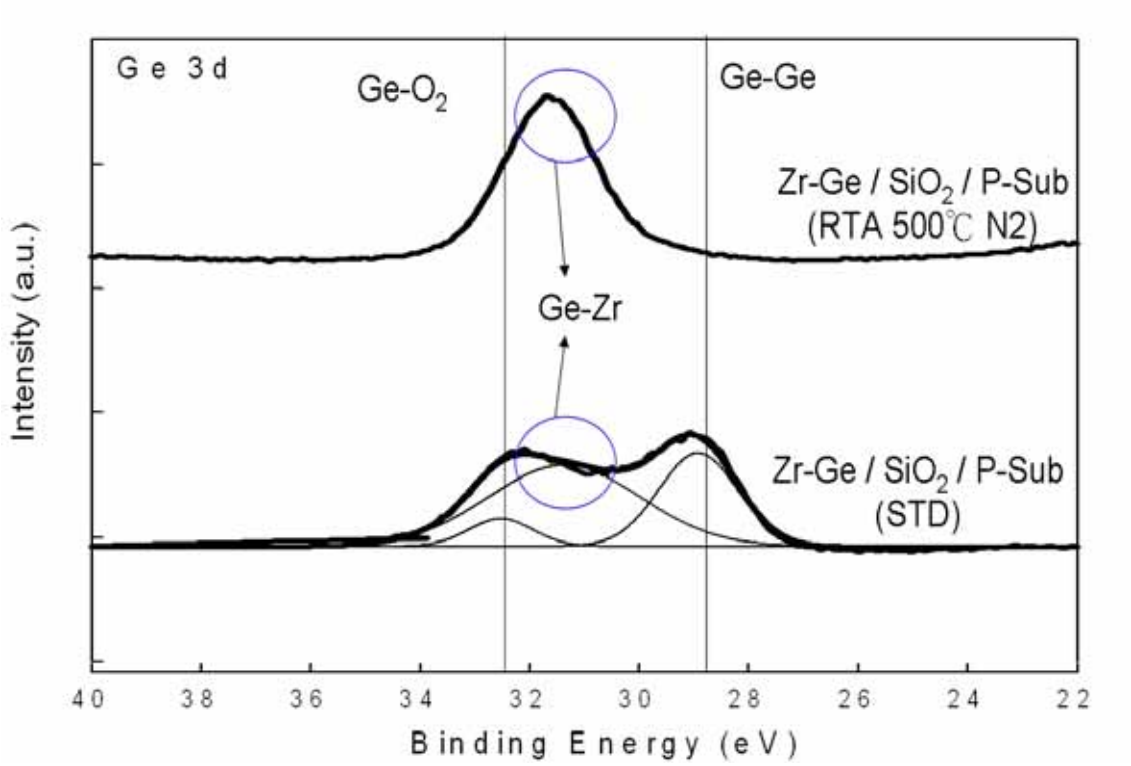


Figure4-28 The X-ray photoelectron spectroscopy (XPS) analysis of structure3 for standard, after RTA treatment at the condition 500C for 30sec in nitrogen ambient for Ge 3d spectra

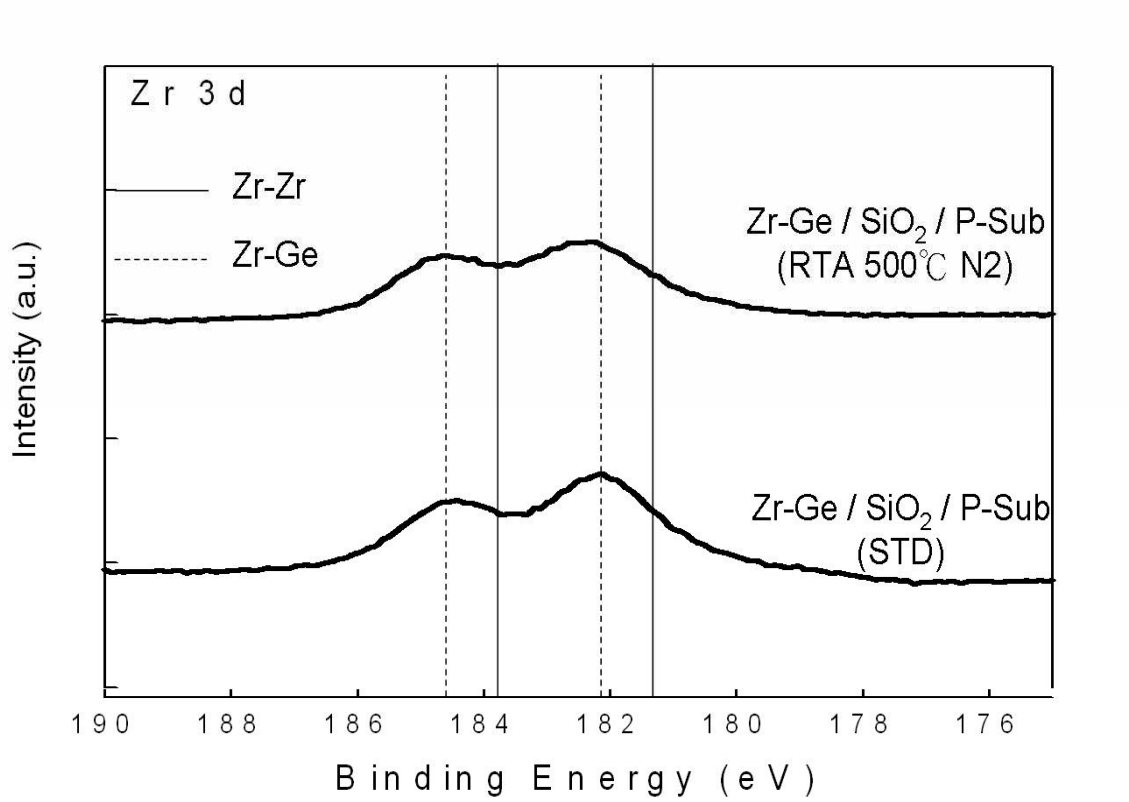


Figure4-29 The X-ray photoelectron spectroscopy (XPS) analysis of structure3 for standard, after RTA treatment at the condition 500C for 30sec in nitrogen ambient for Zr 3d spectra

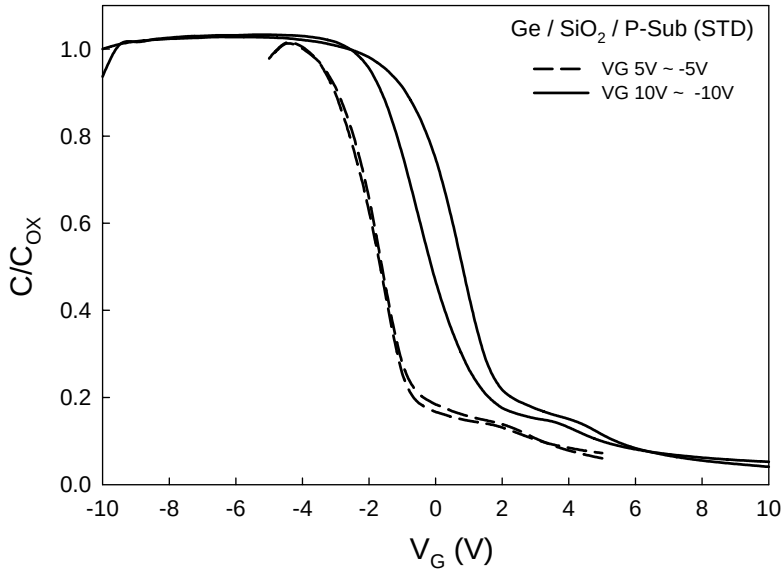


Figure 4-30 The capacitance voltage (C-V) hysteresis of of sample5 for standard under ±5V ±7V and ±10V bidirectional voltage sweeping.

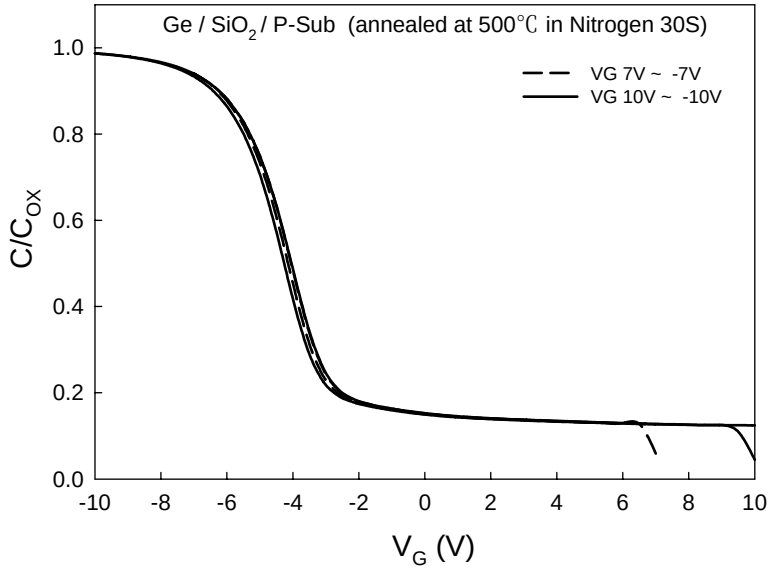


Figure 4-31 The capacitance voltage (C-V) hysteresis of structure 5 after thermal treatment (RTA 500C N2 30S) under ±7V and ±10V bidirectional voltage sweeping.

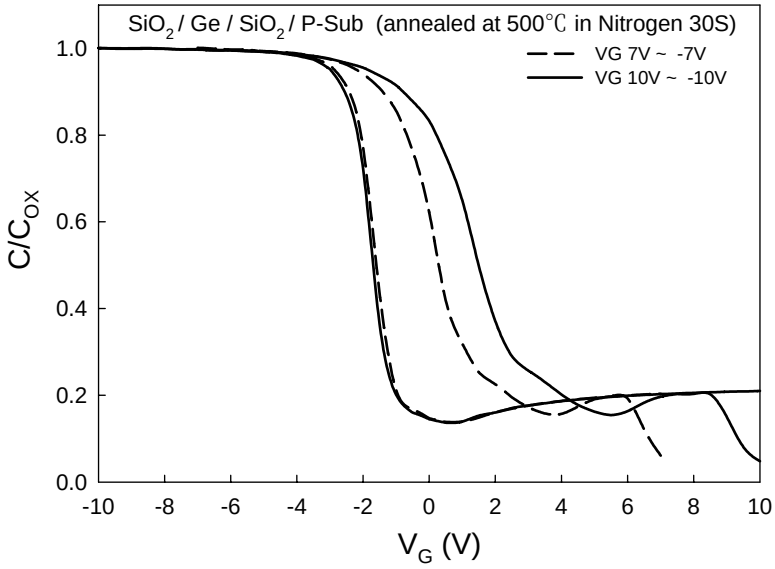


Figure 4-32 The capacitance voltage (C-V) hysteresis of structure 6 after thermal treatment (RTA 500C N2 30S) under ±5V, ±7Vand ±10V bidirectional voltage sweeping.

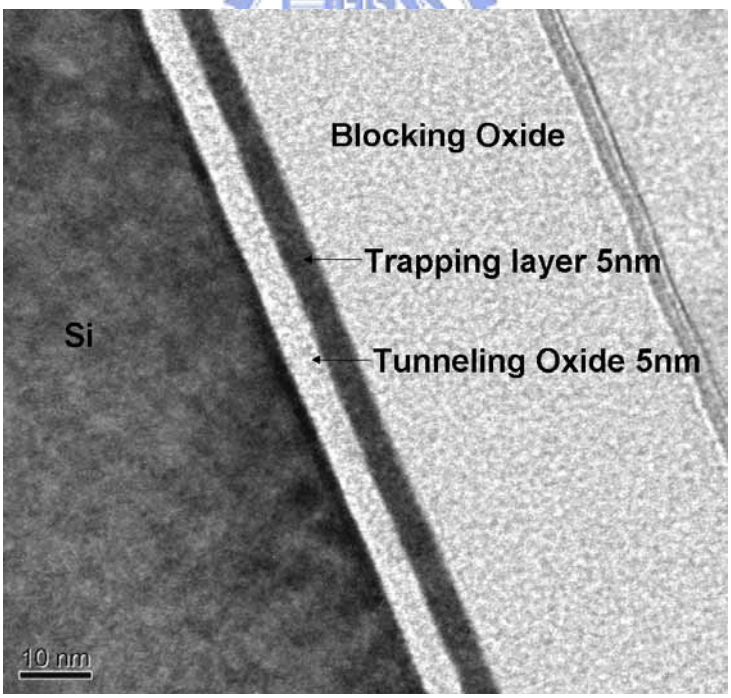


Figure4-33 The transmission electron microscope (TEM) diagrams of structure 6 after thermal treatment (RTA 500C N2 30S)

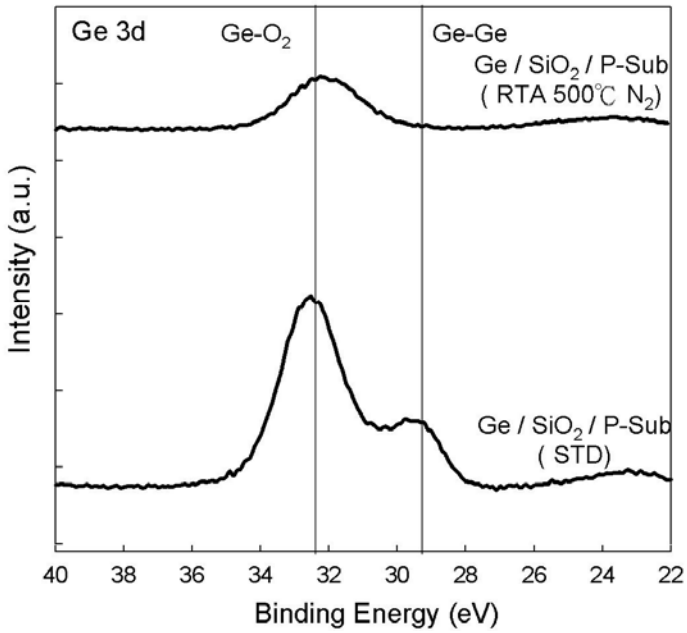


Figure4-34 The X-ray photoelectron spectroscopy (XPS) analysis of structure5 for standard, after RTA treatment at the condition 500C for 30sec in nitrogen ambient for Ge 3d spectra

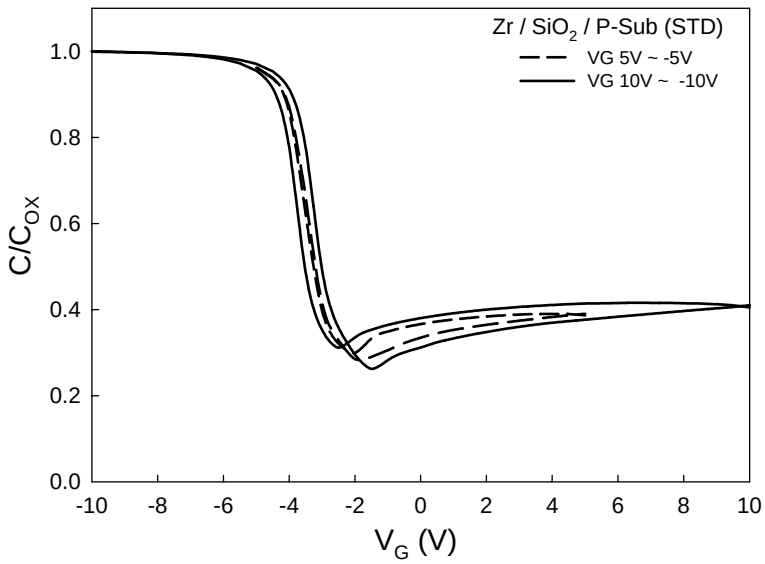


Figure 4-35 The capacitance voltage (C-V) hysteresis of of structure 7 for standard under ±5V and ±10V bidirectional voltage sweeping.

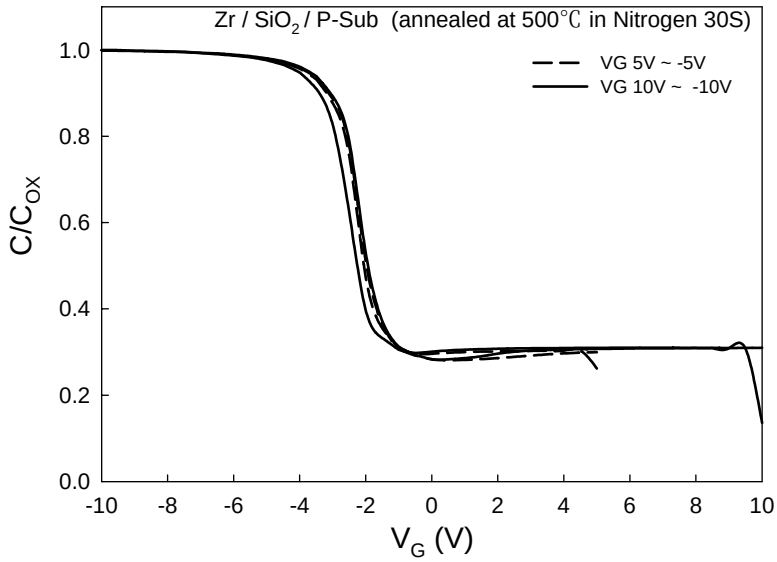


Figure 4-36 The capacitance voltage (C-V) hysteresis of structure 7 after thermal treatment (RTA 500C N2 30S) under ±7V and ±10V bidirectional voltage sweeping.

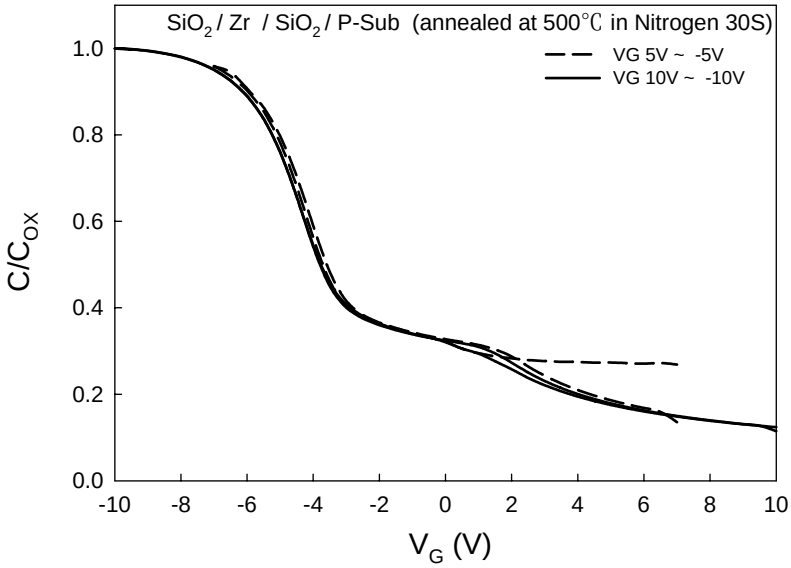


Figure 4-37 The capacitance voltage (C-V) hysteresis of structure 8 after thermal treatment (RTA 500C N2 30S) under ±7V and ±10V bidirectional voltage sweeping.

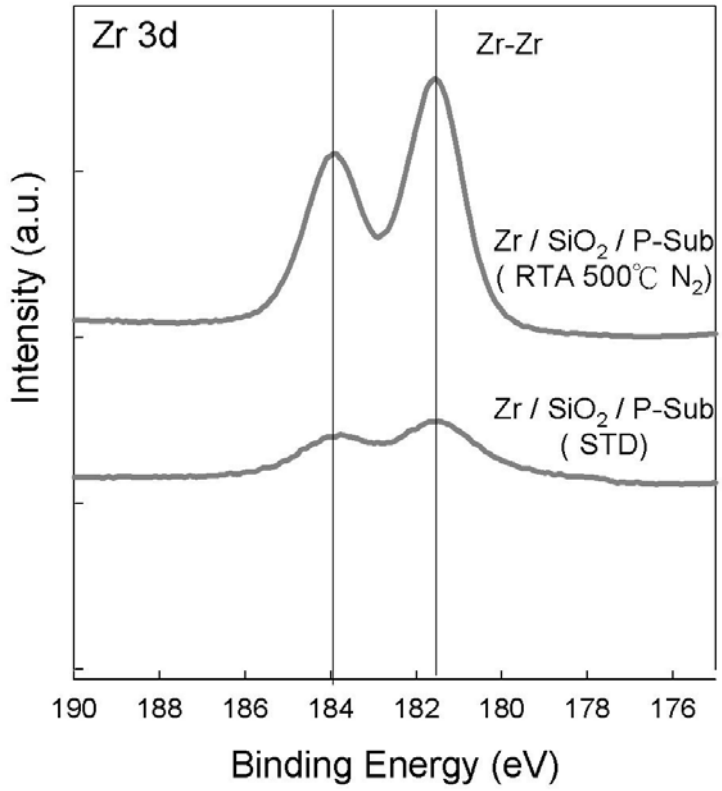


Figure4-38 The X-ray photoelectron spectroscopy (XPS) analysis of structure7 for standard, after RTA treatment at the condition 500C for 30sec in nitrogen ambient for Zr 3d spectra

Chapter 5

Conclusions

5.1 Conclusions

In this study, mew materials Zirconium-Germanium alloy has been successfully fabricated and investigated for the application on NVMS. However, the Zr single layer and Ge single layer are not suitable for charge trapping layer. The MONOS structure with Zr/Ge double layer and Zr-Ge mixed layer as charge trapping layer can support trapping centers for injected charge storage.

The memory windows for the MONOS structure with Zr/Ge double layers as charge trapping layer with capping PECVD SiO2 after RTA treatment at the condition, 600C for 30sec in nitrogen ambient is 8V under ±10V bidirectional voltage sweep. Furthermore, the MONOS structure with Zr-Ge cosputtering layer as charge trapping layer after RTA treatment at the condition, 500C for 30sec in nitrogen ambient is 11V under ±10V bidirectional voltage sweep.

The capping SiO2 before thermal treatment in this process has two major contributions. First, the SiO2 can prevent Ge out diffusion during thermal treatment. Second, the quality of SiO2 with thermal treatment is improved to reduce leakage current. Therefore, the proposed structure with capping SiO2 before thermal treatment can increase memory window and retention characteristics.

The fabrication processes are comparable with the main stream of semiconductor fabrication. The memory of Zr/Ge embedded in SiO2 dielectric is a potential candidate for future NVMS applications.