

Chapter 1

Introduction

1.1 Background

In recent years, the traditional cathode ray tube (so-called CRT) has become less and less in our daily life. The flat-panel display technology gradually turns to be much more popular in this modern society. Among this newest technology, thin film transistor liquid crystal display (so-called TFT-LCD) [1] [2] [3] [4] is the most well-established one. Cost of TFT-LCD is going to be lower and lower with the vast investment of many enterprises and it makes this field become more and more competitive with the conventional displays. However, TFT-LCD still has some inevitable drawbacks, such as : narrow viewing angle 、 slow response time 、 low contrast and so on. As a result, Active matrix organic liquid crystal displays (so-called AMOLED) [5] has attracted much more attention. AMOLED have a high contrast ratio, wide viewing angle, fast response time, high illuminant efficiency , one-third thin of TFT-LCD , flexible [6]. AMOLED doesn't need backlight behind liquid crystal, unlike TFT-LCD. OLED can be illuminant by itself so it can save more power without color filters. Besides, AMOLED can tolerate much more harsh conditions. It can apply to all over the world, including the polar and equatorial areas. Furthermore, low cost is an vital inducement. That is the reason why lots of enterprises and scientists want to invest in this promising field.

No matter TFT-LCD or AMOLED you choose, TFTs are the dominant elements for driving and switching functions. The characteristics of TFTs substantially impact the performance of these two displays. In General, hydrogenated amorphous TFTs (a-TFTs:H) [7]-[10] and low temperature poly TFTs (LTPS) [11]-[16]are major TFTs in the ordinary consuming products. For a-TFTs :H , dominant obstacles are low mobility and threshold voltage shift. However, low mobility can be resolved by enhancing the aspect ratio or the efficiency of luminance. And the compensation pixel circuit is expansively researched for threshold voltage shift issue. On the other hand, LTPS exhibits high mobility and good stability. LTPS can possess higher aperture and it can save more energy. Nevertheless, uniformity issue assures that LTPS inadequately apply in large and high resolution display panel. Therefore, a-TFTs :H have these merits which can't be replaced by poly TFTs. A-TFTs :H is the better choice in order to reduce the cost. Additionally, Uniformity is an inevitable element to make a large size panel.

1.2 Motivation

As the promising technology, AMOLED must have various disadvantages which scientists try to resolve. If a-TFT :H is set as the AMOLED driving element, the threshold voltage shift of a-TFT :H is the biggest obstacle in AMOLED pixel circuits. So far, process of a-TFT :H fabrication is well-established so that the threshold voltage is quite uniform. But it is severely shifted from its initial value by gate-bias stress [17].For OLED structure, the indium-doped tin oxide (ITO)

transparent anode of the OLED is made first on the active-matrix substrate because the sputtering of ITO would affect the quality of the organic active layer. In most hydrogenated amorphous TFT-OLED, the anode of OLED is connected to the source node of TFT. Hence, n-type TFT must consider the threshold voltage shift problem because the current of OLED is controlled by V_{GS} . Conventional pixel circuit, two-TFTs and one capacitor, is not good enough for AMOLED circuit because the output current which depends on the transfer characteristics of amorphous TFT sorely decreases with the threshold voltage shift of TFT. In consequence, the compensation scheme is necessarily to sustain the output current of OLED.

Recently, compensation pixel circuits with hydrogenated amorphous TFTs have been proposed. Numerous compensation methods have been developed such as voltage modulation [18]-[23] and current programming methods. [24] [25] [26] [27]. Current-programmed methods requires a long settling time at a low data current as the result of the high parasitic capacitance of data lines and inconvenient constant current sources. These are critical drawbacks for application to large and high-resolution displays. Therefore, we are going to introduce two new different voltage programming circuits to enhance the degradation of OLED output current in this thesis.

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Chapter 2

Source-follower type compensation circuit

2.1 Introduction

AMOLED have been considered as a promising technology for low cost displays on glass and plastic substrates because of the low-cost and low-temperature process of OLED and a-TFTs [28]. However, the threshold voltage shift of a-TFTs is a critical issue to degrade the image quality of AMOLED panels [28]. Furthermore, OLED is placed on the source node of a-TFT in the conventional pixel circuits (two-TFTs and one capacitor) and OLED current is determined by the voltage difference of the gate and source of the driving TFT. Threshold voltage shifts across OLED raise the source voltage of the driving TFT and the driving current degrades. Therefore, this section will introduce a new source-follower type driving circuit including five n-type TFTs and one capacitor. The function of four TFTs is for switches and the other is for driving TFT. This novel pixel circuit can efficiently eliminate degradation of OLED current.

2.2 Pixel structure and operation

Figure 2-1 presents this proposed circuit which is called source-follower type compensation pixel circuit and its timing scheme. This circuit contains one driving TFT (DTFT), four switching TFT (T1, T2, T3, T4) and one storage capacitor (Cst). There are three timing signals

$(V_{DATA}, [n]scan, [n]EM)$. Among them, V_{DATA} represents a voltage data signal line. V_{DD} and V_{ref} refer to a constant voltage source line and a reference voltage line, individually. According to the timing scheme of the signal line, we have two operation periods : compensation period and display period. Figure 2-2 depicts these two stages. During stage (1), $[n]Scan$ are set at the high level while $[n]EM$ are in the low level. Thus, the switch T1 and T2 are turned on so that V_{DATA} can be charged into the gate node of DTFT, node A, The electro-potential of the left side of Cst, node B, becomes V_{ref} at the same time, shown in figure 2-2 (a). Consequently, this pixel circuit is a source-follower type connection including DTFT and OLED. Assume that voltage across the OLED is V_{OLED} and the threshold voltage of DTFT is V_{th} , respectively. As we can see, the right side of Cst, node C, is going to be charged up to $V_{DATA} - V_{th} - V_{OLED}$ in this circuit. The voltage difference stored in Cst is $V_{ref} - V_{DATA} + V_{th} + V_{OLED}$. Next stage, the display period comes out after the compensation period. During stage (2), $[n]Scan$ are turning to low to turn off the switches T1 and T2. On the contrary, $[n]EM$ are set to high to turn on the switches T3 and T4. Therefore, the right side of Cst is set to ground and the left side of Cst which is connected to the gate of DTFT owing to T3 is boosted to $V_{ref} - V_{data} + V_{th} + V_{OLED}$, immediately. Figure 2-2 (b) shows this analytic result. Stored voltage of Cst is maintained until next frame time. Accordingly, DTFT begins to generate

the current, I_{OLED} , to drive the OLED. Assume that DTFT is operated in the saturation mode :

$$\begin{aligned}
 I_{\text{OLED}} &= K_n [V_{\text{GS}} - V_{\text{th}}]^2 \\
 &= K_n [V_{\text{G}} - V_{\text{S}} - V_{\text{th}}]^2 \\
 &= K_n [(V_{\text{ref}} - V_{\text{DATA}} + V_{\text{OLED}} + V_{\text{th}}) - (V_{\text{OLED}}) - V_{\text{th}}]^2 \dots\dots (2-1) \\
 &= K_n [V_{\text{ref}} - V_{\text{DATA}}]^2
 \end{aligned}$$

According to the equation, I_{OLED} is independent of the threshold voltage of DTFT, V_{th} . It only contains two controllable valuables, V_{ref} and V_{DATA} . As a result, OLED current wouldn't degrade even though threshold voltage shifts tremendously.

2.3 Simulation Results

This pixel circuit simulation has put into practice with a HSPICE simulator. Table 2-1 summarizes the simulation parameters and the control signals. The initial supply voltage modulated such that the I_{OLED} in the following cases was approximately 1 uA as luminance and resolution were designed to be 300 Cd/m² and 133 PPI. Figure 2-3 represents the simulation result of a-TFT :H during threshold voltage shift. We use the software BSIMPRO-plus to fit parameters. This model has a poor transfer characteristics. If our proposed compensation pixel circuits can perform well with this model, we can assure these proposed pixel circuits could fulfill everywhere. Figure 2-4 reveals the simulation result

which shows the three nodes of DTFT : V_{gate} , V_{source} , and V_{drain} .

During the first stage, the compensation period, the right side of Cst would be charged until the DTFT is turned off. At this time, the electric potential at this node attains

$V_{data} - V_{th} - V_{OLED}$. Therefore, the stored voltage in the Cst

is $V_{ref} - V_{data} + V_{th} + V_{OLED}$, as shown in figure 2-3. During the second

stage, the display period, [n]EM turns to be high. The gate node of DTFT is connected to the left side of Cst and the right side of Cst is grounded.

Owing to the charge conservation law, the gate electrical potential of

DTFT becomes $V_{ref} - V_{data} + V_{th} + V_{OLED}$. As a result, this

source-follower type pixel compensates the threshold voltage degradation of the driving TFT and OLED in a frame operation. Furthermore, figure

2-5 represents the simulation results of the output current between this proposed pixel circuit and the conventional two-TFTs and one capacitor

(2T1C) pixel circuit when the threshold shift of DTFT (ΔV_{th}) was set to

2V. According to figure 2-5 (a), the OLED current of the conventional

2T1C structure is fluctuated drastically according to the threshold voltage shift. The degradation range of the conventional pixel circuit is from 1.00

to 0.58uA. The current error rate is calculated to 42%. Assume the

definition of the current error rate is as follows:

$$I_{error} = \frac{I_{initial\ value} - I_{degradation\ value}}{I_{initial\ value}} \times 100\% \dots\dots\dots(2-2)$$

This simulation result apparently confirms that compensating the threshold voltage shift is necessary to guarantee the uniform brightness of OLED pixels and superior gray level expression. According to figure 2-4 (b), it is clear that this novel proposed circuit has compensated the threshold voltage shift. The loss of the OLED current is only 33 nA and the current error rate is merely 3.3%. Therefore, it is verified that the strong immunity to the threshold voltage shift in this proposed pixel circuit is satisfied.

In the normal OLED-TFT display panel, the shift in the voltage across OLED is another concern in spite of the threshold voltage shift of the driving TFT. The threshold voltage of OLED degrades at 0.2mV/h during operation [29]. Figure 2-6 shows the simulated degradation of this proposed pixel circuit and the conventional 2T1C pixel circuit. When the OLED voltage shift is set to 1V, the conventional pixel circuit is degraded from 1 μ A to 0.72 μ A and the current error rate is counted to 28%. So it is inevitable to use a compensation pixel circuit to enhance this drawback. According to figure 2-6 (b), novel pixel circuit drastically improves the quality of OLED panel while the current degradation of proposed pixel circuit is merely 65nA. The current error rate is equal to 6.5%, confirming the effectiveness of the immunity to the degradation voltage across OLED. Table 2-2 (a) and (b) list the simulation result when threshold voltage shifts and OLED degrades respectively. As a result, this source-follower type pixel circuit has an excellent immunity to a-TFT :H and OLED degradation. Figure 2-7 presents the measurement results when a-TFT :H is stressed on 10V and 20V at gate node. According to the stress time and bias voltage, the threshold voltage would degrade as

follows : [14]

$$\Delta V_T(t) = A(V_{ST} - V_{Ti})t^\beta \quad \dots\dots\dots (2-3)$$

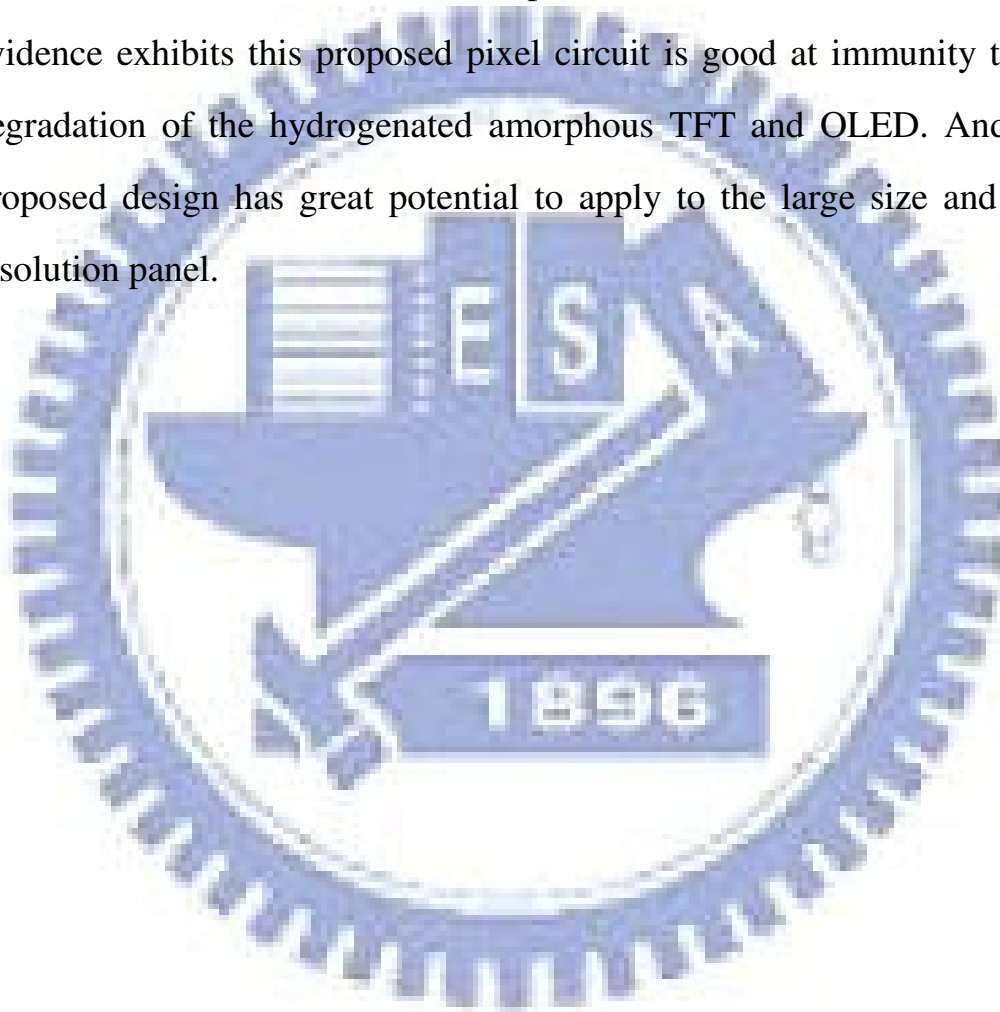
where A and β are the temperature-dependent parameters ; V_{ST} is the gate bias stress voltage ; V_{Ti} is the initial threshold voltage of the TFT, and t is the bias stress time duration. According to this formula, we extract the parameters : $V_{Ti} = 2.53$, $A=0.006$ and $\beta = 0.207$.

Figure 2-8 represents output current of proposed pixel and conventional pixel at different threshold voltage shift. This simulation result shows that OLED current in proposed pixel degrades from 1uA to 0.913uA while OLED current in 2T1C conventional pixel degrades lower than 0.2uA. Furthermore, if we evaluate a real case, OLED degradation and threshold voltage shifts of a-TFT :H both occur. Figure 2-9 depicts the simulation result. Although we operate this source-follower type pixel circuit for 5000 hours, OLED current error is no more than 10%. As a consequence, this novel pixel circuit could take into practice in our daily life.

2.4 Summary

In this chapter, we have developed a novel pixel circuit and its driving scheme for AMOLED with a-TFT :H. It is only composed of five TFTs and one capacitor. We also discuss the simulation results when the threshold voltage shift of the driving TFT and the voltage shift across OLED occur. OLED current degradation is only 3.3% and 6.5% while the threshold voltage shift of driving a-TFT :H and OLED voltage shift is set to 2V and 1V, respectively. And degradation of conventional pixel circuit

is 43% and 28% around when the threshold voltage shift of driving a-TFT :H and OLED voltage shift is set to 2V and 1V, respectively. Therefore, source-follower type compensation pixel circuit is quite better than conventional pixel circuit. Furthermore, current error in this proposed pixel circuit is no more than 10% for 5000 hours operation while current error in conventional pixel circuit is more than 70%. All evidence exhibits this proposed pixel circuit is good at immunity to the degradation of the hydrogenated amorphous TFT and OLED. And this proposed design has great potential to apply to the large size and high resolution panel.



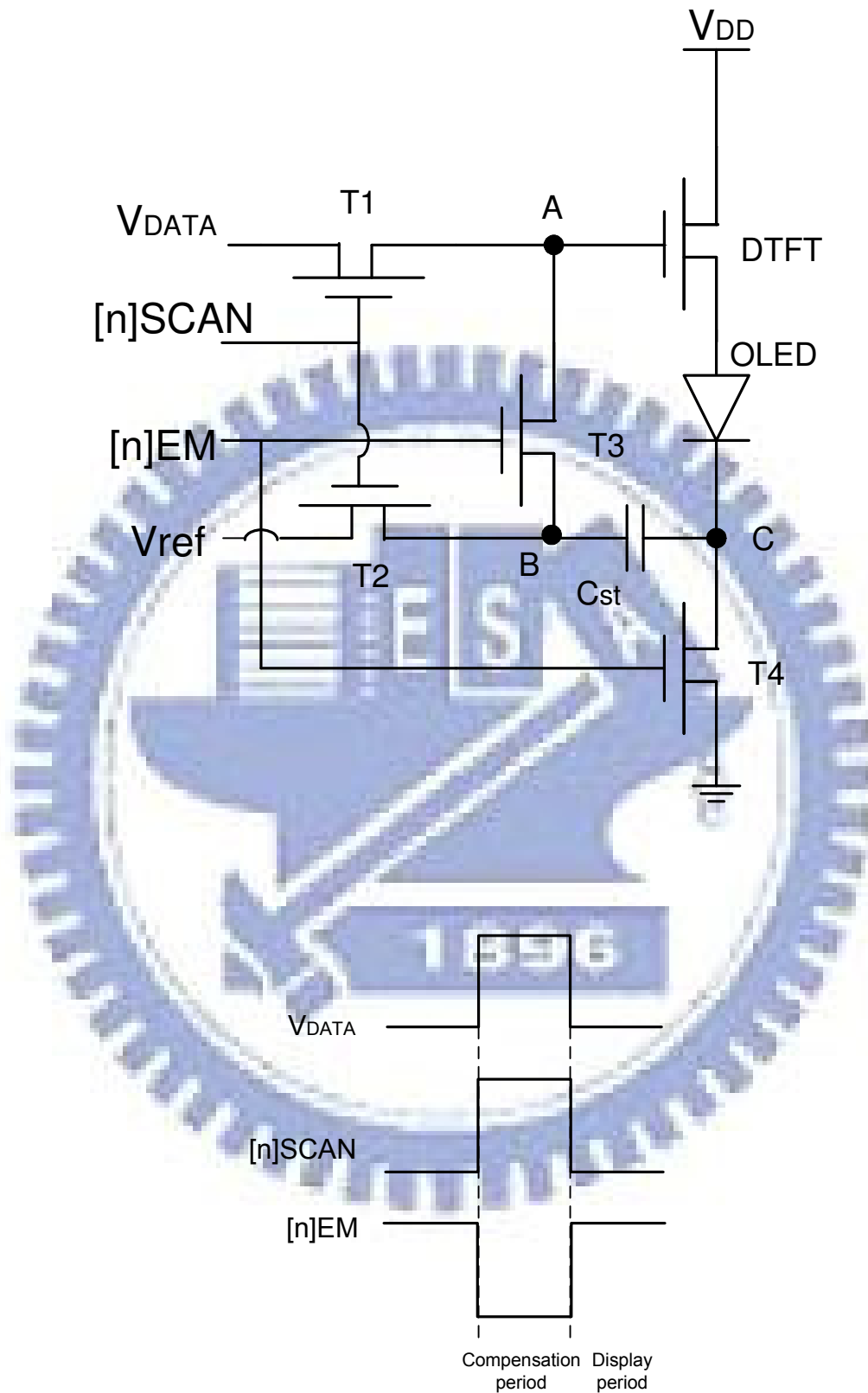


Figure 2-1 the proposed pixel design and timing scheme of the signal line

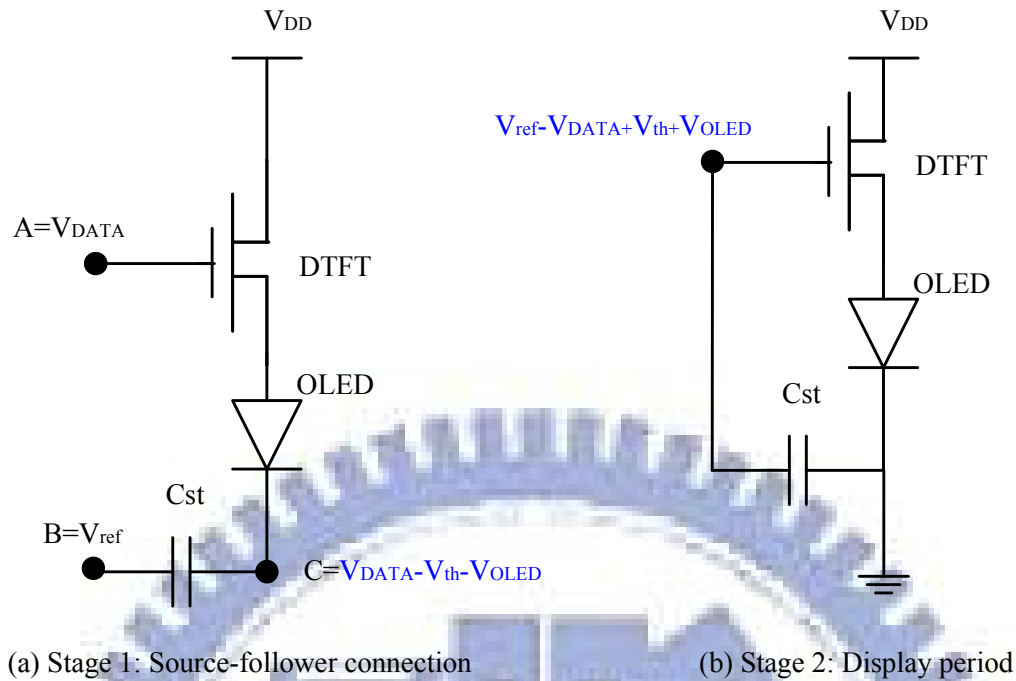


Figure 2-2 stages in operation of proposed pixel circuit (a) compensation period (b) display period

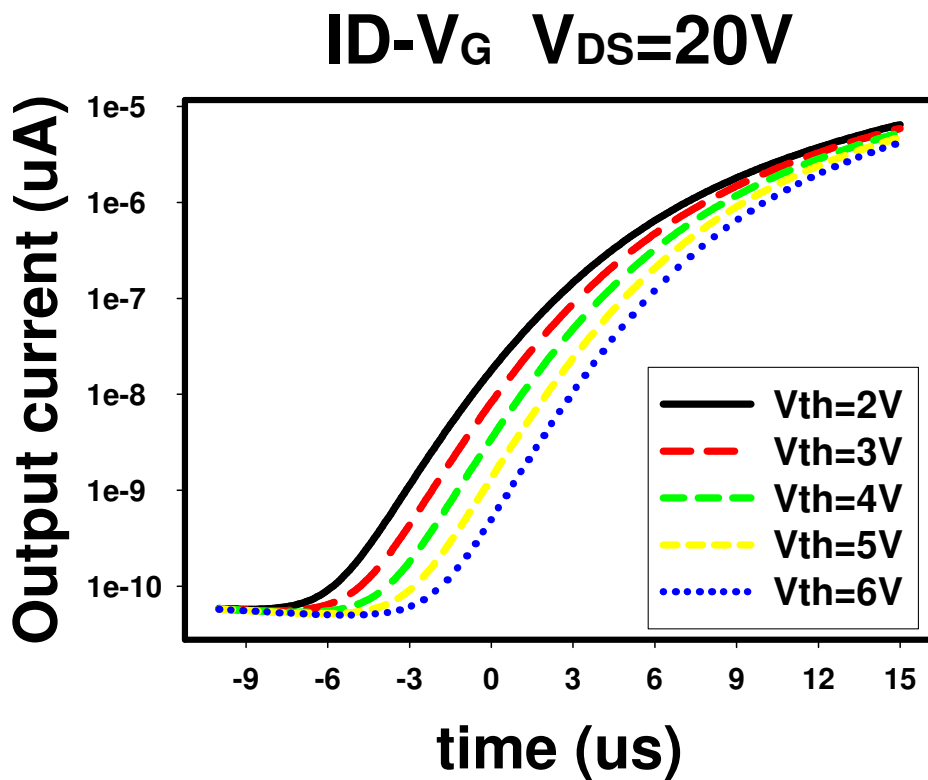


Figure 2-3. simulation result of a-TFT :H during threshold voltage shift

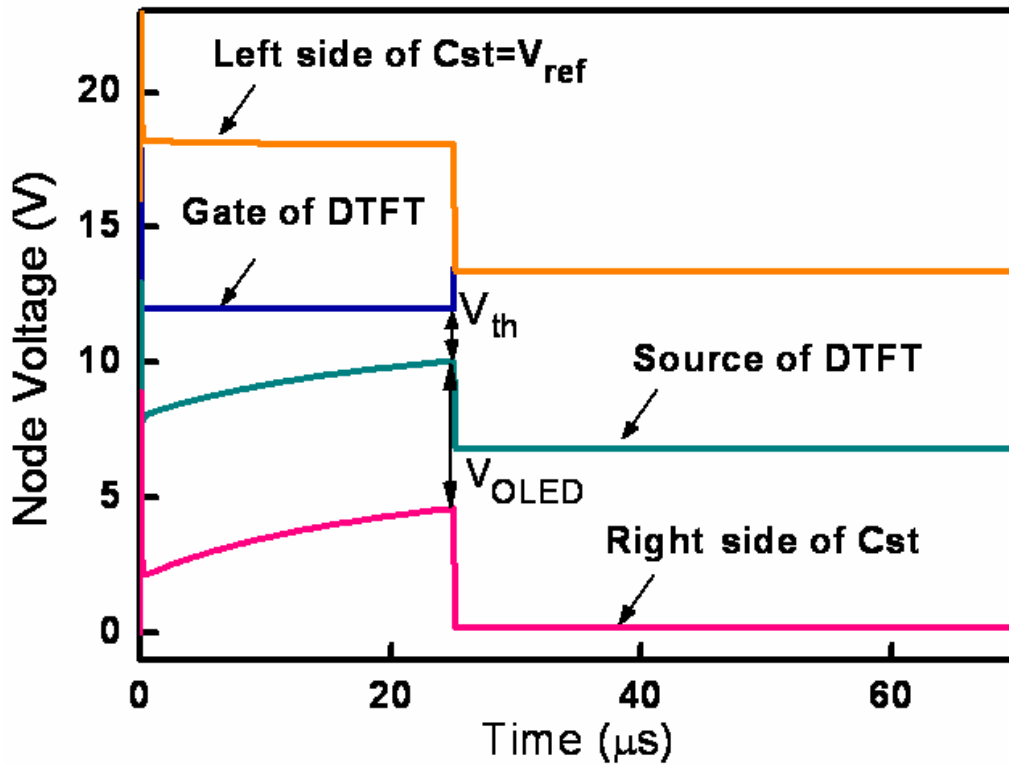


Fig. 2-4 The transient simulation results for the source-follower type structure

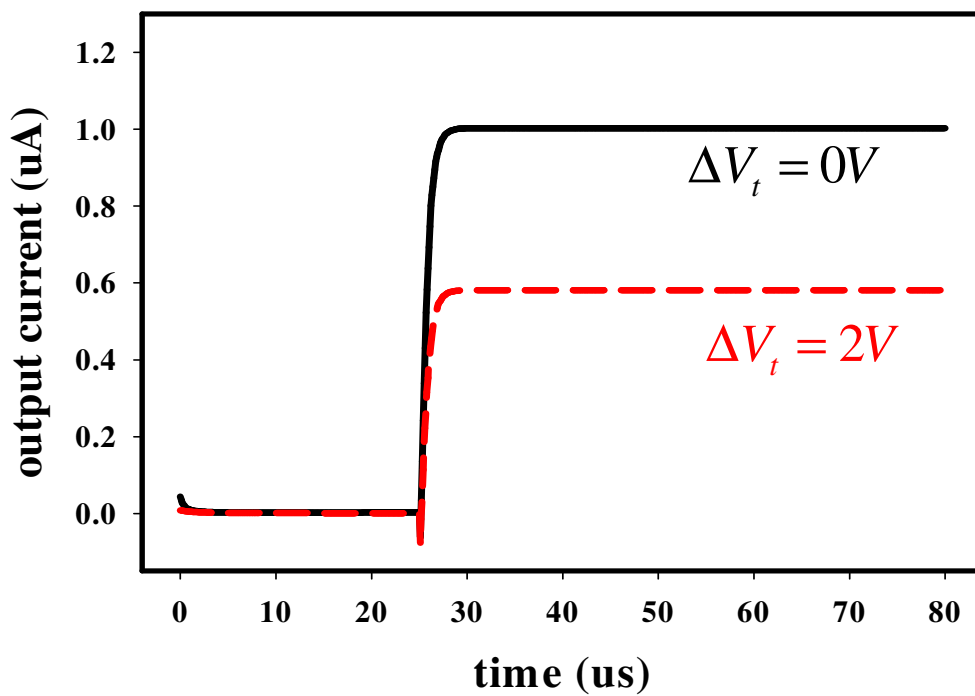


Figure 2-5 (a)Simulation result of the conventional 2T1C pixel circuit. The degradation range of I_{OLED} in 2T1C pixel is from 1.00 to 0.58uA.

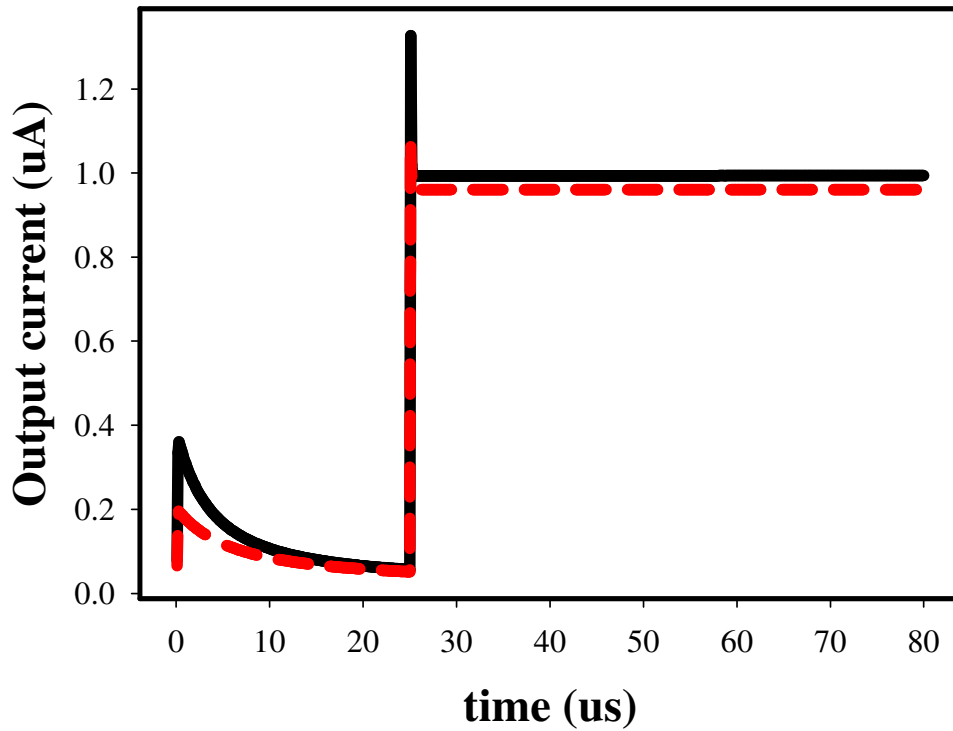


Figure 2-5 (b) Simulation result of the source-follower type compensation pixel circuit as the threshold voltage shift is set to 2.0V.

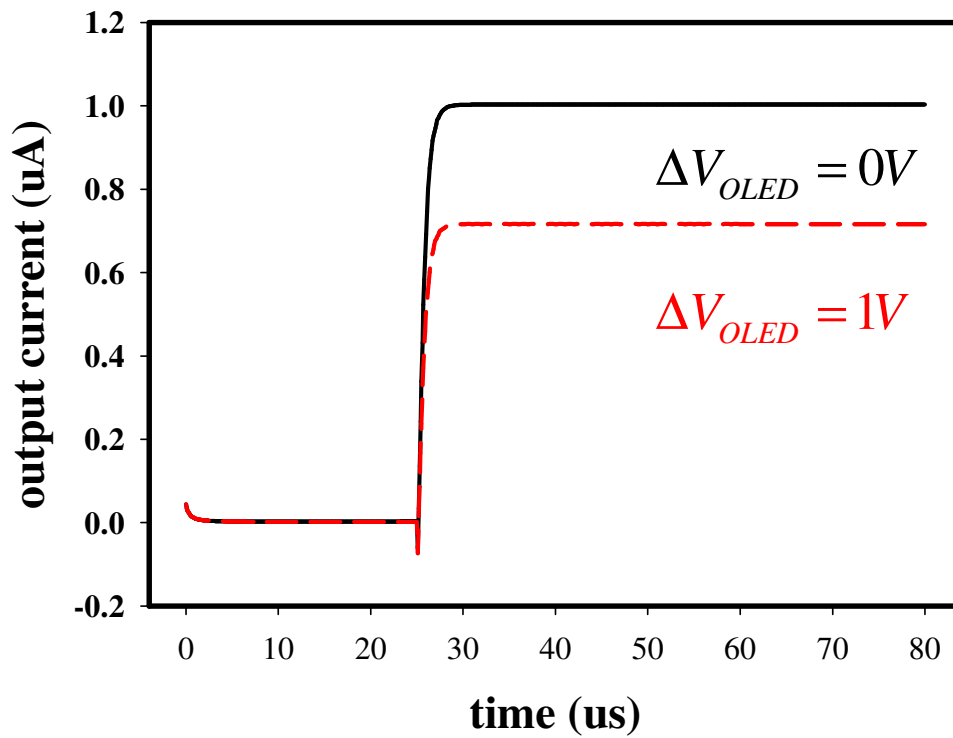


Figure 2-6. (a) Simulation result of the conventional 2T1C pixel circuit.

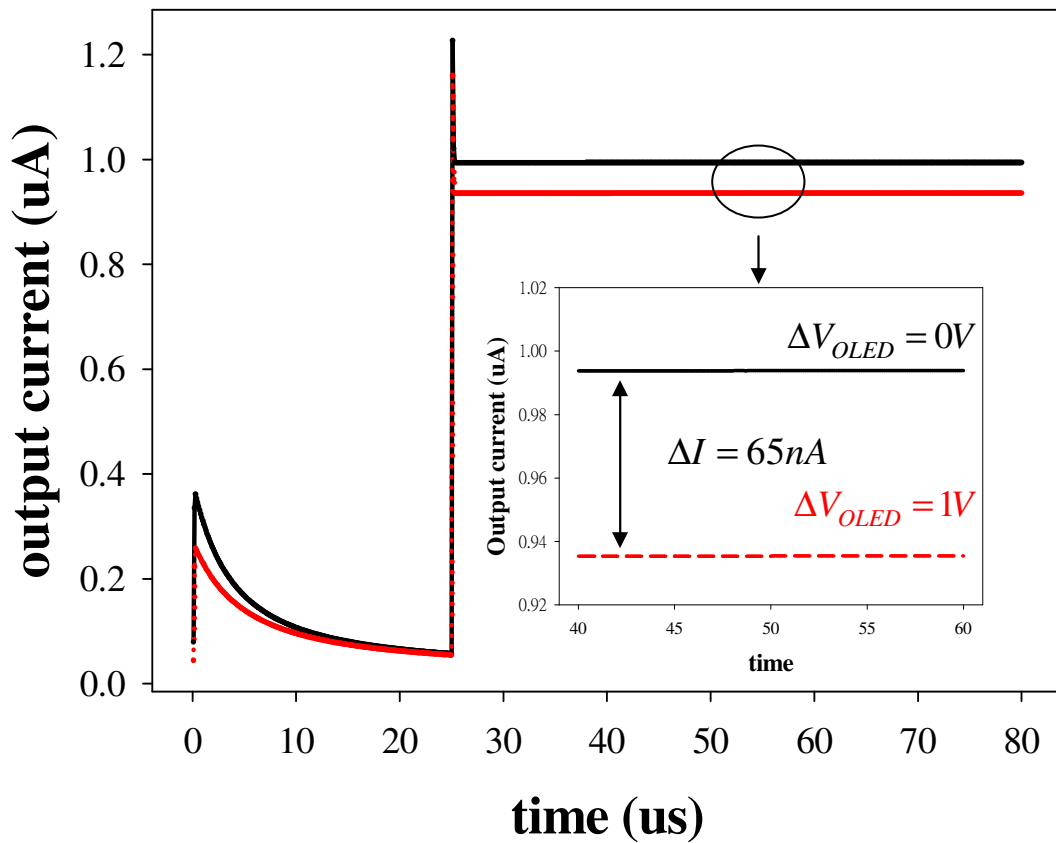


Figure 2-6 (b) Simulation result of the source-follower type pixel circuit as the threshold voltage in OLED is set to 1.0V.

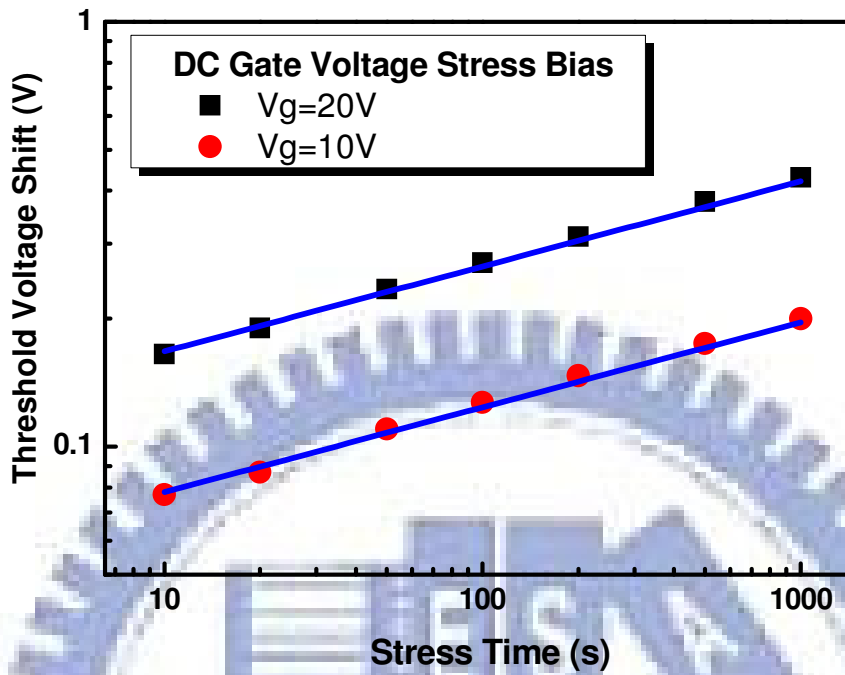


Figure 2-7. Measurement results when a-TFT :H is stressed on 10V and 20V at gate node.

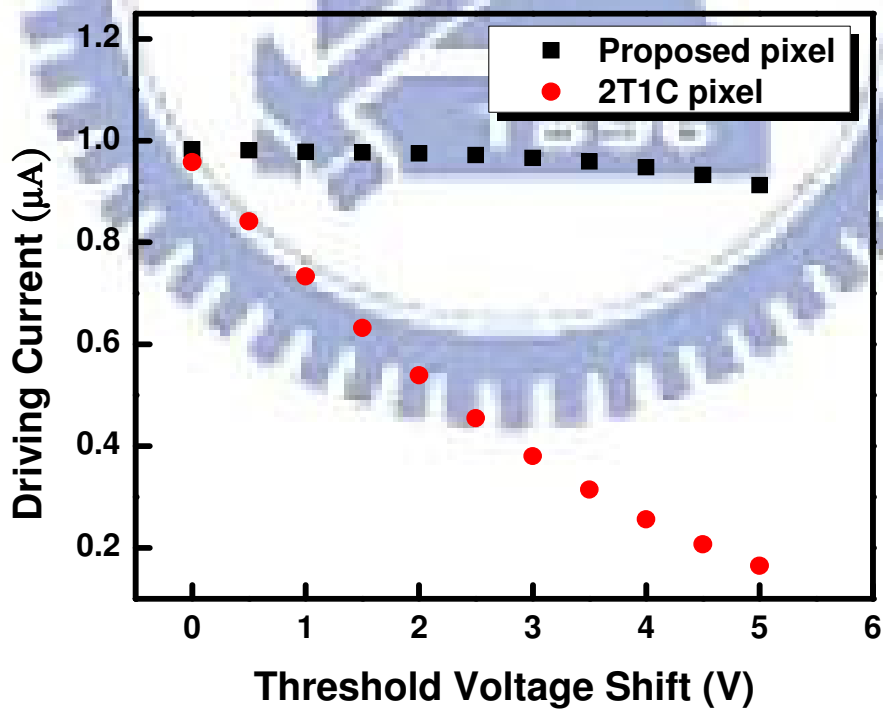


Figure 2-8 output current of proposed pixel and conventional pixel at different threshold voltage shift.

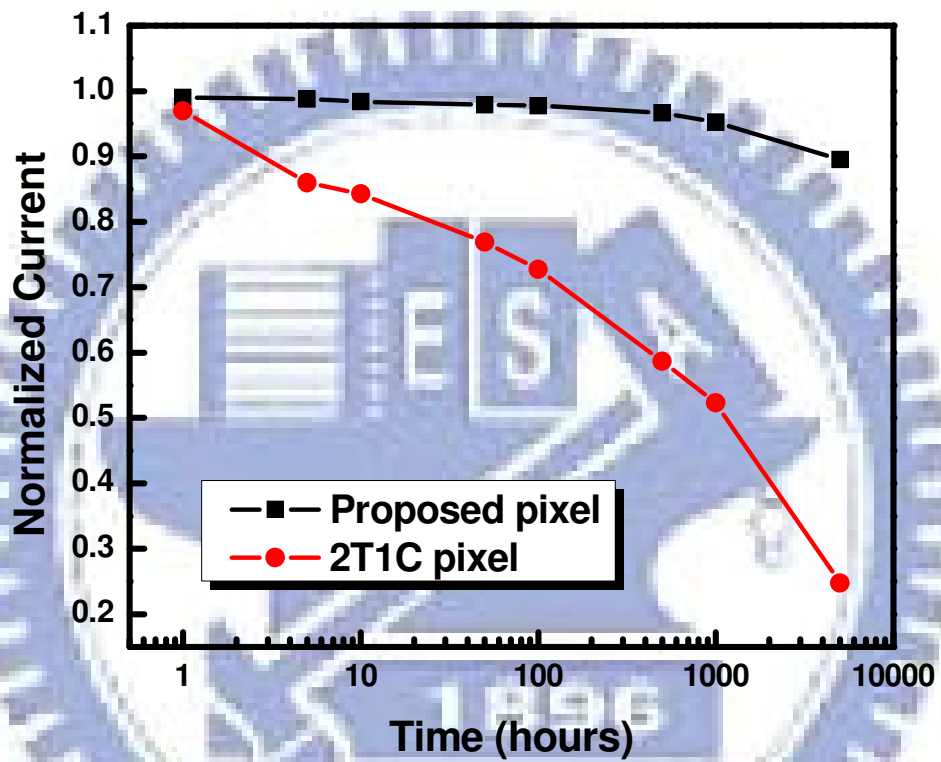


Figure 2-9 stress time versus output current of proposed pixel and conventional pixel

a-Si:H TFT					
V _{th}	W/L (MDTFT)	W/L (T1)	W/L (T2)	W/L (T3)	W/L (T4)
2V	80/4 um	60/4 um	60/4 um	60/4 um	60/4 um
		Control signal line			
C _{st}	W/L (MOLED)	VDD	[n]SCAN	[n]EM	V _{ref}
0.5 pF	150/7 um	15V	30V	30V	18V

Table 2-1. The simulation parameters and the control signals

	OLED current (uA)	current error
I (V _t =2)	1	0%
I (V _t =2.5)	0.89	11.44%
I (V _t =3)	0.78	22.32%
I (V _t =3.5)	0.68	32.55%
I (V _t =4)	0.58	42.04%
I (V _t =4.5)	0.49	50.74%
I (V _t =5)	0.42	58.59%
I (V _t =5.5)	0.35	65.58%
I (V _t =6)	0.28	71.72%

Table 2-2 (a) simulation result when threshold voltage of a-TFT:H degrades

	OLED current (uA)	current error
I (Vt=2 OLED=0)	1	0%
I (Vt=2 OLED=0.2)	0.94	6.26%
I (Vt=2 OLED=0.4)	0.88	12.25%
I (Vt=2 OLED=0.6)	0.82	17.96%
I (Vt=2 OLED=0.8)	0.77	23.40%
I (Vt=2 OLED=1.0)	0.72	28.58%

Table 2-2 (b) simulation result when OLED voltage degrades



Chapter 3

non-leakage type compensation pixel circuit

3.1 Introduction

In the previous chapter, we have introduced a source-follower type pixel circuit. This source-follower type has elevated the drawbacks that the conventional pixel circuit can't fix out. However, there is still some phenomenon that many engineers and scientists concern, especially for large size and high resolution panels. As mentioned above, voltage-programmed pixel circuits (VPPCs) need less addressing time than current-programmed pixel circuits (CPPCs). It assures that choosing VPPCs is the best choice for large size and high resolution panels. Numerous voltage-programmed compensation pixel circuits have been extensively developed. In general, most proposed VPPCs so far have four major cycles : the compensation voltage generation stage (V_{comp}), threshold voltage generation stage, current regulation stage and driving stage [19] [30] [31]. Figure 3-1 exhibits the equivalent models of a general VPPC in every kind of operation [10]. According to figure 3-1 (a), the first stage, the compensation voltage is charged to the gate of the driving TFT (DTFT). The storage capacitor (C_s) is set to hold the gate voltage of DTFT. Then, the drain and gate nodes of DTFT are connected to each other in the second stage. DTFT does not turn off until node A is discharged equal to the threshold voltage of DTFT, as shown in fig 3.1 (b). Electro-potential at node A is stored by C_s . As a result, the threshold

voltage of DTFT is generated during V_T -generation stage. In the figure 3.1 (c), the other side of Cs is connected to high voltage, V_{PG} , to boost node A . At this time, the electro-potential of gate node becomes $V_{PG} + V_T$. Finally, the source of DTFT is connected to OLED in order to radiate in figure 3-1 (d). Therefore, the OLED current is independent of the threshold voltage of DTFT according to the saturation current formula. These kinds of compensation circuits seem perfect. However, there is a critical issue in one of these steps. That is the V_T -generation step. It is an essential issue to determine the threshold voltage generation time, τ . If τ is set too long, the electro-potential is going to be lower than the threshold voltage of DTFT due to the leakage current. On the contrary, If τ is set to be too short, the electro-potential is going to be higher than the threshold voltage of DTFT [32]. Besides, τ is set to be fixed all the time in the pixel operation but the real time of the threshold voltage generation varies all the time. Generation time is dependent of the threshold voltage shift. As a consequence, I am going to introduce another novel compensation pixel circuit, called non-leakage type compensation pixel circuit for AMOLED panels in this chapter. This newest compensation circuit can eliminate this issue by avoiding using V_T -generation cycle. So it doesn't matter how fluctuant τ is. This circuit composes of one capacitor and five a-TFTs :H including one driving TFT and five switching TFTs. This pixel circuit really has an fabulous immunity to the threshold voltage shift of the driving TFT and OLED.

3.2 Novel compensation pixel circuit

3.2.1 pixel structure and operation

Figure 3-2 shows this non-leakage type compensation pixel circuit and its time scheme. In this pixel circuit, we have two operation periods. First of all is compensation period. During this period, the control signal V_{S1} is going high so that the TFT M3 and M5 is going to be turned on. The gate node of M_{DTFT} , node A, is charged up to V_{DD} . At the same time, the gate voltage of the TFT M2 becomes V_{DATA} , as shown in figure 3-3 (a). The voltage of node B is determined by the two TFTs, M_{DTFT} and M_2 when these two TFTs are in operation. Assume these two TFTs are in saturation mode and node B is defined to the output voltage, V_{out} . According to the current through M_{DTFT} equal to through M_2 , we have formula expression as follows :

$$I_1 = I_2$$

$$\Rightarrow K1(V_{GS1} - V_{TH1})^2 = K2(V_{GS2} - V_{TH2})^2$$

$$\Rightarrow (V_{dd} - V_{out} - V_{TH1})^2 = \frac{K2}{K1} (V_{data} - V_{TH2})^2$$

$$\Rightarrow (V_{dd} - V_{out} - V_{TH1}) = \sqrt{\frac{K2}{K1}} (V_{data} - V_{TH2})$$

$$\Rightarrow V_{out} = V_{dd} - \sqrt{\frac{K2}{K1}} V_{data} + V_{TH1} + \sqrt{\frac{K2}{K1}} V_{TH2} \quad \dots\dots\dots(3-1)$$

, where V_{TH1} is the threshold voltage of M_{DTFT} and V_{TH2} is the threshold voltage of M_2 . Therefore, V_{out} can be settled by two variable parameters K1 and K2. These parameters include mobility, width length ratio, and effective capacitor of gate oxide. The capacitor stores the voltage difference, ΔV , between the node A and B at this time :

$$\begin{aligned} \Delta V &= V_A - V_B = V_{DD} - V_{out} \\ &= \sqrt{\frac{K2}{K1}}V_{data} + V_{TH1} - \sqrt{\frac{K2}{K1}}V_{TH2} \dots\dots\dots (3-2) \end{aligned}$$

Figure 3.3(b) depicts the second stage, display period. The control signal V_{S1} is going low. TFT M3 and M5 are turned off. Data voltage can't charge the gate voltage of M2 so that M2 is also turned off. At the same time, the control signal is going high to turn on M4. The electrical potential at node B is pulled to electro-potential at the anode of OLED, V_{OLED} . Because the node A is floating right now, the electro-potential at node A will be boosted by node B. However, voltage difference across the capacitor, C_{st} , is unchanged. Hence, the current across M_{DTFT} is as follows :

$$\begin{aligned} I &= K1(V_{GS} - V_{TH1})^2 = K1(V_G - V_S - V_{TH1})^2 \\ &= K1(\Delta V + V_{OLED} - V_{OLED} - V_{TH1})^2 \end{aligned}$$

$$\begin{aligned}
&=K1\left(\sqrt{\frac{K2}{K1}}V_{data}+V_{TH1}-V_{TH1}-\sqrt{\frac{K2}{K1}}V_{TH2}\right)^2 \\
&=K1\left(\sqrt{\frac{K2}{K1}}V_{data}-\sqrt{\frac{K2}{K1}}V_{TH2}\right)^2 \dots\dots\dots (3-3)
\end{aligned}$$

As a result, OLED current is independent of V_{TH1} . It is merely related to V_{TH2} . Nevertheless, the TFT M_2 is not the dominant driving element in this circuit. The compensation time is quite less than the driving stage. So the degradation of M_2 occurs very slightly. According to the formula (3-3), it wouldn't be an obstacle that V_{TH1} shift occurs constantly.

Furthermore, operation time on TFT M_4 is as long as M_{DTFT} . The degradation on M_4 is as severe as M_{DTFT} , even worse due to higher stress voltage. However, it wouldn't influence our driving current. Although the electro-potential on node B becomes higher due to higher resistance, the electro-potential at node A also becomes higher because the voltage difference stored in C_s wouldn't change. In other words, the voltage difference between gate and source of DTFT is unchanged. Hence, It wouldn't impact OLED driving current.

3.2.2 Simulation results and discussions

Simulation of this compensation pixel circuit has carried out with a HSPICE simulator. Table 3-1 summarizes the simulation parameters and the control signals. Figure 3-4 presents the simulation

result of the three nodes of M_{DTFT} : V_{gate} , V_{source} and V_{drain} . And figure 3-5 shows the time scheme of every signal. During the first stage, the compensation period, the up side of C_{st} , node A, would be charged up to the electro-potential V_{DD} . The control signal V_{s1} is going high so that TFT M3 and M5 are going to be turned on. Node A is charged up to V_{DD} . Node B, the source node of M_{DTFT} becomes the output voltage, V_{out} , which is determined by M_{DTFT} and M_2 . As we can see, the voltage difference, ΔV , stored by C_{st} isn't changed during the transition of these two periods. Hence, the gate voltage of M_{DTFT} holds to turn on M_{DTFT} in the display period. Figure 3-6 shows simulation results of this pixel circuit. Though the threshold voltage shift is 2V, the current degradation is only 32nA. According to the formula [2-2], the current error is counted to be 3.76%. Table 3-2 makes a whole collection of this model's performance. Even the threshold voltage shift degrades to 4V. The current error is only 7% around. During display period, TFT M2 is regarded to be turned off. Nevertheless, a-Si:H model depicts that sub-threshold swing is too large to turn off TFT, as shown in figure 2-1. When the data voltage is set to 2.5V, the leakage current through M2 is compatible to the driving current through OLED. The parasitic effect plays more important role so that the current error goes up to about 15%. However, this non-leakage type compensation pixel circuit has an quite better immunity to threshold voltage shift than the conventional pixel circuit. Furthermore, the anode potential of OLED is connected to one side of C_s during display period. Hence, the gate node of DTFT is boosted. The voltage difference across

C_s is fixed. OLED current wouldn't degrade when OLED degrades during stress. Figure 3.7 shows the simulation result when threshold voltage of OLED degrades 1V. The current merely degrades from 1.105A to 1.091A. The current error is only 1.27%. Therefore, it verifies that this circuit is well behaved as compensation circuit.

3.3 Goh's model

3.3.1 Pixel structure and timing scheme

In section 3.1, we have mentioned the basic operation of normal voltage-programmed pixel circuits (VPPCs). We are going to introduce a typical example of VPPCs in this section. Figure 3-8 represents this kind of model presented by Goh [4]. It composed of four TFTs (three switching TFTs and one driving TFT) and one capacitor (C_{st}). There are three operation cycles. They are voltage compensation stage, V_T -generation stage and driving stage. During the first stage, the timing signal SLT goes high from low to turn on Sw1 and Sw2. CTD goes high to prevent currents from flowing to the OLED while TNO stays high, sustaining Sw3 in the "on" state. When an input data V_{data} is applied to DT, node B becomes V_{data} as shown in figure 3-9 (a). Figure 3-9 (b) shows the second stage. TNO goes to low to turn off Sw3, while SLT and CTD maintain high. The gate voltage of DTFT, node A, is discharged through SW1 and SW2 until Sw2 is turned off. At this time, the electro-potential of node A settles to $V_{data} + V_{TH}$ where V_{TH} is the threshold

voltage of DTFT. The storage capacitor, C_{st} , stores the voltage difference and it maintains the electro-potential of node A during a frame time. Figure 3-9 (c) represents the final stage. TNO goes high to turn on Sw3, while SLT goes to low to turn off Sw1 and Sw2. CTD goes to low to let current flow through OLED. Then, DTFT begins to drive DTFT during a frame time. Because CTD is set to negative value, the anode potential of OLED wouldn't be too high. Although the anode of OLED is connected to the source node of DTFT, the voltage difference between gate and source node of DTFT which is equal to $V_{data} - V_{OLED}$ is going to be influenced by V_{OLED} . As expected, OLED current has a high immunity to threshold voltage shift but OLED current is going to degrade with OLED degradation.

3.3.2 Simulation result and discussions

Table 3-3 summarizes the simulation parameters and the control signals. We use HSPICE as our simulation tool. Figure 3-10 shows the simulation result of Goh's model. As our expectation, the gate potential of DTFT is charged in the first stage. During the second stage, threshold voltage generation, the source node of DTFT is equal to V_{data} . The gate voltage of DTFT is discharged until DTFT is turned off. The voltage difference between gate and source of DTFT becomes V_{th} . And this discharging time is defined as τ before. During display stage, the gate electro-potential is almost maintained. Figure 3-11 shows the OLED current of Goh's model as the threshold voltage shifts from 2V to 4V.

OLED current degrades from 1.1068A to 0.9839A. The current error is counted to 11.1%. Performance of Goh's model is much better than the conventional pixel circuit. Table 3-4 makes a whole collection of Goh's pixel circuit performance when the threshold voltage shift varies 4V. Furthermore, if the operation time goes on, OLED is going to start to degrade. Figure 3-12 shows the simulation result of OLED current as the threshold voltage of OLED shifts 1V. The current degrades from 1.1074A to 0.7896A. The current error is about 28% as high as the conventional pixel circuit. As a consequence, this pixel only has a immunity on threshold voltage shift of the driving TFT.

3.3.3 Threshold voltage-generation issue in these models

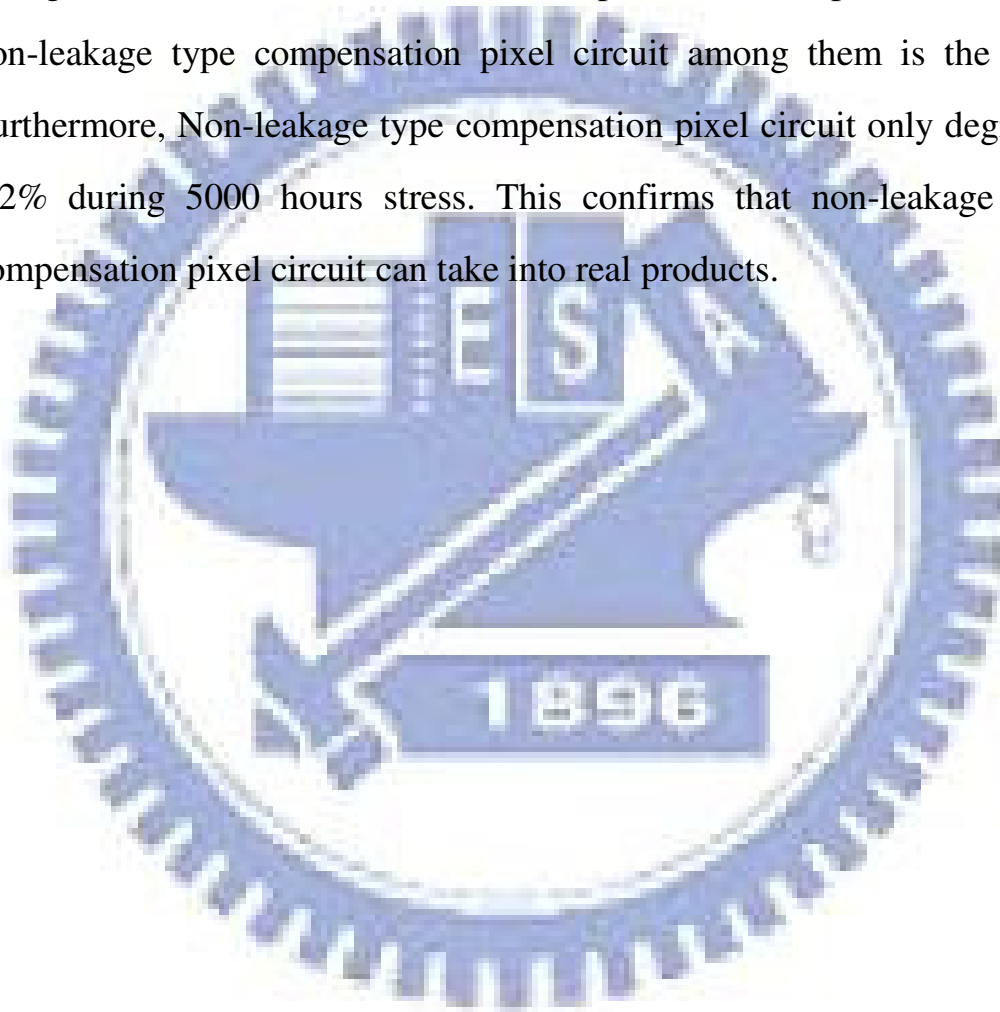
In section 3.1, we have discussed that there is a critical issue about τ . Let us see why τ so important to typical compensation pixel circuit is. Figure 3-13 shows the transient result of gate and source nodes of DTFT as the threshold voltage shifts 4V. At the beginning, τ is set to fit our requirement that the voltage difference between gate and source nodes of DTFT is 2V. However, the threshold voltage continually degrades after long time operation. The leakage current which causes the threshold voltage generation becomes lower and lower due to increasing threshold voltage. On the contrary, it doesn't need as much time as before to attain higher threshold voltage value when the threshold voltage increases. It depends on factors which dominate. As a consequence, current error of Goh's model must be larger than non-leakage type

compensation circuit. Figure 3-14 and 3-15 shows the current error comparison between non-leakage type model and Goh's model when threshold voltage shifts 2V and 4V, individually. Obviously, non-leakage type model is really better than Goh's model, typical threshold voltage generation type model. Figure 3-16 represents the current error comparison between non-leakage type model, Goh's model and conventional model at each threshold voltage. Goh's model and non-leakage type model are both quite better than conventional pixel circuit. And it assures that non-leakage type model is the best model among them. Figure 3-17 shows driving current comparison between non-leakage type model and Goh's model at stress operation. During 5000 hours stress, non-leakage type compensation pixel circuit merely degrades 6.2% while Goh's compensation pixel circuit degrades 17.8%. Although Goh's model is quite better than conventional pixel circuit, non-leakage type pixel circuit is the best among them. Because non-leakage type compensation pixel circuit doesn't have V_t -generation cycle, it eliminates uncontrollable factors.

3.4 Summary

We have introduced a novel non-leakage type compensation circuit. It not only has an excellent immunity to the threshold voltage shift of a-TFTs V_t and characteristics of OLED but also has no threshold voltage generation period. The threshold voltage generation time, τ , is an unstable factor. The less uncontrollable factors compensation pixel circuits have, the more accuracy current error is. Non-leakage type

compensation pixel circuit degrades about 7% and 1.27% when threshold voltage of the driving a-TFT:H shifts 4V and OLED voltage degrades 1V, respectively. The typical voltage-programmed compensation pixel circuit, Goh's model, degrades about 15% when the threshold voltage of driving TFT shifts 4V. Although Goh's model has better immunity to threshold voltage shifts than the conventional pixel circuit, performance of non-leakage type compensation pixel circuit among them is the best. Furthermore, Non-leakage type compensation pixel circuit only degrades 6.2% during 5000 hours stress. This confirms that non-leakage type compensation pixel circuit can take into real products.



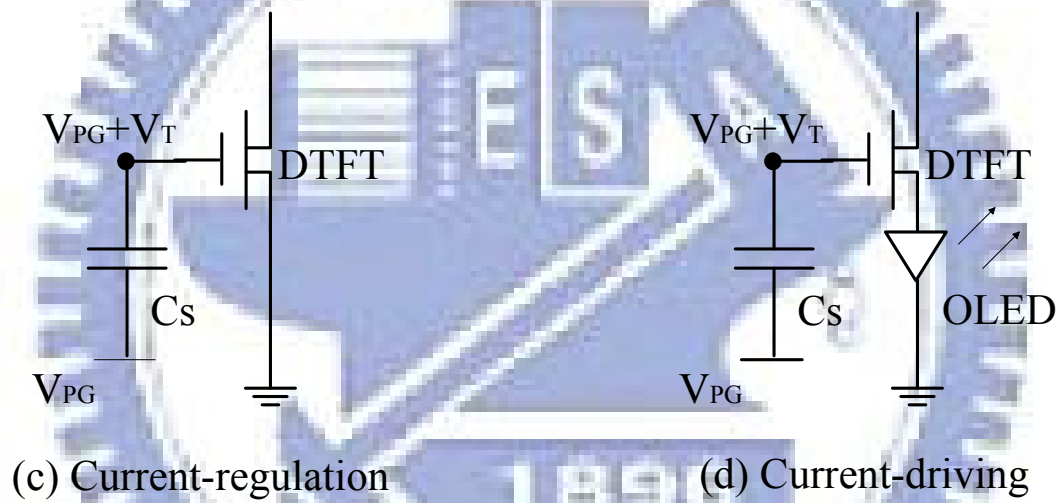
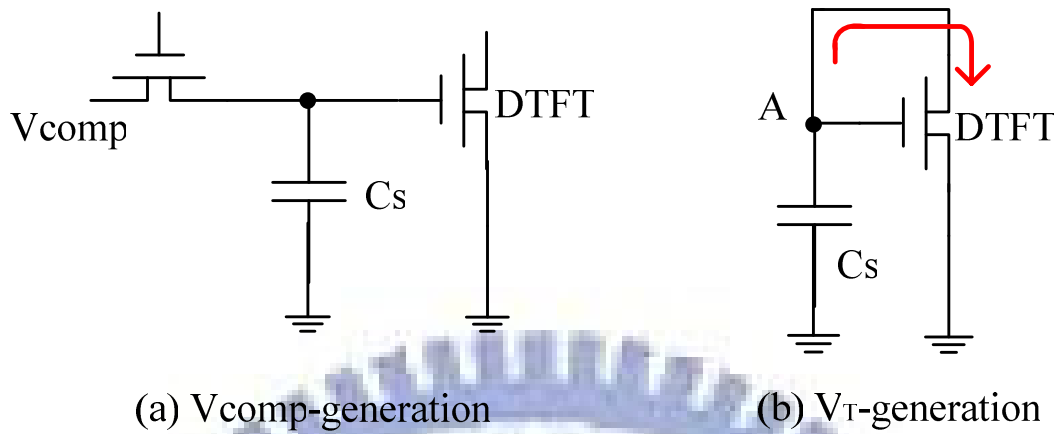


Fig 3-1 Equivalent models for a typical VPPC during different operating
 (a) V_{comp} -generation (b) V_T -generation (c) Current-regulation
 (d) Current-driving

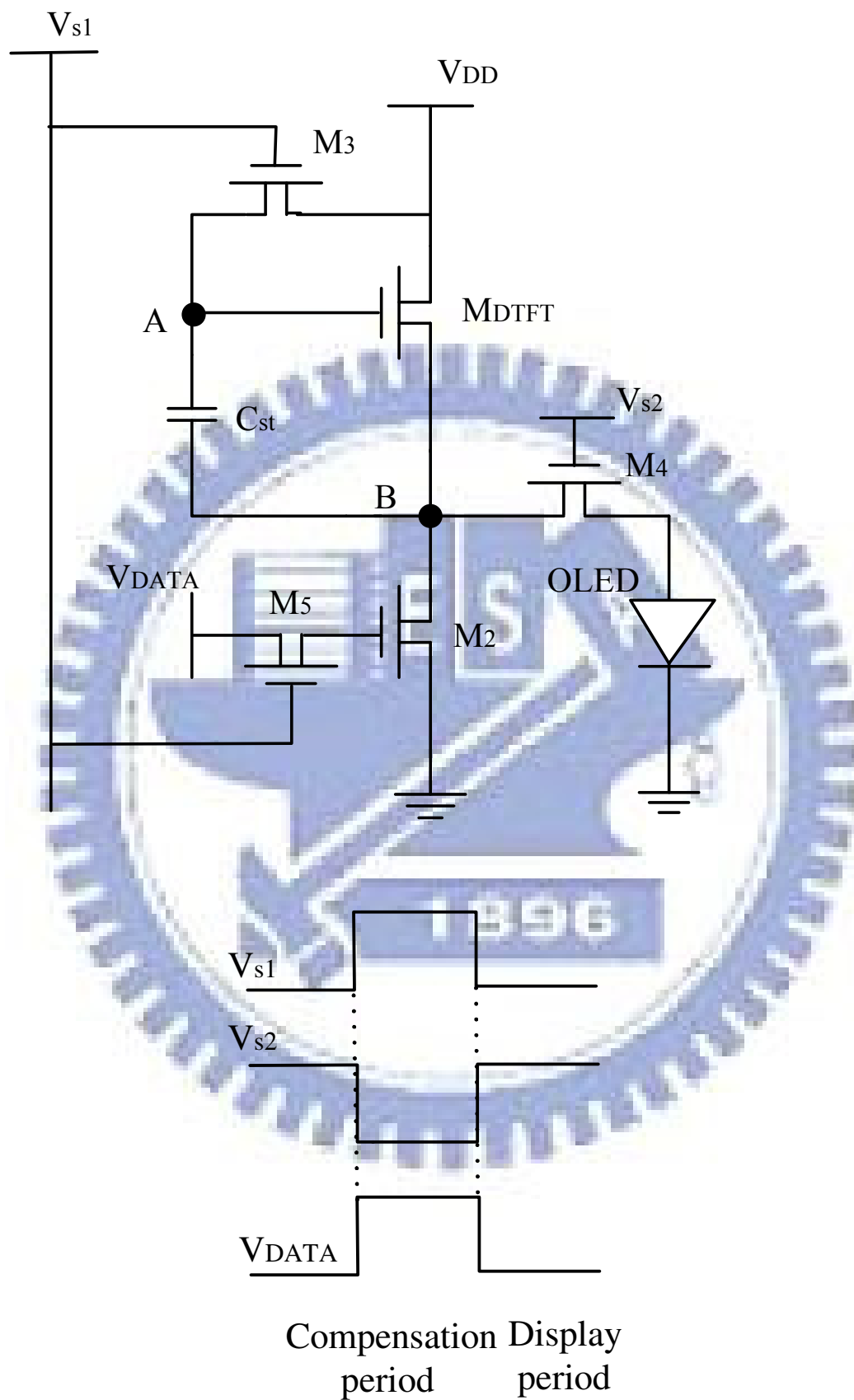


Figure 3-2 non-leakage type compensation pixel circuit and its time scheme

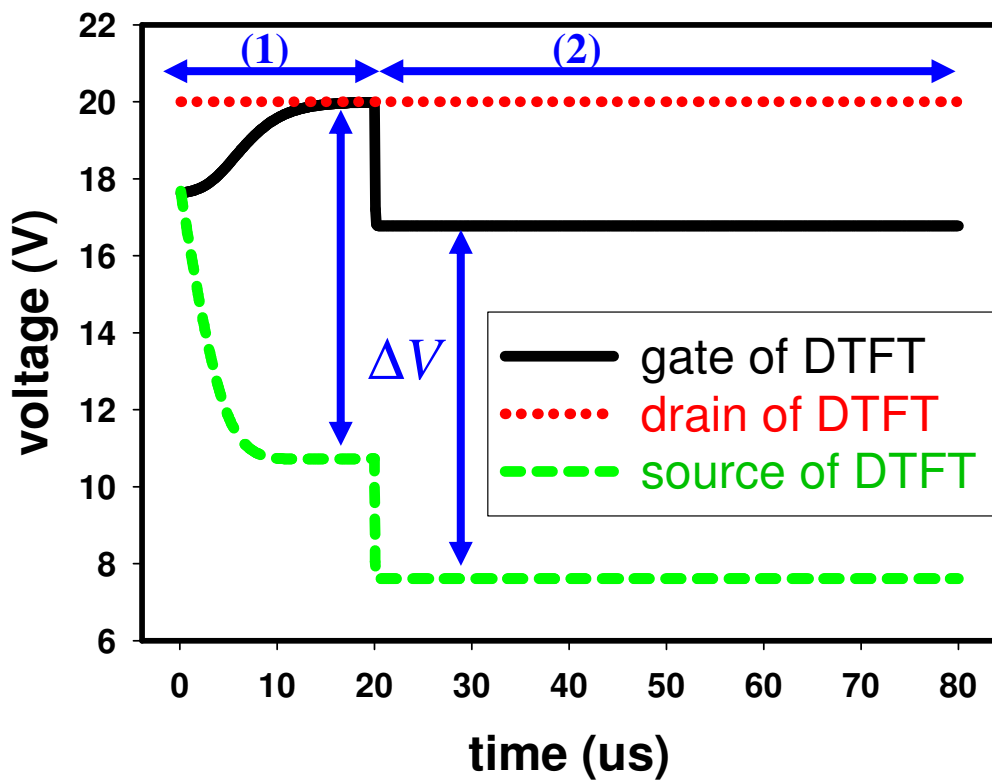
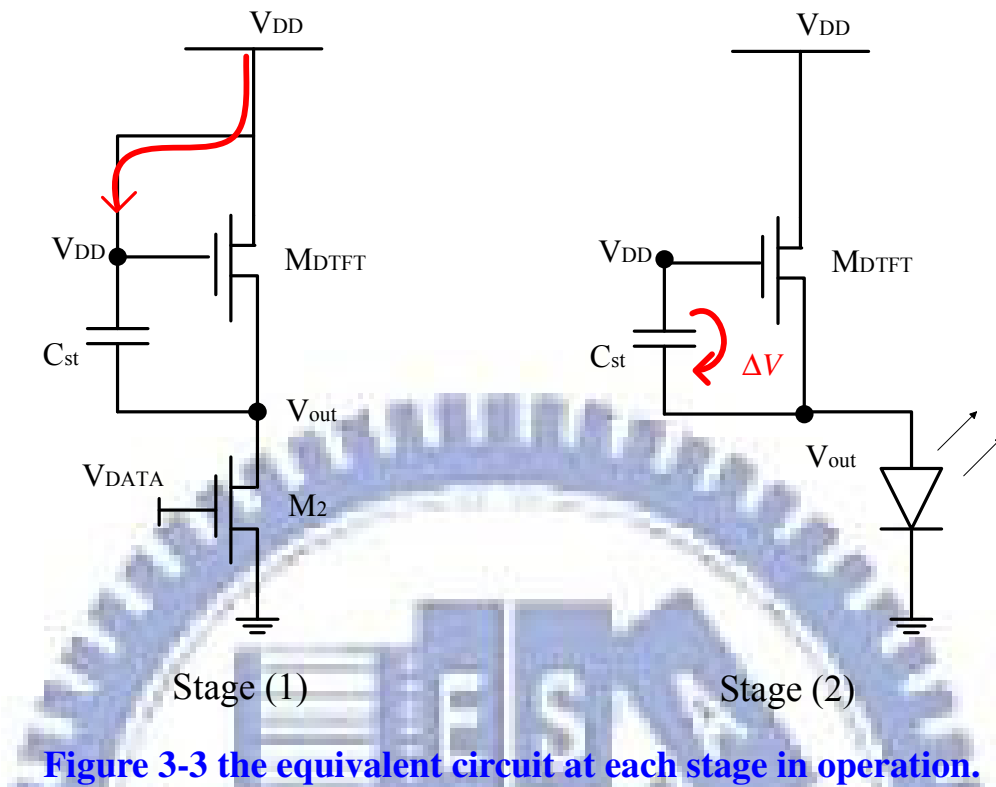


Figure 3-4 simulation result which shows the three nodes of DTFT :

V_{gate} , V_{source} , and V_{drain}

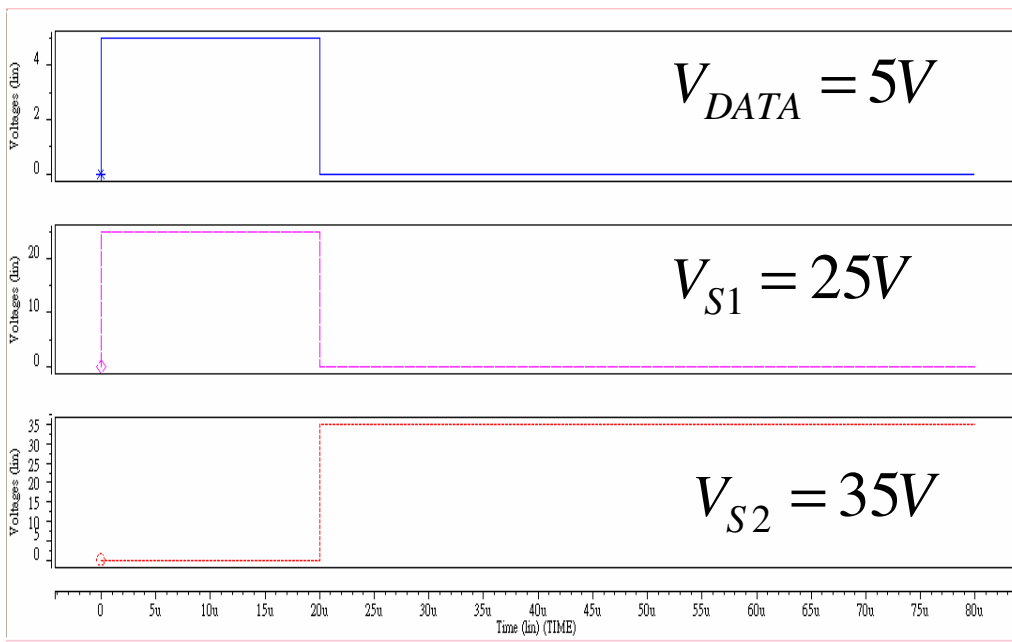


Figure 3-5 simulation result of the signal time scheme

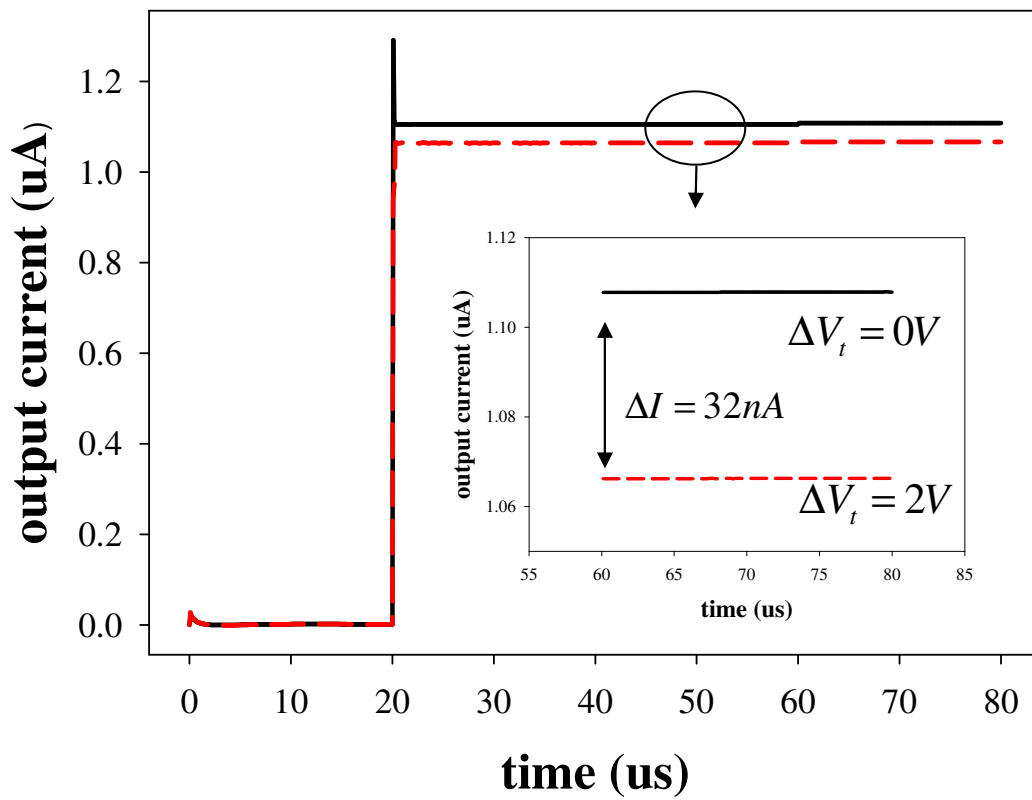


Figure 3-6 Simulation result of this proposed pixel circuit as the threshold voltage shift is set to 2.0V.

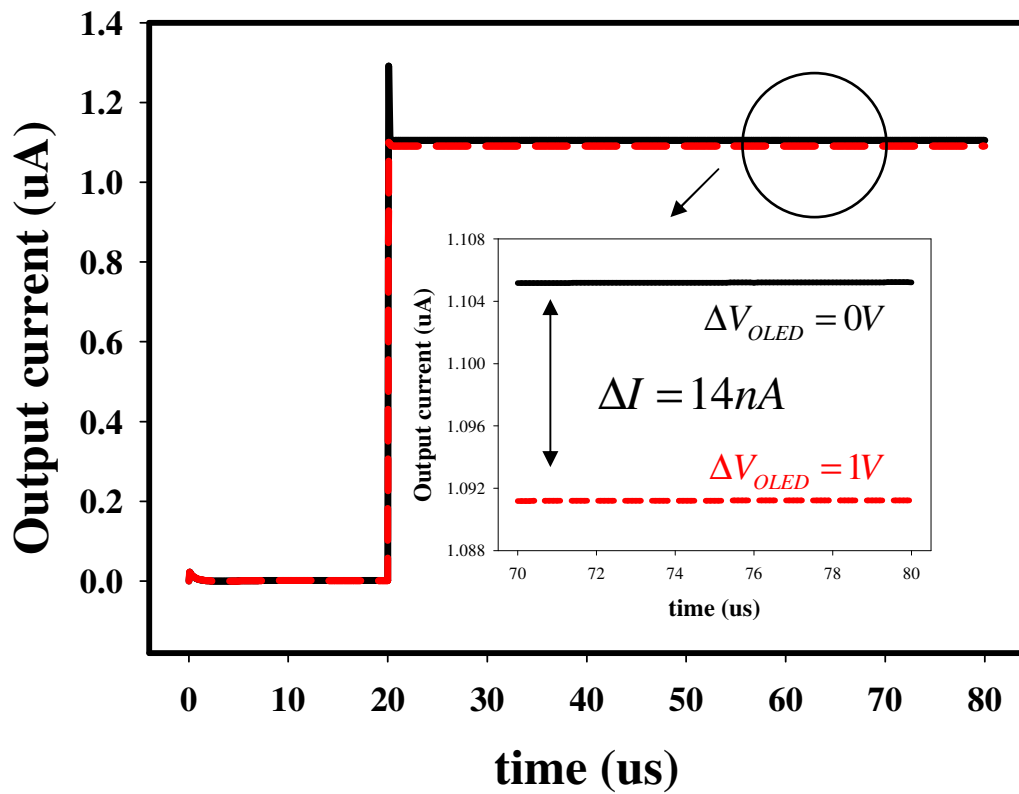


Figure 3-7 Simulation result of this proposed pixel circuit as OLED voltage shift is set to 1.0V.

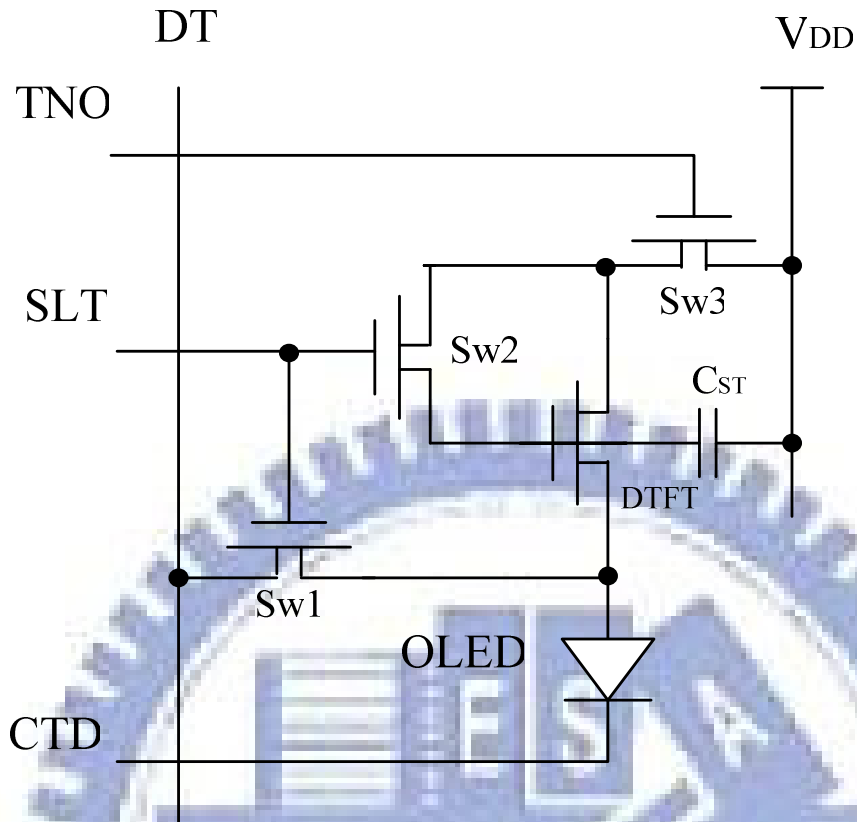


Figure 3-8(a) Goh's proposed compensation pixel circuit

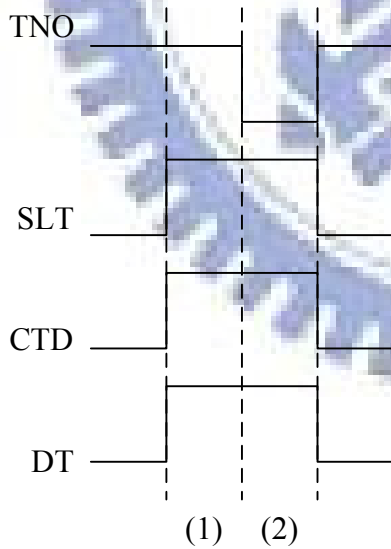


Figure 3-8 (b) time scheme of Goh's model (1) voltage compensation stage (2) V_{TH} -generation input.

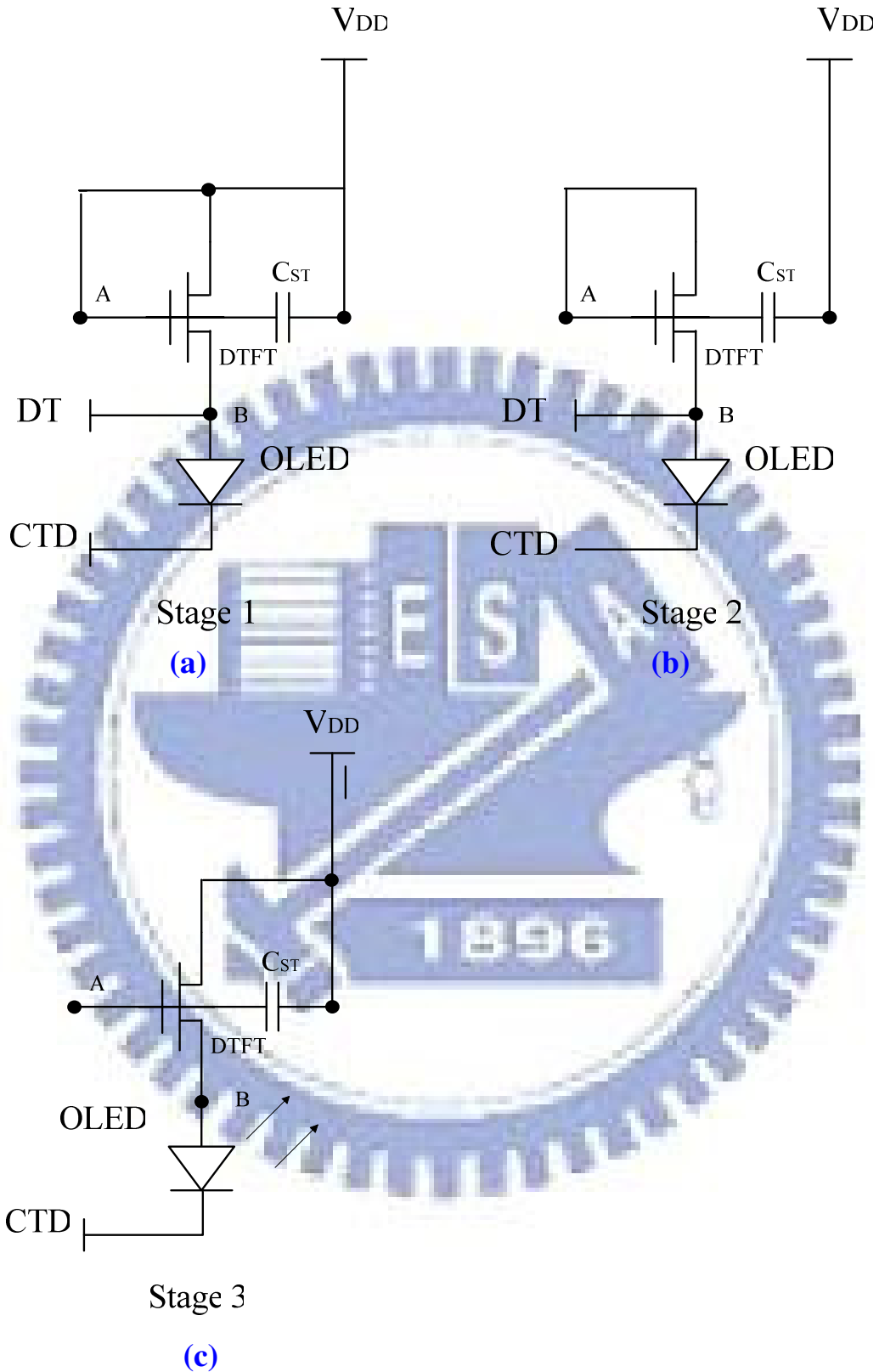


Fig 3-9 equivalent circuit of Goh's proposed pixel circuit in different operating stages (a) voltage compensating stage (b) V_{TH} -generation input stage (c) Display stage

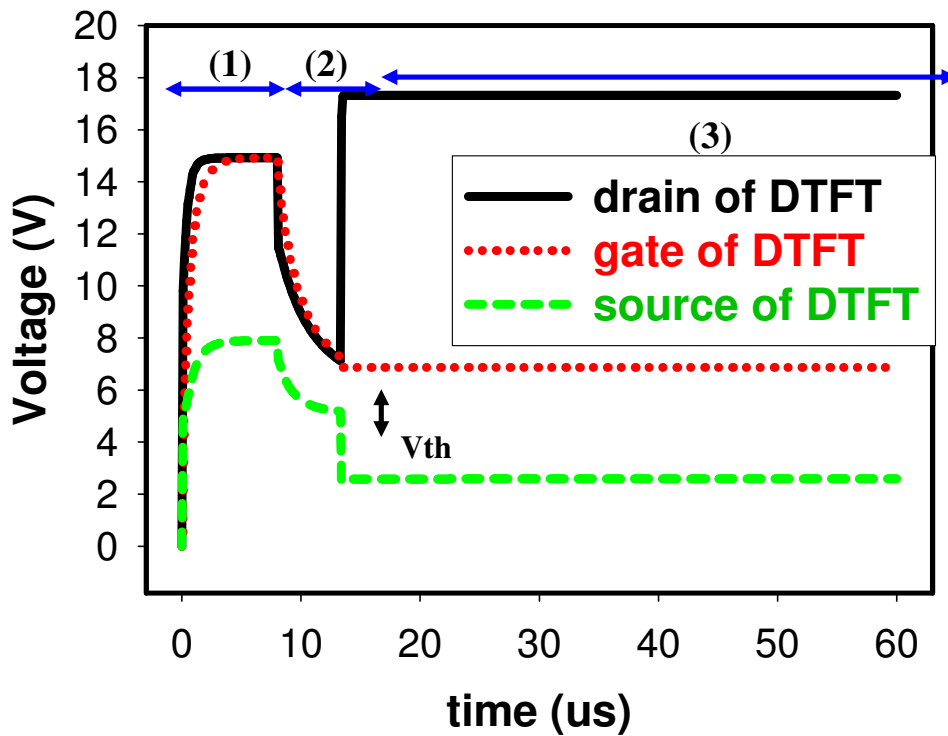


Figure 3-10 Simulation results of the proposed circuit shows gate, drain, and source node voltage of DTFT. (1) voltage compensating stage (2) V_{TH} -generation input stage (3) Display stage

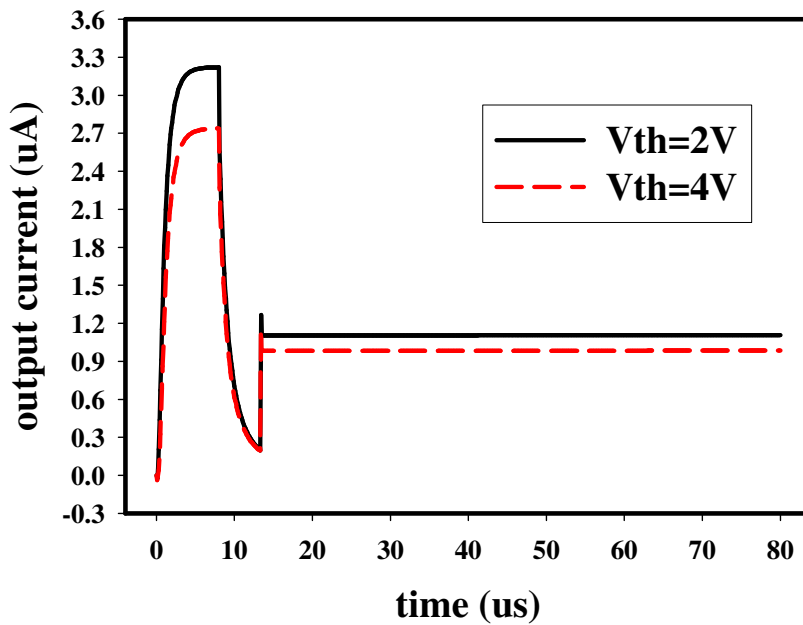


Figure 3-11.. Simulation result of Goh's pixel circuit as threshold voltage shift of DTFT is set to 2.0V.

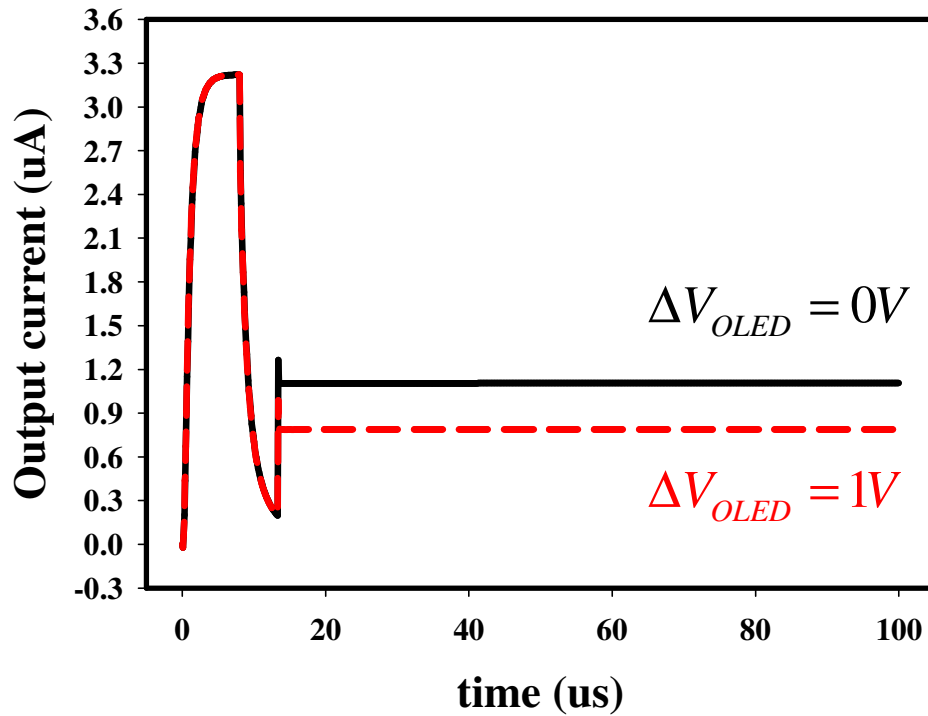


Figure 3-12 Simulation result of Goh's pixel circuit as OLED voltage shift is set to 1.0V.

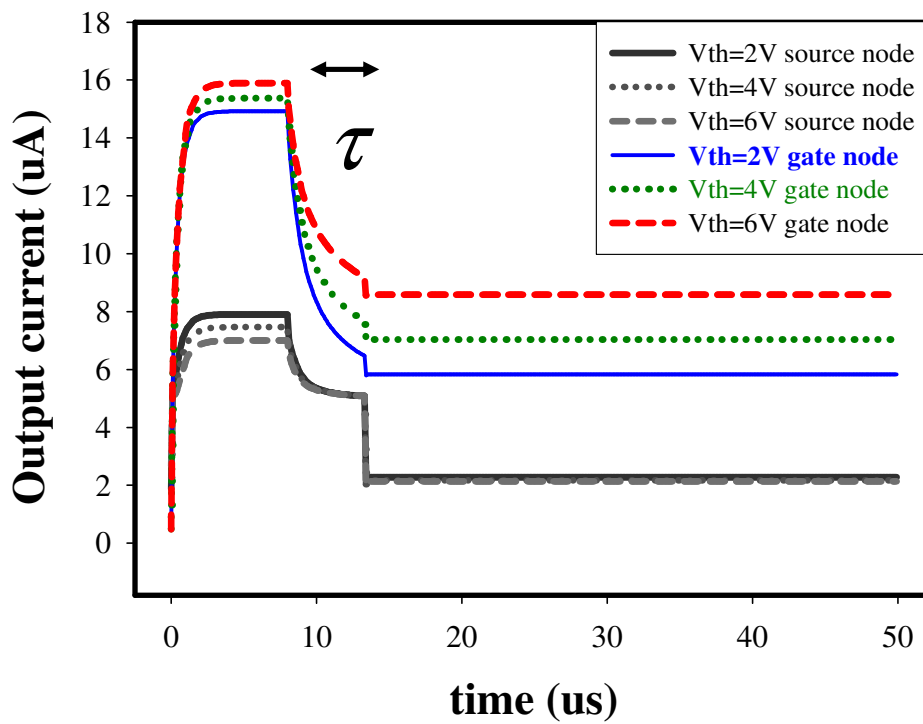


Figure 3-13. the transient result of gate and source nodes of DTFT as the threshold voltage shifts 4V

Vth shift=2V

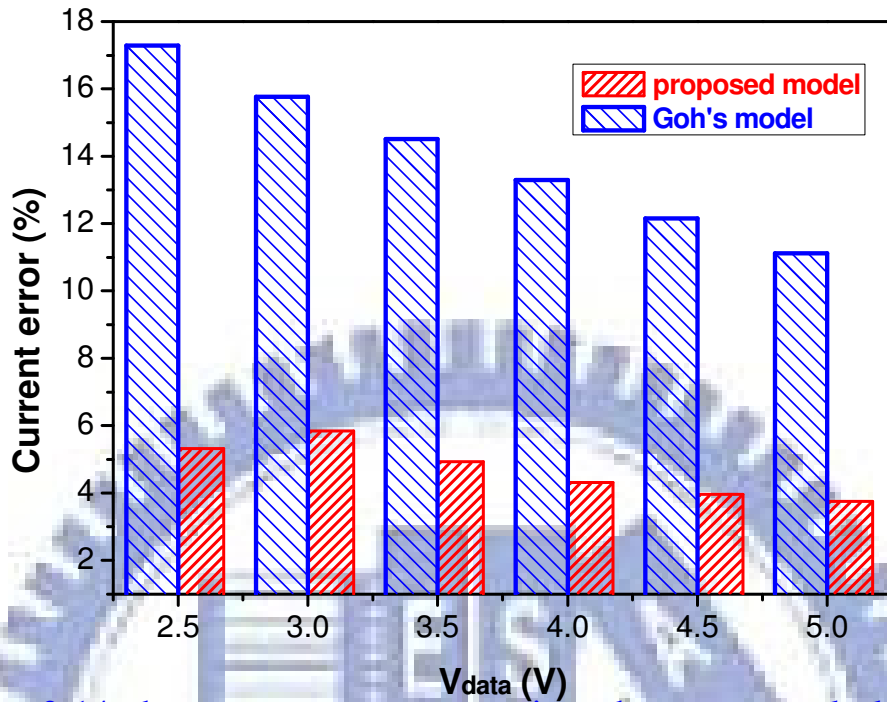


Figure 3-14 the current error comparison between non-leakage type model and Goh's model when the threshold voltage shifts 2V

Vt shift=4V

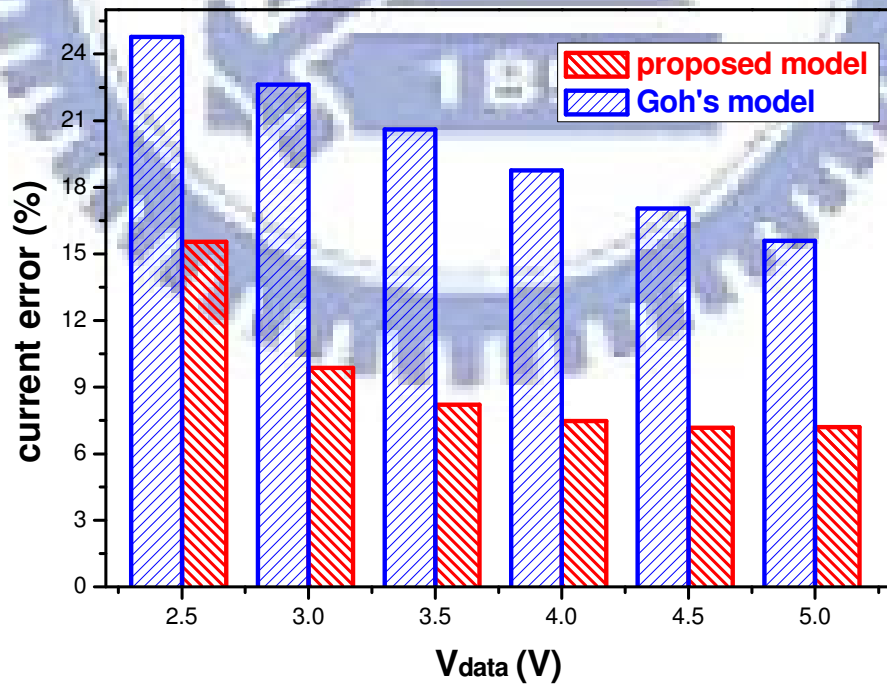


Figure 3-15 the current error comparison between non-leakage type model and Goh's model when the threshold voltage shifts 4V.

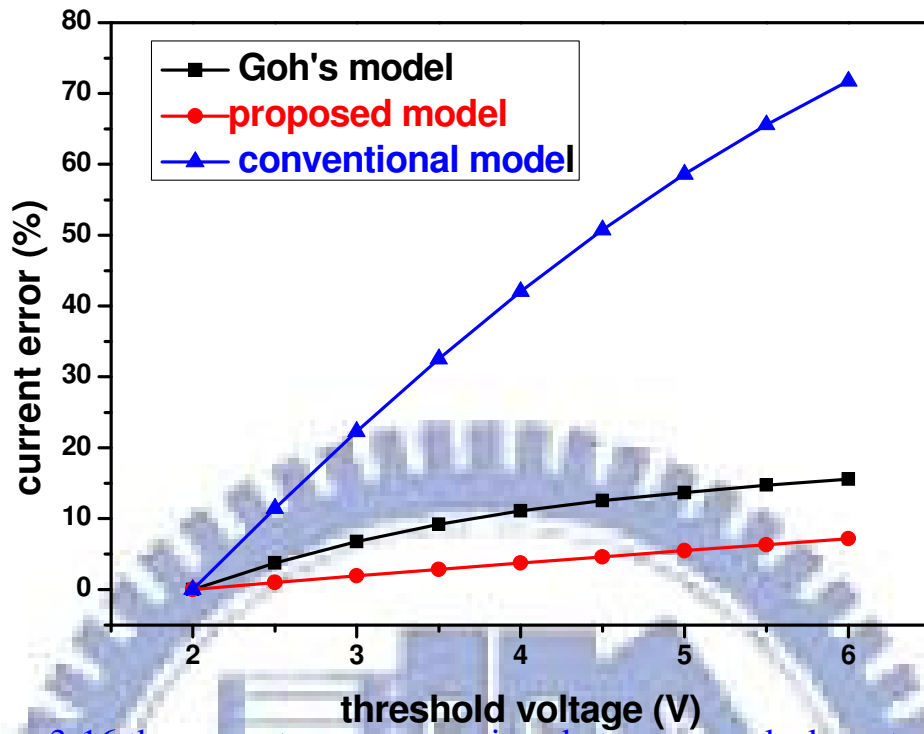


Figure 3-16 the current error comparison between non-leakage type model, Goh's model and conventional model at each threshold voltage.

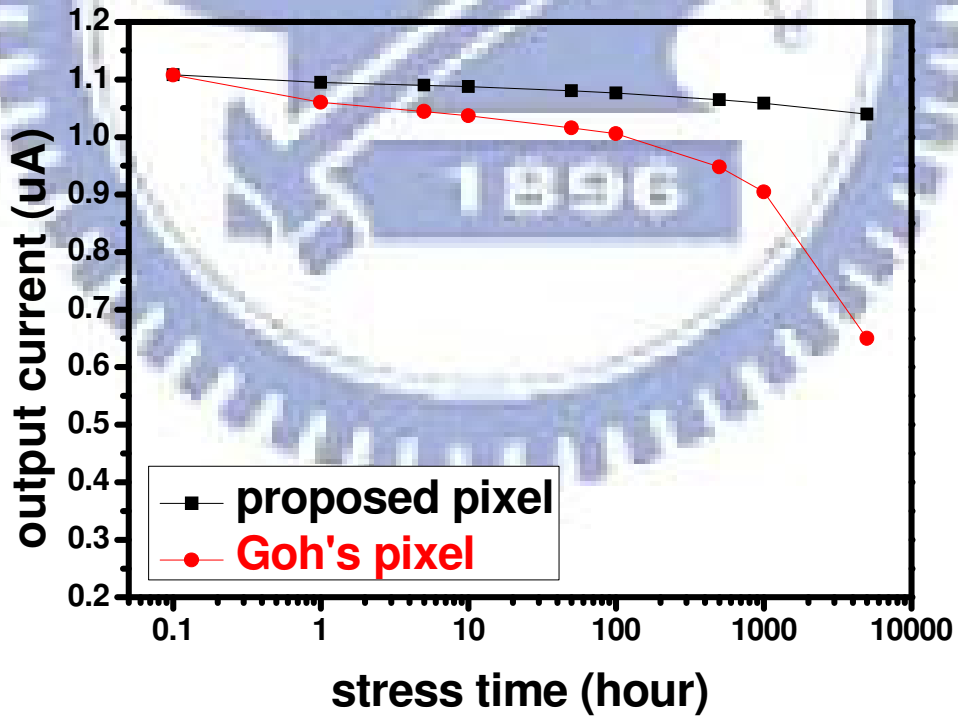
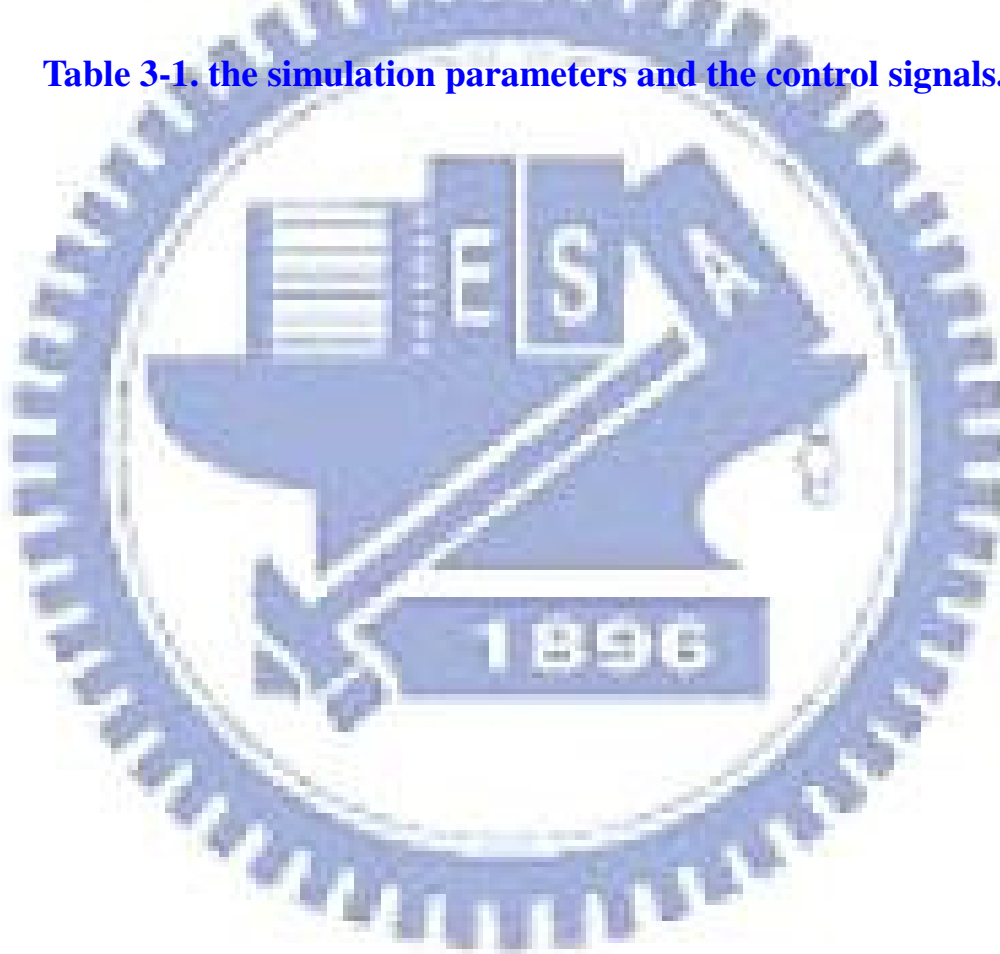


Figure 3-17. driving current comparison between non-leakage type model and Goh's model at stress operation.

a-Si:H TFT					
V _{th}	W/L (MDTFT)	W/L (M2)	W/L (M3)	W/L (M4)	W/L (M5)
2V	35/7 μm	65/3 μm	65/3 μm	65/3 μm	65/3 μm
		Control signal line			
C _{st}	W/L (MOLED)	VDD	V _{s1}	V _{s2}	
0.7 pF	150/7 μm	20V	25V	35V	

Table 3-1. the simulation parameters and the control signals.



Vdata=5v	Current(A)	error rate	Vdata=4.5v	Current (A)	error rate
I ($\Delta V_t=0$)	1.11E-06	0%	I ($\Delta V_t=0$)	8.78E-07	0%
I ($\Delta V_t=0.5$)	1.20E-06	1.02%	I ($\Delta V_t=0.5$)	8.68E-07	1.11%
I ($\Delta V_t=1$)	1.09E-06	1.98%	I ($\Delta V_t=1$)	8.59E-07	2.13%
I ($\Delta V_t=1.5$)	1.08E-06	2.87%	I ($\Delta V_t=1.5$)	8.51E-07	3.07%
I ($\Delta V_t=2$)	1.07E-06	3.76%	I ($\Delta V_t=2$)	8.43E-07	3.96%
I ($\Delta V_t=2.5$)	1.06E-06	4.62%	I ($\Delta V_t=2.5$)	8.36E-07	4.78%
I ($\Delta V_t=3$)	1.05E-06	5.48%	I ($\Delta V_t=3$)	8.29E-07	5.59%
I ($\Delta V_t=3.5$)	1.04E-06	6.33%	I ($\Delta V_t=3.5$)	8.21E-07	6.40%
I ($\Delta V_t=4$)	1.03E-06	7.20%	I ($\Delta V_t=4$)	8.15E-07	7.17%
Vdata=3.5v	Current (A)	error rate	Vdata=3v	Current (A)	error rate
I ($\Delta V_t=0$)	5.13E-07	0%	I ($\Delta V_t=0$)	3.74E-07	0%
I ($\Delta V_t=0.5$)	5.05E-07	1.45%	I ($\Delta V_t=0.5$)	3.68E-07	1.65%
I ($\Delta V_t=1$)	4.99E-07	2.77%	I ($\Delta V_t=1$)	3.62E-07	3.24%
I ($\Delta V_t=1.5$)	4.93E-07	3.91%	I ($\Delta V_t=1.5$)	3.57E-07	4.61%
I ($\Delta V_t=2$)	4.87E-07	4.93%	I ($\Delta V_t=2$)	3.52E-07	5.84%
I ($\Delta V_t=2.5$)	4.83E-07	5.85%	I ($\Delta V_t=2.5$)	3.48E-07	6.94%
I ($\Delta V_t=3$)	4.78E-07	6.70%	I ($\Delta V_t=3$)	3.44E-07	7.97%
I ($\Delta V_t=3.5$)	4.74E-07	7.48%	I ($\Delta V_t=3.5$)	3.41E-07	8.93%
I ($\Delta V_t=4$)	4.71E-07	8.22%	I ($\Delta V_t=4$)	3.37E-07	9.87%
Vdata=4v	Current (A)	error rate	Vdata=2.5v	Current (A)	error rate
I ($\Delta V_t=0$)	6.79E-07	0%	I ($\Delta V_t=0$)	2.61E-07	0%
I ($\Delta V_t=0.5$)	6.71E-07	1.23%	I ($\Delta V_t=0.5$)	2.514E-07	2.50%
I ($\Delta V_t=1$)	6.631E-07	2.36%	I ($\Delta V_t=1$)	2.49E-07	4.66%
I ($\Delta V_t=1.5$)	6.561E-07	3.38%	I ($\Delta V_t=1.5$)	2.44E-07	6.50%
I ($\Delta V_t=2$)	6.50E-07	4.31%	I ($\Delta V_t=2$)	2.39E-07	8.32%
I ($\Delta V_t=2.5$)	6.44E-07	5.16%	I ($\Delta V_t=2.5$)	2.35E-07	10.08%
I ($\Delta V_t=3$)	6.39E-07	5.98%	I ($\Delta V_t=3$)	2.30E-07	11.83%
I ($\Delta V_t=3.5$)	6.33E-07	6.74%	I ($\Delta V_t=3.5$)	2.25E-07	13.63%
I ($\Delta V_t=4$)	6.28E-07	7.47%	I ($\Delta V_t=4$)	2.20E-07	15.55%

Table 3-2. whole collection of non-leakage compensating pixel circuit's performance

a-Si:H TFT				
Vth	W/L (MDTFT)	W/L (Sw1)	W/L (Sw3)	W/L (Sw3)
2V	120/4 um	40/4 um	60/4 um	70/4 um
		Control signal line		
Cst	W/L (MOLED)	VDD	SLT, TNO	CTD
0.3 pF	150/7 um	20V	-1~25V	-3~5V

Table 3-3. the simulation parameters and the control signals



Vdata=5v	Current(A)	error rate	Vdata=4.5v	Current(A)	error rate
I ($\Delta V_t=0$)	1.11E-06	0%	I ($\Delta V_t=0$)	9.24E-07	0%
I ($\Delta V_t=0.5$)	1.07E-06	3.76%	I ($\Delta V_t=0.5$)	8.86E-07	4.08%
I ($\Delta V_t=1$)	1.03E-06	6.81%	I ($\Delta V_t=1$)	8.56E-07	7.40%
I ($\Delta V_t=1.5$)	1.01E-06	9.23%	I ($\Delta V_t=1.5$)	8.31E-07	10.05%
I ($\Delta V_t=2$)	9.84E-07	11.12%	I ($\Delta V_t=2$)	8.12E-07	12.15%
I ($\Delta V_t=2.5$)	9.69E-07	12.54%	I ($\Delta V_t=2.5$)	7.97E-07	13.80%
I ($\Delta V_t=3$)	9.56E-07	13.71%	I ($\Delta V_t=3$)	7.84E-07	15.16%
I ($\Delta V_t=3.5$)	9.44E-07	14.77%	I ($\Delta V_t=3.5$)	7.75E-07	16.14%
I ($\Delta V_t=4$)	9.35E-07	15.59%	I ($\Delta V_t=4$)	7.67E-07	17.06%
Vdata=3.5v	Current(A)	error rate	Vdata=3v	Current(A)	error rate
I ($\Delta V_t=0$)	6.28E-07	0%	I ($\Delta V_t=0$)	5.13E-07	0%
I ($\Delta V_t=0.5$)	5.98E-07	4.80%	I ($\Delta V_t=0.5$)	4.85E-07	5.33%
I ($\Delta V_t=1$)	5.73E-07	8.73%	I ($\Delta V_t=1$)	4.64E-07	9.58%
I ($\Delta V_t=1.5$)	5.54E-07	11.88%	I ($\Delta V_t=1.5$)	4.46E-07	13.02%
I ($\Delta V_t=2$)	5.37E-07	14.51%	I ($\Delta V_t=2$)	4.32E-07	15.76%
I ($\Delta V_t=2.5$)	5.25E-07	16.40%	I ($\Delta V_t=2.5$)	4.20E-07	18.11%
I ($\Delta V_t=3$)	5.15E-07	18.11%	I ($\Delta V_t=3$)	4.11E-07	19.83%
I ($\Delta V_t=3.5$)	5.06E-07	19.46%	I ($\Delta V_t=3.5$)	4.03E-07	21.36%
I ($\Delta V_t=4$)	4.99E-07	20.61%	I ($\Delta V_t=4$)	3.97E-07	22.63%
Vdata=4v	Current (A)	error rate	Vdata=2.5v	Current (A)	error rate
I ($\Delta V_t=0$)	6.791E-07	0%	I ($\Delta V_t=0$)	4.15E-07	0%
I ($\Delta V_t=0.5$)	6.707E-07	4.44%	I ($\Delta V_t=0.5$)	3.91E-07	5.78%
I ($\Delta V_t=1$)	6.631E-07	8.07%	I ($\Delta V_t=1$)	3.72E-07	10.50%
I ($\Delta V_t=1.5$)	6.561E-07	10.96%	I ($\Delta V_t=1.5$)	3.56E-07	14.22%
I ($\Delta V_t=2$)	6.498E-07	13.29%	I ($\Delta V_t=2$)	3.44E-07	17.28%
I ($\Delta V_t=2.5$)	6.441E-07	15.09%	I ($\Delta V_t=2.5$)	3.34E-07	19.70%
I ($\Delta V_t=3$)	6.385E-07	16.59%	I ($\Delta V_t=3$)	3.26E-07	21.51%
I ($\Delta V_t=3.5$)	6.334E-07	17.82%	I ($\Delta V_t=3.5$)	3.18E-07	23.42%
I ($\Delta V_t=4$)	6.284E-07	18.76%	I ($\Delta V_t=4$)	3.13E-07	24.78%

Table 3-4. the whole collection of Goh's pixel circuit performance

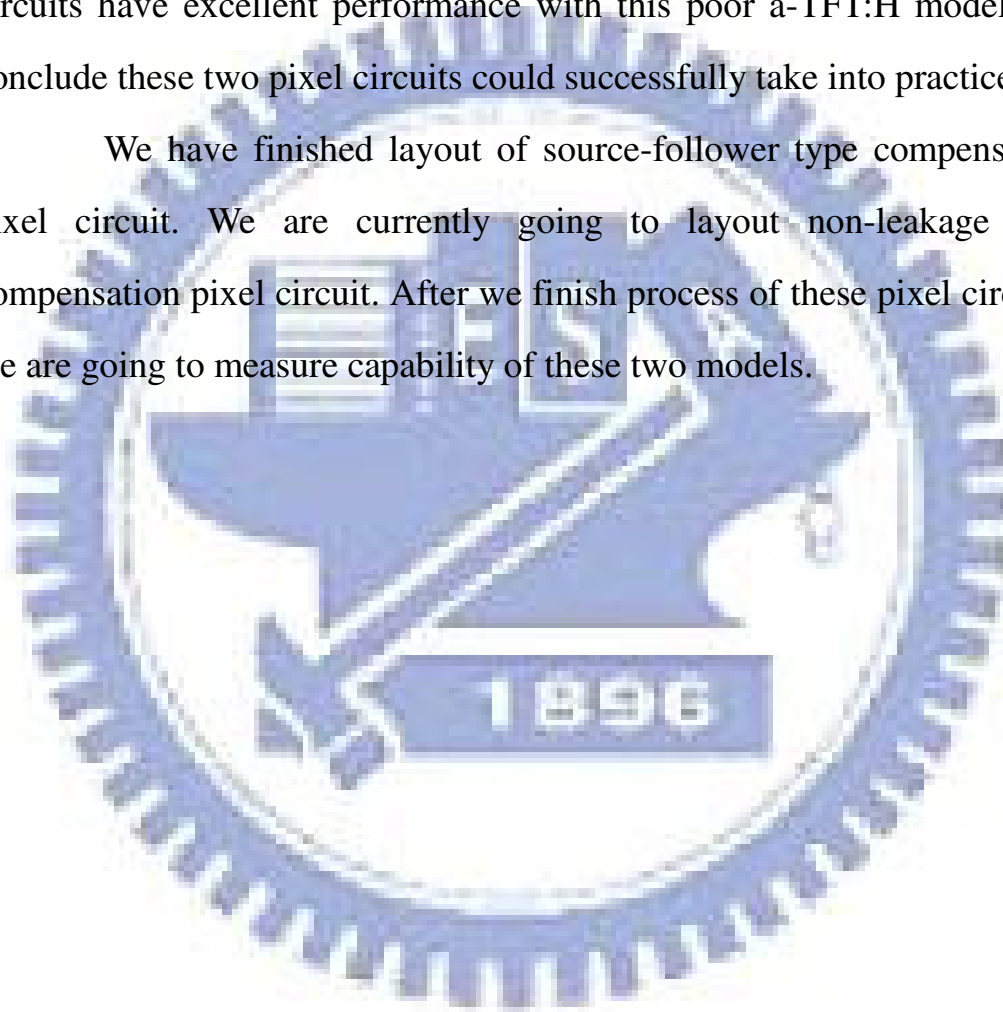
Chapter 4

Conclusions and Future works

AMOLED have attracted more attention in recent years. So far, a-TFT:H is a better choice than LTPS for large and high resolution panel. However, there are two crucial issues to use a-TFTs : threshold voltage shift and OLED voltage degradation. Conventional pixel circuit suffers substantially degradation. As a result, we have introduced two novel pixel circuits to overcome these drawbacks. Firstly, Simulation result of source-follower type pixel circuit is markedly better than conventional pixel circuit. Current error on source-follower type pixel circuit is 3.3% and 6.5% when the threshold voltage of the driving TFT shifts 2V and OLED voltage degradation is 1V, individually. In practical, OLED current is only 6.2% degradation after 5000 hours stress. This source-follower type compensation pixel circuit can apply into products. Secondly, typical voltage-programmed compensation pixel circuits use V_t -generation cycle to compensate the threshold voltage. Nevertheless, V_t -generation time is hard to determine because it varies all the time. As the operation time goes, fixed V_t -generation time would cause significant current error. Therefore, we present a non-leakage type pixel circuit to eliminate current error without using V_t -generation cycle. Simulation result demonstrates that this novel pixel circuit is better than typical compensation pixel circuit. Non-leakage type compensation pixel circuit degrades only 7.3% as threshold voltage shifts 4V and 1.27% as OLED voltage degrades 1V. After 5000 hours stress, non-leakage type

compensation pixel circuit has merely 6.2% degradation. It confirms that non-leakage compensation has a fabulous immunity to a-TFT:H shifts and OLED degradation in practical. Furthermore, our a-TFT:H model has a poor transfer characteristics and we evaluates that a-TFT :H operates in the worst situation : Linear region. As a consequence, two of our pixel circuits have excellent performance with this poor a-TFT:H model. We conclude these two pixel circuits could successfully take into practice.

We have finished layout of source-follower type compensation pixel circuit. We are currently going to layout non-leakage type compensation pixel circuit. After we finish process of these pixel circuits, we are going to measure capability of these two models.



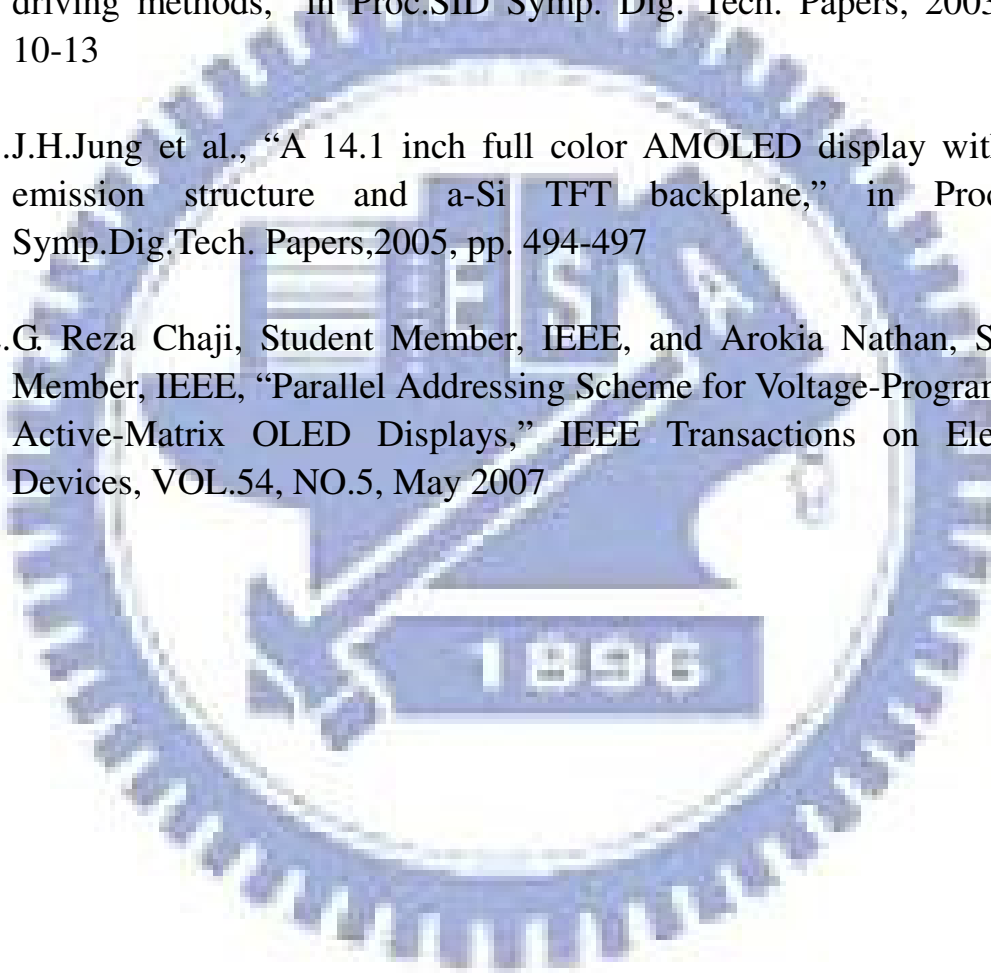
References

1. S. M. Sze, "Physics of Semiconductor Devices", Wiley, New York (1981).
2. M. Quirk and J. Serda, "Semiconductor Manufacturing Technology," Prentice-Hall, Inc., Upper Saddle River, New Jersey 07458. (2001)
3. Donald A. Neamen, "Fundamentals of Semiconductor Physics and Devices," McGraw-Hill, New York (1992)
4. 戴亞翔, "TFT-LCD 面板的驅動與設計 (Design and Operation of TFT-LCD Panels)," 五南圖書出版股份有限公司, Taiwan (2006)
5. 陳金鑫, 黃孝文, "OLED 有機電激發光材料與元件 (Organic Electroluminescent Materials & Devices)," 五南圖書出版股份有限公司, Taiwan (2005)
6. M. Stewart, R. S. Howell, L. Pires, M. K. Hatalis, W. Howard, and O. Parche, "Polysilicon VGA active matrix OLED displays-Technology and performance," in IEDM Tech.Dig.,1998, pp.871-874.
7. S. Luan and G.W. Neudeck, "An experimental study of the source/drain parasitic resistance effects in amorphous silicon thin film transistors," in J. Appl. Phys. 72(2) ,15 July 1992
8. S. Paul, A. J. Flewitt, W. I. Milne, and J. Robertson "Instability measurements in amorphous hydrogenated silicon using capacitance-voltage techniques," in Appl. Phys. Lett., 11 May 2005
9. Yue Kuo, "Thin film transistors material and process-Volume 1: Amorphous silicon thin film transistors," Kluwer Academic Publishers, Boston/Dordrecht/New York/London (2004)

10. S. Martin, C.S. Chiang, J.Y. Nahm, T. Li, J. Kanicki and Y. UGAI, "Influence of the Amorphous Silicon Thickness on Top Gate Thin-Film Transistor Electrical Performances," *Jpn.J.Appl.Phys.* Vol. 40(2001) pp.530-537
11. Yue Kuo, "Thin film transistors material and process-Volume 2: Polycrystalline silicon thin film transistors," Kluwer Academic Publishers, Boston/Dordrecht/New York/London (2004)
12. John Y. W. Seto, "The electrical properties of polycrystalline silicon films," *J. Appl. Phys.*, vol.46,No. 12, Dec. 1975
13. G. Baccarani, B. Ricco and G. Spadini, "Transport properties of Polycrystalline silicon films," *J. Appl. Phys.* 49(11), Nov. 1978
14. J. Levinson, F.R. Shepherd, P. J. Scanlon, W. D. Westwood, G. Este, M. Rider, "Conductivity behavior in polycrystalline semiconductor thin film transistors " *J. Appl. Phys.* 53(2), Feb. 1982
15. K. R. Olasupo and M. K. Hatalis, "Leakage Current Mechanism in Sub-Micron Polysilicon Thin Film Transistors," *IEEE Trans. on Electron Devices*, vol. 43, No. 8, August 1996
16. Y. Uraoka, N. Hirai, H. Yano, T. Hatayama and T. Fuyuki, "Hot Carrier Analysis in Low-Temperature Poly-Si Thin Film Transistors Using Pico-Second Time-Resolved Emission Microscope," *Electron Device Letters*, vol. 24, No. 4, April 2003
17. M.J.Powell, C. Van Berkel, and J.R.Hughes, "Time and temperature dependence of instability mechanisms in amorphous silicon thin film transistors," *Appl.Phys.Lett.*, vol.54,no.14,pp.1323-1325,1989
18. M.A.Dawson and M.G.Kane,"Pursuit of active matrix organic light emitting diode displays," in *SID tech.Dig.*,2001,pp.372-375.
19. J.C. Goh, J. Jang, K.S. Cho, and C.K. Kim, "A new a-Si:H thin film transistor pixel circuit for active matrix organic light emitting diodes," *IEEE Electron Device Lett.*, vol.24,no.9,pp. 583-585, Sep.2003.

20. S.H. Jung, W. J. Nam, and M.K. Han, "A new voltage-modulated AMOLED pixel design compensating for threshold voltage variation in poly-Si TFTs," *IEEE Electron Device Letts.*, vol. 25, no. 10, pp.690-692, Oct.2004.
21. J.H LEE, W.J Nam, S.H Jung, and M.K Han, "A new a-Si:H TFT pixel circuit compensating the threshold voltage shift of a-Si:H TFT and OLED for active matrix OLED," *IEEE Electron Device Lett.*, vol.26, No.12, pp. 897-899, Dec. 2005.
22. C.L.Lin and Y.C.Chen, "A novel LTPS-TFT pixel circuit compensating for TFT threshold voltage shift and OLED degradation for AMOLED," *IEEE Electron Device Lett.*, vol. 28, no. 2, pp. 129-131, Feb.2007.
23. C.L. Lin and T.T. Tsai, "A novel Voltage Driving Method Using 3-TFT pixel Circuit for AMOLED," *IEEE Electron Device Lett.* Vol.28, no.6, June 2007.
24. Y.He, R.Horttori, and J.Kanicki, "Current-source a-Si:H TFT active-matrix organic light-emitting displays," *IEEE Electron Device Lett.*, vol.21, pp.590-592, Nov.2000
25. T. Sasaoka, M. Sekiya, A. Yumoto, J. Yamada, T. Hirano, Y. Iwase, T. Yamada, T. Ishibashi, T. Mori, M. Asano, S. Tamura, and T. Urabe, "A 13.0-inch AMOLED display with top emitting structure and adaptive current mode programmed pixel circuit (TAC)," in *Proc. SID Tech. Dig.*, 2001, pp. 384-387.
26. J.H LEE, W.J Nam, S.H Jung, and M.K Han, "A new current scaling pixel circuit for AMOLED," *IEEE Electron Device Lett.*, vol.25, No.5, May 2004.
27. S.J. Ashtiani, P. Servati, D. Striakhilev, and A. Nathan, "A 3-TFT current-programmed pixel circuit for AMOLEDs," *IEEE Trans. Electron Devices*, vol.52, no.7, pp. 1514-1518, Jul.2005

- 28.P.E. Burrow, S.R. Forrest, T.X. Zhou, and L. Michalski, "Operating lifetime of phosphorescent organic light emitting devices," Appl. Phys. Lett., vol. 76 , no. 18, pp. 2493-2495, May 2000.
- 29.M.J.Powell,C. Van Berkel,and J.R.Hughes, "Time and temperature dependence of instability mechanisms in amorphous silicon thin film transistors," Appl.Phys.Lett.,vol.54,no.14,pp.1323-1325,1989
- 30.J.L.Sanford and F.R.Libach, "TFT AMOLED pixel circuits and driving methods," in Proc.SID Symp. Dig. Tech. Papers, 2003, 99. 10-13
- 31.J.H.Jung et al., "A 14.1 inch full color AMOLED display with top emission structure and a-Si TFT backplane," in Proc.SID Symp.Dig.Tech.Papers,2005, pp. 494-497
- 32.G. Reza Chaji, Student Member, IEEE, and Arokia Nathan, Senior Member, IEEE, "Parallel Addressing Scheme for Voltage-Programmed Active-Matrix OLED Displays," IEEE Transactions on Electron Devices, VOL.54, NO.5, May 2007



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碩士班論文題目：有機發光二極體採用非晶態薄膜電晶體之驅動補償
電路研究

(Enhancement of OLED compensation pixel circuit using amorphous
TFTs)

