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The investigation of capture/emission mechanism in high-*k* gate dielectric soft breakdown by gate current random telegraph noise approach

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In this paper, the trapping/detrapping in high-*k* gate dielectrics has been analyzed by gate current random telegraph noise (I_G) measurement. Gate current is suppressed when traps capture electrons and recovers for empty traps. By statistically extracting capture and emission times, we can understand the trap properties. Besides, the influence will be understood by observing the variation of Gate current fluctuation. Through the analysis of the device after soft-breakdown (SBD), the deterioration of the dielectric will change the capture cross section. Moreover, the traps in the SBD path have been identified as the cause of a huge increase in the gate leakage. © *2008 American Institute of Physics*. [DOI: 10.1063/1.3036681]

High-*k* materials have received more attention in recent years for an attempt to replace the SiO_2. However, one of those important issues in high-*k* materials is the trapping/detrapping behavior which gives rise to drain current and V_T instability during the measurement. Previous approaches in exploring high-*k* traps have been conducted mostly by transient related methods.[1,2] These methods are used to look into the interface and near-interface property but the accuracy is challenged if gate dielectric is heavily destroyed.

In this paper, we will utilize the gate current random telegram noise (I_G RTN) method to study the trapping and detrapping in a high-*k* gate dielectric metal-oxide-semiconductor field effect transistor (MOSFET) device. Applications to observe the process-induced traps and post soft-breakdown (SBD) gate current fluctuation will be demonstrated. In the past, I_G RTN has been used in SiO_2 dielectric capacitors, while it has been used for the study of MOSFET with high-*k* dielectric in this work, from which the device SBD has been quantitatively analyzed.

For the experimental work, high-*k* gate dielectric *n*MOSFETs were fabricated using advanced complementary metal-oxide-semiconductor field effect transistor technology. The gate stack consists of a polycrystalline silicon gate electrode, HfSiO as the high-*k* layer, and a SiON interfacial layer. The transistors have an EOT of 1.2 nm, a gate length of 0.09 μm, and a gate width of 0.2 μm.

Figure 1 shows the band diagram of the device. Gate leakage current is considered as direct tunneling current from the substrate to the positively biased gate. When the traps in the dielectrics are empty, the gate leakage will maintain constant as in Fig. 1(a). As trap energy maintains at a level which is equal to that of channel carriers or below, traps will capture electrons from the channel. When the electrons are trapped, they will raise the nearby potential and lower the leakage, as shown in Fig. 1(b).

Figure 2 shows the gate current versus time, in which RTN signals due to traps in dielectrics before (left) and after SBD (right) were observed. For the measurement in Fig. 2(a) before the SBD, gate leakage is hundreds of picoamperes and exhibits a fluctuation with an order of tens of picoamperes. The capture and/or emission is obviously dependent on the gate bias. Here, τ_c is the capture time and τ_e is the emission time. After SBD, Fig. 2(b), the I_G RTN is different from that observed in Fig. 2(a). As a result of the SBD path, we can see a huge increase in the leakage current (with a third-order increase) and a longer time for capture or emission. The SBD path performs as a channel to open or close one or more conductive paths across the dielectrics. As a consequence, electron trapping/detrapping in defects near (or inside) the SB weak spot will induce some local changes in the barrier height as well as the tunneling probability between two neighboring traps.[3] A single electron trapped in a site inside or very close to the conductive path could in principle blockade the majority of the current flowing through the path, as a result of Coulomb repulsion. In addition, a fraction of the conductive paths is not always available for conduction but can be switched on and off, giving rise to the large current fluctuations.

Figure 3 shows the average emission (τ_e) and capture times (τ_c) as a function of V_G. The average capture and

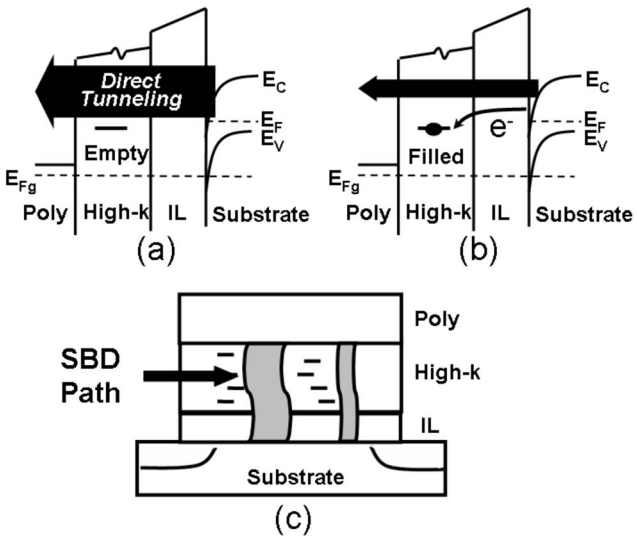

FIG. 1. The band diagram in high-*k* dielectrics (a) with empty trap state where electrons can be captured; (b) with filled trap state and the gate current is reduced. (c) The schematic of SBD paths in the gate dielectric.

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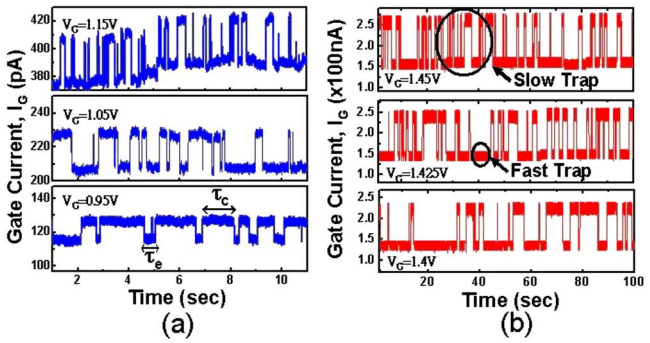

FIG. 2. (Color online) I_G RTN measurement for the device (a) before SRD and (b) after SBD. Capture and emission times are defined in the plot. Note that the gate leakage shows a third-order difference in magnitude.

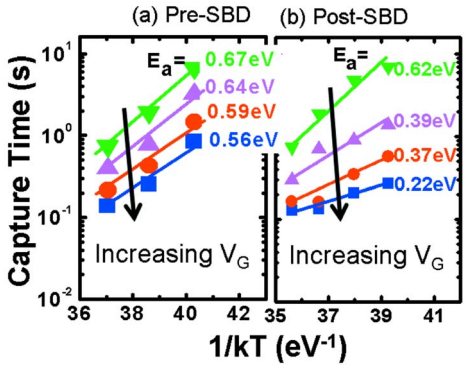

FIG. 4. (Color online) The dependence of capture time with temperature: (a) pre-SBD; (b) post-SBD. The activation energy E_a shows a huge change for devices after the SBD.

emission times are calculated by analyzing numerous switching events for each RTS trace. For pre-SBD, one can see that τ_c for the dielectric traps is an exponential function of gate bias, given by[4]

$$\tau_c = 1/(n\nu_{\text{th}}\sigma), \tag{1}$$

where n is the surface carrier concentration, υ_{th} is the thermal velocity, and σ is the capture cross section of the trap involved. The surface potential ψ_s is a linear function of V_G and $n \sim \exp(q\psi_s/kT)$. Higher carrier concentration or larger V_G implies more electrons participation and reduces the time to capture. On the other hand, time constant of post-SBD is relatively longer than the case of pre-SBD, i.e., τ_c is much longer after device post-SBD. According to Eq. (1), υ_{th} is V_G independent and n increases with gate bias. As a result, the possibility for the increase in capture time in post-SBD is attributed to a smaller σ; i.e., after the formation of conduction path via the device SBD, the effective cross section of traps reduces since some of the traps have been used to built up the SBD conduction path, shown in Fig. 1(c). As a consequence, a smaller cross section for post-SBD gives rise to a longer capture time compared to the pre-SBD ones.

The capture time is influenced by not only capture cross section but also the electric field. Figure 4 shows the temperature dependence of τ_c, which is obviously shorter at higher temperature. Channel carriers are heated at high temperature and more easily surpass the barrier of the capture.[5] The activation energy of capture, E_a, i.e., the slope of ln τ_c versus $1/kT$ plot, is calculated as shown in the plots. The cross section σ can be further related to E_a as[4]

$$\sigma = \sigma_0 \exp(-E_a/kT), \tag{2}$$

where σ_0 is the prefactor of capture cross section. The activation energy is an index to reflect the capture cross section variation, as shown in Eq. (2). Before SBD, negligible change of E_a at different V_G can be seen, i.e., σ is assumed a constant reasonably. After the SBD, Fig. 4(b), we can see a strong dependence of E_a on the gate bias. The main cause is that the capture probability has been enhanced via the SBD path. At high V_G, E_a decreases and is believed to effectively increase the cross section, according to Eq. (2). This amounts to a decrease in the capture time. Hence, the activation energy shows a gate bias dependence feature after SBD.

One major difference can be seen from the comparison of τ_e in Figs. 3(a) and 3(b), in which τ_e shows completely different behavior for pre-SBD and post-SBD. For pre-SBD, τ_e for the dielectric trap is completely independent of V_G. This accounts for the electron escaping through thermionic emission instead of the gate bias; i.e., it shows no field dependence and hence the possibility for direct tunneling back to the substrate or gate is ruled out. In comparison, emission of the electrons trapped within the conventional oxide is electric field dependent.[6] The main difference is that high-k dielectric has larger physical thickness where the electrons captured cannot escape easily through direct tunneling. In other words, time to emission through thermionic emission is much shorter than the time through direct tunneling over the wide barrier. The emission time is given by[7]

$$\tau_e = \frac{\exp[(E_F - E_T)/k_B T]}{g\sigma\nu_{\text{th}} n}. \tag{3}$$

Here, $E_F - E_T$ is the distance from the Fermi energy level to the trap energy level and g is the degeneracy factor, which is usually considered as unity for electrons. Also, from the Arrhenius plot,[8,9] the emission time can be represented by

$$\ln \tau_e T^2 = -\ln \gamma\sigma + (E_{\text{Cd}} - E_T)/kT. \tag{4}$$

Here, $E_{\text{Cd}} - E_T$ is the distance from dielectric conduction band to trap energy level. $\gamma = (\upsilon_{\text{th}}/T^{1/2})(N_c/T^{3/2}) = 3.25 \times 10^{21}(m_n/m_0)$ cm^{-2} s^{-1} K^{-2}, where m_n is the electron density-of-state effective mass.[10] For the post-SBD, the emission time is no longer a constant but varies with gate bias, as shown in Fig. 3(b). It was found that the root cause

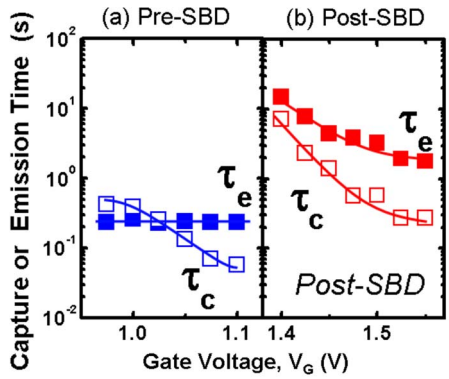

FIG. 3. (Color online) Calculated capture and emission times as a function gate bias for the devices before and after SBD. Note that emission time, in (b), is field dependent after the SBD.

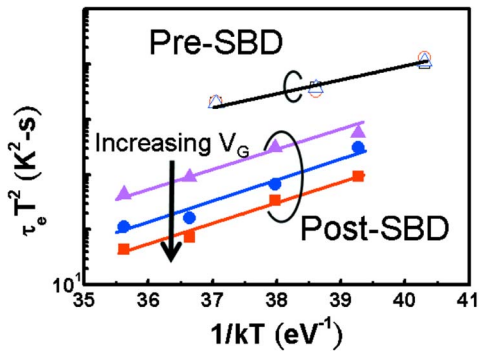

FIG. 5. (Color online) Arrhenius plot for pre- and post-SBD. It shows no changes of τ_e with gate bias, at a specific temperature in pre-SBD case. However, it shows gate bias dependent for post-SBD case. This is attributed to a decrease in the cross section as a result of the formation of a SBD induced conductive path.

is the field dependent property of the capture cross section. It can be justified from the plot in Fig. 5 and Eq. (4). Prior to SBD, the lines in $\tau_e T^2 - 1/kT$ plots have the same slopes and interception with Y-axis, which means $E_{\mathrm{Cd}} - E_T$ is fixed and capture cross section is independent of gate bias. After the formation of SBD path, $E_{\mathrm{Cd}} - E_T$ is roughly identical at distinct gate bias. Nevertheless capture cross section varies with gate bias. It shows the capture cross section decreases with increasing gate bias, from Eq. (4). More importantly, τ_e is largely increased for post-SBD, compared to pre-SBD, as a result of this decreased cross section, σ.

In summary, I_G RTN has been utilized for the study of high-k gate dielectric traps in MOSFETs. The capture and emission mechanisms have been evaluated, especially for a study on the SBD. Several conclusions can be drawn from this study: (1) The gate leakage has been drastically increased as a result of the SBD with a formed conductive path; (2) τ_e and τ_c take longer time since the capture cross section becomes smaller; (3) the major difference between pre-SBD and post-SBD lies in the fact that cross section σ is field dependent for the latter and field independent for the former, shown in Fig. 5, while in most of the studies for SiO_2, σ is considered to be a constant.

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