國 立 交 通 大 學

光電工程研究所

博 士 論 文

晶片黏貼技術應用於三/五族化合物半導體元件效率提升之研究

Study of Efficiency Enhancement for III/V Compound Semiconductor Devices by Wafer Bonding Technique

研 究 生： 李逸駿

指導教授： 郭浩中教授

盧廷昌教授

中華民國九十八年十二月

晶片黏貼技術應用於三/五族化合物半導體元件效率提升之研究

Study of Efficiency Enhancement for III/V Compound Semiconductor Devices by Wafer Bonding Technique

研 究 生：李逸駿　　Student：Yea-Chen Lee

指導教授：郭浩中 教授　　Advisor：Prof. Hao-Chung Kuo

盧廷昌 教授　　Prof. Tien-Chang Lu

國 立 交 通 大 學 電機資訊學院

光電工程研究所

博 士 論 文

A dissertation

Submitted to Institute of Electro-Optical Engineering

College of Electrical Engineering and Computer Science

National Chiao Tung University

in partial Fulfillment of the Requirements

for the Degree of

Doctor of Philosophy

In Electro-Optical Engineering

December 2009

Hsinchu, Taiwan, Republic of China

中華民國九十八年十二月

晶片黏貼技術應用於三/五族化合物半導體元件效率提升之研究

學生：李逸駿　　指導教授：郭浩中 教授
盧廷昌 教授
國立交通大學光電工程研究所

摘　　要

本文主旨是以晶片黏貼的技術製作三五族化合物半導體光電元件之光電特性探討，利用晶片黏貼技術可以達到異質磊晶的需求，也因此克服了三五族化合物光電元件因先天晶格匹配的物理限制下無法製作出的結構並達到較好的光電特性。第一部份是探討將塑膠光纖所用的 650nm 共振腔發光二極體以兩次晶片黏貼之技術，將傳統的砷化鎵基板以高導熱的矽基板取代，並維持與原先相同結構中的正極朝上與上下布拉格反射鏡之化合物半導體材料，所製作出元件的電特性與原先結構相近，而元件光特性上具有較高的光功率輸出、元件對環境溫度與高電流注入影響較低、較低的接面溫度，此外元件於資料傳輸的測試中可達到 622Mbit/sec。第二部分則是介紹晶片黏貼之技術應用在磷化鋁銦鎵的發光二極體元件，前半部份是利用膠合黏貼與溼蝕刻的技術，將傳統吸光且導熱差的砷化鎵基板以高透光的藍寶石基板取代，並以高溫濕蝕刻方式將藍寶石基板側壁做非等相性蝕刻，此具有基板側壁導角的元件將可以大幅增加光淬取效率，另外考量藍寶石基板的散熱特性較差，元件亦製作出覆晶型式且具有側壁導角之發光二極體元件，由於發光區接近矽基板且具有很厚的窗口層於元件表面，因此覆晶型式結構的發光效率與元件特性相較於前者可以大幅提升；而後半段則是利用金屬黏貼技術將砷化鎵基板以矽基板取代，藉此能提高元件在高溫或高電流注入之效率，此外為了提升光淬取效率在元件的表面製作出結構化，其中包含了微米尺寸之碗狀陣列結構，以及在微米碗狀結構中以奈米球塗佈與乾蝕刻方式製作出奈米尺寸之柱狀結構，這相較於傳統表面平整之元件可增加兩倍光淬取效率。第三部分則是介紹將金屬黏貼技術應用在氮化鎵材料之藍綠光發光二極體元件，搭配雷射剝離技術將傳統藍寶石基板以高導熱矽基板取代，首先晶片黏貼前以雷射挖取溝槽將可提升雷射剝離之良率；將優化的鋁銀合金做為歐姆接觸材料與反射層的技術運用結構中，鋁銀合金不但具有高反射率且有較好高溫穩定性，另外為了解決氮表面歐姆接觸不易，高濃度摻雜與清洗方式將可大幅降低接觸電阻，此外優化後氫氧化鉀溶液將可以大幅提升光淬取效率，最後元件相較於傳統藍寶石基板之氮化物發光二極體具有較佳的光電特性、較低的熱阻抗與穩定的可靠度。

Study of Efficiency Enhancement for III/V Compound Semiconductor Devices by Wafer Bonding Technique

Student: Yea-Chen Lee

Advisor: Prof. Hao-Chung Kuo
Prof. Tien-Chang Lu

Institute of Electro-Optical Engineering, National Chiao Tung University

Abstract

This dissertation is study of wafer bonding technique applied for III-V compound semiconductor optoelectronic devices. The wafer bonding technique overcomes hetero-epitaxy growth and achieving better electrical and optical performances which are restricted by physical barrier of lattice match requirement. Firstly, the conventional 650nm RCLEDs for plastic optical fiber with GaAs substrate is replaced with a high thermal conductivity Si substrate by glue bonding and metal bonding technique. This MBRCLEDs is maintained p-side up and DBRs materials structure and without sacrificing electrical performances. The MBRCLEDs has higher output power, high temperature insensitivity, less decay in high current injection, lower junction temperature as compared with conventional RCLEDs. Furthermore, the MBRCLEDs have superior reliability and achieve 622Mbit/ sec. Second, the glue bonding technique is applied to AlGaInP-based LEDs. The conventional GaAs substrate, having inherent drawbacks of poor thermal conductivity and absorbed, is replaced with a transparent sapphire substrate. The sapphire substrate sidewall has geometric shaping by using high temperature chemical etchant. This geometric sapphire shaping LEDs provide superior light extraction efficiency as compared to without one. In order to improve thermal issue in sapphire substrate, the flip-chip structure is applied for improving. The flip-chip AlGaInP-based LEDs have thick window layer of sapphire, which has geometric sidewall shaping, p-side layer close to Si submount for thermal dispersion. This flip-chip structure provides an excellent light extraction efficiency and stable reliability. Furthermore, the metal bonding technique is implemented in AlGaInP-based LEDs, and the GaAs substrate is replaced with Si substrate. The metal bonding LEDs have textured surface for increasing light extraction efficiency. Several textures of micro scale bowls array and nano scale rods added in micro bowls are implemented by anisotropic chemical etching and nano-spheres spin-coating with dry-etching. Comparing to conventional plane surface, the nano-rods added in micro-bowls surface LEDs has two magnitudes output power due to less total internal reflection effect. Finally, the vertical thin film GaN-based LEDs are fabricated by metal bonding and laser-lift-off technique. In order to release internal stress and improve yield after laser lift-off process, a laser cut trench before metal bonding process is used. The optimized Al an Ag composition to form AlAg alloy for p-ohmic contact and high reflector application is applied. The AlAg alloy provides not only high reflectivity but also high thermal stable property. In order to solve n-ohmic contact at N-face n-GaN layer, higher doped n-GaN layer and chemical cleaning at N-face are also implemented. The optimized KOH chemical etchant for surface roughing is applied for enhancing light extraction efficiency. Comparing to conventional sapphire-based GaN-LEDs, the vertical thin film GaN-based LEDs has higher output power under equal current density, lower forward voltage, less wavelength shift under high current injection and high ambient temperature, lower thermal impendence, and higher reliability over 1000hr.

誌謝

經過四年半的博士班生涯，如今能順利取得學位，首先要感謝指導教授郭浩中與盧廷昌教授，經過兩位指導教授耐心的指導與細心教誨下，讓我在這段求學過程中能更佳順利學習與成長，並增加了相關專業知識領域廣度與深度，尤其是郭浩中教授無時無刻的督促與從旁協助，提供相關研究方向與意見，使我在這四年半獲益良多，因此很感謝郭浩中教授對我的提攜。

再來最要感謝的就是碩士班時的學弟兼博士班的同窗李佳恩同學，四年半前一起進入實驗室，四年半後也一起順利的畢業，因我們在實驗室的時間不長，因此這四年半都是相依為命，為了完成畢業的夢想，在實驗上相互幫忙協助與分享結果，資訊互通有無；然而，其間的許多的糊塗事與小插曲也一起渡過與承擔，但其中一些插曲實在仍需再次感謝郭浩中教授的鼎力相助，方能讓我們順利完成學業。

接著要感謝的就是我工作上的貴人，首先最要感謝的是現任禧通科技技術協理邱舒偉博士，感謝邱舒偉博士在我國聯光電服國防役四年與帶我離開後兩年時一路的提攜，從邱舒偉博士身上學到許多專業知識與對事情的執著，也建立我日後對工作上嚴謹的態度；接著要感謝現任聯勝光電總經理張智松博士，感謝張智松博士在國聯光電研發部時期的提攜，並體諒求學過程中所造成的工作困擾；另外感謝現任聯勝光電研發協理顏良吉準博士，感謝顏協理在這兩年中教導我許多過去從未接觸的事物，從顏協理身上獲取無數寶貴的經驗與知識；另外，也感謝目前我工作上的伙伴昌翰、煒竣、逸凡、書帆、琮耀與毅君，感謝你們幫我整理資料、製作樣品與收集相關實驗結果，使我論文資料撰寫能更完整。雖不常在實驗室，但仍感謝許多博士班學弟們的協助，其中包含清華、柏孝、士偉、明華與小賴，感謝你們為我與佳恩所做的一切，也再次感謝學長黃泓文博士於我博士求學生涯最後實質上的協助。

最後，我要把感謝留給我的家人，感謝爸爸、媽媽在我求學過程中做最大努力與無怨無悔的付出，雖然一路風風雨雨、跌跌撞撞，曾經讓您們很失望，但我現今的成就完全歸功於您們全力支持與付出所換來的，感謝您們與逸文對我所付出的一切；最終，感謝未婚妻伊晴六年來的陪伴與照顧，我們將一起努力完成我們未來美好的人生，感謝妳的體諒與付出。也再次感謝曾經幫助過我的人。

逸駿

于 交大光電 2009.12.16

Contents

List of Figures

Chapter 1

Chapter 3

Chapter 4

Chapter 5

CHAPTER 1

Introduction

1.1 Overview

"Wafer bonding" technique generally refers to the process that two mirror-polished wafer adhere to each other. Wafer bonding is alternatively knows as "direct bonding" and "fusion bonding". The wafer bonding technique can combine with any two (ore more) different semiconductor materials on a substrate or film after bonded wafers surface proper polishing and chemical treatment. The wafer bonding technique is independent of whether the bonded materials are crystal or noncrystal, the lattice orientation and parameter, the surface doping type and profile, and the bonded materials thickness. In other words, the wafer bonding technique could solve any materials integrated issue in semiconductor process. Recent years, many groups have been widely investigated wafer bonding technique, especially the III-V compound semiconductors optoelectronic devices are integrated on silicon. The integration of III-V optoelectronic devices on silicon integrated circuits could be formed the optoelectronic integrated circuits (OEICs) [1]-[3]. Te OEICs technique is highly desirable for optical fiber data communications and optical interconnects. The III-V compound semiconductors are main materials for optoelectronic devices, such as optical amplification, laser diodes (LDs), vertical-cavity surface-emitting laser (VCSEL), and light-emitting diodes (LEDs). However, the optical devices of III-V compound semiconductor are grown on III-V materials substrate due to the physical limitation of epitaxy lattice match. Therefore, the integration of III-V optoelectronic devices with silicon for OEICs application could be realized by wafer bonding technique. Wafer bonding technique solves a problem of dislocations caused by the epitaxy lattice mismatch between silicon and relevant III-V compounds semiconductor when the hetero-epitaxial growth is performed. Successful GaAs devices on Si [4], InP/Si [5], and

InP/GaAs [6] wafer bonding have been demonstrated for laser diodes, light-emitting diodes, detectors, and waveguides. Therefore, wafer bonding is an alternative technique for achieving the purpose of growing epi-layer transferred to another substrate or film. By wafer bonding technique, it is accomplished hetero-epitaxial between lattice mismatch materials and without sacrificing devices performances. Therefore, the III-V compound semiconductor optoelectronic devices via this technique are more flexible and valuable for applications.

1.2 Outline of This Dissertation

In this dissertation, the wafer bonding technique is used for enhancing efficiency of III-V compound semiconductor. All of investigations are based on wafer bonding technique, including metal bonding, glue bonding, and twice bonding. The device conventional substrate was removed and replaced with a new substrate, such as a high thermal conductively silicon substrate or a transparent sapphire substrate. After exchanging the conventional substrate, the III-V devices could achieve higher efficiency and characteristic, such as light extraction efficiency enhancement, high temperature insensibility and stability, suitable for high current operating, and stable performances in high temperature ambience.

In chapter 2, the high performances 650 nm resonant-cavity light-emitting diodes (RCLEDs) were demonstrated via high quality epitaxy and excellent chip process. The RCLEDs were designed with different light-output aperture sizes 84, 60, and 40 μm, for different applications of plastic optical fibers. In order to solve the RCLEDs performance in high temperature operation, the metal bonding RCLEDs (MBRCLEDs) with high performances, high temperature insensitively, and high reliability have been successfully fabricated on Si substrates by twice wafer bonding techniques. By wafer bonding technique, the RCLEDs, growing on conventional GaAs substrate, were replaced with a high thermal conductively silicon substrate. MBRCLEDs are that based on RCLED epi-layer structure and

changed GaAs substrate. Therefore, the MBRCLEDs maintained original RCLEDs performances and improve devices characteristic under high temperature ambiance especially. The junction temperature variations of the MBRCLEDs were also relatively smaller as compared with the RCLEDs. Furthermore, the stable beam profile, high reliability over 1000 hours and clearly eye diagram in high temperature operation. These excellent performances of the MBRCLEDs devices should be suitable for high temperature ambiance, high current injection and high data communication applications.

In chapter 3, several methods to enhance AlGaInP LEDs performances were demonstrated. The AlGaInP LEDs performances enhancement key points in this study is to replace the absorbing GaAs substrate with a transparent sapphire substrate or high thermal conductively silicon substrate, and then fabricates surface textured for reducing total internal reflection effect. The LEDs efficiency enhancements are based on wafer bonding techniques of glue bonding and metal bonding process, and the surface roughness, geometric structure and flip-chip techniques were also applied for enhancing AlGaInP LEDs performances. The AlGaInP LEDs with a transparent sapphire substrate were fabricated by glue bonding method. This transparent sapphire substrate is a geometric shaping sidewall (GSS-LEDs) structure by chemical wet etching processes. The GSS-LEDs surface has a nano-roughened texture by natural mask and chemical wet etching processes in order to improve light extraction efficiency. It was demonstrated that the GSS-LEDs structure could not only reduce the TIR effect but increase more probabilities of output light escaping from the transparent substrate due to the oblique sidewall structure. The GSS-LEDs are still not suitable for high current injection or high temperature ambience operating especially in short wavelength of AlGaInP system material. For this reason, a novel flip-chip AlGaInP-LEDs structure which has a thick geometric sapphire substrate (GSSFC-LEDs) window layer were demonstrated using glue bonding and flip-chip bonding techniques. This novel GSSFC-LEDs structure shows higher

output power, longer reliability and higher wall-plug efficiency as compared with GSS-LEDs, conventional flip-chip LEDs (CFC-LEDs), and conventional glue bonding LEDs (GB-LEDs). Finally, the AlGaInP epi-layers were bonded to a high thermal conductive Si substrate via metal bonding technique due to the sapphire is not a perfect substrate in devices, and achieved excellent light extraction efficiency using micro- and nano-scale surface textured technique. This structure, having micro-bowls and nano-rods texture on surface has the highest output power as compared with micro-bowls only and plane surface devices.

In chapter 4, the InGaN/ GaN LEDs efficiency was enhanced by metal bonding, laser lift-off, and surface roughness technique. The conventional InGaN/ GaN LEDs with non-conductive and poor thermal conductivity property of sapphire substrate were replaced with Si substrate. Firstly, a novel and simple structure of single electrode pad (SEP-LEDs) in GaN-based LEDs are demonstrated. The concept was come from laser diode process of face coating. The ITO film was deposited on SEP-LEDs sidewall, and then a conductive current path was formed from chip sidewall to sapphire backside by ITO film. The SEP-LEDs has high performances than conventional lateral LEDs (CL-LEDs) although both substrates are sapphire. It is attributed that SEP-LEDs has more light output area and uniform current spreading properties. However, the SEP-LEDs structure can not be applied in future LED applications of high output power, high efficiency under higher current density, temperature insensitivity operating, and high reliability property after all. For this reason, the InGaN/ GaN vertical thin film LEDs (VTF-LEDs) structure is an important tread toward future LED lighting application. Many techniques and experiments are implanted in VTF-LEDs for improving VTF-LEDs performances and enhancing efficiency, such as high thermal stable Al-Ag alloy metal for reflector and *p*-ohmic contact, laser double cut before LLO process, proper chemical treatment and heavily doped in *n*-GaN layer for solving N-face surface of *n*-GaN issue, and optimized KOH chemical for surface random rough. By above mentioned, it

is demonstrated that the VTF-LEDs with lower forward voltage, uniform current spreading, high efficiency under the same current density, less wavelength variation in high current and high temperature ambience operating, higher maximum junction, and excellent thermal impendence performances as compared with CL-LEDs.

REFERENCE

[1] H. Wada; T. Takamori; and T. Kamijoh, “Room-temperature photo-pumped operation of 1.58-μm vertical-cavity lasers fabricated on Si substrates using wafer bonding”, *IEEE Photon. Technol. Lett.*, vol. 8, pp. 1426–1428, Nov. 1996.

[2] H. Wada; T. Kamijoh, “Room-temperature CW operation of InGaAsP lasers on Si fabricated by wafer bonding”, *IEEE Photon. Technol. Lett.*, vol. 8, pp. 173–175, Feb. 1996.

[3] Long Chen, Po Dong, and Michal Lipson, “High performance germanium photodetectors integrated on submicron silicon waveguides by low temperature wafer bonding”, *Optics Express*, Vol. 16, Issue 15, pp. 11513-11518, 2008.

[4] A. Georgakilas , M. Alexe , G. Deligeorgis , D. Cengher , M. Androulidaki , S. Gallis , Z. Hatzopoulos and G. Halkias “III-V material and device aspects for the monolithic integration of GaAs devices on Si using GaAs/Si low temperature wafer bonding,” *CAS 2001 Proc.* Piscataway, NJ: IEEE, pp. 239, 2001.

[5] Q.-Y. Tong, Q. Gan, G. Hudson, G. Fountain, and P. Enquist, “Low temperature InP/Si wafer bonding”, *Appl. Phys. Lett.* 84, 732 (2004).

[6] Hui Huang, Xiaomin Ren, Xinyan Wang, Qi Wang, and Yongqing Huang, “Low-temperature InP/GaAs wafer bonding using sulfide-treated surface”, *Appl. Phys. Lett.* 88, 061104 (2006).

CHAPTER 2

High-Performance AlGaInP-Based Resonant-Cavity Light-Emitting Diodes in Wafer Bonding Technology

2.1 Introduction

In recent years, low-cost and short-distance-network optical devices based on the polymethyl methacrylate (PMMA) plastic optical fiber (POF) have been widely used for data communication, medium, automotive industry, and industrial sensors etc... The new development of these optical devices were focused on such factors as high power, high efficiency, high modulation speed, high coupling efficiency, reliability, low-cost fabrication, and high temperature insensitivity. On the basis of these requirements, the AlGaInP-based red 650 nm resonant-cavity light-emitting diodes (RCLEDs), according to these requirements, have been developed. A typical RCLED structure consists of an active layer for light emitting placed in a Fabry-Perot (F-P) resonator [1]. The F-P mirrors used are typically quarter-wavelength ($\lambda/4$) thickness semiconductors, dielectric distributed Bragg reflectors (DBRs) [2], or higher reflective metal films [3]. The RCLEDs structures are different from the conventional LEDs in some properties, such as optical profiles of directionality, narrower spectral bandwidth, higher quantum efficiency, higher output intensity, and suitable for optical communication of light sources [4]-[7]. The RCLEDs structure is similar to that of vertical-cavity surface-emitting lasers (VCSELs). Both of them have a high reflectivity (>98%) n-DBR as a function of bottom reflector, but the amount of top p-DBR pairs in RCLEDs structure is less than that in VCSELs. Actually, red visible VCSELs could not be operated in high-temperature environments such as in automobile parts or higher-driving-current modules. The VCSELs devices are sensitive to temperature variations due to inherent material characteristics [8]. Nevertheless, this RCLEDs devices drawback of

temperature sensitivity could be controlled by modifying the detuning cavity wavelength [9]. The detuning wavelength ($\lambda_{detuning}$) means that the different wavelengths of the F-P resonator and the quantum well:

$$\lambda_{detuning} = \lambda_{FP} - \lambda_{QW}, \quad (2\text{-}1)$$

where λ_{FP} and λ_{QW} are the wavelengths of the F-P resonator and quantum well, respectively. The most important function of optimum detuning structure wavelength is that the devices temperature insensitively. In short-distance optical communication applications, POF offers several advantages over glass fiber such as low cost, higher number aperture (NA) for high coupling efficiency, decreasing fiber weight, visible light source for safety, and fiber flexibility. In order to meet these demands for high-performance POF communication, selected a light source to achieve high efficiency, reliability, suitable modulation bandwidth, operating-temperature range extensity, and higher coupling efficiency is very important. Therefore, the visible red 650 nm RCLEDs is more ideal light source than conventional LEDs and VCSELs for the standard step-index polymethyl methacrylate (PMMA) based fibers due to the low-loss band (0.2 dB/m) at 650 nm [10]. The attenuation in plastic fiber is shown in figure 2.1. The preferred communication window of plastic fibers is at 650 nm, where the loss is of the order of 0.1-0.2dB per meter. At even shorter wavelengths, the attenuation in plastic fibers decreases.

In this chapter, we will discuss the high performance of 650 nm RCLEDs devices under special epi-structure and chip process firstly. And then we will introduce the high efficiency and temperature insensitive RCLEDs which were produced using twice wafer bonding technique. Finally, we will present all performances not only electrical and optical properties but also devices performances of applying on POF data communication.

2.2 The RCLEDs Principle Operation and Epi-Structure Design

The epitaxial structure of 650nm RCLEDs is very similar to red VCSELs. Both of them have a high reflective mirror in bottom, which the reflectivity is approximately 100%. Nevertheless, RCLEDs has lower number of periods top DBRs, which normally is between four and eight periods. In the spontaneous emission of RCLEDs is no longer isotropic due to the Fabry-Perot resonances certain wavelengths are allowed for certain directions only. A detailed theoretical analysis of properties of RCLEDs was shown as reference of Benisty et al. [11]. Here the points will be focused on the simple contentions and shows the relationship between the wavelength detuning and the enhancement of light extraction efficiency.

The light source centered between a reflectivity r_1 of top DBRs for electrical field and a bottom DBRs with a reflectivity r_2 can find a formula as following for the electrical field at the top DBRs by calculating the path and phase differences, and summing up for multiple paths in Fabry-Perot cavity:

$$E_{r1}(\theta) = (1-r_1)e^{i\phi}\left[\frac{e^{-i\phi/2}+r_2 e^{i\phi/2}}{1-r_1 r_2 e^{i\phi}}\right], \qquad (2\text{-}2)$$

where θ is the angle between the normal top DBRs vector and the propagation direction of the output light wave. The phase factor ϕ is given by:

$$\phi = 2\pi m\frac{\lambda_{res}}{\lambda}\cos\theta, \qquad (2\text{-}3)$$

where λ_{res} is the resonance wavelength of the cavity and m is the order of the cavity. The light extraction efficiency η_{escape} could be estimated by integrating the power emitted into the escape cone divided by overall power emitted into all direction:

$$\eta_{escape} = \frac{\int_{\theta=0}^{\theta=\theta_c} E_{r1}(\theta')\cdot E_{r1}^{*}(\theta')\sin\theta' d\theta'}{\int_{\theta=0}^{\theta=\pi} E_{r1}(\theta')\cdot E_{r1}^{*}(\theta')\sin\theta' d\theta'}, \qquad (2\text{-}4)$$

where θ_c is the critical angle for total reflection. The intensity of the top DBRs optical filed

which has an m=1 cavity and varied reflectivity was shown in figure 2.2. The useful mode for light extraction, since the output light that propagates in directions with $\theta<\theta_c$ could be emitted through the top DBRs. In figure 2.2, we can find that the mode is concentrated more and more inside the light escape core with increasing the reflectivity of the top DBRs. Depending on the order of the cavity this leads to an optimal reflectivity of the top DBRs under the reflectivity of the bottom DBRs should be approximately to 100%. The light extraction efficiency could be further fine tuned using a detuning d between the quantum well and the normal Fabry-Perot resonance:

$$d = \frac{\lambda_{res} - \lambda_{qw}}{\lambda_{res}}, \qquad (2\text{-}5)$$

This equation is illustrated and shown in figure 2.3. In equation 2-4, the Fabry-Perot resonances have to increase a factor of $sin\ \theta$, thus it could be enhanced more output light to emit in solid angle element. It is useful to have the peak emission wavelength of the quantum wells tuned to be in resonance with the cavity at an oblique angle within the escape cone, and an optimum for the detuning is around d=4% [12]. The AlGaInP RCLEDs design should be comprised a higher reflectivity bottom DBRs and the top DBRs with a reflectivity (r_1^2) around 0.3 to 0.8. In order to fit the extraction into the Fabry-Perot extraction mode and inside the escape cone, the spectrum of quantum well emission should be small enough. The effective cavity length consisting of an active layer and the penetration depths into the DBRs should be as small as possible demanding to use the maximum value of reflective index contrast for reducing the absorption in the DBRs.

An important parameter in view of the POF communication system application is the RCLED modulation bandwidth. Two major factors can influence the modulation bandwidth: the non-radiative recombination lifetime and carrier density in the active region. The small signal modulation bandwidth dependence on non-radiative recombination, injected current (I) and active region volume (V) can be approximated by:

$$f_{-3dB} = \frac{1}{2\pi}\left(\frac{1}{2\tau_{nrl}} + \sqrt{\left(\frac{1}{2\tau_{nrl}}\right)^2 + \frac{BI}{qV}}\right), \qquad (2\text{-}6)$$

where q is the primary charge and B is the band-to-band recombination rate. Usually the carrier loss though leakage current does not taken into consideration but for the red wavelength range the carrier leakage significantly affects the carrier lifetime and the current density. Since the leakage carrier are finally lost by non-radiative recombination outside the active region and it is difficult to discriminate the leakage lifetime, an overall non-radiative recombination lifetime (τ_{nrl}) including the leakage lifetime should be considered.

In this study, the epitaxy structure were grown on a 3-inch GaAs substrate tilted by 6° toward the <111> direction by a low pressure (50 Torr) metal-organic vapor phase epitaxy (MOVPE) system. Trimethylindium (TMIn), trimethylgallium (TMGa), trimethylaluminum (TMAl), phosphine (PH_3), and arsine (AsH_3) were used as the source materials of In, Ga, Al, P, and As respectively. The substrate temperature during the growth of the RCLEDs structures was 750ºC approximately. Si_2H_6 and CCl_4 were used for *n*-type and *p*-type doping sources respectively. The epitaxial structure consist a 35 pairs *n*-DBR of *n*-$Al_{0.5}Ga_{0.5}As$/ $Al_{0.92}Ga_{0.08}As$ layer with Si doping, which the carrier concentration was about 3×10^{-18} cm^{-3}. The reflectivity of the *n*-DBR was over 98% and specific contact resistance was less than 1×10^{-6} Ω-cm^2. The active layer composed of three +1% strain un-doped GaInP quantum wells and 1-λ cavity thickness $(Al_{0.7}Ga_{0.3})_{0.5}In_{0.5}P$ barrier layer between top and bottom DBRs [13]-[14]. The background concentration of quantum wells was less than 1×10^{-16} cm^{-3} and its uniformity of composition and thickness was about 2%.An oxidation layer with a higher aluminum concentration of *p*-$Al_{0.98}Ga_{0.02}As$ was grown on the active layer. A 6 p-DBR pairs of *p*-$Al_{0.5}Ga_{0.5}As$/ $Al_{0.92}Ga_{0.08}As$ layers with C-doped were grown on active layer. Finally, a 5nm thick p^+-GaAs contact layer with heavily doped (over 5×10^{-19} cm^{-3}) was grown on the surface for *p*-ohmic contact layer. Above-mentioned layer by layer were shown in figure 3.4.

2.3 Fabrication Processes of 650 nm AlGaInP-based RCLEDs

2.3.1 Standard 650 nm RCLEDs Processes with GaAs Substrate

In standard 650 nm RCLEDs processing, the wafer was cleaned with a standard solvent firstly. The Ti/ Pt for *p*-ohmic contact ring were deposited on p^+-GaAs cap by electron beam, as shown in figure 2.5.1. Figure 2.5.2 shows that a thick SiN_x about 1 μm was grown on wafer surface by plasma-enhanced chemical vapor deposition (PECVD) as a function of hard masks for mesa dry etching and protection steam during oxidation process. The circular mesa size of 130 μm was defined using standard photolithography and a chemical etchant was shown in figure 2.5.3, and then the inductivity coupled plasma (ICP) etcher were used to etch mesa with BCl_3, Cl_2, Ar and N_2 reactive mixture gas through the p^+-GaAs cap, *p*-DBR, $Al_{0.98}Ga_{0.02}As$ oxidation layer until the active layer was exposed as shown in figure 2.5.4. The wafer was loaded into a 450°C furnace which was filled with steam. A steam reacted to this high Al concentration oxidation layer from this layer edge to center, as shown in figure 2.5.5, and then a high resistivity region of AlO_x material was formed through the wet thermal oxidation process. The final aperture size of 84 μm for light output was produced using wet thermal oxidation process. In order to avoid the steam damage and metal line connection, planarization device structure is necesssry. In figure 2.5.6 shows that the thick polyimide with photography sensitization function was coated on wafer surface. After polyimide was exposed and developed, the wafer was held in a 420°C furnace and N_2 ambience to cure for 2 hours to release stress and strengthen the polyimide structure, as shown in figure 2.5.7. Figure 2.5.8 shows that the SiNx film growing on p-contact metal ring was removed via photolithograph and chemical etching. In figure 2.5.9, *p*-electrode pad of Ti/ Pt/ Au for wire bonding was selective deposited and *n*-GaAs substrate was grind and polished to 100 μm. The *n*-GaAs substrate was deposited with Au/AuGe. Finally, the wafer was thermal annealed in a 380°C

furnace for 10 min and the wafer was diced into 300 × 350 μm^2 chips.

2.3.2 High Performances 650 nm RCLEDs Processes with Si Substrate in Twice Wafer Bonding Technique

As we know, the compound semiconductor of AlGaInP-based materials have several inherent drawbacks, such as the limited barrier height in the GaInP/AlGaInP quantum-well structures and larger thermal resistively due to the large mass difference between gallium and indium [15]-[16]. These GaInP/ AlGaInP quantum wells devices will be affected by high temperature ambiance, so the epi structure needs to be properly designed to high temperature insensitively [17]. Most RCLEDs applications require stability during high temperature operation, and therefore the wafer bonding technique was applied in this study to fabricate 650 nm RCLEDs devices for high temperature insensitive ability. Since the thermal conductivity of Si is 1.31 $W/cm \cdot K^{-1}$ at room temperature, which is larger than GaAs (0.44 $W/cm \cdot K^{-1}$) [12]. We replaced the conventional GaAs substrate with a Si substrate to improve the thermal stability properties via twice bonding techniques of wax-bonding and metal-bonding.

This novel device of metal bonding RCLEDs (MBRCLEDs) epi-structure is approximately to RCLEDs, the difference is that an $In_{0.5}Ga_{0.5}P$ etching stop layer was inserted between the GaAs buffer layer and n-DBRs. The MBRCLEDs processes before GaAs substrate backside Au/ AuGe deposited is the same as RCLEDs chip fabrication. The schematic diagram of the conventional RCLEDs device was shown in figure 2.6.1, and the GaAs substrate was thinned to 100 μm at this time. Figure 2.6.2 shows that the wafer was temporarily bonded to sapphire substrate using wax in vacuum at 120°C ambient. The GaAs substrate and etching stop layer were removed by chemical etching solutions of $1NH_4OH:10H_2O_2$ and $1HCl:10H_2O$ respectively, as shown in figure 2.6.3. Figure 2.6.4 shows that the bonding metals Ti/ Pt/ Au/ In were orderly deposited on the n-Si substrate, and the

AuGe/ Au/ Ti/ Pt/ Au metals were deposited on epi-layer. The Au and In metal were used for eutectic metals in the bonding process. Ti and AuGe metals were used for the Si substrate and n-ohmic contact layers, respectively. The wafer pairs were loaded into graphite jig and an external pressure 0.175 Kg/cm^2 was applied on the wafers during the wafer bonding process. The jig was then loaded into an oven and annealed at a temperature varying from 180°C to 230°C for 120 min in nitrogen ambient for wafer bonding process. After this process was completion, the bonded wafer pairs were immersed in 90°C organic solution to decompose the wax and separate temporary sapphire substrate. The processed wafer was ground and polished down to 150 μm, and then the Ti/ Au metal for Si ohmic contact was deposited on the backside substrate. Finally, the wafer was diced to 300 × 350 μm^2 in this study. The completed MBRCLEDs sketch diagram was shown in figure 2.6.5. The chips were bonded to TO-46 cans for measurement.

2.4 Performances of 650 nm AlGaInP-based RCLEDs and MBRCLEDs

In this investigation, we designed three different light emission aperture sizes of 84, 60, and 40 μm which were shown in figure 2.7. The large aperture was designed for higher output power devices requirement and small aperture devices were applied for higher speed applications. These two fundamental devices properties are trade-off and the epi-structure should be optimized for different requirements. Figure 2.8 described the typical light-current-voltage (*L-I-V*) characteristics of RCLEDs with 84, 60, and 40 μm aperture sizes. The output power of 84, 60 and 40 μm device without epoxy encapsulated under 20 mA forward current operation were 3, 2 and 1.6 mW, respectively. From *I-V* curves, the devices series resistance were 8.4, 14.7, 27 ohm, respectively. Although the 40 μm device presents the lowest output power and the power saturate at lower driving current due to the high current density, the maximum power was 1.6 mW and still suitable to transmitting data through 50 m POF. Figure 2.9 shows the wall-plug efficiency and power characteristics of 84 μm devices. The wall-plug efficiency was as high as 12% and the output power could achieve over 3.5 mW at 20 mA with epoxy encapsulated. R. Wirth *et al.*, who had shown the output power and maximum wall-plug efficiency of 2.9 mW and 9.5% from the same 84 μm emission aperture size and 20 mA driving current and with epoxy [18]. The output power could be compared with to other groups which have even larger aperture size under the equal measurement conditions [14], [17]. In order to approach device temperature insensitive, properly detuning the wavelength between resonant cavity and quantum well is necessary. The output power variation versus detuning wavelength was shown in figure 2.10. The optimized wavelength detuning is 15 nm and the emission power droop from 20°C to 85°C is less than -2dB. P. Sipilä *et al*. who had shown the output power drop versus temperature is -3.8dB from 20°C to 85°C in 20 mA injection [17].

The detuning wavelength will also affect the far field pattern and coupling efficiency in POF applications, although POF has larger fiber core (1 mm) than glass optical fiber (GOF). This investigation was presented that the device with 15 nm detuning wavelength exhibited the far field pattern at 50% power angle of 134°. Figure 2.11 shows that the coupling efficiency into 0.5 NA POF of transmitter remained a high value (>50%) in wide driving current range (10 ~ 90 mA) due to the higher half power angle and output power. This coupling efficiency could be compared with M. Dumitrescu *et al.* [13] report under the same conditions of 0.5 NA POF and 84 μm devices, where their coupling efficiency was less than 35% from 0 mA to 40 mA operation current. Figure 2.12 shows the cut-off frequency -3dB (f_{-3dB}) of these three devices operated under 20 mA. It was demonstrated that the f_{-3dB} for aperture size of 84, 60 and 40 μm were 110.8, 228.6 and 313.3MHz, respectively. For standard POF-based communications, the 84 μm RCLEDs cut-off frequency over 110 MHz and the output power of 3.2 mW was demonstrated under 20 mA current injection. It was demonstrated that the 84 μm RCLEDs devices could achieve to the IEEE 1394b s200 standard. In addition, the devices rise and fall-time is 2.86 ns and 1.08 ns respectively using Hamamatsu Optical Oscilloscope C8188 test equipment. An open eye-diagram with error free was obtained at I_{bias}=30 mA. Since the f_{-3dB} of the 40 μm RCLEDs was 313MHz, the 40 μm devices could achieve IEEE 1394b s400 standard. The 40 μm RCLEDs eye diagram achieved 622 Mbit/s and shown in figure 2.13. In order to achieve high speed RCLEDs, RCLEDs epi-structure needs to modify. This carrier rate model in high speed RCLEDs has the following formula [19]:

$$\frac{\partial n}{\partial t} = -\left(\frac{n}{\tau}\right) - Bn^2 + \left(\frac{J_{inject}}{q \cdot d}\right), \qquad (2\text{-}6)$$

This is the dynamics of the electron carrier uniformly distributed in the active region of RCLEDs structure. Here the τ is the carrier lifetime, B is the electron-hole recombination

coefficient, J_{inject} is the injection current density, and d is the thickness of active layer. From this equation, there are several methods to modulation RCLEDs devices speed. Firstly, the carrier lifetime τ could be reduced by inserting some non-radiate recombine centers in the active region. But this method also decreased the internal efficiency of this structure, which is not desirable. The second way is that increases the current density of injection or decreases the size of emission window. However, these two ways will cause the power droop during higher forward current injection. The last method is reducing the active layer thickness, it could be increase the devices speed without sacrificing other performance. The cut-off frequency and output power of 84 μm RCLEDs devices with single QW were obtained to be 235 MHz and 2 mW at 20 mA, respectively. This performance was suitable for IEEE 1394b s400 standard applications. M.Guina *et al*. had also shown the data of bandwidth versus current, and its cut-off frequency of 84 μm devices is 125 MHz under 20 mA current operating [20]. In addition, an error free open eye diagram for the transceiver using single QW RCLEDs devices at I_{bias} = 30 mA was obtained to be 500 Mbit/s data rate through a graded-index POF over 50 m as shown in figure 2.14.

The high performances MBRCLEDs, having a high thermal conductivity Si substrate, were fabricated via twice bonding technique of glue bonding and metal bonding processes. In figure 2.15.1 shows the scanning electron microscope (SEM) photograph of the MBRCLEDs devices with 300 x 300 μm^2 dimensions. The figure 2.15.2 shows the MBRCLEDs electron-luminescence (EL) state and light intensity profile. The emission area diameter is 84 μm and the dark area of the emission window is metal mesh line for current spreading. In the RCLEDs devices applied requirements, the temperature insensitively properties is a key point. In order to approach the temperature insensitivity, proper detuning the wavelength between cavity and quantum well is necessary. In this study, both of the main epi-structure between RCLEDs and MBRCLEDs are the same and the optimum wavelength detuning is 15 nm.

Figure 2.16 shows the light-current (*L-I*) curves of the MBRCLEDs and the RCLEDs were operated at room temperature (RT), 60°C, and 100°C ambiance. It is observed that the output power of MBRCLEDs decay were less than the RCLEDs. From RT to 100°C ambiance, the output power drop of MBRCLEDs was -0.31, -1.78, and -2.5 dB under 20, 50 and 70 mA current injection respectively. In addition, the output power droop of the RCLEDs were -1.75, -3.03, -5.47 dB during 20, 50, and 70mA current injection respectively. The wall-plug efficiency of the RCLEDs and the MBRCLEDs under room temperature operations were shown in figure 2.17. The maximum wall-plug efficiency of MBRCLEDs was 13.7% under 2.5 mA current injection. In addition, the wall-plug efficiency difference ($\Delta_{efficiency}$) between the MBRCLEDs and the RCLEDs under 20 and 70mA current operating were 1.2% and 1.9%, respectively. Since the thermal conductivity of GaAs is poor than Si substrate, the self-heating effect is relatively obvious in the RCLEDs especially. The phenomenon indicates that although the structure had been optimized detuning wavelength but the self-heating still needs a thermal conductivity path to release especially for high current injection. In junction temperature (*Tj*) measurement, a pulsed generator (KEITHLEY Model 2520) was used to obtain V_f variations in different current injection conditions with a short pulses time of 0.8 μsec. The junction temperature variations (ΔT_j) versus forward voltage of the MBRCLEDs and the RCLEDs under pulsed current operation at room temperature was shown in figure 2.18. It is significantly observed that the junction temperature of the RCLEDs is higher than the MBRCLEDs, the caused of this result is higher thermal resistance of the GaAs material than Si.

The RCLEDs performances will be degenerated with increasing temperature form internal device, and lower internal quantum efficiency was induced due to the more leakage current and non-radiative recombination. This serious leakage current in AlGaInP/ GaInP material is mainly attributed to the relatively low conduction band offset value. In the

MBRCLEDs fabrication processes, the epi-structure would undergo twice bonding processes, which could be damage the thin epi-layers. The above results were demonstrated clearly that the twice wafer bonding processes have not affected the epi-structure. Following, the MBRCLEDs far-field patterns versus different temperature ambiance operating were shown in figure 2.19. The MBRCLEDs were measured under 20 mA and without encapsulating epoxy. The 50% power angle (half-center brightness or 50% of the full luminosity) of the MBRCLEDs under RT and 80ºC is 134º and 126º, respectively. The cause of this result is wavelength detuning between quantum-well and DBR resonance. This special wavelength detuning (15nm) will affect the radiation pattern pass into rabbit ear and reduce the devices temperature sensitively. From figure 2.19 results, the 50% power angle offset is only 8º under RT to 80ºC ambiance operating due to the MBRCLEDs with a better thermal conductivity substrate. Figure 2.20 shows the life-time of the MBRCLEDs and the RCLEDs under a condition of 85°C and 20 mA driving current. Both of the power reliability decay ratio were less than 30% but the MBRCLEDs had a better reliability result due to an excellent thermal conductivity substrate. In figure 2.21 shows the eye diagram measurements were performed to estimate the ability of the MBRCLEDs for high-speed data communication under a condition of devices were operated in 200MHz and 20mA driving current. Eye diagrams at RT and 80ºC have a clear pattern and similar open eye diagram. As above-mentioned performances, the MBRCLEDs are more suitable for working in high temperature ambiance than the RCLEDs such as mobile components, industrial sensor and high-speed data rate transmission applications.

2.5 Summary

In conventional GaAs substrate RCLEDs device summary, AlGaInP-based RCLEDs with high power and high speed were demonstrated. In this investigation, the RCLEDs were designed with different light-output aperture sizes 84, 60, and 40 μm, for different applications of plastic optical fibers. The 40 μm aperture RCLEDs could be achieved that the small-signal modulation bandwidths as high as 310 MHz at a forward current of 20 mA and the output power as high as 1.5 mW. The devices with 84 μm apertures had an output power of more than 3.5 mW at a driving current of 20 mA and a maximum efficiency of over 12 % with an epoxy-encapsulated package. The devices with 40 μm apertures satisfied with the IEEE 1394b s400 standard. Furthermore, the devices showed stable coupling efficiency for various currents and output powers at different ambience temperatures. In addition, the lifetime of devices is over 1300 h, and the power decay is less than 0.5 dB at 85°C for a 40 mA driving current.

Furthermore, we had developed the novel MBRCLEDs devices, having high performances and replacing conventional GaAs substrate with a high thermal conductivity of Si substrate. In 650 nm MBRCLEDs summary, MBRCLEDs has high performances, high temperature insensitively, and high reliability have been successfully fabricated on Si substrates by twice wafer bonding techniques. Although the RCLEDs epi-structure was optimum designed for detuning wavelength, devices are still insufficient for high current injection or high temperature operating. However, MBRCLEDs were based on this structure and using metal bonding technique could improve devices performances especially in high temperature ambiance. The junction temperature variations of the MBRCLEDs were relatively smaller as compared with the RCLEDs. The MBRCLEDs with 84 μm apertures provided high wall-plug efficiency of 13.7 % and a smaller power drooped of -0.31dB from RT to 100ºC due to the better heat dispersion substrate. Furthermore, the stable beam profile,

high reliability over 1000 hours and clearly eye diagram in high temperature operation. These excellent performances of the MBRCLEDs devices should be suitable for high temperature ambiance, high current injection and high data communication applications.

REFERENCE

[1] R. J. Ram, D. I. Babić, R. A. York, and J. E. Bowers, “Spontaneous emission in micro-cavities with distributed mirrors”, *IEEE J. Quantum Electron.*, Vol.31, pp. 399, 1995.

[2] Y.-K. Song, Compound Semiconductor, Vol.6, pp. 53, 2000.

[3] N. E. J. Hunt, E. F. Schubert, R. A. Logan, and G. J. Zydzik, “Extremely narrow spectral widths from resonant cavity light-emitting diodes (RCLEDs) suitable for wavelength-division multiplexing at 1.3 μm and 1.5μm”. *1992 International Electron Devices Meeting (IEDM)* San Francisco, CA, Dec. pp.13-16, 1992.

[4] E. F. Schubert, Y. H. Wang, A. Y. Cho, L. W. Tu, G. J. Zydzik, “Resonant Cavity Light-Emitting Diode”, *Appl. Phys. Lett.*, Vol. 60, pp.921-923, 1992.

[5] E. F. Schubert, N. E. J. Hunt, R. J. Malik, M. Micovic, and D. L. Miller, “Temperature and modulation characteristics of resonant-cavity light-emitting diodes”, *J. Lightwave Technol.*, vol. 14, no. 7, pp. 1721–1728, 1996.

[6] H. De Neve, J. Blondelle, P. Van Daele, P. Demeester, R. Baets, G. Borghs, “Recycling of guided mode light emission in planar microcavity light emitting diodes”, *Appl. Phys. Lett.*, Vol. 70, pp.799-801, 1997.

[7] E. F. Schubert, N. E. J. Hunt, M. Micovic, R. J. Malik, D. L. Sivco, A.Y. Cho, and G. J. Zydzik, “Highly efficient light-emitting diodes with microcavities”, *Science*, Vol. 265, pp.943, 1994.

[8] S. W. Chiou, Y. C. Lee, C. S. Chang, and T. P. Chen, “High-speed red RCLEDs and VCSELs for plastic optical fiber application”, *Proceedings of SPIE*, 5739, pp.129, 2005.

[9] J. F. Carlin, P. Royo, R. P. Stanley, R. Houdre, J. Spicher, U. Oesterle and M. Ilegems, “Design and characterization of top-emitting microcavity light-emitting diodes”,

Semicond. Sci. Technol., Vol.15, pp. 145, 2000.

[10] R. Wirth, C. Karnutsch, S. Kugler, W. Plass, W. Huber, E. Baur and K. Streubel: *Proc. POF2001*, pp. 65, 2001.

[11] H. Benisty, H. De Neve, and C. Weisbuch, "Impact of planar microcavity effects on light extraction-Part I: Basic concepts and analytical trends", *IEEE J. Quantum Electron.*, Vol. 34, pp. 1612, 1998.

[12] R. Wirth, C. Karnutsch, S. Kugler, S. Thaler, and K. Streubel, "Red and Orange Resonant-Cavity LEDs", *Proceedings of SPIE*, 4278, pp.43, 2001.

[13] M. M. Dumitrescu, M. J. Saarinen, M. D. Guina, and M. V. Pessa, "High-speed resonant cavity light-emitting diodes at 650 nm," *IEEE J. Selected Topics in Quantum Electron*, Vol. 8, pp. 219-224, 2002.

[14] K. Streubel, N. Linder, R. Wirth, and A. Jaeger, "High brightness AlGaInP light-emitting diodes," *IEEE J. Select. Topics Quantum Electronics*, Vol.8, pp. 321-332, 2002.

[15] S. W. Chiou, Y. C. Lee, C. S. Chang, and T. P. Cheng, "High speed red RCLEDs and VCSELs for plastic optical fiber application," *SPIE Proc.*, Vol. 5739, pp. 129–133, 2005.

[16] M.-F. Huang, M.-L. Tsai, J.-Y. Shin, Y.-L. Sun, R.-M. Yang, and Y.-K. Kuo, "Optimization of active layer structures to minimize leakage current for an AlGaInP laser diode," *Appl. Phys. A*, Vol. 81, no. 7, pp. 1369–1373, 2005.

[17] P. Sipilä, M. Saarinen, M. Guina, V. Vilokkinen, M. Toivoneen, and M. Pessa, "Temperature behaviour of resonant cavity light-emitting diodes at 650 nm," *Semicond. Sci. Technol.*, Vol. 15, pp. 418–421, 2000.

[18] R. Wirth, C. Karnutsch, S. Kugler, and K. Streubel, "High efficiency resonant cavity LED's emitting at 650 nm", *IEEE Photonic Technol. Lett.*, Vol. 13, p. 421, 2001.

[19] P. Bienstman, R. Bockstaele and R. Baets: "Resonant-cavity light-emitting diode based

parallel Interconnections”, Chapter. 4, p.123, 2000.

[20] M. Guina, S. Orsila, M. Dumitrescu, M. Saarinen, P. Sipilä, V. Vilokkinen, B. Roycroft, P. Uusimaa, M. Toivonen, and M. Pessa, “Light-emitting diode emitting at 650 nm with 200-MHz small-signal modulation bandwidth,” *IEEE Photon. Technol. Lett.*, vol. 12, no. 7, pp. 786–788, Jul. 2000.

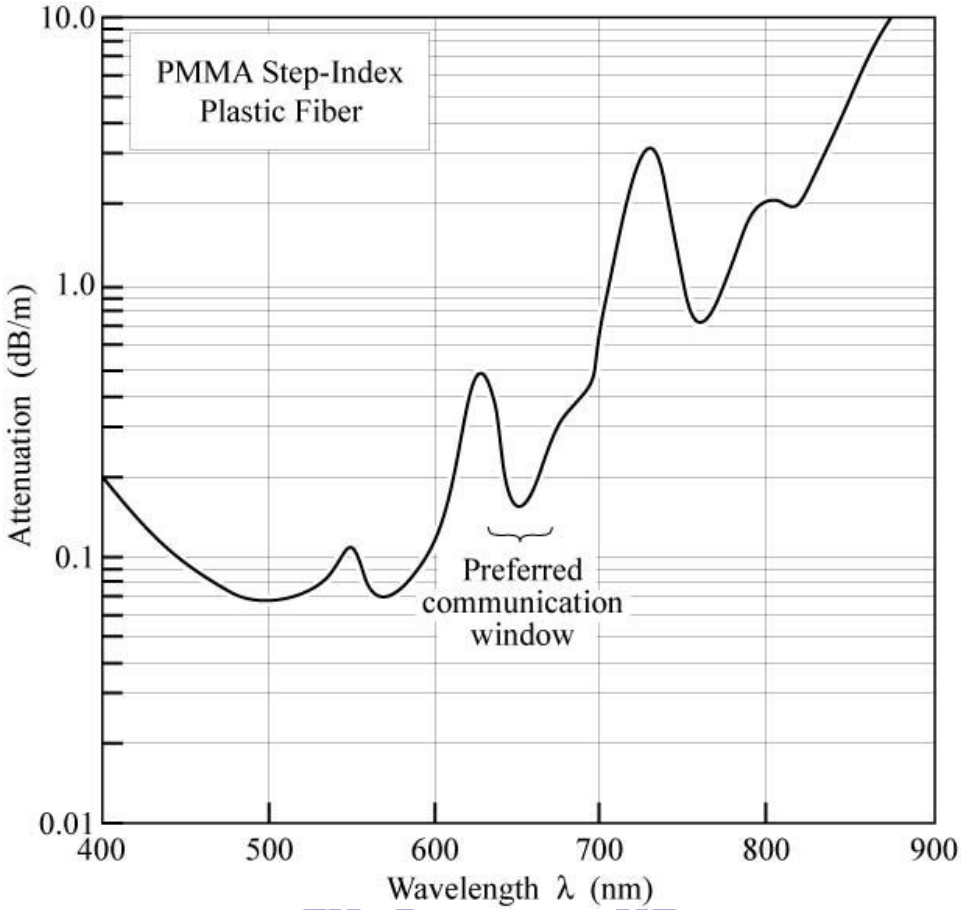


Figure 2.1: Attenuation of a PMMA step-index plastic optical fiber.

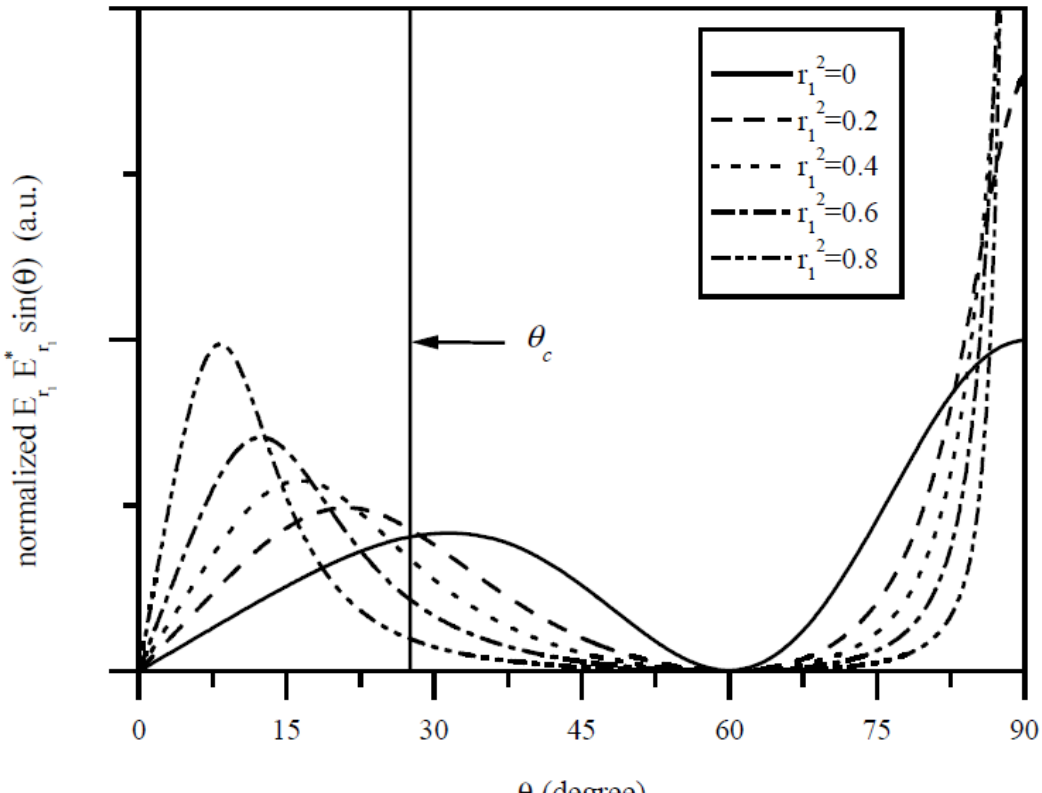


Figure 2.2: Intensity of the optical mode at the top mirror for an m=1 cavity. While the reflectivity of the bottom DBRs was r_2^2=1, the reflectivity r_1 of the top DBRs was varied.

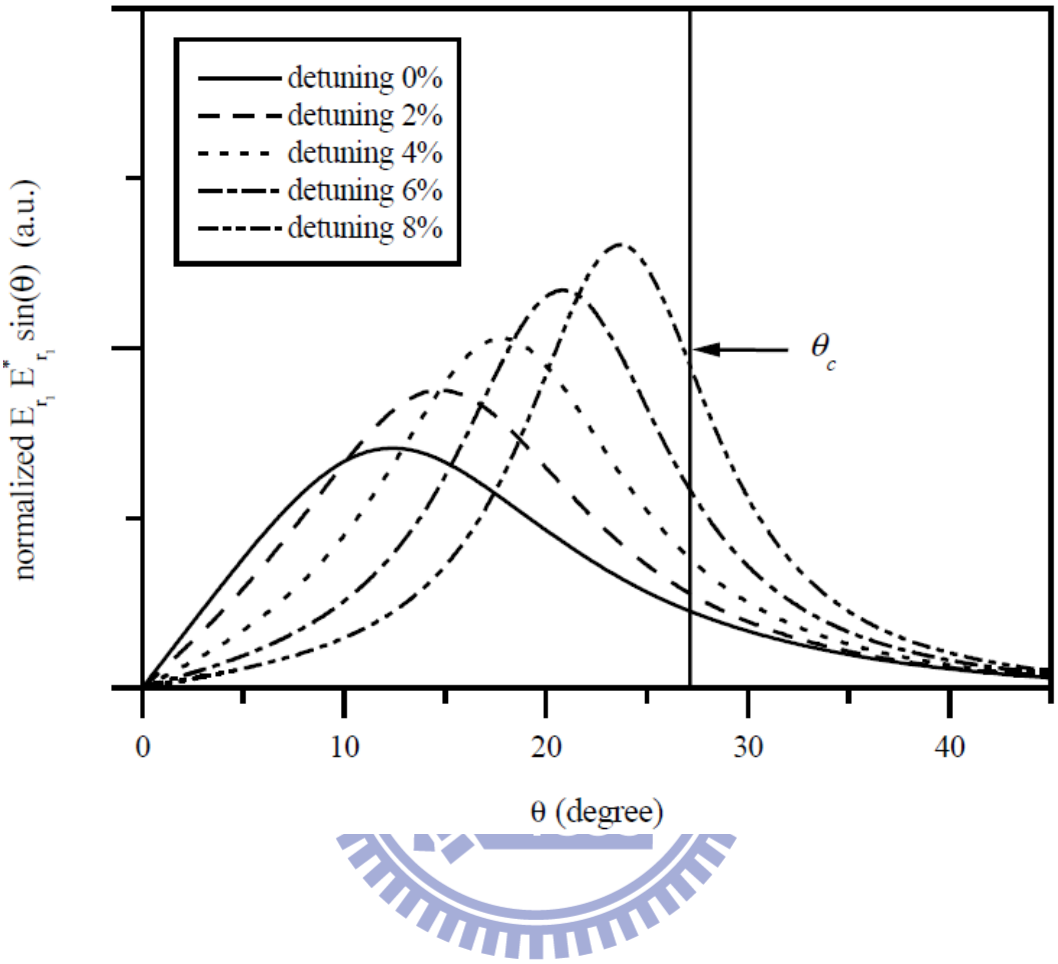


Figure 2.3: Intensity of the optical mode at the top mirror for an m=1 cavity for various detuning *d*. The reflectivity of the top DBRs was r_1^2=0.6 and the bottom DBRs was r_2^2=1.

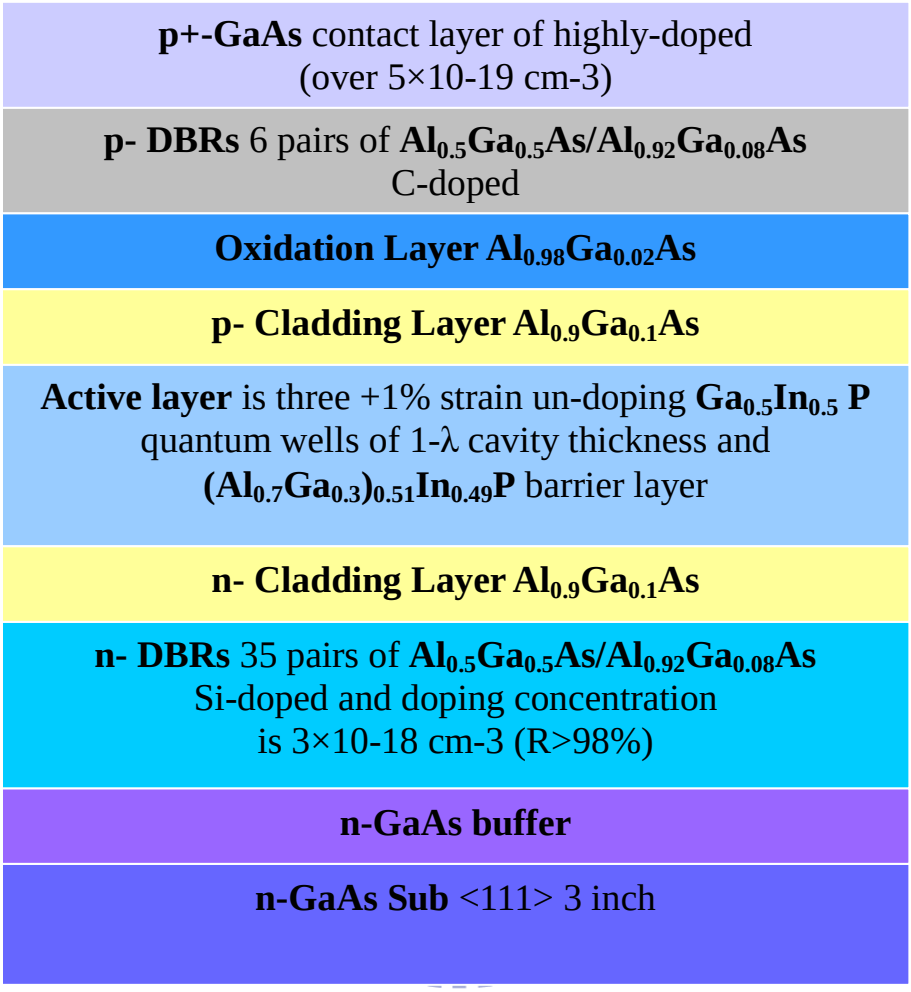
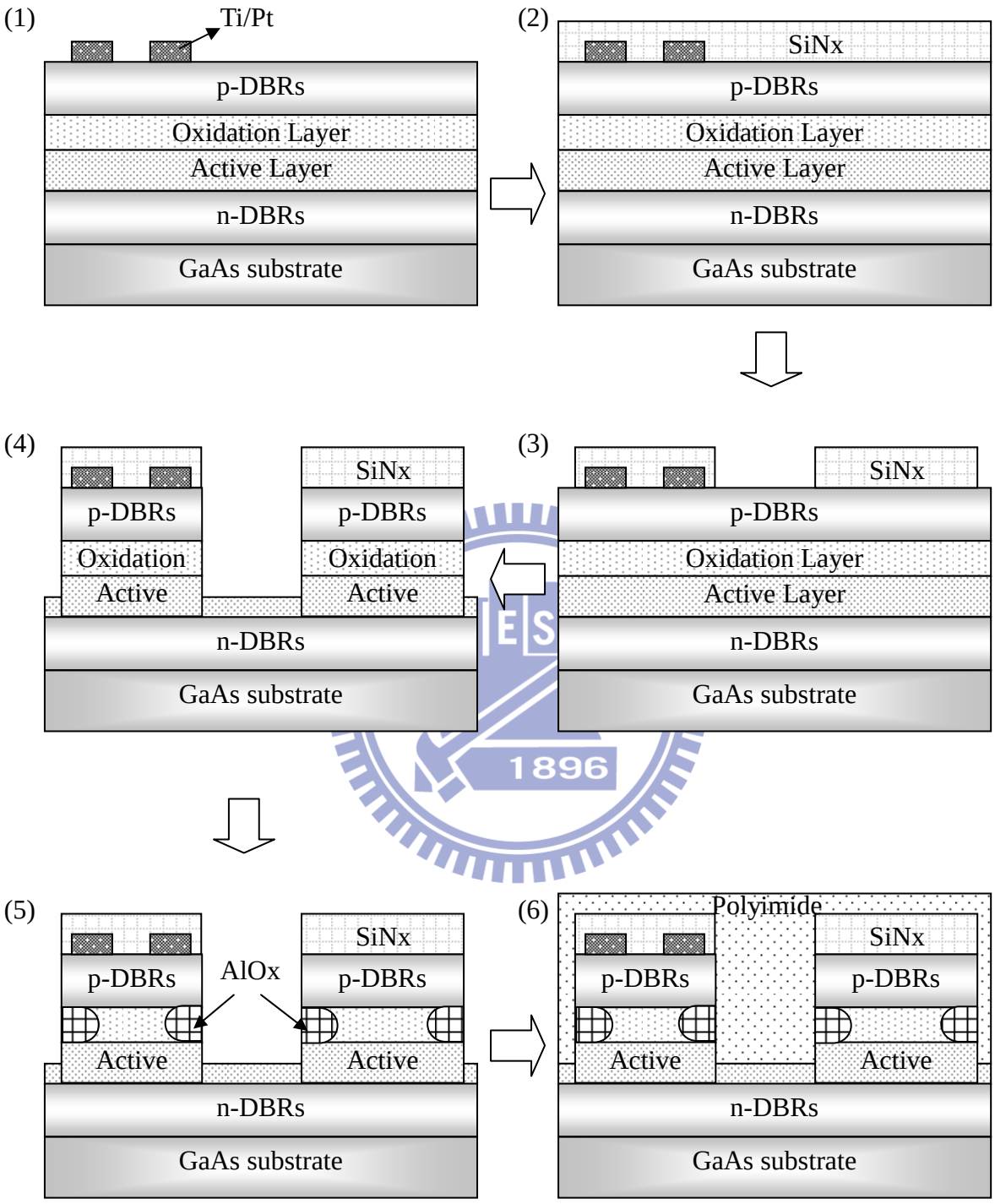


Figure 2.4: The 650nm AlGaInP-based RCLEDs epi-structure.


(1)
Ti/Pt
p-DBRs
Oxidation Layer
Active Layer
n-DBRs
GaAs substrate
(2)
SiNx
p-DBRs
Oxidation Layer
Active Layer
n-DBRs
GaAs substrate
(3)
SiNx
p-DBRs
Oxidation Layer
Active Layer
n-DBRs
GaAs substrate
(4)
SiNx
p-DBRs
p-DBRs
Oxidation
Oxidation
Active
Active
n-DBRs
GaAs substrate
(5)
SiNx
p-DBRs
AlOx
p-DBRs
Active
Active
n-DBRs
GaAs substrate
(6)
Polyimide
SiNx
p-DBRs
p-DBRs
Active
Active
n-DBRs
GaAs substrate

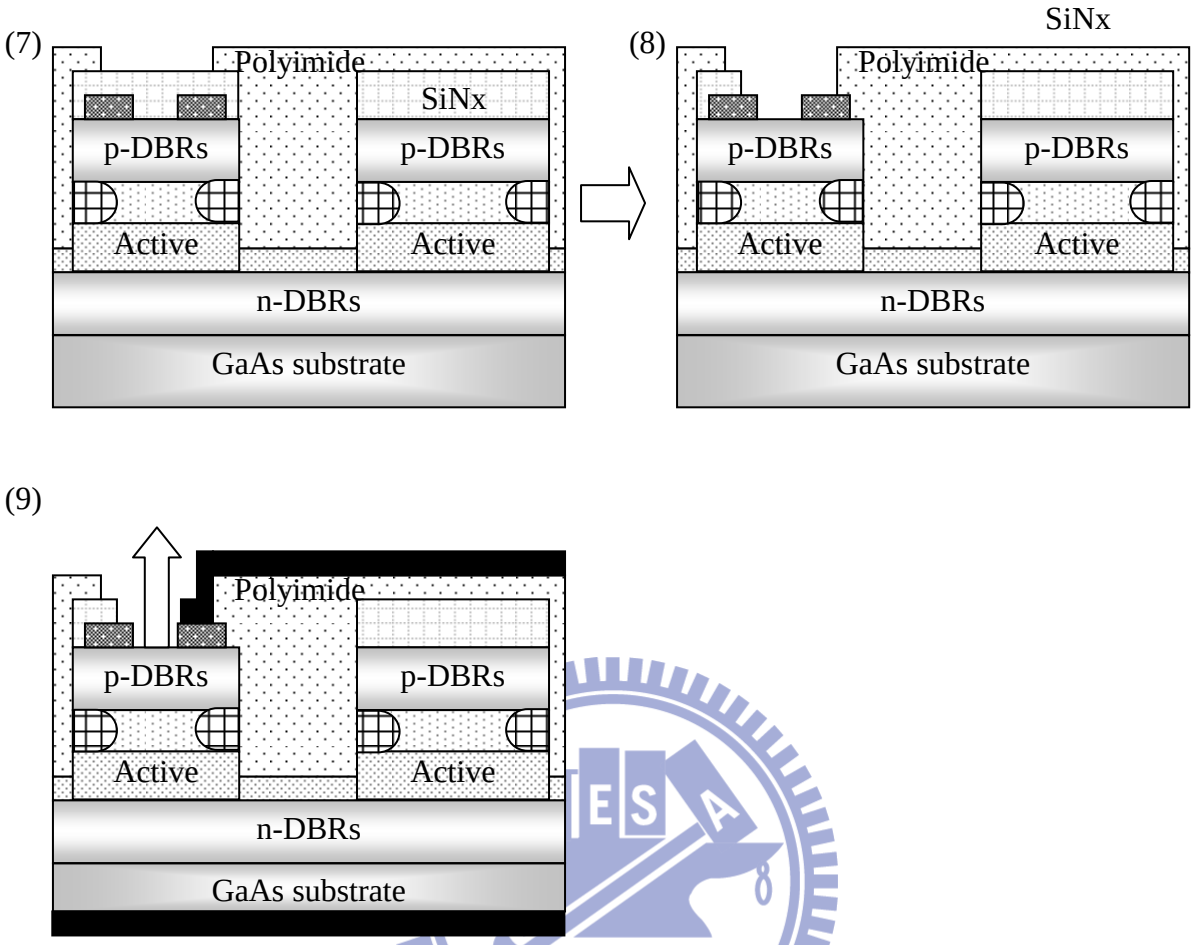


Figure 2.5: Schematic fabrication processes of RCLEDs devices: (1) The Ti/Pt for p-ohmic contact ring were deposited on p^{+}-GaAs cap. (2) A thick SiN_x about 1 μm was grown on wafer surface for mesa dry etching and protection steam during oxidation process. (3) The circular mesa size of 130 μm was defined using standard photolithography and a chemical etchant. (4) Using ICP etcher for dry-etching until the active layer was exposed. (5) A high resistivity region of AlO_x material was formed through the oxidation process. (6) The thick polyimide was coated on surface for planarization device structure. (7) The polyimide final pattern after curing process. (8) SiNx film was removed for metal line connection. (9) Deposited Ti/ Pt /Au for p-electrode pad and Au/ Ge for n-ohmic contact.

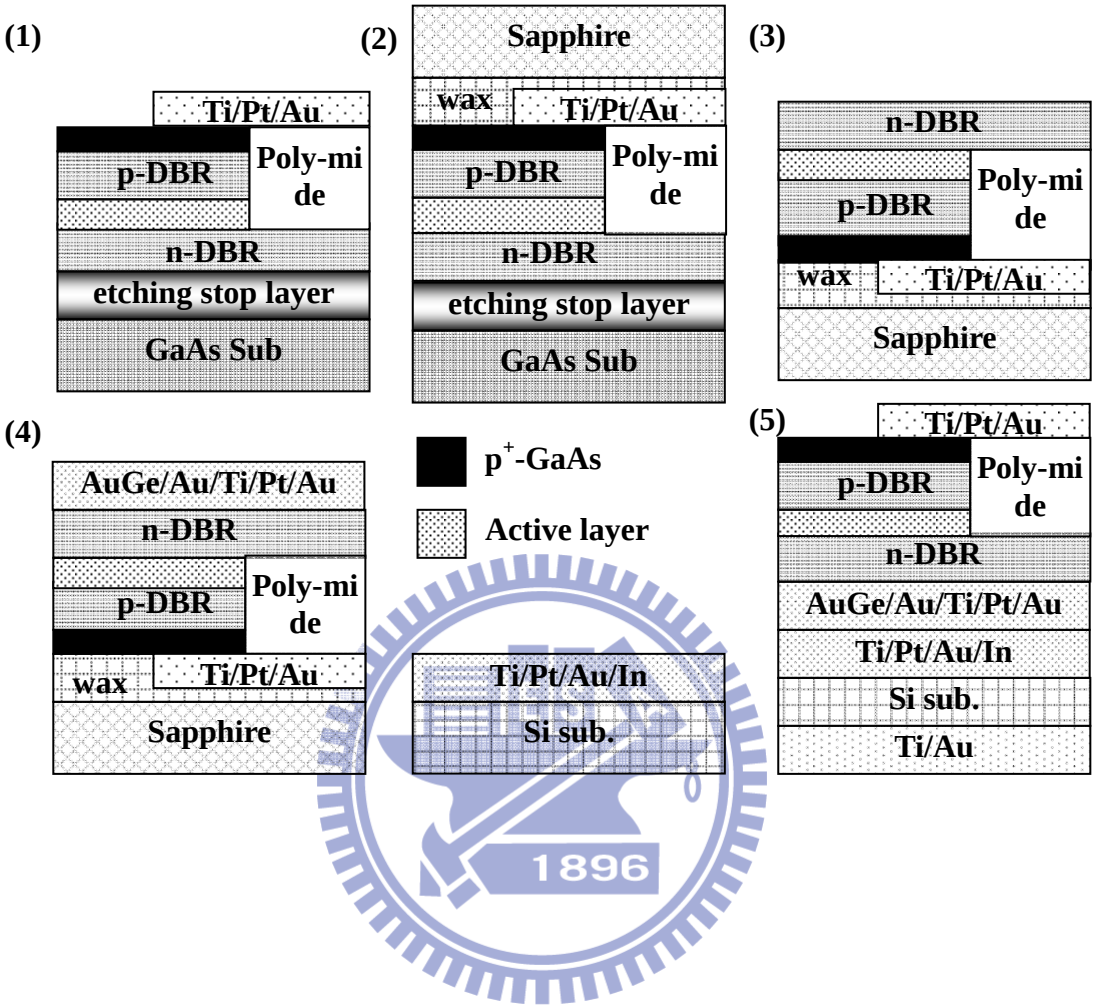


Figure 2.6: Schematic diagram of MBRCLEDs fabrication: (1) The conventional RCLEDs structure. (2) The epi-wafer was temporarily bonded to a sapphire substrate using wax in vacuum ambient. (3) The GaAs substrate and etching stop layer was removed by chemical etching. (4) Bonding metal was deposited on Si and epi-layer surface. (5) The MBRCLEDs process was completed.

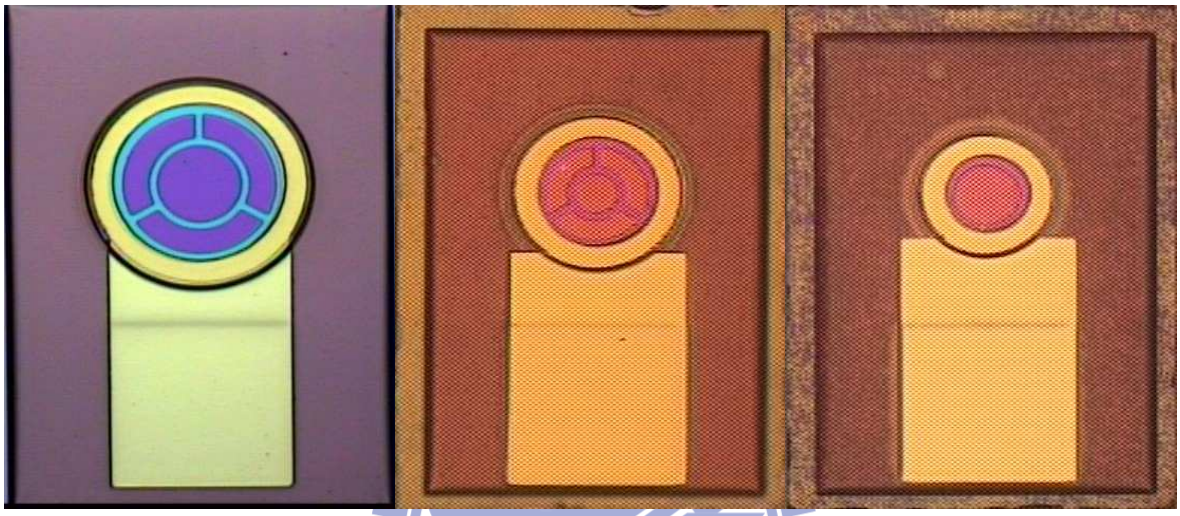


Figure 2.7: The OM figures of three different light emission window sizes of 84, 60 and 40 μm.

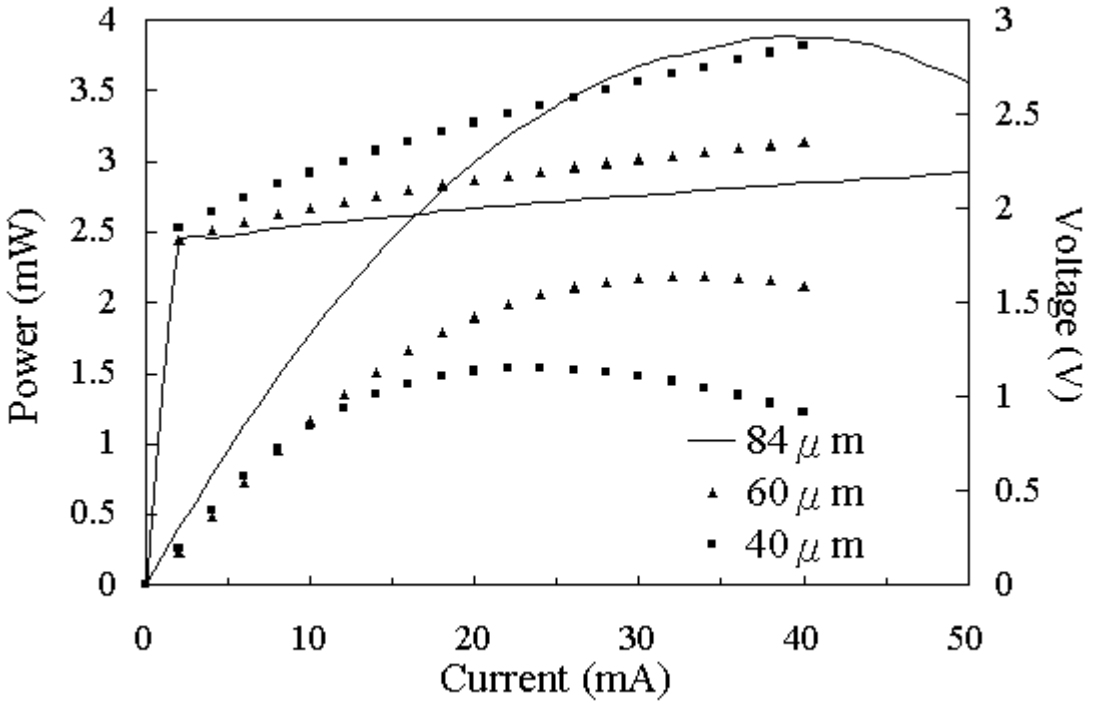


Figure 2.8: The typical light intensity-current-voltage (L-I-V) characteristics of 84, 60, and 40 μm aperture size RCLEDs.

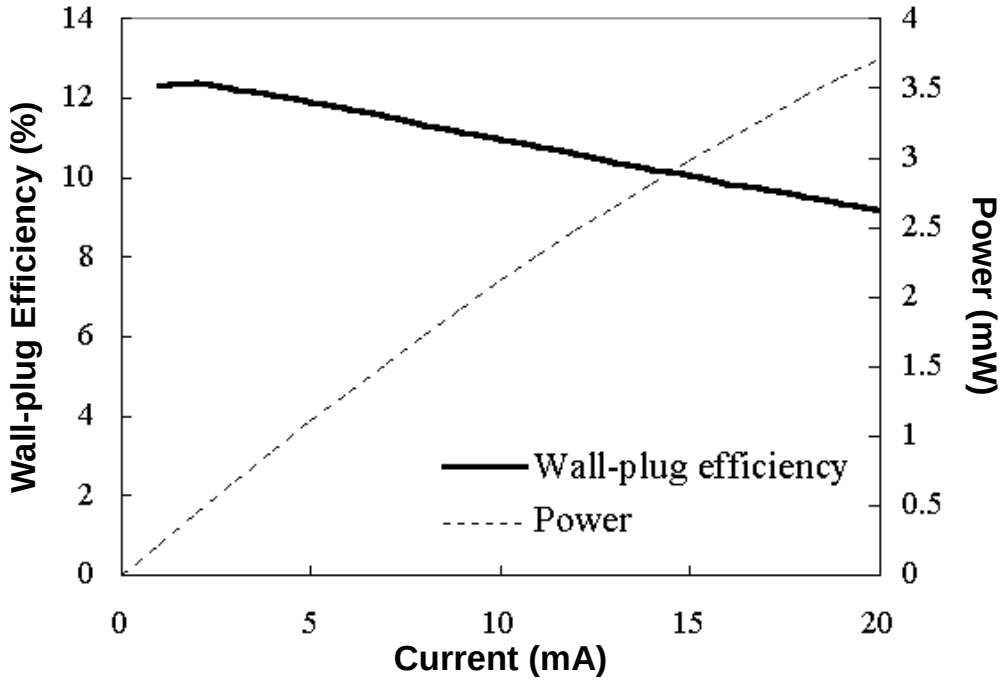


Figure 2.9: The wall-plug efficiency and output power characteristics of 84 μm devices with epoxy encapsulated.

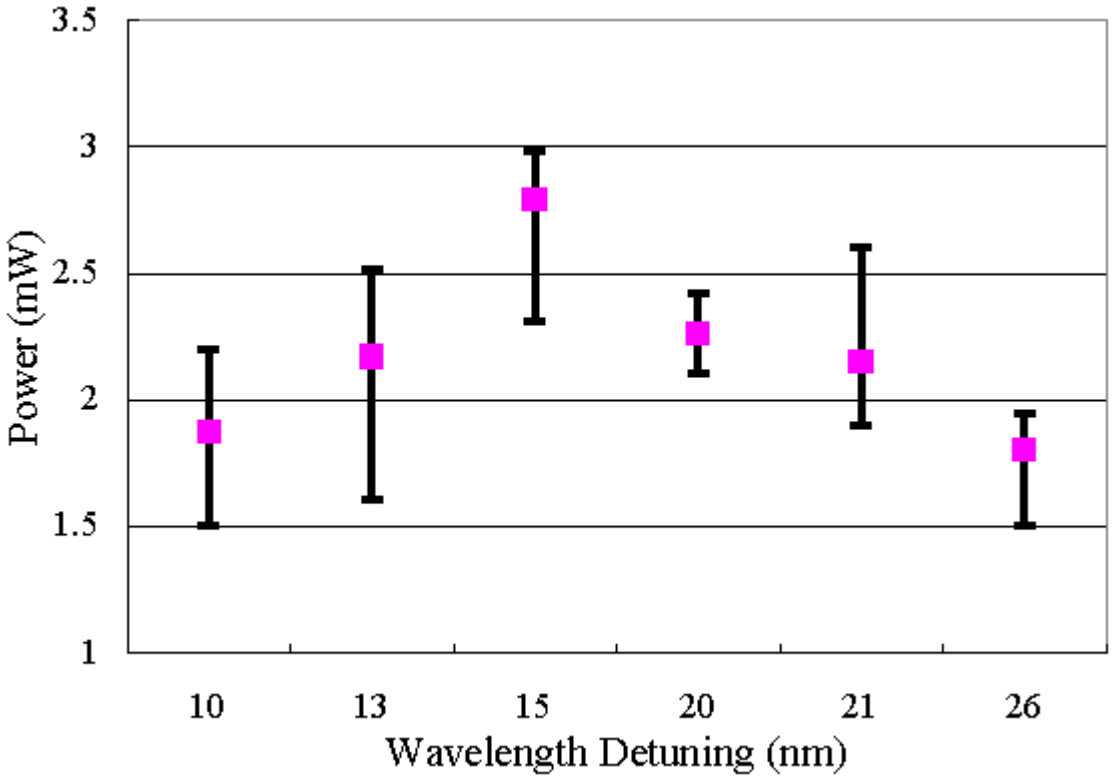


Figure 2.10: The output power variation versus detuning wavelength.

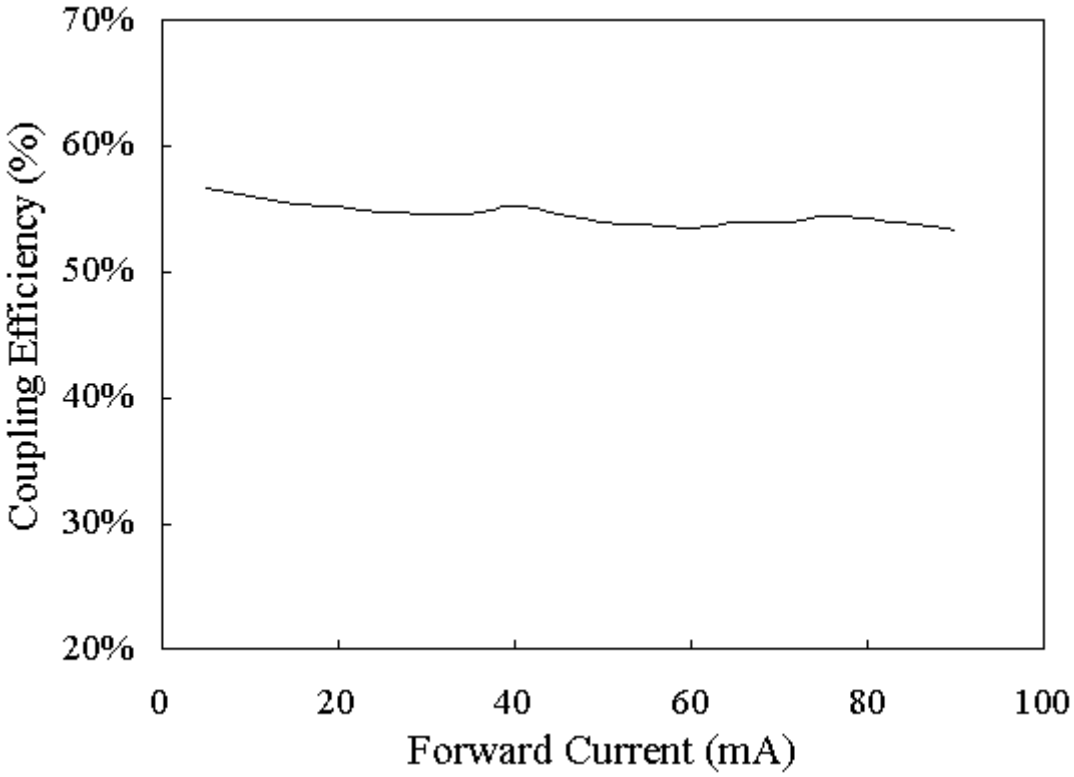


Figure 2.11: The coupling efficiency versus wide driving current into 0.5NA POF.

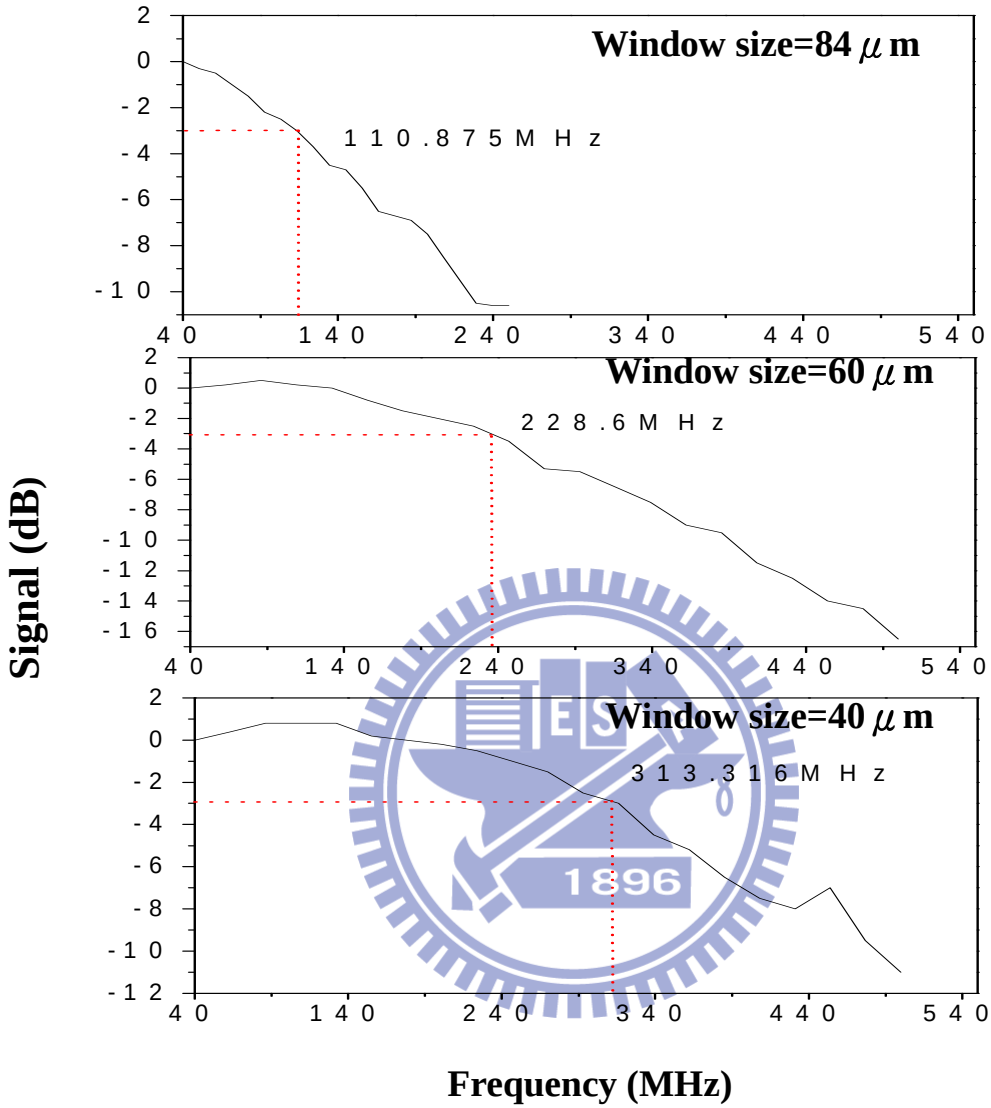


Figure 2.12: The cut-off frequency -3dB (f_{-3dB}) of these three different devices operated at 20 mA.

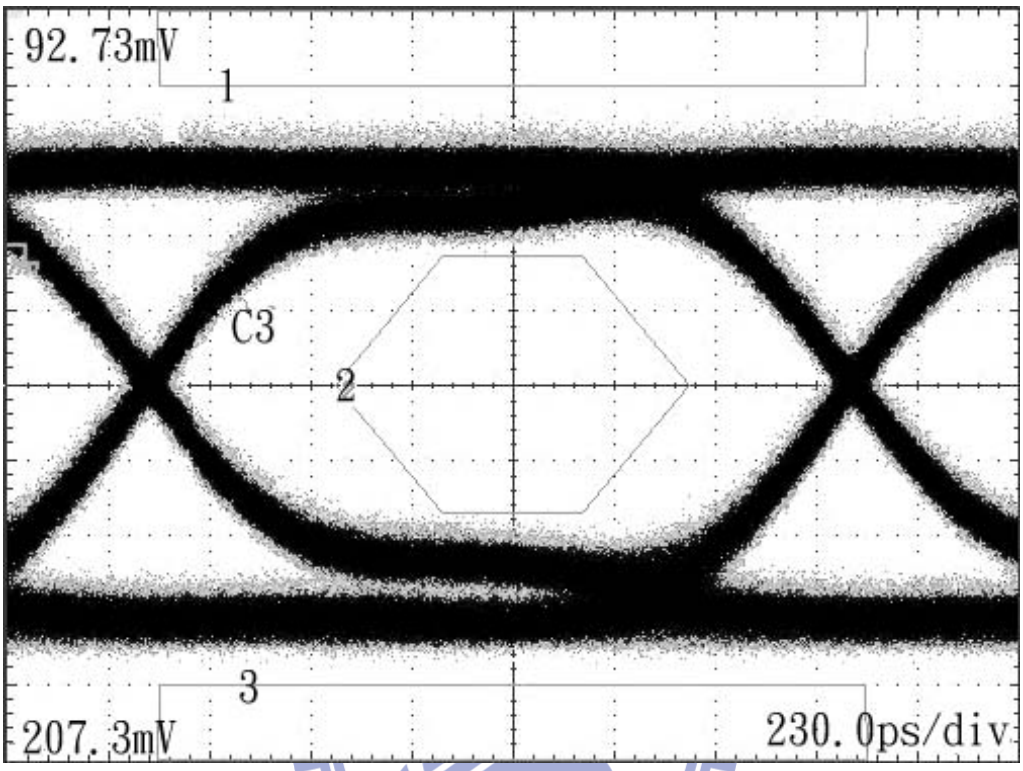


Figure 2.13: The eye diagram of 40 μm RCLEDs could achieve 622 Mbit/s.

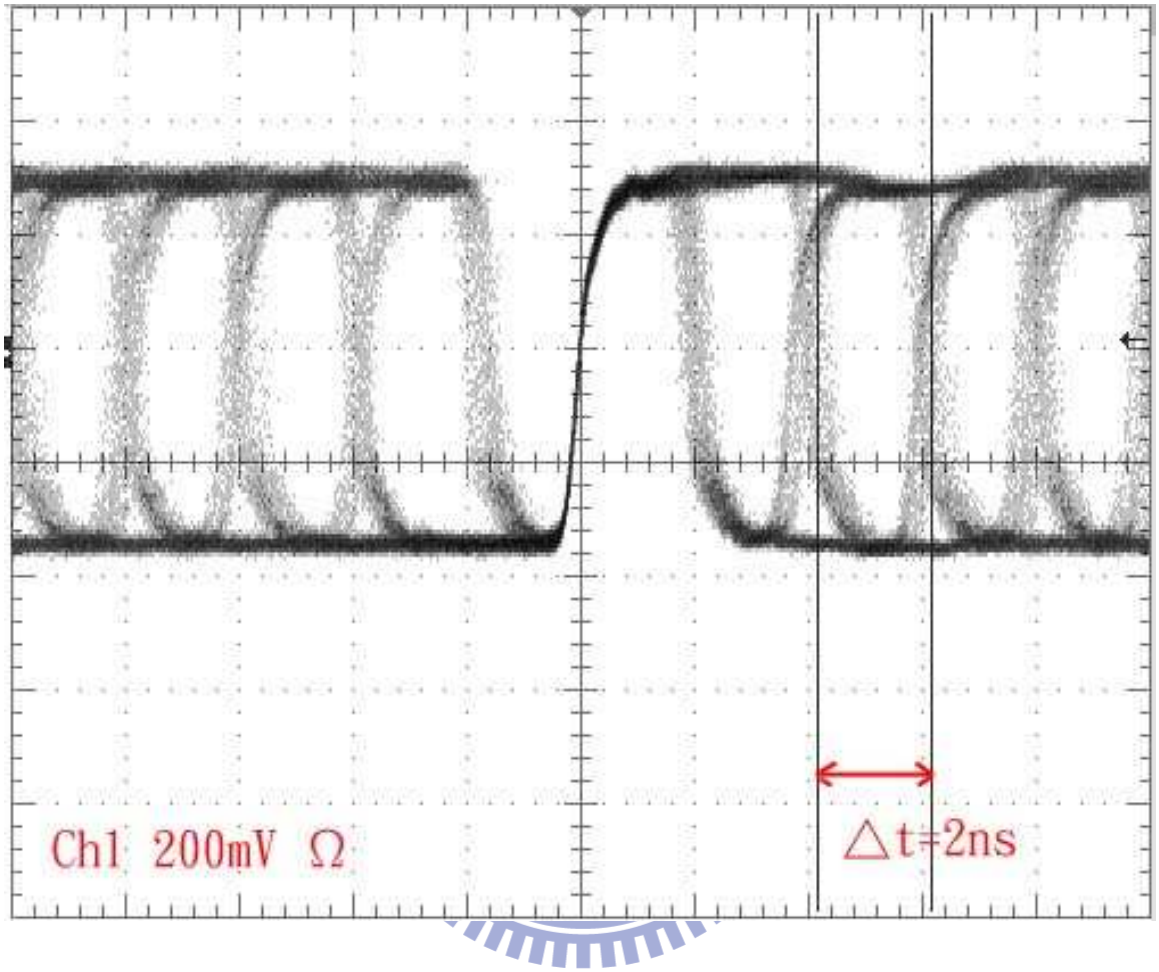
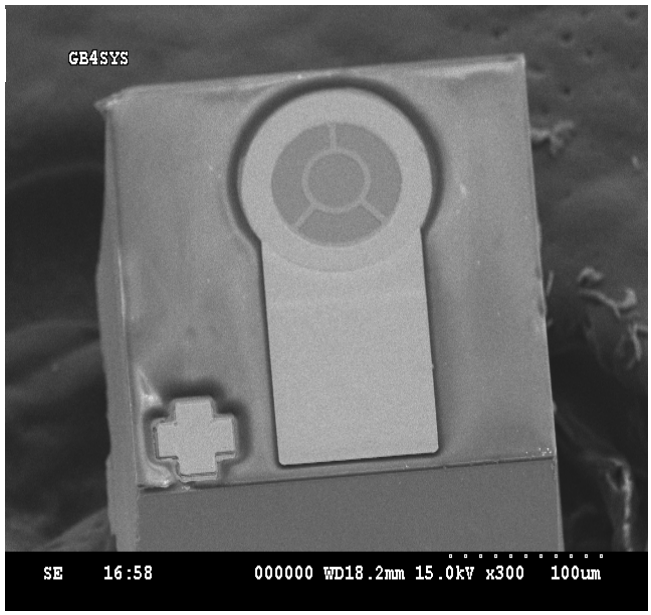


Figure 2.14: The eye diagram for the transceiver using RCLEDs devices with single QW transmitting 500 Mbit/s data rate through graded-index POF over 50 m.

(1)



(2)

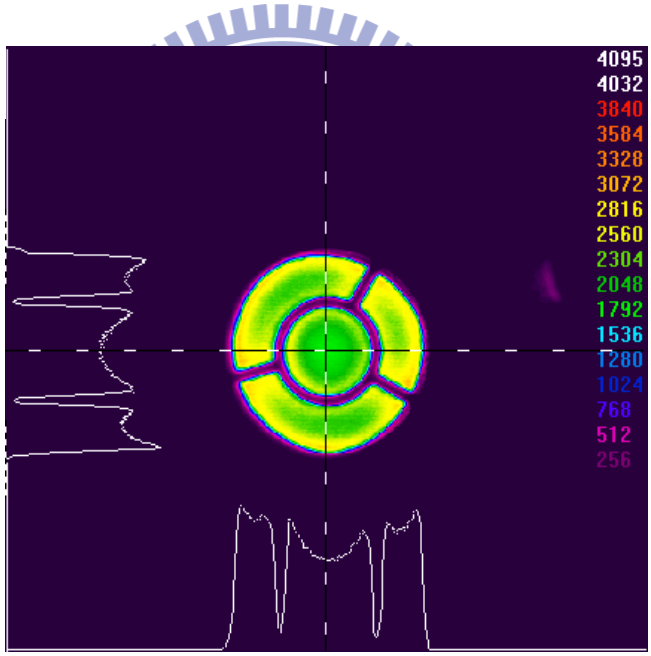


Figure 2.15: (1) The SEM figure of the MBRCLEDs chip profile. (2) The MBRCLEDs device EL state and light intensity distribution under 20 mA current injection.

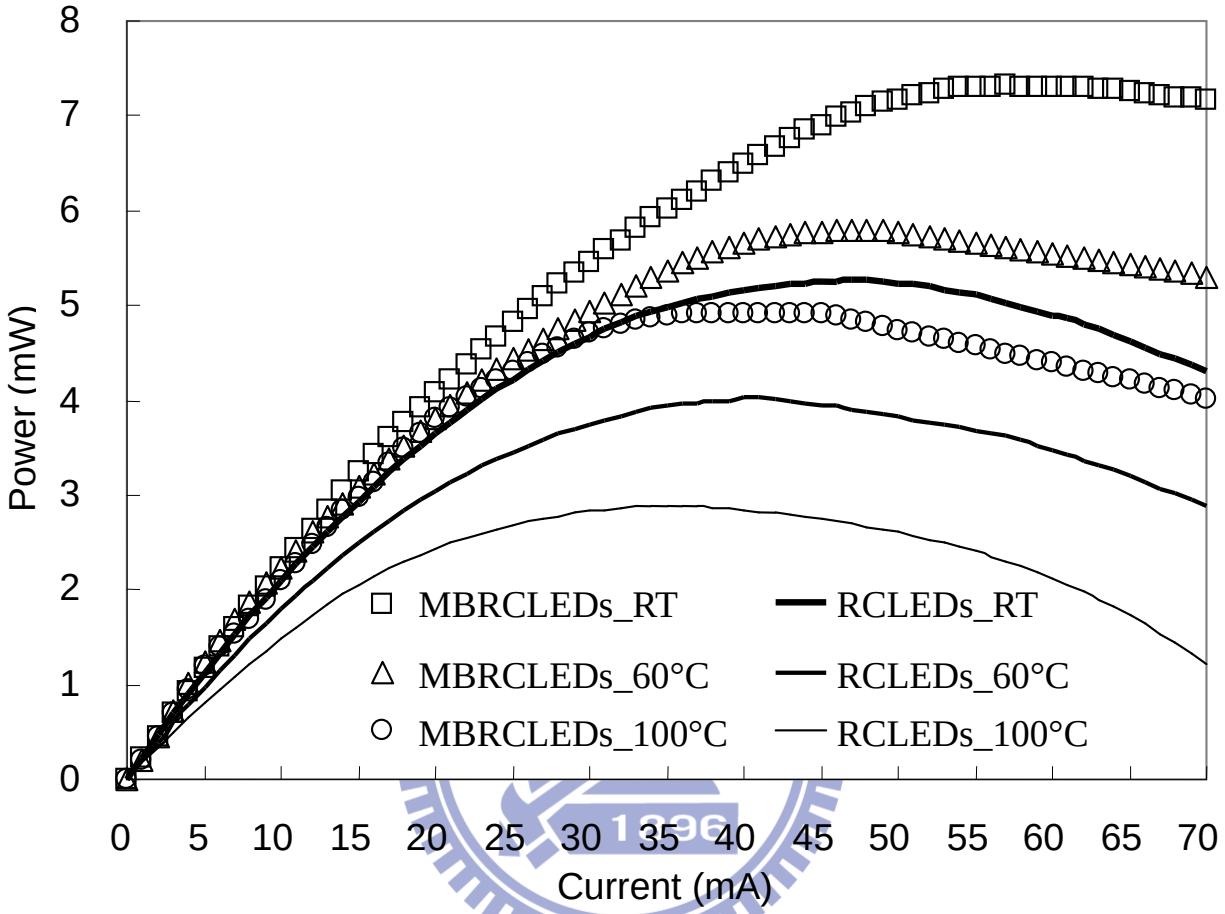


Figure 2.16: The typical intensity-current (L-I) characteristics of the MBRCLEDs and the RCLEDs versus temperature variations.

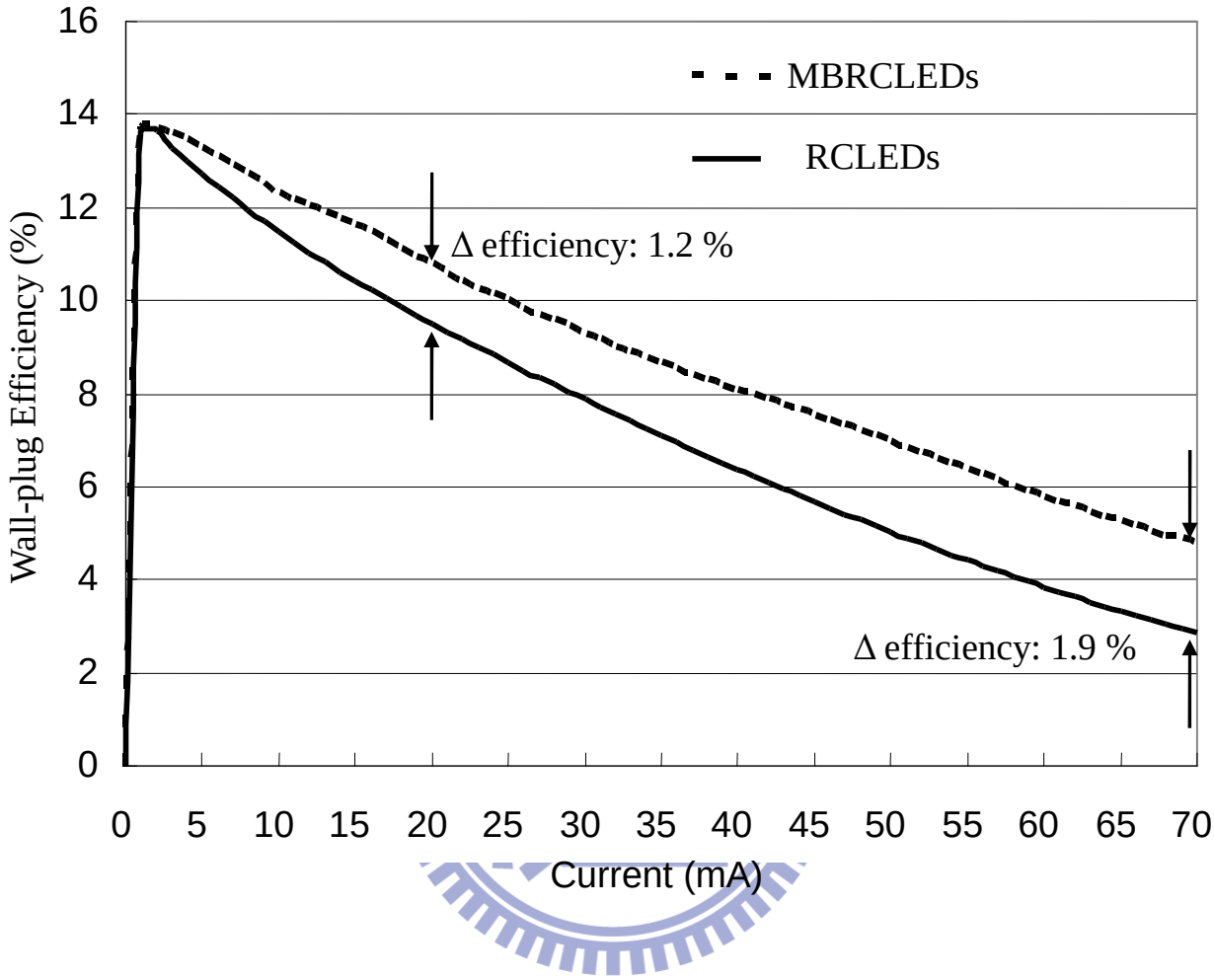


Figure 2.17: The wall plug efficiency as a function of injection current for the MBRCLEDs and the RCLEDs at RT.

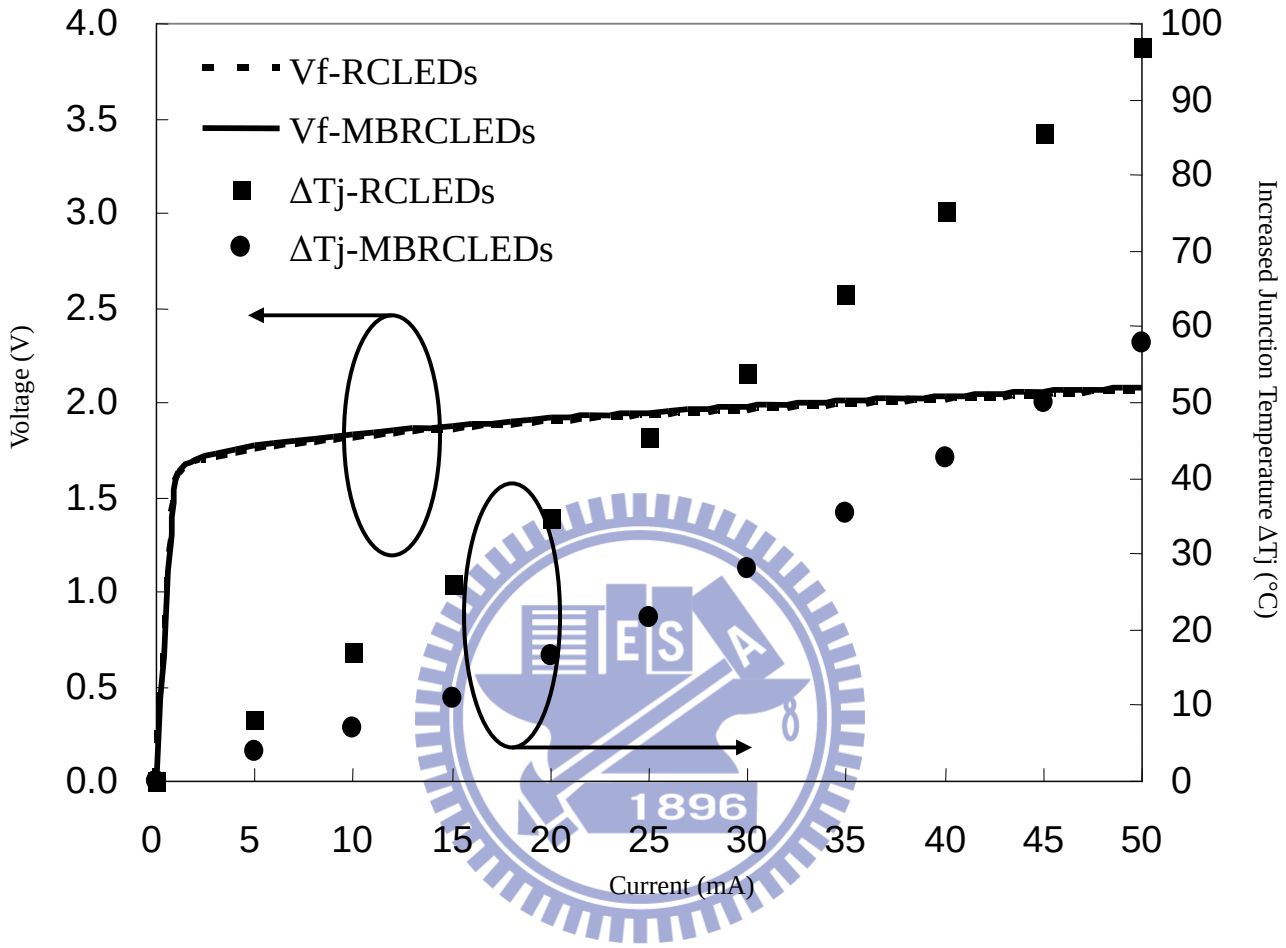


Figure 2.18: The Junction temperature increase (ΔT_j) and forward voltage (V_f) as a function of the injection current for MBRCLEDs and conventional RCLEDs at room temperature.

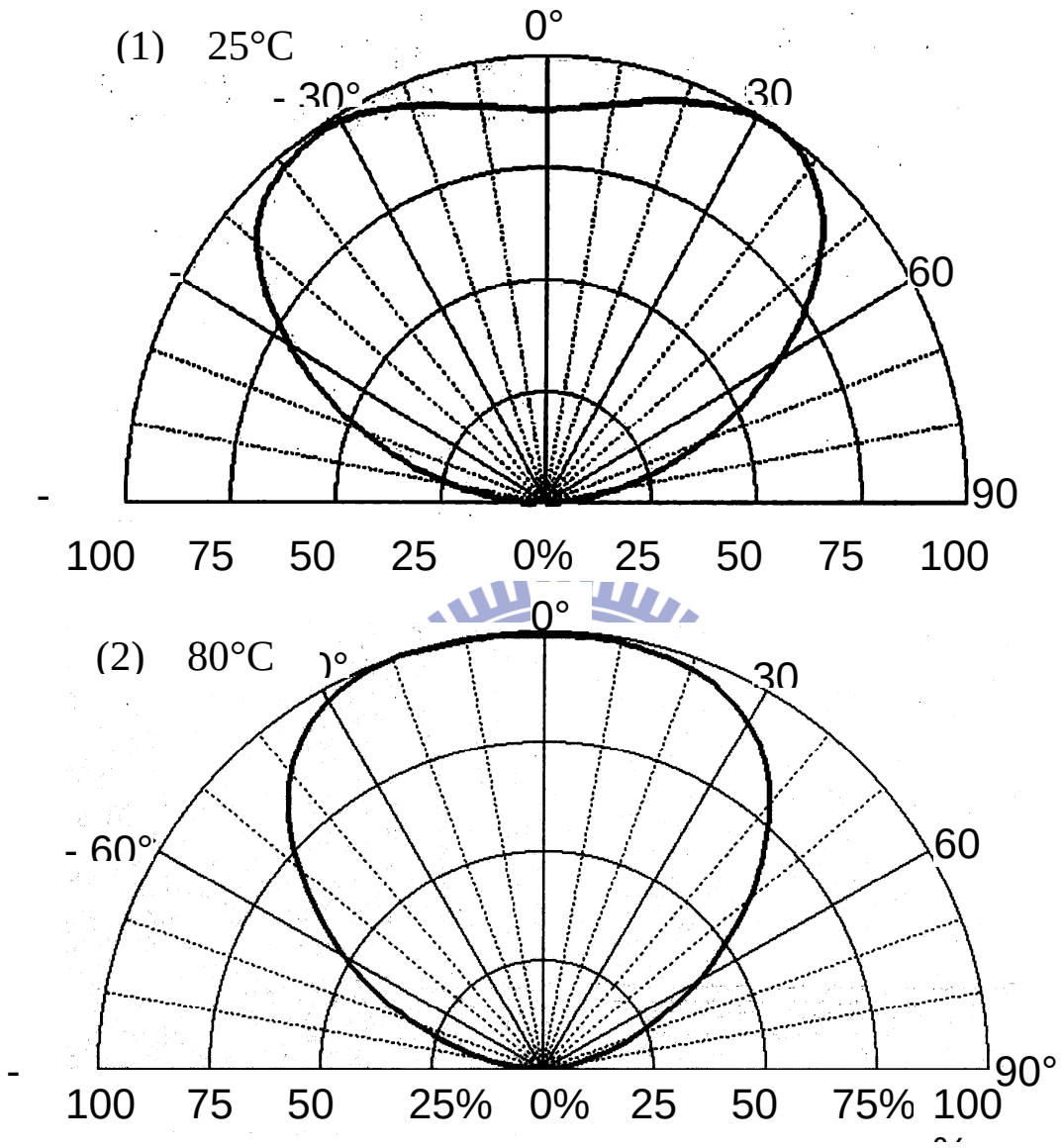


Figure 2.19: The far-field patterns of the MBRCLEDs devices under 20 mA current injection versus ambiance temperature of (1) 25°C, and (2) 85°C.

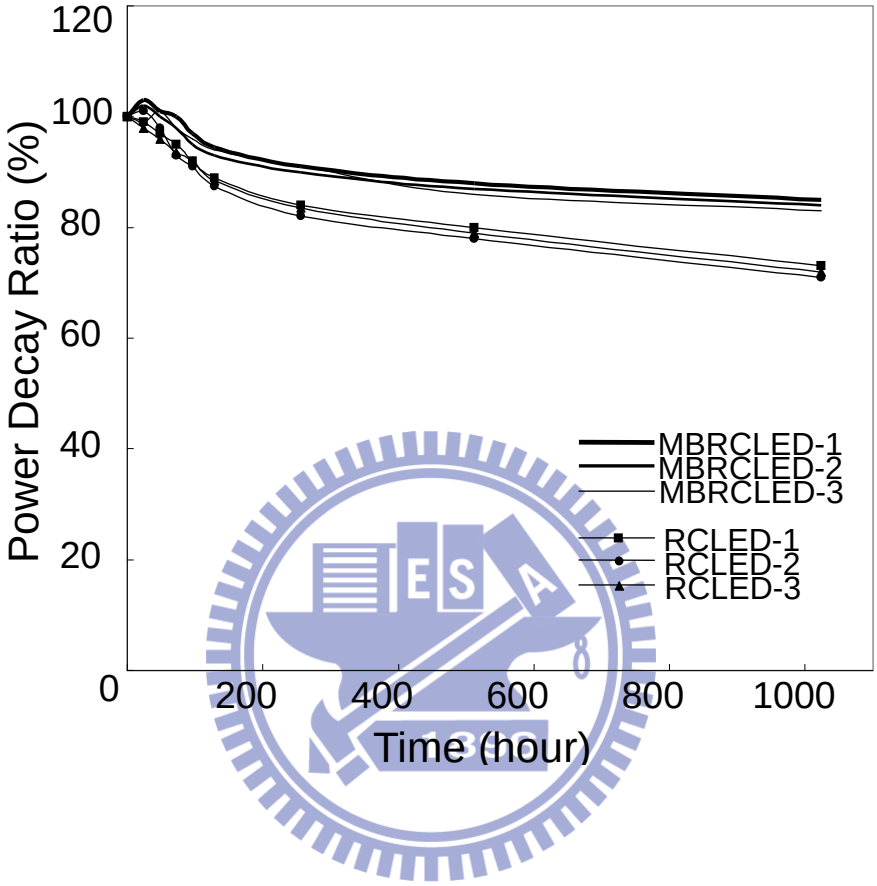


Figure 2.20: Reliability results of the MBRCLEDs and the RCLEDs under a condition of 85°C and 20 mA driving current for life test.

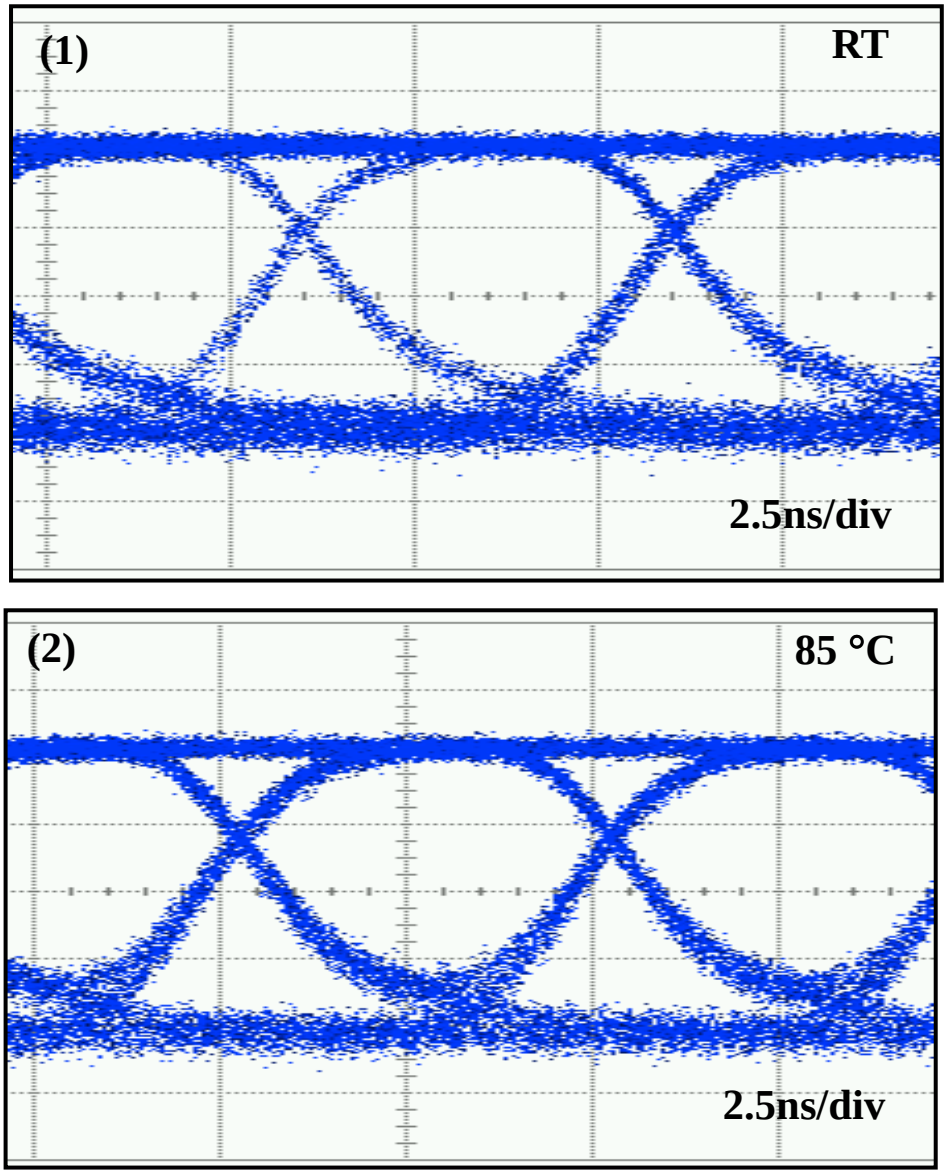


Figure 2.21: (1) 25 °C and (2) 80 °C eye diagram of the MBRCLEDs under 20 mA driving current. The scale in the figure is 2.5 ns/div.

CHAPTER 3

Light Extraction Enhancement of AlGaInP-Based Light-Emitting Diodes in Wafer Bonding Technique

3.1 Introduction

The III-phosphide material system, $(Al_xGa_{1-x})_{1-y}In_yP$, is lattice matched to GaAs substrate for y=0.48. The $(Al_xGa_{1-x})_{1-y}In_yP$-based alloy material with wide commercial availability of high quality GaAs substrate allows for relatively straightforward epitaxial growth of optoelectric devices in this material system, with high quality epi-wafer was demonstrated by metal-organic chemical vapour deposition (MOCVD) as well as molecular-beam epitxay (MBE) method (MBE). The $(Al_xGa_{1-x})_{1-y}In_yP$-based alloy materials with the light output spectrum from the red to yellow-green visible part were made available. Direct bandgap emission is available from x=0 (InGaP) with a ~1.9 eV bandgap and ~650 nm (deep red) to x=0.53 with a ~2.2 eV and ~560 nm (yllow-green). Recently, the high performance AlGaInP-based LEDs were widely used for many applications, such as optical communications, automobile tail light, traffic light, full-color display, interior and exterior display [1], [2]. The AlGaInP-based materials have been continuously improved for many years since the first practical LED was developed in 1962 made of the GaAsP material [3], and this allow material system becomes the most major material for high brightness and high efficiency light-emitting diodes (LEDs) applications. In recent years, the internal quantum efficiency IQE (η_i) AlGaInP-LEDs has closely approached 100% due to the excellent epitaxy technique [4], [5]. Although AlGaInP LEDs has higher internal quantum efficiency than conventional GaN-based LEDs grown on c-plane sapphire substrates, the light extraction efficiency is estimated to be less than the GaN-based LEDs due to the large refractive index difference between the GaP window layer (n=3.2) and air or epoxy. According to the Snall's

law, the critical angle (θ_c) is approximately 18.2˚ and the most of the generated photons will be trapped in the semiconductor due to the total internal reflection (TIR) effect. In addition, the conventional AlGaInP-LEDs have an absorbing substrate and a planar light emitting surface. These effects will serious limit the external quantum efficiency especially in AlGaInP-based material. Therefore, several methods to solve the light extraction of conventional LEDs structure were invented, such as an ultra-thick GaP window layer was grown on the surface [6], replaced the GaAs absorbing substrate (AS) with a GaP transparent substrate (TS) through a directly wafer bonding technique [7], the truncated-inverted-pyramid (TIP) geometry LEDs method to enhance the lateral light output [8], a surface-textured by natural lithography method to increase the critical angle and the probability of emitted light escape from air-semiconductor interface [9], a triangle-like morphology roughness was applied on the surface [10], a surface was deposited a transparent film of CTO (cadmium-tin oxide) or ITO (indium-tin oxide) for enhancing the critical angle and as a function of a current spreading layer [11], a transparent, conductive and lower refractive index film was deposited on device surface [12], a novel technique of omni-directional reflector (ODR) structure could achieve high light extraction efficiency [13], [14], and the absorbing GaAs substrate was replaced with a transparent sapphire substrate which has a geometric shaping sidewall [15], [16]. In this chapter, we presented several methods for enhancing light extraction. Firstly, we used glued bonding to replace the absorbing GaAs substrate with a transparent sapphire substrate, which has a geometric sapphire substrate, for enhancing total output power from devices sidewall. And then, we produced the flip-chip form under this devices structure for solving the poor thermal dispersion sapphire substrate. Finally, we produced surface roughness using micro- and nano-scale surface textured for enhancing light extraction efficiency.

3.2 Enhancing Light Extraction Efficiency of AlGaInP-Based LEDs in Glue Bonding

3.2.1 AlGaInP-Based LEDs with a Geometric Sapphire Substrate

In this study, the AlGaInP-based LEDs with a dominant wavelength (λ_d) at 585 nm were grown on 2-inch GaAs substrates by a low pressure metal–organic chemical vapor deposition (MOCVD) system. The epi-wafer structure consisted of a 0.08 μm-thick *n*-$Ga_{0.5}In_{0.5}P$ etching stop layer grown on a GaAs buffer layer, a 1 μm-thick Si doped n-$(Al_{0.7}Ga_{0.3})_{0.5}In_{0.5}P$, a 0.7 μm-thick Si doped *n*-$Al_{0.5}In_{0.5}P$ cladding layer, a 0.5 μm-thick unintentionally doped active layer with 20 periods $(Al_{0.7}Ga_{0.3})_{0.5}In_{0.5}P$/ $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ multiple quantum wells (MQWs), a 0.7 μm-thick Mg doped *p*-$Al_{0.5}In_{0.5}P$ cladding layer, a 5 μm-thick Mg doped p-GaP window layer. Finally, a 5 nm-thick heavily doped ($p = 1\times10^{-19}$ cm^{-3}) p^+-GaP contact layer was grown on the epi-layer surface for improving the ohmic contact.

In chip process, a c-plane sapphire substrate was lapped and polished from 450 μm thickness to 220 μm before glue bonding process. A 2 μm-thick SiO_2 was deposited onto the front side and backside sapphire substrate via plasma enhance chemical vapor deposition (PECVD), as shown in figure 3.1 (1) and (2) shows that the backside SiO_2 film was defined pattern with 1000 μm×1000 μm using a standard photolithography as a function of the wet-etching hard mask. The patterned sapphire substrate was then immersed into a $3H_2SO_4$:$1H_3PO_4$ solution at an etching temperature of 340°C for 40 min, and then a patterned array sapphire substrate, which has an oblique sidewall was formed, as shown in figure 3.1 (3). The etching rate of the sapphire substrate is closely achieved 1.4 μm per minute in this study. The etching rate depended on the H_3PO_4 concentration and the temperature of etching solution. A 280 nm-thick ITO film as a function of ohmic contact layer was deposited on p^+-GaP surface by e-beam evaporation. Figure 3.1 (4) shows that the epi-wafer was flipped and bonded to a sapphire substrate using commercially available epoxy glue, and the wafer pair was loaded into a furnace under 300°C for 40 min in nitrogen ambiance. After wafer

bonding process, the absorbing GaAs substrate and the etching stop layer were removed by chemical etching solution of NH_4OH based and H_3PO_4: HCl respectively, as shown in figure 3.1 (5). In surface roughed texture processes, thin metal layers of Au/ AuGe (300Å/ 200Å) were deposited on n-AlGaInP layer surface firstly as shown in figure 3.1 (6). The wafer was alloyed by RTA (rapid thermal annealing) at 450°C for 1 min in nitrogen ambiance. Figure 3.1 (7) shows that the densely, strongly and naturally particles with nano-scale were clustered on surface to serve as the wet etching mask. The wafer was immerged into chemical solutions of KI and H_3PO_4 respectively. After etching processes, the n-side up surface with a nano-roughed texture was formed shows in figure 3.1 (8). Then, a regular array of Au/ AuGe n-contact micro-dots shape metal was deposited on the roughed surface. A 280 nm-thick ITO was deposited on the surface as functions of current spreading, transparent conductive layer and lower reflective index window layer. The GSS-LEDs with a chip size of 1000 μm×1000 μm were fabricated using standard photolithography processes which were aligned with backside shaping pattern of sapphire substrate. The devices mesa etching using an etcher of inductively coupled plasma (ICP) until p-side ITO layer was exposed for p-electrode formation, as shows in figure 3.1 (9). Figure 3.1 (10) shows the Ti/ Pt/ Au (100 nm/50 nm/2500 nm) metals were then deposited for the p- and n-electrode pads. Finally, the geometric sapphire shaping wafer was subjected to laser scribed and broken into 1000 μm×1000 μm chips size in this study, as shown in figure 3.1 (11). The chip was bonded on ceramic of PLCC 5050 package model for electrical and optical properties measurements by CAS140CT-152 array spectra-meter system.

A schematic diagram of the AlGaInP-based GSS-LEDs structure with an oblique sidewall substrate and a sandwich transparent conductive ITO layer was shown in figure 3.2 (1). In this study, the oblique sidewall angle of sapphire substrate was depends on the sapphire crystallography. In figure 3.2 (2) illustrated that the different extracted light path of the

GSS-LEDs and the conventional glue-bonding LEDs (GB-LEDs). As this schematic diagram results, the GSS-LEDs with more opportunities of output light escaped from the oblique sidewall of sapphire substrate. Figure 3.3 shows the scanning electron micrograph (SEM) images of sapphire shaping structure (1) cross-section and (2) top views. The oblique sidewall with a 100 μm etching depth could be obviously observed. The crystallography facets were (1102) *R*-plane, (1010) *M*-plane, and (1120) *A*-plane against the (0001) *c*-axis and their angles against the (0001) *c*-axis are about 60◦, 50◦ and 29◦, respectively. In this study, the sapphire was etched for 70 min via the etching rate of about 1.4 μm/ min and the etching depth was about 100μm. Furthermore, the etching structures are all V-grooves. Figure 3.3 (3) is a sample schematic illustration of the phenomenon mentioned above. According to this figure, the total area of (0001) *C*-plane decreases as the etching time increases due to its relatively fast etching rate. On the other hand, the oblique surface of the (1102) crystallography etched facet increases with the etching time resulting in the formation of a V-shape groove. Figure 3.5 (1) and (2) shows the photomicrographs of the GB-LEDs and the GSS-LEDs, respectively. These two kinds device structures were replaced the conventional GaAs substrate with a transparent sapphire substrate. The radiate output light is not only surface emitter but a volume emitter. Besides, it is significantly that the oblique sidewall of GSS-LEDs (2) appears higher brightness under 70 mA current injections as compared with the GB-LEDs (1). As this result, the light extraction efficiency was enhanced via oblique sapphire geometry. The corresponding luminous intensity-current-voltage (*L-I-V*) characteristics of GB-LEDs and GSS-LEDs were measured respectively, as shown in figure 3.6. The forward voltage (at 350 mA) of the GB-LEDs and the GSS-LEDs is 3.30 V and 3.28 V, respectively. Both of the electrical behaviors are very closely and normally. In luminous intensity versus current result, it is clearly observed that the luminous intensity of the GSS-LEDs is larger than the GB-LEDs. Under 350 mA current injections, the power intensity of the GB-LEDs and the GSS-LEDs is

approximately 40.8 mW and 51.7 mW, respectively. It is found that the luminous intensity of the GSS-LEDs without an epoxy lens encapsulated could be enhanced about 26.7% under 350 mA current injections as compared with the GB-LEDs. It is indicated that the oblique sidewall could reduces the total internal reflection and improves the light extraction probability of photons escaping from semiconductor to air. Figure 3.7 shows the normalized output beam pattern of the GB-LEDs and the GSS-LEDs sample under 70 mA current injections, respectively. In this compared figure, it is clearly noted that the 50% power angle of the GSS-LEDs is wider approximately 12.5º as compared with the GB-LEDs. It is afresh indicated that the enhancements of the 50% power angle and output power could be attributed to the geometric sapphire shaping LEDs with an oblique sidewall.

In sumary, the GSS-LEDs with an oblique sapphire geometric substrate were fabricated via glue bonding. In this evolutional GSS-LEDs performances, the light output power could be enhanced 26.7% under 350 mA current injectionsas compared with GB-LEDs. Furthermore, it was demonstrated that the GSS-LEDs structure could not only reduce the TIR effect but increase more probabilities of output light escaping from the transparent substrate with an oblique sidewall.

3.2.2 AlGaInP-Based Flip-Chip LEDs with a Thick Geometric Sapphire Substrate Window Layer

A novel GSS-LEDs which has higher light extraction efficiency than conventional GB-LEDs was demonstrated in last section. However, as we know the sapphire is a poor thermal dispersion material, and it is still not suitable for high current injection or high temperature ambience operating especially in short wavelength of AlGaInP system material. The high temperature and high current density will cause the carriers overflow in shallow quantum well, and this phenomenon will result in poor electron-hole recombination efficiency.

In this section, a novel flip-chip AlGaInP-LEDs structure which has a thick geometric sapphire substrate (GSSFC-LEDs) window layer was demonstrated using glue bonding and flip-chip bonding techniques. The flip-chip LEDs have stable properties in high temperature operation and high current density injection due to the p-n junction is closely to heat dispersion sub-mount. We continue using the geometric sapphire substrate technique in last section, and then combine geometric sapphire substrate with AlGaInP epi-wafer. This geometric sapphire substrate could be a thin window layer as a function of enhancing light extraction. Besides, the flip-chip LEDs could provide an excellent performance in high temperature ambience and high current injection.

The epi-wafer structure of layer by layer is the same as the GSS-LEDs, which has a dominant wavelength (λ_d) at 585 nm, were grown on 2-inch GaAs substrates by a low pressure metal–organic chemical vapor deposition (MOCVD) system. In figure 3.8 shows the chip processes flowcharts. Firstly, a c-plane sapphire substrate was lapped and polished from 450 μm to 250 μm thickness. After that, a 2.5 μm-thick SiO_2 film as a function of the wet-etching hard mask deposited onto the backside of sapphire substrate via plasma enhanced chemical vapor deposition (PECVD) and defined chip size pattern (1000 μm × 1000 μm) via a standard photolithography and following wet etching process. This sapphire substrate which backside has patterning was immersed into a high temperature (350ºC) mixture solution (H_2SO_4/ H_3PO_4) for 65 min. The etching rate of the sapphire substrate is closely achieved 1.5 μm/ min in this investigation (i.e., step 2). The epi-wafer having a nano-scale rough texture was produced on epi-wafer surface of GaP window layer. Nano-scale rough texture surface were formed by a Ni metal ultra-thin film (10nm). After the epi-wafer was treated in the rapid thermal annealing (RTA) under 750ºC ambiance for 1 min, the Ni film was clustered a Ni nano-mask on GaP surface. The rough texture surface was finished after the epi-wafer was suffered an inductively coupled plasma (ICP) etcher process (i.e., step 3). A 280 nm-thick ITO

was deposited on the surface as functions of current spreading, transparent conductive layer and lower reflective index window layer. The epi-wafer was flipped and bonded by glue to the sapphire substrate which has pattern on the backside (i.e., step 4). The wafer pair was loaded into a furnace under 300°C for 40 min in nitrogen ambiance. After wafer bonding process, the absorbing GaAs substrate and the etching stop layer were removed by chemical etching solution (i.e., step 5). The mesa was formed via ICP etcher, terminated until the ITO film was exposed. The Au/ AuGe (100 nm/ 20 nm) metals, which functions as an ohmic contact layer and a higher reflector were deposited on the ITO film and n-AlGaInP pads. Finally, the geometric sapphire shaping wafer was subjected to laser scribed and broken into 1000 μm×1000 μm chips size in this study. The AlGaInP-based GSS-FCLEDs, which has an oblique sapphire shaping sidewall, were flip-chip bonded on silicon sub-mount using Panasonic ultra sonic flip chip bonder for electrical and optical properties measurements by CAS140CT-152 array spectra-meter system (i.e., step 6).

Figure 3.9 (1) is the schematic diagram of the GSSFC-LEDs structure, having an oblique sapphire shaping sidewall and a nano-scale rough texture on the epi-structure surface. The top and cross section profile of scanning electron microscopy (SEM) figures of geometrically shaped sapphire were shown in figure 3.9 (2) and (3). The oblique sidewall angle of 61.8º corresponds to the crystallography angle for the R-plane (1102). The possible escaping photon paths inside this novel GSSFC-LEDs and the conventional flip-chip LEDs (CFC-LEDs) structure are illustrated in figure 3.9 (4). It can be seen that the photon paths inside the structures are equivalent. However, the GSSFC-LEDs could have smaller incident angles provided by the oblique sidewalls, explaining that the GSSFC-LEDs structure has less TIR effect and more opportunities for photons escaping from the oblique sidewall to air. Figure 3.10 (1) is the SEM image of the Ni nano-cluster hard mask layer after 750ºC thermal treatment by RTA system, and each cluster height is approximately 300 nm. Figure 3.10 (2) is

the random rough texture on the GaP surface after ICP dry-etching ($Ar/SiCl_4$) process. The purposes of the rough texture on surface not only provide photons with more opportunities to escape the LEDs structure, but also decrease the TIR effect. In figure 3.11, the curves (a) and (b) shows the wall-plug efficiency of the GSSFC-LEDs and the CFC-LEDs. The maximum wall-plug efficiency is 15.45% and 13.34%, respectively. The curves (c)-(e) presents the corresponding luminous intensity versus current (*L-I*) characteristics of the GSSFC-LEDs, CFC-LEDs and conventional glue-bonded LEDs (CGB-LEDs). The corresponding simplified schematic structures were also shown in figure 3.11. For the CGB-LEDs structure, the epi-layer was bonded on sapphire substrate and its structure is n-side up. In the L-I results (without an epoxy lens encapsulated), it is clear that the GSSFC-LEDs with largest light output power than the CGB-LEDs and CFC-LEDs. The output power enhancement of the GSSFC-LEDs and CFC-LEDs could be effectively advanced from 63.4 to 83.2 mW under 350 mA current injection, corresponding to a 31.2% light extraction efficiency enhancement. Such improvement could be attributed to the oblique interface of the geometric sapphire shaping structure which could increase the probability of photons escaping from semiconductor to air. Furthermore, the output power of CFC-LEDs could be enhanced approximately 56.7% in comparison with the CGB-LEDs at 350 mA. According to the output power results of the CGB-LEDs and CFC-LEDs, the power saturation effect of flip-chip structure (GSSFC-LEDs or CFC-LEDs) is less than the conventional n-side-up CGB-LEDs since the flip-chip structure has a better thermal dissipation path. This worst external quantum efficiency of CGB-LEDs could be ascribed to serious leakage current issue while the device was operated in high current injection or high temperature ambience, especially in AlGaInP-based material devices. This inherent drawback results from the quantum well of AlGaInP/ InGaP, having a lower conduction band offset value as compared with AlGaAs/ GaAs and InGaN/ GaN quantum well [17], [18]. It is important that device temperature

insensitively was improved in glue-bonded structure for AlGaInP-LEDs, although these structures having a lower thermal conductivity 35 W/(m·K). The devices reliability of CFC-LEDs and CGB-LEDs under room temperature ambient and 350 mA current injection for 1000 hour was shown in figure 3.12. The power decay ratio of the CFC-LEDs and CGB-LEDs is 18.4% and 35.2% respectively. The reliability test results show that the flip-chip structures are more sutiable for high current and larger chip size applications. Figure 3.13 shows the devices output beam pattern of CFC-LEDs and GSSFC-LEDs under 70 mA current injection. The 50% power angle of the CFC-LEDs and GSSFC-LEDs is 138.8° and 149.2° respectively. The wider light output angle obtained in GSSFC-LEDs indicates that the power enhancement is resulted from the geometric sapphire shaping.

In order to support this theory of output light enhancement from oblique sidewall, we used the commercial ray-tracing software employing the Monte-Carlo algorithm to obtain trajectory of ray-tracing, enhancement efficiency and spatial intensity distributions of radiometric and photometric data. Figure 3.14 shows the schematic diagrams and simulated ray-tracing images of (1) CFC-LEDs and (2) GSSFC-LEDs. It is very clearly that the intensity of the GSSFC-LEDs obviously exceeds that of CFC-LEDs. The corresponding GSS-FCLEDs ray-tracing images at oblique sidewall indicates that a larger number of lights can be extracted from the oblique sidewall as a results of the reduction of total internal reflection and the enhancing probability of photon escaping from semiconductor to air. Finally, the simulated candela maps images of (1) CFC-LEDs and (2) GSSFC-LEDs were shown in figure 3.15. The figures show the relative quantification data of the CFC-LEDs and GSSFC-LEDs total flux. The total flux incident rays of CFC-LEDs and GSSFC-LEDs are 2912 and 3981, respectively. Therefore, the simulation results can be further supported this theory once again.

3.3 Enhancing Light Extraction Efficiency of Surface Textured AlGaInP-Based LEDs in Metal Bonding

In this section, we will introduce another method for enhancing light extraction of AlGaInP-based LEDs which the epi-layer were bonded on Si substrate in metal bonding technique. This structure is different to prior devices structure, which has a transparent sapphire substrate. The most output light is coming from device surface in this structure, and increasing light extraction is important issue. In this investigation, the absorbing GaAs substrate was also replaced by a high thermal dispersion Si substrate, and then micro-bowls array and nano-rods surface textured processes were implemented, which are created using nano-particle spin coating, dry-etching, and wet-etching techniques.

In this study, the AlGaInP LEDs epi-structure was epitaxially grown on 2-inch GaAs (100) substrates by a low pressure metal-organic chemical vapor deposition (MOCVD) system. This structure with a dominant wavelength (λ_d) at 625 nm comprised a 0.1 μm-thick *n*-$Ga_{0.5}In_{0.5}P$ etching stop layer grown on a GaAs buffer layer, a 2 μm-thick Si doped *n*-$(Al_{0.5}Ga_{0.5})_{0.5}In_{0.5}P$, a 0.5 μm-thick Si doped *n*-$Al_{0.5}In_{0.5}P$ cladding layer, a 0.5 μm-thick unintentionally doped active layer with 20 periods $(Al_xGa_{1-x})_{0.5}In_{0.5}P$/ $(Al_yGa_{1-y})_{0.5}In_{0.5}P$ multiple quantum wells (MQWs), a 0.8 μm-thick Mg doped *p*-$Al_{0.5}In_{0.5}P$ cladding layer, a 5 μm-thick Mg doped p-GaP window layer. Finally, an 8 μm-thick double window layer with an ultra-thin GaAs layer was inserted between the *p*-GaP surface window layer and *p*-$Al_{0.5}In_{0.5}P$ cladding layer [19].

Before the metal bonding process, the AuBe/ Au metal dots were arraying contacted on the *p*-GaP surface as a function of p-type ohmic contact. A SiO_2 layer, which the thickness is equal to the AuBe / Au metal, was selectively deposited on the *p*-GaP window layer. A quarter-wave thick indium-tin-oxide (ITO) was sequentially deposited. Next, a 300 nm silver layer was deposited on the ITO layer to achieve the GaP-SiO_2-ITO-Ag omni-directional

reflector (ODR) design in order to enhance the reflectivity. Besides, the Ti/ W/ Pt/ Au multi-layer were orderly stacked on Ag layer to serve a function of adhesion, barrier, and bonding metal. The surfaces of *p*-type Si substrate were successively deposited Ti/ Au/ In metal for ohmic contact and bonding material. The epi-wafer was flipped and bonded to the Si substrate in 220°C ambience. The absorbing GaAs substrate and the etching stop layer were removed by ammonia- and phosphoric-based chemical etchant after metal bonding process. The AuGe alloy metal for *n*-type contact was deposited on the *n*-$(Al_{0.5}Ga_{0.5})_{0.5}In_{0.5}P$ surface layer. In this study, there are three different surface types of LED-I, LED-II, and LED-III. The surface profile in LED-I devices is plane and without any surface textured. The micro-scale surface textures having periodic arrangement were applied to LED-II surface for enhancing light extraction efficiency. The micro-scale surface textures were produced on 2 μm-thick *n*-AlGaInP layer using photolithography and wet-etching process. The LED-II wafers were immersed in chemical mixture solution of bromine and acetic acid for half minute. And then make sure the etched area was appeared bowl-shaped and its maximum depth was closely 1.2 μm. Each mask dot dimension and distance is 3 μm after photolithograph definition, and the 5 μm wide bowl-shaped texture was created after anisotropic etching process. The last type is LED-III, having micro- and nano-scale texture on surface and was produced using twice surface roughness process. The first step surface roughness process is the same as LED-II, producing micro-bowls array on surface. The second process is a monolayer of silica nano-particles as a hard mask was spin-coated on wafer surface which has micro-bowls array textured on surface. After dry-etching process, the nano-rods were formed in each micro-bowl. Actually, the silica nano-particles were first suspended in de-ionized (DI) water diluted in a solution of surfactant at a volume ratio of 5:1. The surfactant serves to reduce surface tension and helps the nano-particles spread through on surface. This suspension was spin-coated on the wafer surface, and wafer was submitted to thermal treatment for enhancing adhesion. The

silica nano-particles coated wafer was then etched by inductive couple plasma (ICP) etcher, using $SiCl_4$ and Ar reaction gases under a fixed flow rate of 45 and 5 sccm, respectively. The nano-particles masks were removed via dilute hydrofluoric acid. Finally, the AuBe/ Au were deposited on the fractional surface for n-type contact, and an antireflection layer of SiO_2 was selectively covered on top surface. Three types processed wafers (LED-I, LED-II, and LED-III), which has different surface texture were subjected to dicing saw scribed into 300 × 300 μm chip size. Devices were packaged on TO-46 form, and the electrical and optical properties were measured using the Instrument System CAS140CT array spectra-meter system.

A schematic diagram of three different type (LED-I, LED-II, and LED-III) metal bonding AlGaInP-based LEDs were shown in figure 3.16, illustrating the devices structure and surface profile. Figure 3.16 (1) shows the LED-I device structure, having a plane surface. The surface with micro-bowls shape texture (LED-II) and added nano-rods texture covered in micro-bowls (LED-III) were shown in figure 3.16 (2). Figure 3.17 schematic diagrams shows the process of micro-bowls (1) (2) and nano-rods (3) (4) surface textured. Each hard mask dimension and distance of photo resistance dot is 3 μm. After anisotropic wet etching, the 5 μm wide micro-bowls were formed on surface. The silica nano-particles were spin-coated on the wafer surface, which were covered through micro-bowls on surface. After dry-etching and the nano-masks were removed, the nano-rods were formed in micro-bowls and surface. Figure 3.18 (1) shows the SEM image of the LED-II chip profile, and the dimension is 300 μm square. The LED-II device surface was covered with micro-bowls, as shown in figure 3.18 (2) ~ (4). Each bowl dimension of width and depth is 5 μm and 1.2 μm, respectively. Figure 3.19 (1) SEM figure is that the silica nano-particles were spin-coated on wafer surface, and sphere diameter is 120 nm. Figure 3.19 (2) ~ (4) show the nano-rods were formed on surface everywhere including bowl bottom, bowl sidewall, and plane surface.

Figure 3.20 shows the plane surface devices (LED-I), micro-bowls textured surface devices (LED-II), and nano-rods were added in micro-bowls textured surface devices (LED-III) performances of forward voltage and luminous intensity versus injection current. With a injection current of 20 mA, the forward voltage of these three types LEDs are almost approximate 1.95 V, and luminous intensity of LED-I, LED-II, and LED-III is 240, 337, and 397 mcd, respectively. Comparing LED-I to LED-II at 20 mA, 40.8% enhancement of luminous intensity was observed and 65.8% luminous intensity enhancement of comparing LED-I to LED-III. The LED-III exhibits highest luminous intensity, in other words, the LED-III has highest light output on off-axis. Furthermore, added nano-rods textured in micro-bowls textured can enhance 17.7% due to the micro- and nano-scale surface texture conduces the less total internal reflection effect. Figure 3.21 shows the output power and wall-plug efficiency (power efficiency) versus operating current. Under a 20 mA current injection, it was found that output power without epoxy resin encapsulated is 3.43, 4.83, and 5.4 mW for LED-I, LED-II, and LED-III, respectively. Although the total luminous flux is the key issue for the surface textured process, the LED-III still exhibits the maximum output power as compared with LED-I and LED-II. Comparing LED-II to LED-III at 20 mA, 10.1% enhancement of total luminous flux was observed. It means that added nano-rods textured surface could increase the probability of photons escaping from semiconductor to air interface. In other words, LED-III has 10% enhancement of light extraction efficiency ($\eta_{extraction}$) was demonstrated as compared with LED-I. Further, the maximum wall-plug efficiency of LED-I, LED-II, and LED-III is 8.82, 12.74, and 14.15%, respectively. Figure 3.23 shows the 50% power angle of the LED-I, LED-II and LED-III is 115.4, 107.7 and 102.2°, respectively. According to this figure results, the LED-III with highest luminous intensity was established on off-axis once again.

3.4 Summary

In this chapter, we used several methods to enhance AlGaInP LEDs performances. The investigation key points of AlGaInP LEDs performances enhancement is replacing absorbing GaAs substrate with a transparent or high thermal dispersion and fabricating surface textured structure to reduce total internal reflection effect. The LEDs characteristic enhancements were based on wafer bonding techniques of glue bonding and metal bonding process, and the surface roughness, geometric structure and flip-chip techniques were also applied to improve the AlGaInP LEDs performances.

In first section, the AlGaInP LEDs with a transparent sapphire substrate were fabricated by glue bonding method. This transparent sapphire substrate is a geometric shaping sidewall structure by chemical wet etching processes. The GSS-LEDs surface has a nano-roughened texture by natural mask and chemical wet etching processes in order to improve light extraction efficiency. In this evolutional GSS-LEDs performances, the light output power could be enhanced 26.7% under 350 mA current injections. Furthermore, it was demonstrated that the GSS-LEDs structure could not only reduce the TIR effect but increase more probabilities of output light escaping from the transparent substrate due to the oblique sidewall structure. A novel GSS-LEDs which has higher light extraction efficiency than conventional GB-LEDs was demonstrated in last section.

However, as we know the sapphire and glue are poor thermal conductive material, and it is still not suitable for high current injection or high temperature ambience operating especially in short wavelength of AlGaInP system material. For this reason, a novel flip-chip AlGaInP-LEDs structure which has a thick geometric sapphire substrate (GSSFC-LEDs) window layer were demonstrated using glue bonding and flip-chip bonding techniques in the second section. This novel GSSFC-LEDs structure shows higher output power, longer reliability and higher wall-plug efficiency as compared with conventional glue bonding

LEDs. The maximum wall-plug efficiency of the GSSFC-LEDs and the conventional flip-chip LEDs (CFC-LEDs) is 15.45% and 13.34%, respectively. The output power enhancement of the GSSFC-LEDs and CFC-LEDs could be effectively advanced from 63.4 to 83.2 mW under 350-mA current injection, corresponding to a 31.2% light extraction efficiency enhancement. The output power of CFC-LEDs could be enhanced approximately 56.7% in comparison with the conventional glue bonding (CGB-LEDs) under 350 mA current injection. Under room temperature ambient and 350mA current injection for 1000 hour, the power decay ratio of the CFC-LEDs and CGB-LEDs is 18.4% and 35.2% respectively. Finally, the wider light output angle obtained in GSSFC-LEDs indicates that the power enhancement is resulted from the geometric sapphire shaping.

The last section is that AlGaInP epi-layers were bonded to a high thermal conductive Si substrate via metal bonding technique, and appeared excellent light extraction efficiency using micro- and nano-scale surface textured technique. This study has three varieties of LED surface shape. The surface profile of LED-I device structure is plane. The LED-II surface has micro-bowls shape texture by anisotropic chemical etching. The novel LED-III structure surface was covered with the periodical micro-bowls in which the random nano-rods were added. In this evolutional LED-III performances, the light output power could be 65.8% under 20 mA current injection as compared with the plane surface device of LED-I. The total output power could be enhanced 10.1% as compared with LED-II if this nano-rods process was attached in micro-bowls surface. Besides, the LED-III also presented higher wall-plug efficiency than others. Finally, the LED-III structure was demonstrated this micro-bowls and nano-rods surface could not only reduce the TIR effect but increase more probabilities of output light escaping from the rough surface.

REFERENCE

[1] C. P. Kuo, R. Fletcher, T. Osentowski, M. Lardizabal, M. Craford, and V. Robbins, "High performance AlGaInP visible light emitting diodes," *Appl. Phys. Lett.*, vol. 57, pp. 2937-2939, 1990.

[2] H. Sugawara, M. Ishikawa, and G. Hatakoshi, "High-efficiency InGaAlP/GaAs visible light-emitting diodes," *Appl. Phys. Lett.*, vol. 58, pp. 157-160, 1991.

[3] K. Kobayashi, "Room-temperature CW operation of AlGaInP double hetero-structure visible lasers", *Electron Lett.*, vol. 21, pp. 931-932, 1985.

[4] I. Schnitzer, E. Yablonovitch, C. Caneau, and T. J. Gmitter, "Ultra-high Spontaneous Emission Quantum Efficiency 99.7% Internally and 72% Externally from AlGaAs/GaAs/AlGaAs Double Heterostructures," *Appl. Phys. Lett.*, vol. 62, pp. 131-133, 1993.

[5] P. Altieri, D. Eisert, A. Jaeger, R. Windisch, N. Linder, P. Stauss, R. Oberschmid, and K. Streubel, "Analysis of Internal Quantum Efficiency of high-brightness AlGaInP LEDs", *Numerical Simulation of Optoelectronic Devices (NUSOD) Proceedings*, pp. 13-14, 2004.

[6] K. H. Huang *et al.*, "Twofold Efficiency Improvement in High Performance AlGaInP Light-Emitting Diodes in the 555–620 nm Spectral Region Using a Thick GaP Window Layer," *Appl. Phys. Lett.*, vol. 61, pp.1045–1047, 1992.

[7] F. A. Kish, F. M. Steranka, D. C. DeFevere, D. A. Vanderwater, K. G. Park, C. P. Kuo,T. D. Osentowski, M. J. Peanasky, J. G. Yu, R. M. Fletcher, D. A. Steigerwald, M. G. Craford and V. M. Robbins, "Very high-efficiency semiconductor wafer bonded transparent substrate (AlxGa1-x)0.5In0.5P/GaP light-emitting diodes," *Appl. Phys. Lett.*, vol. 64, pp. 2839-2841, 1994.

[8] M. R. Krames, M. Ochiai-Holcomb, G. E. Ho¨ fler, C. Carter-Coman, E. I. Chen, I.-H. Tan, P. Grillot, N. F. Gardner, H. C. Chui, J.-W. Huang, S. A. Stockman, F. A. Kish,M. G. Craford, T. S. Tan, C. P. Kocot, M. Hueschen, J. Posselt, B. Loh, G. Sasser, and D. Collins, "High-power truncated inverted pyramid (AlxGa1-x)0.5In0.5P/ GaP light-emitting diodes exhibiting >50% external quantum efficiency, " *Appl. Phys. Lett.*, vol. 75, pp. 2365-2367, 1999.

[9] R. Windisch, B. Dutta, M. Kuijk, A. Knobloch, S. Meinlschmidt, S. Schoberth, P. Kiesel, G. Borghs, G. H. Döhler, and P. Heremans, "40% Efficient Thin Film Surface Textured Light Emitting Diodes by Optimization of Natural Lithography," *IEEE Trans. Electron Devices*, vol. 47, pp. 1492-1495, 2000.

[10] Y. J. Lee, T. C. Lu, H. C. Kuo, S. C. Wang, T. C. Hsu, M. H. Hsieh, M. J. Jou and B. J. Lee, "Nano-roughening n-side surface of AlGaInP-based LEDs for Increasing Extraction Efficiency," *Mater. Sci. Eng. B*, vol. 138, pp. 157-160, 2007.

[11] David J. Lawrence, Daniel C. Abbas, Daniel J. Phelps, and Frank T. J. Smith, "GaAs0.6P0.4 LED's with Efficient Transparent Contacts for Spatially Uniform Light Emission," *IEEE Trans. Electron Devices*, vol. ED-30, no. 6, pp. 580-585, 1983.

[12] Y. K. Su, H. C. Wang, C. L. Lin, W. B. Chen, and S. M. Chen, "Improvement of AlGaInP Light Emitting Diode by Sulfide Pssivation,'' *IEEE Photon. Technol. Lett.*, vol. 15, no. 10, pp. 1345-1347, 2003.

[13] T. Gessmann, E. F. Schubert, J. W. Graff, K. Streubel and C. Karnutsch, "Omni-directional reflective contacts for light-emitting diodes," *IEEE Electron Device Lett.*, vol. 24, no. 11, pp. 683-685, 2003.

[14] T. Gessmann, H. Luo, J. Q. Xi, K. P. Streubel, and E. F. Schubert, 'Light-emitting diodes with integrated omnidirectionally reflective contacts,' *Proc. SPIE Int. Soc. Opt. Eng.*, vol. 5366, pp. 53-61, 2004.

[15] Yea-Chen Lee, Chia-En Lee, Hao-Chung Kuo, Tien-Chang Lu, and Shing-Chung Wang, " Enhancing the Light Extraction of AlGaInP -Based Light-Emitting Diode Fabricated via Geometric Sapphire Shaping,'' *IEEE Photon. Technol. Lett.*, vol. 20, no. 5, pp. 369-371, 2008.

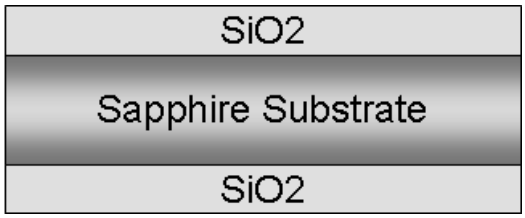
[16] Yea-Chen Lee, Hao-Chung Kuo, Chia-En Lee, Tien-Chang Lu, and Shing-Chung Wang "High Performances $(Al_xGa_{1-x})_{0.5}In_{0.5}P$-Based Flip-Chip Light-Emitting Diode with a Geometric Sapphire Shaping Structure,"*IEEE Photon. Technol. Lett.*, vol. 20, no. 23, pp. 1950-1952, 2008.

[17] D. P. Bour, R. S. Geels, D. W. Treat, D. L. Paoli, F. Ponce, R. L. Thomton, B. S. Krusor, R. D. Bringans, and D. F. Welch, "Strained $Ga_xIn_{1-x}P/(AlGa)_{0.5}$ $In_{0.5}P$ heterostructures and quantum-well laser diodes," *IEEE J. Quantum Electron.*, vol. 30, pp. 593–607,1994.

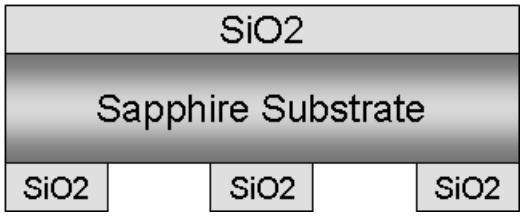
[18] K. Interholzinger, D. Patel, C. S. Menoni, P. Thiagarajan, G. Y. Robinson, and J. E. Fouquet, "Strain-Induced Modifications of the Band Structure of $InGa_xP_{1-x}$-$In_{0.5}Al_{0.5}P$ multiple quantum wells," *IEEE J. Quantum Electron.*, vol. 34, no. 1, pp. 93–100, Jan. 1998.

[19] K.-H Huang, "Efficient Light Emitting Diodes with Modified window Layers," U.S. Patent 5359209, 1994.

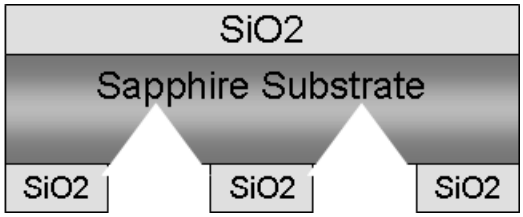
(1)


SiO2
Sapphire Substrate
SiO2

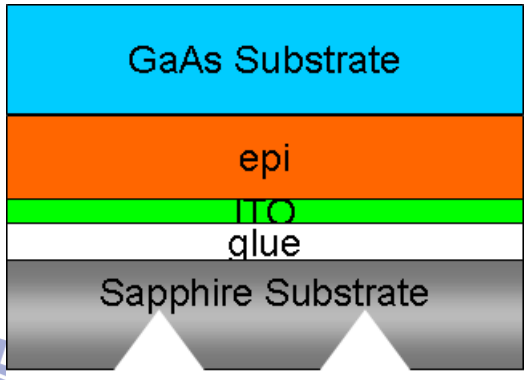
(2)


SiO2
Sapphire Substrate
SiO2
SiO2
SiO2

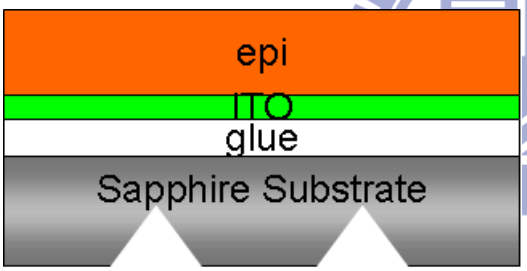
(3)


SiO2
Sapphire Substrate
SiO2
SiO2
SiO2

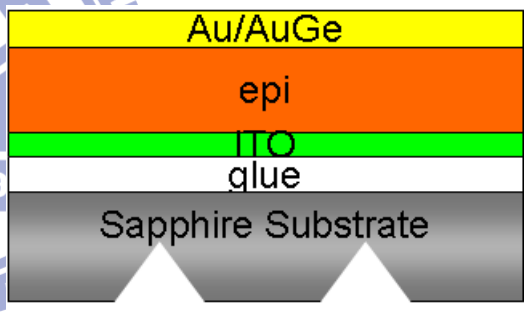
(4)


GaAs Substrate
epi
ITO
glue
Sapphire Substrate

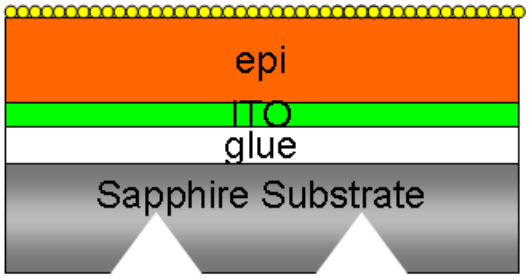
(5)


epi
ITO
glue
Sapphire Substrate

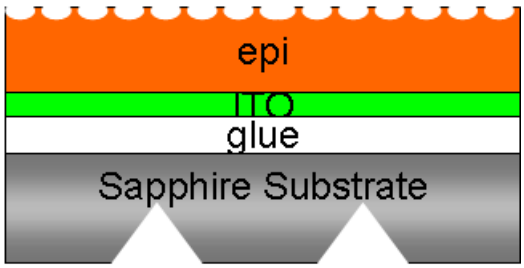
(6)


Au/AuGe
epi
ITO
glue
Sapphire Substrate

(7)


epi
ITO
glue
Sapphire Substrate

(8)


epi
ITO
glue
Sapphire Substrate

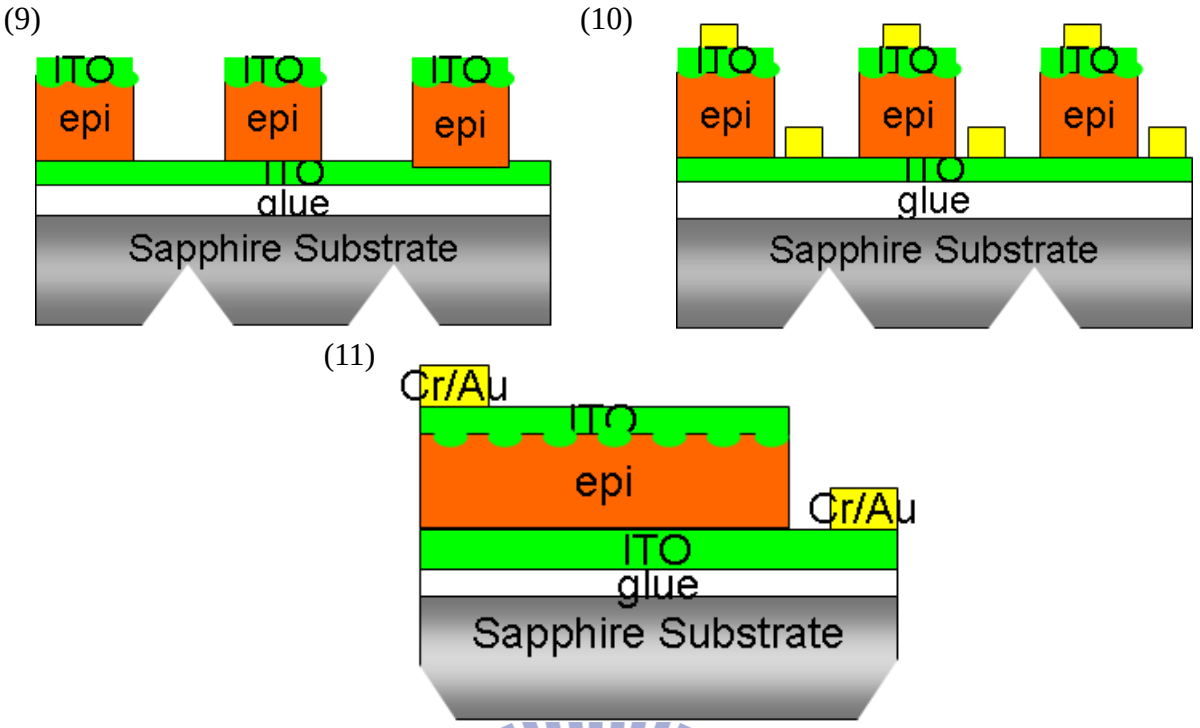


Figure 3.1 : Schematic fabrication processes of GSS-LEDs devices: (1) C-plane Sapphire was thined and polished to 220 μm and then deposited a 2 μm SiO2 on both sides sapphire subatrate. (2) The backside SiO2 film was defined pattern with 1000 μm×1000 μm. (3) After chemical etching, the patterned sapphire, having an oblique sidewall was formed. (4) The epi-wafer was flipped and bonded to sapphire substrate by glue bonding. (5) The GaAs substrate and etching stop layer was removed by chemical etching. (6) A thin metal layers of Au/ AuGe (300Å/ 200Å) were deposited on n-AlGaInP layer surface. (7) A layer which has naturally nano-scale particles were clustered on surface to serve as the wet etching mask. (8) After chemical etching, the random roughed surface was formed. (9) A 280 nm-thick ITO was deposited on the surface and then a mesa isolation processing was produced. (10) The Ti/ Pt/ Au metals were then selected deposited for the p- and n-electrode pads. (11) The wafer was subjected to laser scribed and broken into 1000 μm×1000 μm chips size.

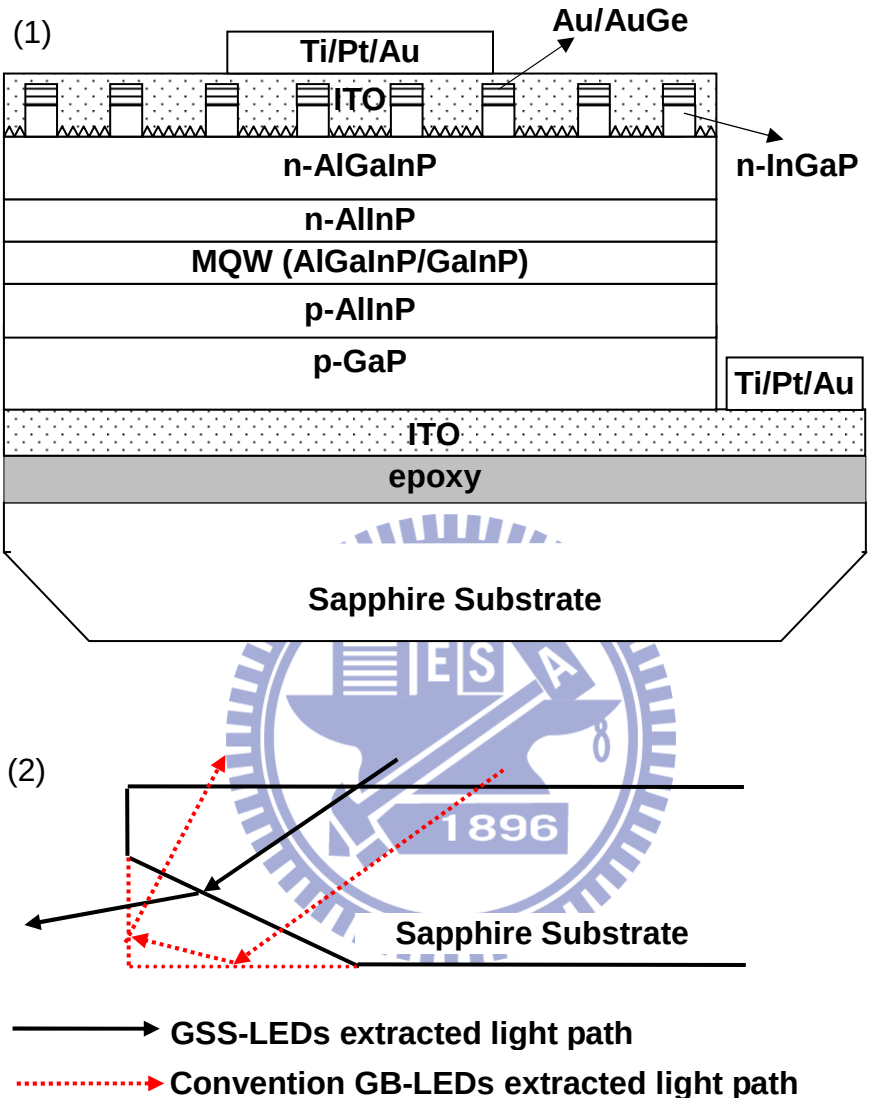
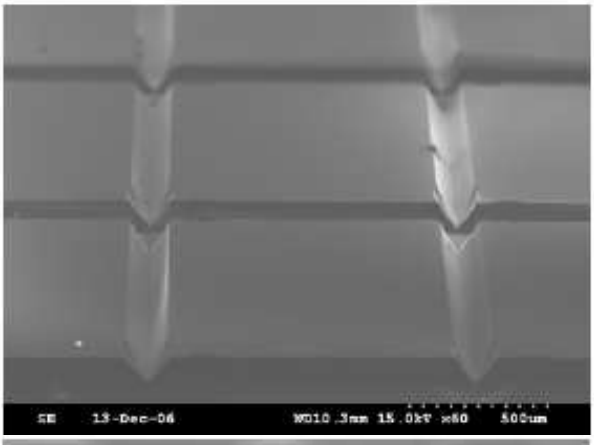
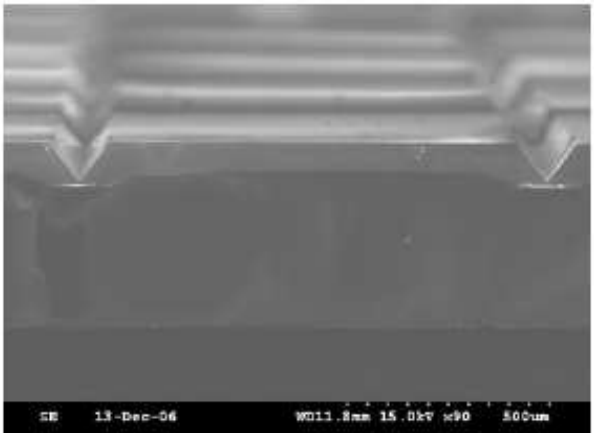


Figure 3.2: (1) Schematic diagram of the AlGaInP-based GSS-LEDs structure with surface textured and sandwich transparent conductive ITO layer. (2) Illustrated that the different extracted light path of the GSS-LEDs and the conventional GB-LEDs.

(1)



(2)



(3)

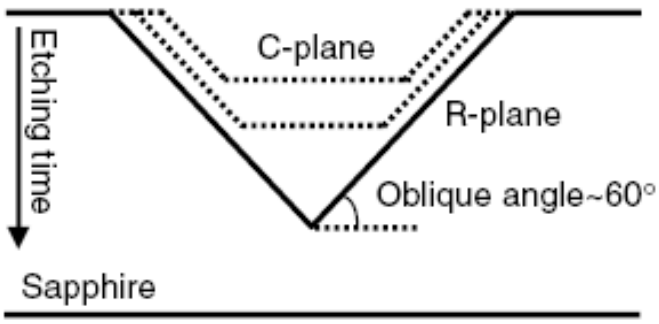


Figure 3.3: Scanning electron micrographs of sapphire shaping structure (1) cross-section and (2) top views. (3) Formation of the V-shape groove with etching time.

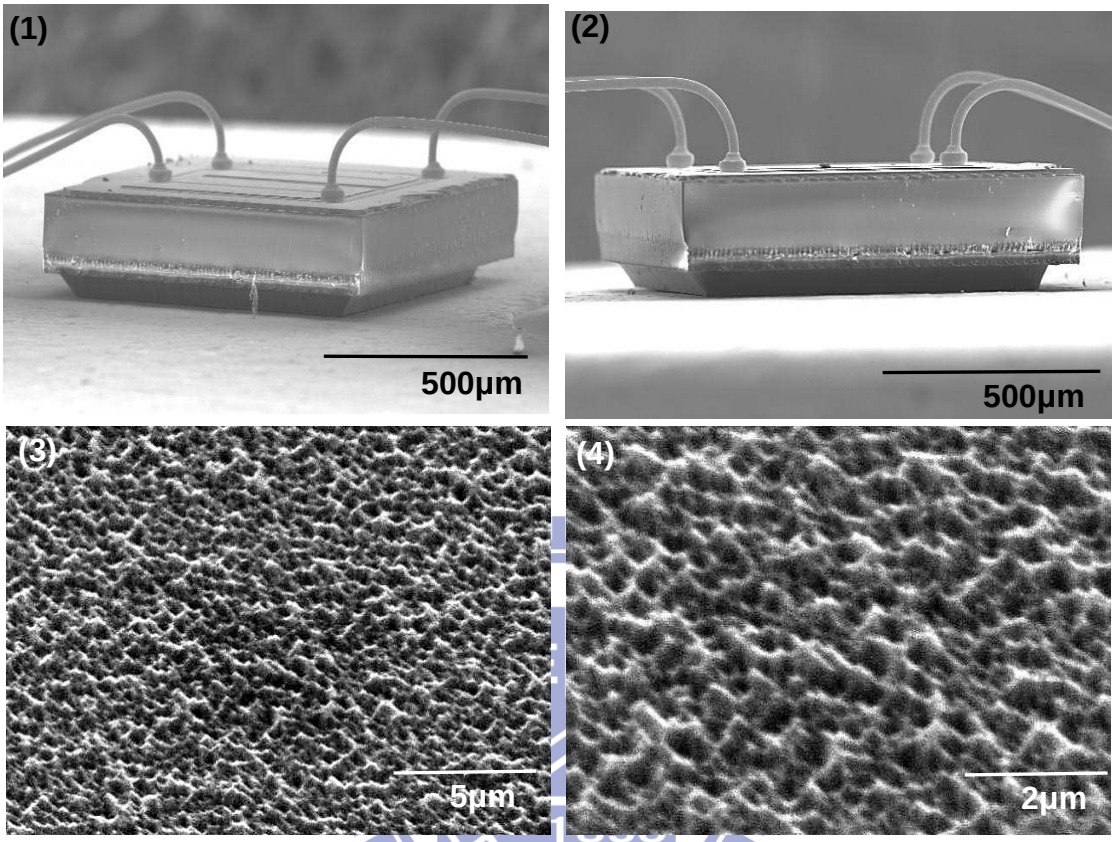


Figure 3.4: SEM images of (1) (2) schematic diagram of the AlGaInP-based GSS-LEDs structure. (3) (4) illustrated the wafer surface with a nano-roughed texture on the thick n-AlGaInP surface layer via natural cluster metal nano-mask and chemical etching processes.

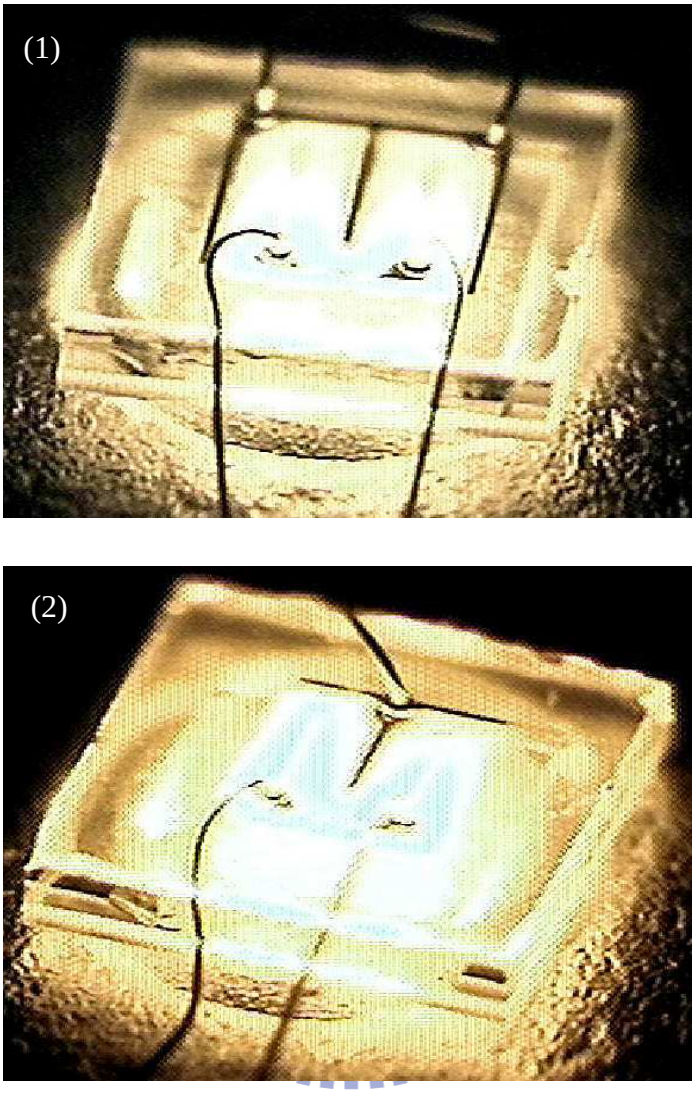


Figure 3.5: A tilted cross-section photomicrographs view of (1) GB-LEDs and (2) GSS-LEDs chip under a forward current 70mA injection.

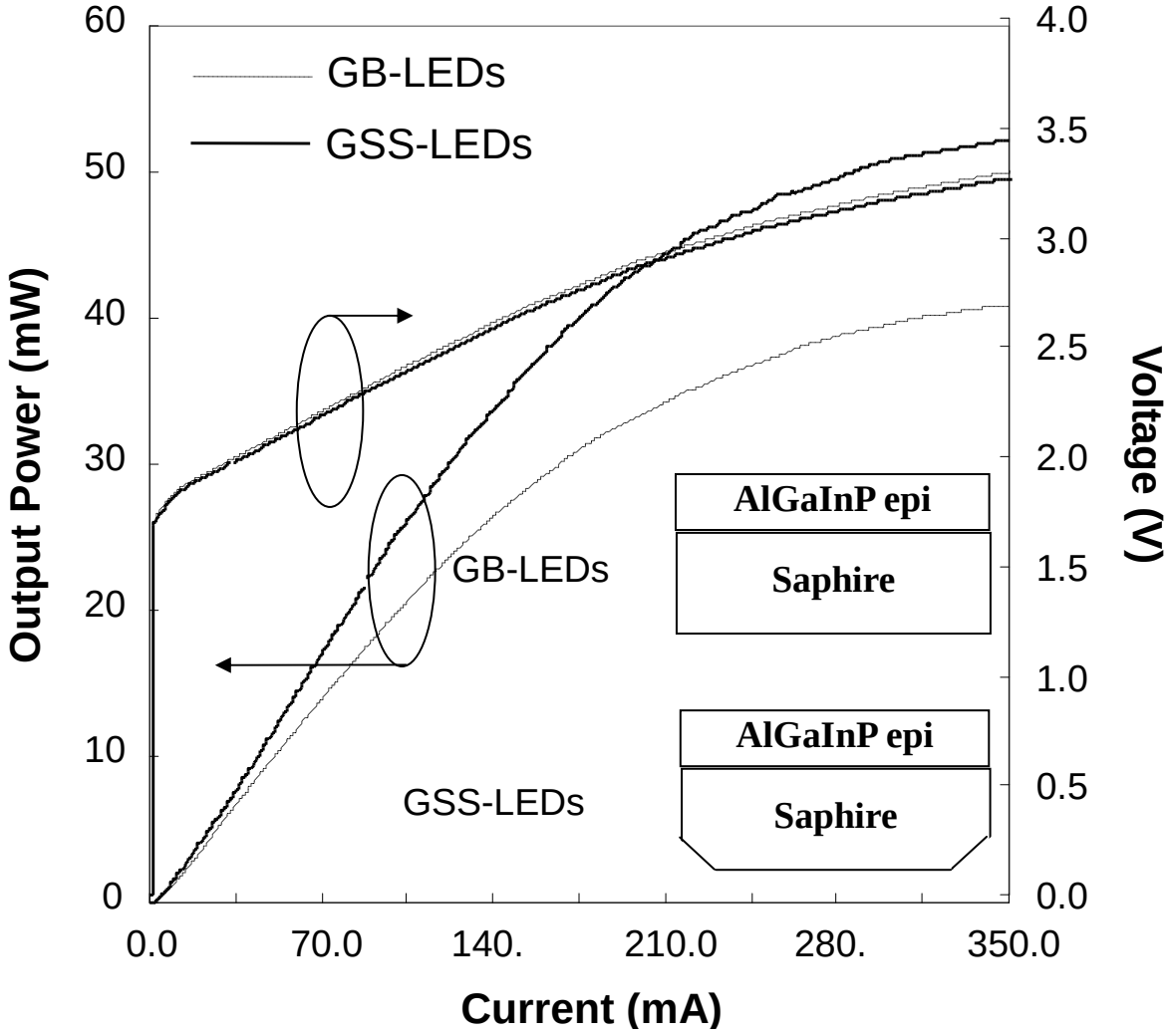


Figure 3.6: The corresponding luminous intensity-current-voltage (L-I-V) characteristics of the conventional GB-LEDs and the novel GSS-LEDs.

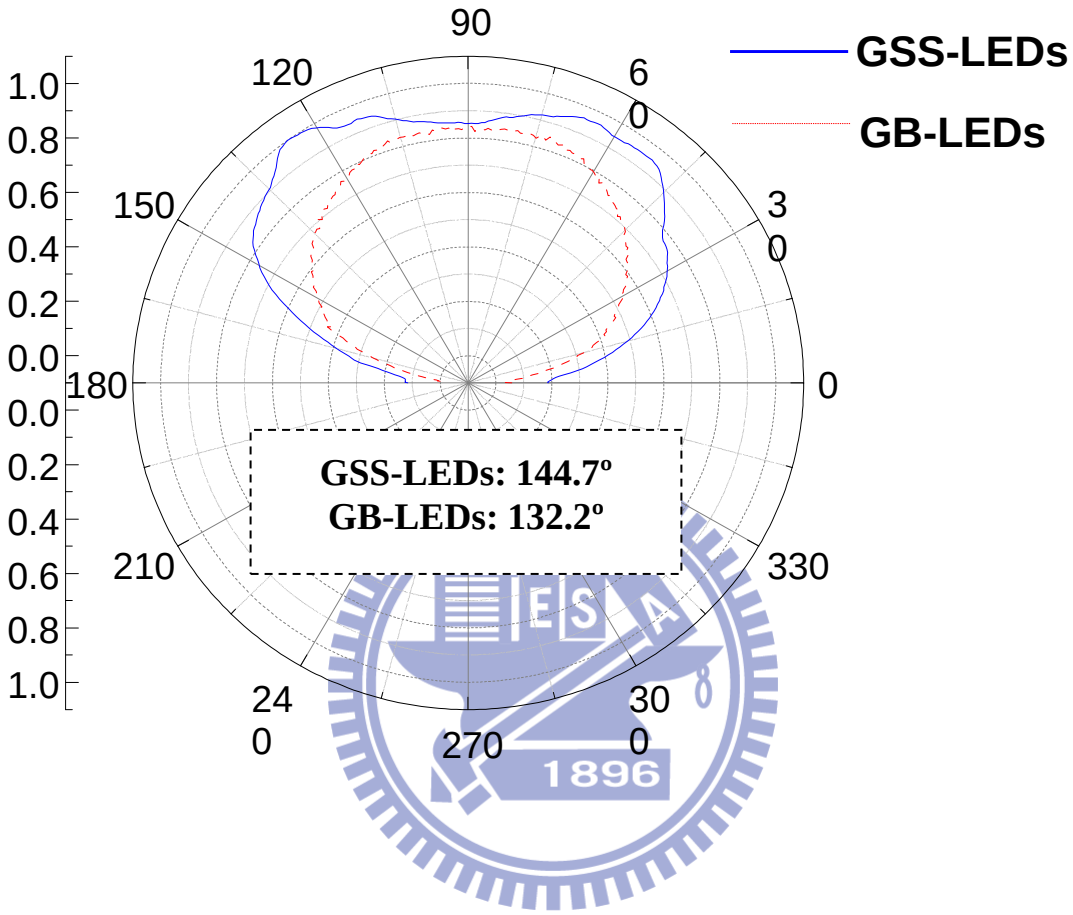


Figure 3.7: Beam patterns of the GB-LEDs and GSS-LEDs under 70 mA current injection.

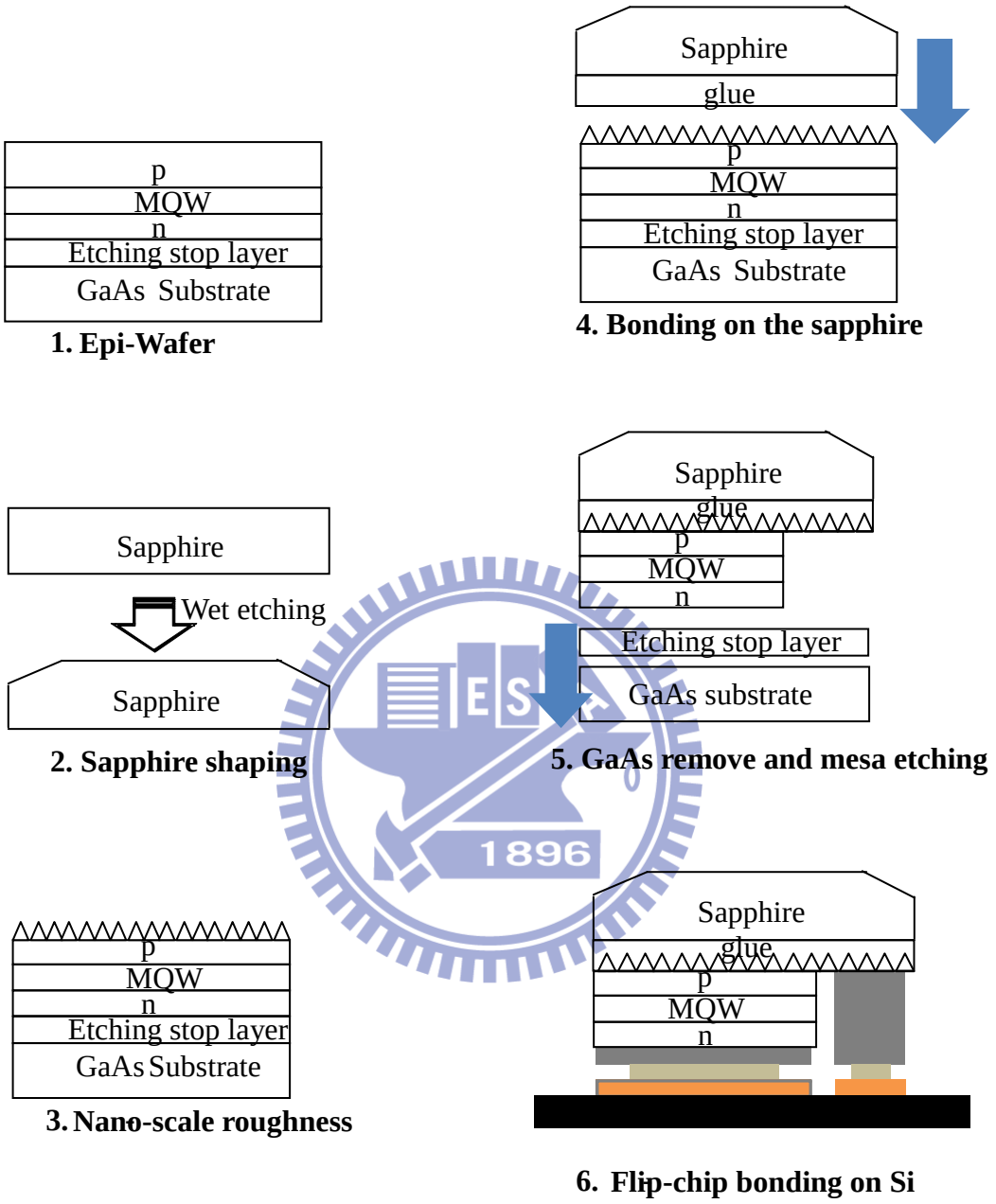


Figure 3.8: Fabrication flowcharts of the GSS-FCLEDs.

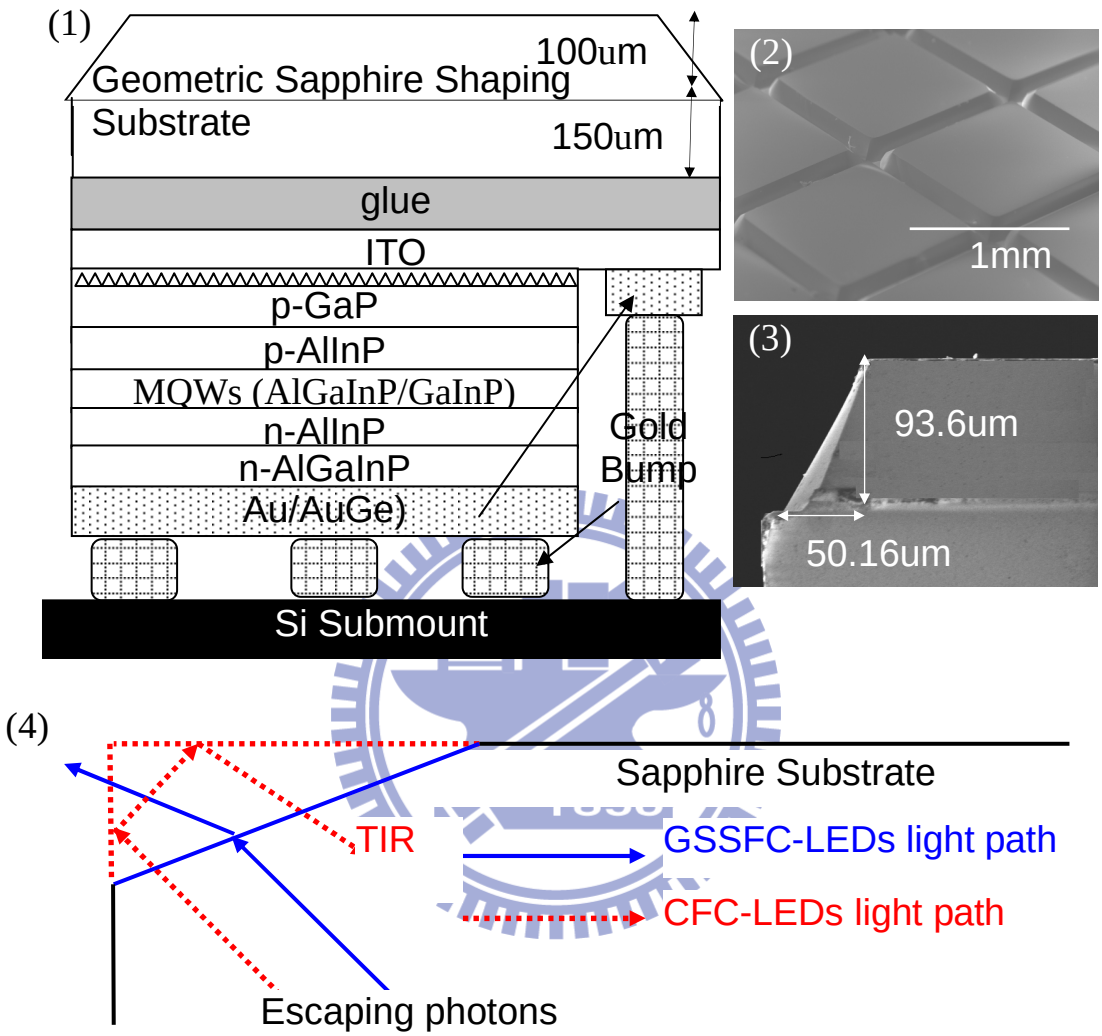


Figure 3.9: (1) Schematic diagram of the AlGaInP GSSFC-LEDs structure. (2) SEM figures of the top view of geometric sapphire shaping substrate profile and (3) Cross section profile. (4) Described with the possible photons paths inside the structure of the GSSFC-LEDs and the CFC-LEDs.

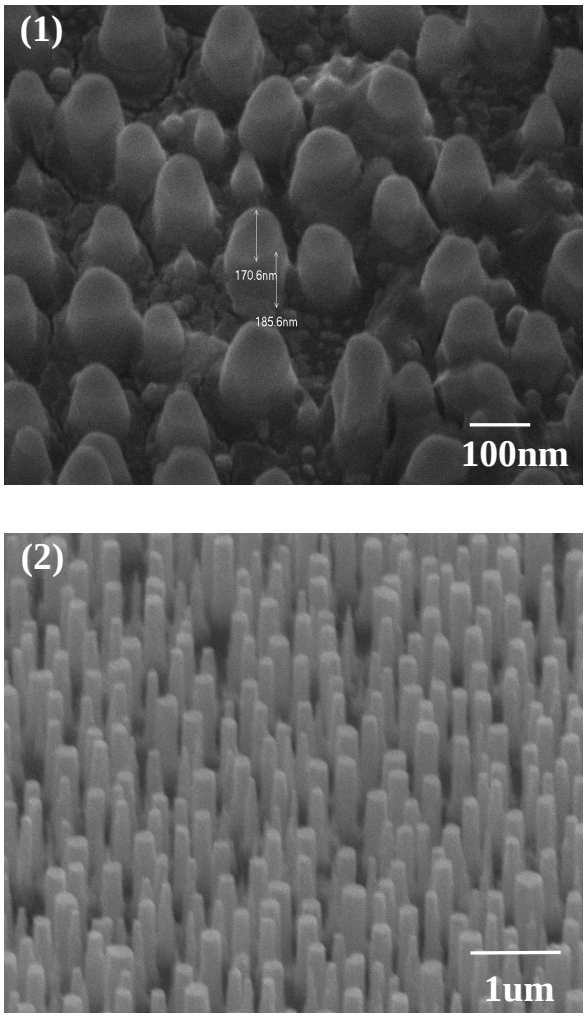


Figure 3.10: (1) Ni nano-cluster hard mask after RTA treatment. (2) Epi-wafer surface with random rough texture after ICP dry-etching process.

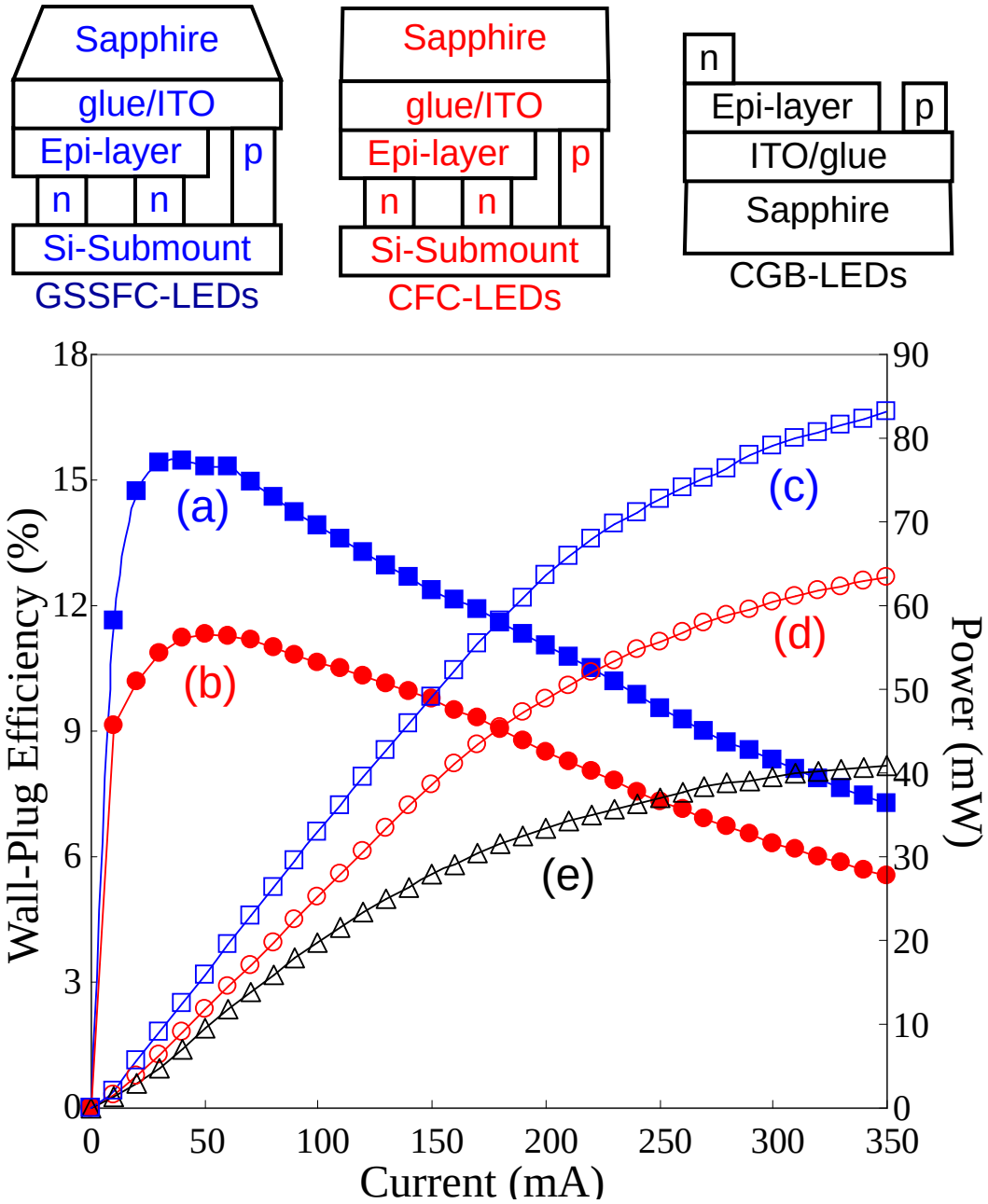


Figure 3.11: (a) (b) The wall-plug efficiency of the GSSFC-LEDs and CFC-LEDs. (c) ~ (e) The L-I characteristics of the GSSFC-LEDs, CFC-LEDs and CGB-LEDs.

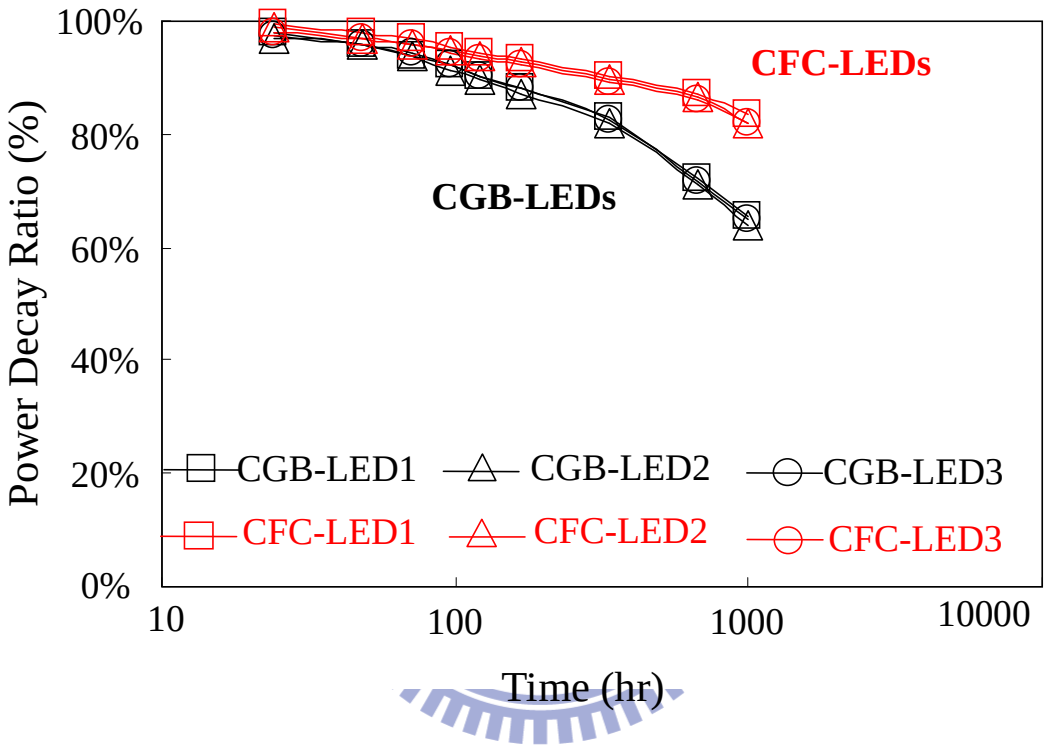


Figure 3.12: Reliability results of the CGB-LEDs and CFC-LEDs under 350-mA current injection in room temperature ambience.

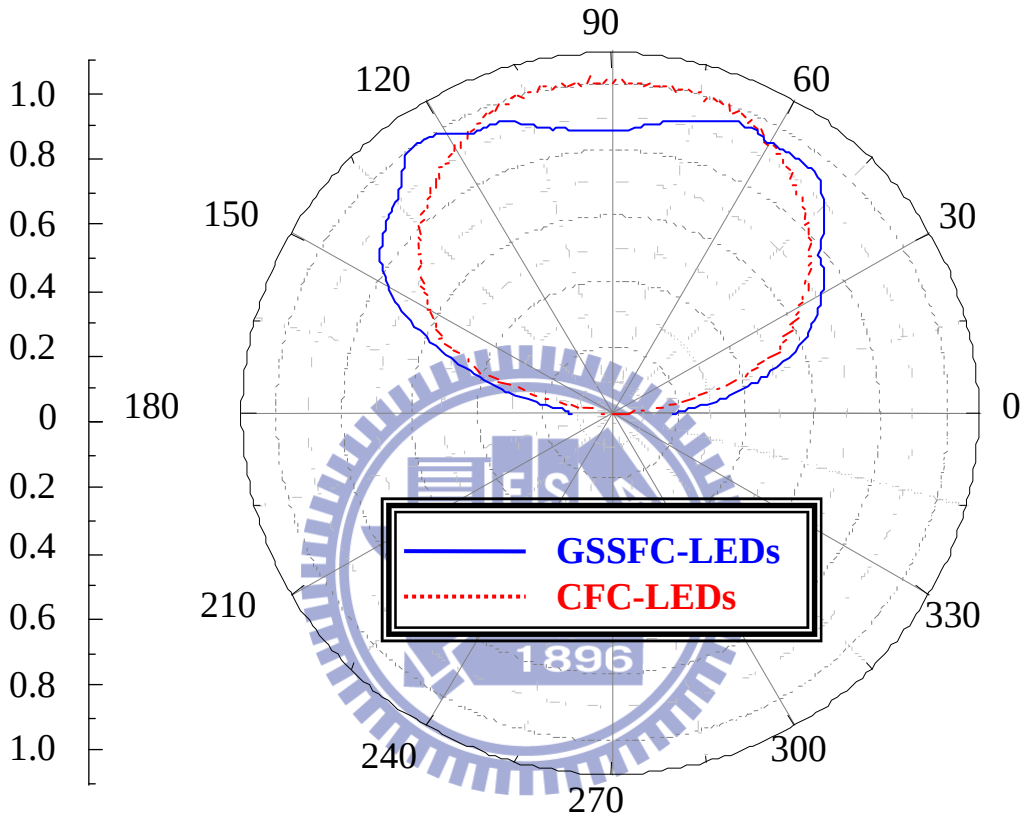
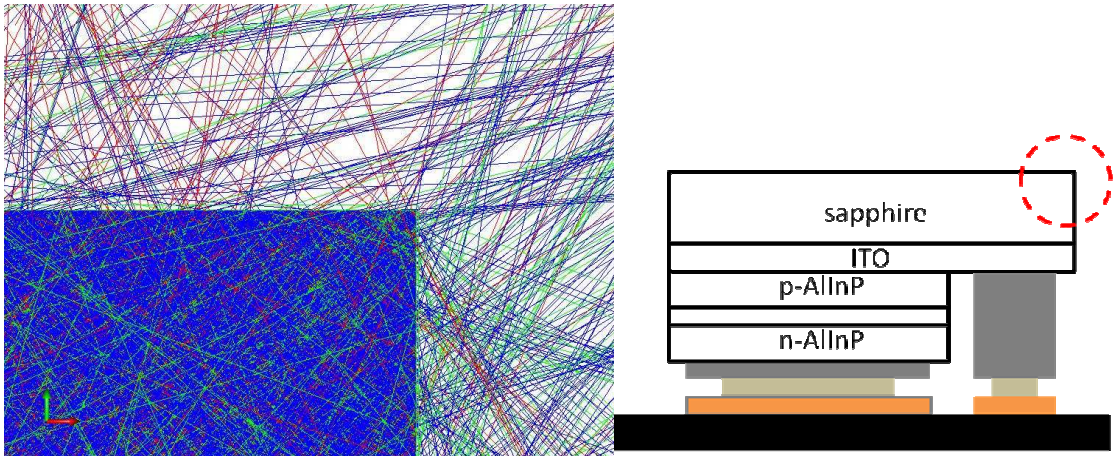


Figure 3.13: The light output pattern of the CFC-LEDs and GSSFC-LEDs.

(1) CFC-LEDs



(2) GSSFC-LEDs

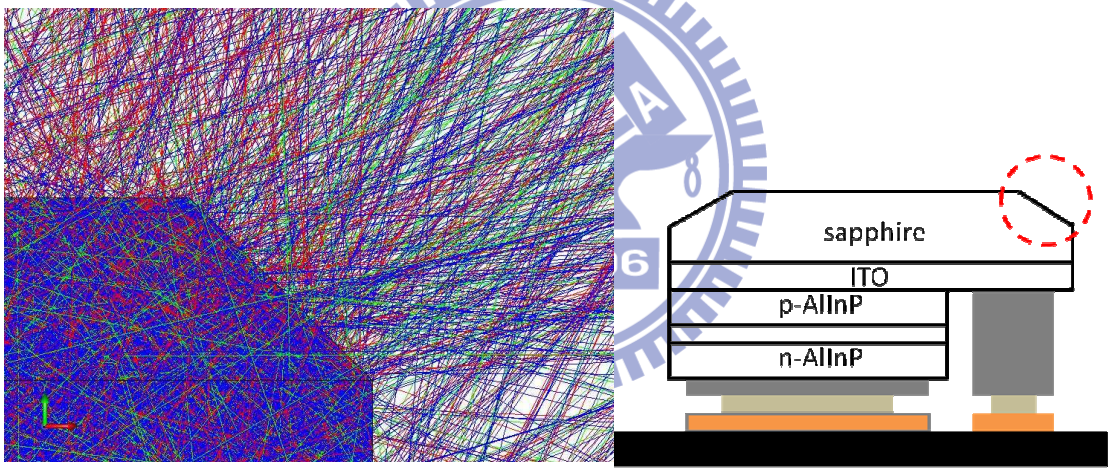
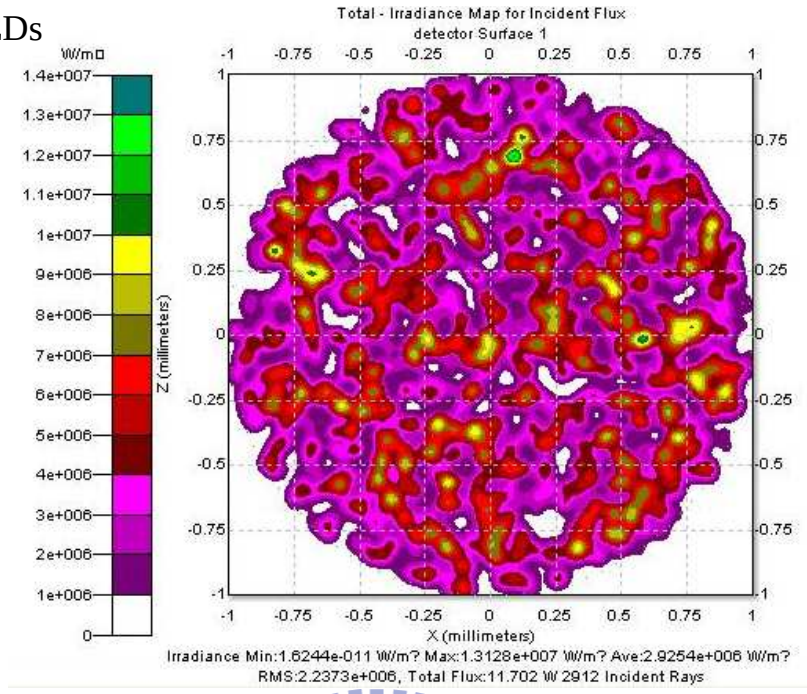


Figure 3.14: The schematic diagram and simulated ray-tracing images of (1) CFC-LEDs and (2) GSSFC-LEDs.

(1) CFC-LEDs



(2) GSSFC-LEDs

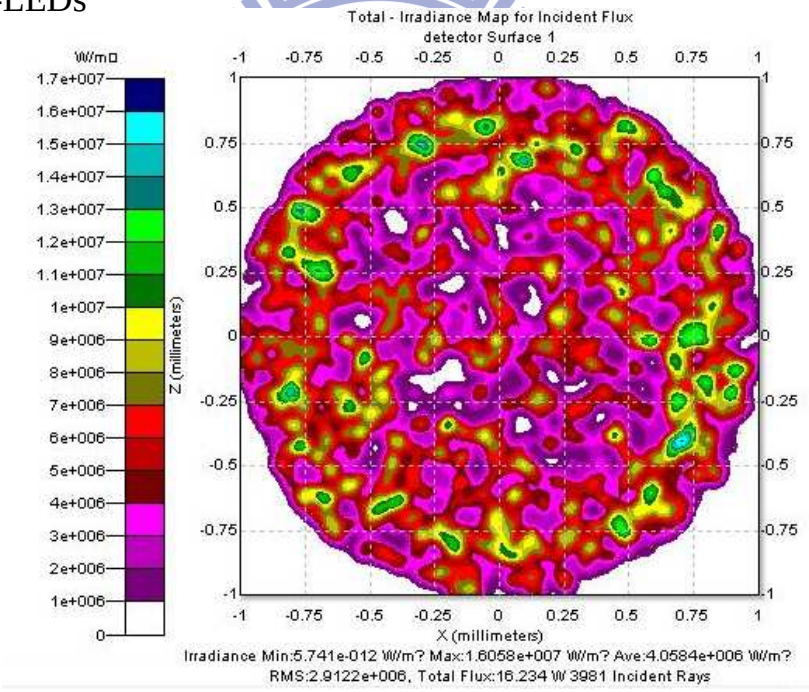


Figure 3.15: The simulated candela maps images of (1) CFC-LEDs and (2) GSSFC-LEDs.

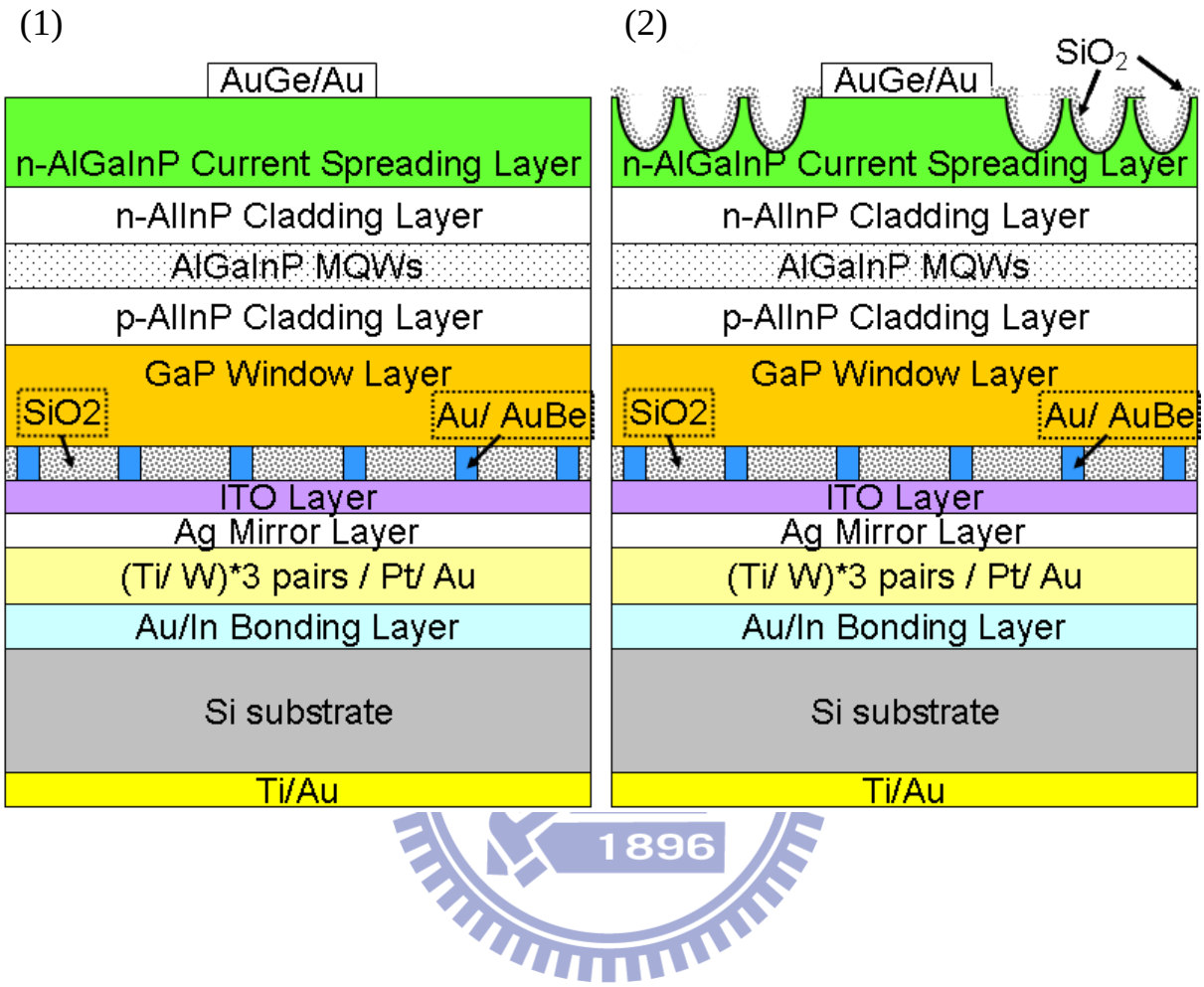


Figure 3.16: Schematic diagrams of the metal bonding AlGaInP-based LEDs (1) The LED-I device structure has a plane surface. (2) The LED-II device has micro-bowls array texture on surface and the LED-III device is added nano-rods texture in moicro-bowls.

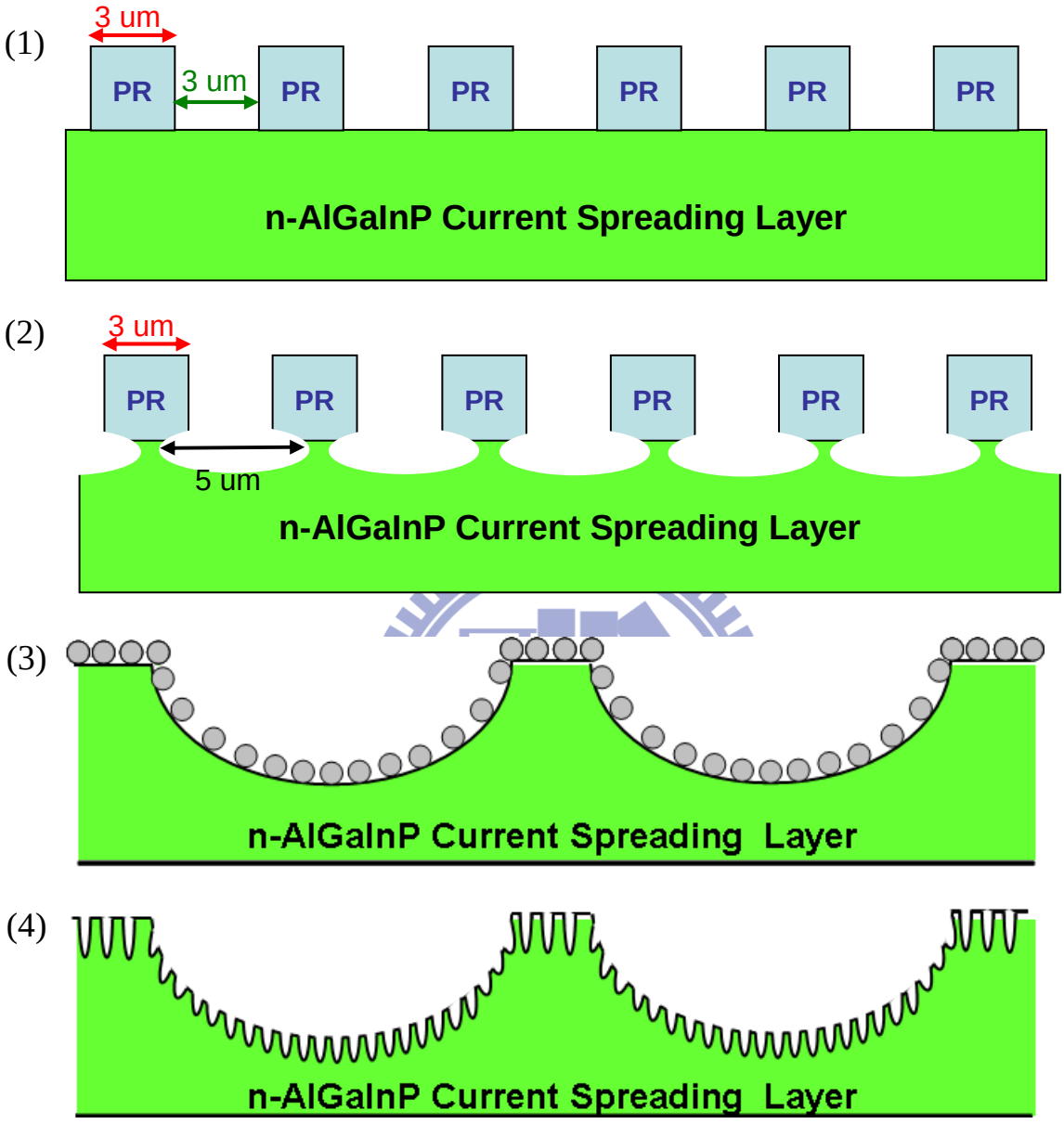


Figure 3.17: Schematic diagrams of (1) Each hard mask dimension and distance of photo resistance dot is 3 μm. (2) After anisotropic wet etching, the 5 μm wide micro-bowls were formed on surface. (3) The silica nano-particles were spin-coated on the wafer surface which has bowl-shaped textured. (4) After dry-etching process, the nano- rods were formed on surface.

`

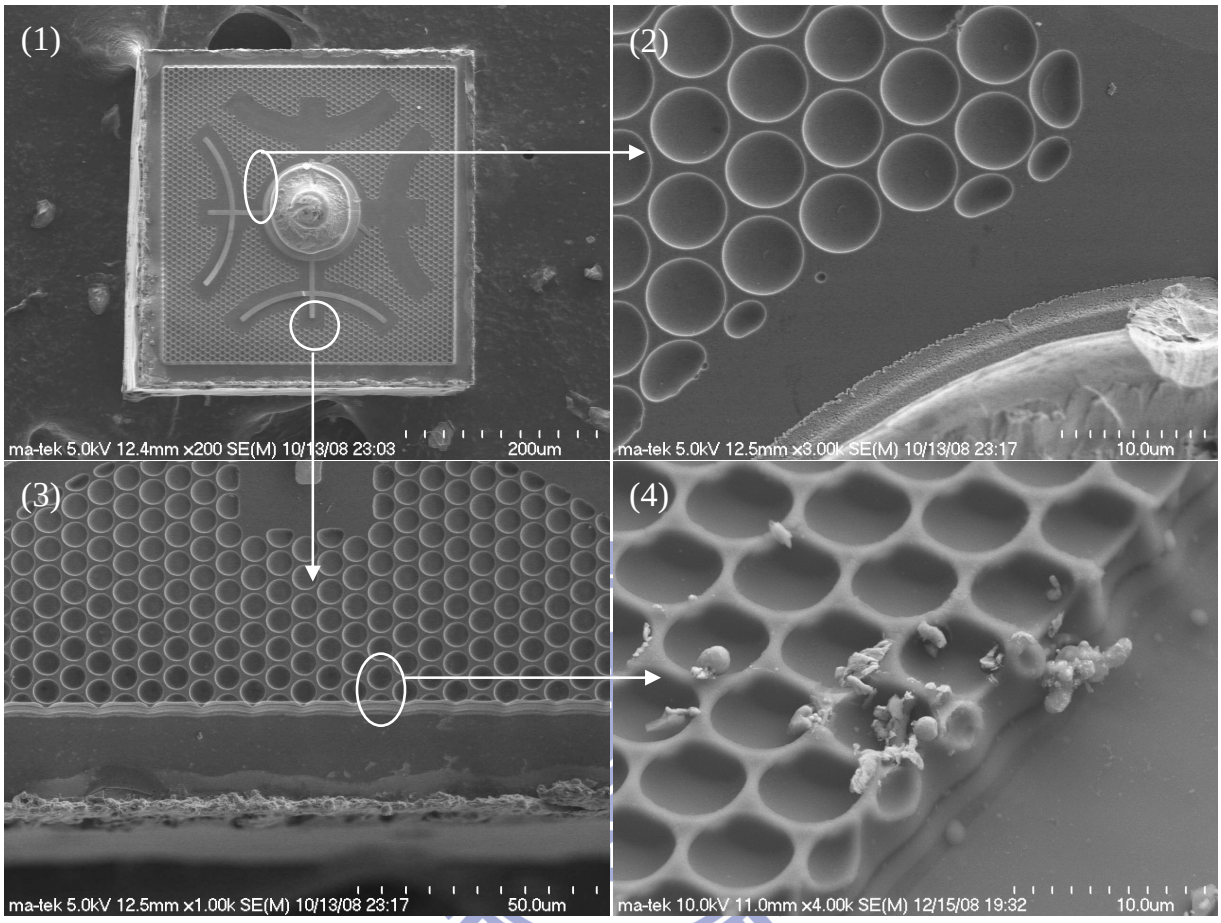


Figure 3.18: SEM figures of (1) The LED-II chip profile. (2) ~ (4) The LED-II surface were covered with micro-bowls.

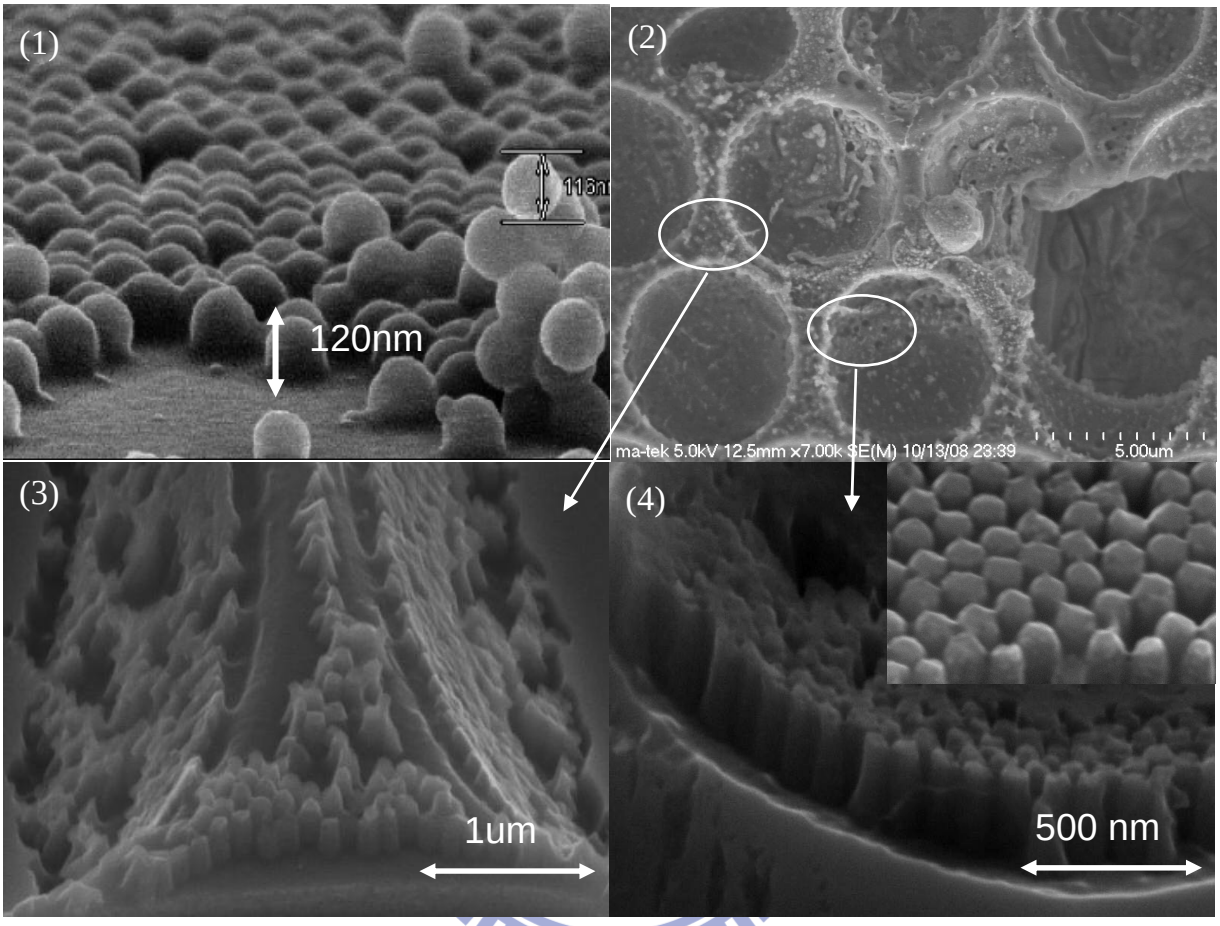


Figure 3.19: SEM figures of (1) The silica nano-particles were spin-coated on wafer surface and sphere diameter is 120 nm. (2) ~ (4) The nano-rods were formed on surface everywhere including bowl bottom, bowl sidewall, and plane surface.

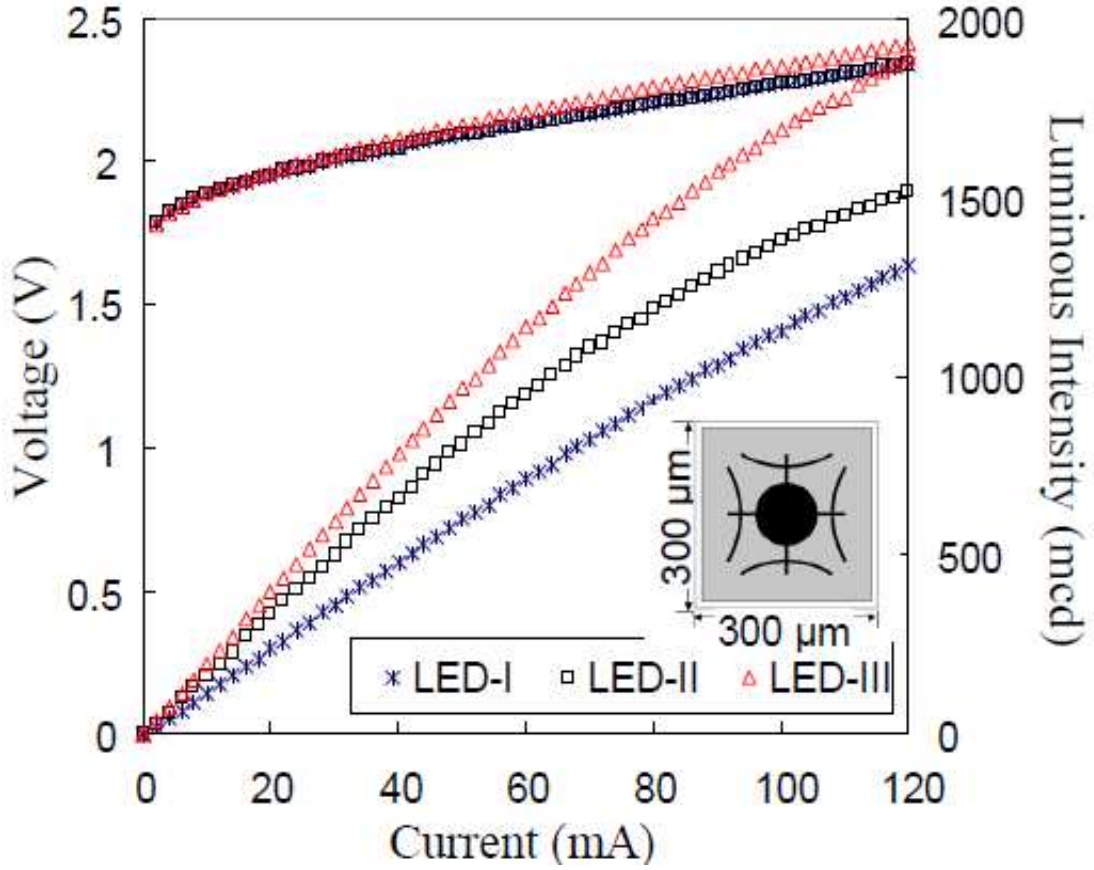


Figure 3.20: The corresponding luminous intensity-current-voltage (L-I-V) characteristics of the LED-I, LED-II, and LED-III.

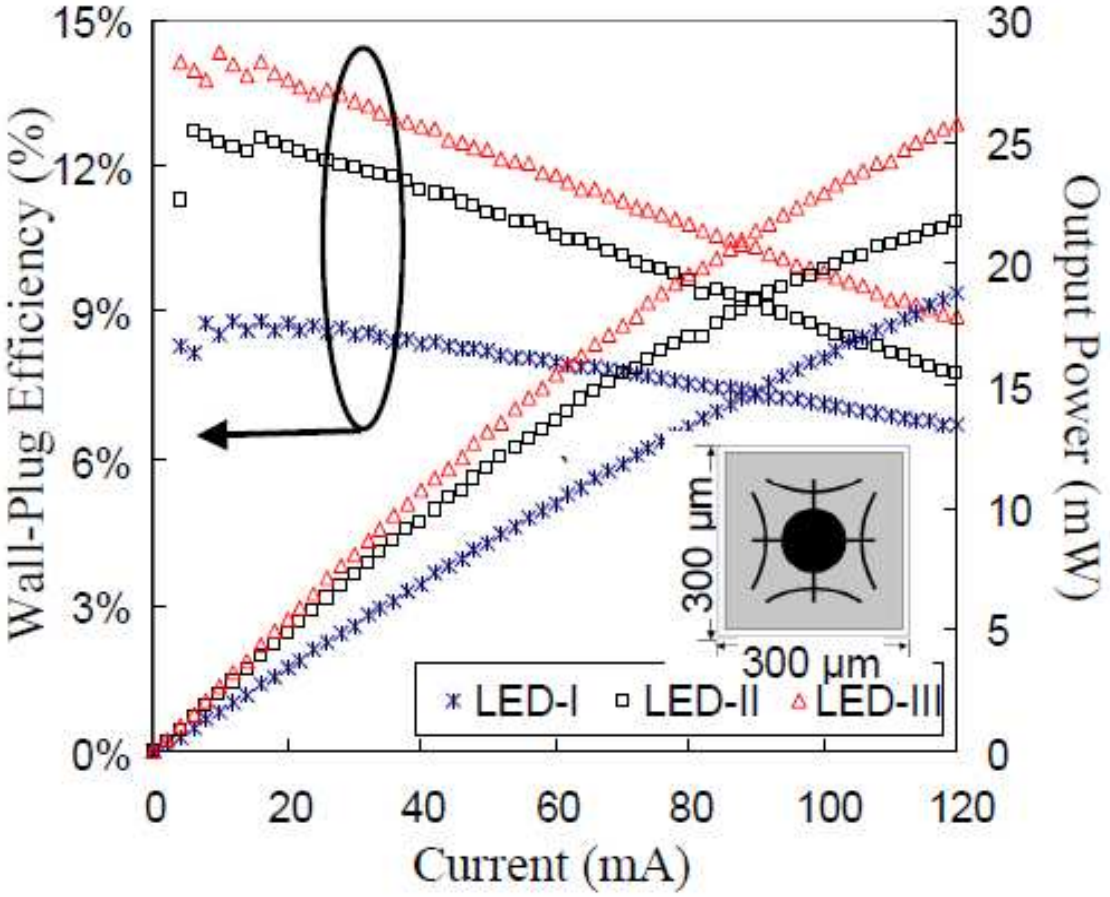


Figure 3.21: The LED-I, LED-II, and LED-III characteristic of the wall-plug efficiency and output power versus current.

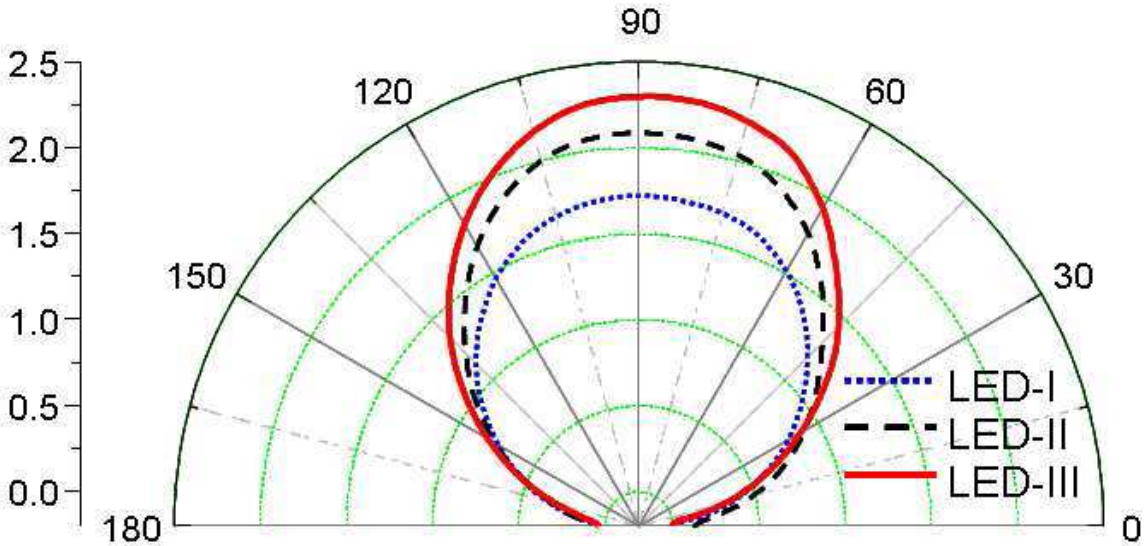


Figure 3.22: The beam patterns of the LED-I, LED-II, and LED-III under 20 mA current injection.

CHAPTER 4

High Performances of InGaN/ GaN Light-Emitting Diodes in Metal Bonding Technique

4.1 Introduction

The III-nitride alloy material of interest for visible spectrum LEDs is $In_xGa_{1-x}N$-based system. This $In_xGa_{1-x}N$ system maintains a direct bandgap across the entire alloy composition range. The key breakthroughs are that the high GaN film grown on an AlN buffer layer [1] and *p*-type GaN in Mg-doped [2]. In the 1980s, the InGaN-based material was ushered in the new applications of GaN-based optoelectronic device development and also led to the realization of high brightness blue, green LEDs and laser diodes in the subsequent decade [3]-[5]. By many years later, there are still several inherent and physical factors which limit the range of useful InGaN-based material. It results form the lack of an InGaN lattice matched substrate (native bulk substrates). So far, the normal used of InGaN-based LEDs epitaxy are lattice mismatched substrate of either c-plane sapphire (Al_2O_3), or silicon carbide (SiC) substrates. The serious lattice mismatch results in very high dislocation density between the InGaN and sapphire (or SiC) substrate. Although having been reduced by improved epitaxial growth techniques from 1×10^{10} cm^{-3} to 1×10^{8} cm^{-3} over the last decade, the dislocation acts as non-radiative recombination center and device degeneration factor in LED or laser diodes [6], [7]. This inherent epitaxy handicap affects the internal quantum efficiency (η_{int}) due to the larger dislocation density in epi-layer structure as compared with the AlGaInP alloy system. Recent years, many techniques were embedded in InGaN/ GaN epi-layer grown on sapphire such as epitaxial lateral overgrowth (ELOG) [8], [9] and patterned sapphire substrate [10]-[13]. Above mentioned is internal quantum efficiency that is most dependent on epitaxy technique and material natural limitation. However, internal quantum efficiency is not only

factor for deciding InGaN-based LEDs performance. The external quantum efficiency (η_{ext}) is the ratio of the number of emitted photons outside the LED device to that of injected electron–hole pairs and is a useful physical parameter to evaluate LEDs performance. It is defined as following:

$$\eta_{ext} = \eta_{\text{int}} \times \eta_{extr}, \tag{4-1}$$

where the extraction efficiency (η_{extr}) is also an important index to determine the most generated photon fall outside escape cones by total internal reflection due to the large refractive index different between GaN and epoxy or air [14]. Thus, many novel techniques were implanted in improving light extraction efficiency such as surface roughness [15]-[17], flip-chip structure [18]-[20], vertical thin film structure via laser lift off (LLO) technique [21]-[24], and thin film flip-chip LEDs [25].

In this chapter, the investigation is focused on enhancing the light extraction, and entire strategies are based on vertical thin film structure by metal bonding technique. As we know, the InGaN-based LEDs which are grown on sapphire substrate have several drawbacks such as non-conductive substrate and lower thermal conductivity (35 W/m-K) as compared wit Si substrate (150 W/m-K). The key issue is difficulty in producing roughness surface due to the innate exitaxy handicap of ultra-thin *p*-GaN cap layer (< 500 nm). Thus, using vertical thin film structure provides an *n*-side up structure, which has a thick *n*-GaN layer on surface (> 4μm) and contributes towards *n*-GaN surface textured processing. Furthermore, the vertical thin film structure is that replacing the poor thermal dispersion sapphire with higher thermal dispersion Si substrate via metal bonding and laser lift-off (LLO) processes. Although the processes of this structure is complex and high cost, vertical GaN thin film LEDs have excellent performances of current crowding free and stable operating under high current injection or high temperature ambient.

4.2 Semi-Vertical InGaN/ GaN Light-Emitting Diodes with Single Electrode-Pad Fabricated on Sapphire Substrate

4.2.1 Introduction

Recently, the wide-bandgap InGaN-based light-emitting diodes (LEDs) have attracted significant attention in many different applications [26]. The InGaN materials are used to develop high performances optical devices [27], and the available substrate for growing InGaN/ GaN materials are GaN, SiC, ZnO, and sapphire substrate. Among these substrates, the sapphire is the best choice for low-cost, mass production, and matures epitaxy technology properties. However, the epi-layer grown on sapphire substrate will be restricted the devices processes and structure, due to the non-conductive sapphire substrate. The lateral structure has less output light area as compared with single electrode pad of vertical structure since the electrode pad were partially occupied the light output area especially in small chip size. In addition, the smaller LEDs chips normally have lower electro-static-discharge (ESD) resistance ability by serious current crowding effect. Finally, two bonding wires requirement for small LED chips is limitation of flexibility package. Recent years, many methods were implanted in order to solve these inherent problems, such as a novel technology of laser lift-off (LLO) was proposed by Wong *et al.* [28]-[31]. This technique promotes GaN-based LEDs with high brightness, high efficiency, high current operation, and thermal stability properties. However, LLO technique has several process issues of high-cost facility system for laser lift-off process, damaging devices issue from laser lift-off process, unstable yield, complex and high cost fabrication procedures, patent issues, and difficult to mass production. Kim *et al.* had published the new method to fabricate vertical GaN-based SEVENS (Sapphire Etched Vertical Electrode Nitride Semiconductor) LEDs chips [32], [33]. The SEVENS LEDs were fabricated by wet-etching from the backside of sapphire substrate until the *n*-GaN contact layer was

exposed, and the schematic structure, microscope and electroluminescence images were shown in figure 4.1. The SEVENS LEDs also have several disadvantages on the devices characteristics and fabrication procedures. The results of electrical properties were unsatisfactory due to the wet-etching depth and uniformity. It is very difficult to control the etching depth without a selective etching stop layer, and the epi-layer could be damaged during the high temperature etching process. Furthermore, in order to expose more *n*-contact area, it is a trade-off between device structure strength and *n*-GaN contact area since the sapphire crystallographic angle. In this article, a novel and simple chip design with single electrode pad (SEP-LEDs) in GaN-based LEDs on sapphire substrate was developed. Details of the electrical and optical characteristics of the novel SEP-LEDs will be reported.

4.2.2 Fabrication of Single Electrode Pad InGaN/ GaN LEDs (SEP-LEDs)

In this study, the GaN-based LEDs were grown on 2˝ diameter c-plane (0001) oriented sapphire substrates using a low-pressure metal-organic chemical vapor deposition (MOCVD) system (Emcore D80). This LED structures with a 470 nm dominant wavelength which consisted of a 30 nm thick buffer layer, a 2 μm thick undoped GaN layer, a 3 μm thick Si-doped *n*-GaN layer, five periods of InGaN/ GaN quantum-well active layer, a 0.2 μm-thick Mg-doped *p*-AlGaN layer, and an Mg-doped p^+-GaN layer. In chip processing, the mesa was defined 160×160 μm^2 by standard photolithography and partial etching by inductively coupled plasma (ICP). Then, the indium-tin-oxide (ITO) film was deposited on *p*-GaN layer by electron-beam (E-beam) system at 300°C chamber as functions of transparent, current spreading and *p*-GaN ohmic layer. The textured ITO having regular 4 ~ 5 μm diameter circles and 2 μm space were fabricated using photolithographic and chemical etching of HCl: H2O (5:1) solution. The corresponding etching depth is approximately 60 nm for enhancing the light extraction [34], [35]. The chip edge was further dry etching until more than 10 μm depth

of sapphire substrate. The purpose of forming this structure is connecting with the n-pad and sidewall more easily, and then a SiO_2 (5000Å) film was deposited on surface and sidewall by E-beam for passivation layer. The Ti/ Al/ Ni/ Au (5 nm/ 200 nm/ 400 nm/ 800 nm) were deposited on *n*-GaN for ohmic contact and *p*-electrode pad (90 μm diameter) on ITO film. At the same time, a high reflective mirror Ti/ Al/ Ni/ Au were also formed on the etched sapphire sidewall. Finally, the processed wafer was subjected to the laser scribed and broken into 180 × 180 μm^2 chips. The chips were separated using expander and each chip space is 300 μm. The expanded chips were flipped and embedded in 1.5 μm thick photo resist and its schematic diagram structure was shown in figure 4.2(a). The flipped chips were transferred to Si wafer, and then the Si wafer was deposited ITO film. After ITO depositing, a conductive current path was formed from chip sidewall to sapphire backside by ITO film. The ITO film was deposited on the sapphire backside and chip sidewall will not only enhance light extraction but also serve as electrical connection between the *n*-GaN layer and chip backside. After that, the expanded chips were transferred to tape again for removing the photo resist using the organic solvent. Finally, single electrode pad GaN-based LEDs (SEP-LEDs) with small chip size was successfully fabricated and the schematic structure diagram was shown in figure 4.2(b). The chips were then bonded on TO-46 with conductive silver-filled glue and without epoxy encapsulation for electrical and optical measurements.

4.2.3 Characteristic of Single Electrode Pad InGaN/ GaN LEDs (SEP-LEDs)

The scanning electron microscope (SEM) image of the SEP-LEDs profile was shown in figure 4.3(a). It's obviously that there is only one electrode pad on chip surface, which is different from the conventional lateral GaN-based LEDs (CL-LEDs). The dimension of SEP-LEDs chip and mesa is 180×180 and 160×160 μm^2, respectively. Figure 4.3(b) shows the detail SEP-LEDs structure and layer. The surface roughness of *p*-GaN and textured ITO layer

were clearly shown in figure 4.3 (c) and (d), respectively. In this study, the surface textured roughness technique was applied to CL-LEDs and SEP-LEDs for enhancing light extraction and reducing internal reflective effect. Furthermore, the surface roughness could enhance probability of emitting light escaping from semiconductor to air (or epoxy). In detail comparisons of CL-LEDs and SEP-LEDs, the chip size (180×180 μm^2) are the same but the SEP-LEDs light emission areas is larger than that of CL-LEDs due to the free of *n*-contact pad. The typical current versus voltage (*I*-*V*) curve was shown in figure 4.4(a). The forward voltage of SEP-LEDs and CL-LEDs under 20 mA current driving is 3.15 and 3.35 V, respectively. The SEP-LEDs presents the lower V_f than that of CL-LEDs, it means that the SEP-LEDs has lower series resistance and better current spreading properties since the special *n*-ohmic contact design was implanted. The SEP-LEDs *n*-contact area is not only circularly covered the chip edge but also covered the sidewall by Ti/ Al/ Ni/ Au. This 3-dimension (3D) ohmic-contact structure is different to the conventional 2-dimension ohmic-contact of CL-LEDs. In other words, the SEP-LEDs have more contact area as compared with CL-LEDs. Figure 4.4 shows the output power and wall-plug efficiency properties of CL-LEDs and SEP-LEDs under various forward current. It is observably observed that the SEP-LEDs have higher output power as compared with the CL-LEDs. The SEP-LEDs and CL-LEDs power under 20 mA forward current is 6.3 mW and 4.3 mW, respectively. Furthermore, the SEP-LEDs exhibits 66.3% wall-plug efficiency enhancement as compared with CL-LEDs at 20mA current injection. The results could be ascribed that the SEP-LEDs has lower series resistance and the larger light emission area. The optical and corresponding electro-luminescence (*EL*) microscope images (at 20 mA) were shown in figure 4.5 (a) and (b). According to the EL intensity image, it is clearly observed the SEP-LEDs presenting an excellent current spreading characteristics. On the contrary, a serious current crowding effect was occurred between the shortest distances of these *p*- and *n*-contact pads of the CL-LEDs.

The current crowding effect will affect device performances such as reduced current injection efficiency, non-uniform lighting area, higher joule heating, and poor reliability issues. In this study, the ESD resistance ability was measured by an Electro-Tech System simulator Model 910. It could provide electrical pulses in the human body model and machine-model. The machine-model applied reverse pulse voltage from 0 V to -1200V for CL-LEDs and SEP-LEDs. Figure 4.6 (a) and (b) shows the I-V characteristics of the SEP-LEDs and the CL-LEDs after a variations reverse pulse voltage injection. According to these figures, both of the leakage current is less than 1 nA at -4V before ESD damaging test. The CL-LEDs curve shows leakage current (larger than 1 μA) after -200 V ESD test, and a deep occurred at 0V after -400V ESD test. This deep of ohmic-like curve indicates that the p-n junction was turn-on (short) after suffering -400V reverse pulse voltage, and the ESD resistance of the CL-LEDs is less than -400V. Furthermore, the leakage current more serious accompany with increasing of reverse pulse voltage. On the contrary, it is clearly that the SEP-LEDs exhibit higher ESD resistance (< -1000V) ability than that of the CL-LEDs due to the uniform current spreading path and the lower series resistance.

4.3 Vertical InGaN/ GaN Light-Emitting Diodes by Metal Bonding Technique

4.3.1 Introduction

Above-mentioned SEP-LEDs is a interesting LED structure, having several properties and advantages such as single electrode pad, more area of light emission and *n*-ohmic contact, uniform current injection (without current crowding effect), high ESD resistance ability, high output power and efficiency, and lower forward voltage. However, SEP-LEDs are suitable applied for small chip and low output power applications due to the poor thermal conductivity sapphire substrate. In future LED marketing and applications, the LED should be provided with high output power, high efficiency under higher current density, temperature insensitivity operating, and high reliability property. The SEP-LEDs structure can not be used in future LED application since these LED performance demands could not be achieved on InGaN epi-layer growing on sapphire substrate. In other words, the InGaN epi-layer must be transferred to a high thermal conductivity substrate such as silicon or copper substrate in LED lighting application. In following investigation, the sapphire substrate was replaced with a high thermal conductivity silicon substrate by metal-bonding and laser lift-off (LLO) technique. The InGaN epi-wafer transferred to Si substrate has several advantages including above-mentioned performances of SEP-LEDs. Therefore, this InGaN/ GaN device structure of vertical thin film LEDs (VTF-LEDs) is an important tread toward future LED lighting application. This chapter will be based on the VTF-LEDs technique and discussed performances of various wavelengths, surface roughness textured method, and modified chip processes.

4.3.2 Fabrication of Vertical Thin Film InGaN/ GaN LEDs (VTF-LEDs)

In this chapter, we will discuss the VTF-LEDs characteristic of cyan (505nm) and blue

(460nm) wavelength by metal-bonding and laser-lift off technique. Furthermore, the optimized VTF-LEDs process will also be presented in following discussion. The chip process of VTF-LEDs is very difficult, complicated, and critical although many groups have been involving in this research in recent years. This study the LED wafers were grown on c-plane sapphire substrate by Thomas Swan Close Coupled Showerhead (CCS) reactor system, which has 19x2 inch capacity. The cyan epi-layer structure with a 505 nm dominated wavelength is composed of a 30 nm GaN low temperature buffer layer, a 4 μm light Si-doped *n*-GaN layer having a lower 4×10^{-18} cm^{-3} carrier concentration, a 2 μm heavy Si-doped *n*-GaN layer having a over 1×10^{-19} cm^{-3} carrier concentration, a ten-period un-doped $In_xGa_{1-x}N$/ GaN MQWs structure, a 50 nm Mg-doped *p*-AlGaN layer, and a 100 nm Mg-doped *p*-GaN cap layer. The blue epi-layer structure with a 460 nm dominated wavelength is almost similar to above mentioned cyan structure expect MQWs indium composition and thickness.

In detail optimized VTF-LEDs chip process, the wafer was submitted to standard clean process before O&R (Ohmic and Reflector) metal film deposited on wafer surface. The O&R film is functions for *p*-GaN ohmic and high reflector. Figure 4.7 (a) shows the O&R metal film of Al/ Ag/ Ni/ Au was respectively deposited on *p*-GaN surface and then load into 500ºC furnace for 30min. After 2nd photolithography, a Ti/ W (2pairs)/ Ti /Au cap metal layers were deposited on O&R film by sputter system and then the wafer was also submitted to thermal treatment in 300 ºC furnace as shown in figure 4.7 (b). In VTF-LEDs chip process, releasing internal stress is an important key issue due to the lattice mismatch between sapphire and InGaN/ GaN epi-layer. Normally, this inherent internal stress should affect yield and performances directly during laser-lift off and undoped GaN removed process. In order to decrease internal stress effect, the wafer was submitted to laser cut for decreasing internal stress effect, due to the die form has less stress releasing as compared with wafer form during laser lift of process. The laser cut depth and width is 20 and 2.5 μm, respectively. As shown in

figure 4.7 (c), the cut area provided for releasing stress and conducing yield enhancement. A 1 μm SiO_2 film was deposited on surface by PECVD, and the patterned SiO_2 was formed after photolithography and chemical etching process as shown in figure 4.7(d). SiO2 film was taken as an etching stop layer during *n*-GaN mesa dry etching. Figure 4.7(e) shows that the barrier metal layers Ti/ W/ Ti/ Ni/ Au and bonding metal layers Ti/ Pt/ Au (B&B metal layers) were sequentially deposited on surface. The metal layers of Ti/ Pt/ Au/ In were successively deposited on a Si substrate for ohmic contact and metal bonding process, as shown in figure 4.7(f). Figure 4.7(g) presents the wafer binding process, the epi-wafer was flipped and bonded to the Si substrate, and then the wafer pairs were loaded into 220°C oven for 2 hours. After wafer bonding process, the bonded structure was subjected to LLO process to form a u-GaN/ *n*-GaN/ MQWs/ *p*-GaN/ metal layers/ Si substrate structure by QMC ELMS-1000 laser lift-off system, as shown in figure 4.7(h). The KrF excimer laser (Lambda Physick LPX200) in QMC ELMS-1000 system, having a 248nm wavelength and 25 ns pulse width was used to separate sapphire substrate. Furthermore, the laser beam with a size of 1.2mm × 1.2mm was incident from the polished sapphire substrate backside into interface of sapphire-GaN buffer to decompose the GaN into Ga and nitrogen. This incident laser flux was set a value approximately 700 mJ/cm^2. The wafer surface has remained Ga byproduct after the whole GaN epi-layer was transferred to Si substrate by LLO process. After wafer pair was immersed into the 70ºC chemical solution of dilute hydrochloric acid, the remained Ga byproduct was removed and shown in figure 4.7 (i). Figure 4.7 (j) shows that the 4 μm un-doped GaN (u-GaN) was removed by inductively coupled plasma reactive ion etching (ICP-RIE of OXFORD Plasmalab 100) until *n*-GaN was exposed. The 6 μm thick photo resist as a function of hard mask for mesa dry etching process was defined under standard photolithography. The wafer was subjected to 2 μm thick *n*-GaN layer dry etching until SiO_2 etching stop layer was exposed, as shown in figure 4.7 (k). In order to enhance the light extraction efficiency, the

rough surface is an important process in VTF-LEDs especially. Before surface roughness process, a 1μm thick SiN_x was grown on wafer surface for hard mask of roughness process by PECVD, as shown in figure 4.7 (l). After photolithography and hydrofluoric acid chemical etching, the *n*-electrode pad and metal mesh line area were covered with SiN_x film except roughed area. Before surface roughness process, the wafer was submitted to surface pre-clean for removing native oxide by hydrochloric acid. Subsequently, the wafer was immersed into a 95ºC and 2 mole concentration KOH solution for 4 min. The wafer surface was suffered chemical wet etching of KOH solution, a random roughness surface was formed on N-face GaN layer and the schematic diagram was shown in figure 4.7 (m). Continually, partial area for *n*-electrode metal pad and metal mesh line which has SiN_x film protected was removed by a standard photolithography and hydrofluoric acid. Figure 4.7 (n) presents that the Cr/ Au (30 nm/ 2000nm) metal layers were selectively formed on wafer surface for *n*-ohmic contact, and then the wafer was subjected to thermal treatment under 280 ºC in nitrogen ambience for 20 min. The wafer of Si substrate was subjected to thin by grinding, and then the Ti/ Au (10nm/ 300nm) were deposited on backside of Si substrate for *p*-type Si substrate Ohmic contact. After all of the chip processes were finished, the VTF-LEDs wafer was submitted to laser scribed into 1200 μm×1200 μm and chip break. Devices were packaged on TO-46 form in this investigation, and the electrical and optical properties were measured using the Instrument System CAS140CT array spectra-meter system.

4.3.3 Characteristic of Vertical Tthin Film InGaN/ GaN LEDs (VTF-LEDs)

Figure 4.8 (a) shows that the chip profile of VTF-LEDs and the chip size is 1200 μm×1200 μm. The current spreading performance in VTF-LEDs metal mesh line design is shown in figure 4.8 (b), and two pad was designed for high current injection. The tilted cross-section electroluminescent (EL) image of green and blue VTF-LEDs are respectively

shown in figure 4.8 (c) and (d). It observably observed that the most radiate light is from device surface, which is different to lateral radiation of conversional sapphire base InGaN LEDs. The laser lift-off in VTF-LEDs chip process is a key point effecting device performances and final yield, and the principle cause is the internal stress between epi-layer and sapphire. It is very important to release internal stress before LLO. Therefore, a concept of previous fabrication trench by JPSA 266nm laser cut system before LLO was implemented in this study. Figure 4.9 shows the wafer surface profile after suffering LLO process, (a) and (b) is having previous laser cut process and without it, respectively. It is clearly observed that this previous fabrication trench could improve the epi-layer damage in LLO process. In other words, the laser cut trench provides a buffer for stress releasing and avoids epi-layer crack from LLO process. In order to develop high performances VTF-LEDs, the high quality ohmic and reflector (O&R) metal layers selection, which were directly deposited on *p*-GaN, is extremely critical. The requirements of O&R metal property are low contact resistance, thermal stability, high reflectivity, and better adhesion ability for *p*-GaN. In general, silver (Ag) reflectors have been widely used for GaN-based LEDs [36]-[40]. Sliver is highly reflective at visible wavelengths and it has reasonable Ohmic behavior. However, the Ag reflector mirror decreases rapidly after the annealing process due to surface agglomeration [37]. Chou *et al.* had presented this contention, Ni (5 nm)/ Ag (150nm) metal layer was deposited on *p*-GaN surface and then submitted to different thermal treatment. The sliver agglomeration variations on *p*-GaN surface under different thermal alloy were shown in figure 4.10. According to this result, selecting a suitable metal with high reflectance and lower contact resistance for *p*-GaN is the first assignment in VTF-LEDs. In this investigation, we selected several possible metal compositions, such as Ni/ Ag (10Å/ 1.2kÅ), Ni/ Ag/ Ni (10Å/ 1.2kÅ/ 500Å), Ni/ Al/ Ti/ Au (10Å/ 1kÅ/ 200Å/ 800Å), and Al/ Ag/ Ni/ Au (50Å/ 1.2kÅ/ 50Å/ 50Å).The O&R metal reflectivity of these various composition under different alloy

temperature were shown in figure 4.11. In pre-alloy data, it was clearly observed that Ni/ Ag / Ni composition has the highest reflectivity (87.3%) and Al/ Ag/ Ni / Au composition is the lowest (72%) at 460nm wavelength. After thermal treatment, reflectivity in most composition is degeneration expect Al/ Ag /Ni/ Au composition. Chou *et al.* had similarly illustrated this phenomenon by X-ray photoelectron spectroscopy (XPS) analysis. The analysis of atomic depth profile was performed on *p*-GaN/ Ni/ Ag and *p*-GaN /Ni/ Al/ Ag before and after thermal treatment at 500°C for 10 min, as shown in figure 4.11. Comparing figure 4.12 (a) and (b), it is observed that a serious inter diffusion occurred at interface between *p*-GaN and Ni/ Ag. After 500°C annealing, Ag atoms diffused into *p*-GaN cap layer. Figure 4.12 (c) is that an Al-rich layer exist near *p*-GaN interface for the as-deposition. After thermal annealing, as shown in figure 4.11 (d), basically the entire atomic profile has no change much. Therefore, a model could explain this Al /Ag / Ni /Au composition properties of higher reflectivity after thermal treatment and high thermal stable in this investigation. The schematic diagram of this theory model was shown in figure 4.13 (a). After an ultra thin Al (50Å) and Ag (1.2KÅ) was successively deposited on *p*-GaN, the ultra thin Al appeared island profile on *p*-GaN surface. Moreover, fewer Al atoms shallowly diffused in *p*-GaN layer and Ag is also not a smooth surface for reflector. Therefore, this agglomeration metal layer can not provider a good plane surface as a function of high reflective mirror, and it results in the lowest reflectivity in above mentioned reflector composition. Figure 4.13 (c) shows the sliver and aluminum phase diagram, Ag and Al atoms have eutectic point at 728K (455°C), and Ag-Al alloy metal was formed after 455°C thermal annealing. Sliver atoms will alloy with aluminum atoms to become AgAl alloy metal layer while the annealing temperature was higher than eutectic temperature point. During AlAg eutectic processing, sliver will trap the aluminum atoms, which were diffusing into *p*-GaN layer. It is contributive enhancing the reflectivity due to the poor reflector of island aluminum; moreover, AlAg alloy layer has a function of a barrier

layer which could avoid sliver atoms diffusing in *p*-GaN by temperature. In other words, AlAg alloy layer provided several functions of good adhesion, high thermal stability, barrier layer, and higher reflective mirror. AlAg alloy also provided a better Ohmic contact property than Al layer; due to Al has lower work function (Φ_{Al}=4.26eV) than Ag (Φ_{Ag}=4.74eV). Figure 4.14 shows that the O&R layer (Al/ Ag/ Ni/ Au) I-V characteristic of as-deposition and after thermal treatment. It was found that a Schottky characteristic curve was appeared in as-deposition, and Ohmic contact was formed after eutectic process. It was illustrated that Al at was diffused in *p*-GaN and the most Ohmic contact for *p*-GaN after as-deposition. After thermal annealing, Ag atoms could trap diffused Al atoms and then AlAg alloy provided a higher work function which was similar to Ag. Briefly, AlAg alloy not only provides a thermal sable high reflective mirror but also approaches an Ohmic contact for *p*-GaN. According to above opinion, the O&R layer composition of Al/ Ag/ Ni/ Au was implanted in this investigation, but it still need to optimize. The effects of aluminum thickness in O&R are totally reflectivity, transparency, and *p*-GaN Ohmic contact. For this reason, several various aluminum thickness conditions (10Å, 50Å, 100Å, 200Å) based on Al/ Ag/ Ni/ Au composition were executed in this experiment. Figure 4.15 (a) shows I-V curve of various aluminum thicknesses after 500ºC thermal annealing. The 50Å aluminum thickness had the lowest contact resistance, and 200Å conditions appeared Schottky characteristic. It was proved that more aluminum contacting with *p*-GaN could increase contact resistance due to aluminum with lower work function than silver. The contact resistance should be increased by aluminum thickness. Figure 4.15 (b) shows reflectivity of various aluminum after 500ºC thermal annealing. The reflectivity enhancement at 455nm between O&R as-deposition and after annealing was also presented in this figure. According to this figure, 50Å aluminum thickness had the highest reflectively than others. The optical function of aluminum and silver layer is a transparent and reflective metal film, respectively. The requirement of aluminum

layer is higher transparency; in other words, ultra-thin aluminum layer was required. It was verified that the reflectivity was enhanced by decreasing aluminum thickness. Above mentioned is that the O&R layer of Al-Ag based composition has higher reflectively after thermal annealing. According to the reflectively enhancement between before and after annealing, it was clearly observed that the variation was also enhanced by decreasing aluminum thickness. But reflectively variation of 10Å aluminum was decreased after 500ºC thermal annealing. It could be attributed to the silver agglomerative phenomenon under high temperature annealing. The agglomerative phenomenon shall result in a weak adhesion due to less stable AlAg eutectic layer at *p*-GaN interface.

In addition, the investigation of *n*-type ohmic contact in VTF-LEDs structure is an important issue, which is different to the conventional sapphire based InGaN LEDs. Generally, both *n*-type and *p*-type ohmic contact were formed on the Ga-face surface of GaN (0001) on sapphire but *n*-type ohmic contact would be formed on the N-face surface of GaN wafer $(000\bar{1})$ for the fabrication of the VTF-LEDs structure. Freestanding GaN wafer has a wurtzite crystal structure which has two different polarities along the c-axis direction, (0001) Ga-face and $(000\bar{1})$ N-face, respectively. The (0001) Ga-face surface is composed of three nitrogen dangling bonds which each point upward the c-plane surface, while $(000\bar{1})$ N-face surface has a single nitrogen dangling bond that points upward [36][37]. Figure 4.16 shows that the schematic of GaN wurtzite crystal structure exhibiting the polarity along the c-axis. The small and large spheres indicated Ga and N, respectively. GaN has Ga-face (0001) polarity on left side and right side is N-face $(000\bar{1})$ polarity. When the direction of the three bonds of the III-element is towards the substrate, the polar structure is defended as Ga-face polarity. On the other hand, when that of the bonds is upward against substrate, it is defined as having N-face polarity. This difference in surface structure affects the device characteristics, especially ohmic contact properties. Karrer *et al.* reported that the crystal polarity of the GaN surface

affects the Schottky barrier height by band bending of conduction and valence bands [38]. Kwak *et al.* also investigated the dependence of ohmic contact property on both Ga- and N-face surfaces of *n*-type GaN and showed the difficulty of achieving ohmic contact on N-face surface of *n*-type GaN [39]. In this study of ohmic contact on N-face, the specific contact resistance was measured by transfer length method (TLM), and the TLM patterns were fabricated by the standard photolithography. TLM patterns which have seven of 100×200 μm^2 rectangular pads with 5, 10, 15, 20, 30, 40, 60, 80, and 100 μm gap spacing were defined. There are few literatures had mentioned relative metal composition applied for N-face *n*-GaN ohmic contact [40] [41]. The mechanics of metal bonding in VTF-LEDs is that using In and Au composition forms $AuIn_2$ alloy under 220°C thermal treatment. All of the subsequent processes temperature should be lower 400°C since In would be separated from $AuIn_2$ alloy. Firstly, Pd/ Ti/ Al (50Å /300Å /5000Å) and Cr /Au (300Å /5000Å) compositions were applied to ohmic contact on N-face *n*-GaN, which has a 5×10^{18} cm^{-3} normal carrier concentrations. Figure 4.17 (a) shows that the I-V curves of Pd/ Ti/ Al and Cr/ Au composition which were deposited on N-face *n*-GaN surface. Although Pd has higher work function (Φ_{Pd}=5.0eV) than Cr (Φ_{Cr}=4.4eV), it seems that Cr/ Au has better ohmic contact characteristic than Pd/ Ti/ Al. Jang *et al.* had mentioned that the first 50Å of Pd layer remained smooth at as-deposition state and no reaction between the Pd and GaN was detected [40]. After annealing at 450°C, Pd-gallium alloy compounds (Ga_xPd_y) were precipitated at the grain boundaries of Ti–Al alloy compounds. It is not insufficient for forming Ga_xPd_y after Pd was suffered 370°C thermal treatment. Besides, Cr/ Au composition presented similar ohmic contact curves after deposition and thermal annealing. In order to achieve ohmic contact on N-face *n*-GaN surface, 1×10^{19} cm^{-3} carrier concentrations heavily doped was applied in *n*-GaN layer. Increasing carrier concentration is contributive to decrease barrier between metal and N-face surface of *n*-GaN, and the I-V performances were shown in figure 4.17 (b).

According to this I-V curve, Pd/ Ti/ Al were still appeared Schottky characteristic due to the insufficient thermal treatment. Nevertheless, Cr/ Au were achieved lower ohmic contact on N-face surface of *n*-GaN as compared with 5×10^{18} cm^{-3} normal carrier concentrations. The improvement could be attributed to heavily doping on *n*-GaN. Beside, the wafer cleaning conditions before metal deposition is another solution which could reduce ohmic contact barrier high issue. Subsequently, the electrical performances of Cr /Au deposited on 1×10^{19} cm^{-3} N-face surface of *n*-GaN, under different surface cleaning method and thermal annealing conditions will be illustrated as following. Figure 4.18 (a) shows Ga-face and N-face ohmic contact behavior under various temperature annealing. Before Cr/ Au deposited on Ga-face and N-face, the samples were immersed in dilute hydrochloric acid (10%) solution for 3 minute. The specific contact resistance (ρ_c) of Ga-face and N-face without thermal annealing is 2.42×10^{-5} Ω-cm^2 and 2.54×10^{-4} Ω-cm^2, respectively, and Ga-face appeared still lower contact barrier than N-face. The N-face was maintained ohmic contact behavior before annealing temperature is lower 250°C. While annealing temperature is over 250°C, the ohmic contact behavior became semi-ohmic and then to Schottky characteristic. This phenomenon is attributed to the diffusion process of Au in Cr/ Au to the *n*-GaN interface, resulting in raising the barrier height at interface. However, the ohmic contact behavior of Ga-face is almost appeared stable state under various annealing temperature. In order to decrease barrier height and achieve Ga-face performance, a higher concentration hydrochloric acid having 50% dilute was implanted in wafer cleaning process. Figure 4.18 (b) presented that ohmic contact behavior of N-face and Ga-face under 250°C thermal annealing for various time. According to this figure, 50% hydrochloric acid cleaning has lower ρ_c (9.71×10^{-5} Ω-cm^2) than 10% (2.54×10^{-4} Ω-cm^2)one at as-deposition state. After u-GaN layer was removed by ICP system, many nitrogen vacancies were existed on *n*-GaN surface. The nitrogen vacancies were contributed to increase surface carrier concentration and reduce the barrier height between

metal and *n*-GaN. Moreover, the nitrogen were released and gallium were remained on surface after u-GaN removed by ICP. The gallium atoms could easily provide Cr/ Au to form an ohmic contact interface. However, the gallium atoms are not a stable metal layer on surface, and these gallium atoms should be recombined with nitrogen vacancy. As the annealing temperature was increased, the ohmic contact behavior should be transferred into Schottky contact due to gallium recombination. Using dilute hydrochloric acid to remove surface gallium atoms should avoid unstable electrical characteristic of device in high temperature or high current injection operating. It was observably observed that the N-face after 50% hydrochloric acid etching has a stable behavior at longer annealing time, due to the most of gallium atoms were removed and less recombination.

In order to emphasize VTF-LEDs advantages, a conventional sapphire-basee InGaN LEDs (CL-LEDs), having a similar chip size was compared with VTF-LEDs. Figure 4.19 (a) is I-V characteristic of VTF-LEDs and CL-LEDs, and the chip profile and current spreading performance were also appeared in figure. The forward voltage of VTF-LEDs and CL-LEDs is normally 3.32 and 3,276 V, respectively. The lumen intensity versus injection current curve was shown in figure 4.19 (b). The lumen intensity of VTF-LEDs and CL-LEDs under 350 mA and 1 A current injection is 84.92 and 50.15 lm, 127.58 and 66.98 lm, respectively. The VTF-LEDs is 1.7 times lumen intensity of CL-LEDs under 350 mA current operating. Actually, both of the chip size is similar but the real effective radiation area is large different, due to VTF-LEDs has only two electrode-pads and without mesa area. The device effective radiation area of VTF-LEDs and CL-LEDs is 1.4 and 0.96 mm^2, and the current density versus lumen intensity characteristic was shown in figure 4.20. Under a 350 $mA \cdot cm^{-2}$ current density operating, the lumen intensity of VTF-LEDs and CL-LEDs is 101.59 and 48.72 lm, respectively. The VTF-LEDs is 2.1 times lumen intensity of CL-LEDs at 350 $mA \cdot cm^{-2}$ current density operating. It was clearly illustrated that VTF-LEDs provided higher radiation

efficiency as compared with CL-LEDs. It was resulted from VTF-LEDs with a high thermal conductive substrate of Si, and Si substrate could improve the CL-LEDs inherent drawback of device degenerated in high current injection. The spectrum characteristic of VTF-LEDs and CL-LEDs were submitted 350 mA in 0°C, 20°C, 60°C, and 120°C ambience, as shown in figure 4.21 (a). In following measurement, both of the package form is TO-46 and each measurement cycle is 2 msec. From 0°C to 120°C ambience, the dominated wavelength variation (ΔWd) of VTF-LEDs and CL-LEDs is 5 nm and 10nm, respectively. The VTF-LEDs has higher temperature stable ability as compared with CL-LEDs, in other words, VTF-LEDs provided a temperature more insensitively ability. Figure 4.21(b) was appeared the dominated wavelength variation (ΔWd) of VTF-LEDs, which were submitted to various current injections of 350, 500, 700, and 1000 mA in room temperature. The VTF-LEDs dominated wavelength variation of an injection current from 350 mA to 500 mA, 350 mA to 700 mA, and 350 mA to 1A is 3 nm, 4 nm, and 5 nm, respectively. According to above mentioned, the VTF-LEDs provided fewer spectra variation in high temperature or high current injection, and it should be suitable applied for advanced applications as compared with conventional sapphire substrate InGaN LEDs.

Enhancing light extraction efficiency in VTF-LEDs structure is an important issue, due to the over 95% radiation light is coming from device surface. However, the large refractive index different between GaN (n~2.5) and air (n=1), and the critical angle for light extraction is only around 23 degree. In this study, chemical etching method for surface roughness process was applied on N-face of *n*-GaN suface, having 2 μm heavy Si-doped thickness and over 1×10^{-19} cm^{-3} carrier concentration. Dilute and heating potassium hydroxide (KOH) solution was applied for N-face of *n*-GaN surface roughness process. Subsequently, the etching depth and surface morphology was systematically studied as a function of times and concentration. Figure 4.22 shows SEM images of etching surface morphology after

immerging in 85ºC 1M KOH chemical for (a) (b) 5min, (c) (d) 6min, (e) (f) 7min, and (g) (h) 8min. SEM images shown in (a) and (b) were inclined and cross-section direction view. The figures highlight the cone-like surface morphology of the etched N-face GaN. The height of cones were approximately 4000~5000Å, and the density of cones were measured to be 10^8~10^9 cm^{-2} after 5min etching time, in addition, each cone size was approximation. After etching time of 6min (c) and (d), the highest cones were around 6500~7500Å. The top of cone was slightly turned into sharp, and each cone size was not like. The highest cone was around 8000~9500Å as shown in (e) and (f) while sample was immerged into KOH chemical for 7min. It was clearly observed that each cone size difference was increased and the density of cones was decreased as compared to etching time of 6min. The cones height were more and more high with etching time of 9min as shown in (g) and (h), and the height of cones were around 10000~11000Å. However, the bases of most cones were stopped at the same level, and the difference of cone height was also increased with etching time. Therefore, the cones density was decreased and cones height difference was increased with increasing etching time. Systematic variation of increasing the KOH concentration to 2M and temperature of KOH chemical were also carried out. Figure 4.23 shows SEM images of etching surface morphology after immerging in (a) (b) 65ºC and (c) (d) 95ºC 2M KOH chemical for 5min. After 2M 65ºC KOH for 5min, the highest cones were around 2500~3500Å. The top of each cone was not sharp as compared to 1M KOH, and each cone top was appeared flat. While the chemical temperature was achieving to 95ºC, the cone height was around 5500~6500Å. After this condition of KOH etching, the cones top were not flat any more and many nano-pillars were existed on top. It was clearly observed that the cons profile were not hexagonal pyramids symmetry and sharp top. It could be attributed to isotropic-like chemical etching and without lattice selective direction, due to the higher concentration and higher temperature KOH etching chemical. Moreover, each cone size was approximation after 2M KOH etching.

It is evident that with an increasing etching time, there is a trade-off between the size and density of hexagonal cones. In 1M KOH and varied etching time experiments, the longer etching times result in larger cones sizes but a lower cone density. Figure 4.24 shows that the hexagonal cones height and light intensity as function of the KOH chemical condition. The lowest light intensity was appeared on plane surface, having no surface textured on surface. The chemical condition of 85ºC 1M KOH for 7min has the brightest light intensity, and the cones height was approached to 8000~9500Å, as shown in figure 4.22 (e) and (f). The condition of 8 min etching time has lower light intensity than 7min one although it has the highest cones height. It was attributed to cone density and size variation. Compared with 8 min etching condition, the 7min one has higher cones density and less each cone size variation. Attempts were made to improve the light extraction efficiency of VTF-LEDs by using optimized surface textures. In other words, the factors of optimized surface textures were hexagonal cones profile as height, density, and shape.

The VTF-LEDs performances of maximum junction temperature (Tj_{max}) and thermal impedance (R_{th}) were essential to estimated advantage. In junction temperature analysis and measurement, the VTF-LEDs and CL-LEDs were operated at 0.1 mA and measured forward voltage under varied ambient temperature (20°C to 150°C), as shown in figure 4.25. The function of 0.1mA current injection is that lower current injection could avoid junction heating from current injection. The forward voltage would be decreased with ambient temperature (junction temperature), and the maximum junction temperature is forward voltage without varying with temperature. Therefore, the maximum junction temperature of CL-LEDs and VTF-LEDs is 120°C and 150°C, respectively. It could be proved that VTF-LEDs are more suitable for higher ambient temperature and higher current operating as compared with sapphire-based CL-LEDs. The thermal impedance is also an important factor to evaluate the device performance and package ability. Both CL-LEDs and VTF-LEDs were also used the

same TO-46 form to package in order to rid of heating from package issue. The thermal impedance $R_{th(j\text{-}c)}$ was defined as following:

$$R_{th(j-a)} = (T_J - T_A) / P_D , \quad (4\text{-}2)$$

where the $R_{th(j\text{-}c)}$ is thermal impedance (°C/W) of device junction to ambient temperature. The T_J, T_A, and P_D mean that junction temperature of device under test, ambient temperature, and device power dissipation, respectively. In thermal impedance calculation, the CL-LEDs and VTF-LEDs were submitted to a special current generator which has a cycle of an appointed injection current for 99.9 ms and then injected a 0.1 mA current for 0.1 msec. The purpose of injecting an appointed current for 99.9 ms is a function of heating device, and then measured a forward voltage under a 0.1mA current operating. The T_J was obtained after forward voltage (at 0.1mA) was matched to figure 4.25. Under 350 and 700 mA current injection, the forward voltage of CL-LEDs and VTF-LEDs is 2.22V and 2.06V, 2.25V and 2.20V, respectively. Consequently, the T_J (at 350 mA and 700 mA) of CL-LEDs and VTF-LEDs is 70°C and 110°C, 50°C and 80°C, respectively. Furthermore, the maximum thermal impedance was also defined as following:

$$R_{th(\max)} = (T_{J(\max)} - T_A) / P_{D(\max)} , \quad (4\text{-}3)$$

The maximum junction of CL-LEDs and VTF-LEDs is 120°C and 150°C, respectively, and the maximum power dissipation is 2.36 W and 5.71 W. According to Eq. (4-3), the maximum thermal impedance of CL-LEDs and VTF-LEDs was obtained 40.14 °C/W and 21.91 °C/W, respectively. In other words, the VTF-LEDs structure could reduce 20°C device temperature from junction heating under per watt operating due to the high thermal dispersion Si substrate. Figure 4.26 shows that the four VTF-LEDs reliability characteristic under 350 mA and room temperature operation, and each variation of voltage and power over 1800 hours was respectively shown in figure 4.26 (a) and (b). The voltage variation has 10% rising over 1800 hours test. The plus or minus 5% power variation was achieved over 1800 hours, and the

variation was stable after 500 hours test. The excellent VTF-LEDs reliability could be attributed to the stable metal composition and high dispersion Si substrate.

4.4 Summary

In this chapter, the InGaN/ GaN LEDs efficiency was enhanced by metal bonding, laser lift-off, and surface roughness technique. The conventional InGaN/ GaN LEDs with non-conductive and poor thermal conductivity property of sapphire substrate were replaced with Si substrate. This structure is different to conventional lateral structure, which the *p*- and *n*-electrode pad were existed at devices surface. Therefore, this structure had many inherent limitations and lower efficiency as compared with vertical structure.

Firstly, a novel and simple structure of single electrode pad (SEP-LEDs) in GaN-based LEDs was demonstrated. The concept was come from laser diode process of face coating. The ITO film was deposited on SEP-LEDs sidewall, and then a conductive current path was formed from chip sidewall to sapphire backside by ITO film. The SEP-LEDs has more mesa area for light output and uniform current spreading ability than CL-LEDs. The SEP-LEDs and CL-LEDs power under 20 mA forward current operating is 6.3 mW and 4.3 mW, respectively. The forward voltage of SEP-LEDs and CL-LEDs under 20 mA current driving is 3.15 and 3.35 V, respectively. The SEP-LEDs presents the lower V_f than that of CL-LEDs. Furthermore, the SEP-LEDs exhibits 66.3% wall-plug efficiency enhancement as compared with CL-LEDs at 20mA current injection. The results could be ascribed that the SEP-LEDs has lower series resistance and the larger light emission area. Furthermore, the SEP-LEDs exhibit higher ESD resistance (< -1000V) ability than that of the CL-LEDs due to the uniform current spreading path and the lower series resistance.

The SEP-LEDs has several advantages in small chip size as compared with CL-LEDs. However, the SEP-LEDs structure can not be applied in future LED applications of high output power, high efficiency under higher current density, temperature insensitivity operating, and high reliability property after all. For this reason, the InGaN/ GaN vertical thin film LEDs

(VTF-LEDs) structure is an important tread toward future LED lighting application. In this chapter, the conventional InGaN /GaN LEDs with a sapphire substrate were replaced with a high thermal conductivity silicon substrate by metal-bonding and laser lift-off (LLO) technique. A concept of previous fabrication trench by JPSA 266nm laser cut system before LLO was implemented in this study. The laser cut trench provides a buffer for stress, heat releasing and avoids epi-layer crack from LLO process. The LLO yield could be improved by this method. The Al/ Ag metal was chosen to deposit on *p*-GaN layer as functions of *p*-ohmic and reflector. The Al/ Ag has thermal stability owing to Ag and Al atoms have eutectic point at 728K (455°C). Sliver atoms will alloy with aluminum atoms to become AgAl alloy metal layer while the annealing temperature was higher than eutectic temperature point. The AgAl provided a higher reflectivity and thermal stability than AgNi, AlNi, Al, or Ag. The investigation of *n*-type ohmic contact issue in VTF-LEDs structure is N-face surface of *n*-GaN $(000\bar{1})$, which is different to the conventional sapphire based of Ga-face (0001) surface. This difference in surface structure affects the device characteristics, especially ohmic contact properties due to the mount of dangling bonds. In order to achieve ohmic contact on N-face surface of *n*-GaN, several methods were implanted such as heavily doped on *n*-GaN layer and chemical cleaning on surface. Enhancing light extraction efficiency in VTF-LEDs structure is an important issue, due to the over 95% radiation light is coming from device surface. In this study, the chemical condition of 85ºC 1M KOH for 7min has the brightest light intensity, and the cones height was approached to 8000~9500Å. The VTF-LEDs has lower forward voltage, uniform current spreading, high efficiency under the same current density, less wavelength variation in high current and high temperature ambience operating, higher maximum junction, and excellent thermal impendence as compared with CL-LEDs. Finally, the VTF-LEDs has a superior reliability performance, the variations of electrical and optical were fewer after 1800 hours operating.

REFERENCE

[1] H. Amano, N. Sawaki, I. Akasaki, and Y. Toyoda, “Metalorganic vapor phase epitaxial growth of a high quality GaN film using an AlN buffer layer,” *Appl. Phys. Lett.*, Vol. 48, pp. 353–355, 1986.

[2] H. Amano, M. Kito, K. Hiramatsu, and I. Akasaki, “P-type conduction in Mg-doped GaN treated with low-energy electron beam irradiation (LEEBI),” *Jpn. J. Appl. Phys.*, Vol. 28, pp. L2112–L2114, 1989.

[3] S. Nakamura, M. Senoh, and T. Mukai, “High-power InGaN/GaN double hetero-structure violet light emitting diodes,” *Appl. Phys. Lett.*, Vol. 62, pp. 2390–2392, 1993.

[4] S. Nakamura, M. Senoh, N. Iwasa, and S.-I. Nagahama, “High-power InGaN single-quantum-well-structure blue and violet light-emitting diodes,” *Appl. Phys. Lett.*, Vol. 67, pp. 1868–1870, 1995.

[5] S. Nakamura, M. Senoh, S. Nagahama, N. Iwasa, T. Yamada, T. Matsushita, H. Kiyoku, and Y. Sugimoto, “InGaN-based multi-quantum well-structure laser diodes,” *Jpn. J. Appl. Phys.*, Vol. 35, pp. L74–L76, 1996.

[6] S. J. Rosner, E. C. Carr,M. J. Ludowise, G. Girolami, and H. I. Erikson, “Correlation of cathode-luminescence inhomogeneity with microstructural defects in epitaxial GaN grown by metalorganic chemical-vapor deposition,” *Appl. Phys. Lett.*, Vol. 70, pp. 420–422, 1997.

[7] S. Nakamura, “The roles of structural imperfections in InGaN-based blue light-emitting diodes and laser diodes,” *Science*, Vol. 14, pp. 956–961, 1998.

[8] Nobuhiko P. Kobayashi, Junko T. Kobayashi, Xingang Zhang, P. Daniel Dapkus, and Daniel H. Rich, “ Epitaxial lateral overgrowth of GaN over AlOx surface formed on Si substrate”, *Appl. Phys. Lett.*, Vol. 74, pp. 2386–2389, 1999.

[9] Shulin Gu, Rong Zhang, Yi Shi, and Youdou Zheng, “Epitaxial lateral overgrowth of GaN on molecular beam epitaxy GaN buffer layers on Si substrates by hydride vapour phase epitaxy”, *J. Phys. D: Appl. Phys*, Vol. 34, pp. 1951–1954, 2001.

[10] Z. H. Feng and K. M. Lau, “Enhanced luminescence from GaN-based blue LEDs grown on grooved sapphire substrates,” *IEEE Photon. Technol. Lett.*, Vol. 17, no. 9, pp. 1812–1814, Sep. 2005.

[11] S. J. Chang, Y. K. Su, Y. C. Lin, R. W. Chuang, C. S. Chang, J. K. Sheu, T. C. Wen, S. C. Shei, C. W. Kuo, and D. H. Fan, “MOCVD growth of InGan/GaN blue light emitting diodes on patterned sapphire substrates,” *Phys. Stat. Sol. (C)*, Vol. 7, pp. 2253–2256, 2003.

[12] D. S.Wuu, W. K.Wang, W. C. Shih, R. H. Horng, C. E. Lee, W. Y. Lin, and J. S. Fang, “Enhanced output power of near-ultraviolet InGaN-GaN LEDs grown on patterned sapphire substrates,” *IEEE Photon. Technol. Lett.*, Vol. 17, no. 2, pp. 288–290, Feb. 2005.

[13] Y. J. Lee, T. C. Hsu, H. C. Kuo, S. C.Wang, Y. L. Yang, S. N. Yen, Y. T. Chu, Y. J. Shen, M. H. Hsieh, M. J. Jou, and B. J. Lee, “Improvement in light-output efficiency of near-ultraviolet InGaN–GaN LEDs fabricated on stripe patterned sapphire substrates,” *Mater. Sci. Eng., B*, Vol. 122, no. 3, pp. 184–187, 2005.

[14] E. F. Schubert, *Light-Emitting Diodes*, Second ed. Cambridge, U.K. Cambridge Univ. Press, 2006.

[15] T. Fujii, Y. Gao, R. Sharma, E. L. Hu, S. P. DenBaars, and S. Nakamura, “Increase in the extraction efficiency of GaN-based light-emitting diodes via surface roughening,” *Appl. Phys. Lett.*, Vol. 84–86, pp. 855–855, 2004.

[16] R. Windisch, C. Rooman, S. Meinlschmidt, P. Kiesel, D. Zipperer, G. H. Döhler, B. Dutta, M. Kuijk, G. Borghs, and P. Heremans, “Impact of texture-enhanced transmission

on high-efficiency surface-textured light-emitting diodes," *Appl. Phys. Lett.*, Vol. 79, pp. 2315–2317, 2001.

[17] H. W. Huang, C. C. Kao, J. T. Chu, H. C. Kuo, S. C. Wang, and C. C. Yu, "Improvement of InGaN–GaN light-emitting diode performance with a nano-roughened p-GaN surface," *IEEE Photon. Technol. Lett.*, Vol. 17, no. 5, pp. 983–985, May 2005.

[18] S. J. Chang, C. S. Chang, Y. K. Su, C. T. Lee, W. S. Chen, C. F. Shen, Y. P. Hsu, S. C. Shei, and H. M. Lo, "Nitride-based flip-chip ITO LEDs," *IEEE Trans. Adv. Packag.*, Vol. 28, no. 2, pp. 273–277, May 2005.

[19] Hibbard, S. P. Jung, C. Wang, D. Ullery, Y. S. Zhao, W. So, H. Liu, and H. P. Lee, "Low resistance high reflectance contacts to p-GaN using oxidized Ni/Au and Al or Ag," *Appl. Phys. Lett.*, Vol. 83, pp. 311–313, 2003.

[20] Y. Kondoh, S. Wantanabe, Y. Kaneko, S. Nakagawa, N. Yamada "Nitride Semiconductor Light Emitting Device Having a Silver p-Contact," Transl.: U.S. Patent 6, 194, 743.

[21] M. K. Kelly, O. Ambacher, R. Dimitrov, R. Handschuh, and M. Stutzmann, "Optical process for liftoff of group III-nitride films," *Phys. Stat. Sol. (A)*, Vol. 159, pp. R3–R4, 1997.

[22] W. S. Wong, T. Sands, and N. W. Cheung, "Damage-free separation of GaN thin films from sapphire substrates," *Appl. Phys. Lett.*, Vol. 72, pp. 599–601, 1998.

[23] V. Haerle *et al.*, "High brightness LEDs for general lighting applications using the newThinGaN technology," *Phys. Stat. Sol. (A)*, Vol. 201, pp. 2736–2739, 2004.

[24] D. Morita *et al.*, "Watt-class high-output-power 365 nm ultraviolet light-emitting diodes," *Jpn. J. Appl. Phys.*, Vol. 43, pp. 5945–5950, 2004.

[25] O. B. Shchekin *et al.*, "High performance thin-film flip-chip InGaN-GaN light-emitting diodes," *Appl. Phys. Lett.*, Vol. 89, pp. 071109, 2006.

[26] H. X. Jiang, S. X. Jin, J. Li, J. Shakya, and J. Y. Lin, “III-nitride blue microdisplay,” *Appl. Phys. Lett.* Vol.78, pp. 1303-1305, 2001.

[27] S. Nakamura and S. F. Chichibu 2000 *Introduction to Nitride Semiconductor Blue Laser Diode and Light Emitting Diodes*. London, U.K.: Taylor and Francis.

[28] W. S. Wong, T. Sands, N. W. Cheung, M. Kneissl, D. P. Bour, P. Mei, L. T. Romano, and N. M. Johnson, “InxGa1-xN light emitting diodes on Si substrates fabricated by Pd-In metal bonding and laser lift-off”, *Appl. Phys. Lett.*, Vol. 77, pp. 2822-2824, Oct. 2000.

[29] W. C. Peng, and Y. S. Wu, “Performance of InGaN-GaN LEDs fabricated using glue bonding on 50-mm Si substrate,” *IEEE Photon. Technol. Lett.*, Vol. 18, pp. 613, 2006.

[30] W. Y. Lin, D. S. Wuu, K. F. Pan, S. H. Huang, C. E. Lee, W. K. Wang, S. C. Hsu, Y. Y. Su, S. Y. Huang, and R. H. Horng, “High-Power GaN–Mirror–Cu Light-Emitting Diodes for Vertical Current Injection Using Laser Liftoff and Electroplating Techniques”, *IEEE Photon. Technol. Lett.*, Vol. 17, pp. 1809-1811, 2005.

[31] O. B. Shchekin, J. E. Epler, T. A. Trottier, T. Margalith, D. A. Steigerwald, M. O. Holcomb, P. S. Martin, and M. R. Krames, “High performance thin-film flip-chip InGaN-GaN light-emitting diodes,” *Appl. Phys. Lett.*, Vol.89, 071109, 2006.

[32] S. J. Kim, Y. S. Choi, Y. H. Han, and C. Y. Kim, “Vertical chip of GaN-based light-emitting diode formed on sapphire substrate,” *Phys. Stat. Sol.*, Vol. 202, pp. 2034, 2005.

[33] S. J. Kim, “Improvement of GaN-based light-emitting diode by indium-tin-oxide transparent electrode and vertical electrode,” *IEEE Photon. Technol. Lett.*, Vol. 17, pp. 1617, 2005.

[34] R. H. Horng, C. C. Yang, J. Y. Wu, S. H. Huang, C. E. Lee, and D. S. Wuu, “GaN-based light-emitting diodes with indium-tin-oxide texturing window layers using natural lithography”, *Appl. Phys. Lett.*, Vol.86, 221101, 2005.

[35] S. M. Pan, R. C. Tu, Y. M. Fan, R. C. Yeh, and J. T. Hsu, “Improvement of InGaN–GaN Light-Emitting Diodes with Surface-Textured Indium–Tin–Oxide Transparent Ohmic Contacts,” *IEEE Photon. Technol. Lett.*, Vol. 15, No. 5, pp. 649-651, 2003.

[36] M. Sumiya, K. Yoshimura, T. Ito, K. Ohtsuka, S. Fuke, K. Mizuno, M.Yoshimoto, H. Koinuma, A. Ohtomo, and M. Kawasaki, “Growth mode and surface morphology of a GaN film deposited along the N-face polar direction on c-plane sapphire substrate” *J. Appl. Phys.* Vol. 88, pp. 1158-1160, 2000.

[37] M. Sumiya and S. Fuke, “Review of polarity determination and control of GaN” (invited paper) *MRS Internet J. of Nitride Semicond. Res.* Vol. 9, pp.1-32, 2004.

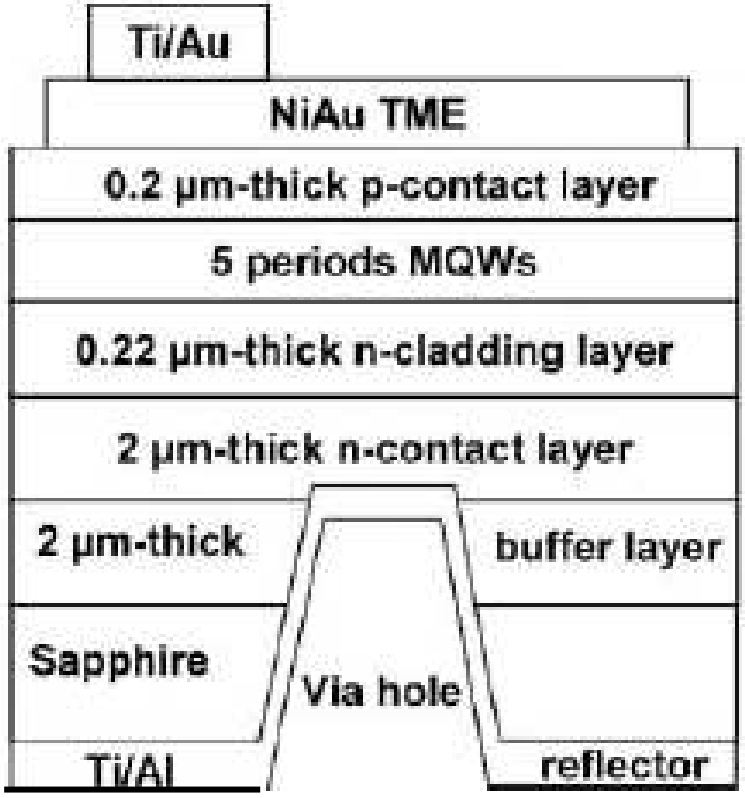
[38] Uwe Karrer, Oliver Ambacher, and Martin Stutzmann, “Influence of crystal polarity on the properties of PtÕGaN Schottky diodes”, *Appl. Phys. Lett.*, Vol.77, pp.2011-2013, 2000.

[39] Joon Seop Kwak, K. Y. Lee, J. Y. Han, J. Cho, S. Chae, O. H. Nam, and Y. Park, “Crystal-polarity dependence of Ti/ Al contacts to freestanding n-GaN substrate”, *Appl. Phys. Lett.*, Vol.79, pp.3254-3256, 2001.

[40] T. Jang, S. N. Lee, O. H. Nam, and Y. Park, “Investigation of Pd/Ti/Al and Ti/Al Ohmic contact materials on Ga-face and N-face surfaces of *n*-type GaN”, *Appl. Phys. Lett.*, Vol.88,193505, 2006.

[41] H.W.Jang, J.-H.Lee, and J.-L.Lee, “Characterization of band bendings on Ga-face and N-face GaN films grown by metalorganic chemical-vapor deposition”, *Appl. Phys. Lett.*, Vol.80, pp.3955-3957, 2002.

(a)



(b) (c)

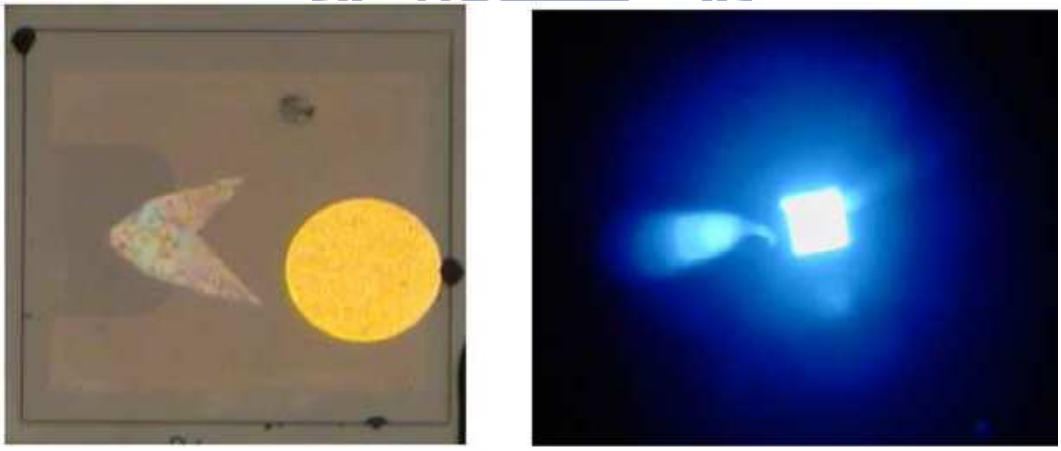


Figure 4.1: (a) Schematic diagram of SEVENS LEDs structure (b) Microscope image of chip, and (c) Electroluminescence photograph image under 20-mA current injection for SEVENS-LED fabricated by sapphire wet etching.

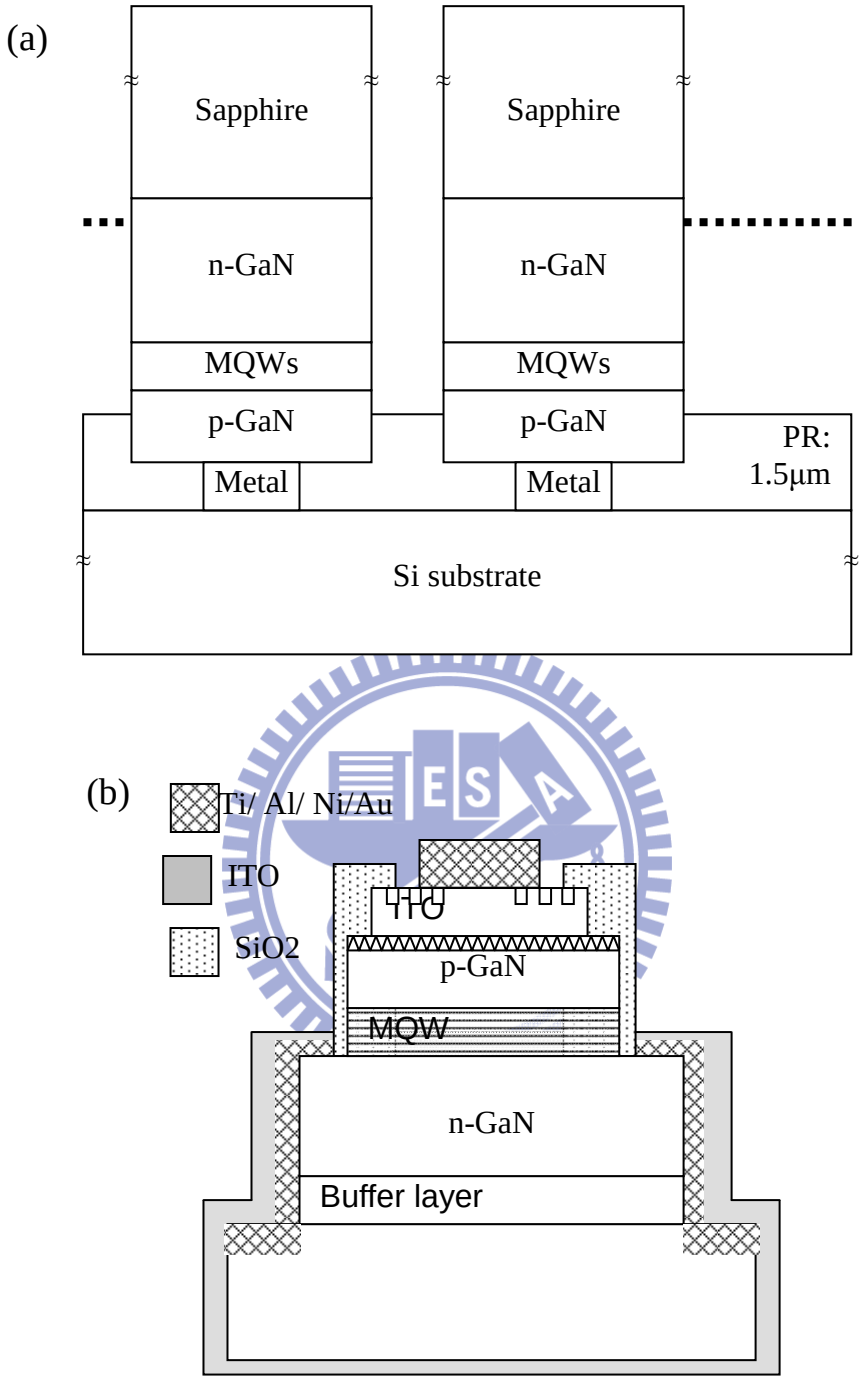


Figure 4.2 : Schematic diagrams of (a) The expanded chips were flipped and embedded in PR (b) The structure of single electrode pad GaN-based LEDs (SEP-LEDs) fabricated on sapphire substrate.

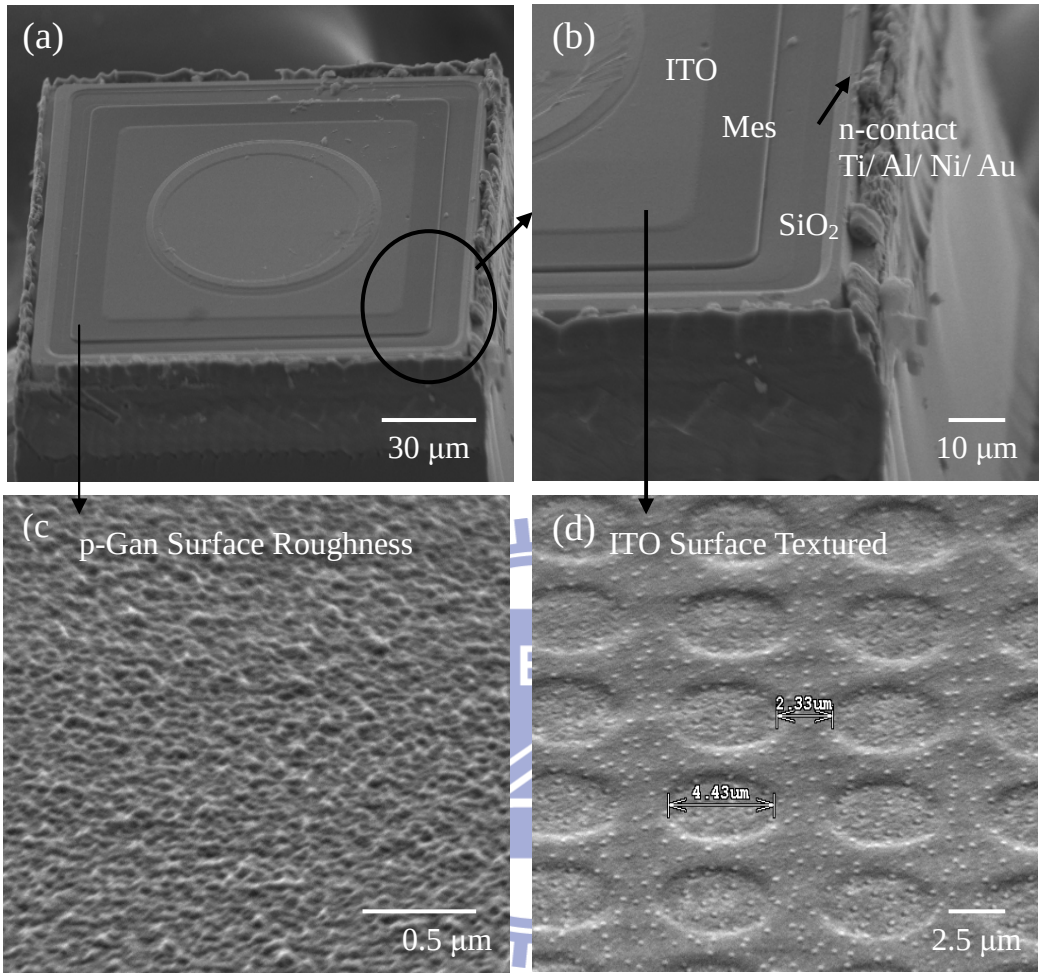


Figure 4.3: Scanning electron microscope (SEM) images of (a) Chip profile (b) Detail description (c) Top-view of p-GaN surface roughness (d) Surface textured of ITO layer by photolithography and chemical wet-etching.

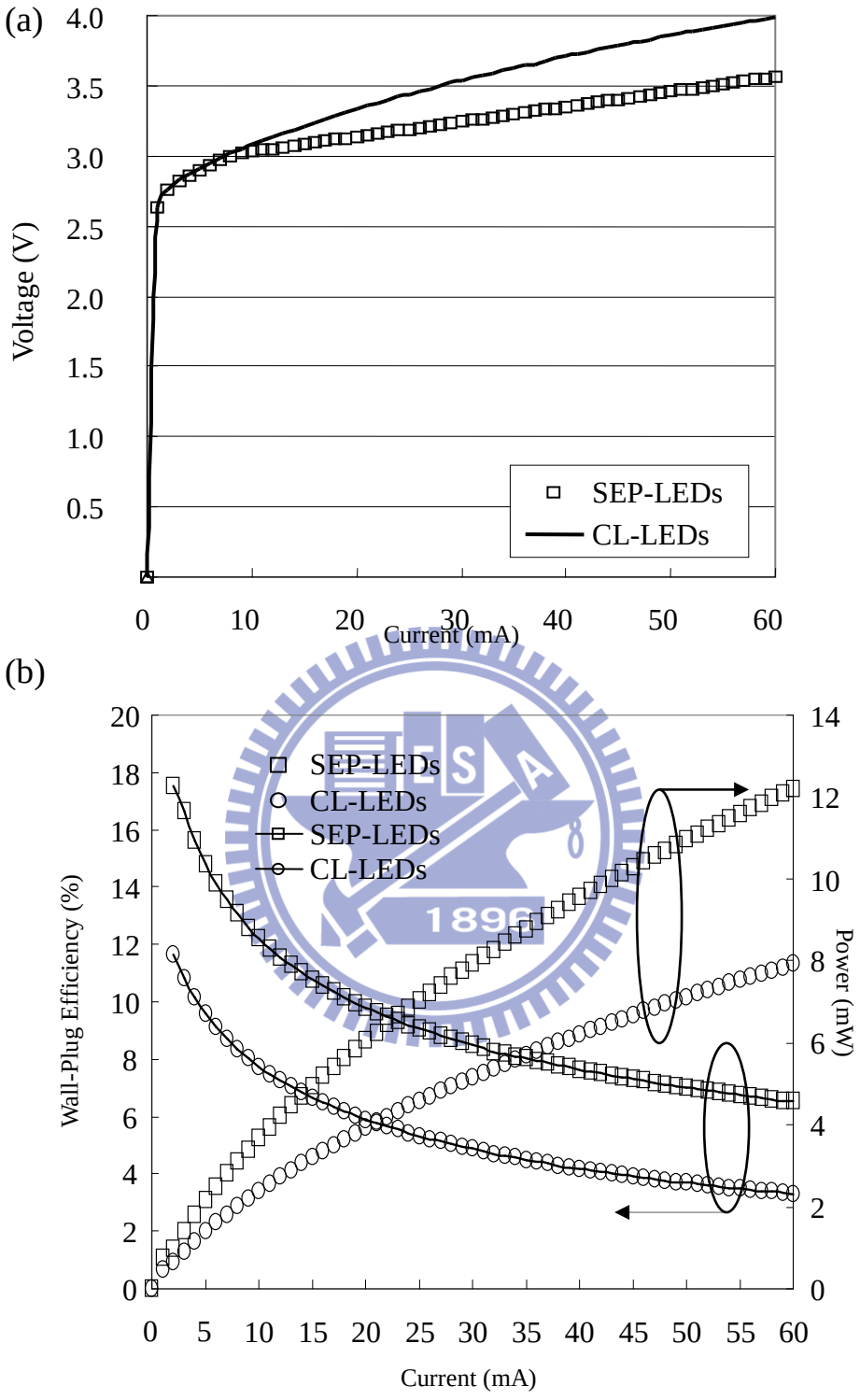


Figure 4.4: (a) Typical current versus voltage (I-V) characteristics of SEP-LEDs and CL-LEDs (b) Wall-plug efficiency and output power in relation to injection current of SEP-LEDs and CL-LEDs.

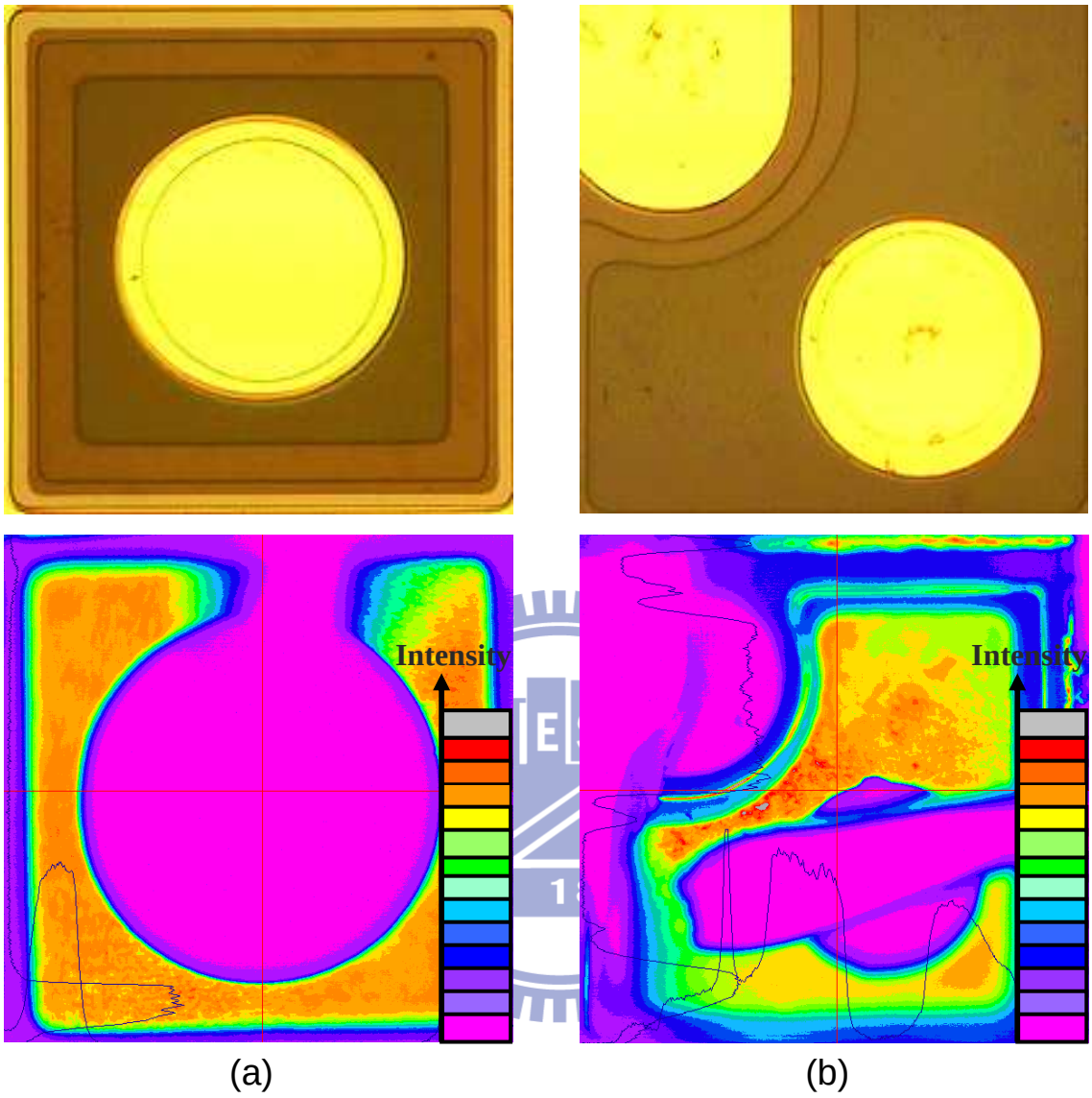


Figure 4.5: Optical and electro-luminescence (EL) microscope images of (a) SEP-LEDs and (b) CL-LEDs.

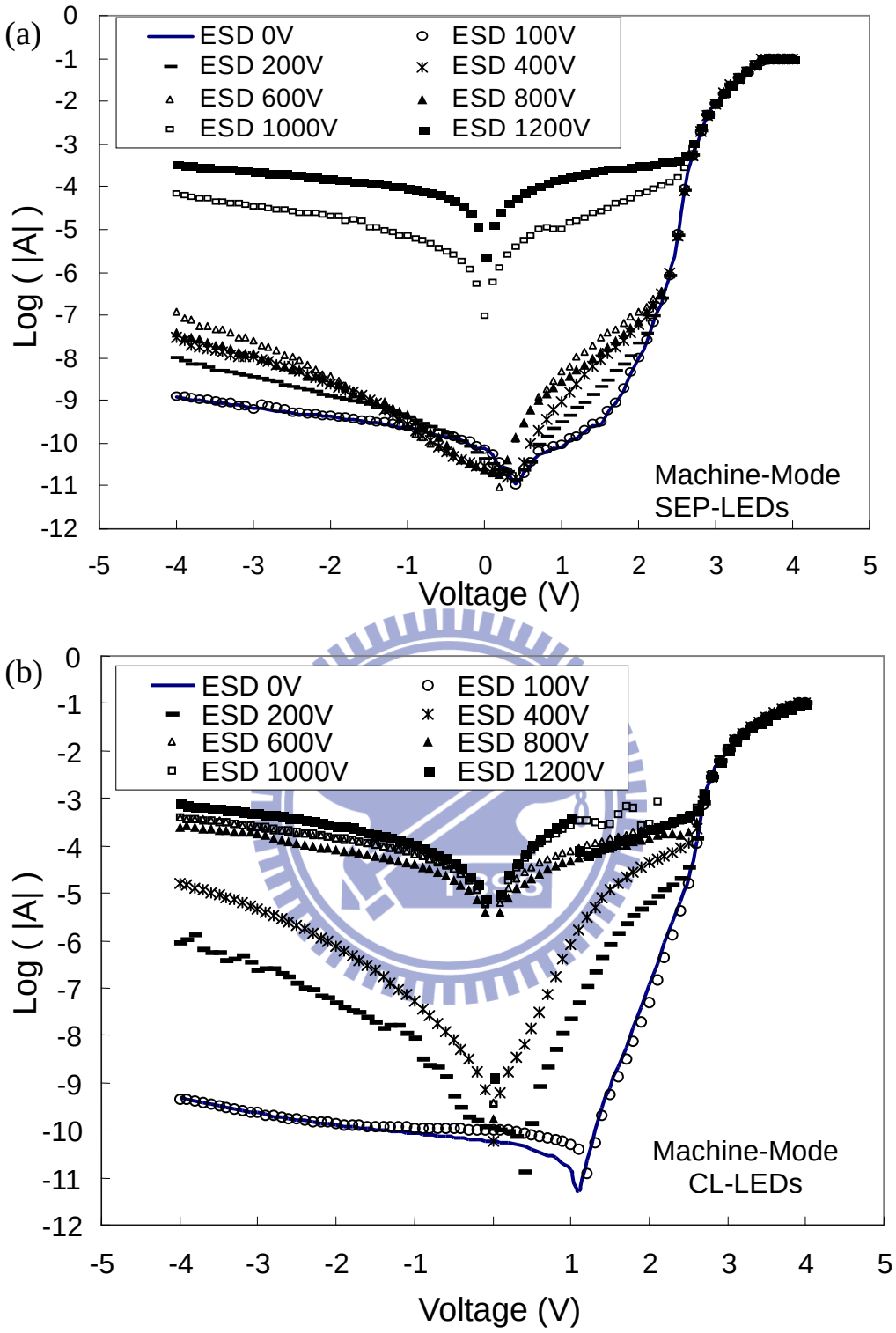


Figure 4.6: I-V characteristics as a function of a reverse pulse voltage in a machine-model ESD driving for (a) SEP-LEDs (b) CL-LEDs.

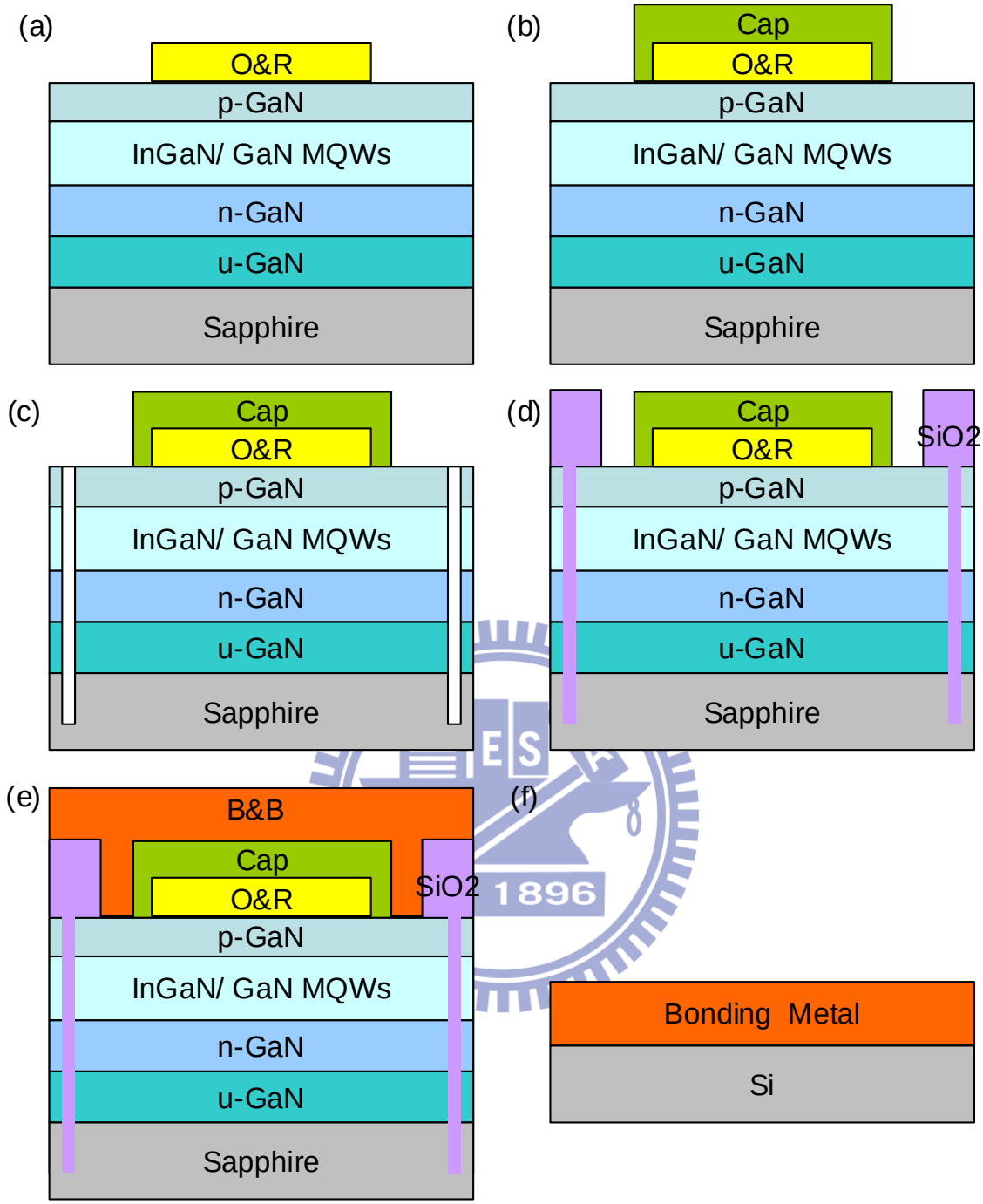


Figure 4.7: (a) The O&R metal film of Al/Ag/Ni was respectively deposited on p-GaN surface. (b)Cap layer of Ti/W (2 pairs)/Ti/Au was deposited on O&R. (c) The wafer was submitted to laser cut for releasing internal stress. (d) SiO_2 film was taken as an etching stop layer during n-GaN mesa dry etching. (e) The barrier metal layers Ti/ W/ Ti/ Ni/ Au and bonding metal laters Ti/ Pt/ Au (B&B metal layers) were sequentially deposited on surface. (f) The bonding metal layers Ti/ Pt/ Au/ In were deposited on a Si substrate.

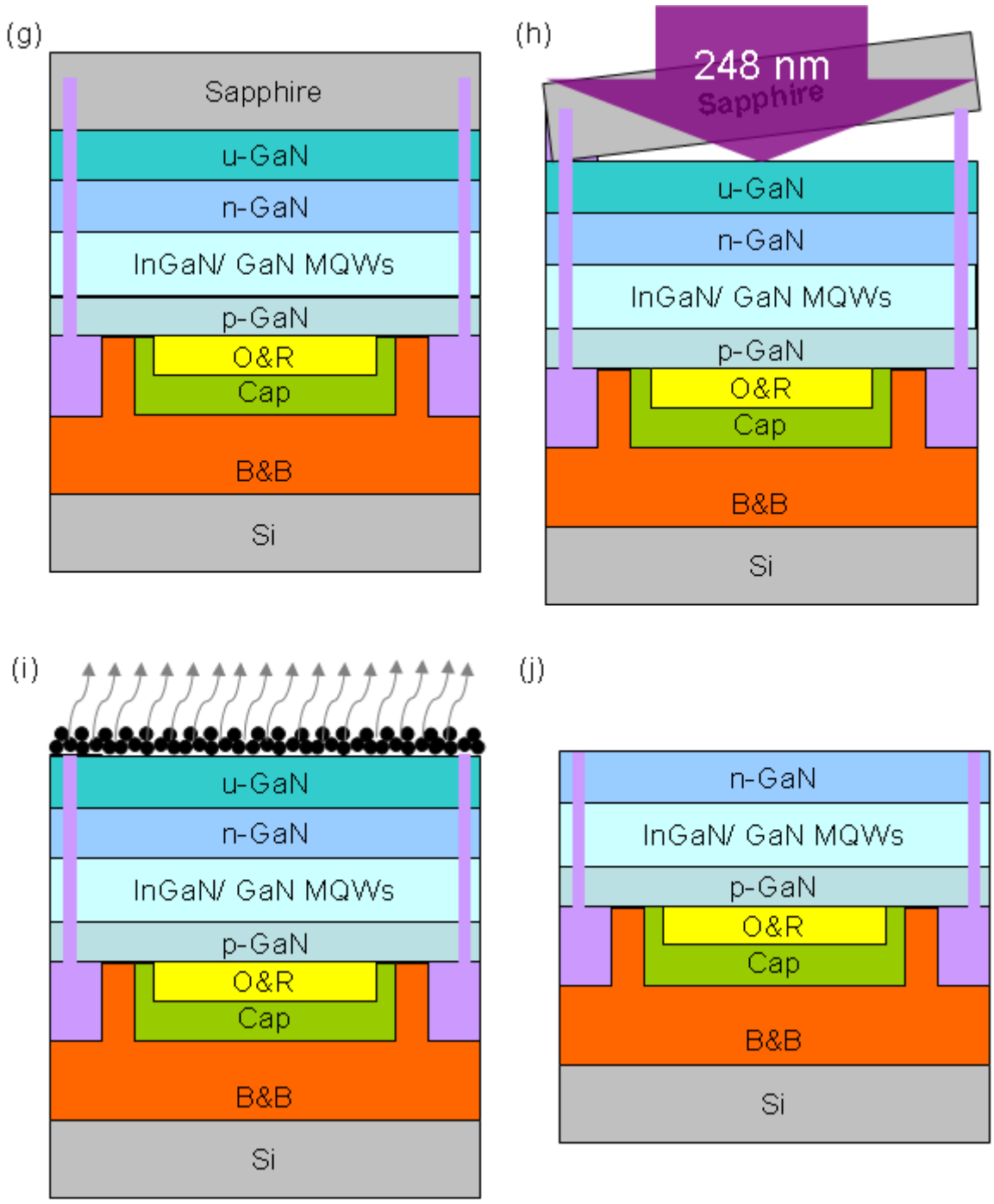


Figure 4.7: (g) The epi-wafer was flipped and bonded to the Si substrate. (h) The laser lift-off process. (i) The surface byproduct of Ga was removed by chemical etching. (j) Un-doped GaN was removed until n-GaN was exposed.

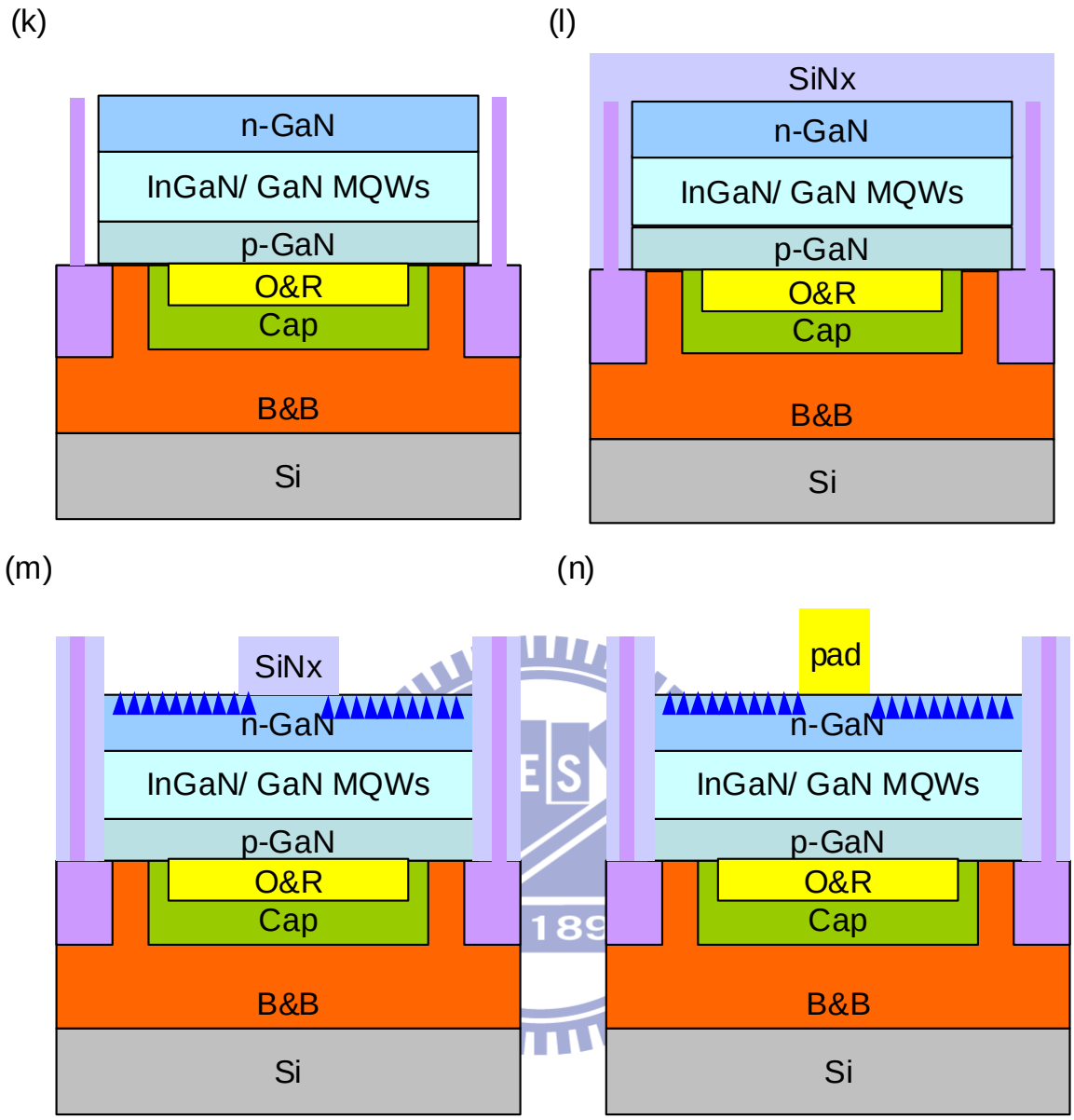
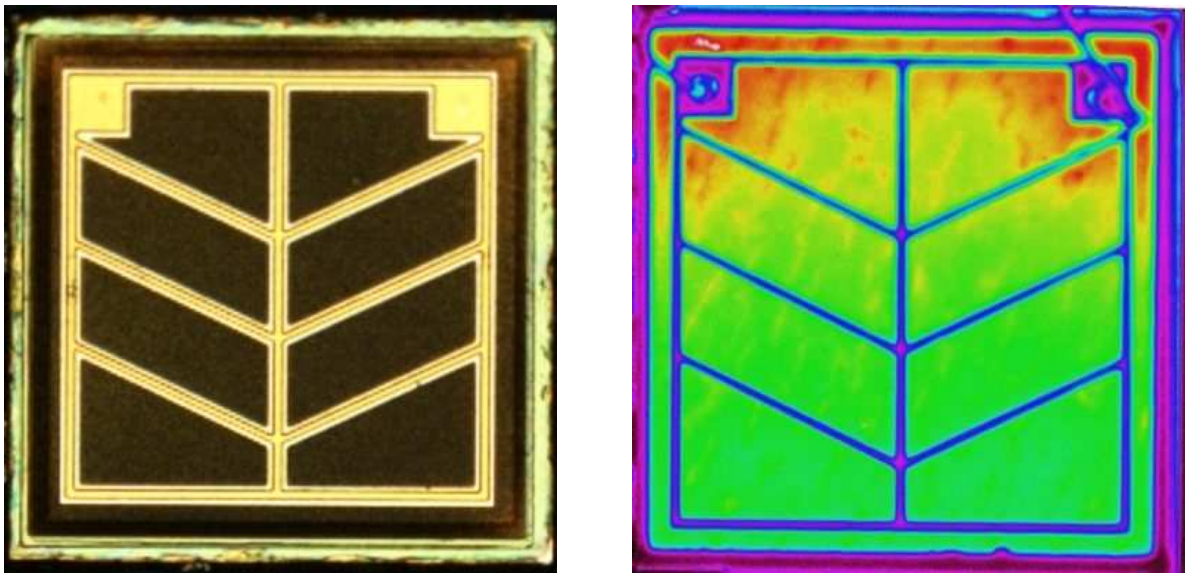


Figure 4.7: (k) The wafer was subjected to dry etching n-GaN layer until SiO_2 etching stop layer was exposed. (l) A thick SiN_x was grown on wafer surface for hard mask of roughness process. (m) A random roughness surface was formed on N-face GaN after KOH chemical wet etching. (n) The Cr /Au metal layers were selectively formed on surface for n-ohmic contact.

(a) (b)



(c)

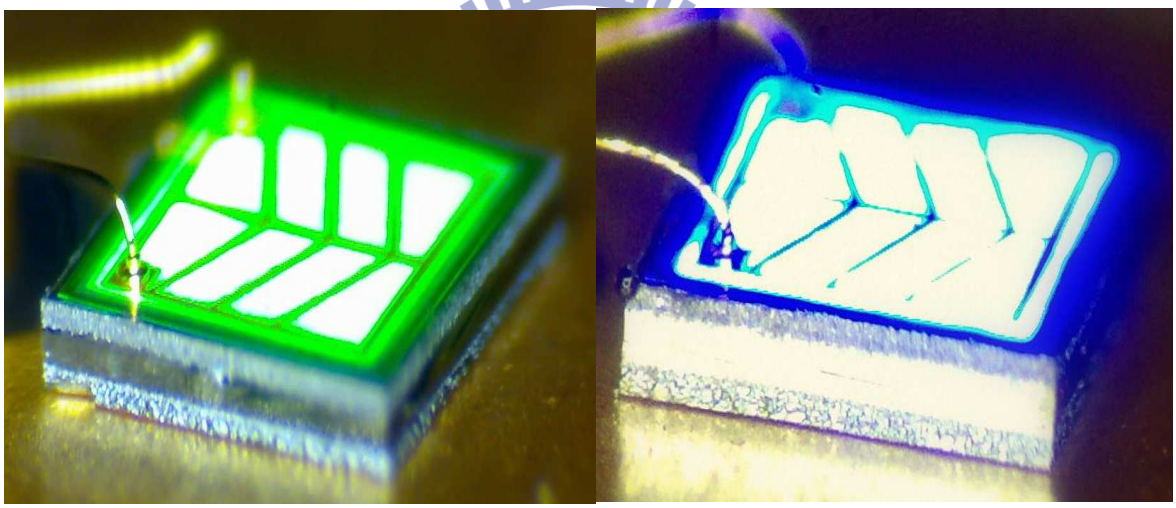
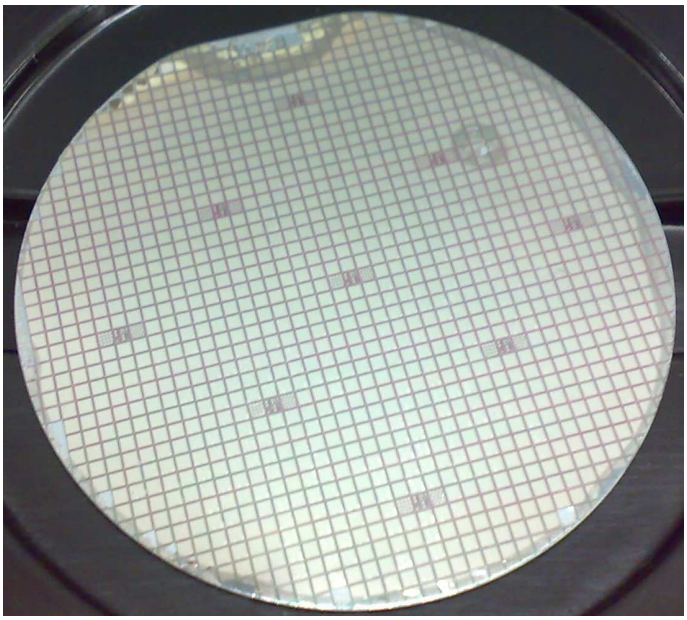


Figure 4.8: (a) The chip profile of VTF-LEDs and the chip size is 1200 μm×1200 μm. (b) The current spreading performance in VTF-LEDs metal mesh line design. (c) The tilted cross-section electroluminescent (EL) image of green and blue VTF-LEDs.

(a)



(b)

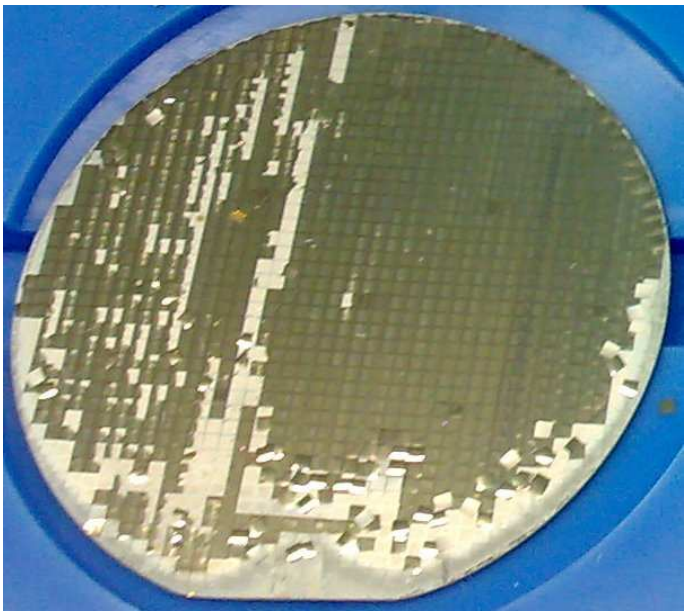


Figure 4.9: The wafer surface profiles after suffering LLO process, (a) With a previous fabrication trench by laser cut system. (b) Without a previous fabrication trench.

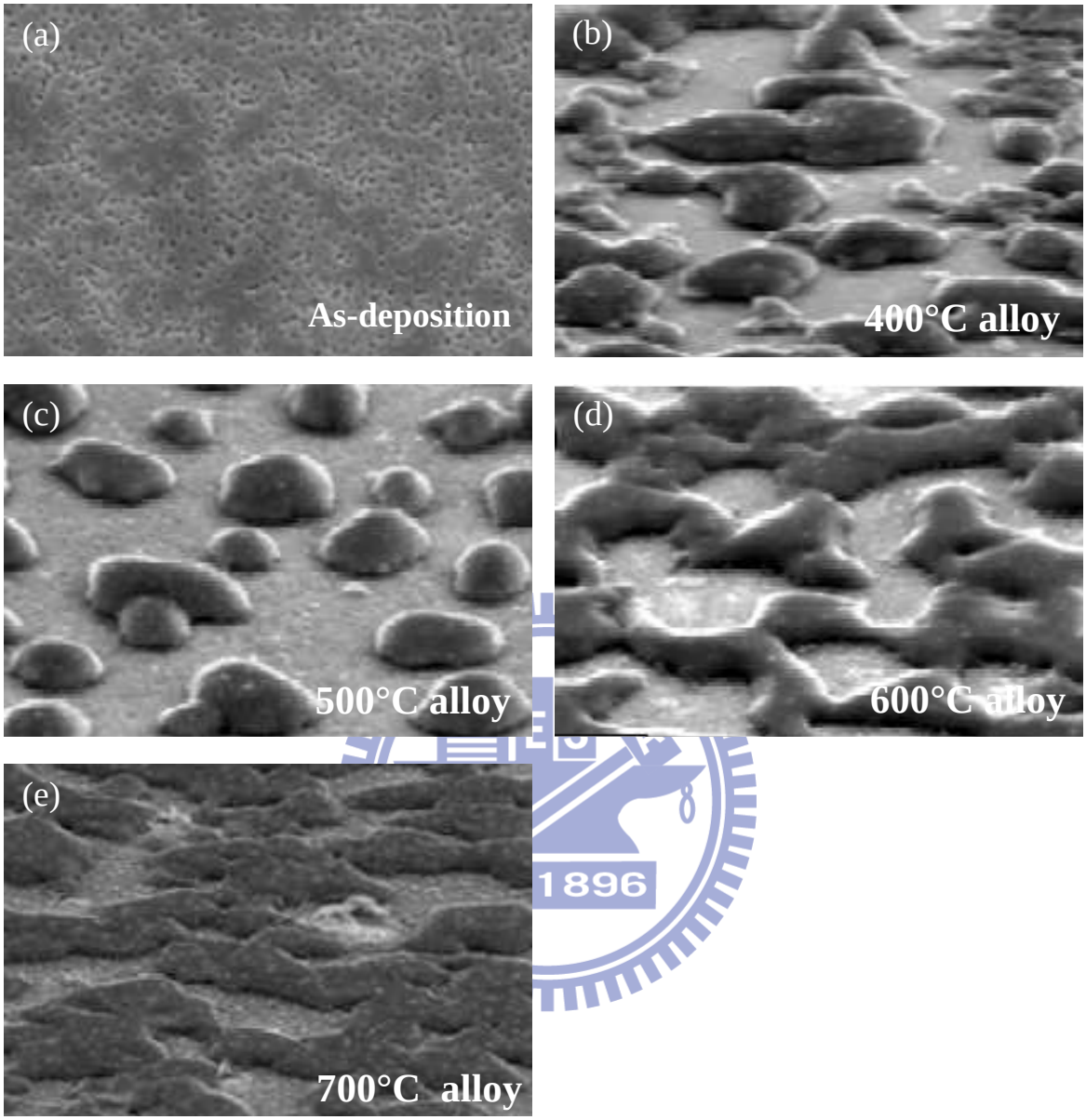
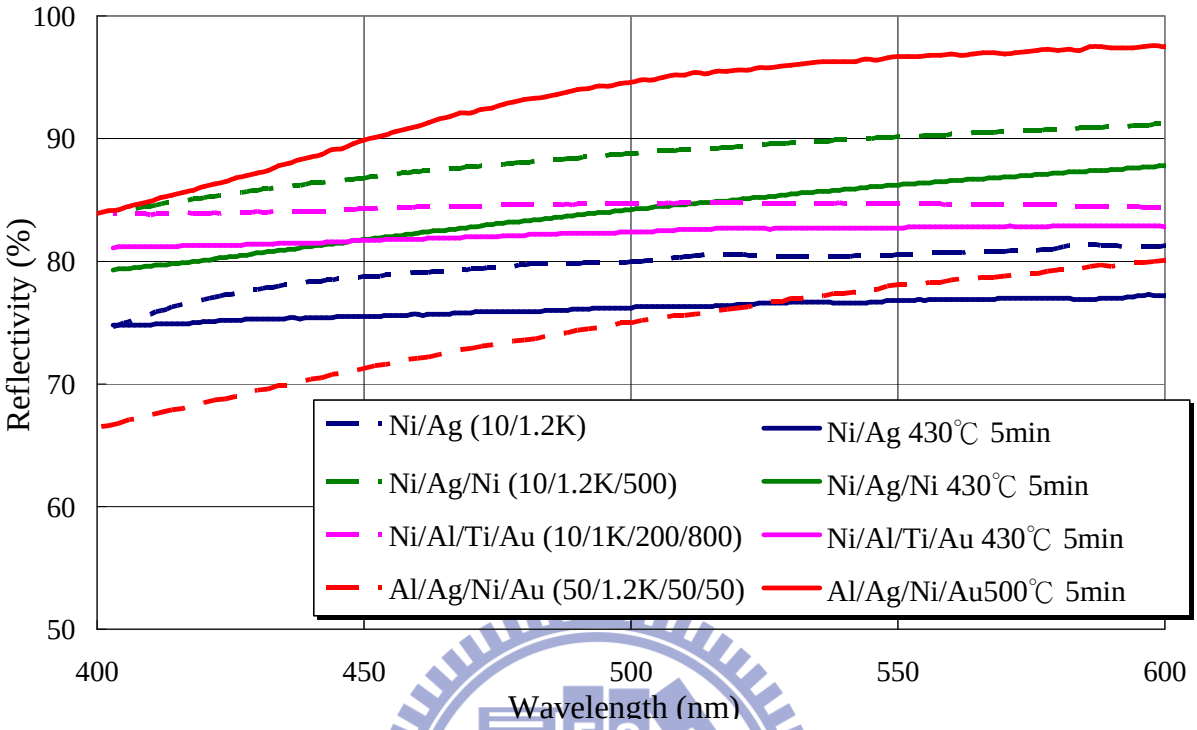


Figure 4.10: The SEM figures of Ni/ Ag (50nm/ 150nm) metal on p-GaN surface after. (a) as-deposition (b) 400°C (c) 500°C (d) 600°C (d) 700°C different thermal treatment.



		Reflectance @460nm	Reflectance @520nm
Ni/Ag (10/1.2K)	non-alloy	79.10%	80.60%
	430℃	75.70%	76.50%
Ni/Ag/Ni (10/1.2K/500)	non-alloy	87.30%	89.40%
	430℃	82.30%	85.10%
Ni/Al/Ti/Au (10/1K/200/800	non-alloy	84.50%	84.80%
	430℃	81.80%	82.70%
Al/Ag/Ni/Au (50/1.2K/50/50	non-alloy	72.00%	76.10%
	500℃	90.80%	95.50%

Figure 4.11: The O&R metal reflectance of various compositions under different alloy temperature.

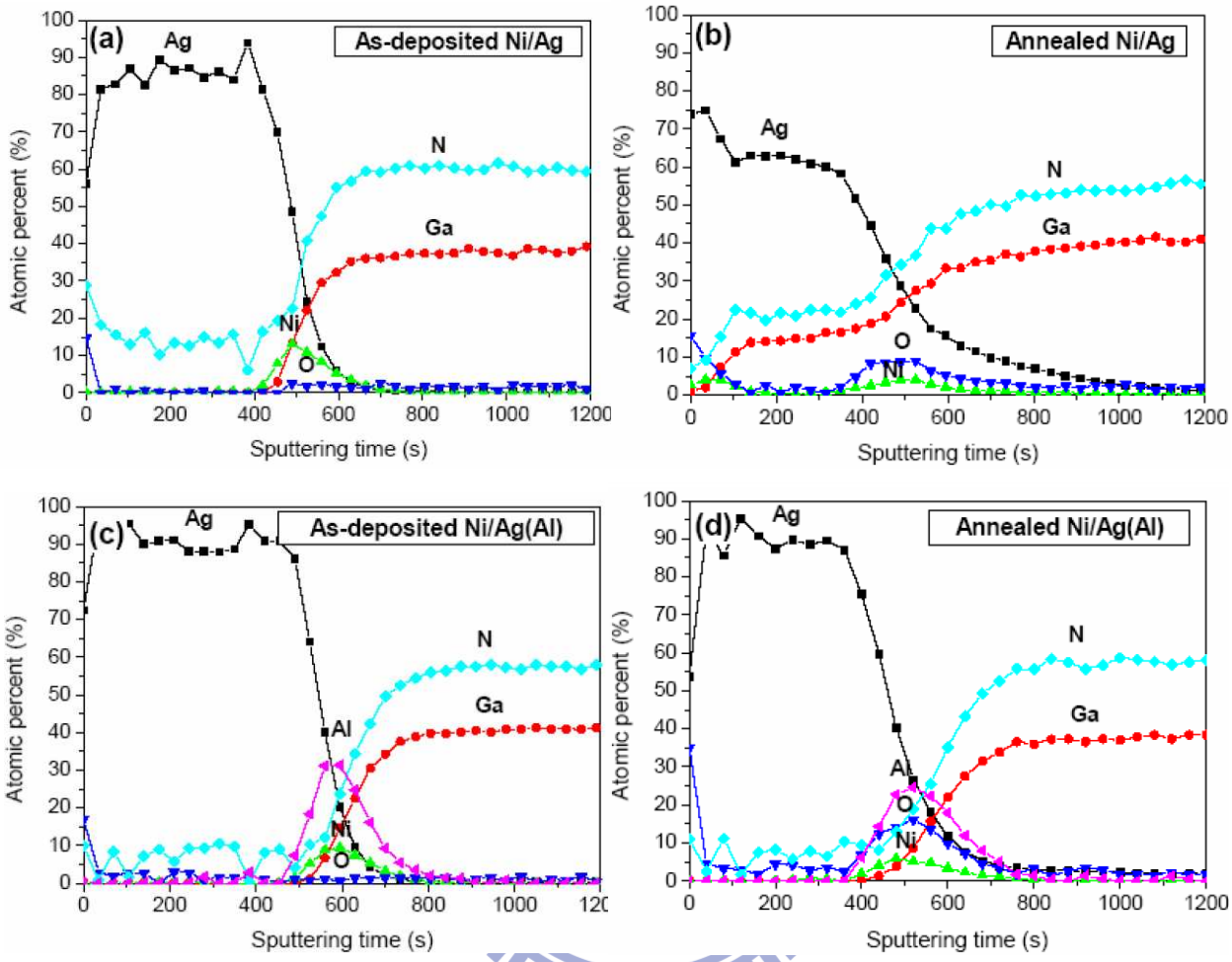


Figure 4.12: XPS atomic depth profile of Ni/ Ag and Ni/ Al/ Ag composition before and after thermal treatment at 500°C in ambient air.

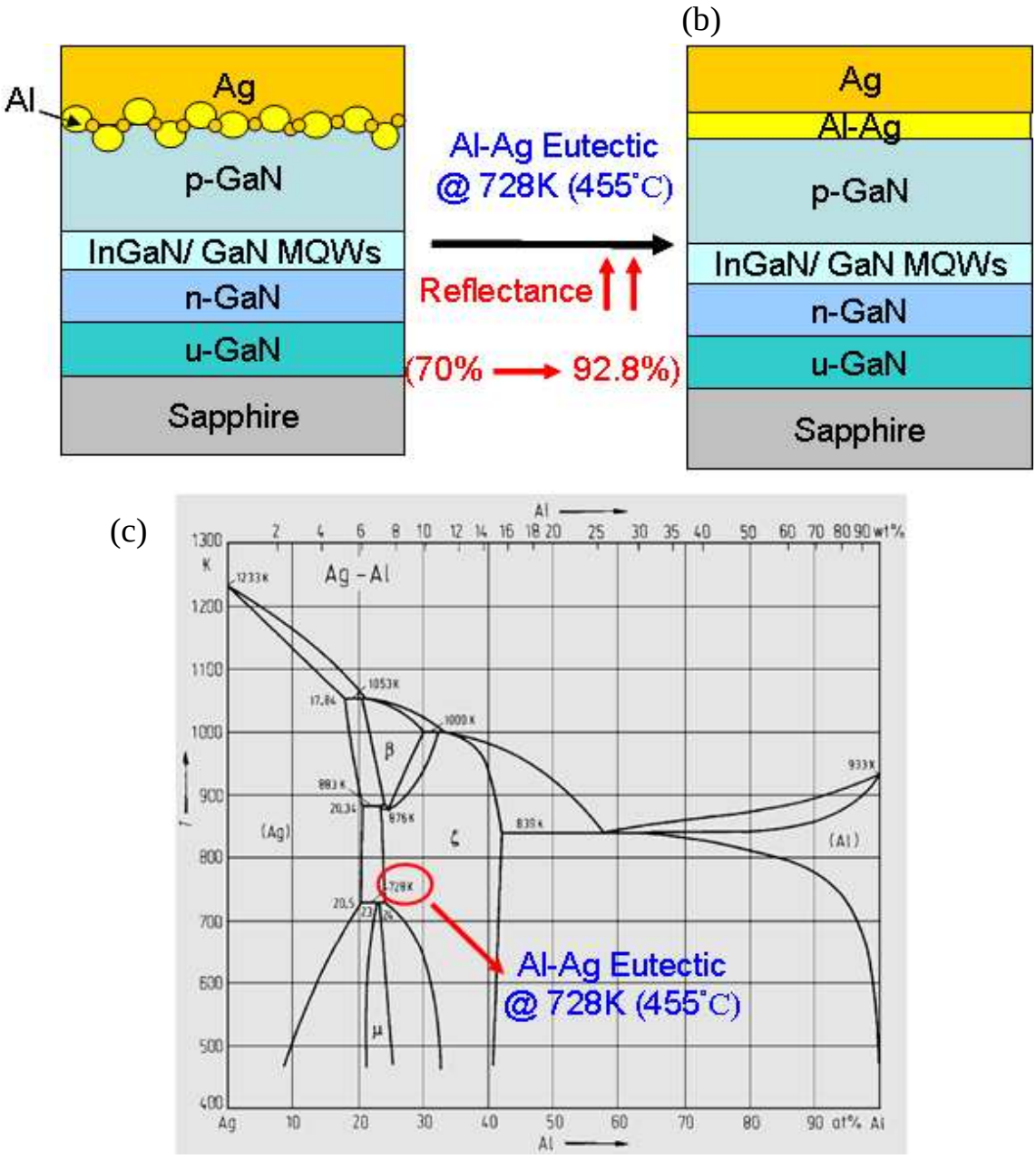


Figure 4.13: The schematic diagram of (a) Al/ Ag was deposited on p-GaN. (b) After thermal annealing, an AlAg eutectic layer was formed. (c) The AlAg eutectic phase diagram.

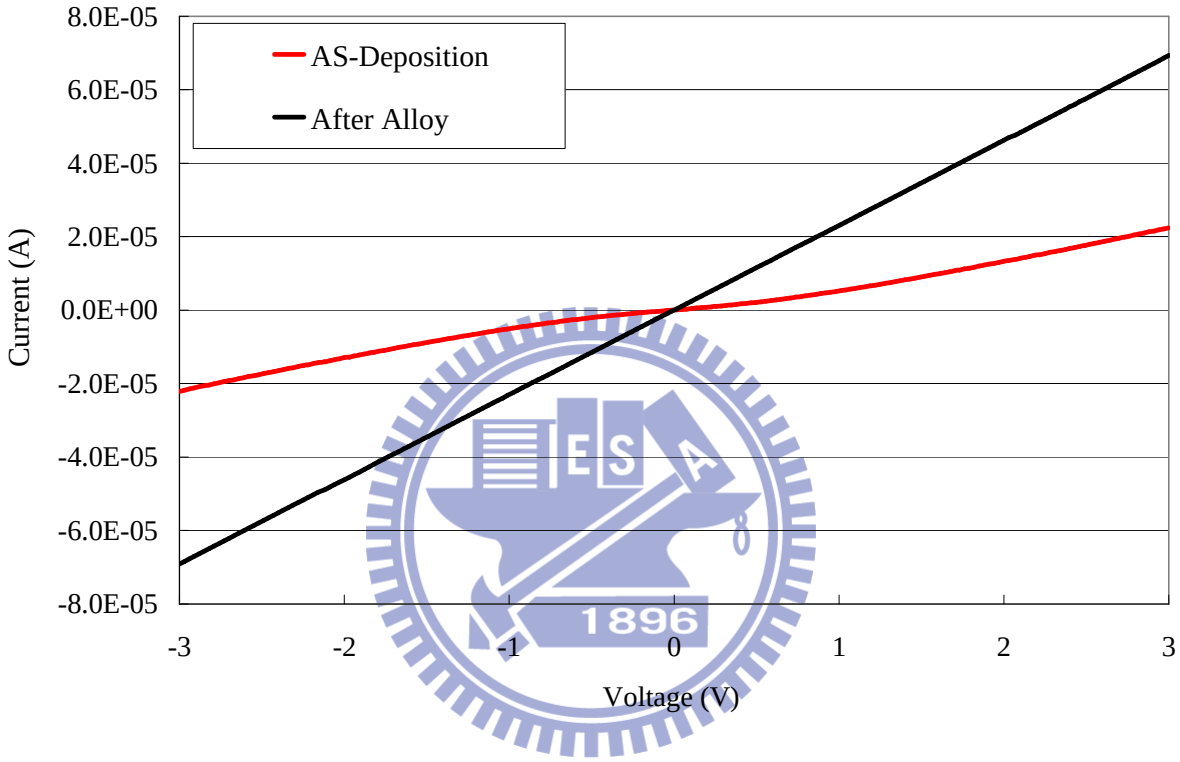


Figure 4.14: The current-voltage characteristic of O&R layer as-deposition and after thermal treatment.

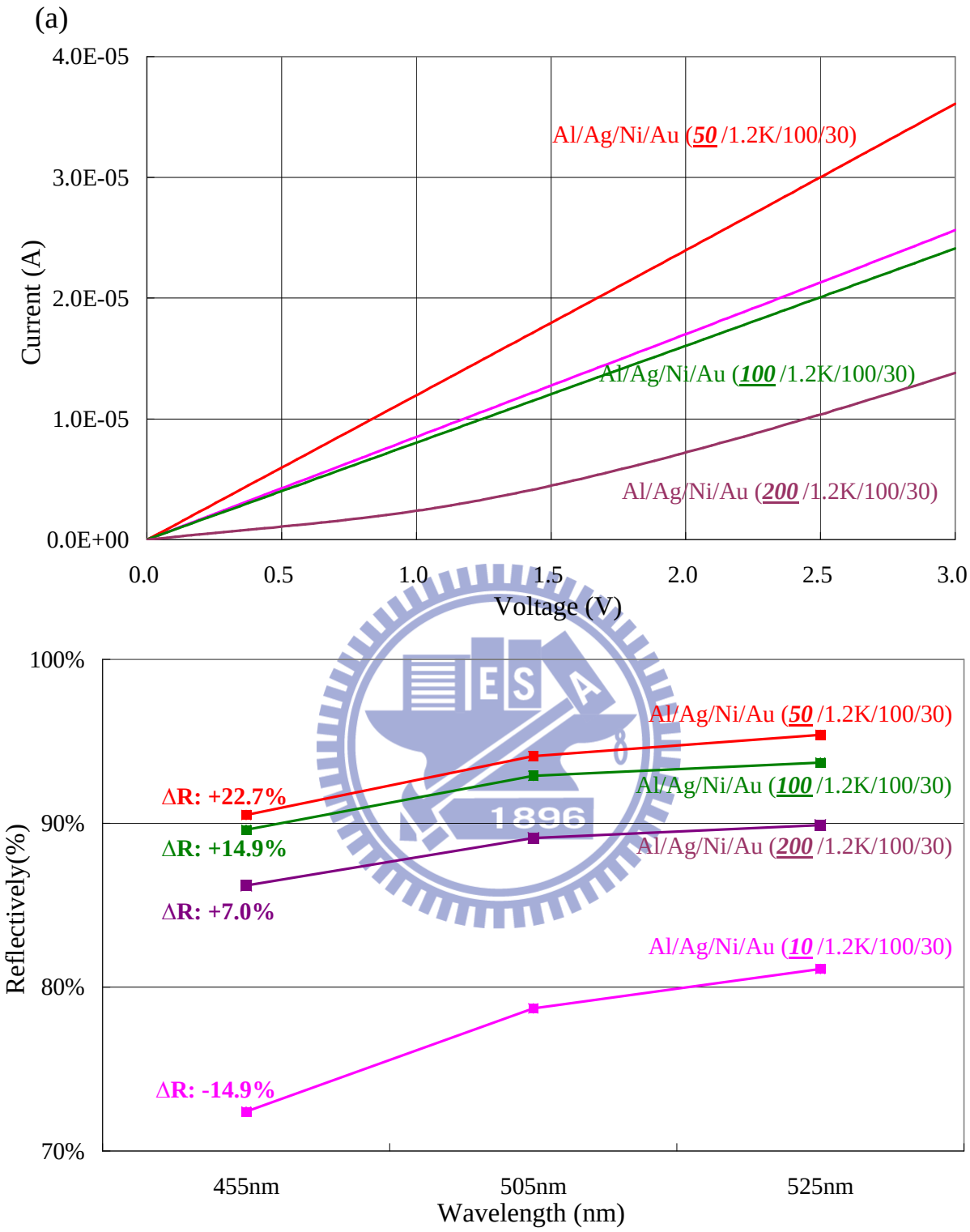


Figure 4.15: (a) The I-V curve, and (b) Reflectively of various aluminum thicknesses after 500ºC thermal annealing

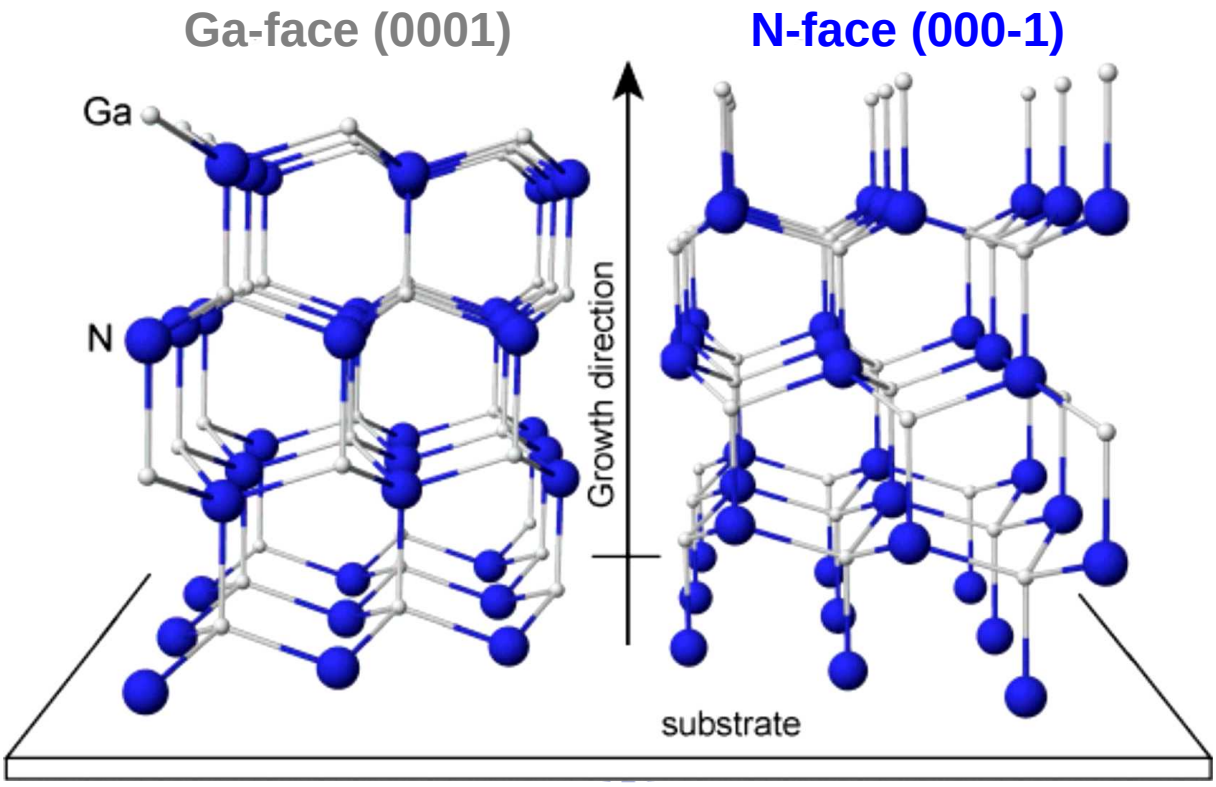


Figure 4.16: Schematic illustration of GaN wurtzite crystal structure exhibiting the polarity along the c-axis.

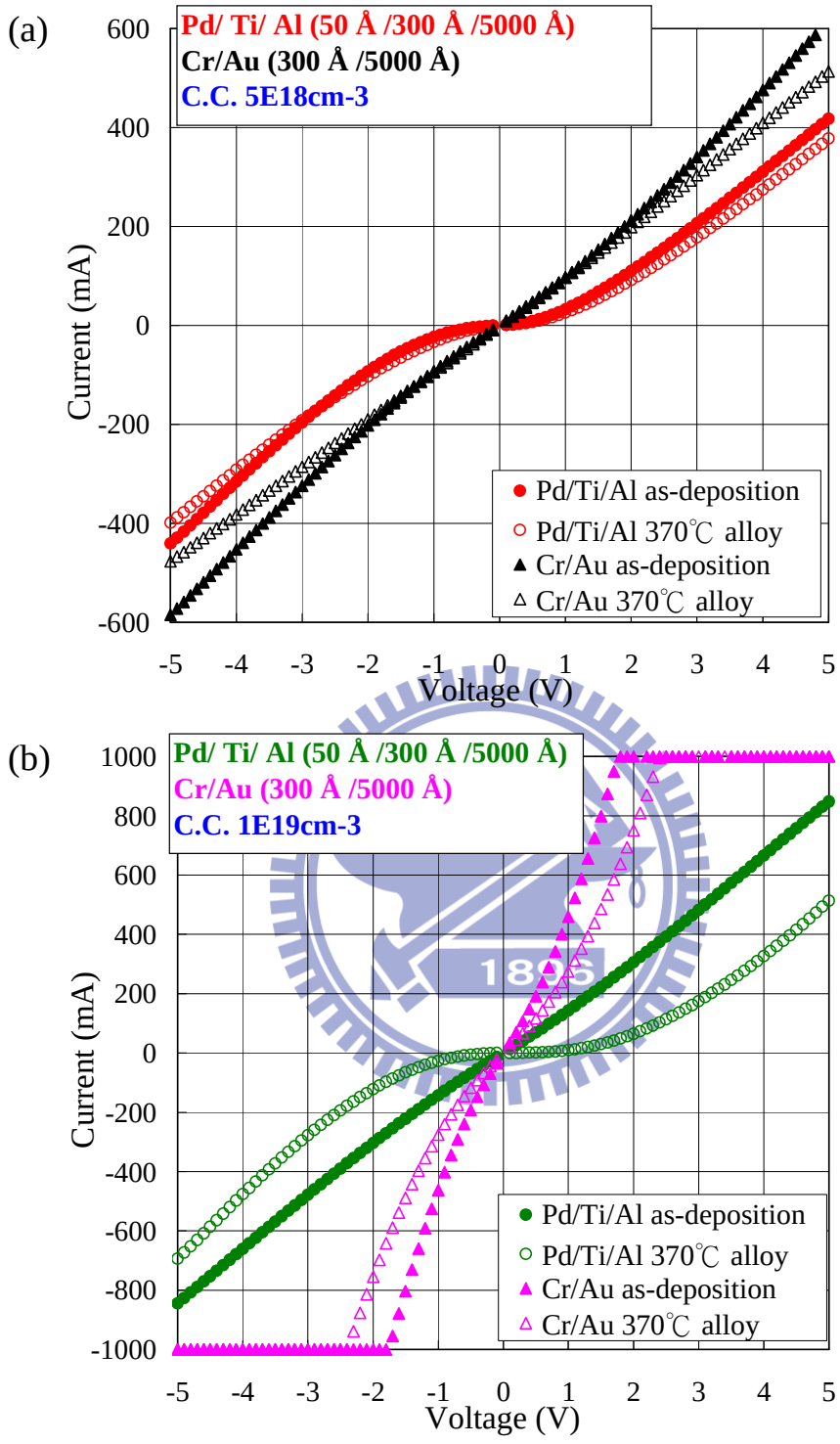


Figure 4.17: The I-V curves of Pd/ Ti/ Al and Cr/ Au deposited on N-face surface of n-GaN, which has (a) 5×10^{18} cm^{-3} carrier concentrations and (b) 1×10^{19} cm^{-3} carrier concentrations.

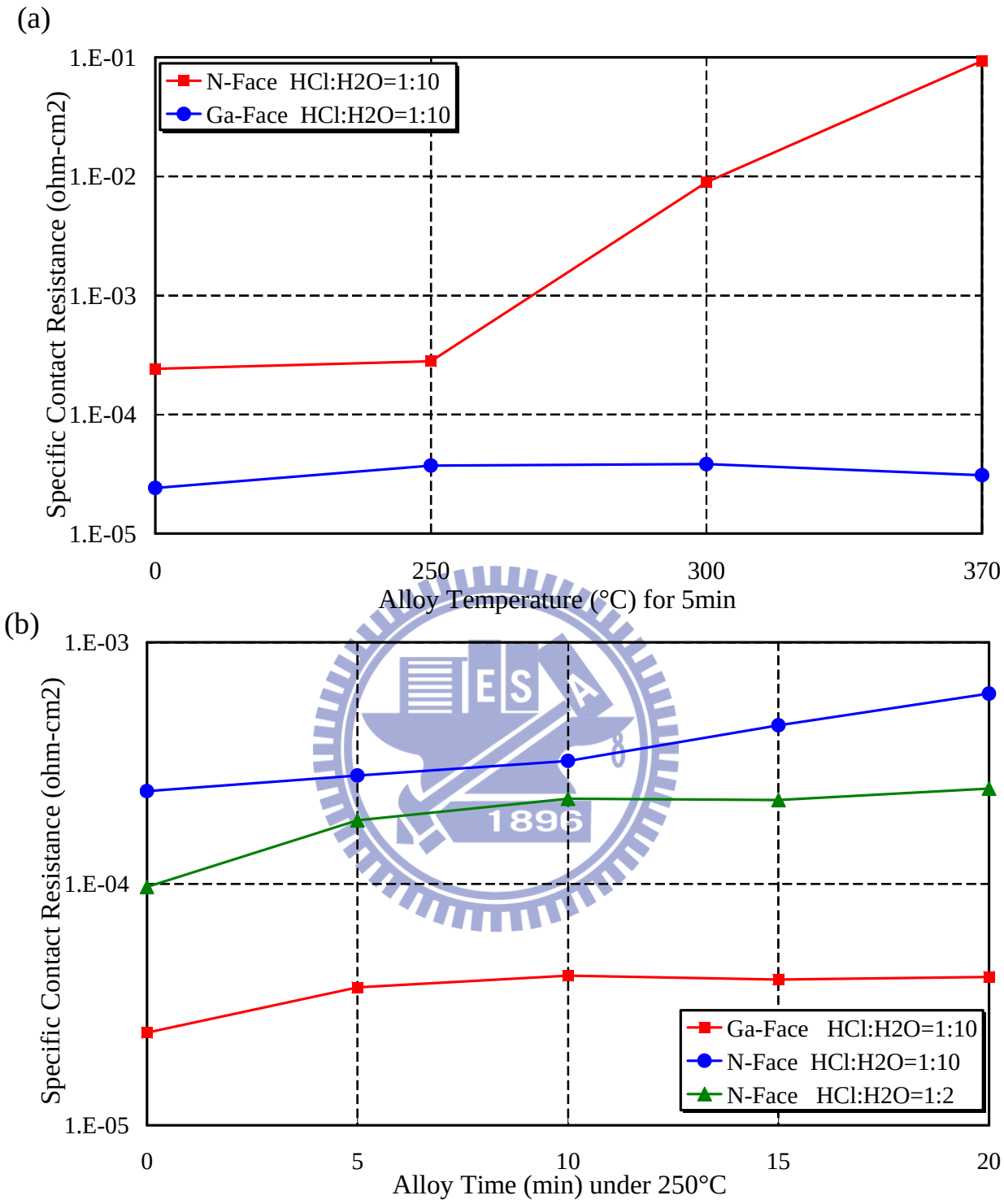


Figure 4.18: The specific contact resistance of (a) Ga-face and N-face under various alloy temperature and (b) Different chemical treatment of Ga-face and N-face under various alloy time.

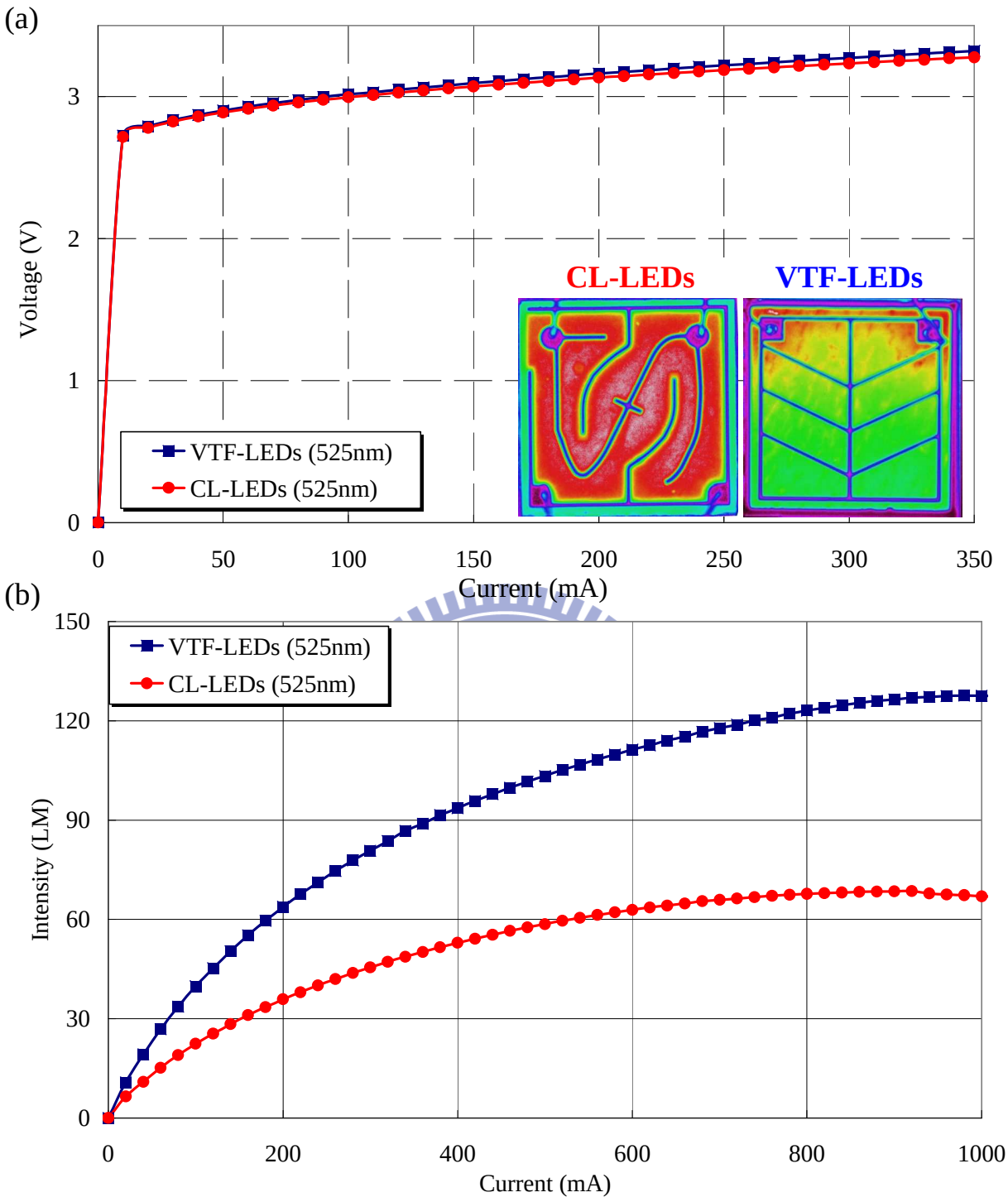


Figure 4.19: The (a) current-voltage and (b) lumen intensity characteristic of VTF-LEDs and CL-LEDs.

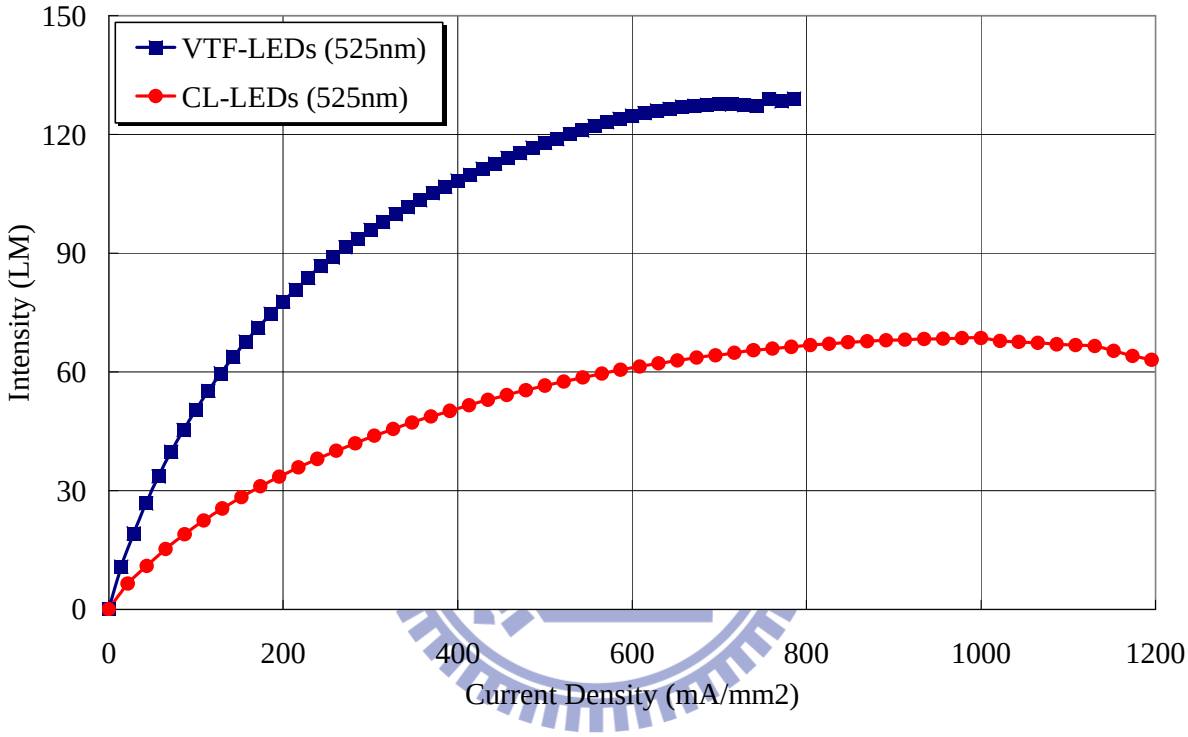


Figure 4.20: The current density versus lumen intensity of VTF-LEDs and CL-LEDs.

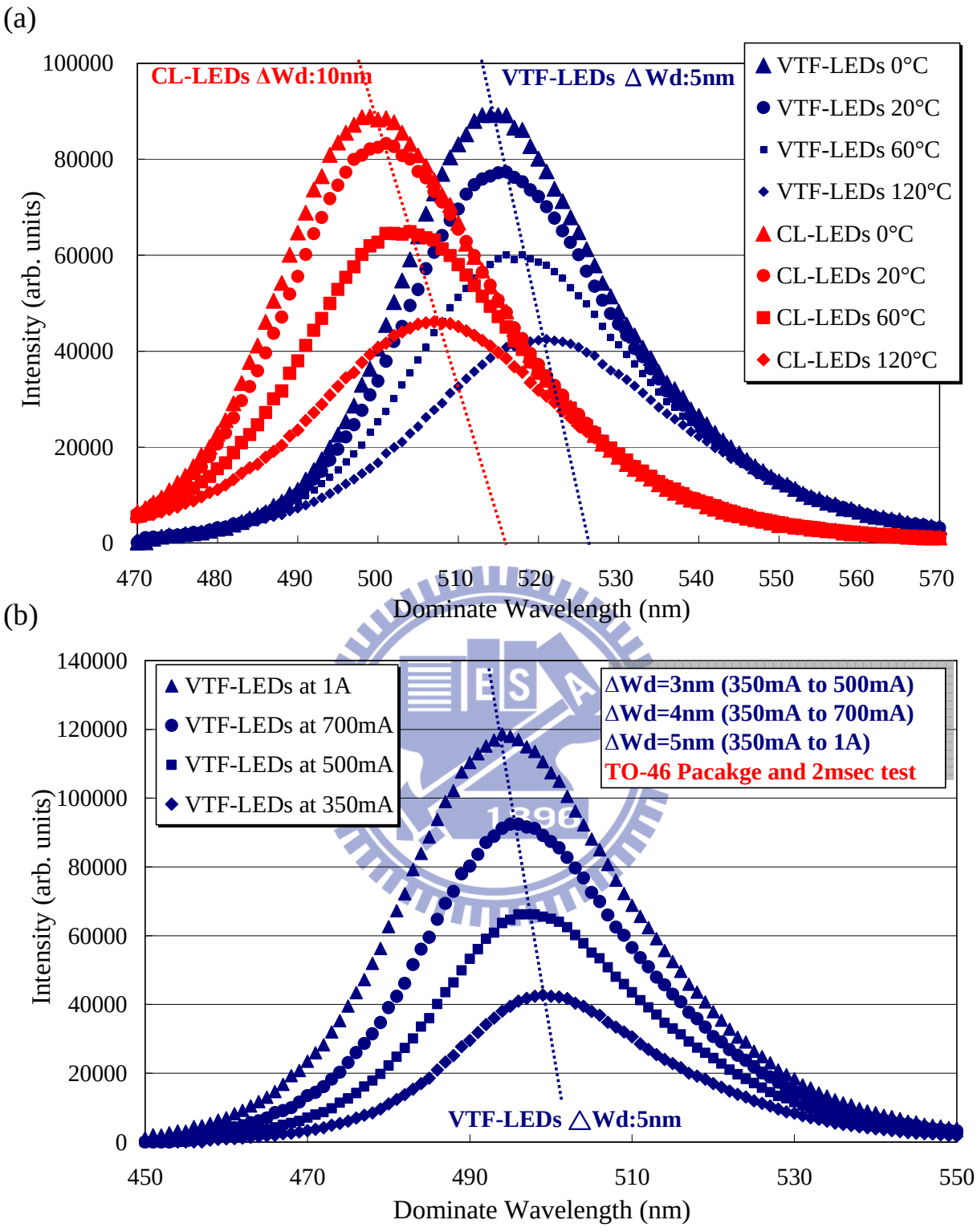


Figure 4.21: (a) The spectrum variation of of VTF-LEDs and CL-LEDs under different ambience. (b) The spectrum variation of VTF-LEDs under different current injection.

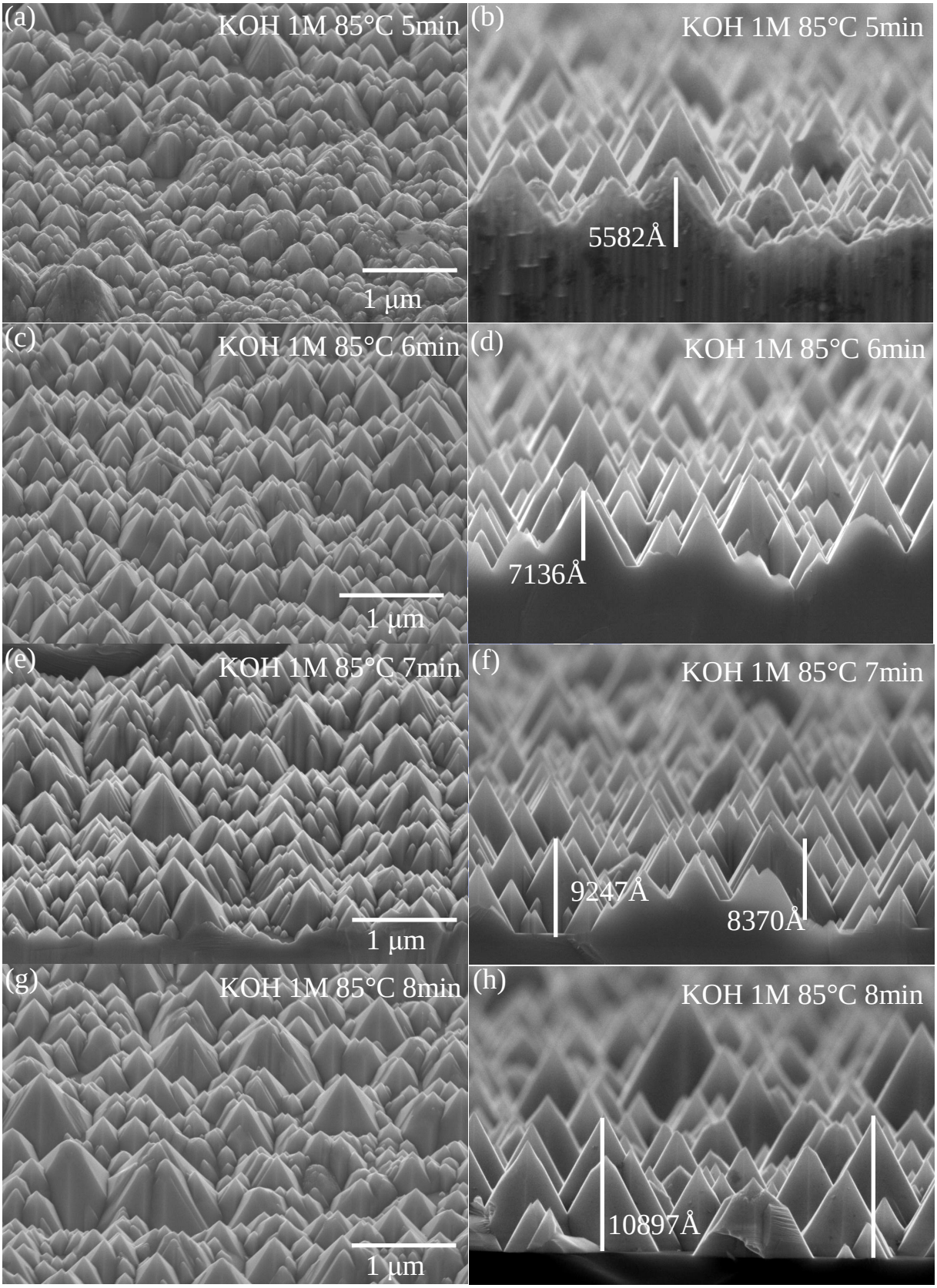


Figure 4.22: SEM images of the N-face surface morphology after immerging in 85ºC 1M KOH chemical for (a) (b) 5min, (c) (d) 6min, (e) (f) 7min, and (g) (h) 8min.

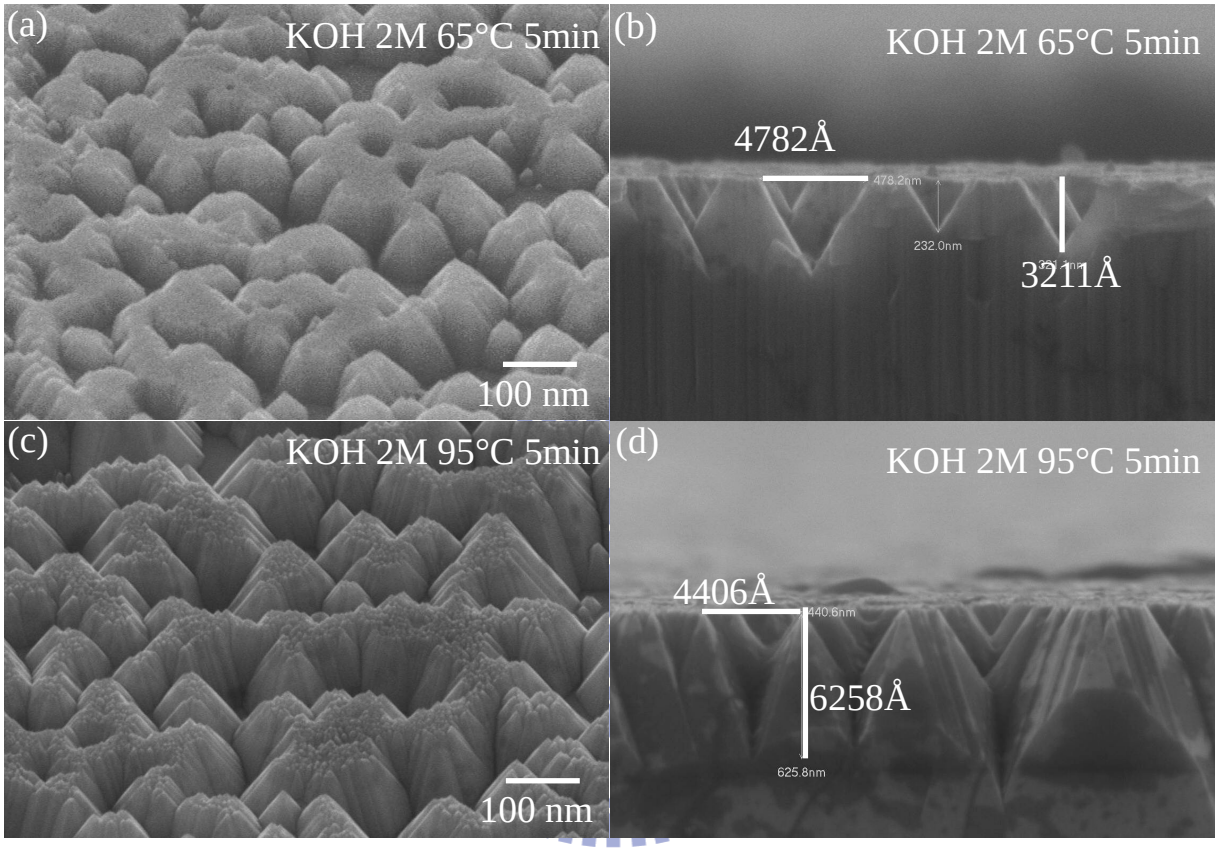


Figure 4.23: SEM images of the N-face GaN etching morphology using (a) (b) 65ºC and (c) (d) 95ºC 2M KOH for 5min.

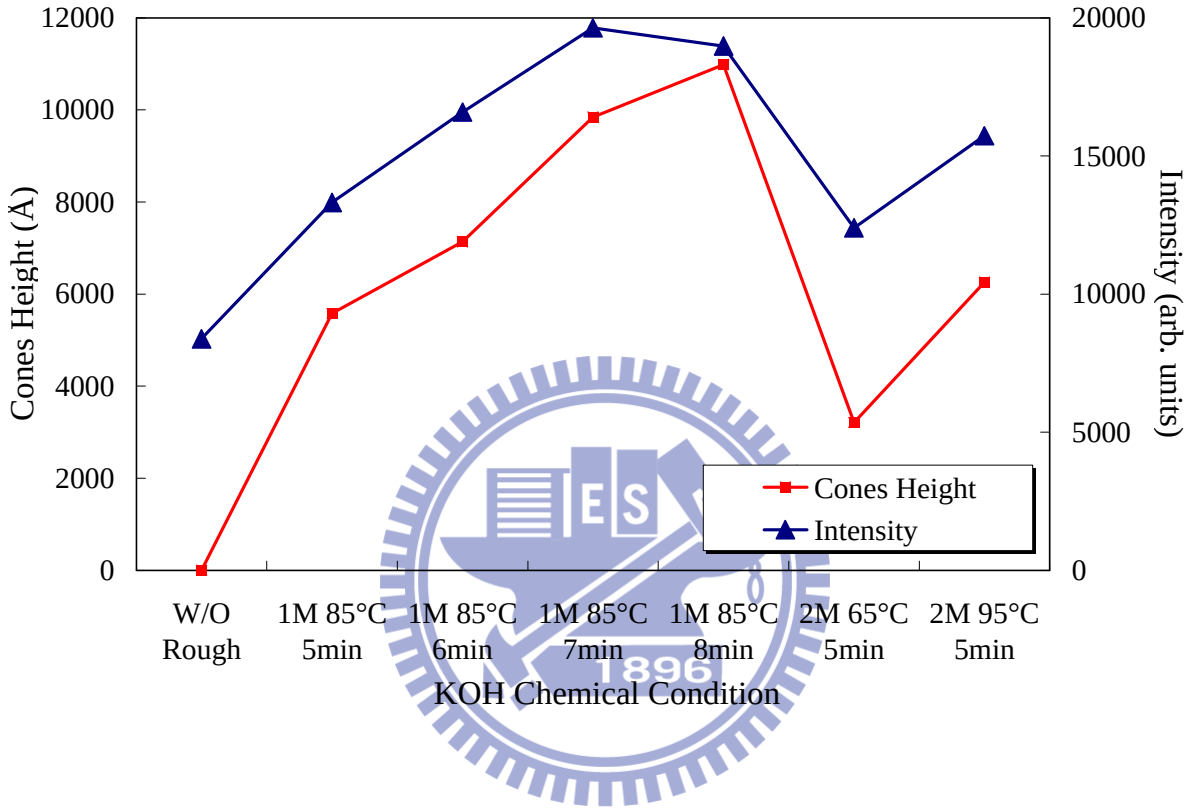


Figure 4.24: The hexagonal cones height and light intensity as function of the KOH chemical condition.

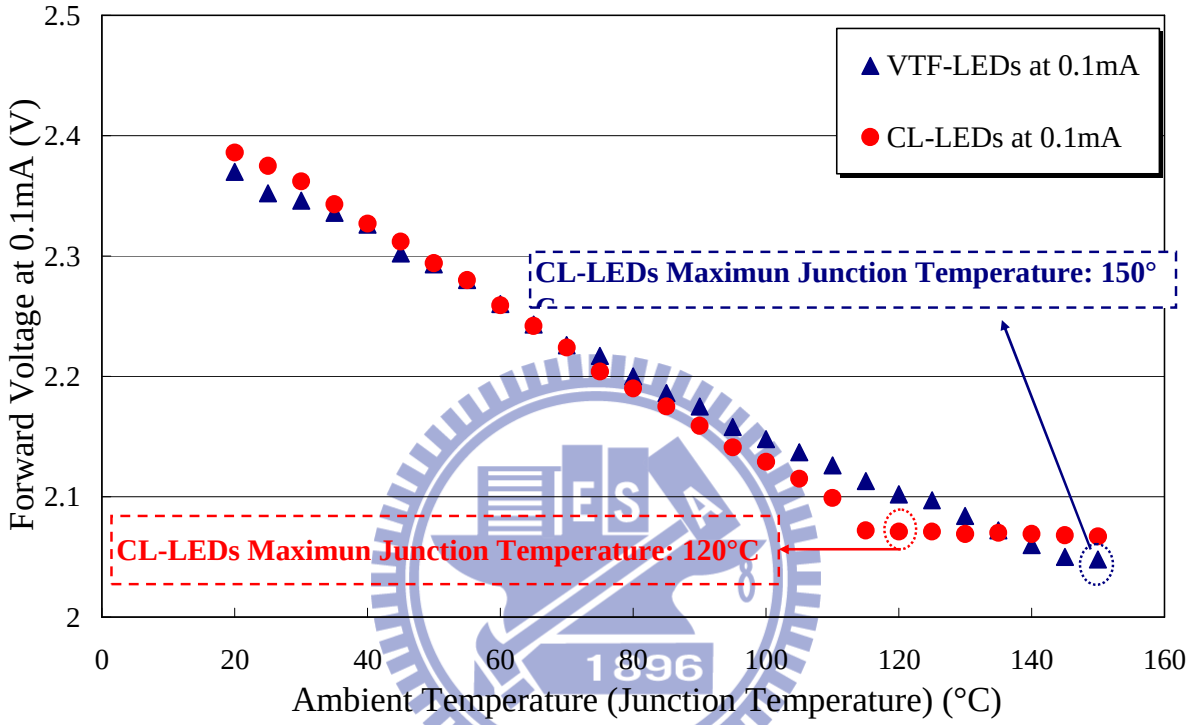


Figure 4.25: The VTF-LEDs and CL-LEDs were operated at 0.1 mA and measured forward voltage under varied ambient temperature (20°C to 150°C).

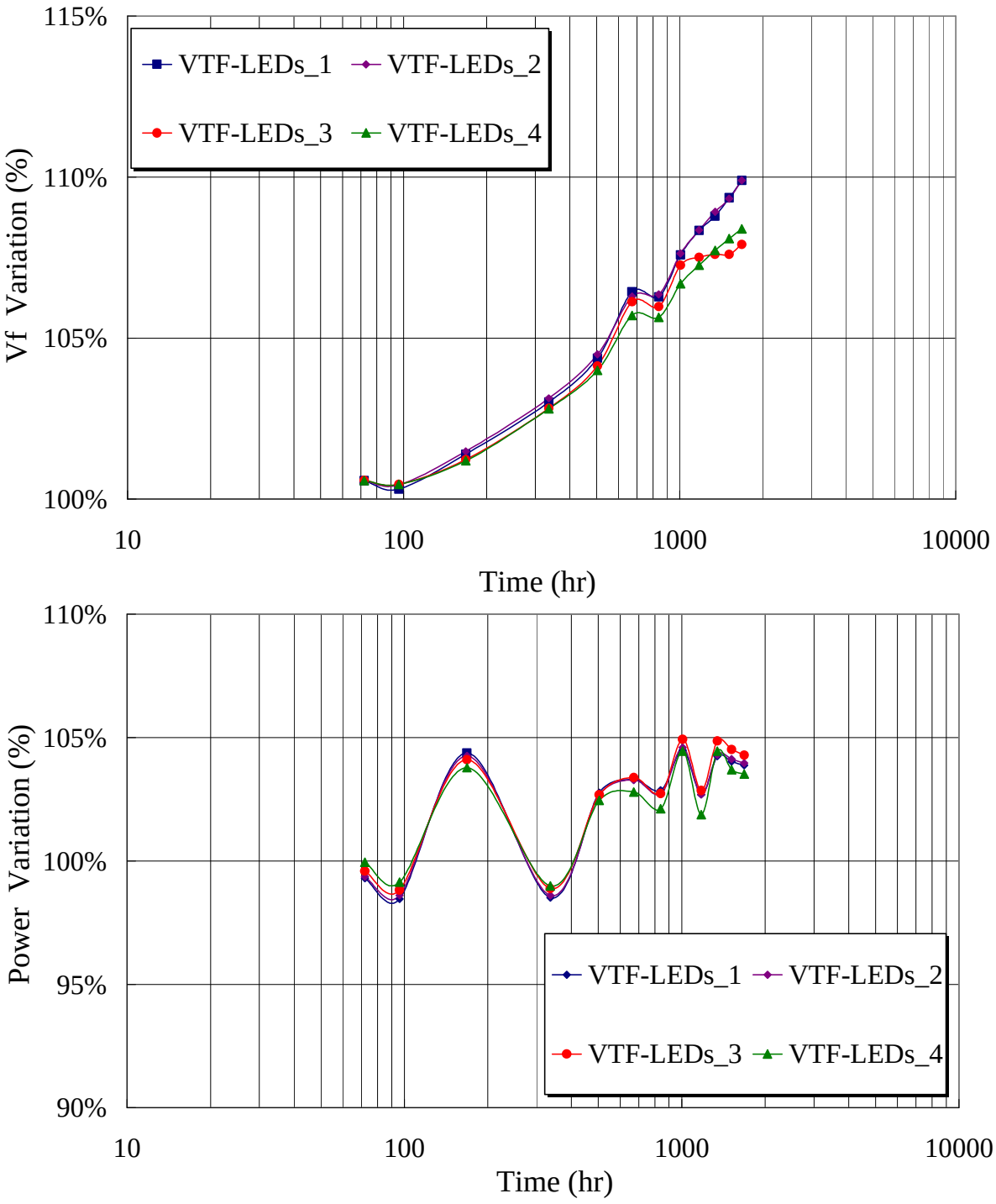


Figure 4.26: The VTF-LEDs reliability performance of (a) forward voltage variation and (b) power variation under 350 mA and room temperature for 1800 hours.

CHAPTER 5

Conclusions and Future Works

In summary, we have studied the wafer bonding technique applied to III-V compound semiconductor devices of AlGaInP-based RCLEDs, AlGaInP-based LEDs, and GaN-based LEDs in this dissertation. It is demonstrated that the wafer bonding technique is helpful to enhance efficiency and improve device inherent drawbacks from material limitation. The wafer bonding provides an ability that is the hetero-epitaxial growth without restricting lattice match. Furthermore, the primary device characteristic will not be sacrificed after wafer bonding process. By this wafer bonding technique, it is beneficial for III-V compound semiconductor devices applying to more advanced applications, such as high data rate communications, high power lighting marketing, and high efficiency requirements.

High-Performance AlGaInP-Based Resonant-Cavity Light- Emitting Diodes in Wafer Bonding Technology

In the case of AlGaInP-based MBRCLEDs with a silicon substrate have been fabricated by twice bonding. Firstly, the conventional RCLEDs with a GaAs substrate have superior performances due to the excellent epitaxy structure design and chip process. The 40 μm aperture RCLEDs could be achieved that the small-signal modulation bandwidths as high as 310 MHz at 20 mA current injection. The RCLEDs devices with 84 μm apertures had an output power of more than 3.5 mW at a driving current of 20 mA and a maximum efficiency of over 12 % with an epoxy-encapsulated package. Furthermore, the high performances MBRCLEDs, having a high thermal conductivity Si substrate, were fabricated via twice bonding technique of glue bonding and metal bonding processes. It is observed that the output power decay of MBRCLEDs were less than the RCLEDs. From RT to 100°C ambiance, the

output power droop of MBRCLEDs were -0.31, -1.78, and -2.5 dB under 20, 50 and 70 mA current injection respectively. The RCLEDs output power droop were -1.75, -3.03, -5.47 dB during 20, 50, and 70mA current injection respectively. The wall-plug efficiency difference ($\Delta_{efficiency}$) between the MBRCLEDs and the RCLEDs under 20 and 70mA current operating were 1.2% and 1.9%, respectively. The junction temperature variations of the MBRCLEDs were relatively smaller as compared with the RCLEDs. The MBRCLEDs with 84 μm apertures provided high wall-plug efficiency of 13.7 % and a smaller power drooped of -0.31dB from RT to 100ºC due to the better heat dispersion substrate. Furthermore, the stable beam profile, high reliability over 1000 hours and clearly eye diagram in high temperature operation. These excellent performances of the MBRCLEDs devices should be suitable for high temperature ambiance, high current injection and high data communication applications.

Light Extraction Enhancement of AlGaInP-Based Light- Emitting Diodes in Wafer Bonding Technique

The AlGaInP-based LEDs with a high thermal conductivity Si substrate or a transparent, shaped sapphire have been fabricated by metal bonding or glue bonding techniques. The purpose is enhancing light extraction efficiency, high performances in high current operating, and improving inherent drawbacks of devices. The GSS-LEDs with an oblique sapphire geometric substrate were fabricated via glue bonding. In this evolutional GSS-LEDs performances, the light output power could be enhanced 26.7% under 350 mA current injections as compared with GB-LEDs. Furthermore, it is proved that the GSS-LEDs structure could not only reduce the TIR effect but increase more probabilities of output light escaping from the transparent substrate with an oblique sidewall. Another novel flip-chip AlGaInP-LEDs structure which has a thick geometric sapphire substrate (GSSFC-LEDs) window layer are produced using glue bonding and flip-chip bonding techniques. As

compared with the conventional flip-chip AlGaInP-LEDs (CFC-LEDs), the GSSFC-LEDs have higher output power and wall-plug efficiency under the same injection current. The light intensity of GSSFC-LEDs have 31% enhancement as compared to CFC-LEDs. According to the output power results of the CGB-LEDs and CFC-LEDs, the power saturation effect of flip-chip structure (GSSFC-LEDs or CFC-LEDs) is less than the conventional n-side-up CGB-LEDs since the flip-chip structure has a better thermal dissipation path. It is helpful for devices applied to high current injection application, especially in short wavelength of AlGaInP-based LEDs. Last case of efficiency enhancement is AlGaInP-LEDs are bonded on Si substrate. The surface roughness textured in this structure is important, and there are three different surface types of LED-I, LED-II, and LED-III. The surface profile in LED-I devices is plane and without any surface textured. The micro-bowl surface textures having periodic arrangement were applied to LED-II surface, and the devices surface with micro-bowls added nano-rods is LED-III. Furthermore, added nano-rods textured in micro-bowls textured can enhance 17.7% due to the micro- and nano-scale surface texture conduces the less total internal reflection effect. The maximum wall-plug efficiency of LED-I, LED-II, and LED-III is 8.82, 12.74, and 14.15%, respectively. The 50% power angle of the LED-I, LED-II and LED-III is 115.4, 107.7 and 102.2°, respectively. According to the results, the LED-III with highest luminous intensity was established on off-axis once again.

High Performances of InGaN/ GaN Light-Emitting Diodes in Metal Bonding Technique

Firstly, the single electrode pad (SEP-LEDs) in GaN-based LEDs was demonstrated. The SEP-LEDs provides more mesa area for light radiation and uniform current spreading ability performances. The SEP-LEDs and CL-LEDs power under 20 mA forward current operating is 6.3 mW and 4.3 mW, respectively. The forward voltage of SEP-LEDs is similar to conventional GaN LEDs. Tthe SEP-LEDs also exhibits 66.3% enhancement of wall-plug

efficiency. Furthermore, the SEP-LEDs exhibit higher ESD resistance (< -1000V) ability due to the uniform current spreading path and the lower series resistance. Actually, the InGaN/ GaN vertical thin film LEDs (VTF-LEDs) structure is an important tread toward future LED lighting application. The conventional InGaN /GaN LEDs with a sapphire substrate were replaced with a high thermal conductivity Si substrate by metal-bonding and laser lift-off (LLO) technique. In order to improve total yield of epi-layer transfeered to Si substrate, the laser cut trench concept was applied for stress, heat releasing and avoids epi-layer crack from LLO process. The Al/ Ag metal was chosen to deposit on *p*-GaN layer as functions of *p*-ohmic and reflector. The Al/ Ag has thermal stability owing to Ag and Al atoms have eutectic point at 728K (455°C). Therefore, AlAg alloy is more suitable for applying to *p*-GaN ohmic and reflector metal in VTF-LEDs process. As we know, it is difficult to achieve *n*-ohmic contact on N-face surface of *n*-GaN $(000\bar{1})$. Several methods are implanted such as heavily doped on *n*-GaN layer and chemical cleaning on surface. Enhancing light extraction efficiency in VTF-LEDs structure is an important issue, and KOH chemical is implemented for surface random roughness process. The chemical condition of 85ºC 1M KOH for 7min has the brightest light intensity, and the cones height was approached to 8000~9500Å. The VTF-LEDs has lower forward voltage, uniform current spreading, high efficiency under the same current density, less wavelength variation in high current and high temperature ambience operating, higher maximum junction, and excellent thermal impendence as compared with CL-LEDs. Finally, the VTF-LEDs has a superior reliability performance, the variations of electrical and optical were fewer after 1800 hours operating.

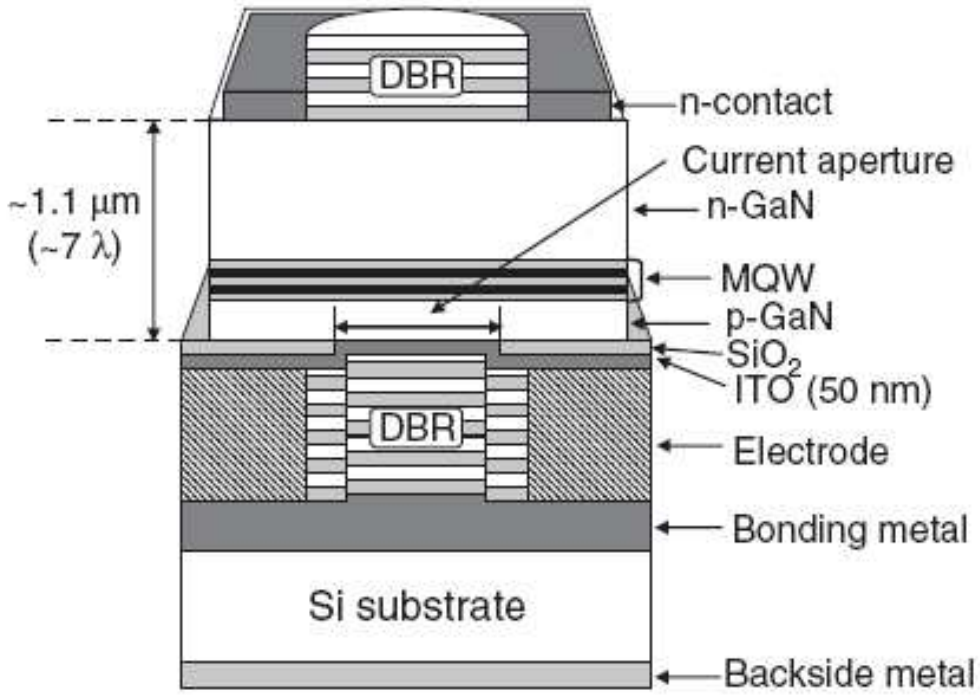
Future Works

With these achievements, we have the enough wafer boning technique ability to further develop novel, advanced III/V compound semiconductor devices such as GaN-based vertical-cavity surface emitting laser diodes (VCSELs) and without considering lattice mismatch epitaxial growth. By the wafer bonding technique could be able to solve not only lattice mismatch in epitaxy but also material inherent restriction. In InGaN/ GaN-based electroptical devices epitaxial growth, the totally thickness of n-GaN layer must over 4 μm-thick. It is caused of epi-layer quality and doped requirement. Therefore, it is difficult to achieve some requirements of electroptical device, such as short cavity length requirement for VCSELs and photonic crystal LEDs.

Recently, the GaN-based VCSELs are very attractive for high-density optical storage, laser printing and display applications due to their superior characteristics, which include a low threshold current, single longitudinalmode operation, a circular spot profile, and the ability to be used in two-dimensional arrays. The success of optically pumped GaN-based VCSELs however current-injection lasing of GaN-based VCSELs at room temperature has not been realized. This is mainly due to two problems. One is the lack of suitable semiconductor distributed Bragg reflectors with high reflectivity and high conductivity performance. The other problem is that it is difficult to obtain a low-resistive *p*-type GaN layer for the current spreading layer required for lateral current injection. In order to overcome above mentioned problems, a novel structure in future shoul be developed by metal bonding and laser lift-off process as shown in figure 5.1(a). In detail structure, an indium tin oxide (ITO) layer is inserted between *p*-GaN layer and DBRs, and Ta_2O_5/ SiO_2 diecectric DBRs are used for *p*- and *n*-DBRs materials. In micro-cavity VCSELs, the conventional AlN/ GaN materials for *n*-DBRs are replaced with Ta_2O_5/ SiO_2 diecectric DBRs due to difficult and inherent handicap epitaxy in DBRs material quality. This n-side up and vertical current

injection structure has a highly thermally conductive Si substrate by wafer bonding and the sapphire substrate was removed by laser lift-off. By this way, we can reduce the *n*-GaN layer thickness for reducing cavity length. Therefore, CW lasing is able to achieve under this VCSEL structure at RT by current injection and less issue in epitaxy. Furthermore, we could also implement wafer bonding and laser lift-off technique to produce optically pumped GaN-based VCSELs, as shoen in figure 5.1(b). We can simply identify qualities of multiple quantum wells, dielectric *p*- and *n*-DBRs, and VCSELs optical performances previously. By this way, we have more chance of achieving GaN-based micro-cavity VCSELs at RT by CW current-injectin operation.

(a)



(b)

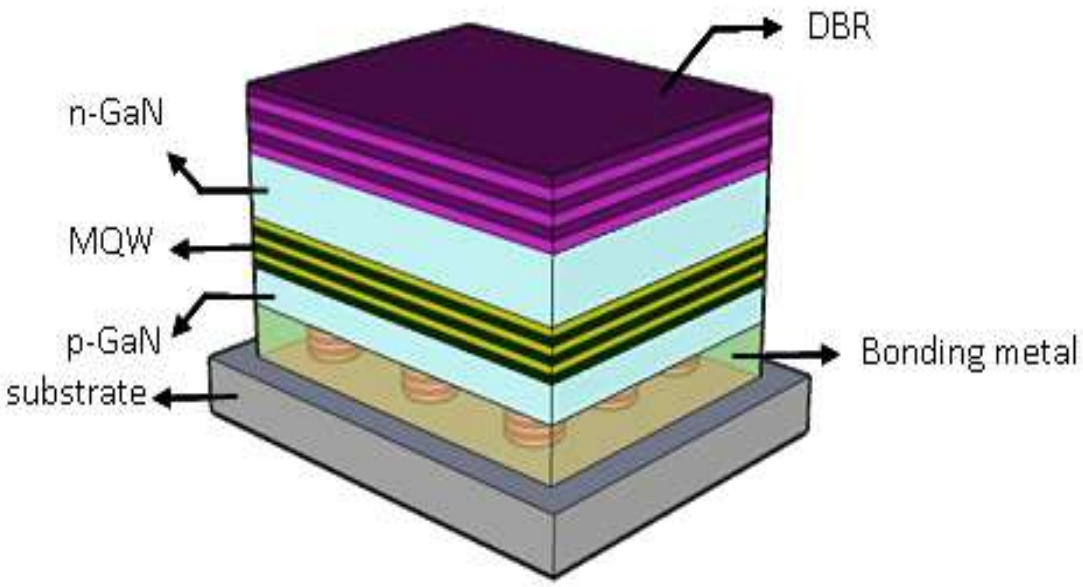


Figure 5.1 Schematic diagram GaN-based VCSELs structure of (a) vertical current injection and (b) optical pumping configuration fabricated by using wafer bonding and laser lift-off process.

Publication List

Journal Papers:

- ***Yea-Chen Lee***, Chia-En Lee, Bo-Siao Cheng, Tien-Chang Lu, Hao-Chung Kuo*, Shing-Chung Wang, and Shu-Woei Chiou, "High-Performance 650 nm Resonant-Cavity Light-Emitting Diodes for Plastic Optical-Fiber Application," *JJAP*. vol. 46, no. 4B, pp. 2450-2453, 2007

- ***Lee, Y. C.***, Kuo, H. C., Lee, C. E., Lu, T. C., Wang, S. C., and Chiou, S. W., "High-Temperature Stability of 650-nm Resonant-Cavity Light-Emitting Diodes Fabricated Using Wafer-Bonding Technique on Silicon Substrates," *IEEE Photon. Technol. Lett.* vol. 19, no. 14, pp. 1060-1062, 2007.

- Chia-En Lee, ***Yea-Chen Lee***, Hao-Chung Kuo, *Senior Member, IEEE*, Meng-Ru Tsai, B. S. Cheng, Tien-Chang Lu, Shing-Chung Wang, *Life Member, IEEE*, and Chia-Tai Kuo,"Enhancement of Flip-Chip Light-Emitting Diodes With Omni-Directional Reflector and Textured Micropillar Arrays," *IEEE Photon. Technol. Lett.* vol.19, no.16, pp. 1200-1202, 2007

- Chia-En Lee, ***Yea-Chen Lee***, Hao-Chung Kuo, *Senior Member, IEEE*, Meng-Ru Tsai, Tien-Chang Lu, Shing-Chung Wang, *Life Member, IEEE*, and Chia-Tai Kuo, "Luminance Enhancement of Flip-Chip Light-Emitting Diodes by adopting a geometric sapphire shaping structure," *IEEE Photon. Technol. Lett.* vol.20, no.3, pp. 184-186, 2007.

- C. E Lee, ***Y. C. Lee***, H. C. Kuo, M. R. Tsai, T. C. Lu and S. C. Wang," High brighness GaN-based flip-chip light emitting diodes by adopting geometric sapphire shaping," *Semicond. Sci. Technol.* **23** no. 2, pp. 1-5, 2007.

- ***Y. C. Lee***, C. E. Lee, H. C. Kuo, T. C. Lu and S. C. Wang," Enhancing the light extraction of AlGaInP based LEDs fabricated via geometric sapphire shaping," *IEEE Photon. Technol. Lett.* vol.20, no.5, pp. 369, 2008.

- C. E. Lee, ***Y. C. Lee***, H. C. Kuo, T. C. Lu and S. C. Wang," High Brightness InGaN/GaN Flip-Chip Light-Emitting Diodes with Triple Light Scattering Layers," *IEEE Photon. Technol. Lett.* vol.20, no.8, pp. 659, 2008.

- C. E. Lee, ***Y. C. Lee***, H. C. Kuo, T. C. Lu and S. C. Wang," Further Enhancement of Nitride-Based Near-Ultraviolet Vertical-Injection Light-Emitting Diodes by Adopting a Roughened Mesh-Surface," *IEEE Photon. Technol. Lett.* vol.20, no.10, pp. 803, 2008.

- ***Y. C. Lee***, C. E. Lee, T. C. Lu, H. C. Kuo and S. C. Wang, "Small GaN-based light-emitting diodes with a single electrode pad fabricated on a sapphire substrate," *Semicond. Sci. Technol.* **23**, pp. 1-5, 2008.

- ***Yea-Chen Lee***, Hao-Chung Kuo, Chia-En Lee, Tien-Chang Lu, and Shing-Chung Wang, "High Performance $(Al_xGa_{1-x})_{0.5}In_{0.5}P$-Based Flip-Chip Light-Emitting Diode with a Geometric Sapphire Shaping Structure," *IEEE Photon. Technol. Lett.* vol.20, no.23, pp.1950, 2008.

- C. E. Lee, C. F. Lai, ***Y. C. Lee***, H. C. Kuo, T. C. Lu, and S. C. Wang, "Nitride-Based Thin-Film Light-Emitting Diodes with Photonic QuasiCrystal Surface," I*EEE Photon. Tech. Lett*., V21, N5, p331~333, 2008.

- Chia En Lee, B.S. Cheng, ***Yea-Chen Lee***, Hao-Chung Kuo, Tien-chang Lu, and Shing-Chung Wang, "Output Power Enhancement of Vertical-Injection Ultraviolet Light-Emitting Diodes by GaN-Free and Surface Roughness Structures," *Electrochem. Solid-State Lett*., V12, N12, H44-H46, 2008.

- ***Yea-Chen Lee***, Hao-Chung Kuo, Bo-Siao Cheng, Chia-En Lee, Ching-Hua Chiu, Tien-Chang Lu, Shing-Chung Wang, Tien-Fu Liao, and Chih-Sung Chang, "Enhanced Light Extraction in Wafer-Bonded AlGaInP-Based Light-Emitting Diodes via Micro- and Nano-Scale Surface Textured," *IEEE Electron. Device Lett*., Vol.10, No.10, pp.1054, 2009.

- ***Yea-Chen Lee***, Hao-Chung Kuo, and Tien-chang Lu, "Light Extraction Enhancement of Metal Bonding AlGaInP-Based Light-Emitting Diodes by Varied Surface Textures,"

Electrochem. Solid-State Lett., 2009 (under review).

- ***Yea-Chen Lee***, Hao-Chung Kuo, and Tien-chang Lu, "Enhancing the Output Power of InGaN/GaN LEDs Using AlAg Alloy Omnidirectional Reflector for Electrode Pads and Mesh-Line Metal," *Electrochem. Solid-State Lett*., 2009 (under review).

- ***Yea-Chen Lee***, Hao-Chung Kuo, and Tien-chang Lu, "Output Power Enhancement in InGaN Light-Emitting Diodes by Omnidirectional Reflector of AlAg Alloy for Pads and Mesh-Line," *IEEE Electron. Device Lett*., 2009 (under review).

- ***Yea-Chen Lee***, Hao-Chung Kuo, and Tien-chang Lu, "Investigation Light Intensity and Electrostatic Discharge of GaN-Based Light-Emitting Diodes with Photonic Quasi-Crystal Patterned on P-GaN Surface and N-side Sidewall Roughing," *IEEE Electron. Device Lett*., 2009 (under review).

Conference Papers:

- ***Y. C. Lee***, C. E. Lee, S. W. Chiou, H. C. Kuo, T. C. Lu and S. C. Wang, "High performance of 650 nm resonant cavity light emitting diodes for plastic optical fiber applications", B-3-5, the 2006 International Conference on **Solid State Devices and Mayterials 2006** (SSDM 2006) Yokohama, Sept 12-15, 2006 (oral presentation)

- ***Yea-Chen Lee***, Chia-En Lee[1], Hao-Chung Kuo[1], Shing-Chung Wang," Improving Light Extraction Efficiency of $(Al_xGa_{1-x})_{0.5}In_{0.5}P$-Based Flip-Chip Light-Emitting Diode with a Geometric Sapphire Shaping Structure", **Solid State Devices and Materials 2007** (SSDM 2007)

- Bo-Saio Cheng, ***Yea-Chen Lee,*** Chia-En Lee, Hao-Chung Kuo, Tien-Chang Lu, and Shing-Chung Wang, "Improving Light Extraction Efficiency of $(Al_xGa_{1-x})_{0.5}In_{0.5}P$-Based Flip-Chip Light-Emitting Diode with a Geometric Sapphire Shaping Structure," **Solid State Devices and Materials 2008** (SSDM 2008)

- Bo Siao Cheng, ***Yea Chen Lee***, Hao Chung Kuo, Tien Chang Lu, Shing Chung Wang, "Light Extraction Enhancement of Wafer-Bonded AlGaInP-Based Light-Emitting Diodes with Micro- and Nano-Scale patterned Surface," **Solid State Devices and Materials 2009** (SSDM 2009)