國 立 交 通 大 學

光電工程學系 光電工程研究所

博 士 論 文

多晶矽薄膜電晶體的空間與時間變動性探討

Characterization of the Spatial and Temporal Variation of Poly-Si TFTs

研 究 生：黃士哲

指 導 教 授：戴亞翔 博士

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摘要

本論文探討多晶矽薄膜電晶體的在空間與時間上的特性變動。本論文雖然主要動機出發於主動式顯示器電路應用，但其結果則可擴大應用於顯示器以外的領域。本文首先討論在量產線上的元件特性變動，發現元件的變動特性除了有很嚴重變動範圍之外，其變動行為亦沒有模型能夠精確描述；這將在設計多晶矽薄膜電晶體電路時造成很大的問題。因此我們先參考在在金-氧-半導體電晶體(MOSFETs)結構中對於元件變動的討論，並且以類似的方式針對薄膜電晶體的變動性提出可能的變動因素。由此我們提出一”枕木型”布局方式並對此布局內的元件參數進行統計。此枕木型布局方式的特色是元件間的距離盡可能的縮到最小並且在此最小間距內，兩相鄰元件間的長距離變動(long-range variation)可以大幅降低。所量測到的元件參數呈現非對稱且不集中的分佈，與先前一般所預測的高斯分佈有明顯落差。利用電子學裡的小信號想法，我們可以將兩相鄰元件間的長距離變動與微觀變動(micro variation) 區分開，並可以進一步探討元件間的微觀變動模型。對元件的起始電壓與載子遷移率而言，N 型與 P 型元件其微觀變動行為均呈現較集中與對稱的行為。我們提出兩個數學式以精確描述其微觀變動的參數分佈，並根據此兩模型探討元件的變動行為在數位與類比電路上造成的

影響。此外，我們亦利用此模型預測元件在不同元件尺寸下的變動行為。在論文研究方向上，利用枕木型元件布局可使元件的變動範圍大幅減小，以起始電壓為例，其標準差由 0.5 V 縮減至 0.03 V，這將有助於我們之後的元件時間變動性的討論，不會因元件空間上的變動行為而遮蓋住其在時間上的變動行為。

接下來我們討論元件在時間上的變動性。此處，元件的時間變動性可以單純的理解為其在直流與交流下的可靠度行為，並將於不同的章節裡個別討論。對於元件在直流操作下的可靠度行為，我們首先回顧元件在兩大劣化機制下，亦即為熱載子效應與自發熱效應，先前文獻已經發表的劣化行為。雖然已有很多文獻探討元件在這兩大劣化行為下所產生的元件特性改變，關於這兩個操作條件下元件的電容行為部份卻只有零星的文獻。我們討論在這兩個劣化行為下元件的電容特性變化，發現元件模擬軟體並不能很完整的描述元件的電容特性在不同量測頻率下的行為。因此我們採用另一個方法，利用相對較易取得的元件電流特性推論元件的電容特性，提出一由閘極界電層電容與通道電阻所組成的元件模型，利用探討元件的阻抗中的電容項與電阻項，我們定義一個特別的點 P_C 以幫助我們利用元件的電流特性去探討其電容特性。由於阻抗的電容項與量測頻率有關，P_C 的位置亦與量測頻率有關。利用這個方式，我們探討元件在兩個主要劣化條件下的行為，同時也提出在這兩個操作條件下，元件在操作後的電路模型。對於兩個特別的電容特性在關閉區的行為，亦即 N 型元件在自發熱操作條件後與 P 型元件在熱載子操作條件後的現象，將會有一特別的討論。

接下來我們探討元件在閘極交流操作下的劣化行為。由應用端出發，我們發現元件在液晶顯示器面板內絕大部分時間處於閘極關閉區而其集極則持續給予交流訊號。然而，關於這個操作條件卻沒有任何已知的文獻探討其劣化行為。比較其閘極與源極電壓差以及閘極與集極電壓差，我們可以將其操作條件類比為閘極關閉區內的交流操作，而其源極與集極則均接地。N 型元件在這樣的操作條件下，其電流特性出現了載子遷移率的下降，而電容則有扭曲(Distortion)的現象。對 P 型元件，其電流特性則出現了載子遷移率的上升，而電容則在關閉區出

現異常的上昇。我們亦探討元件的劣化行為與閘極電壓的參數，以及其電壓範圍、頻率與工作週期(Duty cycle)的關聯。然而，由於其閘極電壓均低於其起始電壓，在通道裡應該沒有通道載子，也因此這個劣化行為無法利用先前由 Uraoka 所提出的模型解釋。在此我們依然使用前文所使用的元件模型，並且同樣討論元件在此操作條件下的阻抗行為。我們推論在此操作情況下元件的源極與集極接面將會有很大的電場，並進一步造成元件的劣化。然而，這樣的推論無法被直接驗證因為我們並沒辦法直接探測元件內的電壓分佈，因此我們使用一稱作 gated p-i-n 測試結構，其結構與 TFT 相似但其一端源極與集極的參雜經過更改，使其橫向結構類似一 p-i-n 元件。採用這種結構的特色是這樣的元件擁有和與 TFT 相似的結構，但其通道內的電壓可以由一端的接面控制，進而可以讓其另一接面上形成大電場。這樣，經由比較交流操作後的 TFT 與直流操作後的 gated-p-i-n 元件，我們先前所提出的理論獲得證實—處於很大逆向偏壓源極與集極接面的劣化是閘極關閉區下交流操作的劣化主因。關於 N 型與 P 型元件的不同劣化行為亦有深入討論。此外，亦比較了幾個相似的劣化條件，發現不論載子的來源來自於導通區的集極電流，或是關閉區的漏電流，抑或是由導通區切向關閉區時，由通道區被空乏掉的載子，一但接面上有大電場的產生，均會出現類似熱載子效應的劣化行為；由另一角度來看，其亦可被總結為一廣義的熱載子效應。總結而言，本文所提出的模型與其劣化模型將會為元件的時間變動特性提供有用的資訊，也可幫助評估元件的時間變動行為。

Characterization of the Spatial and Temporal Variation of Poly-Si TFTs

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Abstract

This work focuses on the variation behavior of poly-Si TFTs both spatially and temporally. This work is mainly enlightened from, but not limited to, the display electronics. First the spatial variation of the devices is studied for the devices from the mass production line. The serious variation behavior and no description nor trend for the device variation makes it rather difficult for designers to develop the circuits composed of poly-Si TFTs. Thus we referred to the cases in MOSFETs and analogically proposed factors for the variation behavior for poly-Si TFTs. Based on the idea, the special layout called crosstie layout is proposed, measured and the device parameters are extracted and statistically summarized. The feature of the crosstie layout is that the devices are located as close as possible and in such case the long-range variation can be greatly reduced for the two adjacent devices. The device parameters show apparent asymmetric and non-centered distribution, which is much different from the usual Gaussian distribution assumption. A method enlightened from the electronics is proposed to decouple the long-range and micro variation and by finding the difference between the adjacent devices the true micro variation profile

can be examined. The micro variation behaviors for the threshold voltage and mobility are found to be more centered and symmetric for both n-type and p-type devices. Two equations are proposed to well fit the micro variation and also based on the models the effects of device variation on the analog and digital circuits are simulated and discussed. In addition, based on the models, the projected device variation behavior for devices with different device dimension is also provided. By utilizing the crosstie layout, the variation behavior of the devices is greatly reduced, take the threshold voltage for instance, from 0.5 V to 0.03 V. The reduced variation also facilitates the following study of temporal variation, in which the effect of spatial variation can be greatly relieved and not to cover the effect of temporal variation.

Then we focus on the temporal variation of poly-Si TFTs under various operation conditions. Here the temporal variation can simply correspond to the reliability issue under DC and AC operation, which would be respectively discussed in the separate chapters. For the DC operation section, we first review the two main degradation mechanisms for the poly-Si TFTs under DC operation, namely the hot carrier effect and the self heating effect. Though there have been so many papers on the device degradation behavior under these two stress conditions, there are very few papers about their capacitance behavior. We study the C-V behavior for the device after the two stress conditions and find that the simulation tool may be incomplete in properly describing the frequency dependence in the C-V curves. Thus we use another approach to infer the C-V curves from the readily-accessible I-V curves. Based on the proposed model composed of the gate insulator capacitance and channel resistance, we compare the magnitude of the capacitance term and the resistance term for the device's impedance and the critical point called P_C is found to help distinguish the ON region and the OFF region in the C-V curves inferred from the I-V curves. Since the capacitance term is dependent on the measuring frequency, the position of the point

P_C also changes with the measuring frequency. Following the same manner, the C-V behavior for the device after the two stress conditions are examined and the corresponding circuit elements, possibly the capacitance or the resistance, are proposed respectively. Special discussion would be given on the capacitance behaviors for the n-type device after self-heating stress and the p-type after hot carrier stress since they both somehow show the increase of the capacitance for the lower gate voltage in C-V curves.

Next we study the reliability behavior for the device under gate dynamic operation. Started from the application, we find that in TFT-LCD applications the TFTs in the pixels mostly stay in the gate turned-off region with the drain signal dynamically toggling. However, there is almost no study of the reliability behavior on such operation condition. We consider the gate-to-source voltage difference V_{GS} and the gate-to-drain voltage difference V_{GD} and analogically study the reliability behavior for the gate voltage dynamically toggling in the OFF region while the source and drain electrodes are both grounded. The device shows mobility decrease in the I-V curves and shift as well as distortion in its C-V curves for the stressed n-type device, while for the p-type device the mobility increases and the OFF current decreases after stress. The dependency for the device degradation on the pulse parameters, namely the pulse range, the frequency and the duty ratio of the applied signal, is also studied. However, since the pulse voltage is all kept below its threshold voltage, there should be no channel carrier induced beneath the gate electrode and thus the degradation behavior could not be explained by the model proposed previously by Uraoka. At this point we resort to the circuit model again and one more time we discuss the impedance under such stress condition. It is then inferred that under the gate AC operation the channel resistance and the large electric field across the junctions could be the main degraded region. Nevertheless, such inference is hard

to probe and we use another test structure named the gated p-i-n device, in which the device has the similar structure to TFTs but one side of the doping is changed to make the device laterally resemble the p-i-n diodes. The feature for adopting such gated p-i-n device is that this device has the similar structure to the TFTs while the channel voltage can be set from one side of the electrodes. Thus, this enables us the capability of forming large electric field across one junction to simulate the condition of gate AC OFF region stress for poly-Si TFTs. Then, by examining the capacitance curves of the AC-stressed TFTs and the DC-stressed gated p-i-n devices after stress, the aforementioned mechanism is verified. The degradation in junction with the large electric field on it is thus found to be responsible for the degradation of gate dynamic operation in the OFF region and the discussion for the different behaviors for the n-type device and p-type device is also provided. Also the reliability behaviors under several other stress conditions are discussed. It is found that, no matter what the carrier source may be the inversion channel carriers, the leakage current or even the inversion channel carriers swept because the gate pulse is to be turned-off, once the large electric filed is across the junction, the carriers would more or less become the hot carrier and result in the similar degradation behavior. In other words, they can be categorized as the "generalized hot carrier effect." To summarize, the finding of the mechanism as well as the proposed circuit model should provide useful information for the understanding and evaluation of the temporal variation for poly-Si TFTs.

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Chapter 1

Introduction

1-1 Overview of poly-Si TFT technology

Thin film transistor is a metal-oxide-semiconductor structure that can be fabricated on various kinds of substrates by using almost all kinds of deposition techniques [1-1]. Recently as for the substrates there have been the glass substrates, flexible substrates, stainless steel and so on. And as for the active region material, the film could be the silicon-based semiconductor, metal oxide and organic material [1-2]. The main feature of the TFT itself is the device can be formed upon various substrates and the material can be chosen from the applicable sources other than the high temperature single crystalline silicon wafer [1-3]. Such feature makes the TFT very suitable for the active display electronics since for each pixel the switching element is required and it is almost impossible for the single crystalline silicon device to be formed inside the respective pixel [1-4]. The first generation of active matrix liquid crystal displays (AMLCDs) used a-Si:H TFT as the pixel switching device. The main advantages of the a-Si:H TFT are the low process temperature (no higher than 600 degree Celsius) that can avoid damaging the glass substrate and the low leakage current that can avoid grey level shift as the TFT is turned off. However, the low electron field effect mobility (typically below 1 $cm^2V^{-1}S^{-1}$) of a-Si TFTs limits the capability of advanced and integrated circuit. Integration of the driving circuit on display panel in parallel with the same substrate is very desirable not only to reduce the module cost but to improve the system reliability.

For the last decade, polycrystalline silicon thin-film transistors (poly-Si TFTs)

have attracted much attention because of their widely applications in active matrix liquid crystal displays (AMLCDs) and organic light-emitting diodes (OLEDs). Compare with a-Si:H TFTs, poly-Si TFT can provide higher electron mobility (by two orders of magnitude) and its higher driving current allows smaller TFT size to be used as the pixel-switching elements, resulting in higher aperture ratio and lower parasitic gate-line capacitance for improved display performance. In addition to flat panel displays, poly-Si TFTs have also been applied into some memory devices such as dynamic random access memories (DRAMs), static random access memories (SRAMs), electrical programming read only memories (EPROM), electrical erasable programming read only memories (EEPROMs). Among the poly-Si technologies, low temperature polycrystalline silicon thin-film transistors (LTPS TFTs) are primarily applied on glass substrate since higher process temperature may cause the substrate bent and twisted. Up to now, hundreds of researches have been reported to develop various technologies for improving the performance and reliability of LTPS TFTs. Since the electron field-effect mobility of LTPS TFTs is larger than a-Si:H TFTs but smaller than MOS transistors, it is expected that matured poly-si technology may realize several special functions such as the DAC (digital to analog converter), touch panels and sensors, even the memory and MPEG decoder as shown in figure 1-1[1-5]. Figure 1-2 shows the roadmap as for the expected development for the poly-Si TFTs as well as the integrated functions [1-5]. Researchers expect that as the mobility and the device performance keeps improving, the driver circuits and some special value-added functions can thus be formed by the use of poly-Si TFTs even for the lower performance CPU (Central processing Unit) and eventually form the system on glass (SOG) technology. In 2003 Sharp announced the prototype of the system on glass technology with the 8-bit CPU on it, as shown in figure 1-3 [1-6]. This somehow proved that for the display electronics the poly-Si TFTs can replace the

externally connected bond ICs and the perspective of the SOG technology is truly applicable.

1-2 Review and Motivation

Though the adoption of the poly-Si TFTs may be of beneficial, the devices are found to suffer serious variation, as shown in figure 1-4 [1-7]. Devices from predominant process condition still exhibit electrical behavior variation. Though the device structure is similar to MOSFETs, the variation behaviors of TFTs are much worse than those of MOSFETs. In the application using MOSFETs with high sensitivity to the mismatch variations such as current mirrors, digital-to-analog converters, and sense amplifiers, the statistical variation analysis would be a very important verification step. Owing to the low process temperature, poly-Si TFTs have different process from IC industry. Since the variation of device behavior may directly affect the circuit performance and reliability prediction, it would be of practical interest to have a clear understanding of how the variation may come and the behaviors the variation could be. In the scope of this thesis, since the poly-Si TFTs are capable of advanced circuitry and the perspective of SOG, the uniformity issue would become more critical. Another point of the study on device variation is that refer to the previous study the diversified device behavior would seriously affect the study of device reliability, and thus before studying the temporal variation it is required to find the devices with the variation effect as small as possible. In chapter 3 we studied the variation behavior as well as the effect of device variation on the circuit performance.

As for the temporal variation, it is also another point required to be deeply understood. From the practical viewpoint, the understanding of the reliability for the device under DC and AC operation can help designers to properly evaluate and estimate the practical device as well as the circuit performance. And as for the

viewpoint of studying the mechanism, the deeper understanding of the mechanism can also help to devise methods to reinforce the device reliability. Though there are many papers on the I-V behaviors of poly-Si TFTs under DC stress, there are very few papers on the C-V behaviors for the device after DC stress, as shown in figure 1-5 [1-8]. In chapter 4, we would study the current transfer characteristics, namely the I_D-V_G curves, and the capacitance characteristics for the device under DC operation.

On the other hand, as for the device under AC operation, though in this case it would be more similar to the conditions in the real operations, there are not so many papers on it as in the case for the device under DC operation, in which the summary is given in figure 1-6 [1-9]. As for the AC operation, there are more parameters for the applied signal and it should be a good starting point to study the reliability for the conditions in applications. In real applications, the TFTs mainly act as the switches and thus the applied gate signal would toggle between the ON and OFF regions, in which the reliability for the devices had been reported by Uraoka [1-10]. However, there is still an important part that has not been reported and such operation condition occurs for most of the time in the pixel driving in the TFT-LCD panels. That is, the reliability for poly-Si TFTs under gate OFF region with the drain AC signals. In chapter 5 we studied the reliability behavior of the poly-Si TFTs under such operation conditions and proposed the model to describe it. The model is verified by using a special test structure and the discussion for the difference between the AC operation and the DC operation in the OFF region is also provided. Though the motivations for all the aforementioned three parts are all originated from the real applications, the mechanisms as well as the models should still provide valuable information for the designers from the viewpoints both of the real application and mechanism understanding.

1-3 Thesis Structure

There are six chapters in this dissertation, in which can be summarized in figure 1-7. First the poly-Si technology is introduced in chapter 1 and then the experimental, such as the fabrication and the measurement of the devices, is described in chapter 2. Then, we focus on the spatial variation first; the parameter distribution and the impact as well as the insights of the variation would be studied in chapter 3. Next, we study the temporal variation, in which the device behavior, namely the I-V and C-V behaviors after DC and AC operation, would be examined for both n-type and p-type devices and thereafter the similar circuit model is used to describe the degradation in chapter4 and 5. Chapter 6 gives the summaries and future work. The structure is in the other way listed below for indexing:

Chapter 1 Introduction

1-1. Overview of poly-Si TFT technology

1-2 Review and Motivation

1-3 Thesis Structure

Chapter 2 Experimental

2-1 Device Fabrication

2-2 Equipment and Experiment Setup

2-3 Extraction Methods of Device Parameters

Chapter 3 Characterization of Spatial Variation of Poly-Si TFTs

3-1 Review and Motivation

3-2 Classification and Characterization of Variation

3-3 Impacts and Insights of Device Variation

3-3-1 Impacts of Device Variation on Circuit Performance

3-3-2 Insights of Device Variation

3-4 Summaries

Chapter 4 Characterization of Temporal Variation of Poly-Si TFTs: under DC Operation

4-1 Review and Motivation

4-2 Reliability Behavior under DC Operation: n-type Device

4-3 Reliability Behavior under DC Operation: p-type Device

4-4 Comparison and Discussion

4-5 Summaries

Chapter 5 Characterization of Temporal Variation of Poly-Si TFTs: under AC Operation

5-1 Review and Motivation

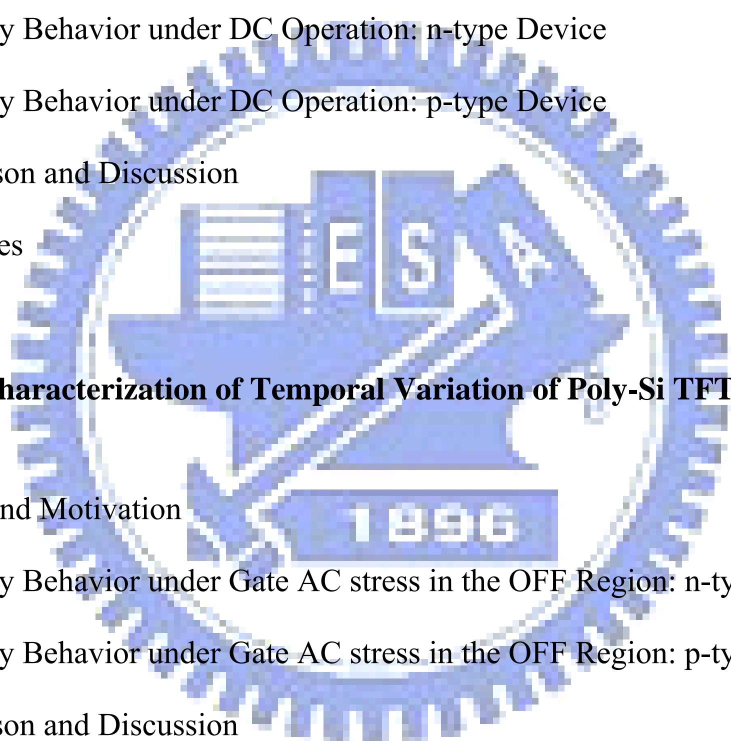
5-2 Reliability Behavior under Gate AC stress in the OFF Region: n-type Device

5-3 Reliability Behavior under Gate AC stress in the OFF Region: p-type Device

5-4 Comparison and Discussion

5-5 Summaries

Chapter 6 Summaries and future work



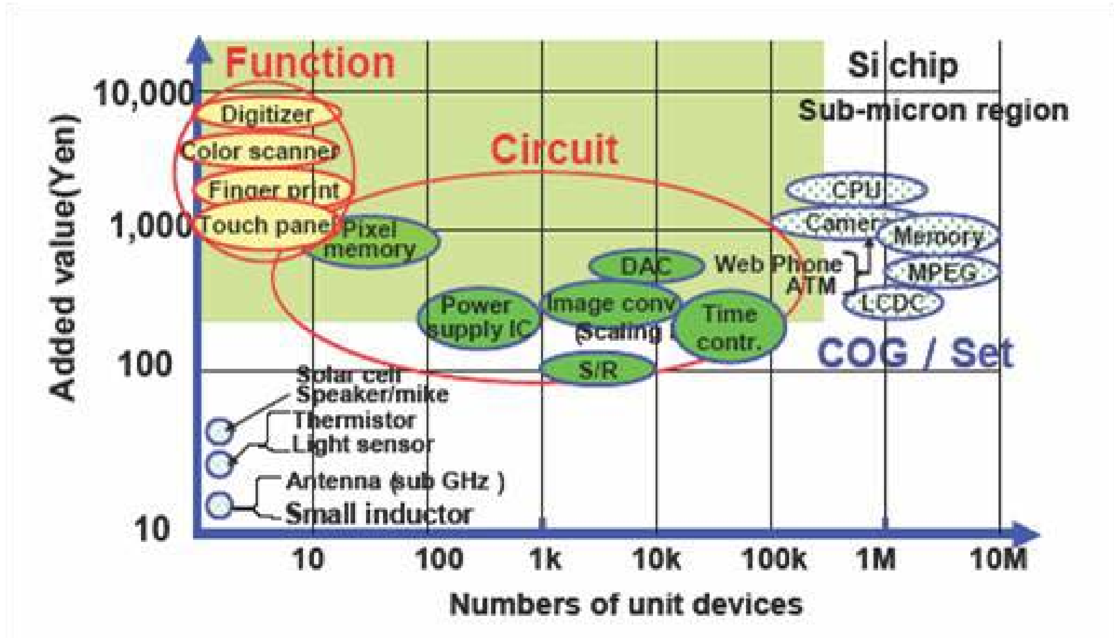
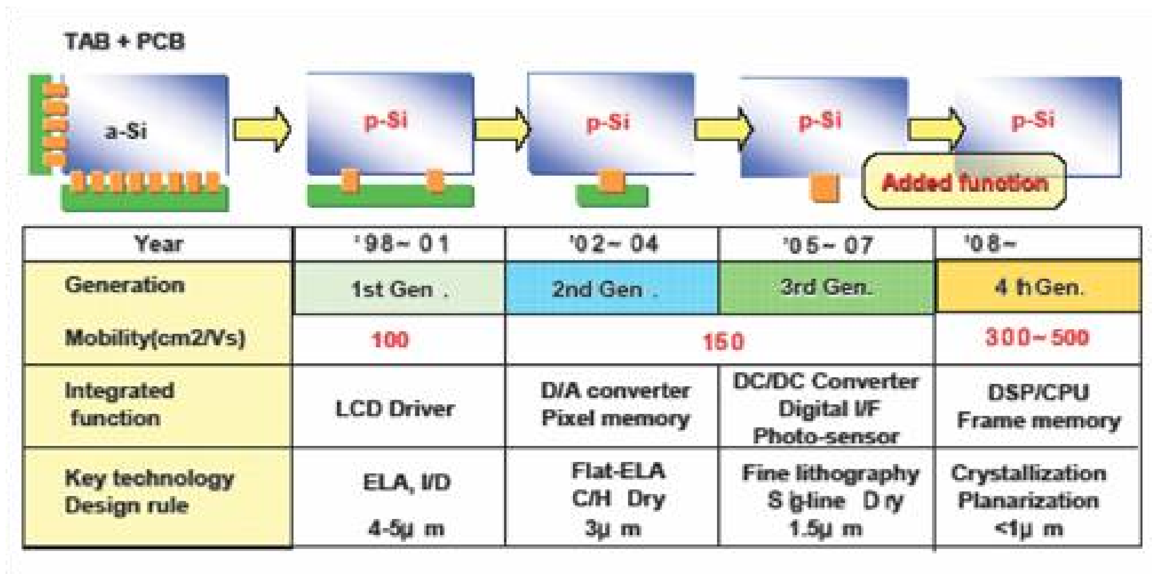


Figure 1-1 The possible value-added functions for the poly-Si TFT circuits

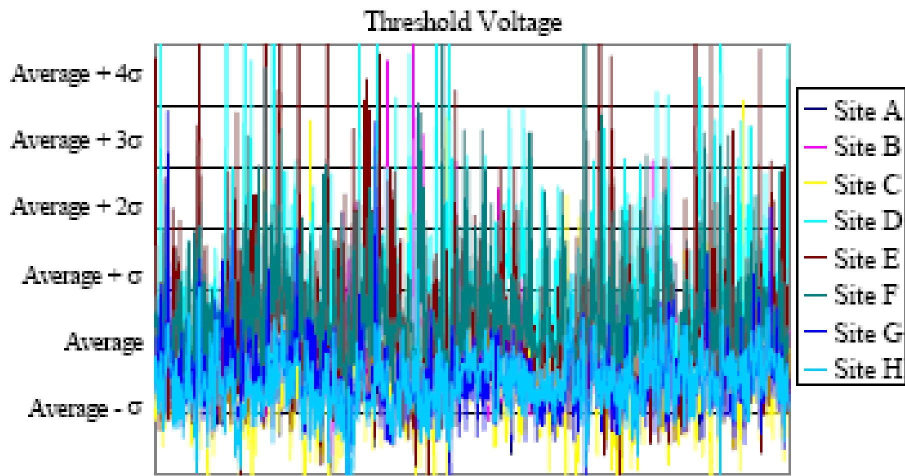


Year	'98~ 01	'02~ 04	'05~ 07	'08~
Generation	1st Gen .	2nd Gen .	3rd Gen.	4 h Gen.
Mobility(cm2/Vs)	100	150		300~500
Integrated function	LCD Driver	D/A converter Pixel memory	DC/DC Converter Digital I/F Photo-sensor	DSP/CPU Frame memory
Key technology Design rule	ELA, I/D 4-5μ m	Flat-ELA C/H Dry 3μ m	Fine lithography S g-line D ry 1.5μ m	Crystallization Planarization <1μ m

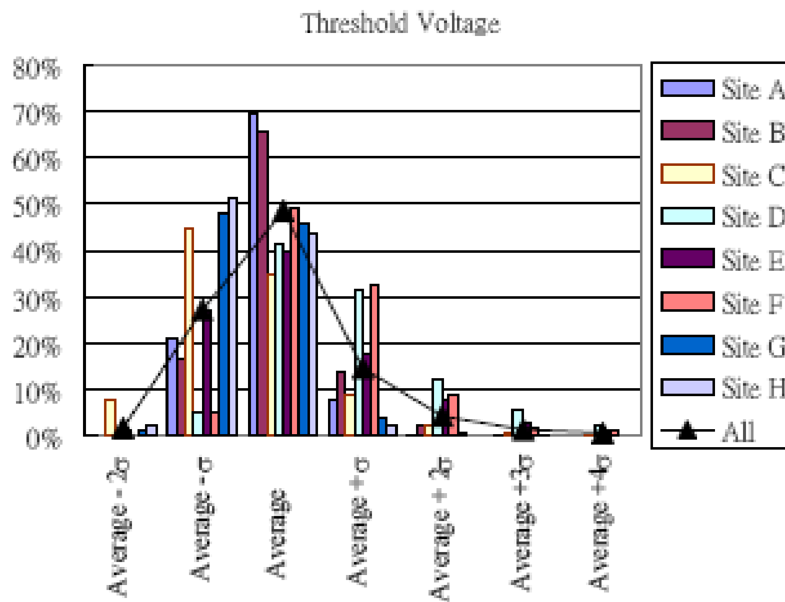
Figure 1-2 The roadmap and the perspectives for the poly-Si TFT development

1896

Figure 1-3 The system on glass prototype with the poly-Si TFT technology from Sharp



(a)



(b)

Figure 1-4 Device parameters for poly-Si TFTs in which the serious variation occurs

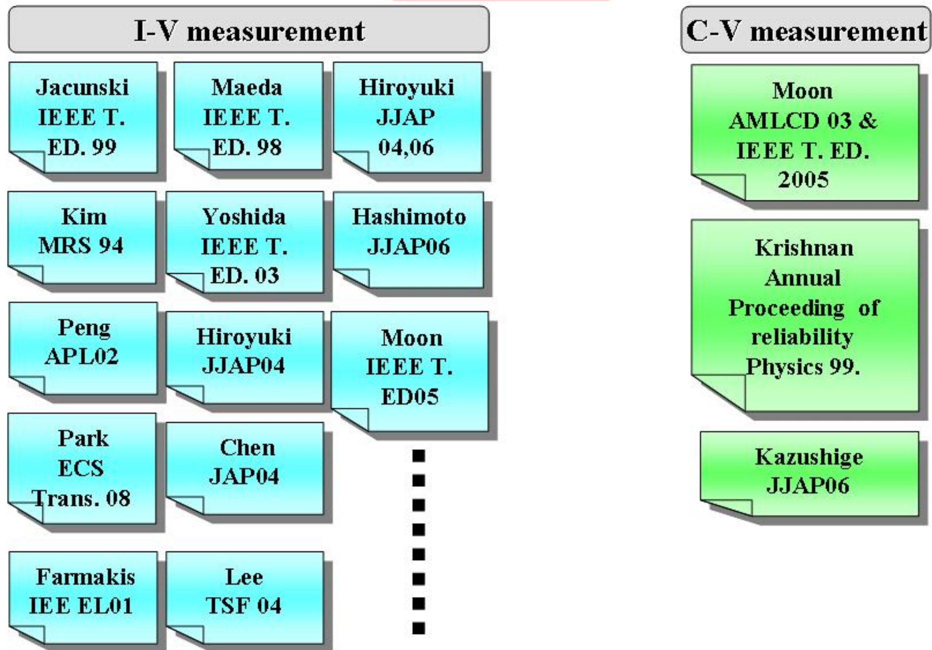


Figure 1-5 Comparison and summary for the previous reliability works on the I-V and C-V behaviors for poly-Si TFTs

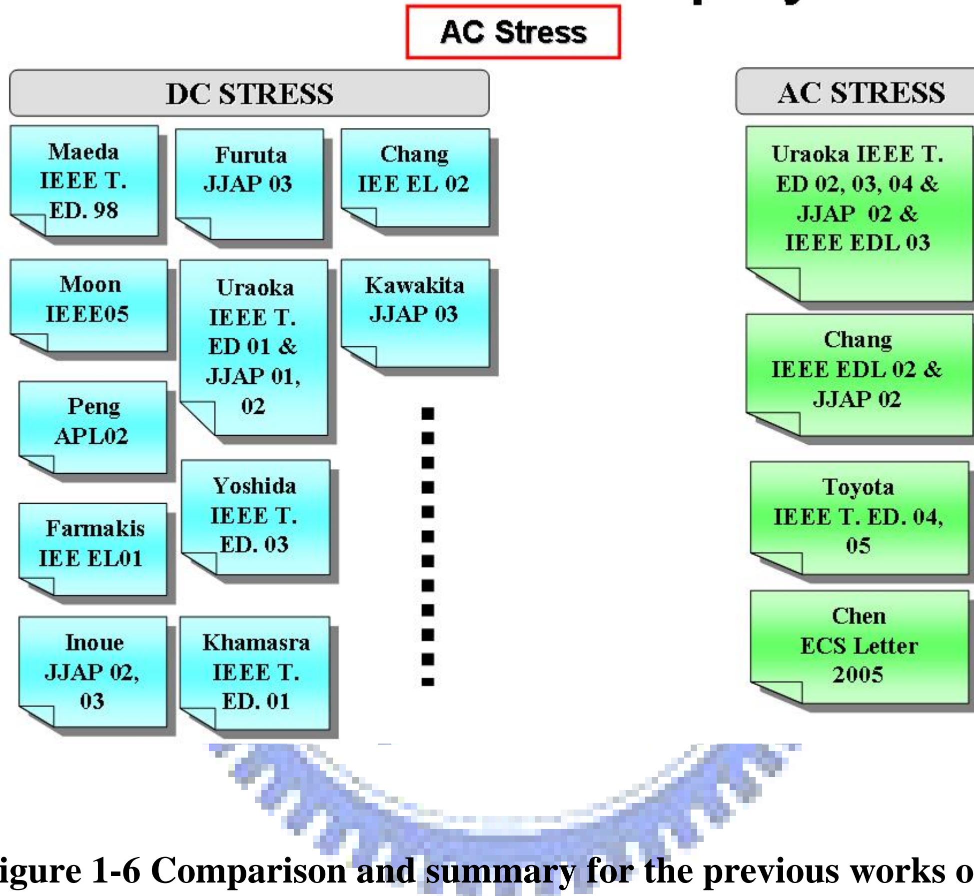


Figure 1-6 Comparison and summary for the previous works on the reliability behaviors for poly-Si TFTs under DC and AC operation

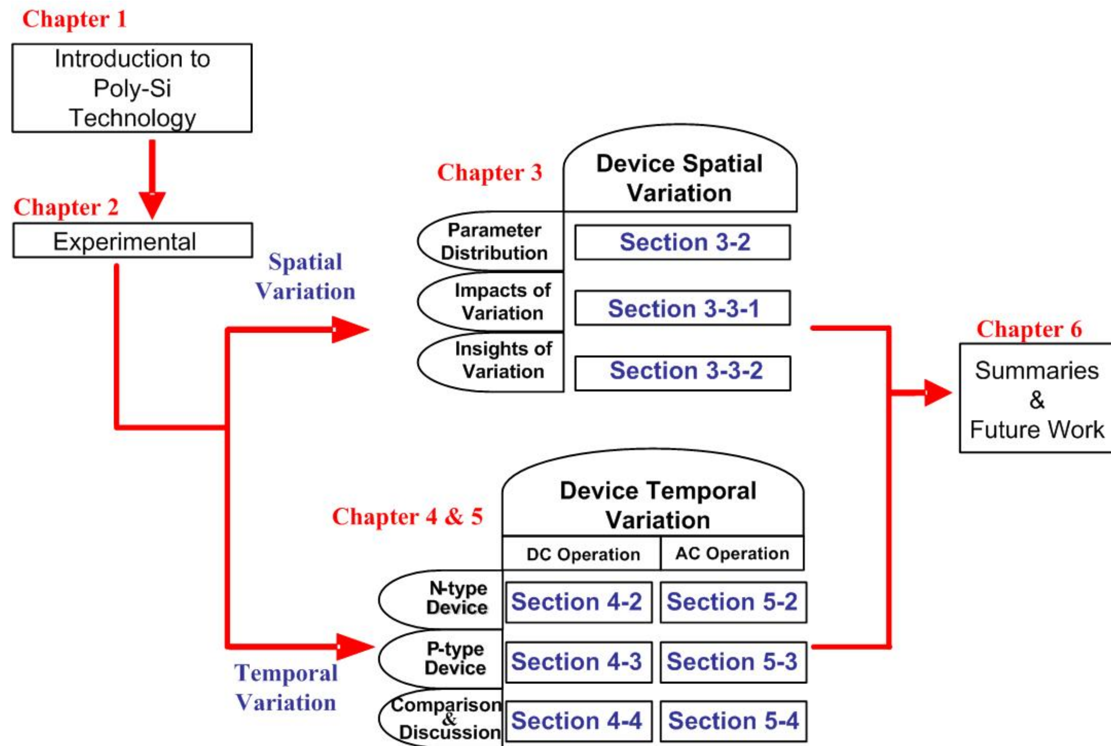


Figure 1-7 The figure illustrating the structure of this dissertation

Chapter 2

Experimental

Before going deep into the characterization of the poly-Si TFT, the experimental is described in this chapter. In section 2-1, the device fabrication flow is described. Next, the way how the device is measured and stressed and how the device parameters are extracted are explained.

2-1 Device Fabrication

The process flow of TFTs is described below. Top gate LTPS TFTs with width / length dimension of 20 μm / 5 μm were fabricated using low temperature process. Firstly, the buffer oxide and a-Si:H films with thickness of 50 nm were deposited on glass substrates with PECVD. The samples were then put in the oven for dehydrogenation. The XeCl excimer laser of wavelength 308 nm and energy density of 400 mJ/cm^2 was applied. The laser scanned the a-Si:H film with the beam width of 4 mm and 98% overlap to recrystallize the a-Si:H film to poly-Si. After poly-Si active area definition, 100 nm SiO_2 was deposited with PECVD as the gate insulator. Next, the metal gate was formed by sputter and then defined. For n-type devices, the lightly doped drain (LDD) and the n$^+$ source/drain doping were formed by PH_3 implantation with dosage 2×10^{13} cm^{-2} and 2×10^{15} cm^{-2} of PH_3 respectively. The LDD implantation was self-aligned and the n$^+$ regions were defined with a separate mask. The LDD structure did not use on p-type devices. The p$^+$ source/drain doping was done by B_2H_6 self-align implantation with a dosage of 2×10^{15} cm^{-2}. Then, the interlayer of SiN_X was deposited. Subsequently, the rapid thermal annealing was conducted to activate the dopants. Meanwhile, the poly-Si film was hydrogenated.

Finally, the contact hole formation and metallization were performed to complete the fabrication work. The structure cross section view for the n-type poly-Si TFT is given is figure 2-1. The gated p-i-n devices, proposed to verify the validity of the reliability mechanism in chapter 5, are fabricated in parallel with the poly-Si TFTs to ensure the identical process condition.

2-2 Equipment and Experiment Setup

In this section, the equipments to measure the device characteristics, namely the transfer behavior I_D-V_G curves and the capacitance curves, are described. In addition, the apparatus to DC or AC stress the device as well as the AC pulse waveform is also illustrated.

The I_D-V_G curves for the devices are measured by the Agilent 4156A precision semiconductor parameter analyzer. The C-V curves of the gate-to-source capacitance C_{GS} and gate-to-drain capacitance C_{GD} before and after stress with different frequencies are measured with the HP 4284A precision LCR meter. The concept of operation of the apparatus is to find the effective impedance of equivalent circuit of the device under test between the probing nodes and via the circuit theory, the capacitance of the device can then be obtained. Before measuring the capacitance behavior, for every frequency the measure correction is performed with the open-circuit and short-circuit mode respectively for the needles before and after probing the electrode to eliminate the effect of the parasitic components in the surrounding and during probing.

The DC stress is performed by the Agilent 4156A precision semiconductor parameter analyzer, which is the same one to measure the transfer characteristics. The AC stress is performed by the Agilent 41501B pulse generator. Several parameters for the stress pulse are modulated to examine the dependence of device reliability on the

applied pulse parameters. The basic parameters of AC signal consists of frequency (f), signal high level (Vgh), signal low level (Vgl), high-level time (Vgh), low-level time (Vgl), rising time (Tr), and falling time (Tf). Fig. 2-2 shows the waveform of the AC signal. In AC signal, the definition of individual parameter is given as follow:

$T = Tr + T_vgh + Tf + T_vgl$

$f = 1/T$

Duty ratio = (T_vgh)/T

and T is the signal period.

2-3 Extraction Methods of Device Parameters

Three important device parameters are extracted and studied in this work: the threshold voltage V_{TH}, the sub-threshold swing S.S., and the field effect mobility Mu.

Plenty methods are used to determine V_{TH}, which may be the most important parameter in application. In most of the researches on TFT, the constant current method is adopted. In this work the threshold voltage is determined by this method, which extract V_{TH} from the gate voltage at the normalized drain current Id=10 nA for Vd=0.1V.

Sub-threshold swing, S.S (V/dec), is also a typical parameter to describe the control ability of gate toward channel. The sub-threshold swing should be ideally independent of drain voltage and gate voltage. However, in reality, the sub-threshold swing might increase with drain voltage due to short-channel effects. It might as well be affected by the serial resistance and interface traps and therefore become related to the gate voltage. In this work, it is defined as the minimum amount of gate voltage required to increase drain current by one order of magnitude.

The field effect mobility, Mu, is determined from the maximum

transconductance g_m at low drain voltage, which in this work 0.1 V is used. The transfer characteristics of poly-Si TFTs are similar to those of conventional MOSFETs, so the first order the first order I-V relation in the bulk Si MOSFETs can be applied to the poly-Si TFTs, which can be expressed as

$$I_D = \mu_{FE} C_{ox} \frac{W}{L} [(V_G - V_{TH}) V_D - \frac{1}{2} V_D{}^2] \qquad (2\text{-}1)$$

, where

C_{ox} is the gate oxide capacitance per unit area,

W is channel width,

L is channel length,

V_{TH} is the threshold voltage.

If the drain voltage Vd is much smaller compared with ($V_G - V_{TH}$), then the drain current can be approximated as:

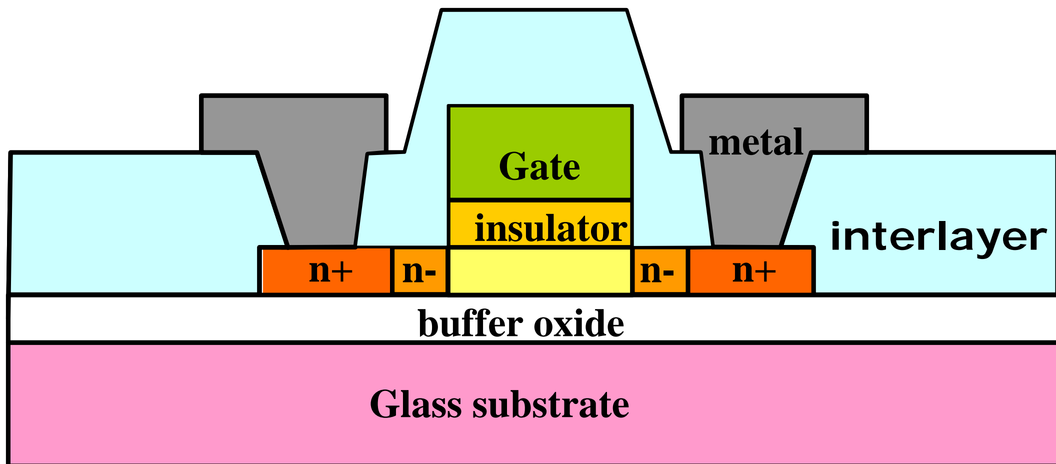
$$I_D = \mu_{FE} C_{ox} \frac{W}{L} (V_G - V_{TH}) V_D .$$

And therefore the electron field effect mobility can be expressed as:

$$\mu_{FE} = \frac{L}{C_{ox} W V_D} g_m$$

Where the transconductance is defined as:

$$g_m = \frac{\partial I_D}{\partial V_G} \bigg|_{V_D = const.} = \frac{W C_{ox} \mu_{FE}}{L} V_D$$



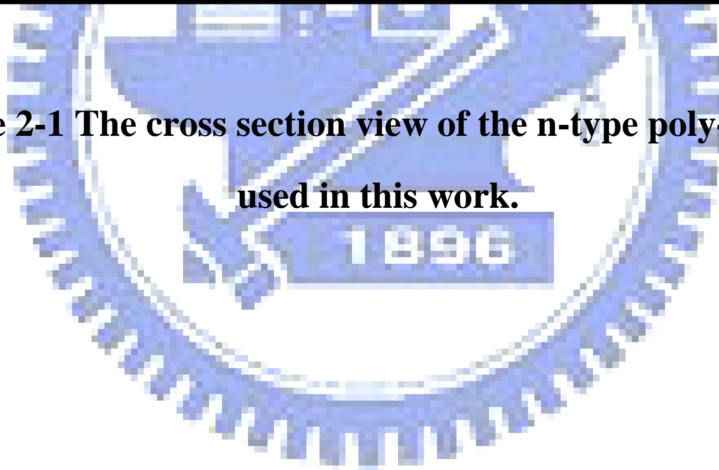


Figure 2-1 The cross section view of the n-type poly-Si TFTs used in this work.

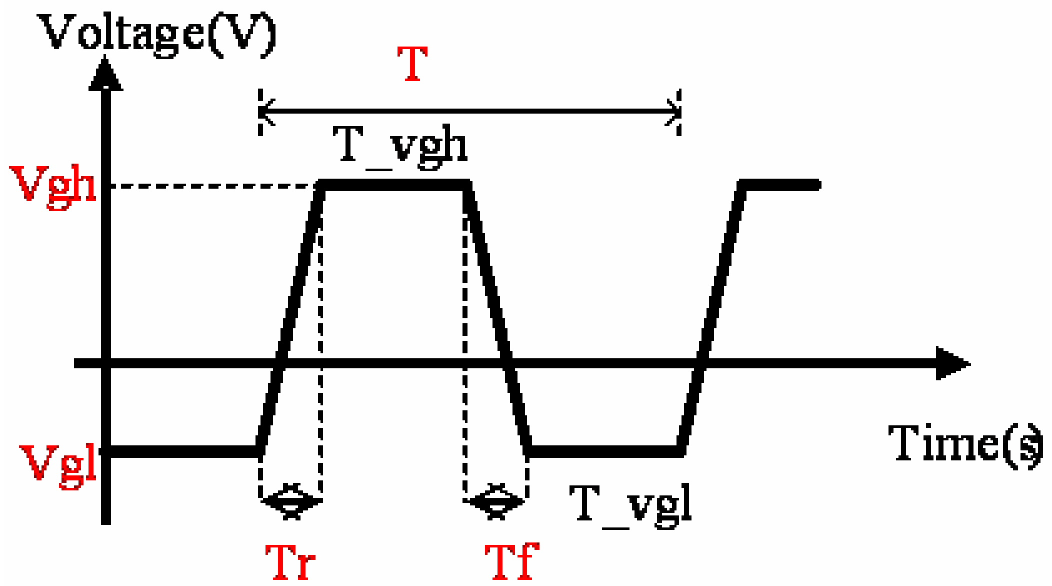


Figure 2-2 The figure illustrating the basic parameters of the AC pulse

Chapter 3

Characterization of Spatial Variation of Poly-Si TFTs

3-1 Review and Motivation

As mentioned in chapter 1, poly-Si TFTs are expected to form the in-pixel switches and the integrated circuits for the display backplane electronics. Some value-added functions are also expected to be formed with the poly-Si TFTs [3-1]. For these circuits, panel designers need to evaluate the performance by the simulator with device model. The device model is expected to precisely describe the device behavior such that the simulation results can fit the real circuit performance as close as possible.

However, poly-Si TFTs are found to suffer from serious device behavior variation, which may not be well described by the model [3-2, 3-3]. So far though there are many papers on the design issues of the influenced circuit performance from the fluctuating poly-Si device behavior, there are very few papers on the variation behavior of poly-Si TFT itself [3-4~3-8]. Because its device structure is similar to MOSFETs (Metal-Oxide-Silicon Field Effect Transistors), it should be a good beginning to first review the variation behavior of MOSFETs and compare it to the case of poly-Si TFTs.

In MOSFETs, the device variation can be characterized as the local variation by short correlation distance and the global variations characterized by long correlation distances, where the correlation distance is defined as the distance in which a process disturbance affects the device performances [3-9]. If this distance is shorter than the usual distance between devices, the disturbance constitutes a local variation and affects few devices (e.g. a charge trapped in the gate oxide layer). For the global

variation, which is characterized by process disturbances with longer correlation distances (e.g. the gate oxide thickness fluctuation across the wafer surface), it affects all the devices within a specific region. Therefore, the devices placed at longer distance are more affected by global variations than devices placed close to each other. For the case of the poly-Si TFTs, since there are grains randomly located in the active region, the variation behavior may be more complicated than that in MOSFETs.

So how serious is this variation behavior of poly-Si TFTs? Refer to previous work, the parameters of the devices on the same spot from different glasses in the mass production line are measured and extracted and the values are given in the table below [3-10]. Table 3-1 gives the summarized values of the average (AVG) and the standard deviation (STD) for the threshold voltage V_{TH} and mobility Mu for the devices located on the spot A to spot H on different glasses as shown in figure 3-1. Refer to the tables, the large standard deviation values of the parameters show that the devices suffer from serious variation problem and there is no apparent trend for such behavior. For example, if the film thickness variation dominates the variation, then the device parameter may show some kind of trend for the device located in the center part than those in the outer part. That is to say, for instance, the STD value would be larger for the devices on the C, D, E, and F spots than those on the A, B, G, H spots. Nevertheless, there is no such trend and the parameters for the eight spots just exhibit certain kind of random fluctuation. In other words, these parameters for the devices from the mass production line just somehow reveal that the variation behavior for the poly-Si TFTs truly exists and may not be neglected.

What does these SPC (Static Process Control) data mean to designers? First, as shown in figure 3-2, the serious variation for the devices means that in addition to the slim design window for the aggressive V.S. conservative design /low-yield V.S. high-yield design, the designers also need to design for the fluctuating device

performance. This would become an extra design issue and the corresponding over-design techniques could be difficult. For some applications, such as in the display panels as the poly-Si TFTs are most commonly applied, in some extreme cases designers even need to modify the circuit because of such serious device variation problem [3-11~3-12].

Another issue is that the true profile of the device variation itself is still not clear. From the SPC data designers could only get a rough idea about the range of the device variation on different glasses but the range and the behavior of the devices located near each other is still unknown. For example, in real applications circuit blocks usually contain devices locate within the range around several hundred micro-meters. In such cases the variation behavior could play an important role in the circuit performance and the aforementioned SPC data may not be applied. As mentioned before, the variation behavior could be different for the devices locate far away or close to each other. Therefore, it would be necessary to examine the variation behavior for the devices locate near each other since it could be more similar to the cases in real applications. Knowing the range and the behavior of the short-range variation would help designers to properly evaluate and estimate the circuit performance.

In light of the structure of this dissertation, there is still one point for the study of the spatial variation. Refer to previous works, the large device performance variation would greatly affect the examination of the device reliability [3-13]. Therefore, before the study of temporal variation, it would be necessary to somehow find the devices with small variation range to facilitate the following reliability study. In this chapter, section 3-2 focuses on the spatial variation and a similar table listing the possible variation sources for poly-Si TFTs is given. To avoid confusion, the local and global variations used in the notation of MOSFET variation are changed to long-range and

micro variation for poly-Si TFTs. A special layout is proposed to study the short-range variation and over 1000 devices in the layout are measured and the device parameters are extracted and summarized. A method inspired from the small signal concept in the electronics is utilized to decouple the long-range and micro-variation. The profiles for the micro variation of V_{TH} and Mu are obtained and two equations are found to describe these profiles. Based on the two equations, the impacts of the device variation on the circuit performance are discussed in section 3-3-1, while the insights of the device variation behavior for different device dimension are discussed in section 3-3-2. The discussion and the summary for this chapter are given in section 3-4.

3-2 Classification and Characterization of Variation

For the case of poly-Si TFTs, the possible variation factors are given in table 3-2, in which the "ploy-Si grain size/number variation and grain boundary" are specially added to the micro variation factors. In order to investigate the relationship between uniformity issue and device distance, a special layout of the devices adopted in this work is shown in Fig 3-3 (a). This layout features the minimum distance that the two devices can locate, which is 40 micron meters when considering the design rules, and the captured picture of the proposed layout is shown in Fig. 3-3 (b). The structure of the poly-Si film and the gate metal are in the order that resembles the crosstie of the railroad and therefore afterward this layout is called the crosstie type layout of poly-Si TFTs. Within this short device distance, the long-range variation may be ignored, and the variation of device behavior can therefore be reduced to almost micro variation alone. In order to obtain the more accurate parameter distributions of crosstie layout TFTs, large amount of device parameters are required. In this work, more than one

thousand devices are measured and the parameters are extracted.

The distributions of threshold voltage (V_{TH}) and mobility (Mu) for both the n-type and p-type TFTs are shown respectively in Fig. 3-4 (a) and (b). The average and the standard deviation values for device parameters of the TFTs are given in table 3-3. It can be seen that both Vth and mobility of the n-type and p-type TFTs do not follow the Gaussian distribution, which contradicts the usual expectation for the device parameter distribution. This reveals that the conventional Gaussian distribution may not be precise in describing device parameters. Besides, the distribution of mobility exhibits severe asymmetric behavior. Since the distributions are not symmetric, it would be difficult to build a model to describe the parameters for circuit simulation. In other words, another grouping method should be adopted.

Figure 3-5 (a) shows the V_{TH} distribution of the devices with respect to device position, while figure 3-5 (b) shows that for mobility distribution. The distribution resembles the small signal concept in electronics. This means that the parameter distribution may be taken as the sum of the large signal and the small signal, as shown in figure 3-6. That is to say, the variation for poly-Si TFTs could be the long-range variation superimposed with a smaller value of micro variation. If the parameter difference is calculated within the two nearest devices, the large signal can then be subtracted and the true profile of the small signal can then be shown. In this case, the long-range variation can be diminished and the micro variation can then be investigated. The distribution of the V_{TH} difference of the two nearest n-type TFTs and p-type TFTs are respectively shown in Fig. 3-7 (a) and (b), while that of the mobility difference for n-type and p-type devices are shown in Fig. 3-8 (a) and (b). The minimum distance of the devices is 40 um as shown in figure 3-3 (a). It can be seen that both the distributions of V_{TH} and mobility difference for the devices show symmetric behavior and are quite centered than Gaussian distribution. This reveals

that micro variation may have a much concentric effect for the devices than Gaussian distribution.

Since the distributions of the parameter difference are symmetric, it would be necessary to find a model for circuit simulation. For the distribution of the difference of V_{TH}, Gaussian-Lorentzian cross product is applied to the fitting, which is

$$y = \frac{a}{\left(1+d\left(\frac{x-b}{c}\right)^2\right)*\exp\left((1-d)*\frac{1}{2}\left(\frac{x-b}{c}\right)^2\right)}$$

where

a is the peak value of the distribution

b is the center of the distribution

c is fitting parameter related to the width of the distribution

d is fitting parameter varying from 0 to 1; 0 represent the pure Gaussain function and 1 means a pure Lorentzian distribution

As for the distribution of the difference of Mu, the Lorentzian distribution is applied to the fitting, which is

$$y=\frac{a}{1+\left(\frac{x-b}{c}\right)^2}$$

where

a is the peak value of the distribution

b is the center of the distribution

c is fitting parameter related to the width of the distribution

In statistics, the coefficient of determination (R square) is a common index for evaluating the similarity between the proposed model and the real data. Generally, if the value of R square is above 0.7, it means that the specific model shows good agreement with the data [3-14]. In this work, the values of R square of the above

fittng curves, as shown in the figures, can both approach 0.9, representing the good validity between the proposed model and the real data. However, there could be still other equations that could provide higher fitness for describing the micro variation and the corresponding effects on circuit performance. Since the R square reaches above 0.9 for the two proposed models in describing the distribution, it could still be fair enough to use these models to evaluate the effect of device variation on both the circuits and also the study of the variation behavior for the devices with different dimension.

3-3 Impacts and Insights of Device Variation

In this section, based on the two proposed models to describe the device parameter variation, the impacts of device variation are discussed. The differential pairs and the ring oscillator, as the benchmarks of the digital and analog circuit, are adopted to study the influnces of device variation in section 3-3-1. On the other hand, by using the models the variation behavior for the device with different device width is also studied. With the help of the interdigitated layout, the variation behaviors for the poly-Si TFTs as well as the a-Si TFTs and single-crystal MOSFETs are examined and compared.

3-3-1 Impacts of Device Variation on Circuit Performance

(a) For the analog circuits: In the integrated circuit application, coupling effect is a serious problem for signal transmission. Output signal suffering from serious coupling effect may lead to errors of the retrieved signal and affect the corresponding design window. In order to reinforce the immunity to the noise and the coupling effect during the transmission, the differential signals are widely used for analog circuit design. For the display applications, the differential pairs are commonly used in many

blocks of display electronics, such as the input stage of operational amplifier. Figure 3-9 shows the basic differential pair structure, where R_D is the resistive load and Rss represents the output impedance of current bias; differential signals are applied to the gate terminal of transistor M1 and M2.

The quality of data transmission will benefit by the use of differential signal. However, device variation would be a serious problem for differential pair. Since these devices are nominally identical, the variation of the device characteristics will result in errors in retrieving the signal and affect the accuracy of the differential signal. In conventional MOSFET circuits, the variation between M1 and M2 is very low and can be suppressed under the well-controlled process. As compared to CMOS technology, poly-Si TFTs suffer form worse device variation and the effect of output signal variation may hence be more complicated. In order to evaluate the circuit performance of differential pair by poly-Si TFTs, the aforementioned variation models would be adopted to simulate the circuit performance with device variation.

The common mode rejection ratio (CMRR) is a common index for the capability of differential pair against the common mode noise, which can be written as

$$CMRR = \left| \frac{A_{dm}}{A_{cm\text{-}dm}} \right| \cong \frac{\mu(V_{GS}\text{-}V_{th}) + 2\mu^2 C_{ox} \frac{W}{L} (V_{GS}\text{-}V_{th})^2 Rss}{\mu \Delta V_{th} + \Delta\mu (V_{GS}\text{-}V_{th})}$$

In the equation above, the ΔV_{th} and $\Delta\mu$ terms represent the differences of threshold voltage and mobility of the two transistors. In this work, the CMRR value is used as the index to examine the accuracy of each simulation skill and model.

Before the simulation, it is essential to transform the parameter distribution into the corresponding value for Monte Carlo simulation. In this work, a method of range mapping is used. Take the distribution consisting of four variables as example, as

shown in figure 3-10 (a). Based on the probability, a table of range mapping can be established, as shown in figure 3-10 (b). For a series of uniformly random values in the range from 0 to 1 generated by the computer, the corresponding series can be obtained by looking up table in figure 3-10 (b). If 0.3 is randomly picked from computer, the variable B will be chosen according to Fig. 3-10 (a). Thus, the distribution from the look-up values will match that shown in figure 3-10 (a). In light of statistics thoery, a certain number of data for each distribution can be generated to get the stable and reliable simulation result. In this work, 210,000 times of data transformation for each distribution are executed to obtain the best and stable result for the Monte Carlo simulation.

In simulation, the V_{GS} is set to 5V, which is the voltage at the quiescent point. The output impedance of current bias is 3 MΩ, which is extracted from the output resistance at the corresponding bias point. To compare the effects of the device variation on circuit performance with different models, two distribution models are adopted in the Monte Carlo simulation to calculate the CMRR value under the constant device distance of 200 μm. One is the extracted distribution and the other is the widely-adopted Gaussian distribution. The parameters of Gaussian distribution used here are 1.69V, 0.03V, 59.66 cm^2/Vs and 7.84 cm^2/Vs, which respectively correspond to the mean value and the deviation of the threshold voltage and mobility from the measured database as shown in table 3-3.

The simulation of the cumulative distribution of the CMRR value in dB is shown in Fig. 3-11. The results of Monte Carlo method with Gussian distribution and the real extracted distribution are represnted by lines with circles, squares and triangles individually. The line with circle symbols is plotted by Monte Carlo method with Gussian distribution. As for the line with squares and triangles, they are done by Monte Carlo method with the extracted distribution. For the line with squares, the

threshold voltage and mobility and their difference are substituted with real parameter and proposed model. For the line with triangles, the difference term are from the parameters randomly generated from the proposed model while other device parameters are replaced with the average value from the measured database. It can be observed that the lines with squares and triangles are almost overlapped, and this reveals that the difference terms dominate the simulation result of CMRR value. Therefore, the simulation procedure can be simplified as only change the the difference terms instead. Among the lines with circles and triangles, it is found that the curves of the cumulative probability exhibit a difference of 10 dB in average and cross at about 55 dB. It is attributted to the sharper distribution of the difference of V_{th} and Mu in reality than the Gaussian distribution.

If all the real measured data are used in calculation (the line with inverted triangles) under the constant device distance 200 μm, it can be observed that lines with squares, triangles and inverted triangles are almost the same. The simulation result shows that the Monte Carlo method with the extracted distribution is more accurate than that with Gaussian model. Generally speaking, the specification of the CMRR value in commerical IC is usually desired to reach above 60dB. Obviously, design with the conventional Gaussian simulation method will lead to errors in estimating the circuit performace of differential pair as compared with the real measured data. However, it should still be noticed that if it is required to reach a confidence level of 98 % , the CMRR specification of the circuit should be set below 50 dB based on the extracted distribution, instead of 53 dB corresponding to Gaussian model. As for the average performance, simulation using Gaussian distribution might lead to differences in prediction. Since the proposed model is the distribution originated from real data, it should provide a more credible description of the device performance for a large amount of devices. From the viewpoints of real application,

this simulation results suggest that designers should consider the device parameter profile in addition to the average and standard deviation values in simulating the effect of variation. Considering the mean and standard deviation value only could lead to over- and under-estimation of circuit performances.

(b) For the digital circuits: In this part, the effects of device variation on the digital circuits are investigated. Though digital circuits may not require high definition of the signals as the analog circuits do, the effect of device variation may still lead to the errors of the output signals. In this work, ring oscillator is set as our benchmark of investigation because of its sensitivity to the simulation model. Because there are more than one hundred devices in the circuits, the long-range variation may take place and form the trend in the device parameter distribution. Since so far there is no adequate description to depict the effect of long-range variation on the device parameters, the method used in discussing the output variation of differential pairs may not be suitable here. In other words, another comparing method should be adopted to investigate the effect of micro variation in ring oscillators.

The ring oscillator circuit may not be categorized as the digital circuit, yet it is still widely used in digital circuits to provide required timing information. The figure of the implemented circuit and the test device is shown in figure 3-12. 105 stage ring oscillator is fabricated and a test device is placed just by the ring oscillators. Since the effect of variation could not be compared device to device in the circuit, the upper and lower bounds of variation range are used instead. The test device locates very close to the circuit that it can be inferred the long-range variation can be taken as negligible and only micro variation exists. The simulation will be done by three conditions sim_typ, sim_ff and sim_ss. The sim_typ is that all the devices are simulated with the measured test device parameter directly. This depicts the condition that the measured device parameter is the same as all the devices inside the ring oscillator circuit. For

the case that the micro variation exists between the test device and the devices in the circuits, two conditions are taken into consideration, as shown in Fig. 3-13. Sim_ff is simulated with the possibly high mobility and low threshold voltages of both N-TFT and P-TFT at 99.5% and 0.5% of the variation model respectively. This simulation condition describes the conditions that the test device parameters are just the worse performance than those in the circuit. In other words, the devices in the ring oscillator are faster than the test device with the magnitude of 0.5% slow in mobility and 99.5% high in Vth in the population according to the proposed micro variation model based on measured data. On the other hand, sim_ss is with the possibly low mobility and high threshold voltages at 0.5% and 99.5% of the variation model respectively. This represents the conditions that the test device just has the better performance than those in the circuit. The parameters used in simulation are shown in table 3-4. Fig 3-14 (a) and (b) show the simulation results with micro variation for the 105 stage ring oscillator as the operating voltage is 5V and 10V, respectively. In this work, 22 sets of ring oscillators and their corresponding test devices next to each other are fabricated and the measured. In these figures, the data are sorted by the measured frequency. It can be seen that for both operating voltages, the simulation data from the sim_ff and sim_ss form the gap of the operating frequency. It can be seen that the measured data all fall in this gap. This represents that proposed model can fairly describe the range of the micro variation for the devices in the ring oscillator. Besides, there is no large difference between the measured data and the simulation data with the parameters from the test device. This may reveal that though the micro variation exists between the devices in the ring oscillator, the effect of the micro variation on the overall performance will be averaged and therefore the micro variation may be ignored in the simulation of ring oscillator. However, it should also be noted that the range of the measured operating frequency is so large comparing to the gap of the lowest driving

frequency of the simulation data S.S. and F.F. This means that though the micro variation may be ignored in the ring oscillator simulation, the long-range variation may instead influence the performance and the effect can be very critical. This finding would be important in the characterization and simulation of the digital circuit simulation.

3-3-2 Insights of Device Variation

Typically, the dimension of the transistors in analog circuits is larger than that in digital circuits. On the other hand, signal in the analog circuits may require higher precision than that in the digital circuits since the latter may only need to distinguish the high or low signal of the applied voltage. In certain analog circuit, a very high matching behavior between devices is desired. In addition to the simplest structure, the interdigitated layout, several layout techniques with the more complicated structure are proposed to reach the high matching behavior between the devices, such as common centroid layout technique, and the dummy device technique [3-15~3-16]. In the following section, therefore, only the variation behavior of poly-Si TFTs in the interdigitated layout method is discussed. Figure 3-15 shows the idea of interdigitated layout. The idea is that the devices are placed in a cross-over form and the finger number represents how many devices are electrically-connected to each other. For example, two-finger interdigitated layout means that the number N_{TH} and $(N+2)_{TH}$ devices are electrically connected, and the same for the $(N+1)_{TH}$ and $(N+3)_{TH}$ devices.

The V_{TH} variation behaviors between the interdigitated devices with different fingers for n-type devices are shown in figure 3-16, while those behaviors of the p-type devices are shown in figure 3-17. On the other hand, the mobility variation behaviors of the n-type and p-type devices for different fingers of interdigit are respectively shown in figure 3-18 and figure 3-19. The values of the standard

deviation for these distributions with different interdigit finger numbers are given in table 3-5. It can be observed that, for both V_{TH} and mobility and for both n-type and p-type devices, the distribution is becoming more centralized and the profile becomes narrower as the finger number increases, which reveals that the variation of these parameters decreases with interdigit finger number. Besides, the center of these distributions move closer to zero as the finger number increases. Gaussian distribution is used to fit the profile of the parameter variation in the interdigitated layout and the coefficient of determination, as shown for each parameter in the figures 3-16 to 3-19, increases with finger number. The meaning of the coefficient of determination is given in section 3-2. This reveals that though the true profile of micro variation is not clarified yet, the parameter variation of the poly-Si TFTs is essentially approaching Gaussian distribution in the interdigitated layout method as the finger number increases.

Figure 3-20 (a) shows the standard deviation value of V_{TH} with different interdigit finger numbers, while figure 3-20 (b) shows that of mobility. It can be observed that both n-type and p-type curves follow the same trend and the difference between the n-type and p-type devices keeps a constant gap. Besides, it is discovered that the micro variation of V_{TH} of p-type device is larger than that of n-type devices in the interdigitated arrangement, which can be attributed to the BF_3 channel implant for V_{TH} adjustment. These implanted boron atoms could form the shallow state near the valence band in the poly-Si bandgap and may then turn out to be a variation factor for the p-type devices [3-17]. Besides, it is also found that the mobility variation of n-type device is larger than that of p-type, which can be attributed to the activation and uniformity of the LDD region for the n-type devices.

The interdigitated layout is essentially extending the device width and therefore the well-known “law of area” may be used to model the variation behavior. The "law

of area" states that the device parameter mismatch is inversely proportional to the root of the channel area [3-18]. This indicates that the larger the device dimension is, the less variation these devices would suffer. This also means that the variation behavior would be worse in the small dimension devices than that in the large dimension devices. Owing to the randomly-distributed grains in the poly-Si film, the parameter variation of poly-Si TFTs could show a different behavior than MOSFETs. Figure 3-21 (a) shows the V_{TH} variation for different finger numbers and the fitting curve, while figure 3-21 (b) shows that of mobility variation. The "law of area" equation used in this work is given as:

$y = a + \frac{b}{\sqrt{x}}$, where a and b are the fitting parameters.

The fitting parameters "a" and "b" for V_{TH} and mobility and also for n-type and p-type devices are given in table 3-6. Referred to table 3-6, the fitting parameter "a" and "b" respectively represent how the variation would be as the device width is very large and how the variation would worsen as the device width shrinks. For V_{TH}, it is discovered that parameter a is very small for both n-type and p-type devices, meaning that the variation of the large width device would show similar V_{TH} variation behavior for n-type and p-type devices. The parameter "a" is negative for the n-type device, and what does the negative variation mean? Of course there is no "negative variation" and the device dimension could never be infinitely large. This just represnets that the variation could be suppressed to a very low value and also the "law of area" may not be adequate enough to describe the overall trend and may just provide some limited insights. For the fitting parameter "b" for p-type device is slightly larger than that for n-type device, meaning that the aforementioned channel doping effect could gradually become dominant as the device width decreases. On the other hand, for mobility, it is found that the parameter "a" for n-type device is much larger than that for p-type

device. This reveals that, as the device width increases, the grain number and electrical behavior variation in the channel region may be gradually averaged and thus the LDD variation may be the main factor responsible for the larger mobility variation, making the mobility variation in n-type devices larger than that in p-type devices. However, as the device width becomes smaller, the number of grains in the channel could greatly differ from each other and thus the value of mobility variation for both n-type and p-type devices would slowly become similar and the effect of LDD variation may be less important. To summarize, the micro variation behavior for the poly-Si TFTs can really be suppressed to a relatively small value for the device with very large dimension. For designers, this finding of device variation behavior with respect to different device width could be of great help in realizing and modeling of device variation and can also assist designers to properly evaluate the device parameter variation for poly-Si TFTs with different dimensions.

For further studying the variation behavior, it would be of practical interest to study the variation behavior of the silicon-based devices with different crystallinity behavior. Figure 3-22 shows the standard deviation for V_{TH} for different type of devices. More than 400 crosstie devices of amorphous silicon TFTs are measured and statistically summarized. The amorphous silicon TFT is of the conventional inverted stagger structure. The data of the single crystal silicon is referenced from Chee Lin Yum in Bachelor's thesis on Electrical Engineering [3-19]. The fitting parameters and the corresponding coefficients of determination (r^2) are given in table 3-7.

Referred to table 3-7, it is shown that the coefficients of determination are all above 0.7, indicating that the law of area can be used for describing the variation for the devices with different grain structures. For fitting parameter "a," it is discovered that the parameter for single crystal silicon MOSFETs is very small, meaning that the variation would almost be eliminated for the very large width devices. In addition, the

parameter "a" for amorphous silicon TFT is around four times larger than that of poly-Si TFTs. This reveals that the micro variation behavior of amorphous TFT may be worse than that in poly-Si TFTs, which may result from the micro structure and film thickness fluctuation of the amorphous silicon film.

For the fitting parameter "b," it is found that the variation of n-type poly-Si TFTs is ten times larger than n-type single crystal silicon MOSFETs. Furthermore, the parameter "b" of amorphous silicon TFTs is three times larger than that of n-type poly-Si TFTs. For p-type devices, the parameter "b" of poly-Si TFTs is one hundred times larger than that of single crystal silicon MOSFETs. Since parameter "b" can be taken as the increase rate for device variation as the device width shrinks, it can be inferred that the variation of amorphous silicon TFT would be worse than that of poly-Si TFTs and the single crystal MOSFETs would exhibit slow increase of device variation as the device width decreases. This can be attributed to the micro structure and grain behavior of the silicon layer for the devices. The preparation of the single crystal silicon film takes long time in the high temperature environment (around 1000 degree Celsius). Silicon atoms may get enough energy and time to form the good bonding and crystallinity, therefore the structure of the silicon film would be of good quality and uniformity. However, the film preparation for poly-Si film in this work is by using the excimer laser to recrystallize the deposited amorphous film and therefore the film structure may not be as good as that of the single crystal silicon film in MOSFETs. On the other hand, the preparation for amorphous film is just by PECVD deposition and there may be very small grains in the silicon film. Besides, in this work the amorphous silicon TFT is of the conventional bottom gate structure is adopted and film thickness variation of the amorphous silicon film may also result in device variation.

Owing to the higher device mobility, poly-Si TFTs are expected to replace bond

ICs and form the circuits for some specific applications. From the viewpoint of circuit design, higher driving current of the poly-Si devices is desired. From the simple current equation, it means that the ratio of device width over length (W/L) should be higher to obtain the higher driving current without changing the process method. For poly-Si TFTs, it is reported that reducing the device length to around 2 um will introduce serious short channel effect and that could result in the inaccuracy between the circuit design and the real device performance [3-20]. Another way to increase driving current is to enlarge the device width. An additional point for increasing the device width is that the larger channel width means that there are more grains in the channel region and the device variation behavior may be relieved. Therefore, in order to have higher driving current and lower variation issue, one option is to increase the width of poly-Si TFTs. From the discussions above, it is shown that the variation can be gradually reduced and for the very large device dimension the micro variation can truly be suppressed. Though the variation can not be fully eliminated, for some applications, such as the pixel design in AMLCD (Active Matrix Liquid Crystal Display), such variation behavior for large-width device might still pass the 8 mV criteria in the grey level voltage definition of the 8-bit panel specification. However, for some circuits requiring high signal precision, such variation in device performance should be taken into consideration. Furthermore, for the pixel design in AMOLED (Active Matrix Organic Light Emitting Diode) driven with poly-Si TFTs, since there may not be sufficient space for the very large device, panel designers should design for such variation and the compensation methods may still be necessary for the high performance panels. The impact of this work is to provide the behavior of device variation for different device width and furthermore to find the order of variation when the device width is very large. This would be helpful for circuit and panel designers in evaluating the variation behavior of poly-Si TFTs and designing for

variation if necessary.

3-4 Summaries

Poly-Si TFTs have the similar structure to the MOSFETs, and so do the application field when it comes to the integrated circuits. As in the field of MOSFETs, when the technology node reaches sub-micron, the variation issue gradually becomes a big problem. The variation, possibly comes from the line edge roughness (LER), dopant fluctuation and discrete film thickness distribution, could gradually become one of the main design issues, namely DFM (Design for Manufecturing). As for poly-Si TFTs, though the device dimension is not as small as the MOSFETs, the variation issue is still an issue to consider. Though it is generally believed that the device variation mainly comes from the grain distribution, there are rare studies about how the designers should tackle the device variation in designing the poly-Si TFT circuits. This chapter focuses on the variation behavior of poly-Si TFTs, as well as the impacts on the circuit design. The projected device variation behavior for the devices with different channel width and the insights of the intrinsic variation behavior are also studied. Though the main field of poly-Si TFT application still focuses on the display electronics, which may not require the high uniformity standard as the MOSFETs do, these studies should still help designers to properly evaluate and estimate the variation behavior both for device and circuit performance. With the high demand of the value-added functions in the display system, poly-Si TFTs in the circuits could face the tougher uniformity requirement and the understandings presented in this chapter should be of great help.

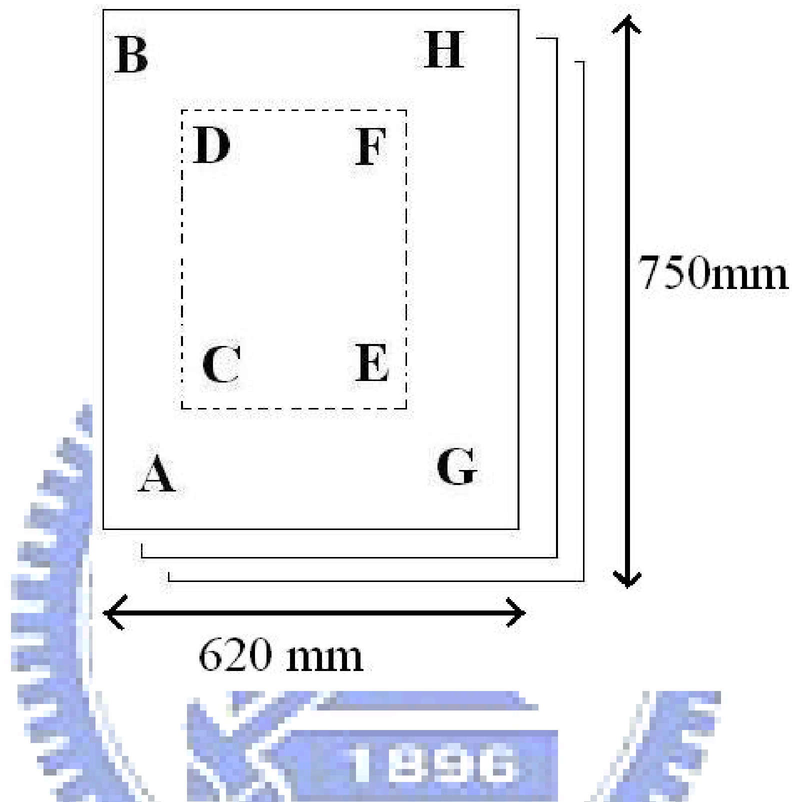


Figure 3-1 The devices locate on the eight spots on different glasses in the mass production line are measured and extracted for studying the variation

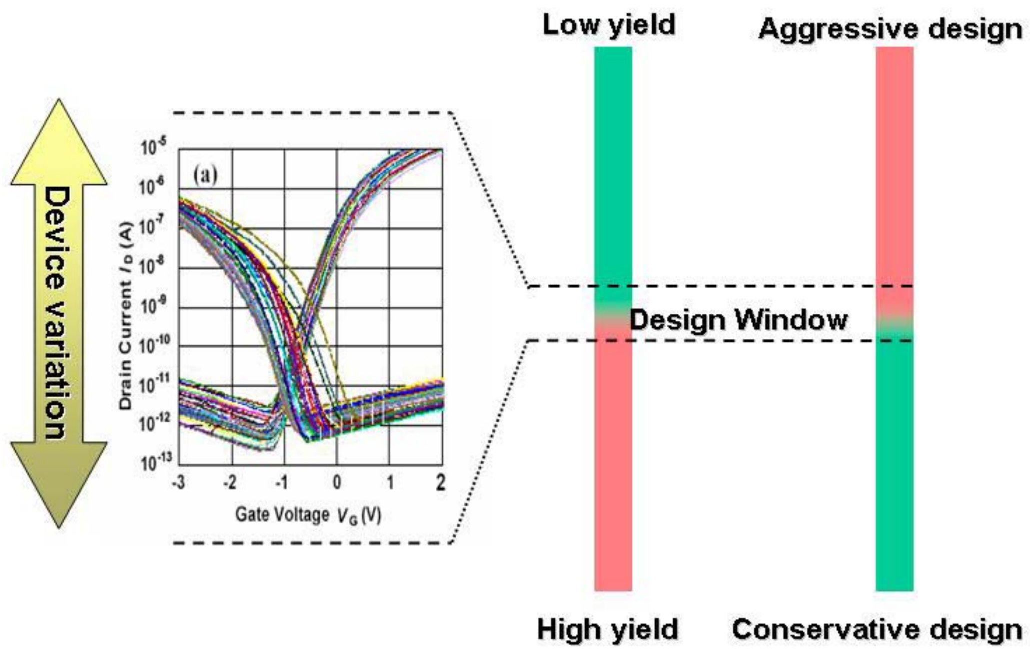


Figure 3-2 The figure illustrating the design issues as well as the device variation issue

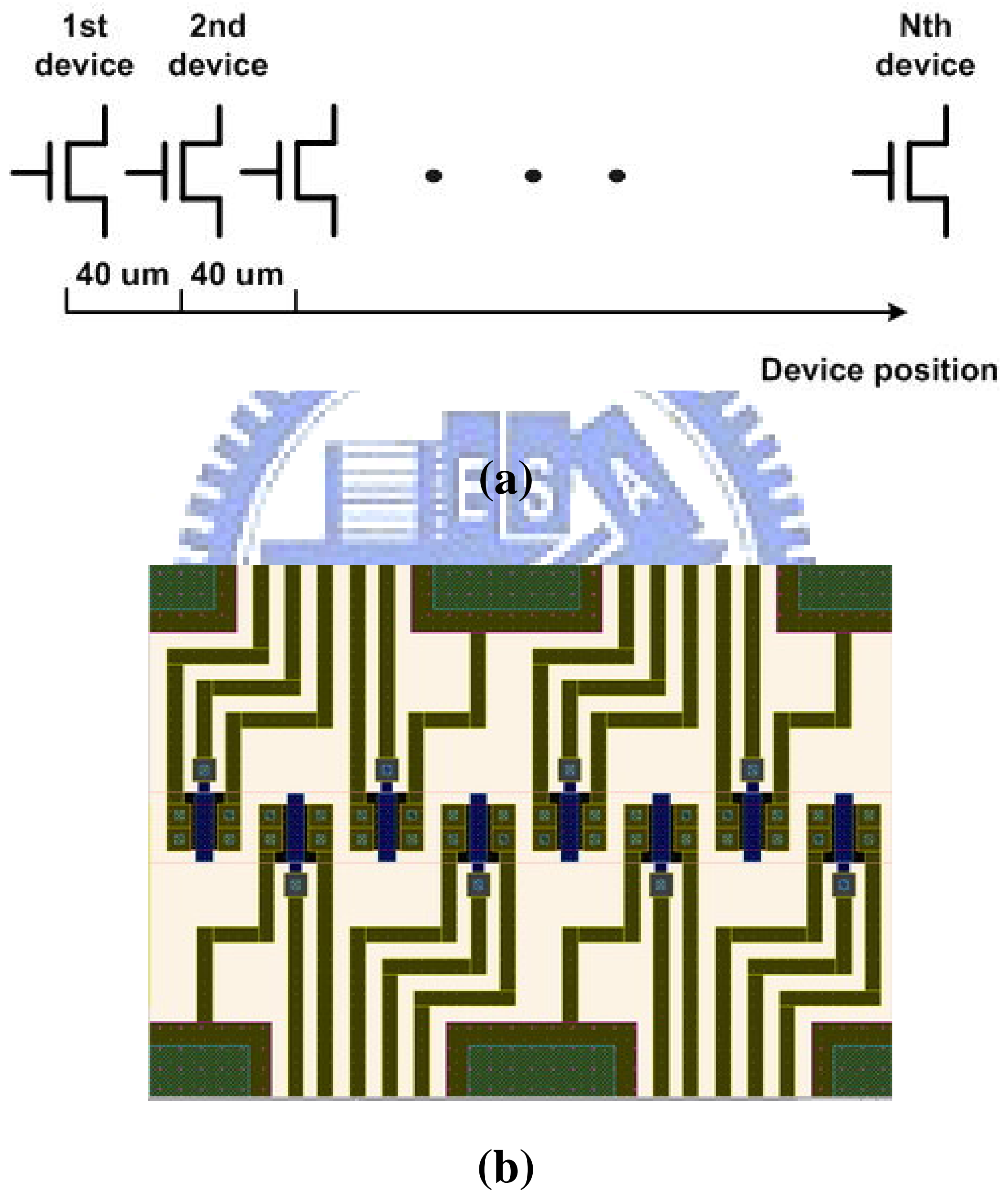
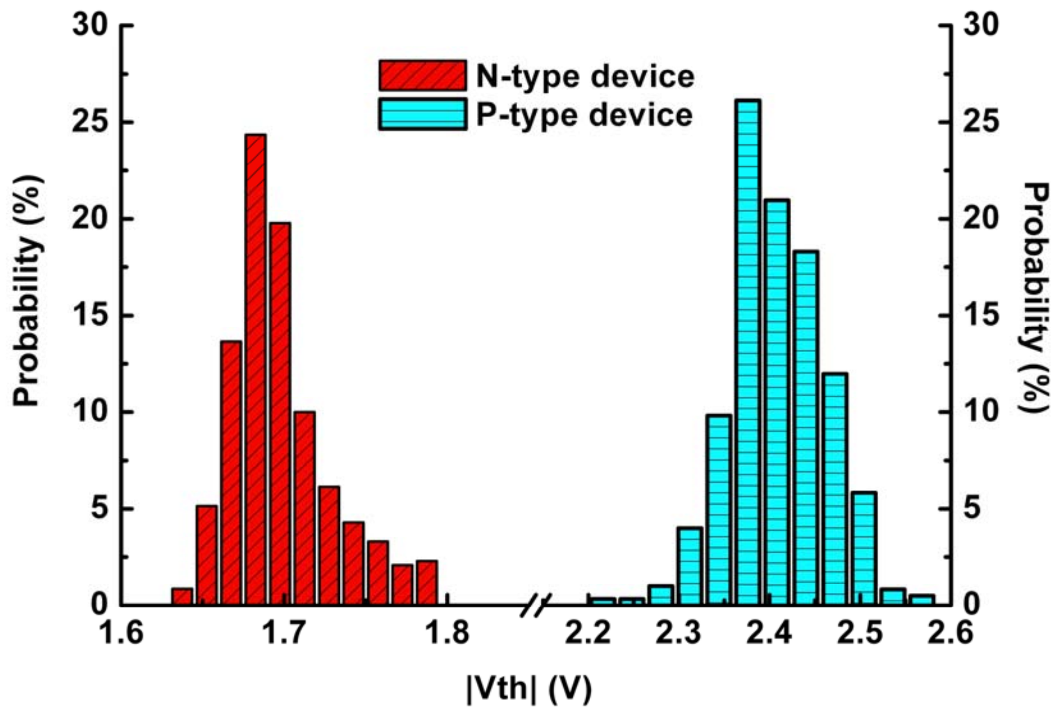
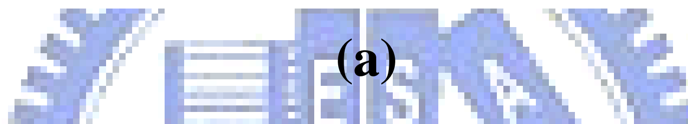
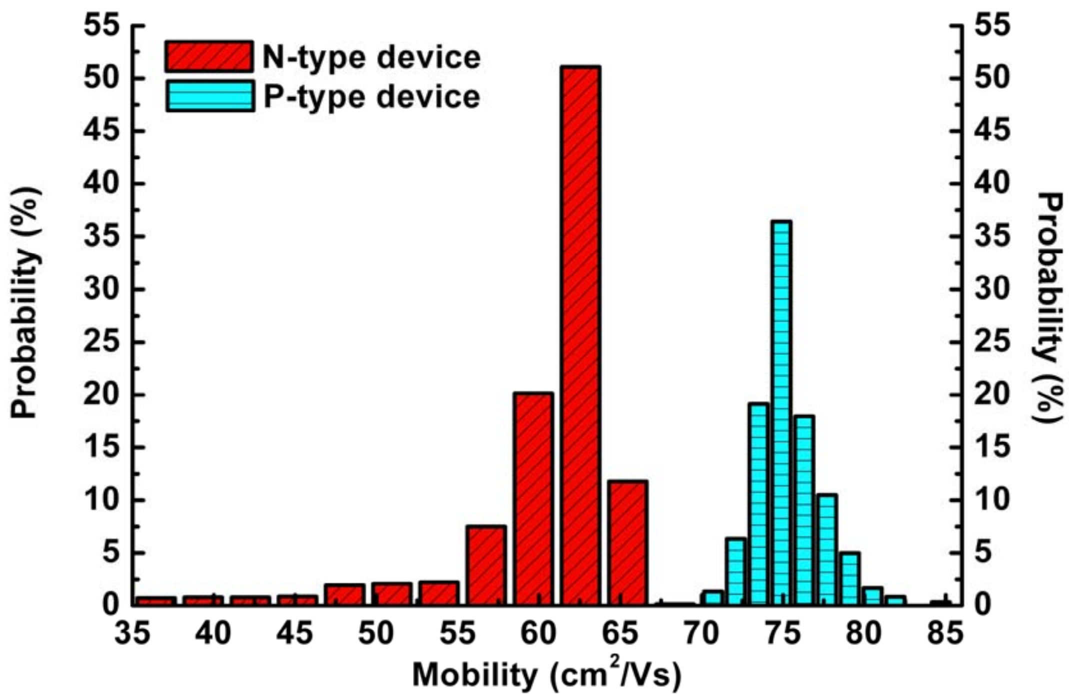


Figure 3-3 (a) The figure illustrating the proposed crosstie layout. (b) The captured picture of the proposed layout



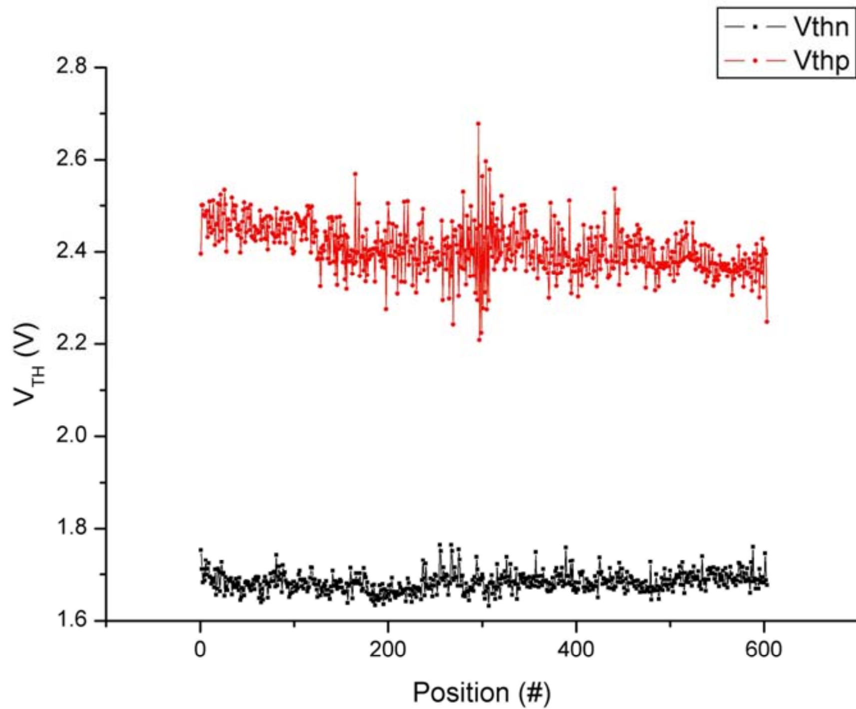


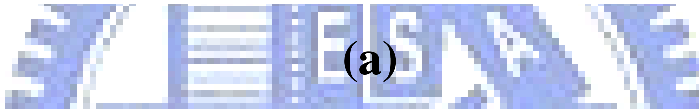
(a)



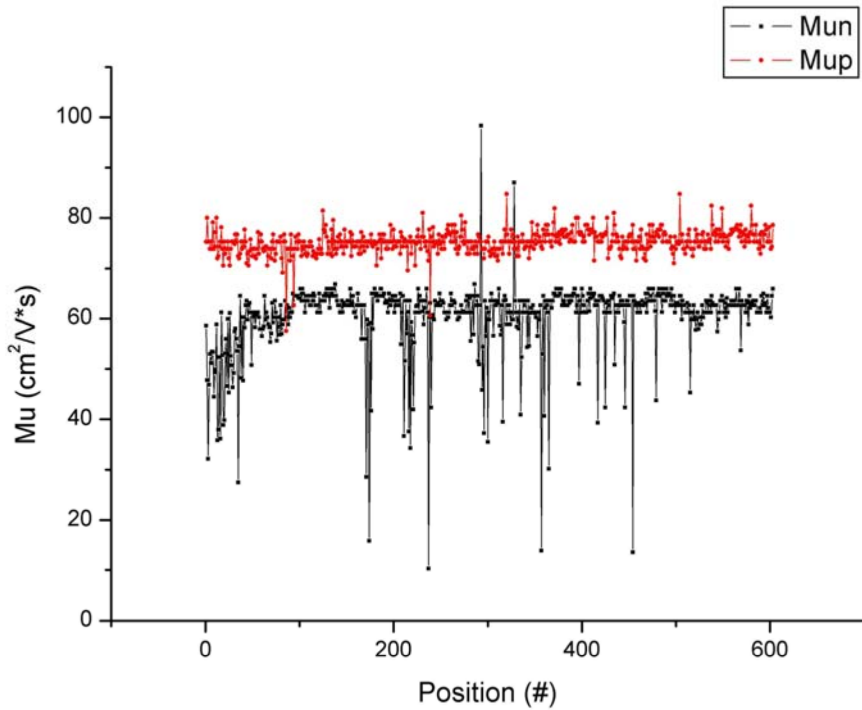
(b)

Figure 3-4 (a) The V_{TH} and (b) the mobility distribution of the measured crosstie devices for both n-type and p-type devices



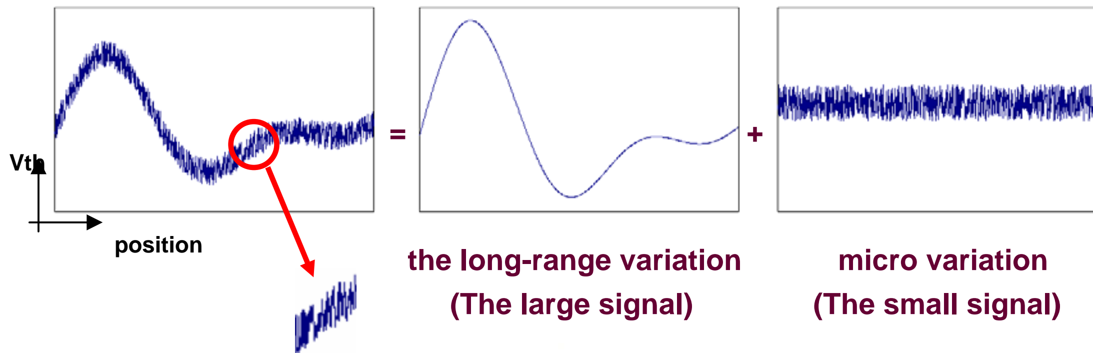


(a)



(b)

Figure 3-5 The distribution of the device parameters with distance for (a) V_{TH} and (b) mobility



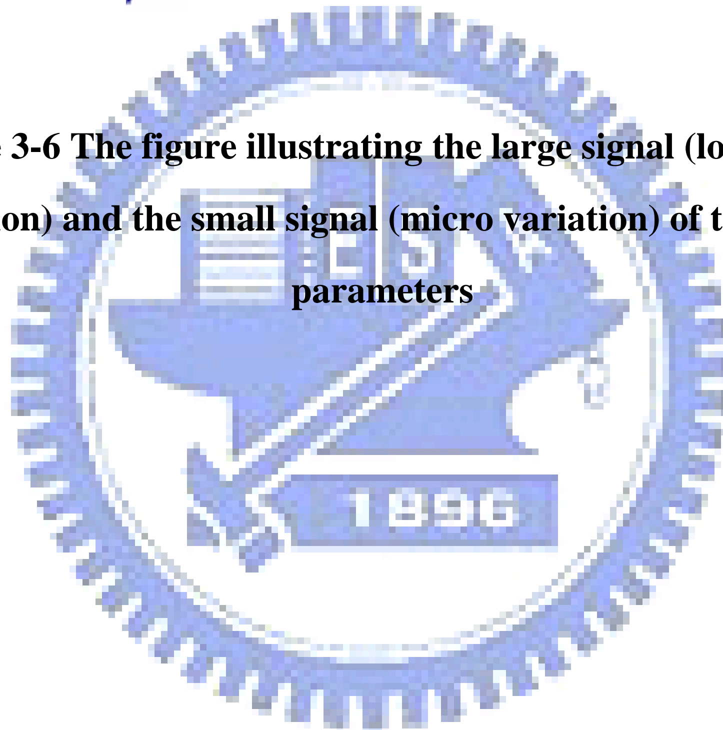
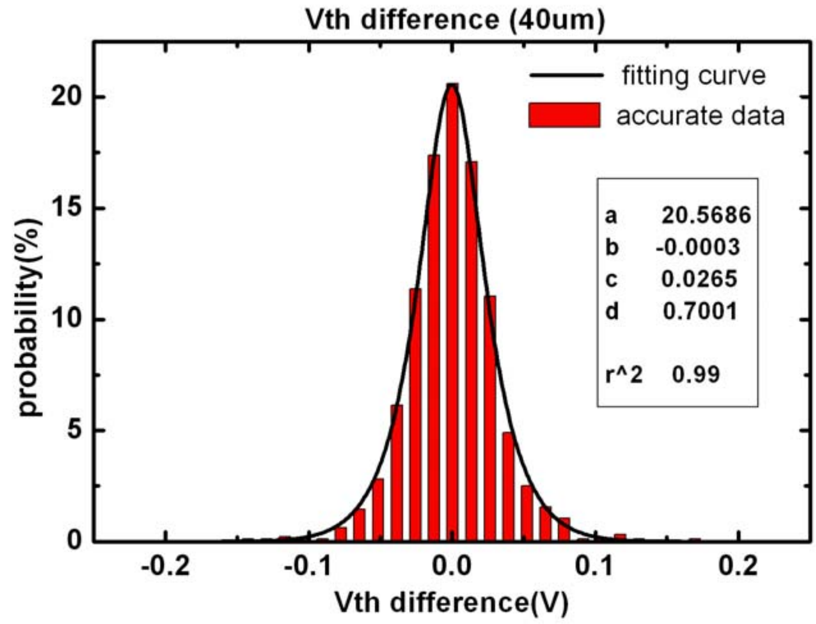
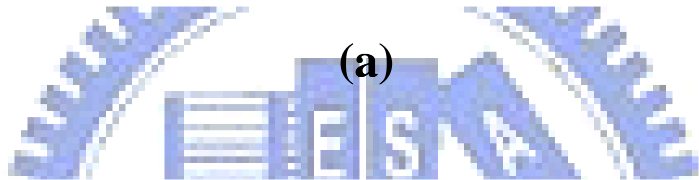
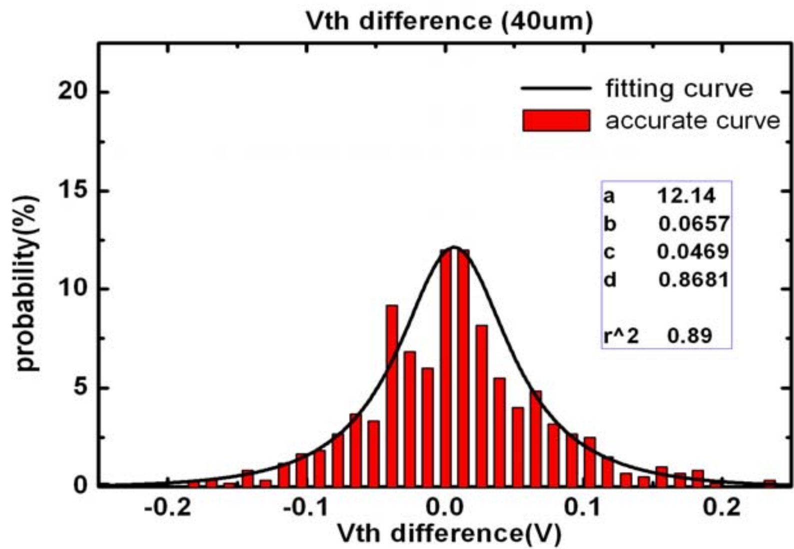


Figure 3-6 The figure illustrating the large signal (long-range variation) and the small signal (micro variation) of the device parameters



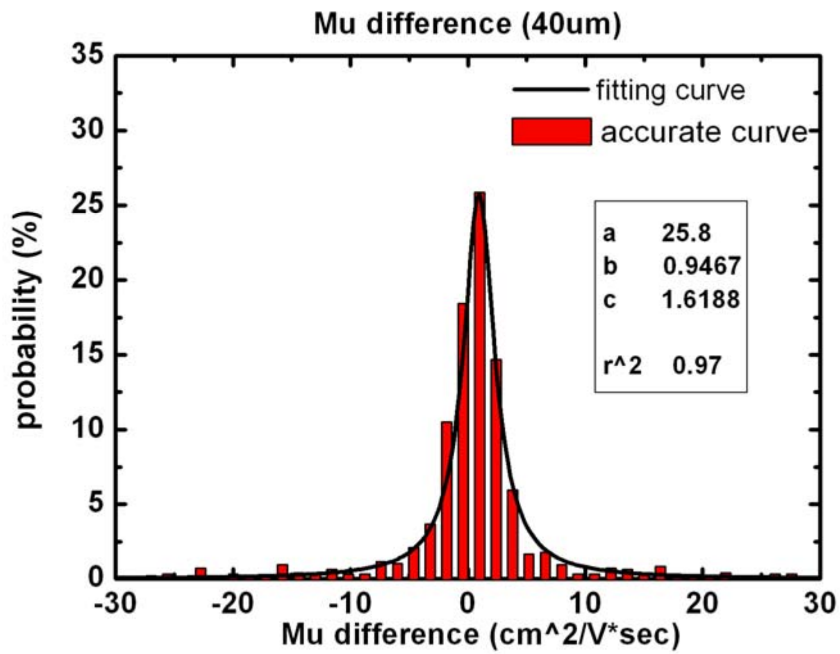
(a)

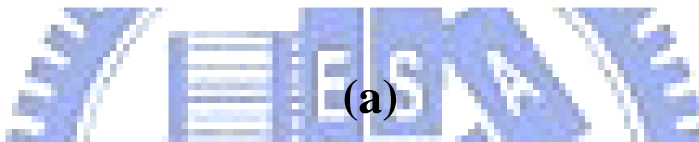




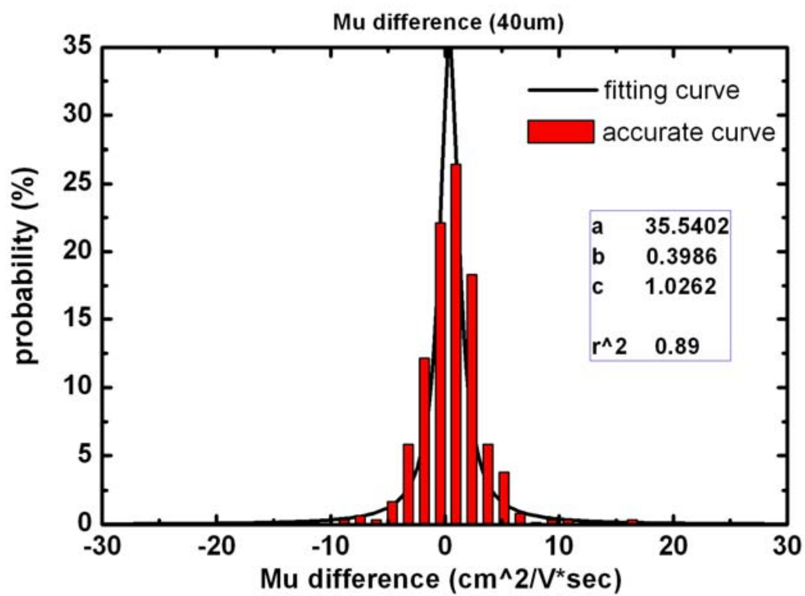
(b)

Figure 3-7 The data and the equation describing the V_{TH} variation for the (a) n-type and (b) p-type devices





(a)



(b)

Figure 3-8 The data and the equation describing the mobility variation for the (a) n-type and (b) p-type devices

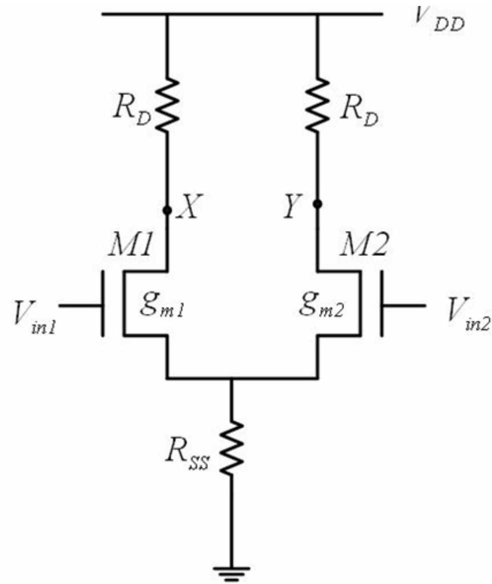
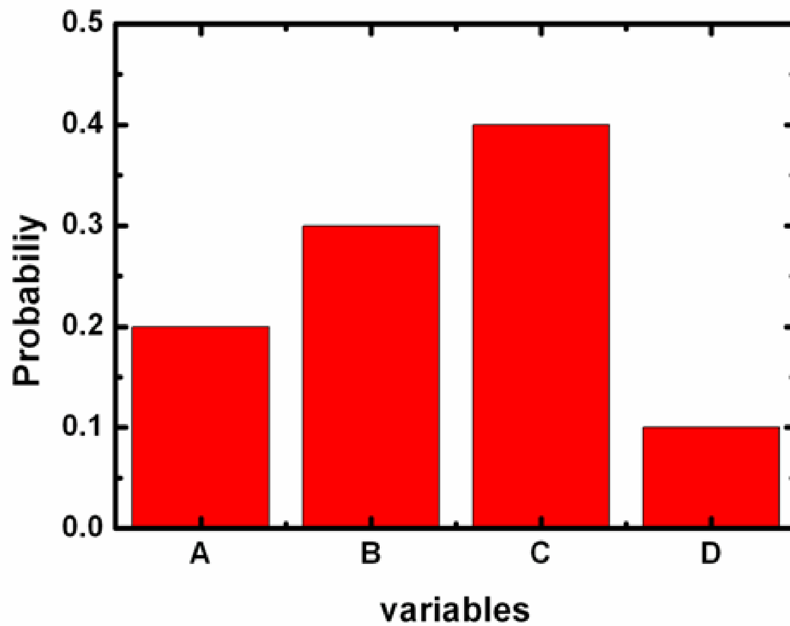
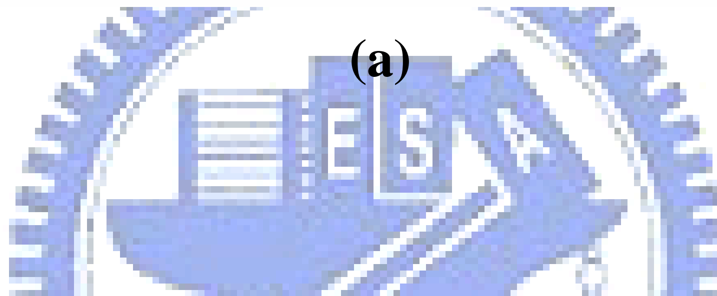


Figure 3-9 The conventional structure of the differential pair circuit



(a)



Random value	Corresponding variable
0 ~ 0.2	A
0.2 ~ 0.5	B
0.5 ~ 0.9	C
0.9 ~ 1.0	D

(b)

Figure 3-10 (a) The simple distribution for the variable mapping. (b) A look up table for the variable mapping base.

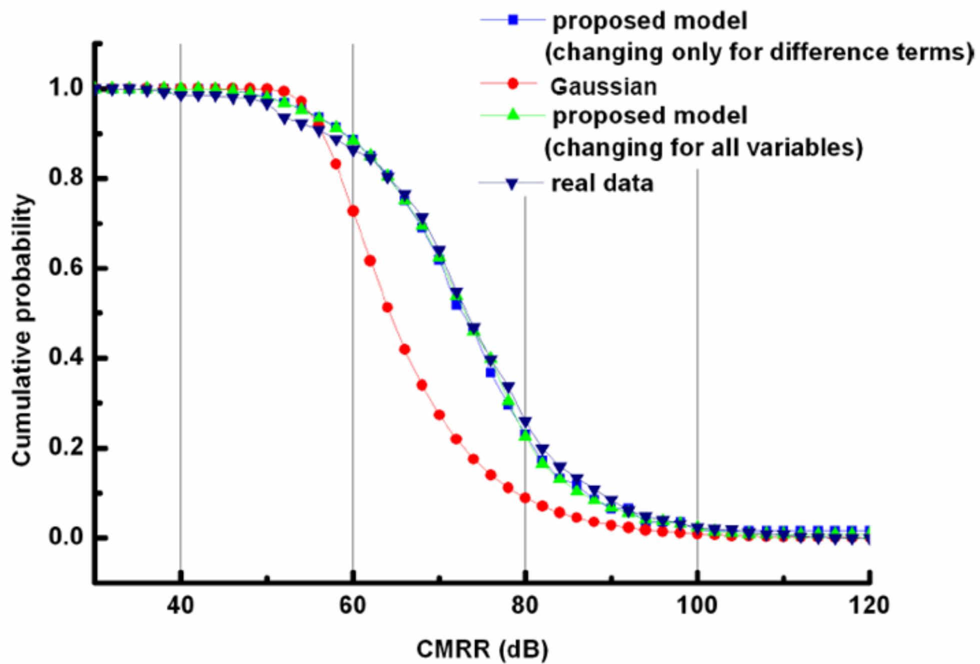


Figure 3-11 The cumulative distribution for the CMRR value of differential pair with different device parameter model

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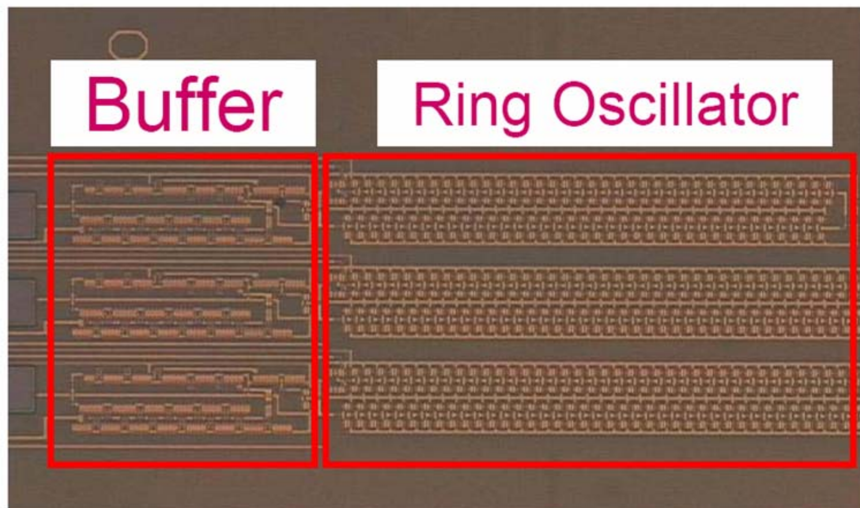


Figure 3-12 The photograph of the fabricated ring oscillator circuits

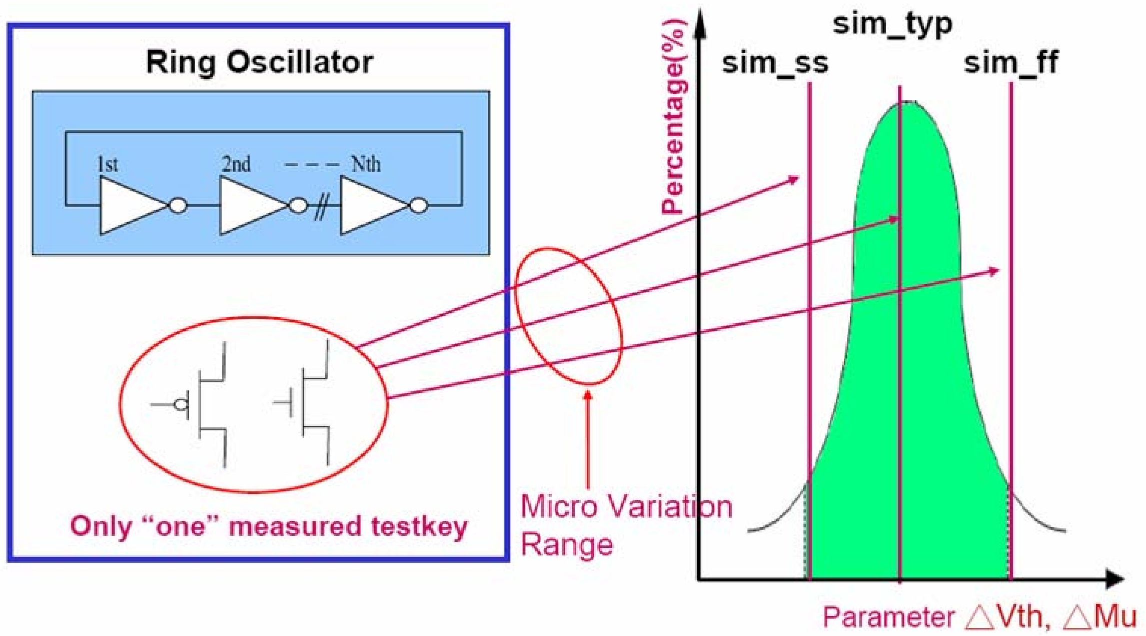
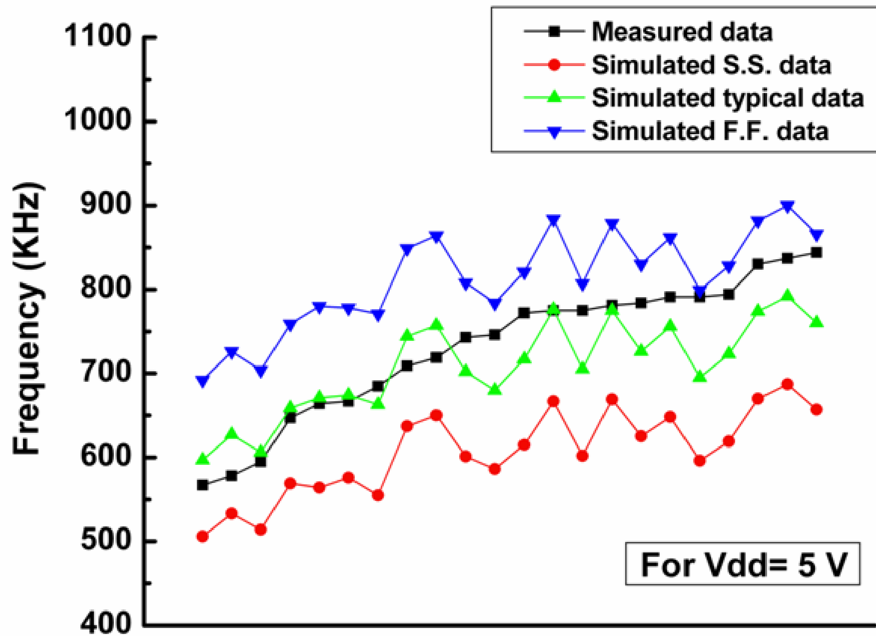
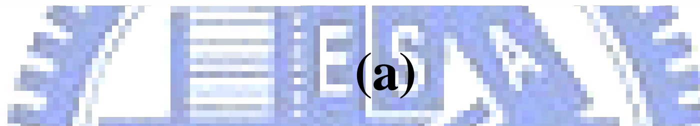
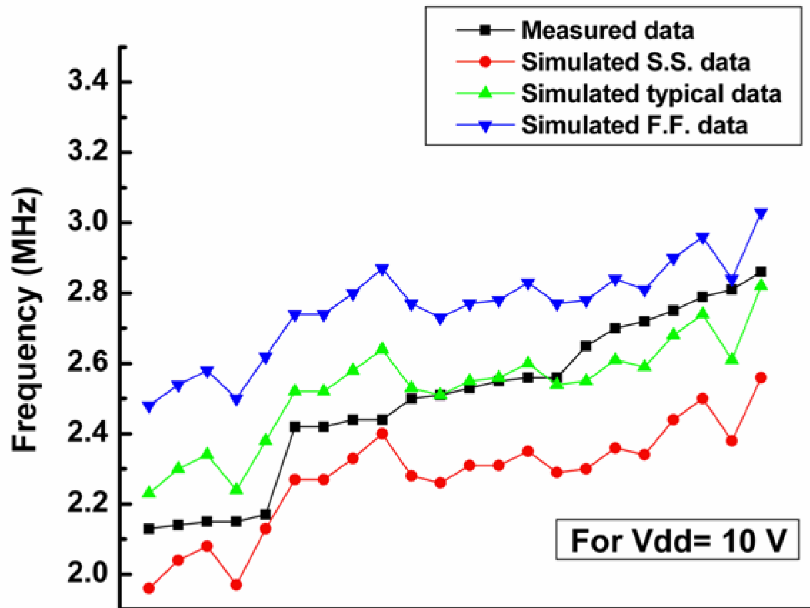


Figure 3-13 The figure illustrating the upper and lower bound of the device variation model





(a)



(b)

Figure 3-14 The simulated and measured ring oscillator operating frequency with (a) operating voltage 5 V and (b) 10 V

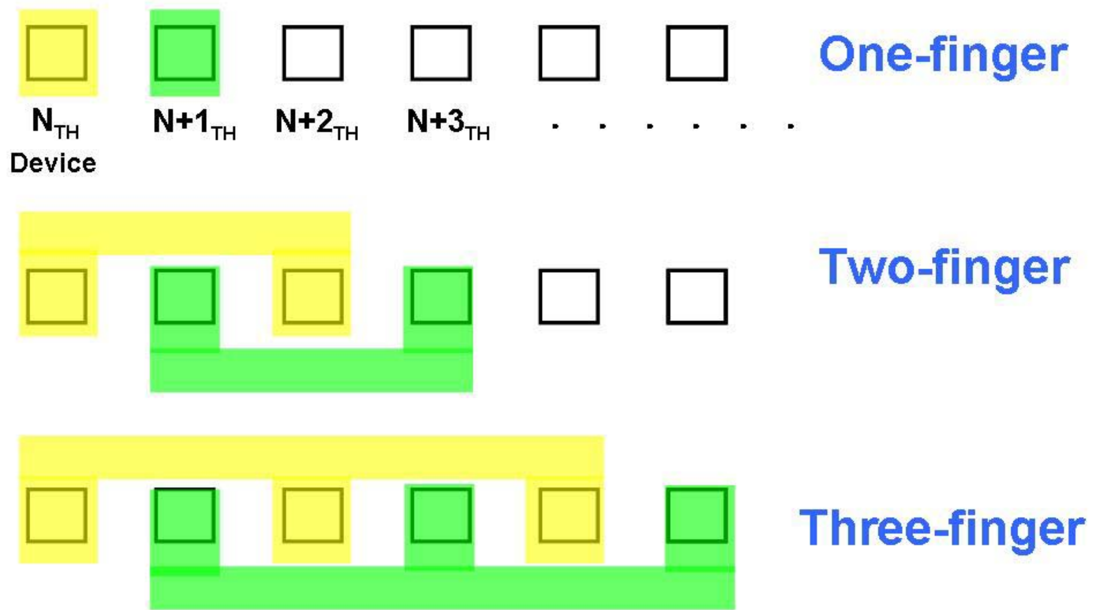


Figure 3-15 The interdigitated connection with different finger numbers

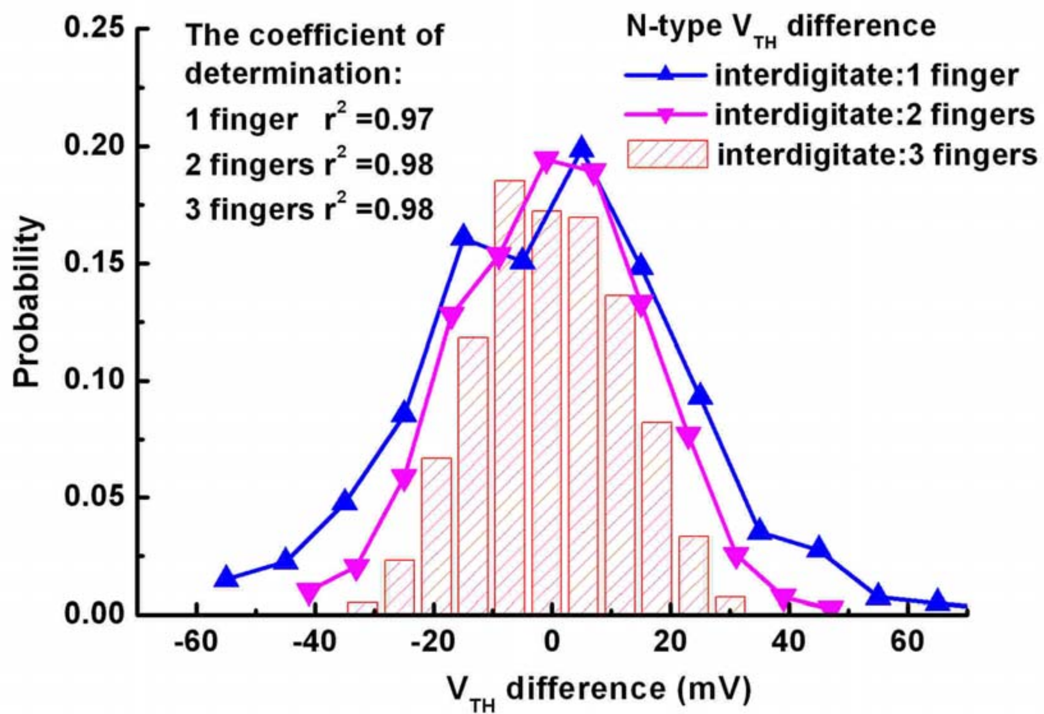


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Figure 3-16 The V_{TH} difference distribution of n-type devices in the interdigitated layout with different finger numbers

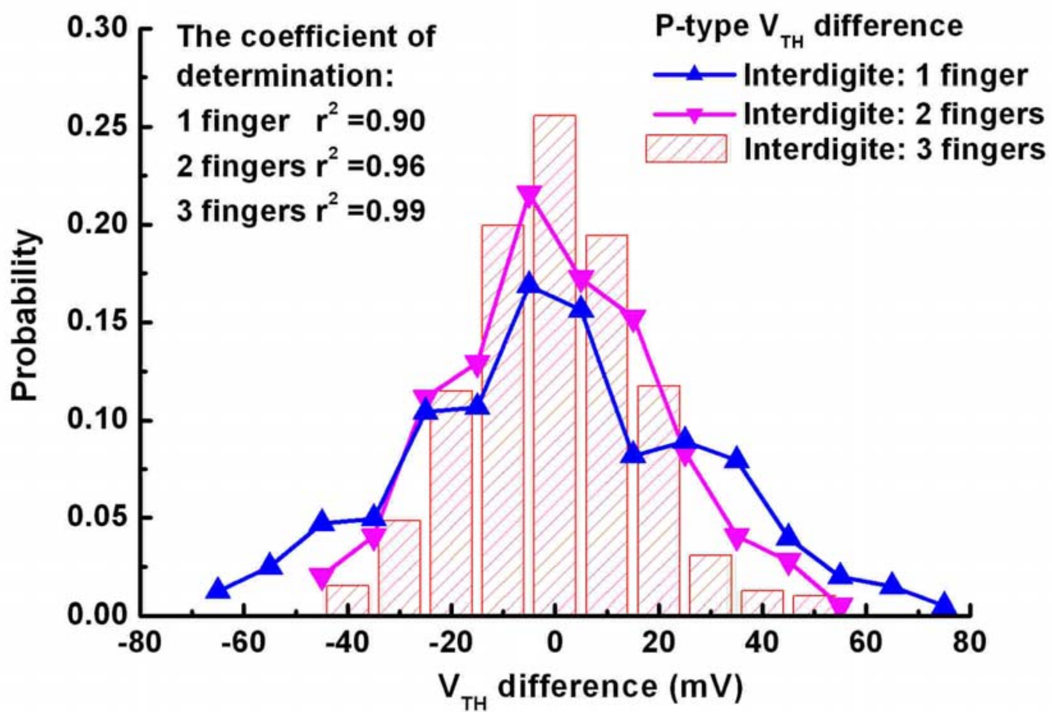

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Figure 3-17 The V_{TH} difference distribution of p-type devices in the interdigitated layout with different finger numbers

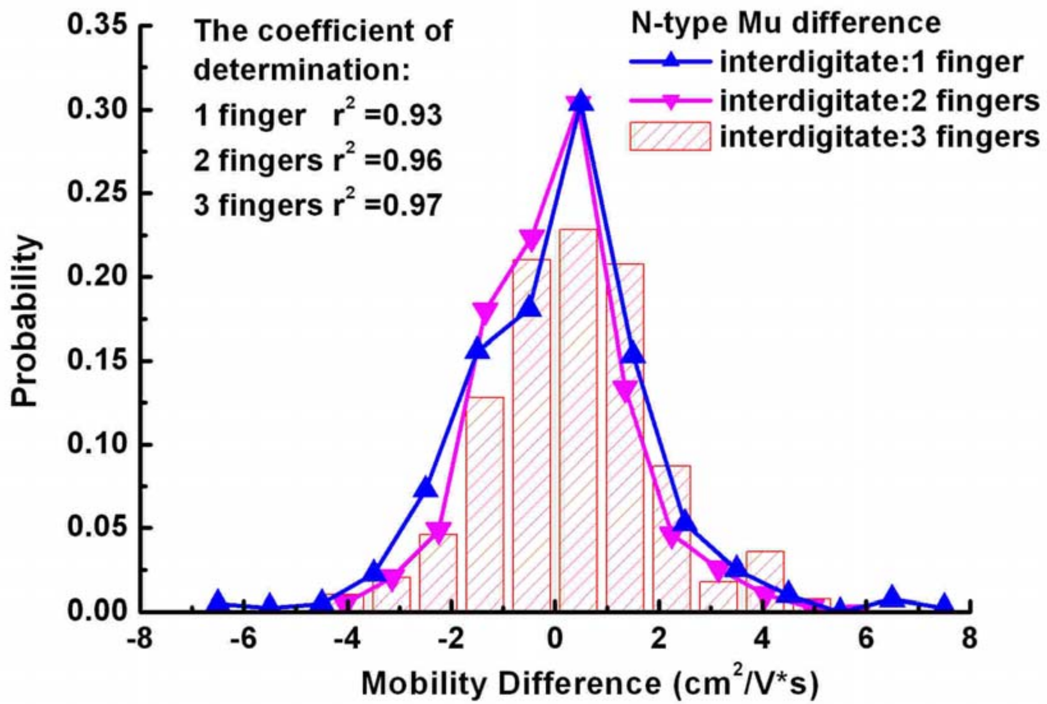

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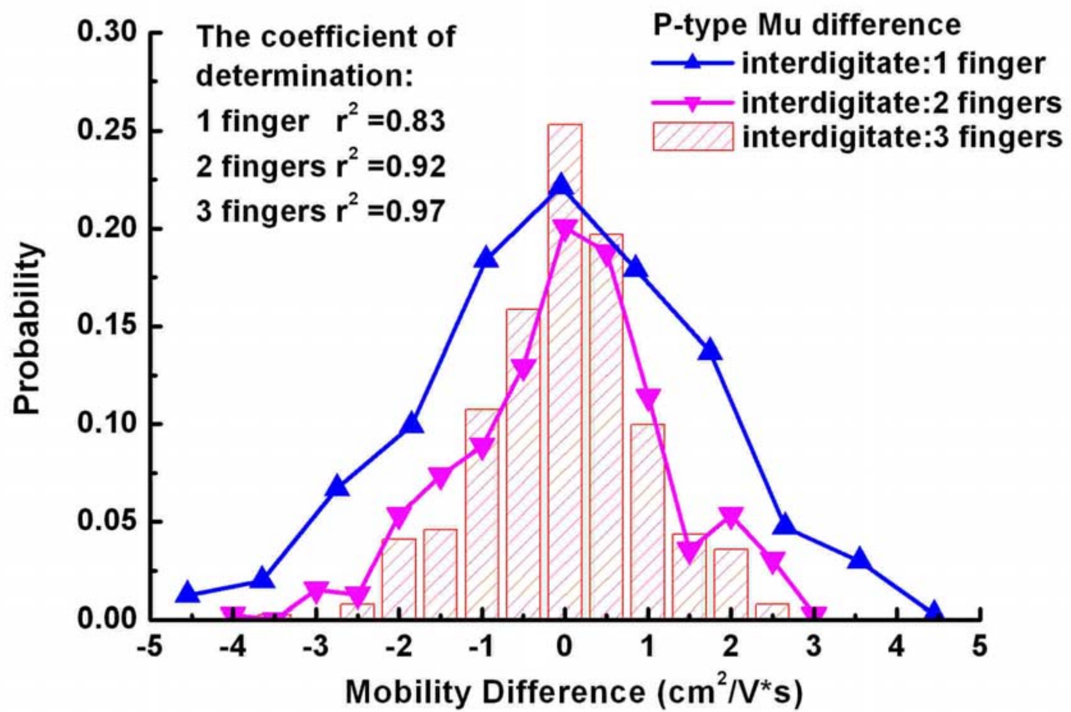
Figure 3-18 The mobility difference distribution of n-type devices in the interdigitated layout with different finger numbers



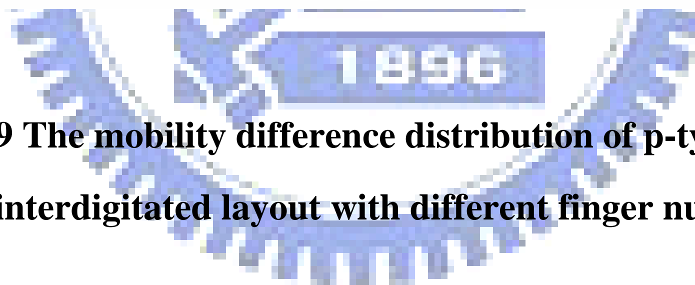


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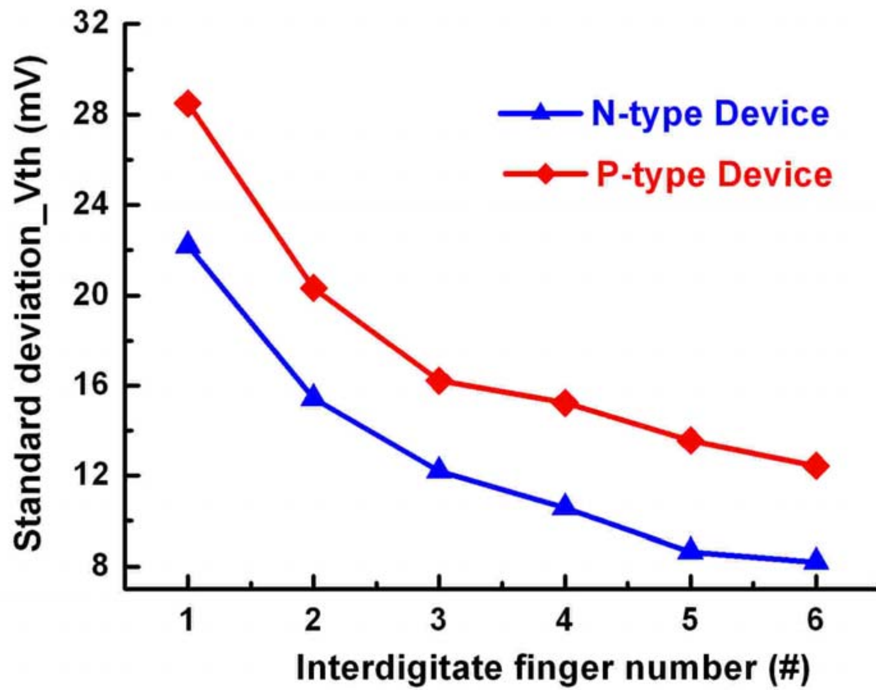
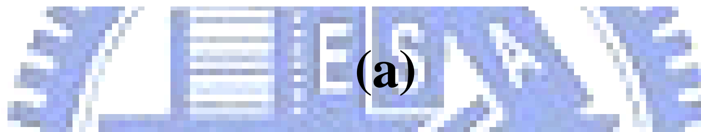
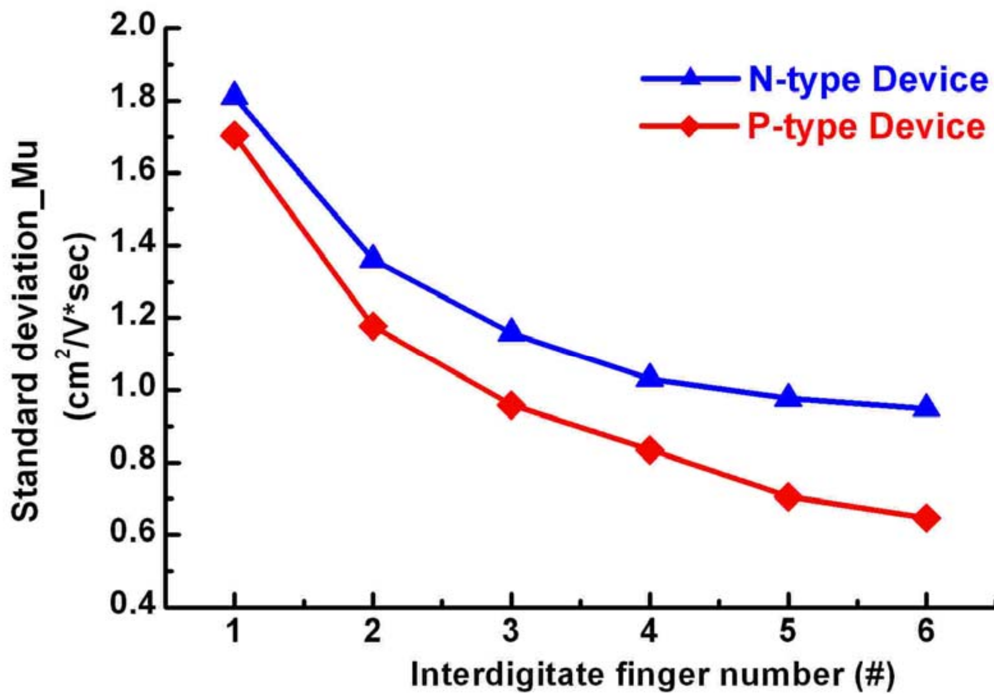
Figure 3-19 The mobility difference distribution of p-type devices in the interdigitated layout with different finger numbers



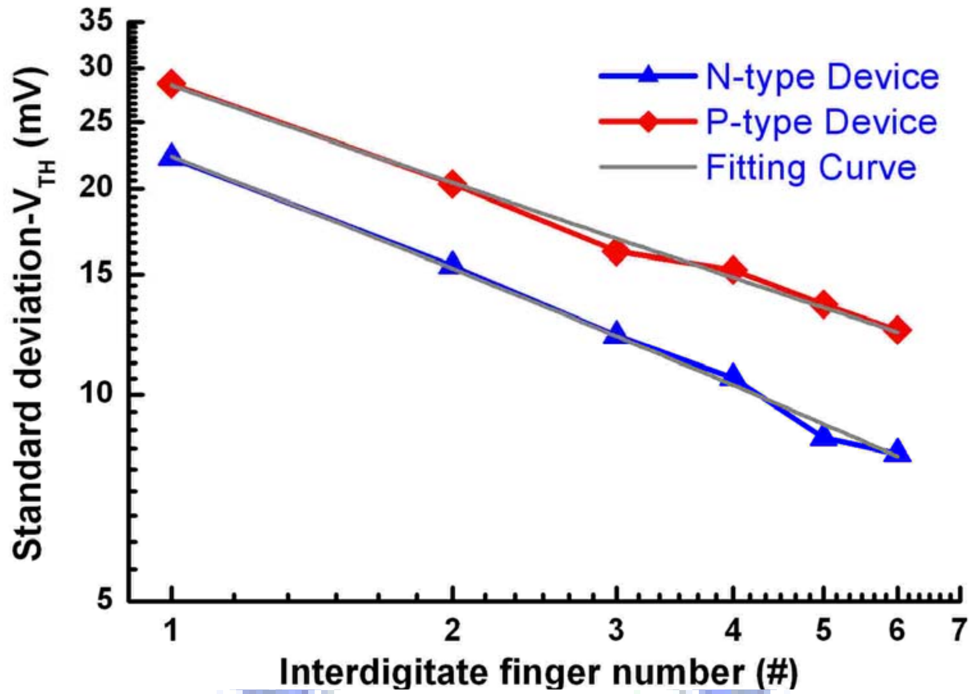


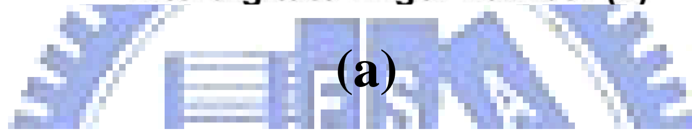
(a)



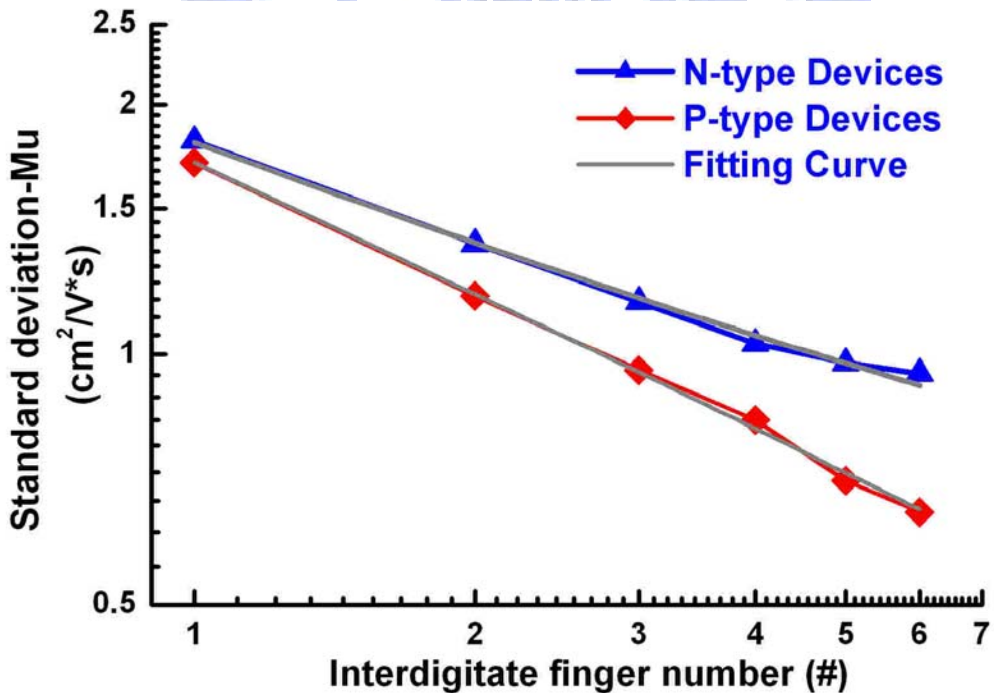
(b)

Figure 3-20 The standard deviation of the device parameter with different interdigit finger number for (a) V_{TH} and (b) mobility





(a)



(b)

Figure 3-21 The log-scale standard deviation of the device parameter with interdigit finger number and the fitting curve for (a) V_{TH} and (b) mobility

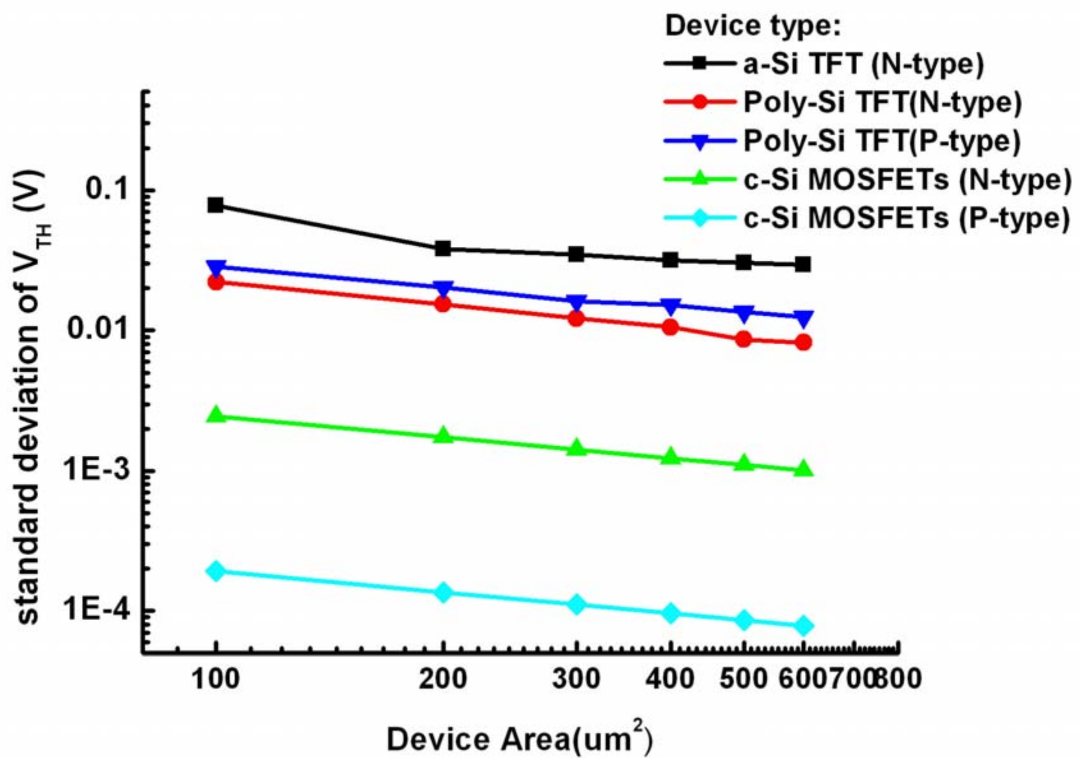


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Figure 3-22 The standard deviation of V_{TH} for different types of devices and for both n-type and p-type devices

V_{TH}	AVG	STD
Site A	1.273	0.5168
Site B	1.226	0.3486
Site C	0.961	0.3638
Site D	1.299	0.5226
Site E	1.148	0.4976
Site F	1.281	0.4633
Site G	1.084	0.3472
Site H	1.038	0.334

Mobility	AVG	STD
Site A	69.37	11.264
Site B	78.4	12.303
Site C	72.89	11.723
Site D	76.43	12.576
Site E	72.58	11.672
Site F	75.05	12.243
Site G	69.81	10.64
Site H	76.87	11.084

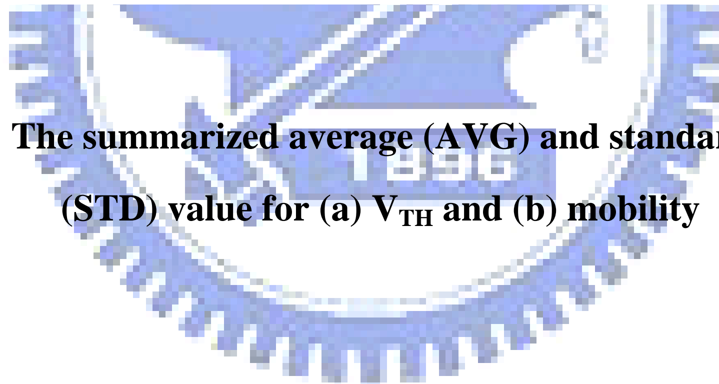

Table 3-1 The summarized average (AVG) and standard deviation (STD) value for (a) V_{TH} and (b) mobility

	Long-range variation	Micro variation
Effect on device parameters	Common trends over a range	Random fluctuate among devices
Possible factors	Film thickness fluctuation, ion implantation dosage, channel length/ LDD length difference	defect sites, defect density, activation efficiency poly-Si grain size/number variation, grain boundary
Design skills	Common variation ➔ Worst case simulation	Random Variation ➔Monte Carlo simulation

Table 3-2 The table illustrating the possible factors for long-range and micro variation as well as the corresponding design techniques

	Average	Standard Deviation
N-type: Vth (V)	1.69	0.03
N-type: Mu (V/dec)	59.66	7.84
P-type: Vth (V)	-2.41	0.05
P-type: Mu (V/dec)	75.31	2.29

Table 3-3 The average and standard deviation value for V_{TH} and mobility for the devices in the crosstie layout

Population in the proposed micro variation model	0.50%	99.50%
ΔVthn (V)	-0.147	0.142
ΔMun (cm^2/Vs)	-10.223	9.723
ΔVthp (V)	-0.155	0.150
ΔMup (cm^2/Vs)	-9.216	8.716

Table 3-4 The upper and lower bound of the parameters used in the simulation of ring oscillator

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Device Type	N-type		P-type	
Standard Deviation	{△Vth} (mV)	{△Mu} ($cm^2/V*s$)	{△Vth} (mV)	{△Mu} ($cm^2/V*s$)
One-finger	22.2	1.8108	28.49	1.7043
Two-finger	15.4	1.3619	20.33	1.1776
Three-finger	12.2	1.1585	16.21	0.9579
Four-finger	10.6	1.0312	15.23	0.8344
Five-finger	8.7	0.9765	13.56	0.7055
Six-finger	8.2	0.9482	12.44	0.6465

Table 3-5 The standard deviation value for V_{TH} and mobility difference with different interdigit finger number

Standard Deviation of {△V_{TH}}	Device	Parameter "a" (V)	Parameter "b" (V*um)
	N-type	-0.0016	0.24
	P-type	0.0013	0.27
Standard Deviation of {△ Mu }	Device	Parameter "a" ($cm^2/V*s$)	Parameter "b" ($cm^2/V*s$)*um
	N-type	0.3081	14.93
	P-type	-0.0765	17.81

Table 3-6 The fitting parameters for fitting the standard deviation of interdigitated layout of poly-Si TFTs

{△VTH} using interdigit layout

Device Type	Coefficient of Determination (r^2)	Fitting Parameter "a" (V)	Fitting Parameter "b" (V*um)
a-Si TFT (N-type)	0.8913	0.0079	0.79
Poly-Si TFT (N-type)	0.9981	-0.0016	0.24
Poly-Si TFT (P-type)	0.9959	0.0013	0.27
c-Si MOSFET (N-type)*	1	2.7E-7	0.024
c-Si MOSFET (P-type)*	1	-9.0E-11	0.001

*Ref.: Chee-Lin Yum, bachelor's thesis, 1996

Table 3-7 The fitting parameters and the coefficient of determination (r^2) for fitting the standard deviation of interdigitated layout of various kinds of devices

Chapter 4

Characterization of Temporal Variation of Poly-Si TFTs: under DC Operation

Preface: In this chapter the reliability behavior of poly-Si TFTs under DC operation is examined. We respectively studied the current transfer characteristics, namely the I_D-V_G curves, and the capacitance characteristics for the device under DC operation. Though there are many papers on the I-V behaviors of poly-Si TFTs under DC stress, there are very few papers on the C-V behaviors for the device after DC stress. In section 4.1, the two main degradation behaviors for the poly-Si TFTs under DC operation, namely the hot carrier and the self heating effect, would be first introduced. The motivation for this chapter would then be described and also the reason we use a special approach to study its capacitance behavior is also provided. A simple device model consisting of the gate capacitances and channel resistances would be introduced and by studying the impedance of the model the short-circuit region and the open-circuit region, or equivalently the ON region and the OFF region, would be inferred and derived. Such model can be used to explain the frequency-dependence behavior, or the dispersion behavior, in the capacitance curves for the device after stress. In section 4-4 the special discussion would be focused on the capacitance behaviors for the n-type device after self-heating stress and the p-type hot carrier stress since they both somehow show the increase of the capacitance for the lower gate voltage during C-V measurement. The validity and the insights of the model are also discussed in section 4-5.

4-1 Review and Motivation

The reliability study of poly-Si TFTs under DC operation can be started with the device parameter change, such as V_{TH}, mobility, ON current, after various stress conditions in the stress map [4-1~4-2]. Refer to figure 4-1 and 4-2, Inoue *et al.* reported that for the n-type poly-Si TFTs, V_{TH} shows apparent degradation as the stress drain voltage V_{DS} and gate voltage V_{GS} are both high. As for the ON current, it is found that it shows obvious degradation for the two regions: one is for the large V_{DS} and V_{GS}, like the previous condition, and the other one is for the large V_{DS} and the V_{GS} is smaller than 10 V. Later, Seok-Woo Lee *et al.* reported that similar behavior can be observed for both n-type and p-type devices that for these two specific regions device would suffer from apparent degradation, as shown in figure 4-3 [4-3]. In the stress map, these two stress conditions show most significant degradation and for the rest of the stress conditions the degradation is almost negligible. These two regions, as characterized as the self heating effect and the hot carrier effect, would be briefly explained in the following article.

Self heating effect, like the one reported in the SOI (Silicon On Insulator) devices, originated from the poor dissipation behavior of the substrate [4-4]. As the operation voltage for V_{DS} and V_{GS} are high, the current conducting in the channel is high and the joule heat, which can be rough calculated as $P=I_{DS} * V_{DS}$, would become large and if the heat can not be dissipated in time it will be accumulated in the active region, as shown in figure 4-4[4-5]. As for the main application field for poly-Si TFTs, the devices are fabricated on glass substrates and the heat transfer coefficients for the films in the device structure are shown in figure 4-5 [4-1]. As can be observed in the figure, if joule heat is generated in the poly-Si film during operation, the films surrounding poly-Si film with much smaller heat transfer coefficients than poly-Si

film would in turn hinder the active region from dissipating heat. Figure 4-6 shows the transfer characteristics for the poly-Si TFTs before and after self heating stress [4-2]. For the stressed device, the subthreshold region, the threshold voltage, the OFF current, the ON current as well as the device mobility is greatly degraded. It was then proposed that the accumulated heat in the channel region would cause the release of hydrogen and in turn deteriorate the effect of passivation. The deep states, originally passivated by the hydrogen atoms, would then be exposed as shown in figure 4-7 and then jeopardize the conduction of the current. [4-1]

Hot carrier effect, to which the similar case in MOSFET device can be referred, has another story from the self heating effect. For the case in MOSFETs, the carriers can have sufficiently high energy to have collision with silicon bonds when the applied V_{DS} is large [4-6]. The generated electron-hole pairs from the collision would have different flow direction. The carriers collected from the substrate can provide useful information in analyzing the degradation mechanism [4-6]. Back to this work, poly-Si TFTs have the similar structure to MOSFETs, but there is no substrate electrode to collect the carrier so that it would be more difficult to examine the mechanism. The absence of the back electrode may also change some faces of the behavior. Figure 4-8 shows the degradation behavior for the poly-Si TFTs stressed with different gate voltages as the drain voltage is fixed at 15 V, while figure 4-9 shows that for the device with different drain voltage as the gate voltage is fixed at 5 V [4-7]. It can be seen that the device degradation gets more serious as V_{DS} increases, just like the case for MOSFETs. However, for poly-Si TFT the degradation is most severe when the gate voltage is around its threshold voltage, which is different from the case MOSFETs in which the effect is most severe for the V_{GS} is around half of V_{DS} [4-8]. Since the hot carrier effect is largely dependent on the drain field, the LDD (Lightly-Doped Drain) structure is adopted to enhance the reliability and it is also

found that this structure also works for poly-Si TFTs, as shown in figure 4-10 [4-7]. The effect of hot carrier stress on the device performance is shown in figure 4-11, in which the stressed device shows lower ON current and correspondingly the device mobility as well as the increase of the OFF current [4-7]. This is mainly attributed to the increase of the tail states after stress. For p-type devices, the dominant mechanism turns out to be the electron trapping in the gate dielectric film and for p-type MOSFETs the effect is called the HEIP (Hot-Electron Induced Punchthrough) effect or the channel shortening effect, in which the trapped electrons would help induce holes and effectively the channel length seems to be shortened [4-9]. Such behavior also occurs for p-type poly-Si TFTs, in which the effect is the increased device mobility and decreased OFF current [4-10]. The transfer characteristics and the schematic figures are given in figure 4-12 and 4-13.

It can then be summarized that the reliability for poly-Si TFTs can be mainly attributed to two mechanisms, namely the hot carrier effect and the self heating effect [4-2]. Though there have been so many papers on the device reliability behaviors after stress, there are very few papers on the capacitance behavior for the stressed device. The study of their C-V behaviors helps us to further understanding of the underlying mechanism since it would enable us to find their behavior locally near the source or the drain junction, while the I-V behavior may just show the overall performance for the whole channel. Another point for the study of the C-V behavior is that for the display electronics, the field in which the poly-Si TFTs are mostly applied, the gate-to-drain capacitance C_{GD} would play an important role in addressing the pixel voltage. As shown in figure 4-14, the pixel voltage would suffer from the feed-through effect and the voltage difference can be described with the equation, in which the voltage shift is directly proportional to the capacitance of the transistor C_{GD} [4-11]. Theoretically in the OFF region, there should be no capacitance value for the

self aligned TFT. But the parasitic behavior may affect this feed through effect and also the device after stress may also have different capacitance behavior for such operation condition. Therefore, the capacitance behavior for the device should be well studied to get a clear understanding for the degradation mechanism and also for the evaluation in the application.

Refer to our previous work, we utilized the two-dimensional numerical simulation tool DESSIS to study the capacitance behavior [4-12~4-13]. In the simulation, the grain boundaries inside the poly-Si film are accounted by using the "effective medium approach," which treats the poly-Si film as a uniform material with the density of localized states in the forbidden gap [4-14]. We tried to fit the capacitance behavior for the stressed device by adjusting the defect density and position both in the physical position and the band diagram. Also, we adjusted the electron and hole cross section to try to fit the capacitance behavior under different measuring frequencies. The simulation results may somehow describe the distortion and shift of the capacitance curves for the stressed device, nevertheless as for the frequency part still the simulation tool may be impotent to describe. From the physical viewpoint this may be explained by the fast state and slow state theory, but we could not find the tool to verify our assumption. Thus, in the following section, we turn to the readily-accessed device transfer characteristics and propose a circuit model that can help us infer the C-V behavior and the corresponding frequency behavior from the I-V behavior. Discussion for the validity of the model for the n-type device is given in section 4-2 and section 4-3 gives that for p-type devices. Special discussion for the capacitance behavior in the OFF region, namely $|V_{GS}| < |V_{FB}|$, would be given in section 4-4.

4-2 Reliability Behavior under DC Operation: n-type Device

Before going deep to the reliability behavior of the devices under DC stress, the I-V and C-V behavior for the fresh device would be introduced first. Figure 4-15 shows the transfer characteristics for the fresh n-type poly-Si TFT, and figure 4-16 shows the normalized capacitance curves with two measuring frequencies for the device. Since the device is of the symmetric structure for the source and drain region, the C_{GS} curves would show the identical behavior to the C_{GD} curves for the fresh device. Referred to the two figures, V_{TH} in the I-V curves plays an important role in defining the ON and OFF region while the flat band voltage V_{FB} in the C-V curves designates the turned-on region and the turned-off region. Referred to the very nature of the physics for V_{TH} in I-V behavior and V_{FB} in C-V curve, these two important parameters also have similar definition. However, from the curves alone there is no apparent connection between these two important parameters. Also, V_{FB} seem to correspond to different values for different measuring frequencies, which is very different from the usual expectation.

In order to explain the frequency dependence of the capacitance behaviors as well as to establish the connection between the I-V and C-V curves, a circuit model consists of channel resistances and gate insulator capacitances is proposed, as shown in figure 4-17. For the unstressed device, the model is composed of the distributing insulator capacitance (C_{in}), channel resistance (R_{ch}), junction capacitance (C_j), and contact resistance (R_C). The C-V behavior and the I-V behavior can be correlated by considering the impedance of the device in this model. As the gate voltage is much higher than V_{TH}, the channel is turned on and the channel resistance will become very small in this case. The total impedance would be dominated by the insulator capacitance. Hence the major part of the signal current to be measured will flow

through the channel resistance and the measured capacitance would be the summation of C_{in}. On the other hand, as the gate voltage is far below V_{TH}, the channel resistances R_{ch} are high such that they would block the signal deep in the channel. Therefore, the measured C-V behavior in this region may actually represent the capacitance behaviors by the edges of the channel. However, for the transient region, neither the resistance nor the capacitance would dominate the impedance. Hence both the capacitance effect and the resistance effect should be considered. Since the capacitive impedance is frequency dependent, the frequency dependence of the measured C-V curves shown in figure 4-16 can be observed.

Figure 4-18 shows the normalized capacitance curves and the total resistances R_{DS} at different C-V measuring frequencies, where the R_{DS} is extracted from the I_D-V_G curves at V_D=0.1 V. For the gate voltage is around V_{TH}, the channel resistance would go through a transient region that the magnitude of the channel resistance would rapidly decrease from around 10^9 to 10^4 Ω. A critical point of the impedance behavior can be selected as the channel resistance R_{ch} equals to the capacitance term $1/2\pi f C_{in}$, which just falls in the transient region of the capacitance curves for the measuring frequency 50 kHz to 1 MHz. The term f represents the measuring frequency. The solid arrow in figure 4-18 represents the point that the total channel resistance R_{DS} equals to the capacitance term $1/2\pi f\, C_{TFT}$ for different C-V measuring frequency, where C_{TFT} is 40 fF representing the gate insulator capacitance of the TFT. The point P_A is the point where the channel resistance R_{DS} is 10 times larger than the capacitance term $1/2\pi f\, C_{TFT}$, and the point P_B is the place when the channel resistance R_{CH} is 10 times smaller. For this study, the arrows respectively point out the 80 MΩ and 4 MΩ of the R_{DS}, corresponding to the impedance of C_{TFT} at the applied frequencies of 1 M Hz and 50 kHz. The 80 MΩ and 4 MΩ two points are called P_C. For the gate voltage lower than P_A, the conductivity of the device is considered to be

low enough that the channel resistance can be taken as open circuit and is labeled as the "O. C. region," in which "O. C." represents "Open Circuit." For the gate voltage larger than P_B, the channel becomes so conductive to be considered as short circuit, and is labeled as "S.C. region," where "S. C." means "Short Circuit." Meanwhile, for the gate voltage between P_A and P_B, since the capacitive term and the resistive term of the impedance are comparable, neither of them can be ignored. By utilizing the proposed circuit model and discussing the impedance of the device, the ON region or the corresponding "S. C. region," can be found for the region the gate voltage is larger than the P_B point. Similarly the OFF region, or the "O. C. region," can be found for the region the gate voltage is smaller than the P_A point, as shown in figure 4-18. The finding of the O. C. region and the S. C. region is calculated from the I-V curves and the C-V curves are found that can be well described by the two regions. This means that the C-V curves show its maximum in the S. C. region and the minimum in the O. C. region. This reveals that by considering the value and position of P_C the C-V behavior can be inferred from the I-V curves. Since the value of the capacitance term is dependent on the measuring frequency, the point P_C would also be affected by the measuring frequency and this is just the feature of this model. In the following section the I-V and C-V behavior as well as their correlation for the device under hot carrier stress and self heating stress will be discussed in the same manner.

Figure 4-19 shows the I_D-V_G transfer characteristics before and after 500 seconds of hot carrier stress with the conventional forward and reverse connection. Here the stress condition is that the drain voltage is equal to 20V and the gate voltage is 1 V larger than V_{TH}, namely 2.8 V. It can be seen that as compared with the unstressed device, the stressed device shows lower ON current and almost unchanged subthreshold region. However, the difference of the ON current of the stressed device between the forward and reverse connection indicates that the states distribute closer

to the drain, which is similar as the MOSFETs. Figure 4-20 (a) shows the normalized gate-to-source capacitance C_{GS} curves before and after stress with different measuring frequencies, and figure 4-20 (b) shows those of the C_{GD} behaviors. The C_{GS} curves of the stressed device show almost no difference as compared with the unstressed device. Nevertheless, the C_{GD} curves of the device after stress somehow show anomalous behaviors. The C_{GD} curve of the stressed device measured at 50 kHz is almost the same as that before stress, but the curve at 1 MHz measuring frequency shows apparent stretch for the gate voltage is just above the flat band voltage V_{FB}. In other words, the degradation behavior of the C_{GD} curves of the device after hot carrier stress is frequency dependent. Comparing the two figures, it can again verified that the degradation mainly occurs near the drain junction and the frequency-dependent stretch out in the C_{GD} behaviors reveals that the state creation should be responsible for the degradation, which is also in consistent with the case in MOSFETs. In order to examine the frequency dependence of the C-V behavior of the devices after hot carrier stress, the C_{GS} and C_{GD} curves of the stressed devices at different applied frequencies are measured, as shown in figure 4-21 (a) and (b). The C_{GS} curves of the stressed device show only negligible shift for different applied frequency. However, in addition to the shift, the C_{GD} curves show apparent stretch between different measuring frequencies for the gate voltage higher than V_{FB}. The higher the measuring frequency applies, the more the C_{GD} curve stretches.

Figure 4-22 (a) and (b) are the normalized capacitance characteristics of C_{GS} and C_{GD} with the total resistance R_{DS} extracted from the I_D-V_G curves for the device after hot carrier stress. Here, the P_C is represented as the green lines with the arrow and acts as the reference point in R_{DS} curve and C-V curve. Figure 4-23 (a) shows the circuit model for the device after hot carrier stress. The term C_{deg} and $R_{ch,deg}$ represents the increase of the capacitance and resistance owing to the generated tail states during

stress. Figure 4-23 (b) shows the corresponding location in the bandgap of the capacitance C_{deg}. Because the tail states are mainly related to the operation of the gate voltage above V_{TH}, the state capacitance C_{deg} would respond at the gate voltage larger than V_{FB}. Under this gate voltage, the Fermi level is drawn near to the bottom of the conduction band E_C and then fills the capacitance C_{deg}. For the low measuring frequency of 50 KHz, the point P_C locates at 80 Mega ohm, in which the R_{DS} curve is located at the faster-switch point. The capacitive term $1/2\pi f \cdot C_{TFT}$ is relatively larger than the channel resistance at the gate voltage slightly larger than V_{TH}. Therefore the measured C_{GS} and C_{GD} characteristics would quickly attain the gate capacitance in the channel and saturate at C_{TFT}. Hence the effect of the degradation component C_{deg} may not be obvious. However, for the high measuring frequency of 1 MHz, the channel resistance can only be ignored till the gate voltage is much larger than V_{TH} and thus the effect of the C_{deg} components can be apparent. In other words, the degradation in the C-V behaviors for the device may only be observed at higher measuring frequencies, where the effect of the degraded capacitances can be obvious and not covered.

Figure 4-24 gives the transfer characteristics for the device under the self heating stress for 500 seconds. The stress condition is that both V_{GS} and V_{DS} equal to 18V. For the stressed devices, the increased V_{TH} and the subthreshold swing, and also the decreased ON current can be observed in both the forward and reverse connection. Figure 4-25 (a) shows the C_{GS} curves before and after stress with different frequencies, while figure 4-25 (b) shows the corresponding curves of C_{GD}. Compared to those before stress, the stressed C_{GS} and C_{GD} curves exhibit two main changes, namely the positive shift for the gate voltage near the flat band voltage V_{FB} and the increase for the gate voltage just below V_{FB}. The stretch and shift in the positive direction for the gate voltage near V_{FB} are considered to be attributed to the increase of the deep states

during stress. On the other hand, the increases of the C-V curves for the lower gate voltage possibly come from the interface states [4-12]. Figure 4-26 (a) and (b) are the normalized capacitance C_{GS} and C_{GD} and the total resistances R_{DS} extracted from the I_D-V_G curves. Here, the P_C is again represented as the green lines. Figure 4-27 (a) shows the proposed circuit model of the device after self heating stress. The capacitance C_{deep} is added to the device, representing the increase of the deep states during stress. In addition, the C_{deg} is also introduced to represent the capacitance corresponding to the interface states induced by the high voltage difference V_{GS} during stress [4-12]. Figure 4-27 (b) and (c) show the corresponding location in the bandgap of the capacitance C_{deep} and C_{deg}. Because the deep states in the channel would affect the operation for the gate voltage near V_{FB}, the position of the C_{deep} is located near the Fermi level E_F in the bandgap. On the other hand, because the C_{deg} is found to influence the conduction for the gate voltage below V_{FB}, the corresponding position of the C_{deg} is set to locate partly below E_F. Refer to figure 4-26 (a) and (b) , in the O.C. region, since all the channel resistances are taken as opened, in the device the model is reduced to only the capacitances at the edges. Thus the C_{deg} resulting from the interface states and the C_{deep} from the self heating effect would lead to the increase of the C_{GS} and C_{GD} curves for the lower gate voltage, respectively. In this region, the different frequency dependences for C_{GS} and C_{GD} curves reflect the different responses of the states near the source and the drain, respectively. As the gate voltage increases, two effects make the C_{GS} and C_{GD} curves change with gate voltage. Firstly, the Fermi level is drawn near to E_C and the interface states are thus getting filled. Secondly, the channel resistance would also be gate voltage dependent. Hence the stretch and shift of the C-V curves in the transient region may include the effect of the increase of the C_{deep} and the decrease of R_{ch}. For the higher gate voltages, all the states are filled and the channel resistances are very low, making the measured capacitance

C_{GS} and C_{GD} saturate at C_{TFT}. The proposed model may fairly explain the frequency-dependent degradation of the capacitance curves after both the hot carrier and self heating stress conditions.

4-3 Reliability Behavior under DC Operation: p-type Device

Before discussing the behaviors of the device performance for the p-type device after stress and the corresponding device model, again we examine the device performance for the fresh device. Figure 4-28 shows the initial transfer characteristics of typical p-type TFTs, while figure 4-29 shows the C-V behavior of the device. Since for the fresh device the behavior should be identical for the forward and reverse measurement, thus the behavior in the forward connection is the same to that in the reverse connection, so are in the manners for the C_{GS} and C_{GD} behaviors. Based on the same idea and the same circuit model for the device, figure 4-30 shows the normalized C_{GS} curves and the total resistance R_{DS} at different C-V measuring frequency, where R_{DS} is extracted from the I_D-V_G curves at V_D=0.1 V. The point P_C is represented as the green arrow and the points P_A and P_B are defined in the same manner as in the previous section. As can be observed in the figure, the S. C. region and the O. C. region can well designate the turned-on and turned-off region in the C-V curves both for the measuring frequency 50 kHz and 1 MHz.

Figure 4-31 (a) shows the I-V curves before and after the hot carrier stress, as the stress condition is that V_{GS} and V_{DS} are -3 V and – 20 V with time duration 500 seconds. Referred to the figure, the device performance shows no obvious change other than the decrease of the leakage current. The decreased leakage current in the forward measurement indicates that the electric filed in the channel edge near the drain was relieved. [4-15] In addition, the transconductance of the device, which can be utilized to find the device mobility, shows apparent increase as shown in figure

4-31 (b). This phenomenon is similar to the hot-electron-induced punchthrough (HEIP) in MOSFETs [4-16], the primary hot-carrier degradation mechanism of PMOSFETs and can be attributed to negative charge trapping in the gate oxide. The injection of electrons into the oxide causes drain extension and thus reduces the effective channel length. This mechanism would result in the increase of the transconductance with stress time and therefore the on current shall increase. Since the collision-generated electrons would be happening near the drain junction, the localized and nonuniform buildup of oxide traps charges should be mainly located near the drain junction.

The normalized C_{GS} curves before and after stress measured with different frequencies is given in figure 4-32 (a) and figure 4-32 (b) shows those of the C_{GD} curves. After stress, the C_{GD} curve for the two measuring frequencies will both increase in the off region. The increase in the C_{GD} could be explained that the operation increases the overlapped capacitance. On the other hand, after stress the C_{GS} value was not altered, and hence the phenomenon may attribute to the charge trapping near the drain. Though the C-V behavior may somehow be explained by the trapped charges and the overlapping capacitance, it would be of interest to see how the previous proposed model fit in the hot carrier effect for the p-type devices. Figure 4-33 (a) and (b) are the normalized capacitance characteristics of C_{GS} and C_{GD} with the total resistance R_{DS} extracted from the I_D-V_G curves for the device after hot carrier stress. The P_C, represented as the green arrow, is the reference point in R_{DS} curve and in C-V curve. And figure 4-34 shows the circuit model for the device after stress, in which the R_{ch}' means the locally-changed resistance because of the oxide-trapped charges near the drain side. For the two figures, it can be observed that since the transfer characteristics in the subthreshold region shows no apparent change, the corresponding R_{DS} behavior is almost the same and so is the derive of the point P_A and P_B. Comparing figure 4-30 and 4-33, it can be found that they are almost the same

except for the increase for the gate voltage lower than V_{FB} in the C_{GD} curves for the stressed device. It may somehow reveal that the proposed method may not be capable of describing the behavior for the device in the OFF region, since in this region the R_{DS} is too large.

Figure 4-35 shows the I-V transfer characteristics for the TFT before and after self heating stress. The stress condition is that both V_{GS} and V_{DS} equal to -18V and the time duration is 500 seconds. For the stressed device, it can be seen that the V_{TH} shifted in negative direction both for the forward and reverse connection. Besides the shift, in the subthreshold region the curves for the stressed device show no apparent distortion, meaning that the trapped charges may be the dominant mechanism instead of deep state creation. For this point the behavior is quite different from the self heating effect on n-type devices. Figure 4-36 (a) shows the C_{GS} curves before and after stress for the p-type device after self-heating stress with different measuring frequencies, while figure 4-36 (b) shows that curves of C_{GD}. For the stressed device, it can be observed that the large shift occurs for both the C_{GS} and C_{GD} curves and for both measuring frequencies, which indicates that the degradation mainly should come from the trapping charges. Figure 4-37 (a) and (b) are the normalized capacitance C_{GS} and C_{GD} and the total resistance R_{DS} extracted from the I_D-V_G curves, and figure 4-38 gives the proposed device model for the stressed TFT. The R_{ch}' represents the channel resistance influenced by the self heating stress. The trapped charges make the threshold voltage shift in the negative direction and in the model this should effectively make the resistance larger than the fresh device. Back to the R_{DS} curves, the shift of the subthreshold region in the I-V curves would make the R_{DS} curves shift and correspondingly the point P_C would locate at the more negative gate voltage. For the C-V versus R_{DS} curves, though both the I-V and C-V curves show large shifts, the calculated P_C and the corresponding O. C. region/S. C. region could still fairly fit in

the region to describe the C-V curves both for the C_{GS} and C_{GD} curves and for the two measuring frequencies. This may indicate that the proposed circuit model to correlate the I-V and C-V curves can be utilized to describe the device behavior both for the initial and stressed device characteristics.

4-4 Discussion

Though in the previous section, it is shown that the proposed device model can be used to infer the C-V curves from its I-V curves by considering the impedance, the method still has some incompleteness. The proposed method can be used to calculate the transient region and it assumes that the device is turned-off for the gate voltage is below its V_{FB} and the R_{DS} at this time would be so large that there should be no capacitance could be measured. However, if due to some kind of stress the capacitance at the edge is changed or the channel resistance is locally reduced, the signal may then propagate deeper some place inside the channel region or some degradation capacitance may be measured. Refer to the C_{GS} curves for the n-type device after self heating stress, as shown in figure 4-25 (a), and the C_{GD} curves for the p-type device after hot carrier stress, as shown in figure 4-32 (b), they both exhibit some kind of capacitance increase in the OFF region. Such behavior can not be inferred from the I-V behavior, let along its frequency dependence. Though this may be the incompleteness of the method, it somehow indicates that for the transient and ON region, the C-V behavior can be calculated from the correlation between the I-V and C-V method proposed in this work. And the capacitance behavior for the gate voltage below V_{FB}, which can not be inferred from the I-V behavior, can truly unveil the device behavior locally near the source or drain region.

4-5 Summaries

In this chapter the device performance under DC operation, including its I-V and C-V behavior, is closely examined. A circuit model containing the channel resistance, the gate insulator capacitance and the contact resistance is proposed and the device's I-V and C-V performance are found that can be correlated by considering the device impedance where the resistance term equals to the capacitance term. The critical point is called P_C and since the capacitance term is frequency dependent the location of P_C is also dependent on the measuring frequency in C-V measurement. The method to infer the C-V behavior from its I-V behavior is utilized to see its validity on the fresh device and the device under hot carrier stress and self heating stress. The method is found to fairly describe the C-V behavior but for the stressed device, if the stress causes the increase of the capacitance or the decrease of the resistance at the edge, in the OFF region the C-V curves could be altered and such change could not be inferred from its I-V curves. This may reveal that the study for the device performance via the C-V measurement may still be an important technique to study the behavior near the channel edge and the behavior may be shown in the OFF region of the C-V curves. The proposal of the device model as well as the interpretation of the C-V curves should provide important information for designers for evaluating the device performance. Also, it should be helpful for the study of device reliability and the deeper understanding of the degradation mechanism.

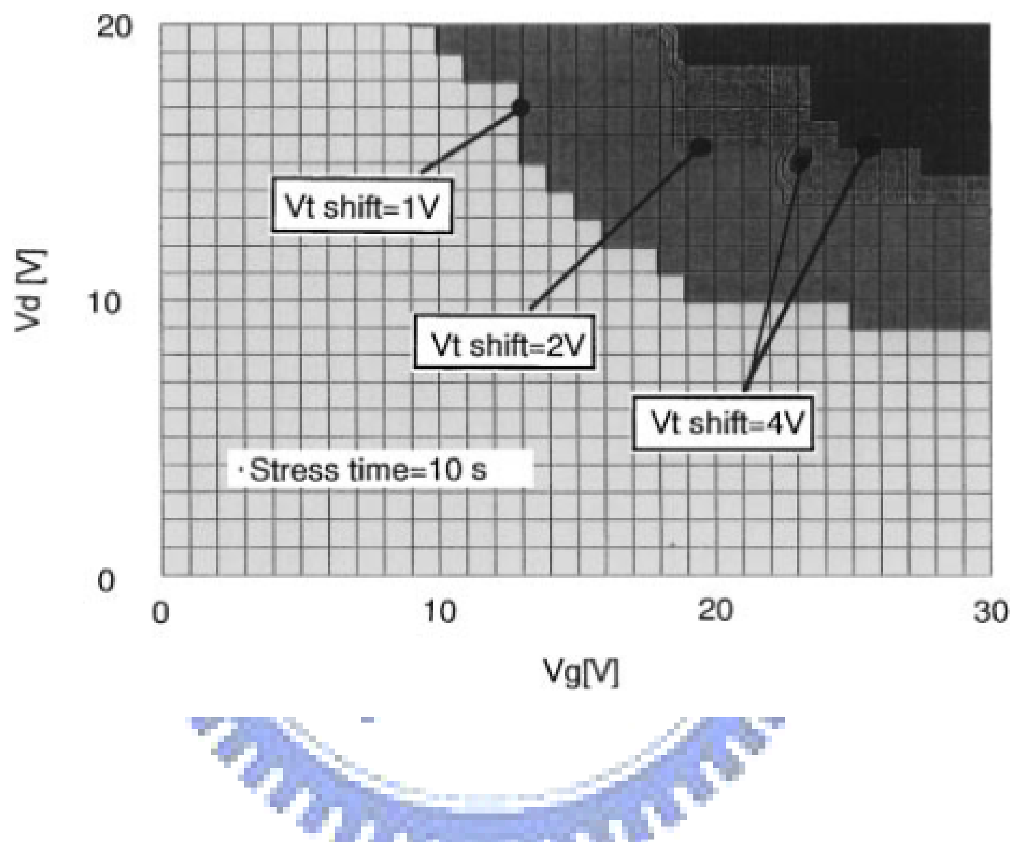


Figure 4-1 The threshold voltage shift under various stress conditions in the stress map

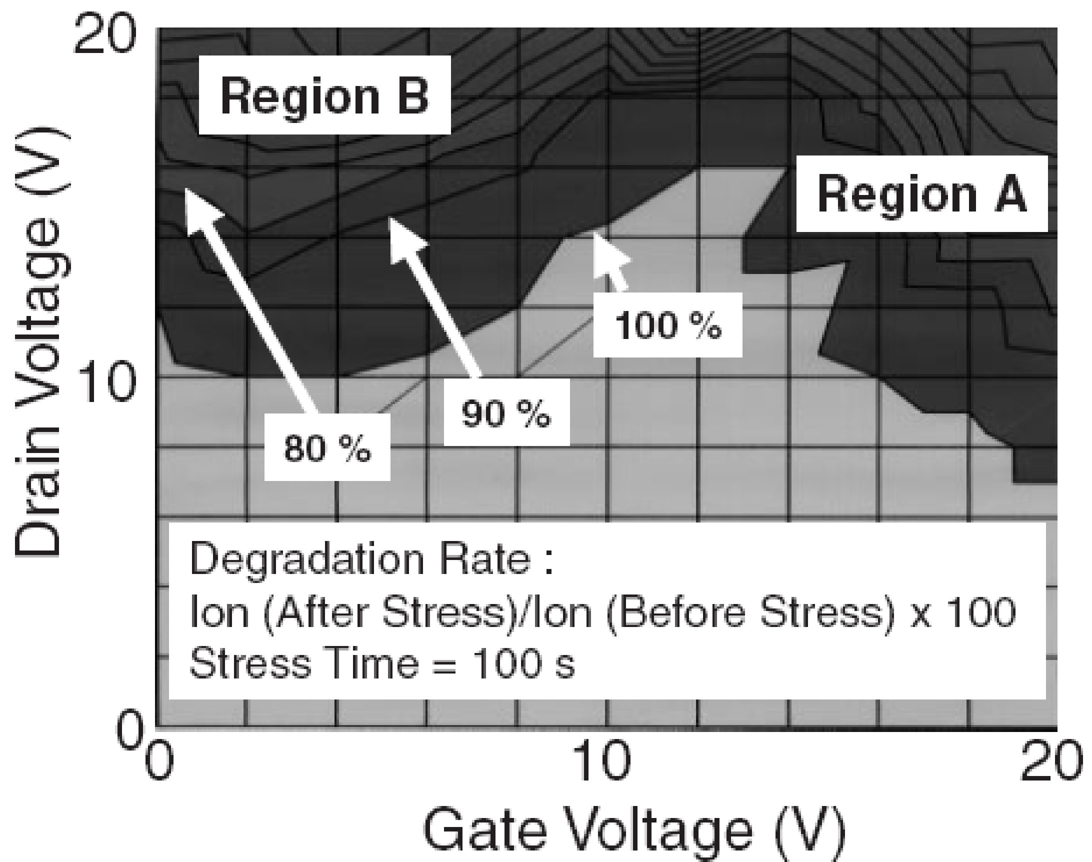


Figure 4-2 The ON current degradation under various stress conditions in the stress map

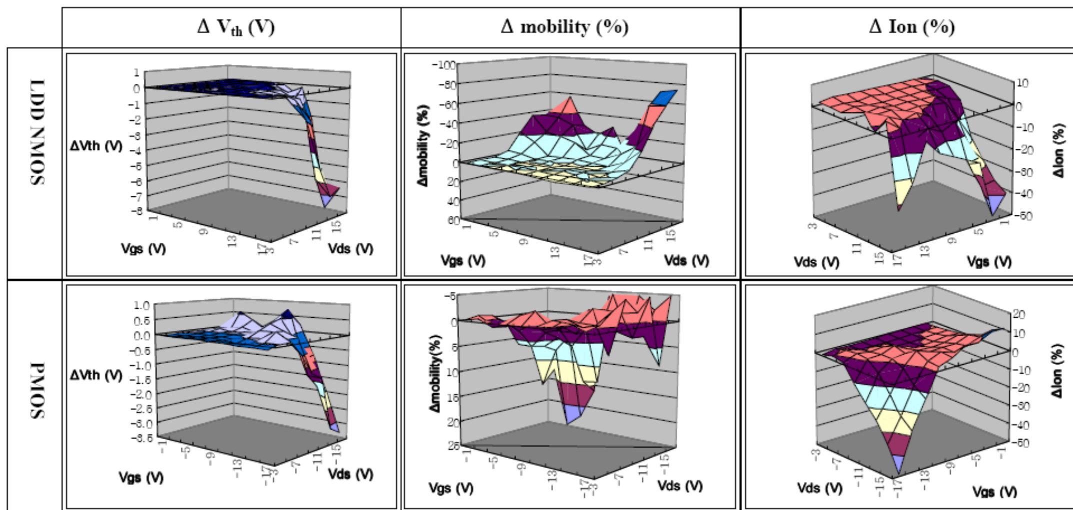


Figure 4-3 The threshold voltage, mobility and ON current for the LDD NMOS and PMOS devices under various stress conditions in the stress map

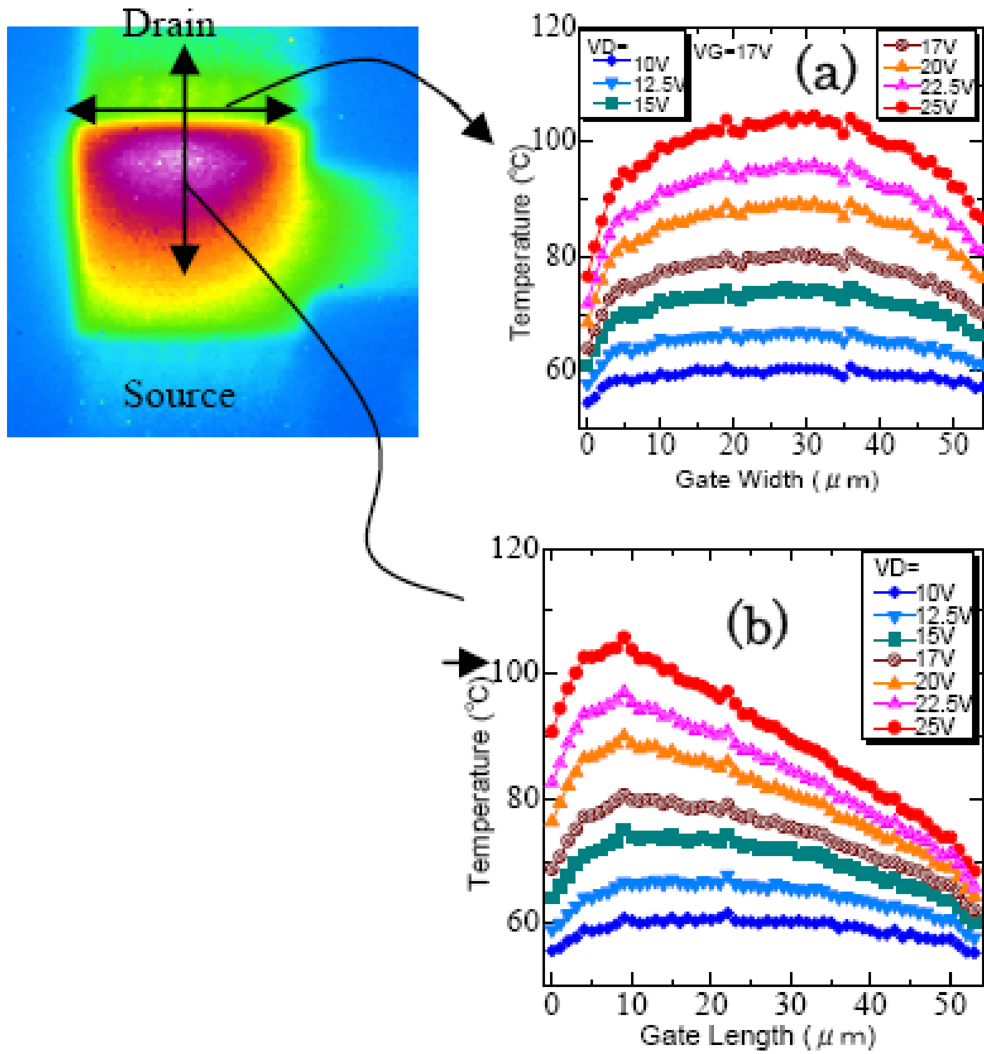


Figure 4-4 The profile of Joule heat generated in the channel for the device under self heating stress

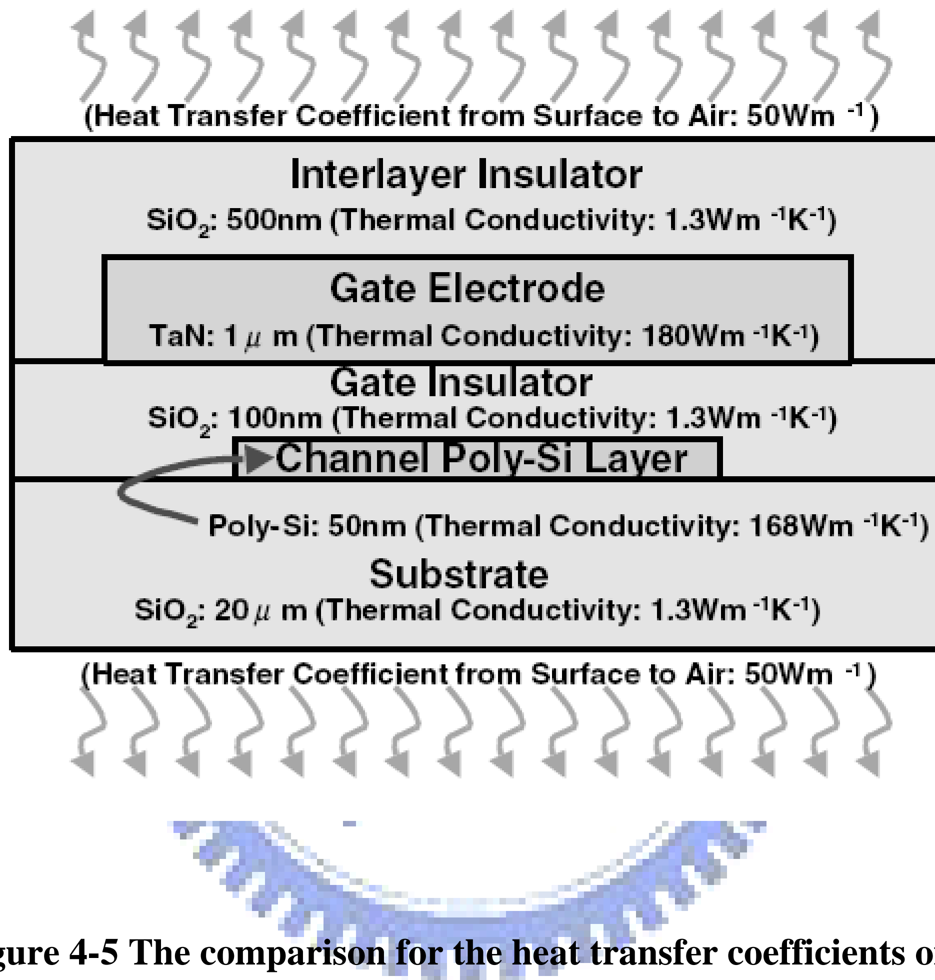


Figure 4-5 The comparison for the heat transfer coefficients of the films for the poly-Si TFTs

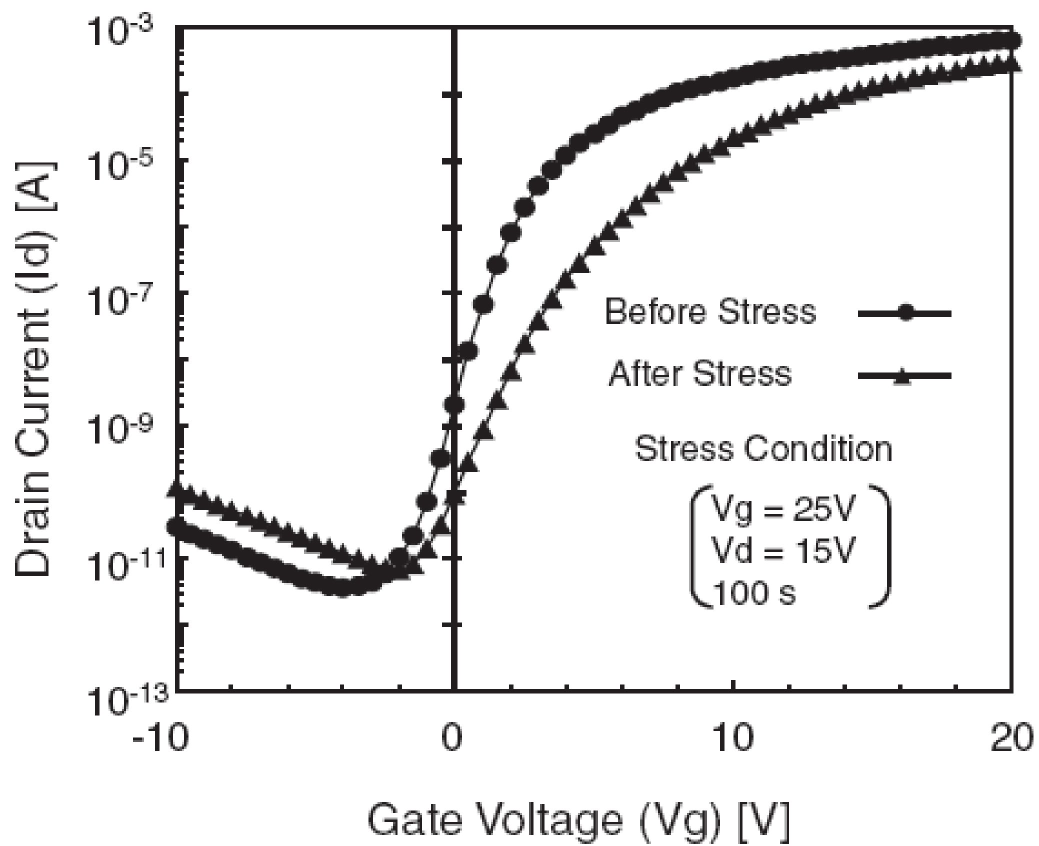


Figure 4-6 The transfer characteristics for the n-type device after self-heating stress

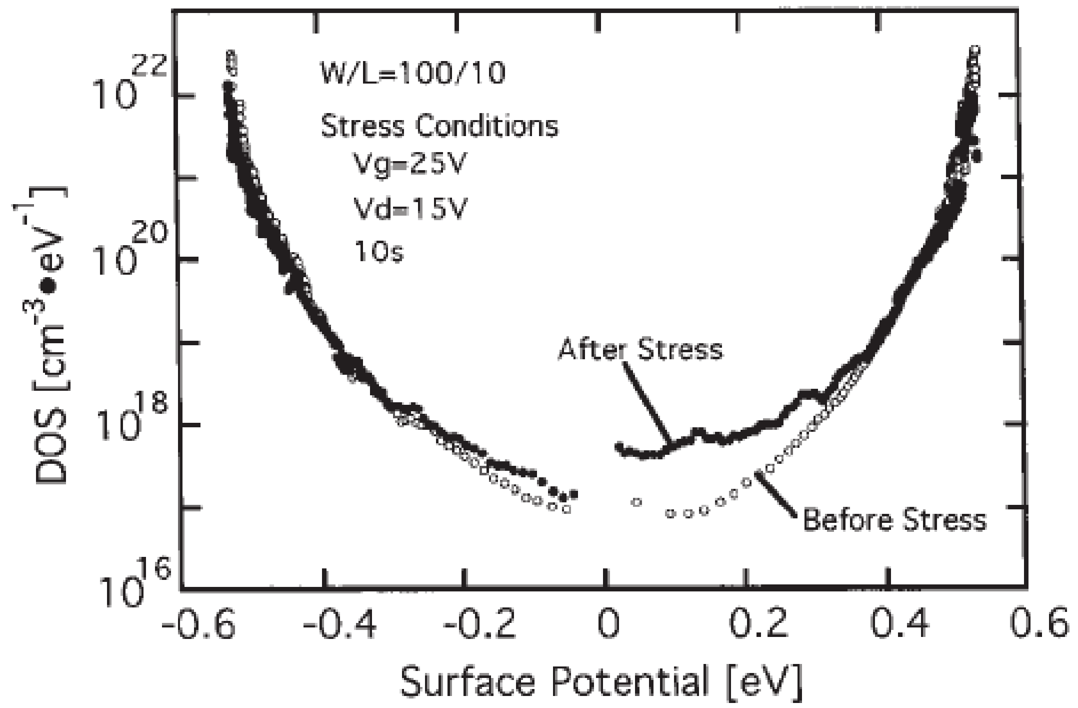


Figure 4-7 The density of states (DOS) for the device before and after self heating stress

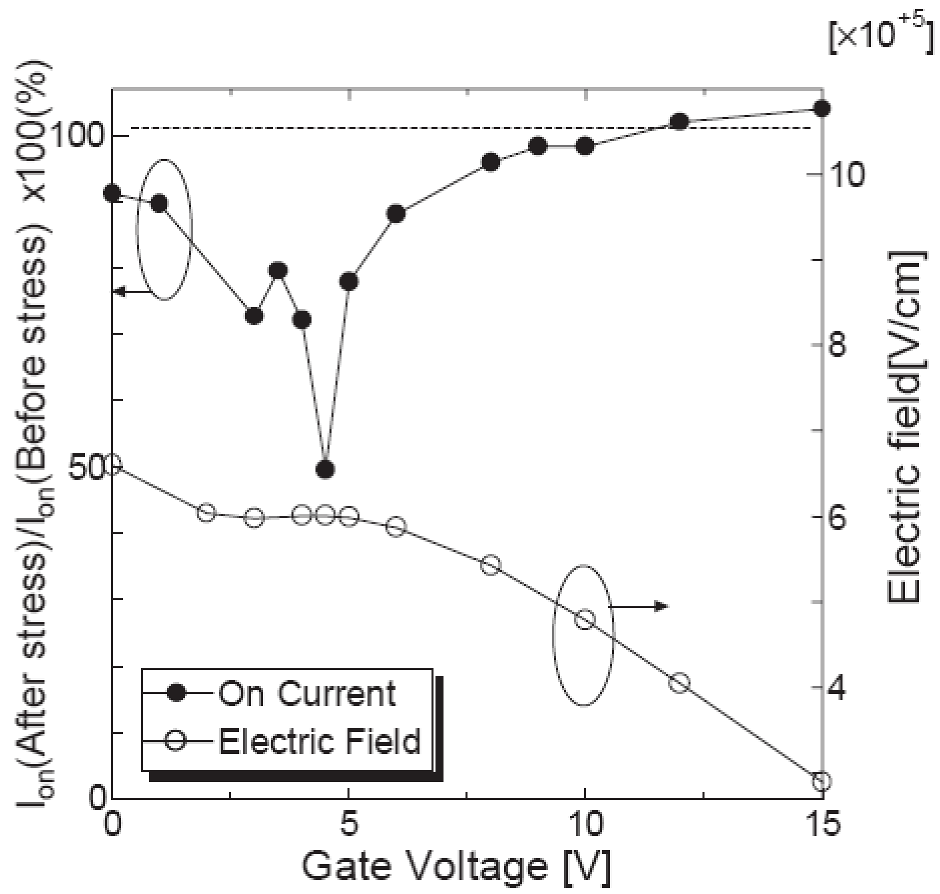


Figure 4-8 The ON current degradation and the electric field for the device under hot carrier stress with various gate voltages

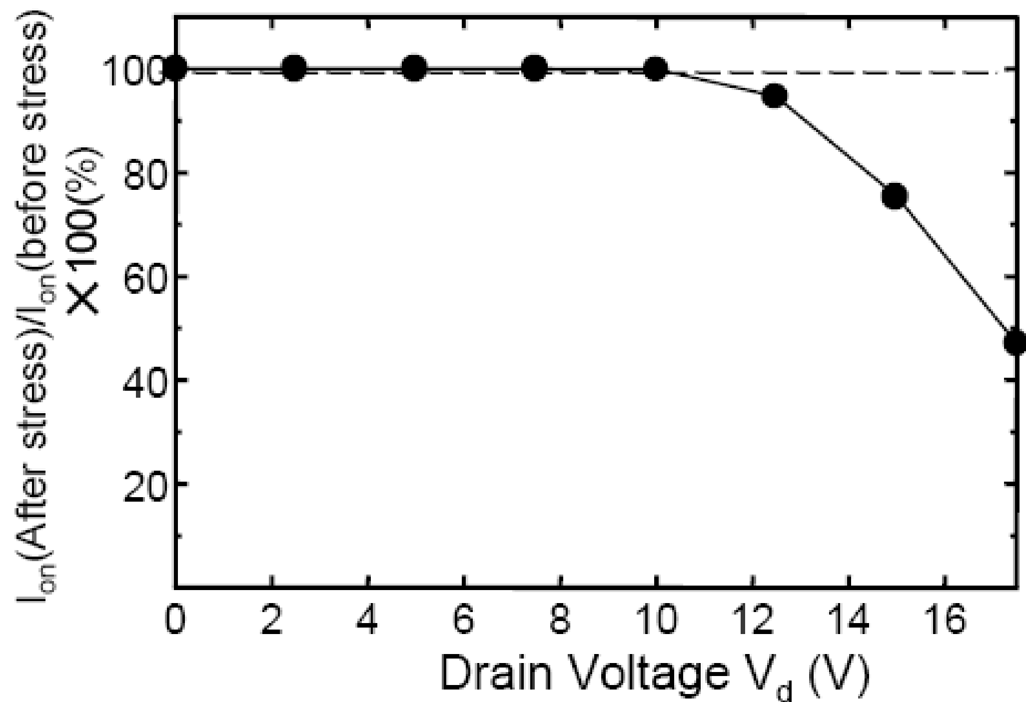


Figure 4-9 The ON current degradation for the device under hot carrier stress with various drain voltages

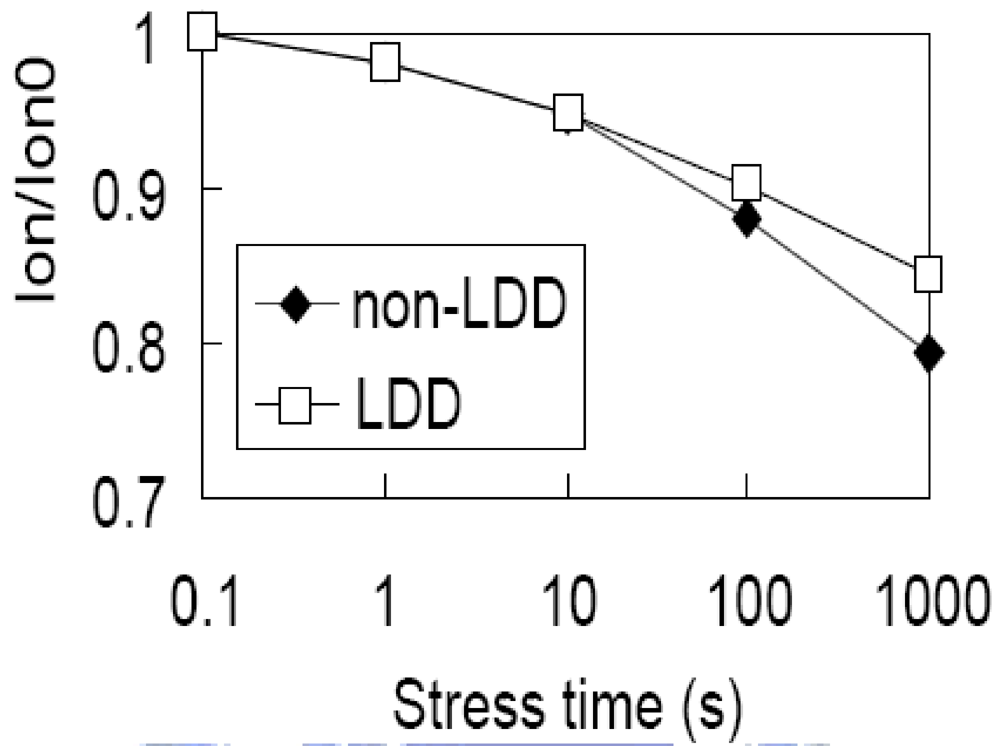


Figure 4-10 The ON current degradation for the device under hot carrier stress with and without the LDD structure

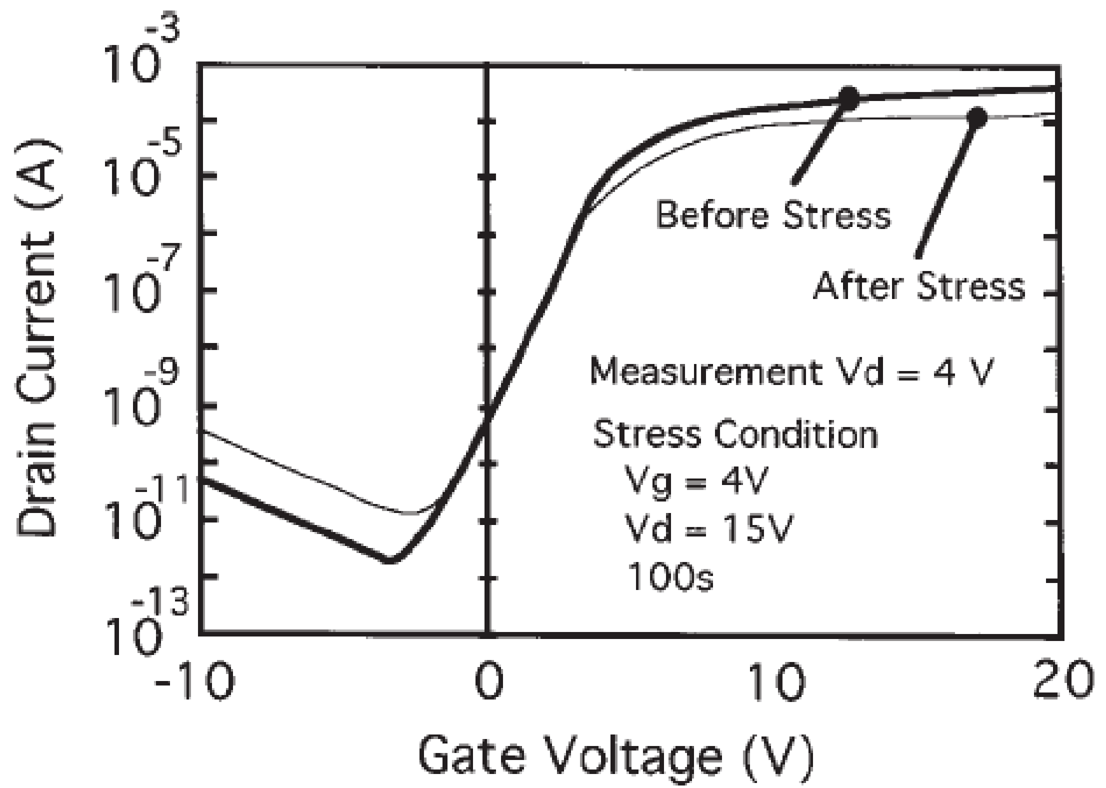


Figure 4-11 The transfer characteristics for the n-type device after hot carrier stress

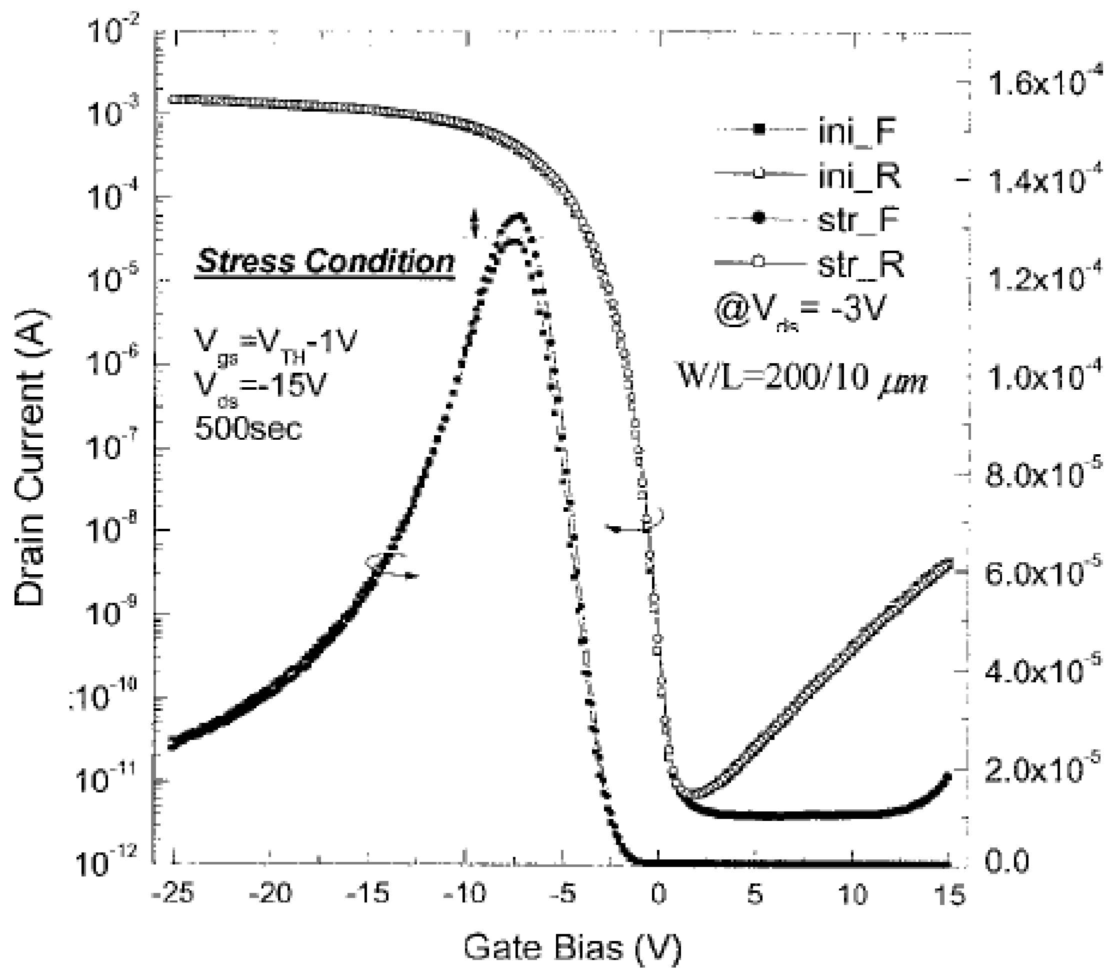


Figure 4-12 The transfer characteristics for the p-type device after hot carrier stress

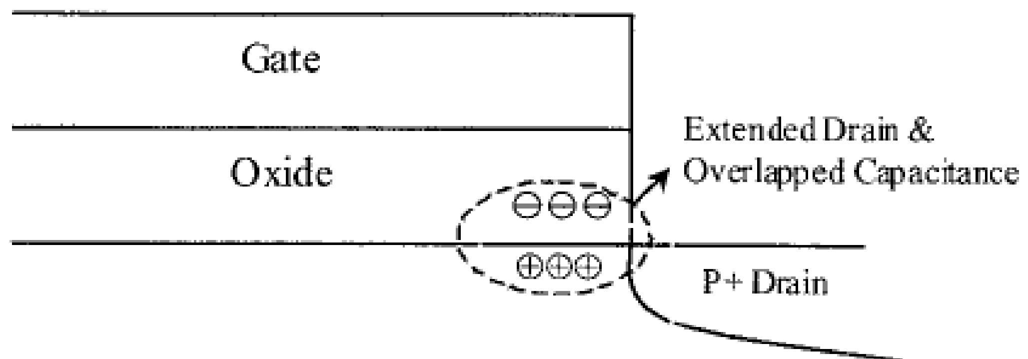
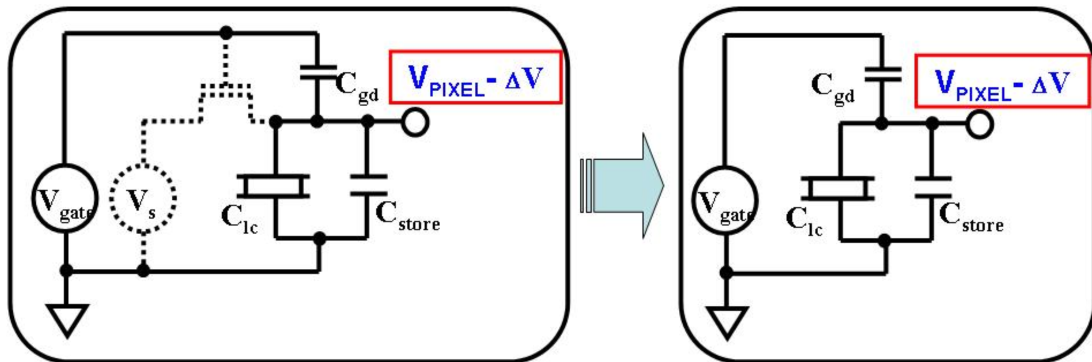


Figure 4-13 The proposed mechanism for the increase of the mobility for the p-type device after hot carrier stress

As the pixel charging is finished and the TFT is turned off:



The Kick-back voltage (or the feed-through voltage) is given as:

$$\Delta V = \frac{C_{gd}}{C_{gd} + C_{lc} + C_s} \times \Delta V_{gate}$$

Figure 4-14 The kick-back voltage in addressing the pixel voltage in TFT-LCD panels

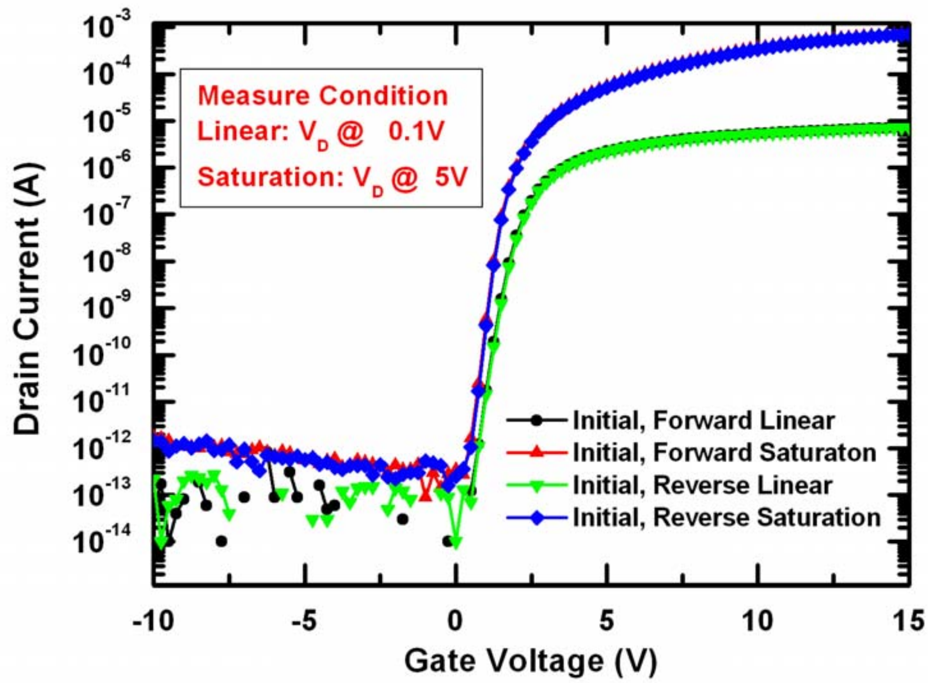


Figure 4-15 The transfer characteristics for the fresh n-type device

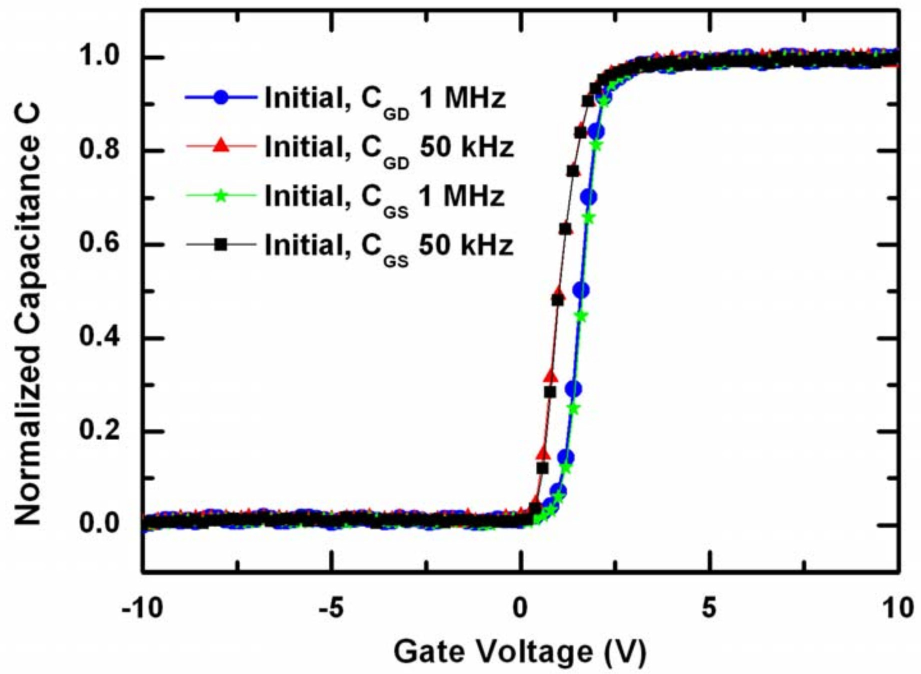


Figure 4-16 The normalized capacitance curves for the fresh n-type device

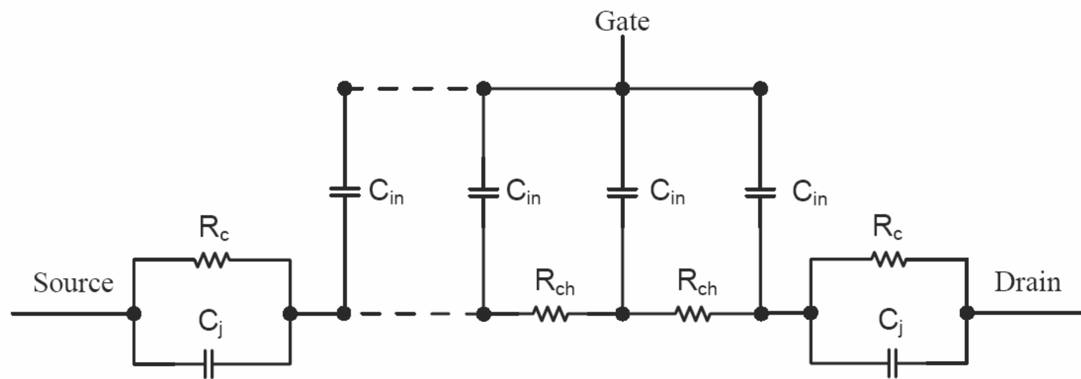


Figure 4-17 The proposed circuit model for poly-Si TFTs

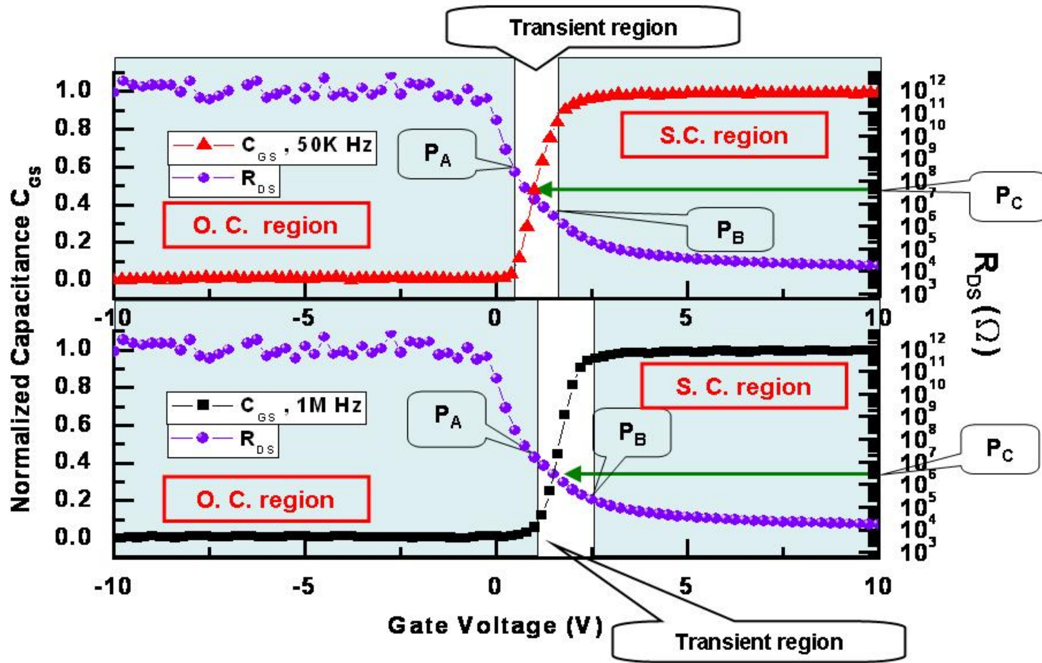


Figure 4-18 The R_{DS} curves V.S. capacitance curves for the fresh n-type device

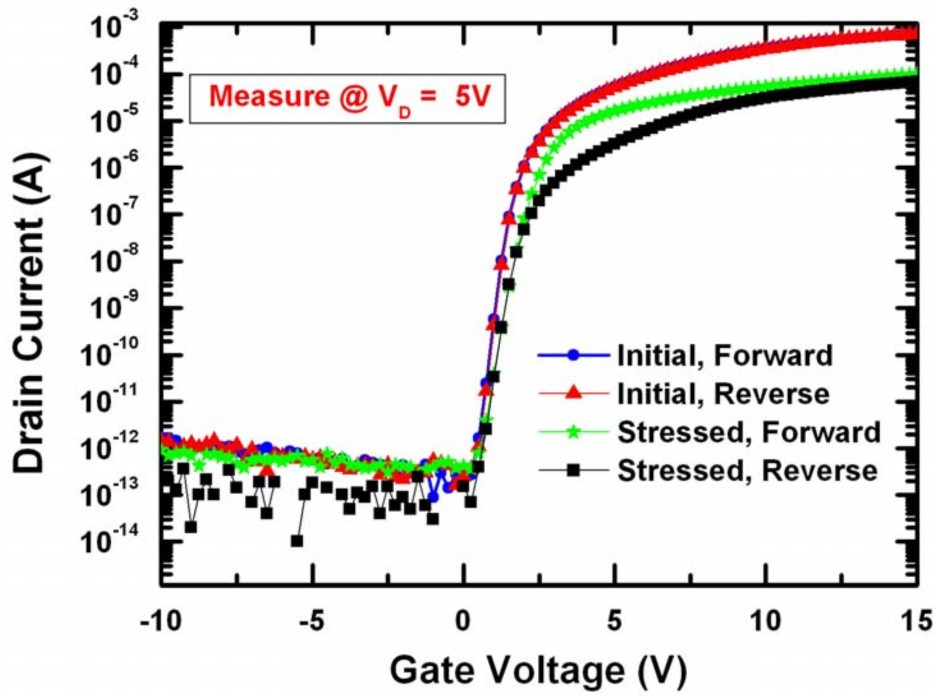
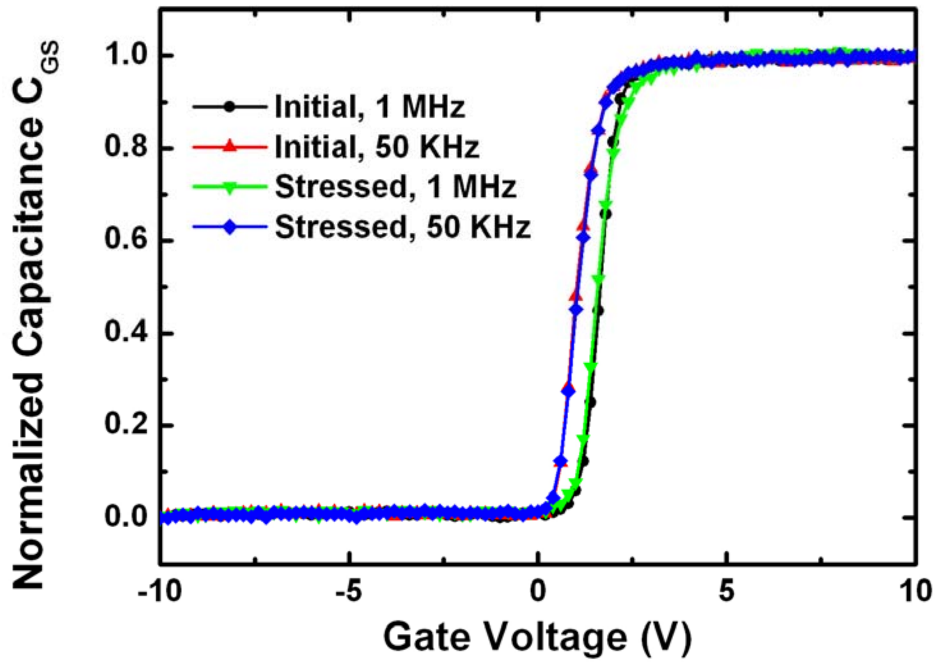
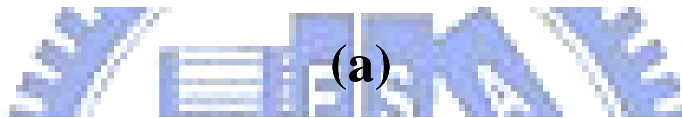
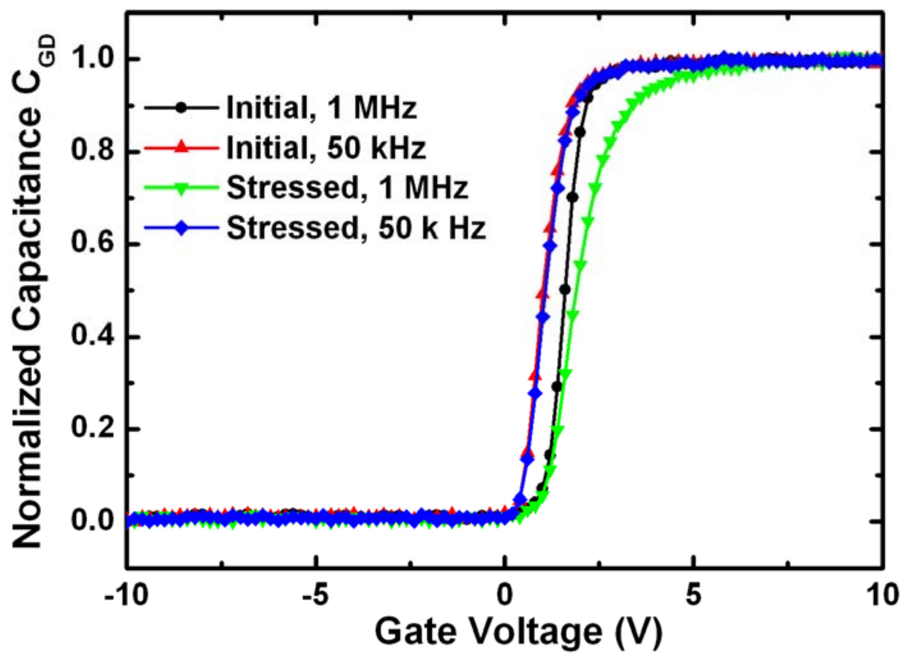


Figure 4-19 The transfer characteristics for the n-type device before and after hot carrier stress



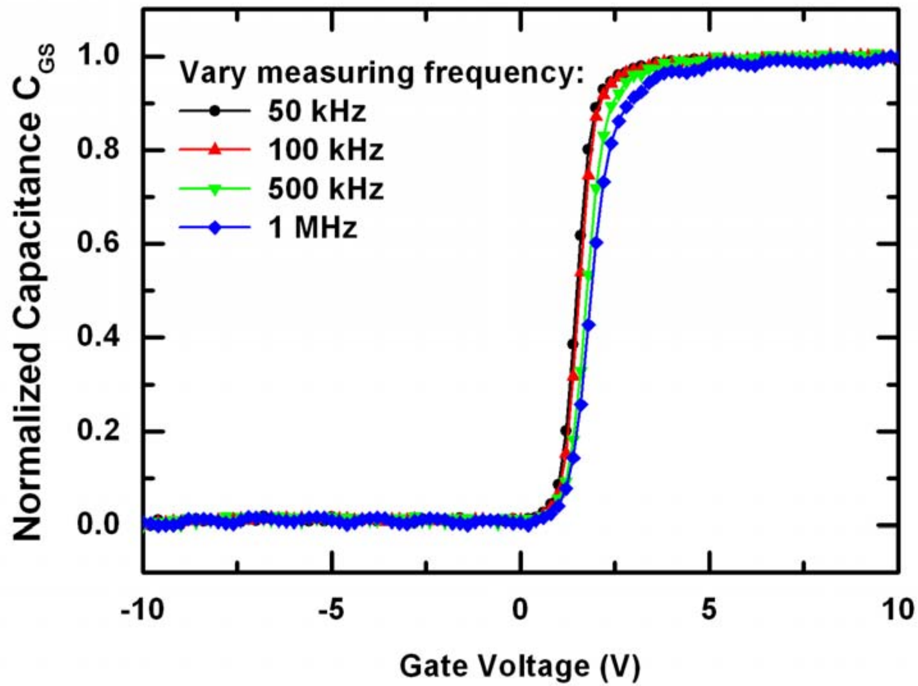


(a)

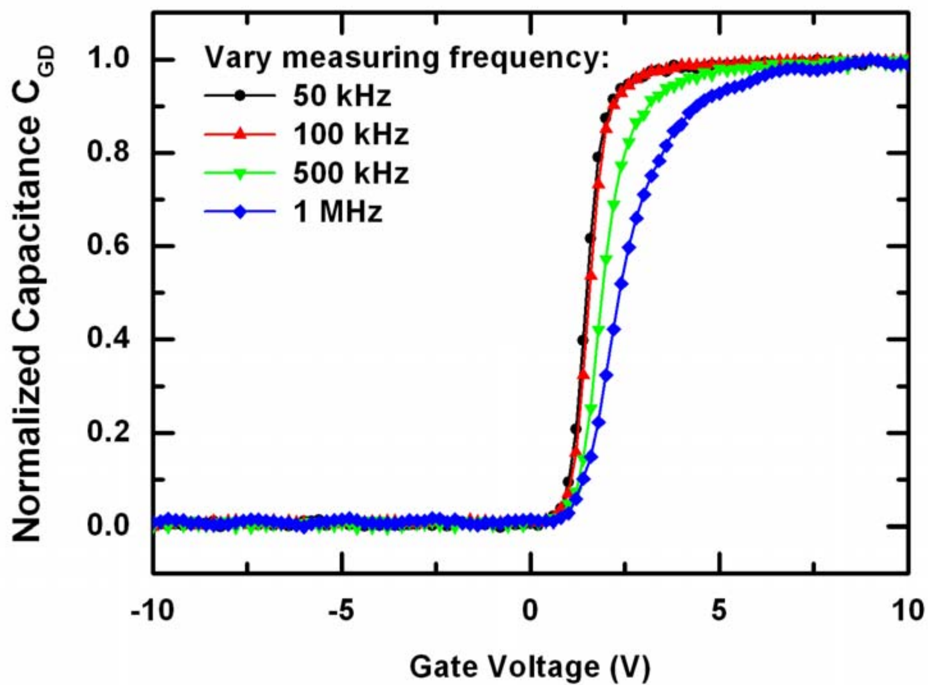


(b)

Figure 4-20 The normalized capacitance curves of (a) C_{GS} and (b) C_{GD} curves for the device before and after hot carrier stress

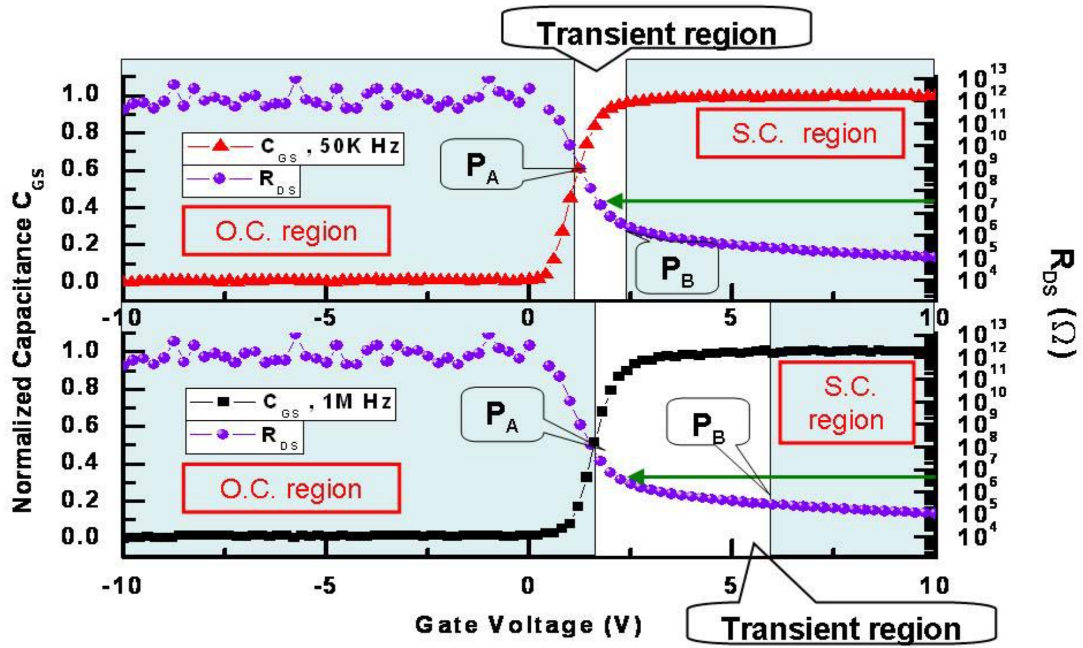


(a)

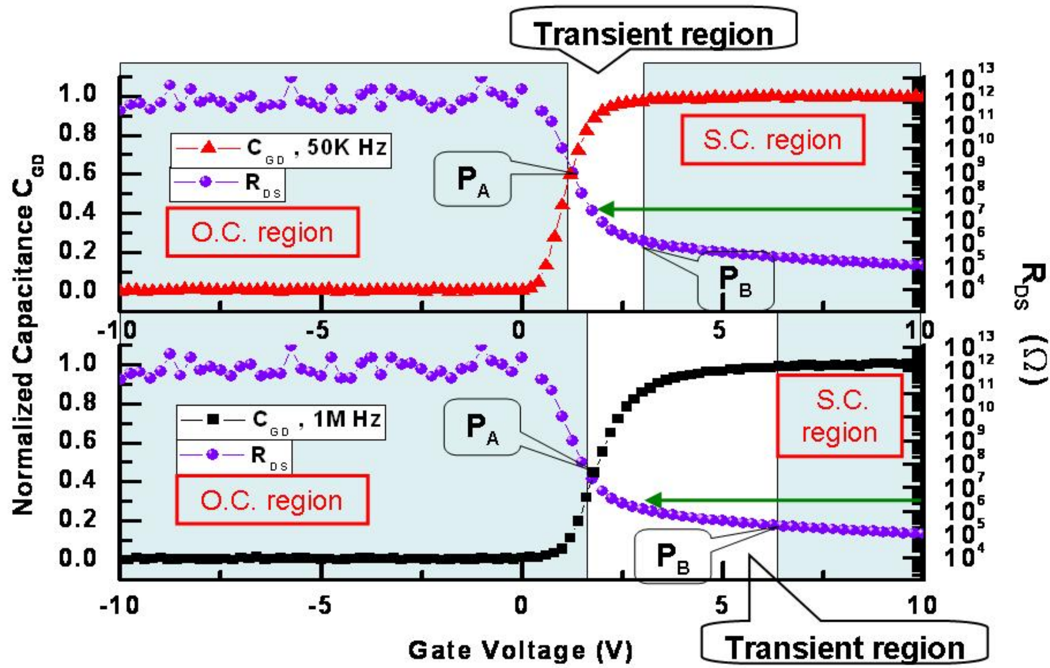


(b)

Figure 4-21 The normalized capacitance curves of (a) C_{GS} and (b) C_{GD} curves for the device after hot carrier stress with various measuring frequencies

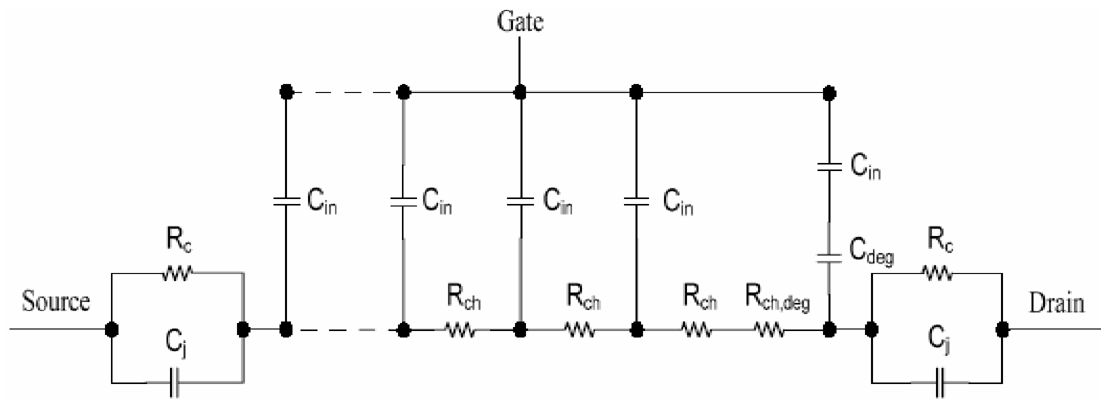


(a)

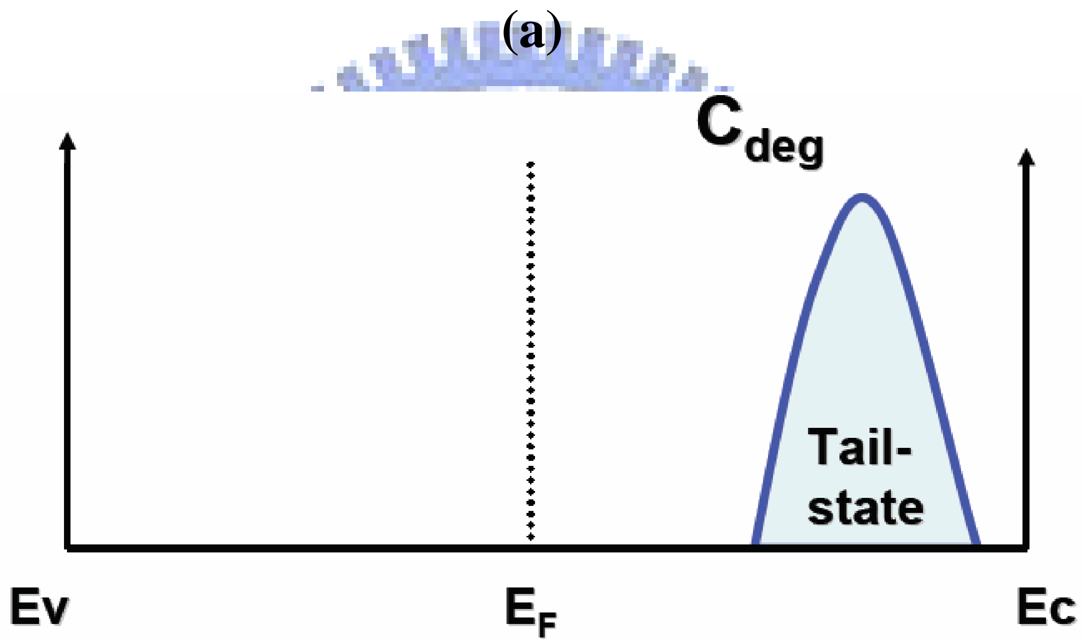


(b)

Figure 4-22 The R_{DS} curves V.S. the (a) C_{GS} and (b) C_{GD} curves for the device after hot carrier stress



(a)



(b)

Figure 4-23 (a) the proposed circuit model for the device after hot carrier stress and (b) the figure illustrating the corresponding location of C_{deg} in the bandgap

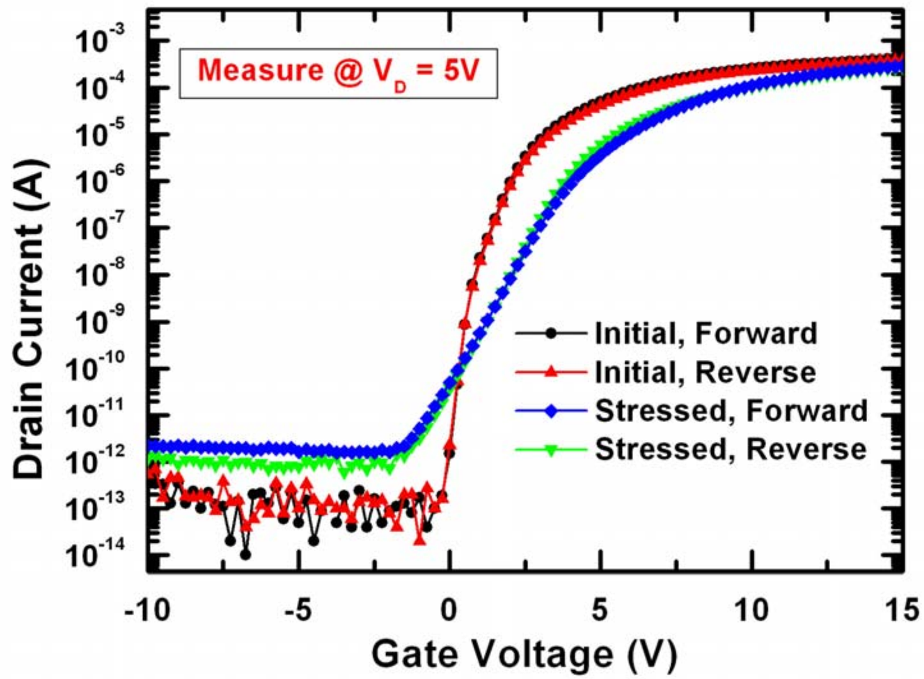
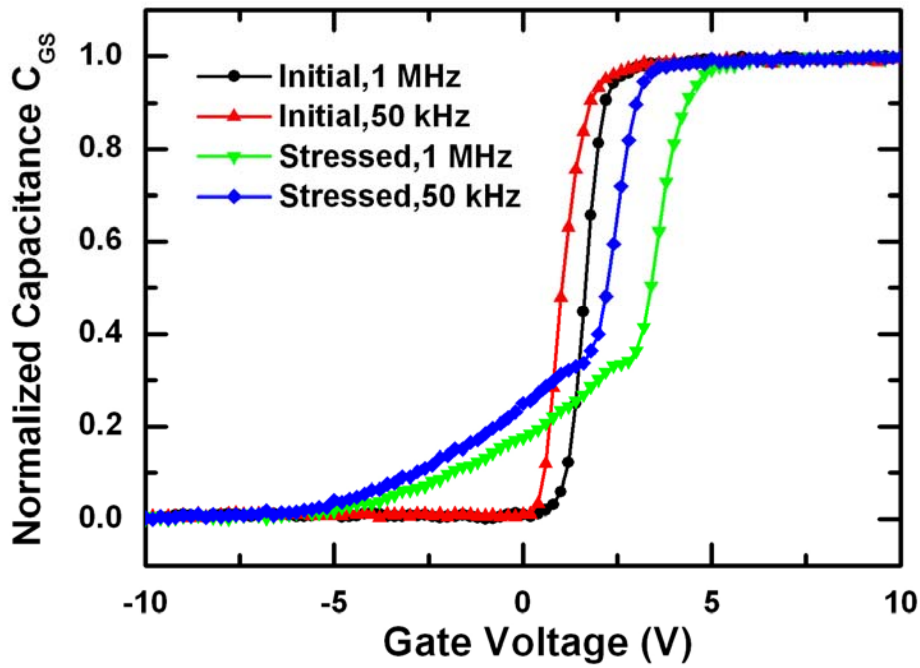
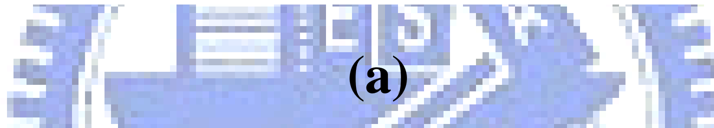
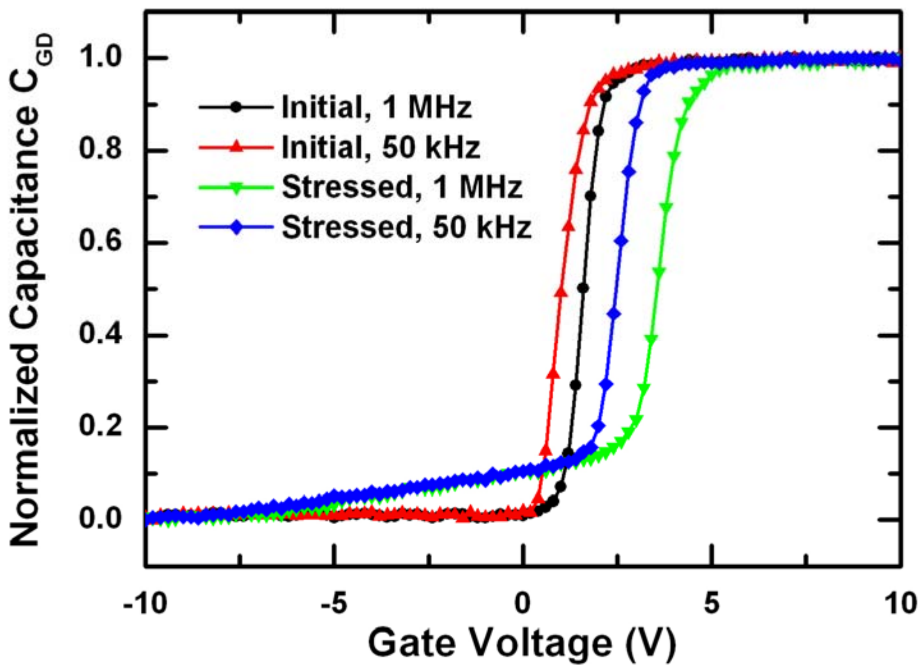


Figure 4-24 The transfer characteristics for the n-type device before and after self heating stress



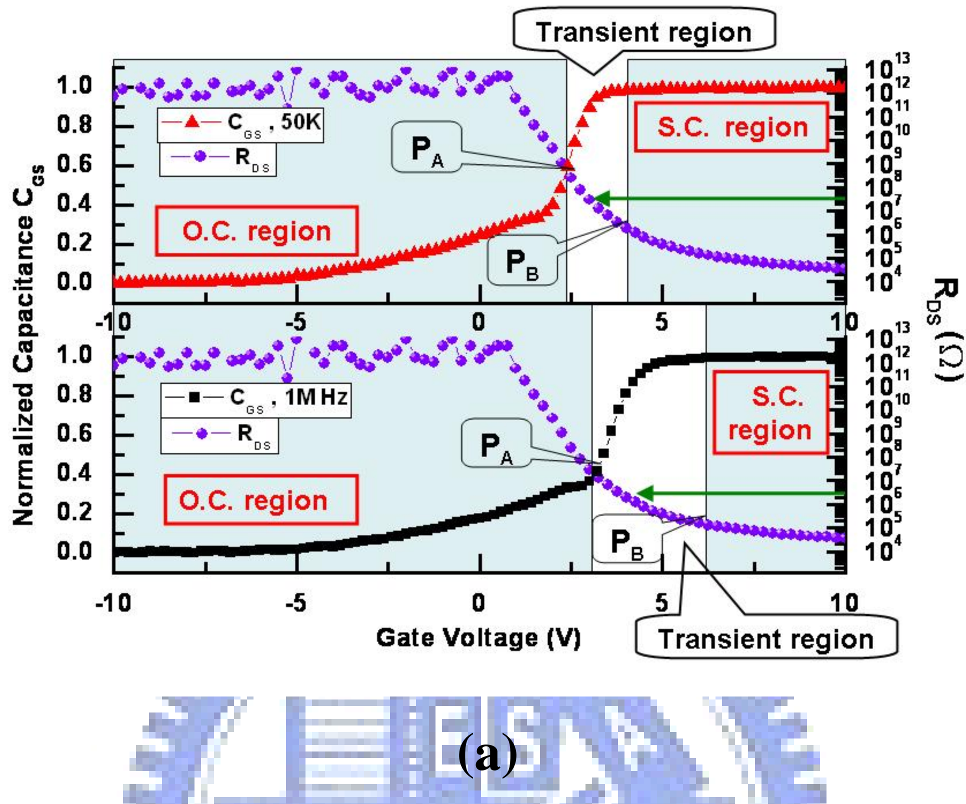


(a)

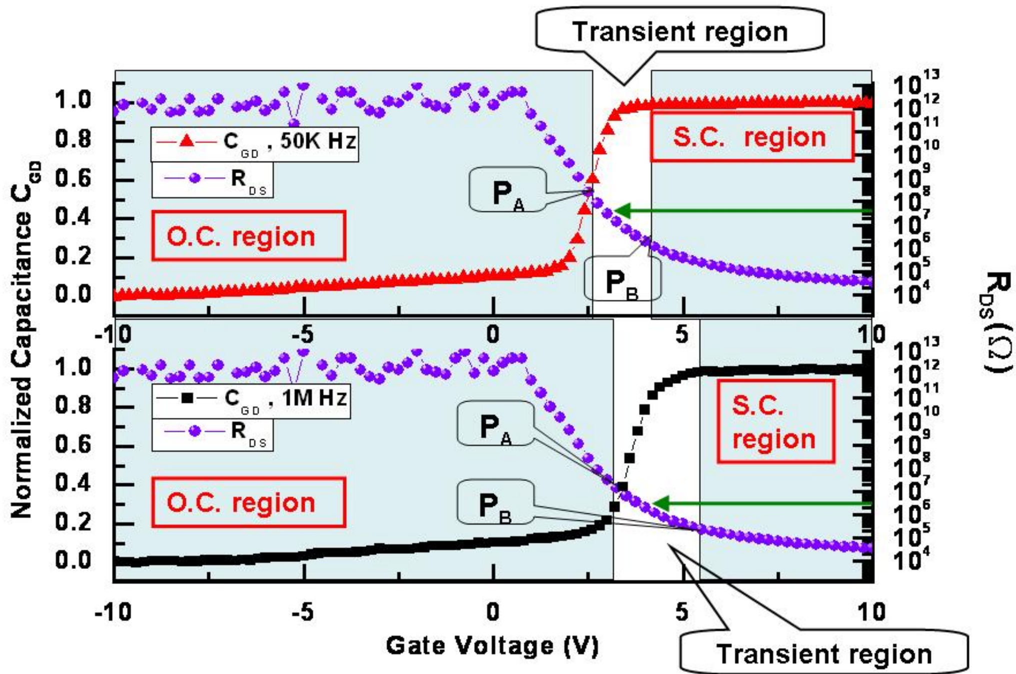


(b)

Figure 4-25 The normalized capacitance curves of (a) C_{GS} and (b) C_{GD} curves for the device before and after self heating stress

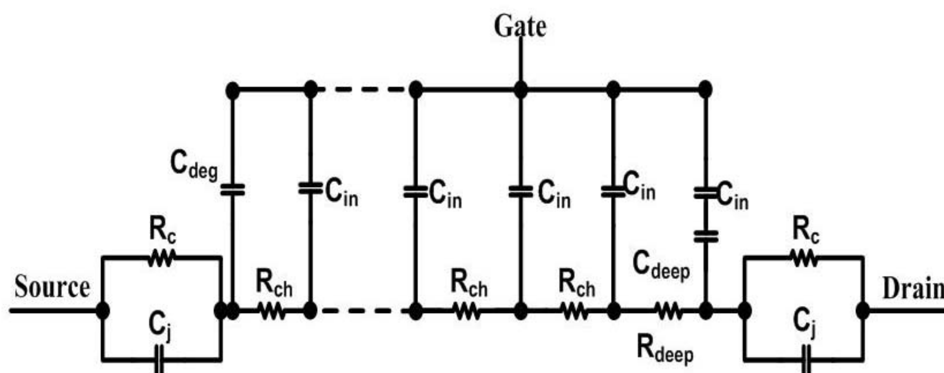


(a)

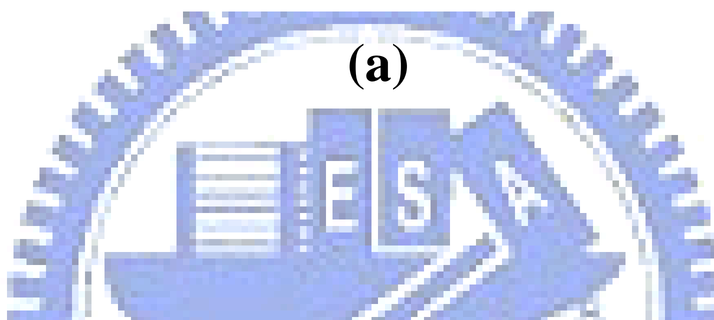


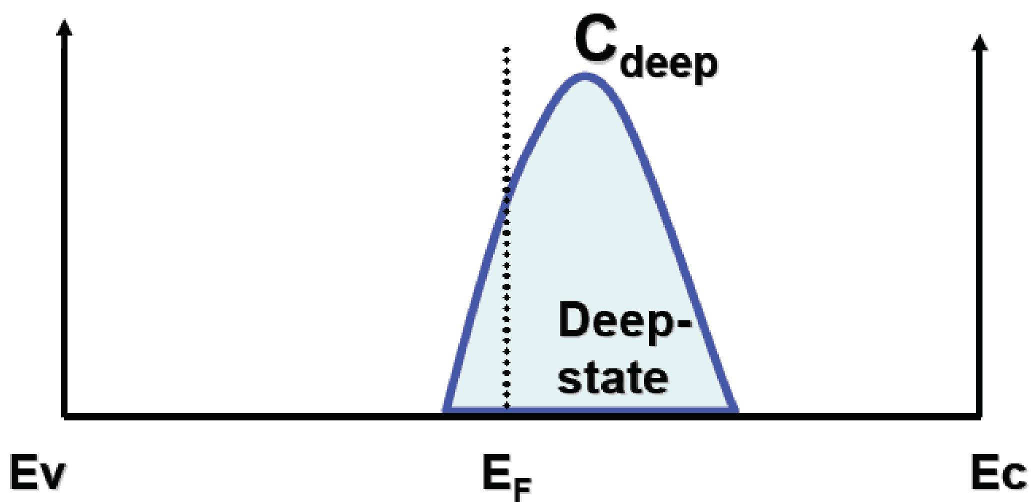
(b)

Figure 4-26 The R_{DS} curves V.S. the (a) C_{GS} and (b) C_{GD} curves for the device after self heating stress

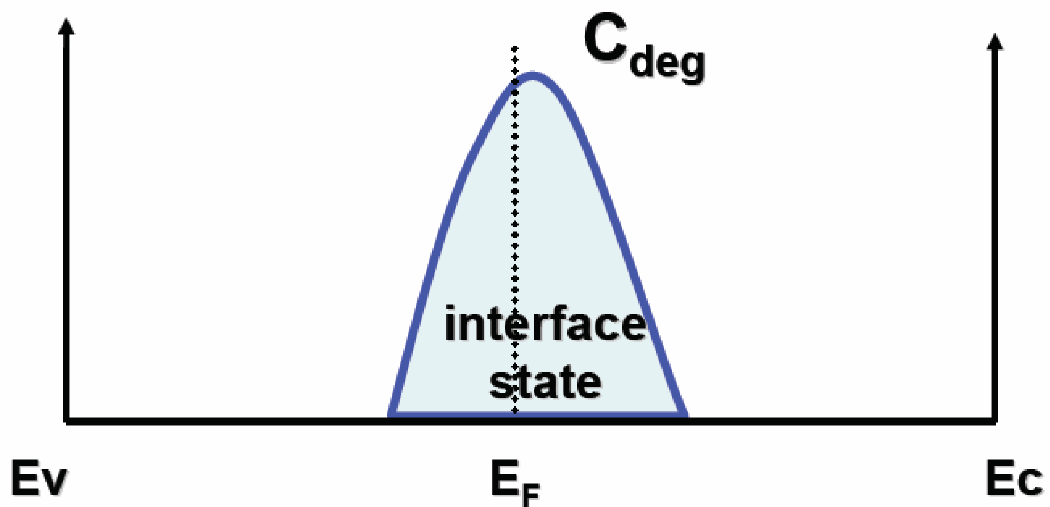


(a)





(b)



(c)

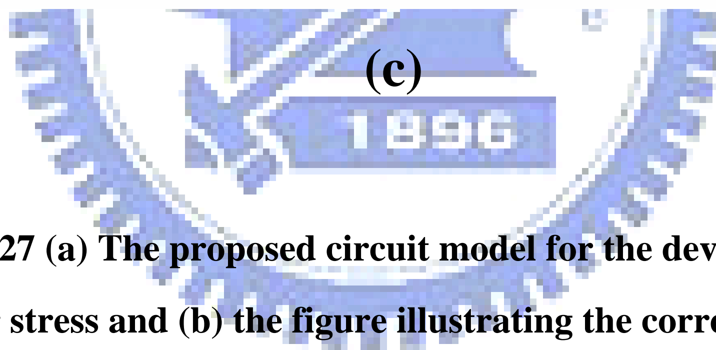


Figure 4-27 (a) The proposed circuit model for the device after hot carrier stress and (b) the figure illustrating the corresponding location of the C_{deep} in the bandgap and (c) the location of the C_{deg} in the bandgap

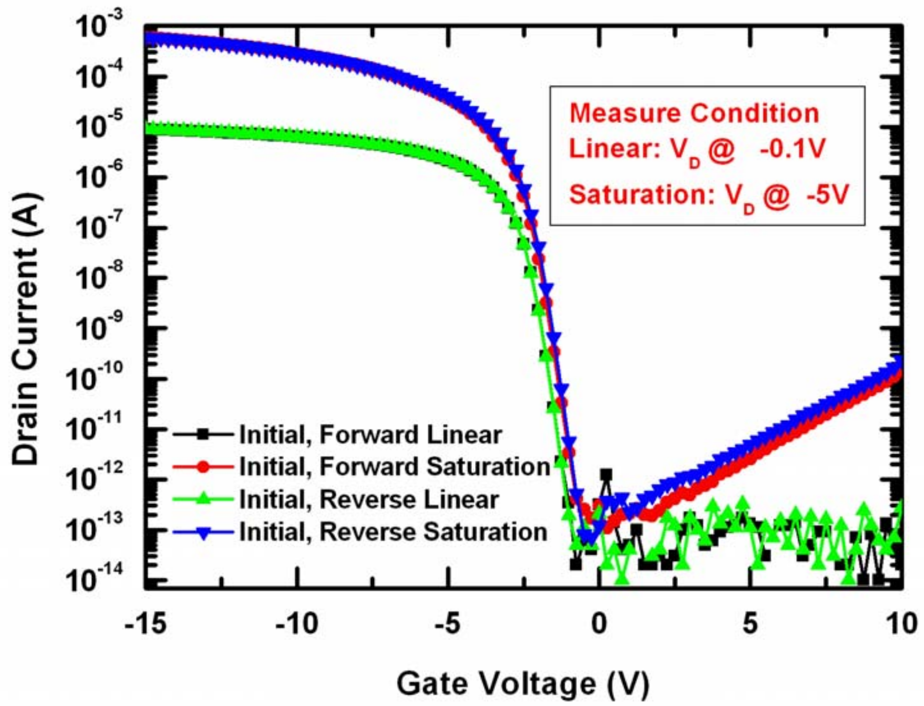


Figure 4-28 The transfer characteristics for the fresh p-type poly-Si TFT

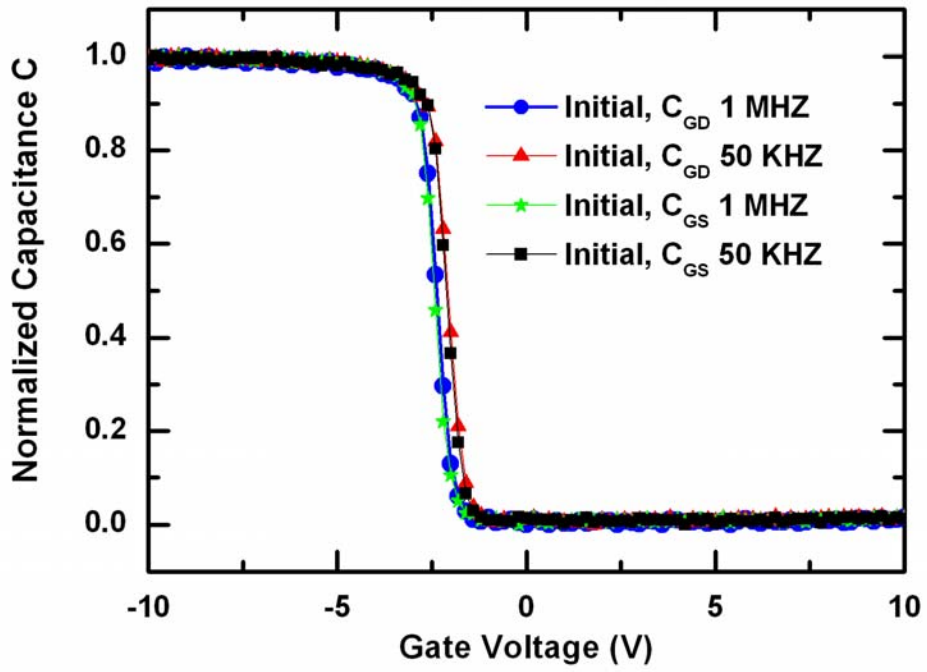


Figure 4-29 The normalized capacitance curves for the fresh p-type device

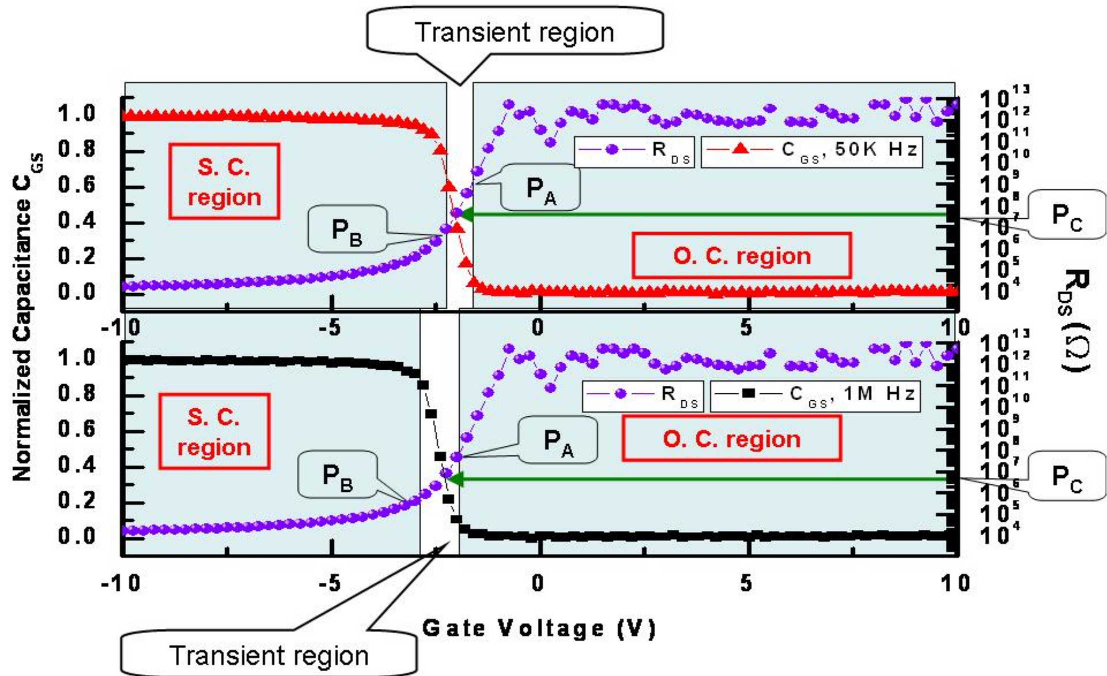


Figure 4-30 The R_{DS} curves V.S. capacitance curves for the fresh p-type device

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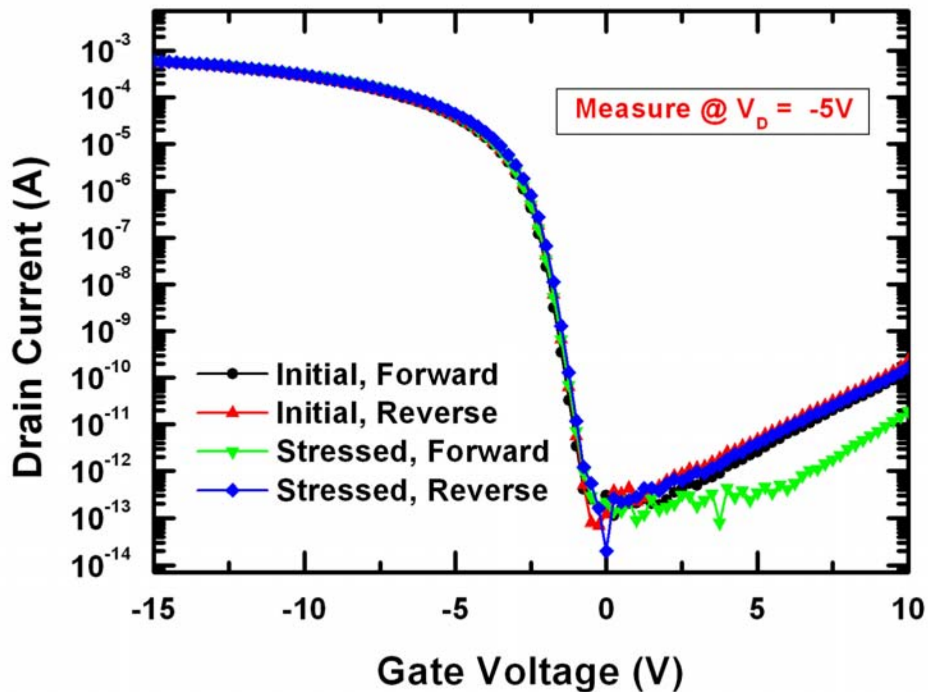
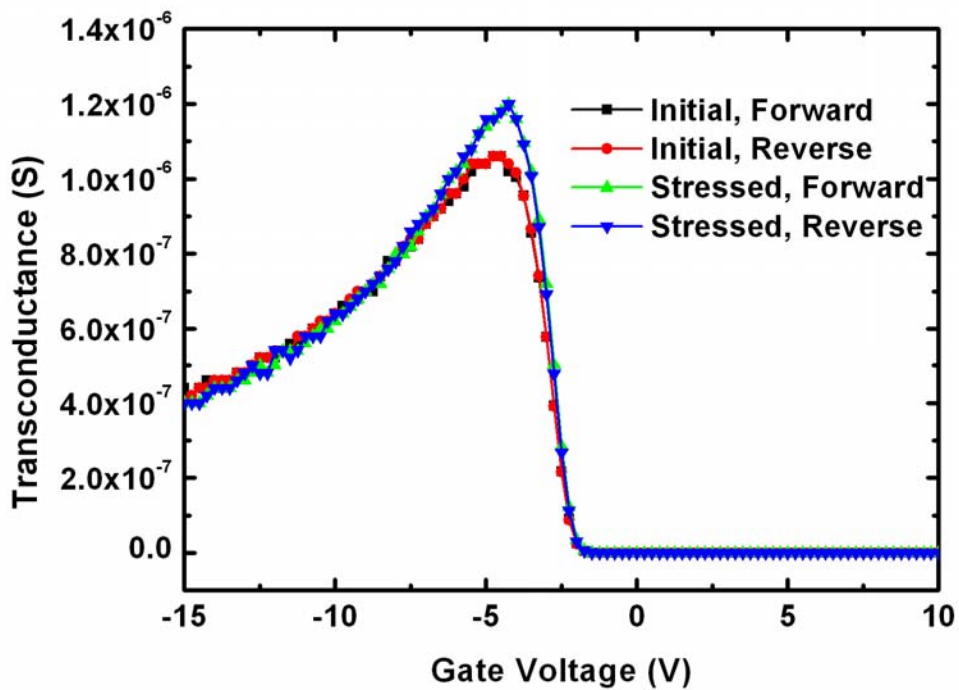
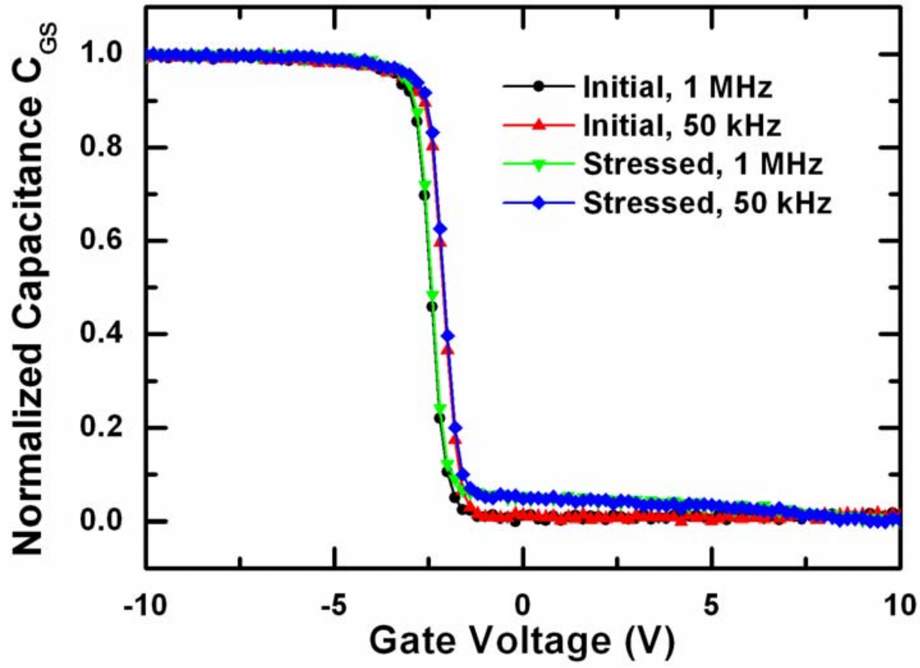


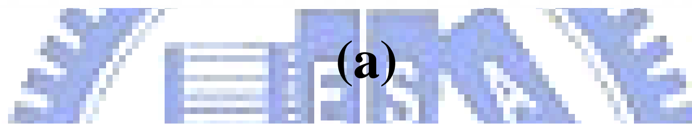
(a)



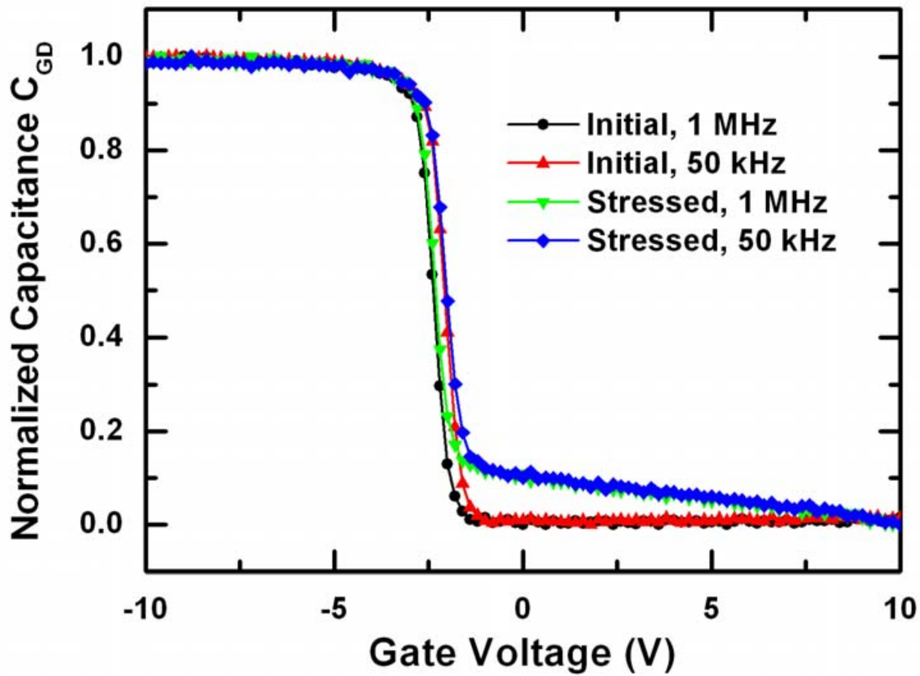
(b)

Figure 4-31 (a) The transfer characteristics and (b) the transconductance curves for the p-type device before and after hot carrier stress



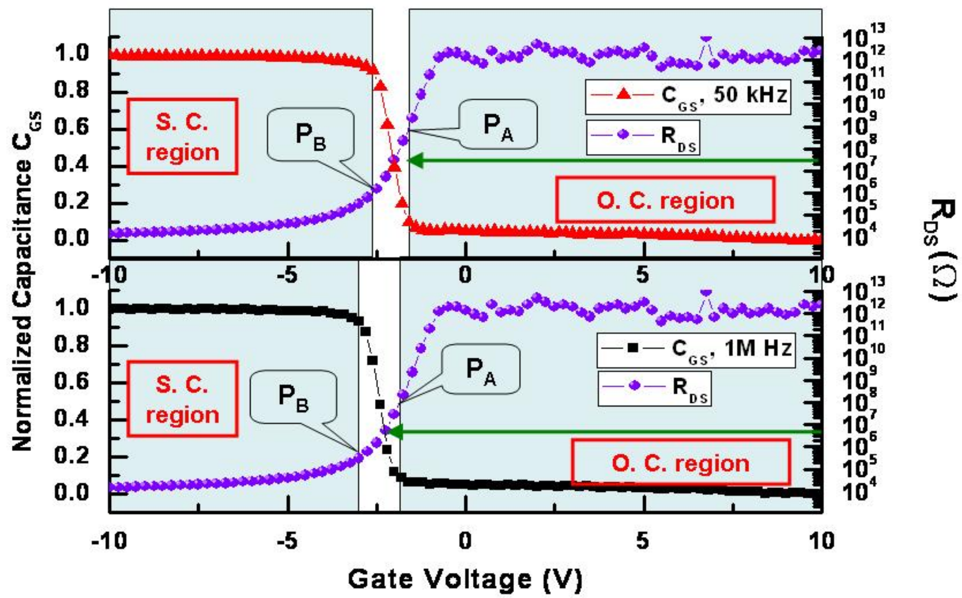


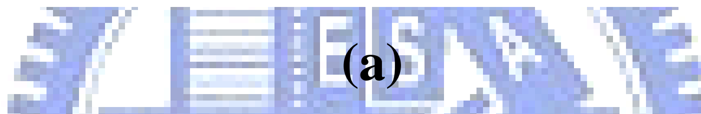
(a)



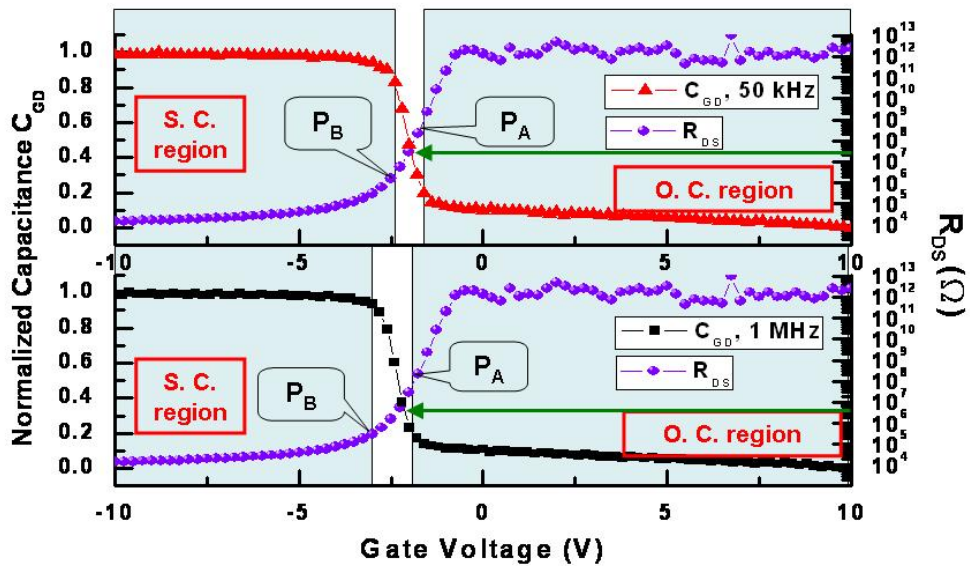
(b)

Figure 4-32 The normalized capacitance curves of (a) C_{GS} and (b) C_{GD} curves for the p-type device before and after hot carrier stress



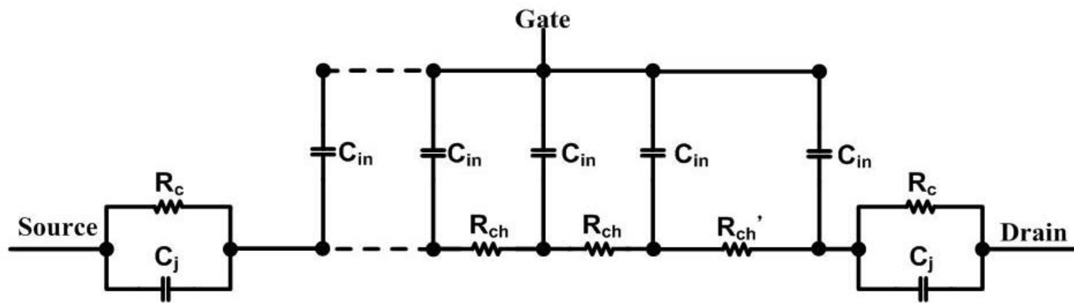


(a)



(b)

Figure 4-33 The R_{DS} curves V.S. the (a) C_{GS} and (b) C_{GD} curves for the p-type device after hot carrier stress



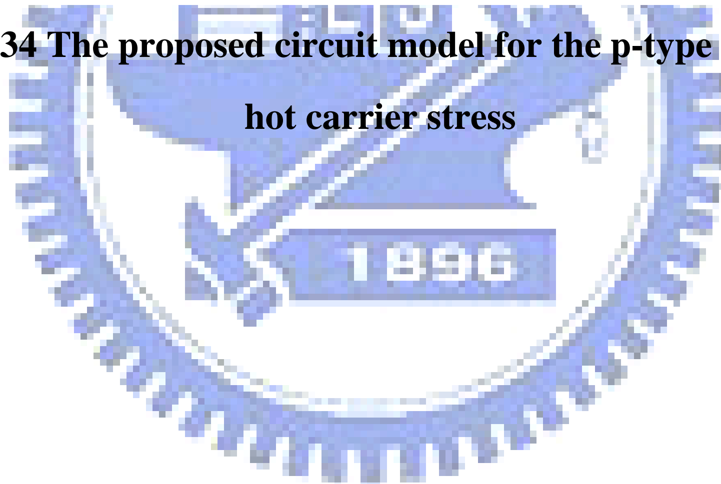


Figure 4-34 The proposed circuit model for the p-type device after hot carrier stress

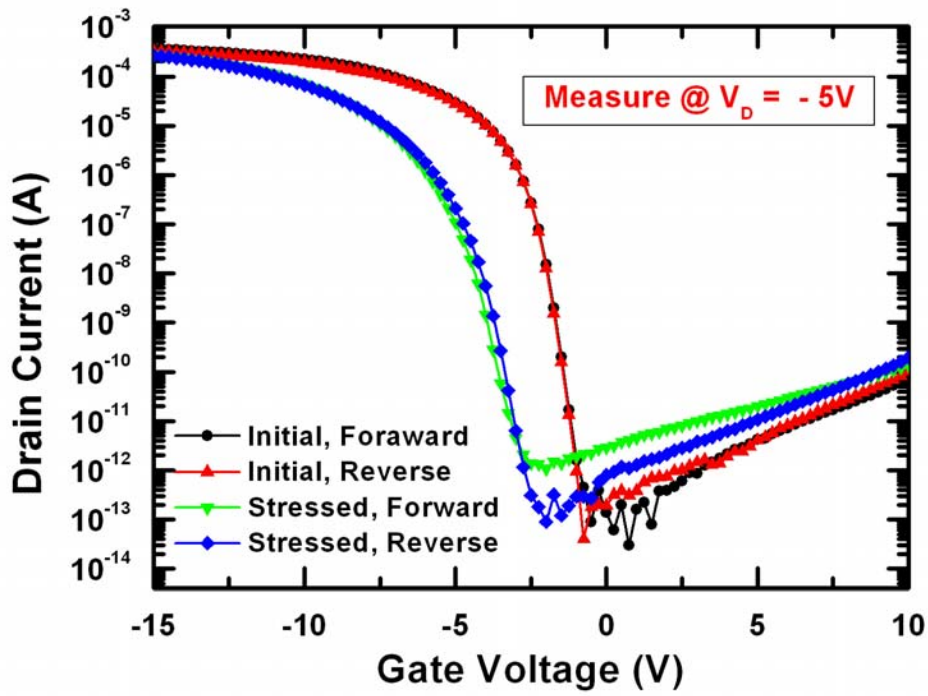
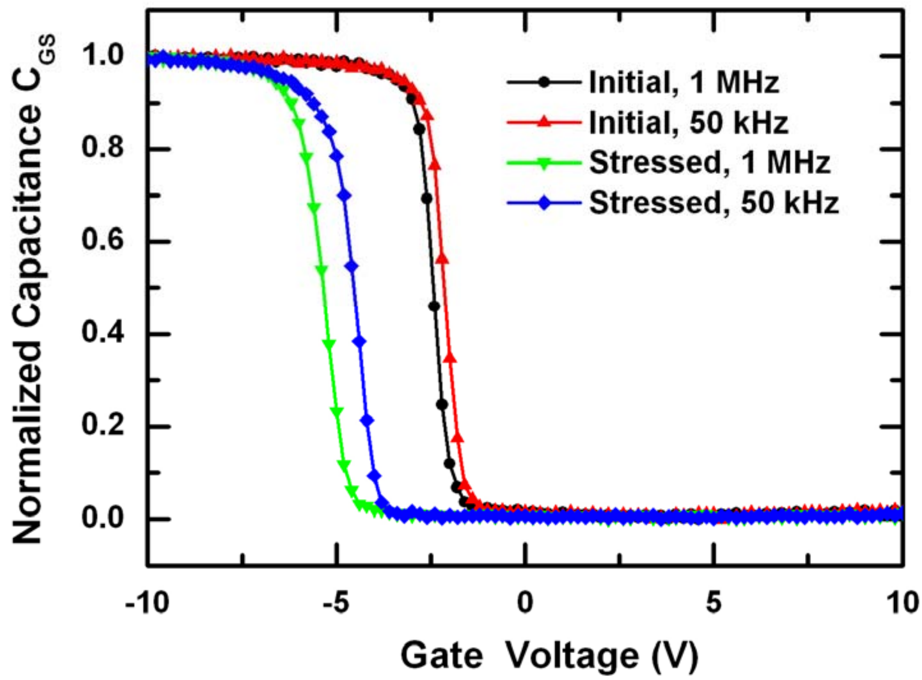
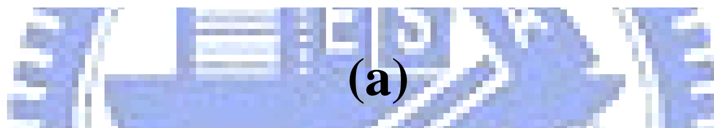
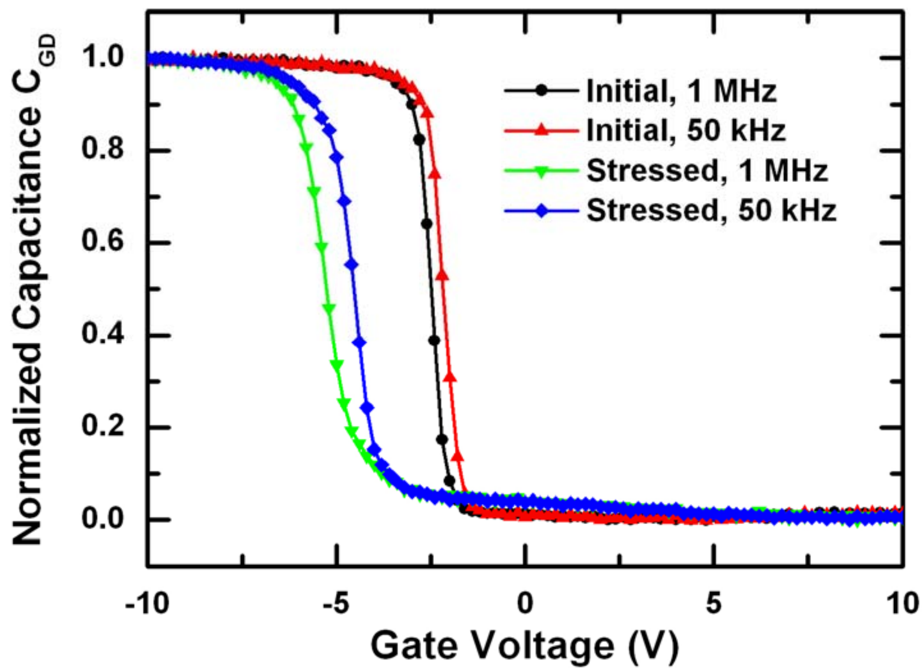


Figure 4-35 The transfer characteristics for the p-type poly-Si TFT before and after self heating stress



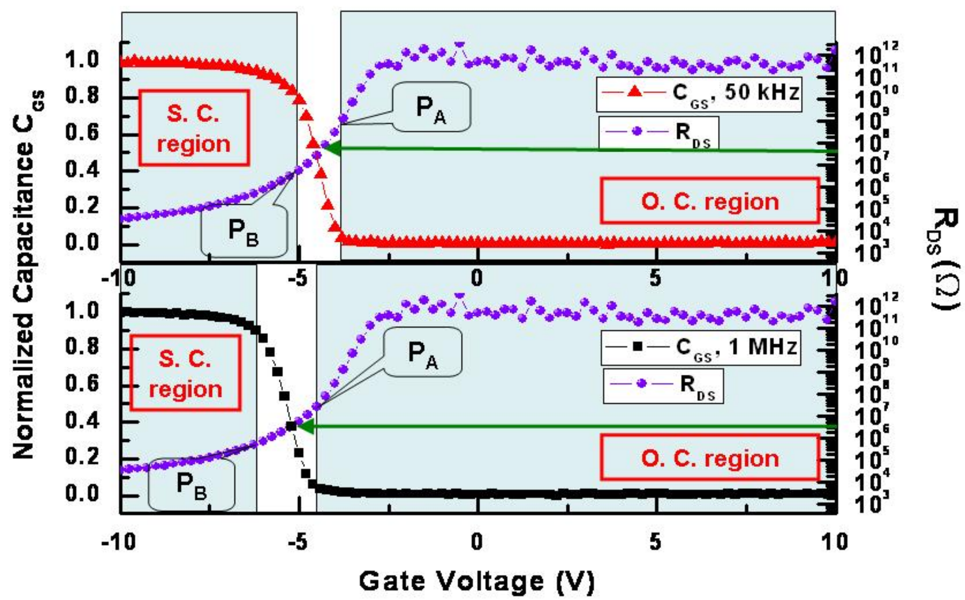


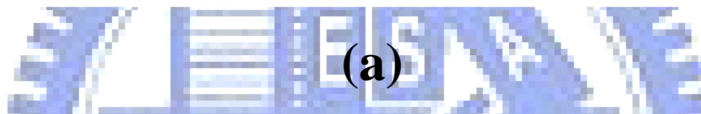
(a)



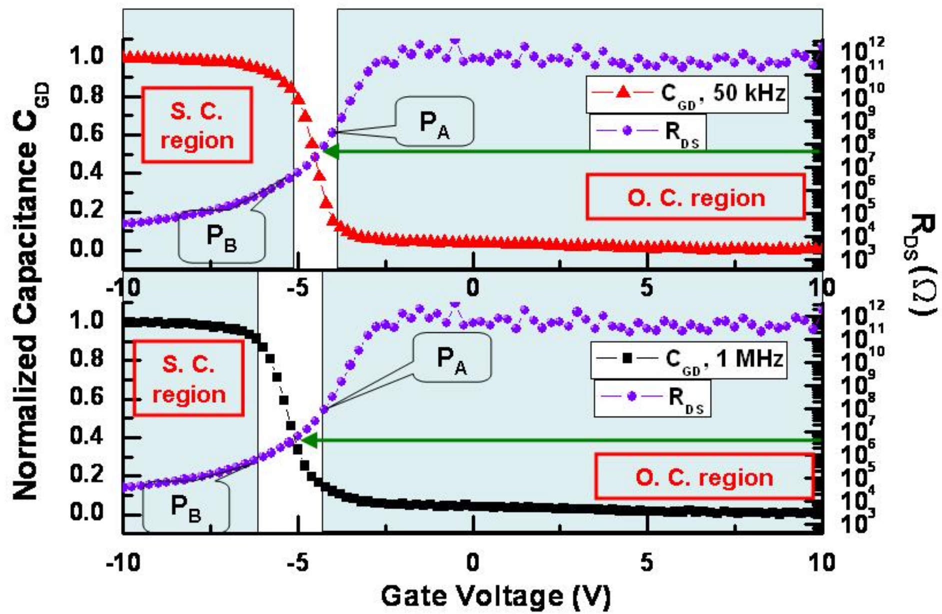
(b)

Figure 4-36 The normalized capacitance curves of (a) C_{GS} and (b) C_{GD} curves for the device before and after self heating stress





(a)



(b)

Figure 4-37 The R_{DS} curves V.S. the (a) C_{GS} and (b) C_{GD} curves for the p-type device after self heating stress

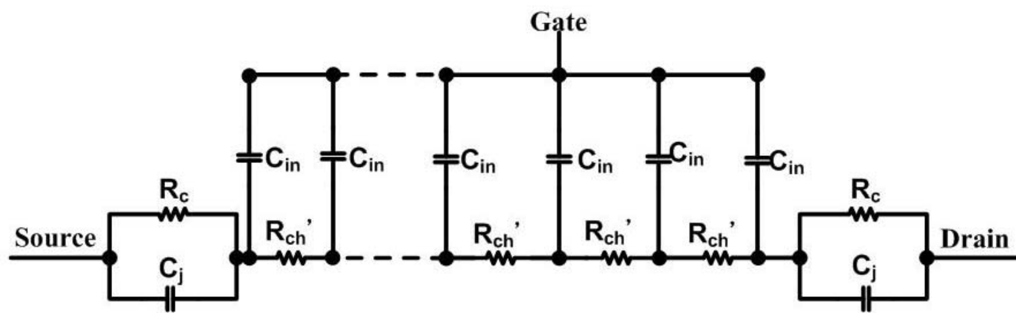


Figure 4-38 The proposed circuit model for the p-type device after self heating stress

Chapter 5

Characterization of Temporal Variation of Poly-Si TFTs: under AC Operation

Preface: In this chapter the reliability behavior of poly-Si TFTs under AC operation is discussed. First the previous papers would be reviewed for the study on the reliability behavior under gate AC operation. Then, we will focus on the behavior under gate AC stress in the OFF region. One motivation for such reliability is the pixel driving for the poly-Si TFTs in the LCD applications, which would be briefly described in section 5.1. The reliability behavior for both n-type and p-type poly-Si TFTs would be studied in section 5.2 and 5.3. Their I-V and C-V behaviors as well as the degradation dependency on the gate pulse parameters, such as level, duty and frequency, would be examined. Then, the similar device circuit model as introduced in chapter 4 would be applied and the voltage drop on each element in the model during operation would be discussed. Based on the discussion, the gated p-i-n device, which has a similar structure to poly-Si TFTs, is introduced. These gated p-i-n devices, manufactured in parallel with the poly-Si TFTs, are DC-stressed and measured. The similarity of the C-V curves between the AC-stressed poly-Si TFTs and DC-stressed gated p-i-n devices indicates the validity of the proposed model. A more detailed discussion of the degradation mechanism and the insights of this finding would also be provided in section 5.5.

5-1 Review and Motivation

Owing to the better crystallinity of the channel region, poly-Si TFTs have the

better driving ability and are expected to form some more advanced applications which the a-Si:H TFTs may not [5-1~5-3]. Take the display system as the example, in which the poly-Si TFTs are mostly applied so far, the poly-Si TFTs are expected to form both the in-pixel switches and the integrated driving circuits. In that case, the devices would face the high-frequency and high-voltage operation. That means the devices could have some kind of Electrical-Over-Stress (EOS) issue. These devices in the pixels could face even tougher conditions if the frame rate gets higher, which means that the allowed time to charge the capacitors is fewer and the driving voltage needs to be higher. If the poly-Si TFTs are to form the integrated circuits, then the device could even need to face more complicated gate and drain pulse signals.

Refer to previous works, there have been studies reported on the reliability issues of the dynamic operation for a-Si:H TFTs and poly-Si TFTs. As for a-Si:H TFTs, the story is relatively simple. Chun-Sung Chiang *et al*. reported that the degradation of the a-Si:H TFT under the gate pulse operation can be modeled with the "effective stress time" and proposed equations to describe the threshold shift for both the positive and negative voltage operation [5-4]. However, the story for the reliability behavior of poly-Si TFTs is more complicated. Yukiharu Uraoka *et al*. reported that the degradation behavior of poly-Si TFTs is closely related to the parameters of the gate pulse.[5-5~5-6] Refer to figure 1, the transfer characteristics for the device after gate dynamic operation with range ± 15 V with the grounded source/drain electrodes shows apparent decrease on the device mobility and the ON current. Also, the device after stress shows increase of the OFF current and almost unchanged sub-threshold region and threshold voltage. They continued to use the emission microscope to further study the explicit degradation and figure 5-2 shows the emission intensity of the device during stress. It can be clearly observed that the emission intensity reaches its maximum when the applied gate pulse moves from positive 15 V to negative 15 V,

namely the period to turn off the device. It was then proposed that the induced channel carriers would react with the silicon bonds as the pulse signal switched from ON to OFF, as shown in figure 5-3. At this time the channel carriers are swept to source and drain junction and the faster change the pulse signal, the higher velocity these carriers would have and hence the worse degradation there could be near the source and drain junction. Similar behaviors are found for the p-type devices under gate pulse toggling between the ON/OFF regions, as shown in figure 5-4. The stress condition is also ± 15 V applied to the gate electrode and the source and drain electrodes are grounded. The device performance actually improves after stress. Increased device mobility as well as the decreased OFF current are observed for the stressed device. They claimed that the similar mechanism takes place for the channel carriers and the correspondingly generated states would be responsible for such degradation.

However, these studies are still far from the real applications since the operation conditions are quite different from the aforementioned ± 15 V condition. Thus, the understanding may be just of limited help to the designers. In this chapter we started from the real applications for the poly-Si TFTs. Refer to figure 5-6, a conventional active matrix TFT-LCD panel consists of the scan-line (row) drivers and the data-line (column) drivers and the respective pixel can be addressed with the specific scan-line and data-line driver in the checker-board pattern. The common driving method is to write the pixels one row at a time. For example, when the signal is to write the n_{TH} row, only the n_{TH} row would be applied with the high voltage to turn on the TFTs in the same row and for the rest of the rows the signal is applied with the low voltage to have them kept in the OFF region. And for the pixels in the n_{TH} row, the data-line driver would apply the signal to the respective data-line such that the pixels would be addressed with the voltage to be charged. After charging the pixels, the n_{TH} row

would be applied low voltage to make the TFTs in each pixel to be in the OFF region and the subsequent row, namely the $n+1_{TH}$ row line, would be applied high voltage to turn on the switch TFTs and then the voltages to be addressed could be charged from the data-line to the respective pixel. In this manner, the sequential rows as well as the pixels can be addressed and charged (or discharged). Within one frame time, the switch TFTs are turned on only for the time when the row is applied with the high voltage and mostly the devices are kept in the OFF region with the data-line toggling in order to charge the pixels on other rows. As the high demand for the increase of the frame rate from 60 Hz to 120 Hz, the switch TFTs are having fewer time to charge the capacitors and some even higher voltages could be applied to charge the pixel in the limited time. This would arise one issue that the OFF region and high voltage drain AC stress could lead to certain kind of degradation. Considering the gate-to-drain voltage drop (V_{GD}) and gate-to-source voltage drop (V_{GS}), it could be more appropriate to study the gate OFF region AC stress with both source and drain grounded as shown in figure 5-7. One point of this analogy is that the reliability of the ± 15 V gate AC pulse was reported while there are very rare studies on the reliability of the OFF region gate AC stress. The understanding from the previous report may provide helpful information for this study. Another point for such study is that the three-level driving, which utilizes the storage-on-previous-gate driving scheme, would have the similar pulse signal applied to the gate electrode, in which the reliability study may also be of great help [5-7]. In the following study, the reliability for both n-type and p-type device under gate AC pulse signal in the OFF region is examined via the I-V and C-V behaviors. Furthermore, the dependence of the degradation on the pulse parameters and the underlying mechanism would be discussed.

5-2 Reliability Behavior under Gate AC stress in the OFF Region: n-type Device

Figure 5-8 shows the current transfer characteristics for the device before and after stress with the measuring drain voltage 0.1 V. The stress condition is that the gate voltage swings between 0 and – 20 V, 500 kHz and the duty cycle is 50 %. The source and drain electrodes are grounded. Refer to the figures, the device after stress shows apparent degradation in the device mobility and the corresponding ON current. The device mobility degrades to around half of the initial value after 1000 second stress. The device also shows small shift in its subthreshold region and the threshold voltage. Such degradation is kind of similar to the results of the hot carrier effect, which is discussed in chapter 4. However, as for the stress condition in this work, the gate voltage is kept all below the device's threshold voltage, which is around 1.7V, and at this time there should be no induced channel carriers formed beneath the gate electrode, not to mention the "hot" electrons and the corresponding impact ionization event. To compare and to gain more information, the current behavior for the device under DC gate OFF region stress is given in figure 5-9 with the measuring drain voltage 0.1 V. The stress condition is that the gate is applied with DC – 20 V and both the source and drain are grounded. As can be seen in the figure, the device after stress shows slight increase of device mobility and the ON current, OFF current as well as the subthreshold region is almost unchanged. The I-V behavior difference between the gate AC stress and DC stress reveals that the dominant mechanism for these two stress conditions could be very different.

In order to study the explicit mechanism, the C-V behaviors are also examined. Figure 5-10 shows the normalized gate-to-drain capacitance C_{GD} curves before and after gate AC stress with different measurement frequencies. Refer to this figure, the

capacitance curves for the stressed device show slight shift for the lower measurement frequency (200 kHz) and for the higher measurement frequency, namely 2 MHz, the capacitance curves show both shift and distortion. In other words, the capacitance behavior after stress shows the frequency-dependent degradation, which in turn indicates that there are some states created during stress. As comparison, the capacitance behavior for the device under gate DC stress is shown in figure 5-11. Only slight shift for the capacitance curves of the stressed device can be observed. Once again, from the capacitance curves it is shown that the degradation behaviors for the device under gate AC and DC stress in the OFF region are very different, and this also unveils that the dominant mechanism beneath could also vary from each other.

Some pulse parameters of the applied signal are examined to find the dependence of them in order to find the more explicit mechanism of the degradation behavior. Figure 5-12 to 5-14 show the mobility degradation with respect to different gate pulse parameters, namely, the gate pulse level, the frequency and the duty cycle of the gate AC pulse. For all these three stress conditions, the source and drain electrodes are all grounded and the gate electrode are applied with the AC signal in the OFF region. Figure 5-12 (a) shows the dependence of the pulse range with the grids of the figure in linear scale, while figure 5-12 (b) is in the logarithmic scale. Refer to the figure, the mobility degradation shows apparent dependence on the voltage range of the applied gate pulse. For the gate AC voltage swinging between 0 and – 15 V, the mobility shows very slight degradation even as the stress time reaches 1000 seconds. However, as the swing range increases, the mobility shows obvious degradation. For the swinging range 0 to -22.5 V, the mobility is only around 35 % of its initial value as the stress time reaches 1000 seconds. Besides, the curves does not saturate as the stress time increases. Figure 5-13 shows the mobility degradation for the device under gate AC pulse operation in the OFF region with the swinging range 0 to – 20 V. As

can be observed, the device degradation is dependent on the applied signal frequency. For the three applied frequencies, the degradation behaviors show the similar trend. The higher the frequency of the applied signal, the worse the device degradation. Figure 5-14 gives the behavior of the device degradation for the device under different duty cycles of the applied gate signal. In this figure, the applied voltage is also 0 to – 20 V and it is found that the degradation shows the dependence on the duty cycle of the applied signal. The degradation is worse for the duty cycle of 10 % and eased for the larger duty cycle, which in other words means that the degradation is more serious if the applied gate signal stays in the V_{GD} equals to – 20 V for the longer time.

Though it is found that the degradation is worse for the signal comes with larger gate pulse range, higher frequency and smaller duty cycle value, still so far we can not find the reason for such degradation since there should be no channel carriers formed with the gate AC signal applied all in the OFF region. In the following section, the degradation of the p-type device under gate AC operation in the OFF region is also studied and presented. It is hoped that the result from the study of the p-type device under AC operation could help us to find the clear mechanism for such operation.

5-3 Reliability Behavior under Gate AC stress in the OFF Region: p-type Device

Figure 5-15 shows the transfer characteristic curves for the p-type poly-Si TFT before and after stress. The stress condition is that the gate AC signal toggles between 0 and 20 V with the duty ratio 50 % at 500 kHz and the source and drain electrodes are grounded. Refer to this figure, the transfer behavior of the device after stress shows improved device performance such as the increased mobility, decreased leakage current and shifted V_{TH} in the positive direction. Such performance

improvement is just similar to the effect of channel shortening as described in chapter4. However, in this case, during stress there should be no channel carriers since the applied gate voltage is toggling all in the OFF region. In comparison, the transfer behavior of the p-type poly-Si TFTs under DC operation in the OFF region is given in figure 5-16. The stress condition is that the stress gate voltage is DC 20 V and the source and drain electrodes are grounded. The transfer curves as well as the transconductance curves for the device after such stress show slight V_{TH} shift in the positive direction. However, the mobility and leakage behavior after stress show almost identical behavior as compared to the fresh device, which is very different from figure 5-15. This may reveal that the dominant mechanism for p-type poly-Si TFT under gate AC in the OFF region could be very different from that under gate DC stress.

In order to find a more explicit understanding of the dominant mechanism, the corresponding capacitance behaviors are measured. Figure 5-17 shows the normalized capacitance curves of the device under gate AC stress, while figure 5-18 shows that under gate DC stress. As for figure 5-17, the capacitance curves show apparent increase for the gate voltage still in the OFF region and this increase is independent of the measurement frequency, which is just similar to the behaviors shown in section 4-3. On the other hand, as shown in figure 5-18 the C-V curves for the device after gate DC stress show only slight V_{FB} shift as compared to the C-V curves of the fresh device. This reveals that, once again, the degradation behaviors for the device under gate AC and DC stress in the OFF region are very different.

Figure 5-19 (a) shows the mobility increase of the p-type poly-Si TFTs under gate AC for the figure in linear scale while figure 5-19 (b) shows that in the logarithmic scale. As shown in figure 5-19, the mobility increase of the device after AC stress also shows the power-law time dependence as in the case of DC hot carrier

stress [5-8], and such mobility increase can be as high as 30% when the operation time reaches 1000 seconds. In addition, such increase apparently depends on the applied gate voltage, though the applied voltages all fall in the OFF region. Though the mechanism is still unknown for the degradation for both n-type and p-type device, such dependence on the swinging range for the applied gate pulse in the OFF region may be similar. Figure 5-20 shows the mobility degradation ratio for the device under gate dynamic stress 0~ +20 V with different stress frequencies, while figure 5-21 shows the degradation for the gate pulse with different duty ratios. Refer to figure 5-20, it can be observed that the mobility degradation shows no apparent dependency on the applied gate pulse frequency, which is much different from that in the n-type devices. On the other hand, for the dependency on the duty ratio of the gate pulse, the device degradation also shows large mobility difference for the duty ratio 10% and 50 %, in which the gate pulse with larger duty ratio comes the larger device mobility difference. However, for the duty ratio 50% and 90%, the degradation shows no apparent dependency where the mobility difference for these duty ratios somehow overlaps for the stress time larger than 150 seconds. This reveals that the underlying mechanism may be independent on the duty ratio of the gate pulse. In other words, the degradation is dependent on the applied voltage range, and independent on the pulse frequencies and duty ratio values.

5-4 Comparison and Discussion

So far we have studied the degradation behaviors for the device under gate AC dynamic operation in the OFF region and their dependence on the gate pulse parameters, which are summarized in table 5-1. In brief, the degradation for the n-type poly-Si TFTs under such operation results in the decrease of mobility and ON current as well as the shift and distortion in the capacitance behavior. The degradation is

worse for the gate pulse with larger range, higher frequency and smaller duty ratio. On the other hand, the degradation in the p-type poly-Si TFTs leads to the increase of device mobility, correspondingly the increase of ON current. Also, the device shows the anomalous increase of the capacitance for the gate voltage lower than the flat band voltage and such increase is independent of the measuring frequency. The degradation is larger for the larger voltage swinging range but different from n-type devices, the mobility change shows the independence of the frequency and the duty ratio. And, the most obvious difference is, the operation makes the mobility decreased for the n-type device, while in the p-type devices the mobility actually increases after stress.

So how could we explain such degradation? Since the swinging voltage all stays below the threshold voltage, in such stress condition there should be no channel carriers formed and thus such degradation behavior may not be explained by Uraoka's model [5-5]. In the following discussion we resort to the similar model to the one we had discussed in chapter 4, as shown in figure 5-22. Cin, Rch, Cj and R_C represent the gate insulator capacitance, the channel resistance and the source/drain junction capacitance and contact resistance, respectively. The impedance between gate and source/drain can be expressed by $Z= Rch+(1/j2\pi fCin)$, where f represents the operation frequency. Under DC and low frequency operations, the impedance is dominated by the capacitance term and the applied gate voltage would mainly drop across the gate insulator. For high frequency AC operations, the capacitance term becomes smaller and both the capacitance and resistance terms should be considered. Nevertheless, for the OFF region AC operation, there is no induced channel formed, making the channel resistance become relatively large and possibly even become the dominant term in the impedance. Back to this work, the source and drain electrodes are grounded and the pulse signal toggling in the OFF region is applied from gate, the voltage drop would mainly occur across Rch and the diodes and therefore such large

voltage drop on the diodes or the channel resistance could lead to the degradation.

However, such assumption is difficult to verify because the voltage drop in the channel can hardly be probed. Theoretically we need to use the measuring equipments with very large impedance to probe the channel voltage in order not to interfere the channel voltage distribution during stress, and thus such approach may not be feasible. Therefore, in this work, the gated p-i-n device is adopted, where one side of the source/drain doping in fabricating n-type TFT is changed from n- and n+ to p+. The cross section view and an equivalent band diagram of the gated p-i-n device are shown in figure 5-23. Laterally, the device consists of the p+ region, the intrinsic region and the n-/n+ region, which is just similar to the p-i-n diodes used in the optoelectronic sensors [5-9]. In addition, there are the dielectric films and the metal gate above the intrinsic layer, making the device different from the conventional p-i-n diodes and instead making the device similar to the structure of TFTs. Therefore, the structure with the gate above enlightens us of the name, "gated p-i-n device," which can also suggest readers to differentiate it from the conventional p-i-n diodes. The feature for adopting such gated p-i-n device is that this device has the similar structure to the TFTs while the channel voltage can be set from one side of the electrodes. Thus, this enables us the capability of forming large electric field over one junction to simulate the condition of gate AC OFF region stress for poly-Si TFTs. Then, by examining the capacitance curves of the TFTs and gated p-i-n devices after stress, the aforementioned mechanism can be verified.

Figure 5-24 shows how we made the n-side junction in the reverse-bias for the gated p-i-n device to verify our assumption for the n-type poly-Si TFT under gate AC operation in the OFF region. The gated p-i-n device is DC-stressed for 200 seconds with voltage of the gate electrode, the p-side electrode, and the n-side electrode set to -20V, -5V, and 20V, respectively. The biases are chosen such that the large electric

field would occur at the N-side junction while the P-side junction would occupy only small part of the lateral voltage difference V_{NP}. In this case, the voltage mainly occurs at the N-side junction, and if the DC-stressed behavior for the gated p-i-n device resembles the degradation behavior of the gate AC-stressed TFT, then it can thus be inferred that the degradation can be attributed to the largely-biased junction. Figure 5-25 shows the normalized gate-to-n-side capacitance C_{GN} curve for the gated p-i-n device before and after stress. For the C_{GN} curves before and after stress, it can be observed that after stress the C_{GN} curve shows similar behavior to the n-type TFT after gate AC stress, in which the C-V curve measured with the lower frequency shows the slight shift while the curve with the higher measuring frequency shows both shift and distortion. The similarity of the capacitance curves between the stressed TFT and gated p-i-n device reveals the verification of the proposed mechanism.

Figure 5-26 shows the similar method to verify our assumption for the p-type poly-Si TFTs. The stress condition is that the stress gate voltage, N-side voltage and the P-side voltage are 15 V, 10 V and -15 V. During such stress condition, based on the similar idea discussed, the lateral voltage difference V_{NP} would mainly occur at the P-side junction. Figure 5-27 gives the normalized gate-to-p-side capacitance C_{GP} before and after 200 second DC stress. Refer to the figure, the C_{GP} curves after stress show the apparent increase for the gate voltage in the OFF region and this increase is independent of the measuring frequency, which is just similar to the curves for the gate AC-stressed TFTs as shown in figure 5-17. The similarity between the C_{GD} and C_{GP} curves for the AC-stressed TFT and DC-stressed gated p-i-n device indicates the validation of the proposed mechanism. On the other hand, as for the gate DC stress in the OFF region, as shown in figure 5-9, 5-11, 5-16 and 5-18, based on the proposed model the V_{TH} and C-V curve shift could also be explained by the trapped electrons uniformly in the gate dielectric layer and not confined near the source and drain

region because the voltage drop would mainly occur at the capacitors in the proposed distributed circuit model. Thus, based on the model in brief the difference for the degradation mechanism under gate DC and AC stress can be attributed to voltage drop on the different elements and correspondingly different behaviors for the elements under the high voltage applied upon.

So far we have found that the dominant degradation mechanism for the device under gate AC operation in the OFF region is the junction under large electric field. And back to table 5-1, the dependence for the gate pulse can all be explained by the proposed model: the worse degradation is found to occur for the larger level, higher frequency and smaller duty ratio and this can all be attributed to the higher voltage difference on the junctions. There is still one question left: how is such operation condition having different effects on the n-type and p-type devices? The explanation is given as follows: for n-type devices, as shown in figure 5-10, the dispersion behavior of the C-V curves indicates that the state creation may be the main signature of the degradation and this can be attributed to the avalanche behavior at the junction. A thermally-activated electron in the depletion region flows from p-side to n-side. Since the junction is largely reverse-biased, the electron could get sufficient high energy and have collision with the silicon bonds, generating electron-hole pairs. The collision may continue for the following electrons and avalanche may occur in the depletion region, generating significantly large number of electrons and holes as well as leaving states in the depletion region, just as shown in the left side of figure 5-28. Since the generated electrons or holes could in turn gain enough high energy and then have collision with the silicon bonds, the degradation could be even worse with longer stress time and the mechanism itself has no stopping mechanism in it and hence the degradation could fall in a vicious circle.

However, for the p-type device, the device degradation shows similar behavior to

that after DC hot carrier stress, which is proven to be attributed to the locally trapped-charges in the gate dielectric. As in this case, though there are no impact ionization events to provide the electrons, they may still come from the largely reversed-biased junction as shown in the right side of figure 5-28. These electrons, come from the leakage current in the source/drain junction, flow to the channel region and may be attracted by the gate voltage. They may in turn flow towards the gate dielectric and eventually get trapped in the dielectric layer. Since these electrons come from the source and drain junctions, they should as well get trapped in the dielectric layer near the source and drain junction, resulting in the similar behavior to the channel shortening behavior as described in chapter 4. Though for the not-so-largely reverse-biased junction there could still be the electrons leaked through the junction, they may not move towards the gate dielectric if the applied gate voltage is not large. These trapped electrons could help ease the potential distribution near the source/drain junction, which would then decrease the probability for the electrons to get leaked from the junction and trapped in the dielectric layer. As more electrons get trapped in the dielectric layer, the potential is smoother and it would be more difficult for the following electrons to get leaked and then trapped in the gate dielectric. Therefore, the mobility degradation would get slower as time elapsed and could eventually saturate, as shown in figure 5-19 (a). The finding as well as the mechanism for the device under gate dynamic operation in the OFF region should provide valuable information for the designers in designing the high performance and complicated circuit functions composed of poly-Si TFTs.

Since now the degradation for the poly-Si TFT under gate AC stress in the OFF region is found to be caused by the largely reversed-biased junction, it would be of practical interest to compare the degradation behavior with other stress conditions whose degradation also come from the junctions with large electric field. The first

condition one may think about is the DC hot carrier effect as discussed in chapter 4. Figure 5-29 and 5-30 give the I-V and C-V behaviors for the n-type device before and after DC hot carrier stress. The stress condition is the gate voltage V_{GS} is 3 V and drain voltage is 15 V and the stress duration is 200 seconds. The I-V curves are the behaviors in the reverse connection with the measuring drain voltage equals to 5 V. Referred to the figures, it can be observed that the degradation behavior is similar to but much worse than the gate AC-stressed device in the OFF region as shown in figure 5-8, where after 1000 second stress the mobility falls to around half of the initial value for the stress gate voltage ranging between 0 V and – 20 V. As for the DC hot carrier stress, the mobility drops to only about 10% of the initial value as the stress duration is only 200 seconds. The C-V curves for the device after hot carrier stress also show worse degradation as compared to those in gate AC stress. On the other hand, the I-V and C-V behaviors for the p-type device after DC hot carrier stress are shown in figure 5-31 and 5-32. The stress condition is that the gate voltage is -3 V and the drain voltage is -20 V and the time duration is 200 seconds. Comparing figure 5-31 and 5-32 with figure 5-15 and 5-17, it is discovered that for p-type device the behavior and the degree of degradation is almost the same between the DC hot carrier stress and the gate AC stress in the OFF region. On the differences between the DC hot carrier stress and the AC gate stress, one big point is that for the DC hot carrier stress the carriers come from the induced carrier and thus the number of carrier should be greatly larger than the leaked carriers for the gate AC stress in the OFF region. It can thus be inferred that the degradation after DC hot carrier stress would be worse than that after gate AC stress in the OFF region.

It should then of interest that what if the device is stressed only with the large DC drain voltage in the OFF region. In this case the large electric field should be on the drain side only and the carrier source is the leakage current in the junction as well,

which can be more similar to the case under gate AC stress in the OFF region. Figure 5-33 and 5-34 show the I-V and C-V degradation behavior for the n-type device after drain DC stress. The stress condition is gate voltage is -5 V and the drain voltage is 20 V and the duration is 200 seconds. Before this study, it would be surprising that the device under such stress condition shows similar degradation behavior to that under gate AC stress in the OFF region and therefore similar to that under DC hot carrier stress since there should be no channel carriers. However, from the discussion given in this chapter, it is found that the leaked carriers through the junctions under large electric field would show the similar behavior to the hot carrier and the difference is just the degree of degradation. Figure 5-35 and 5-36 show the I-V and C-V curves for the p-type device before and after drain DC stress. The stress condition is that the gate voltage is 5 V and the drain voltage is -20 V. Similar degradation behaviors for both the I-V and C-V are observed as compared with the previous two stress conditions.

So we have discussed the case that the large electric field across the junction could lead to the degradation whether the carrier source is the leakage current or the DC turned-on current. There is still another one case to be discussed. Uraoka *et al.* studied and reported the degradation behavior for the device under gate AC stress toggling between ON/OFF. [5-5~5-6] It is discovered that during the rising/falling time of the gate signal the inverted channel carriers would rushing to the source and drain junction because of the electric field. In this case the carrier source is the channel carriers swept to the junctions when the gate pulse is to turn off the device. Figure 5-37 and 5-38 show the I-V and C-V behaviors for the n-type device after gate AC stress toggling between ON/OFF. The stress condition is that the gate voltage swings between + 15 V and – 15 V with the source and drain electrode grounded. The time duration is 200 seconds. The stressed I-V and C-V behaviors are found to be very similar to the previous three stress conditions. As for the p-type device, similar

study had been done. Figure 5-39 and 5-40 give the degradation behavior for the p-type device after gate AC stress. The stress condition is also that the gate voltage swings between + 15 V and – 15 V and duration is also 200 seconds. The behavior is also found to resemble to the previous three stress conditions discussed in this section. To summarize, figure 5-8, 5-29, 5-33, 5-37 show similar I-V degradation behavior for the n-type device under various stress conditions, while figure 5-15, 5-31, 5-35, 5-39 show those for the p-type devices. There C-V behaviors also resemble to each other. Thus, no matter what the carrier source may be the inversion channel carriers, the leakage current or even the inversion channel carriers swept because the gate pulse is to be turned-off, once the large electric filed is across the junction, the carriers would more or less become the hot carrier and result in the similar degradation behavior. In other words, they can be categorized as the "generalized hot carrier effect." Figure 5-41 shows the mobility degradation ratio under various stress condition for the n-type device. Generally, the degradation behaviors show similar trend with stress time. It can be observed that the degradation is worst for the ON region DC hot carrier stress. This can be attributed to the larger amount of channel carriers flowing in the channel and thus the chance to become hot carriers is higher. The degradation under ON/OFF gate AC stress and OFF region drain DC stress is about the same, and is worse than the OFF region gate AC stress. Figure 5-42 shows the degradation behavior under different stress conditions for the p-type device. The behaviors show no apparent difference from each other and this can be attributed to the electron-trapping in the gate dielectric film. This finding of the degradation behavior under different stress condition would be of great help in evaluating and estimating the device reliability. Some drain engineering techniques, such as the profiling and designing of the LDD region may be adopted to reinforce the device reliability.

5-5 Summaries

In this chapter the degradation mechanism of the poly-Si TFTs under gate dynamic operation in the OFF region is studied with the help of the proposed test structure, gated p-i-n device. The largely reverse-biased source and drain junctions are found to be the root cause of such degradation and the degradation has different effect on the n-type and p-type devices. This study as well as the understanding of the degradation behavior would be beneficial for circuit designers in designing the complicated circuits consisting poly-Si TFTs with the gate pulse toggling in the OFF region. One insight that can be enlightened from this understanding is that if the operation for the key device would be staying in the OFF region with the gate pulse toggling below its threshold voltage, certain kind of drain engineering, such as the adjustment of the doping profile and length of the LDD region, should be considered to reinforce the reliability of the source and drain junction. To summarize, along with the similar model proposed in chapter 4 and 5, the degradation mechanism can be studied and traced down to the key component to facilitate the study of the degradation behavior. This should be useful in the evaluation of device performance and also the development of devices with better reliability.

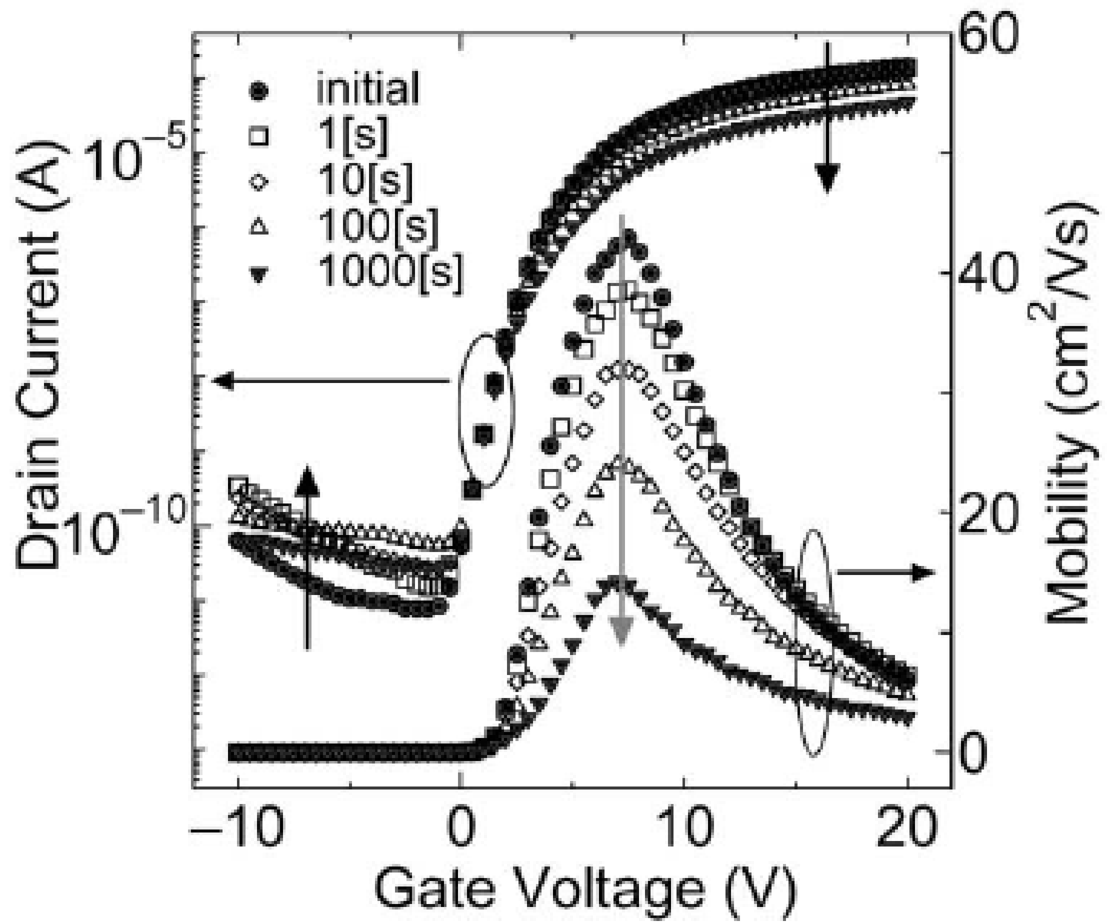


Figure 5-1 Transfer characteristics and device mobility for the n-type device under the gate dynamic stress ranging between + 15 V and – 15 V

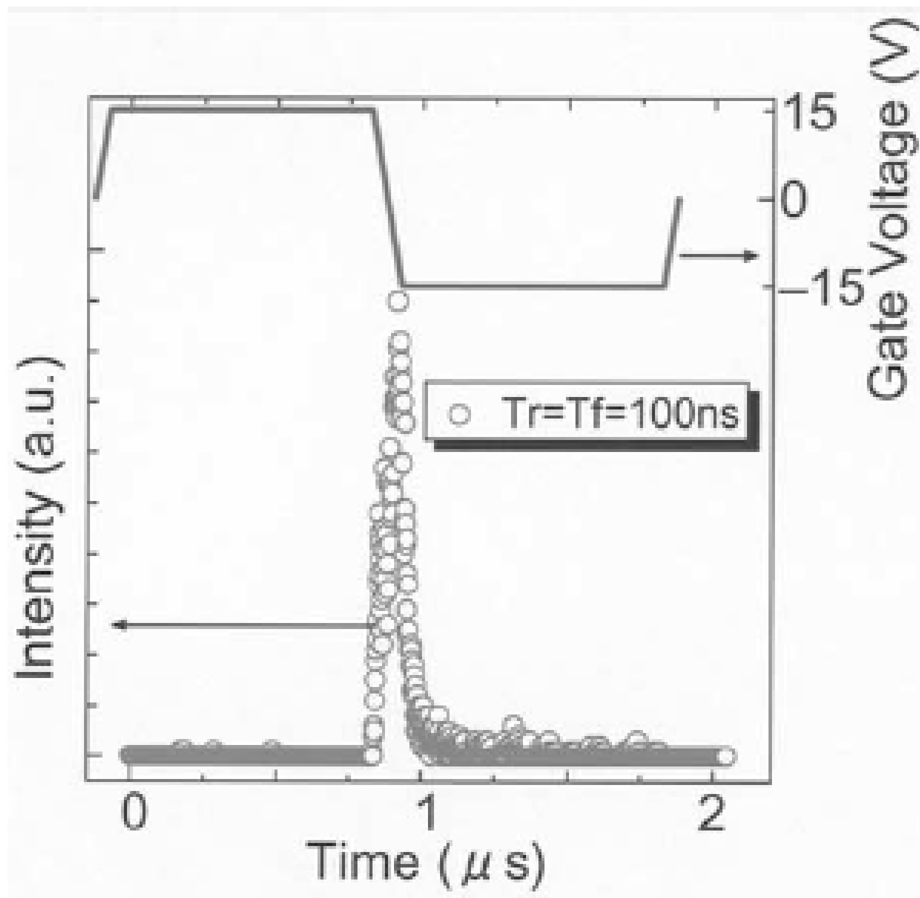


Figure 5-2 The emission microscope data for the device under gate dynamic stress ranging between + 15 V and – 15 V

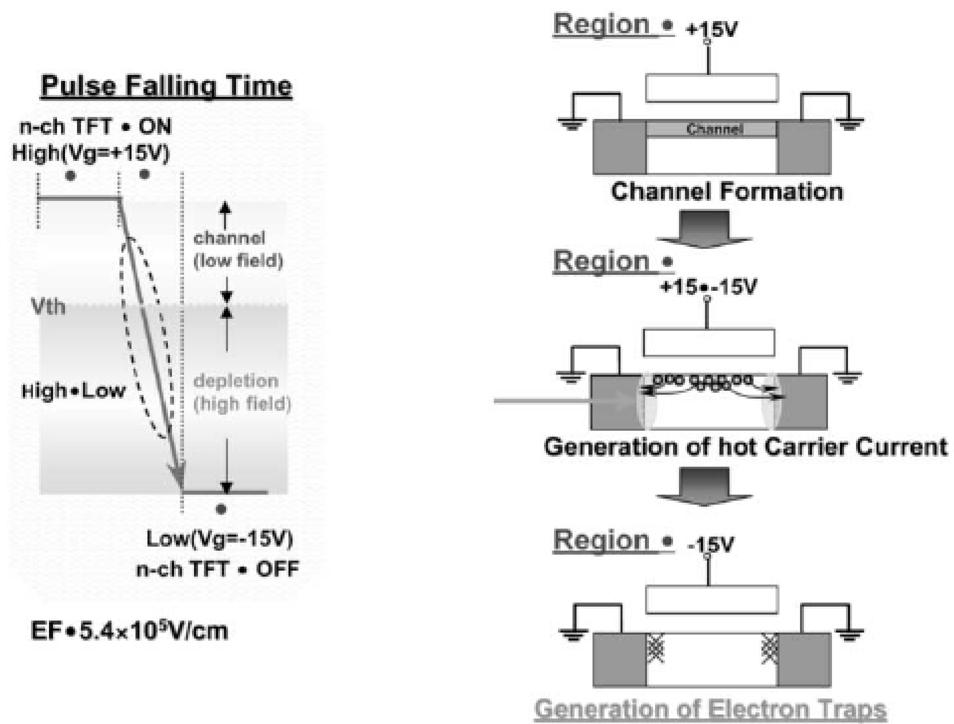


Figure 5-3 The model describing the mechanism for the degradation of n-type device under the gate dynamic stress ranging between + 15 V and – 15 V

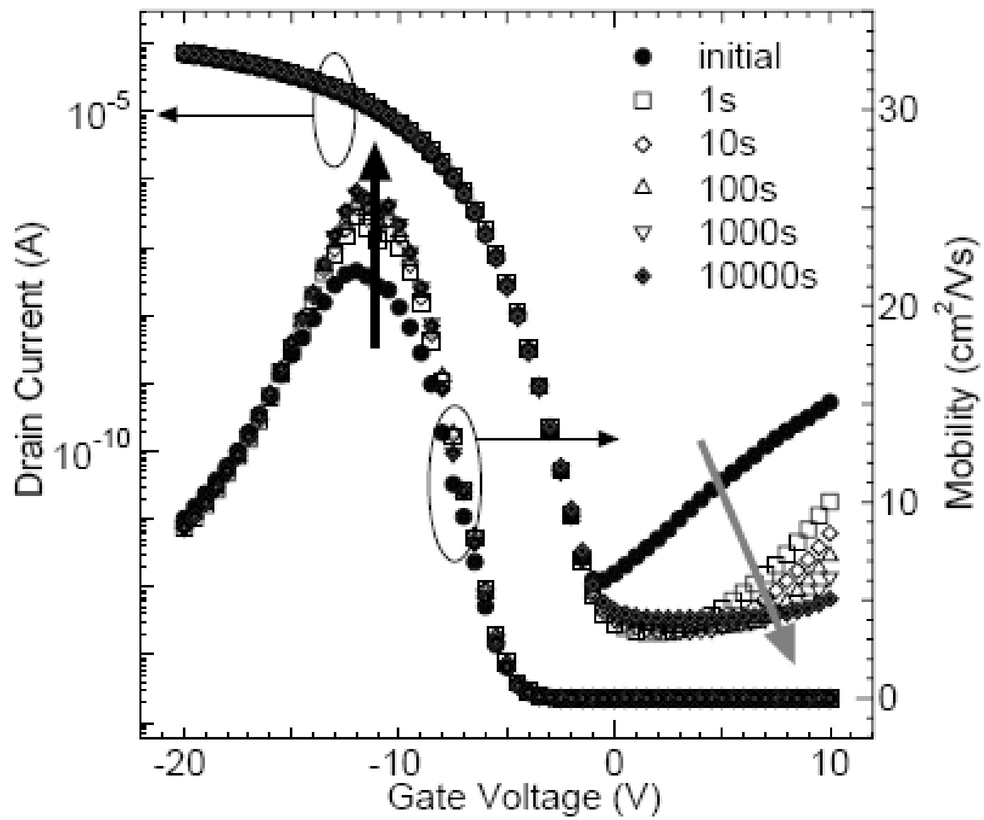


Figure 5-4 Transfer characteristics and device mobility for the p-type device under the gate dynamic stress ranging between + 15 V and – 15 V

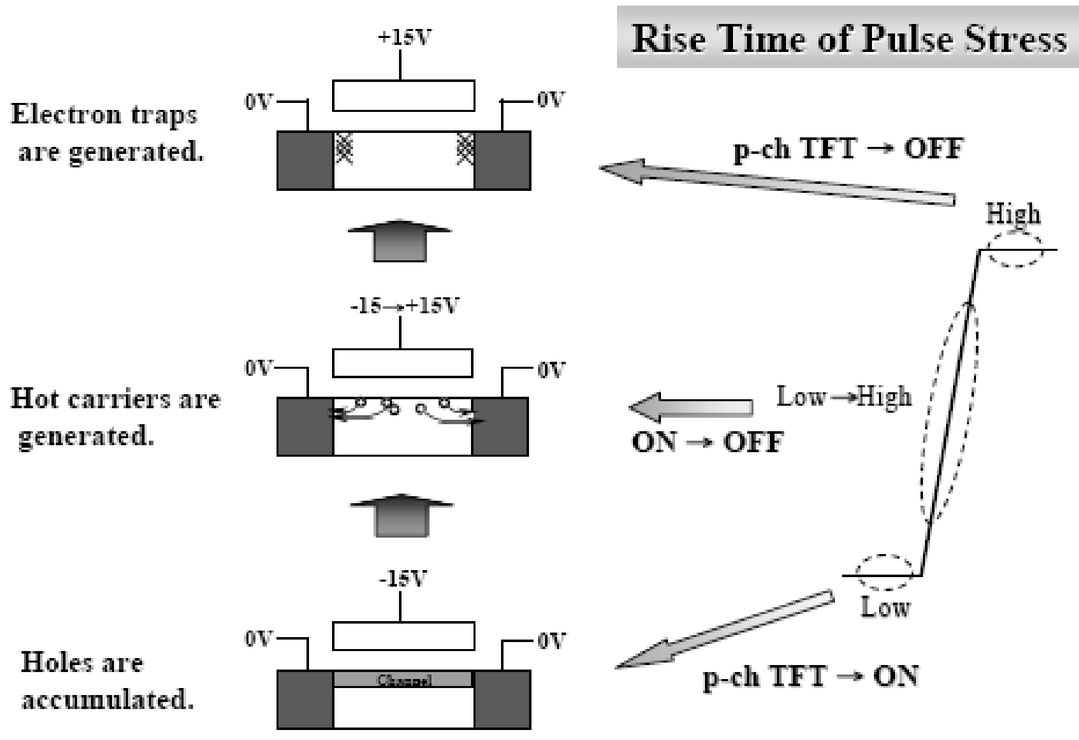


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Figure 5-5 The model describing the mechanism for the degradation of p-type device under the gate dynamic stress ranging between + 15 V and – 15 V

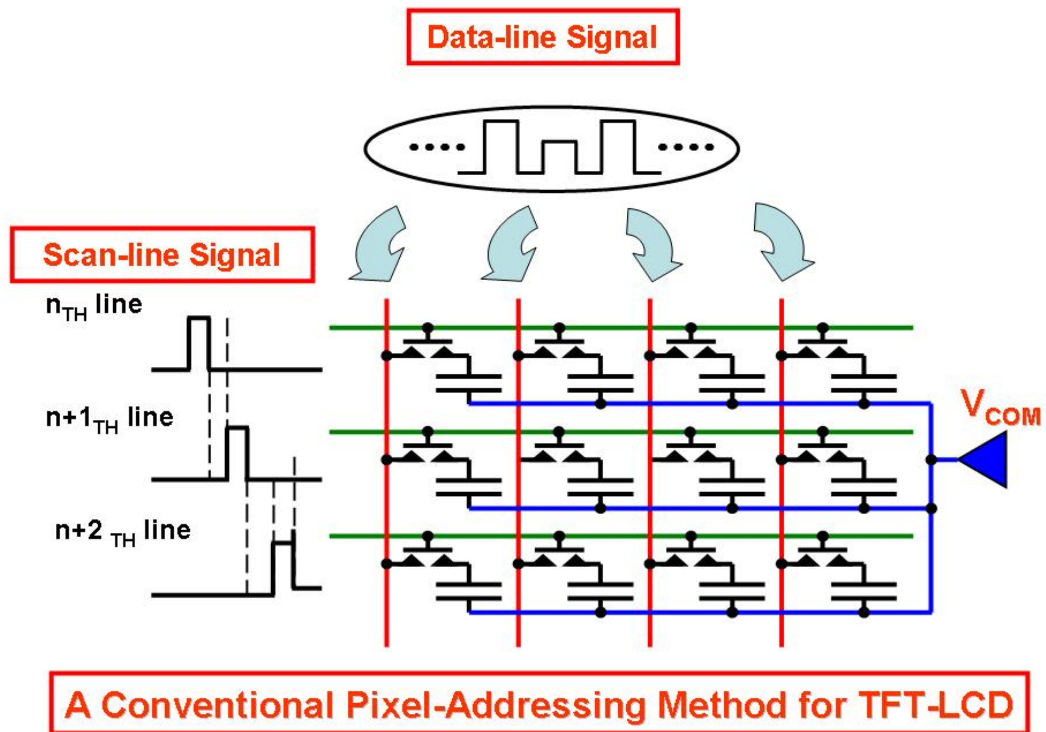


Figure 5-6 A conventional pixel-addressing method for the TFT-LCD panels

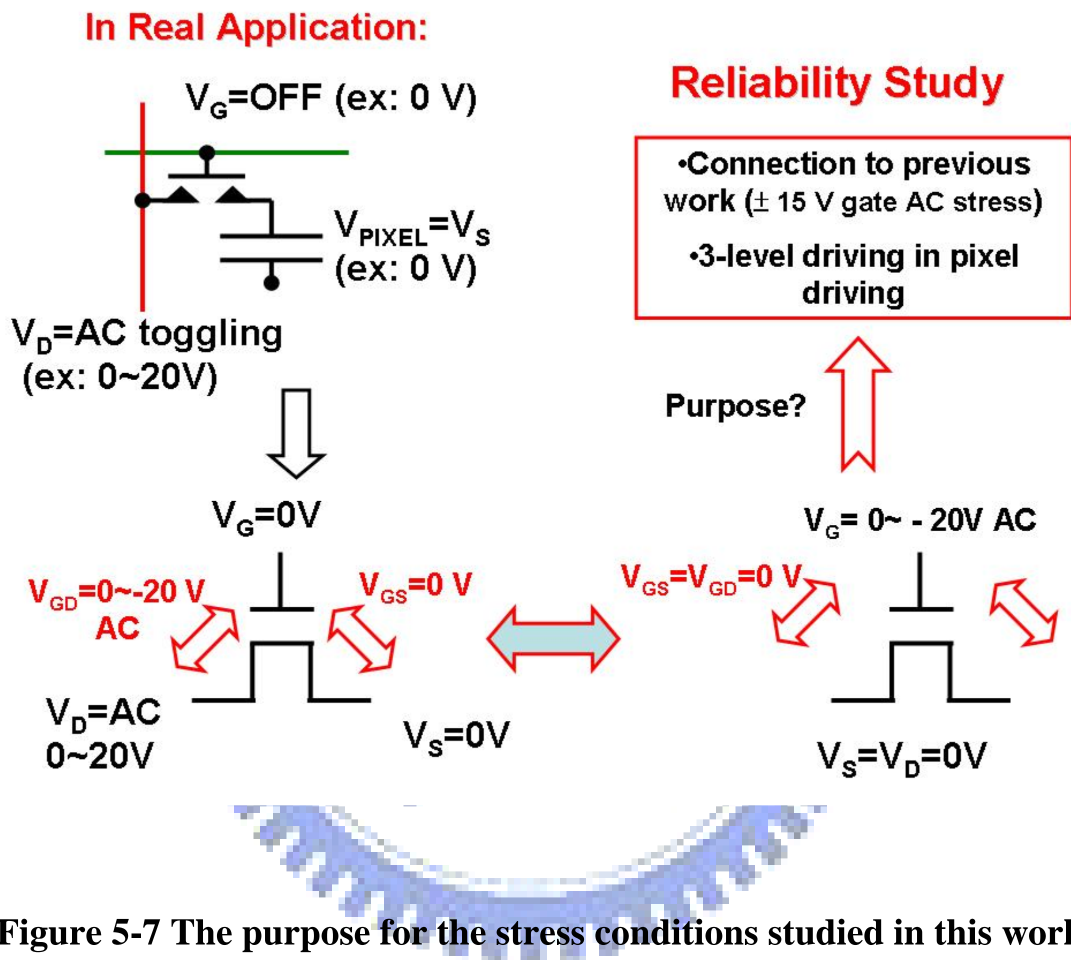
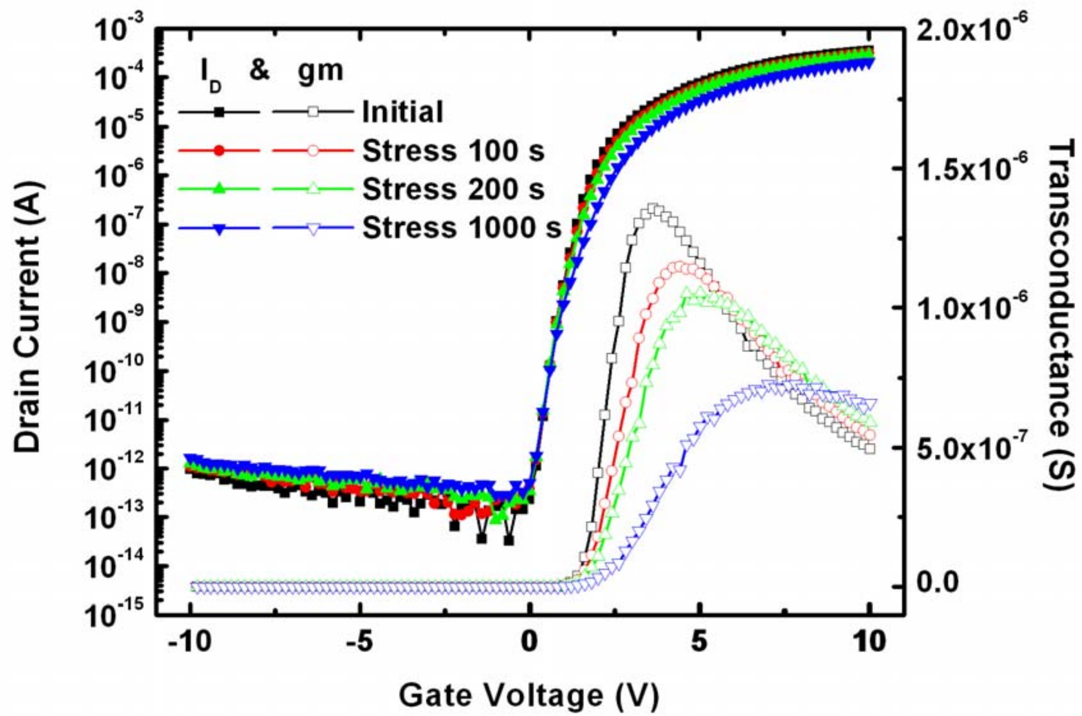


Figure 5-7 The purpose for the stress conditions studied in this work



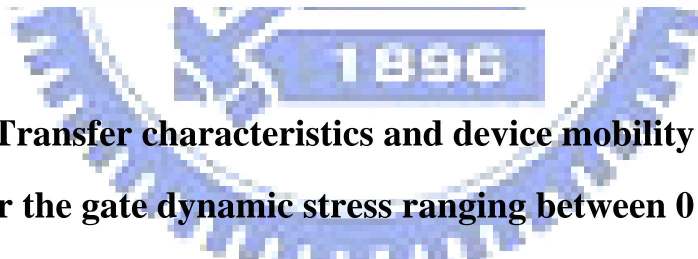


Figure 5-8 Transfer characteristics and device mobility for the n-type device after the gate dynamic stress ranging between 0 V and – 20 V with the grounded source and drain electrodes

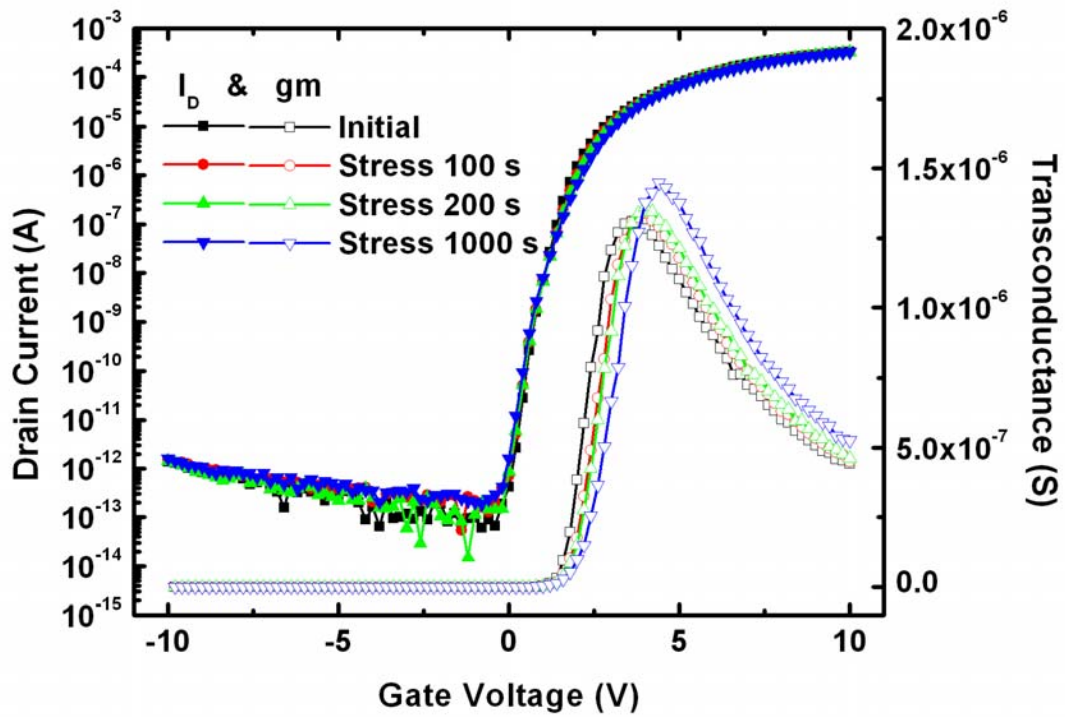


Figure 5-9 Transfer characteristics and device mobility for the n-type device after the gate DC stress – 20 V with source and drain electrodes grounded

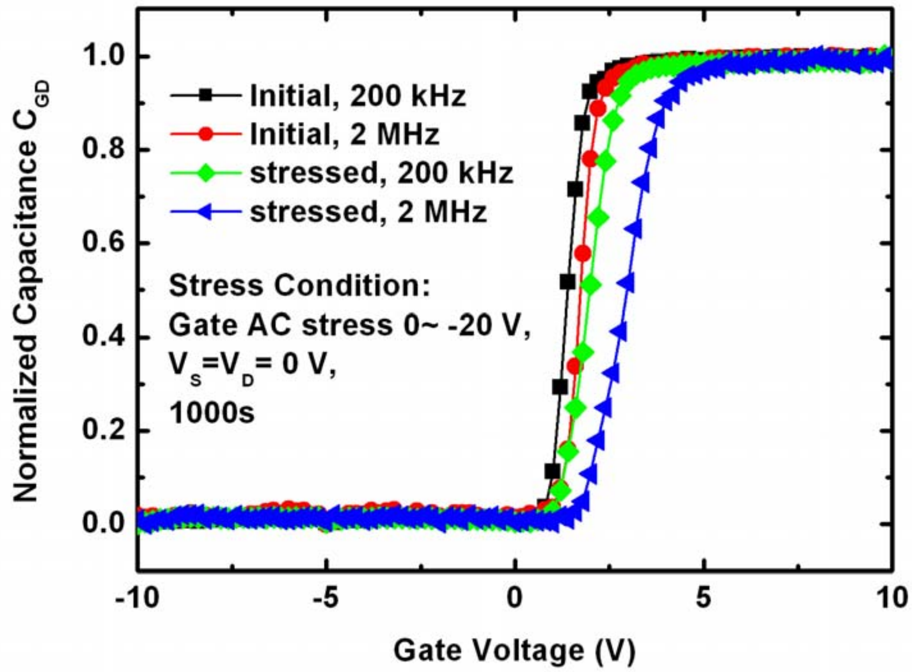


Figure 5-10 Normalized capacitance C_{GD} for the n-type device after the gate dynamic stress ranging between 0 V and – 20 V

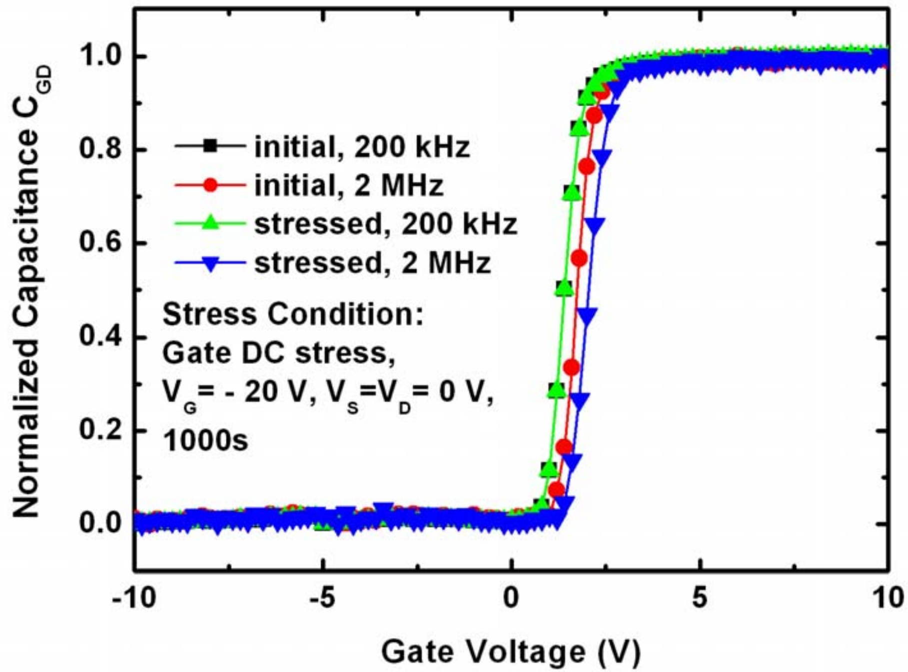


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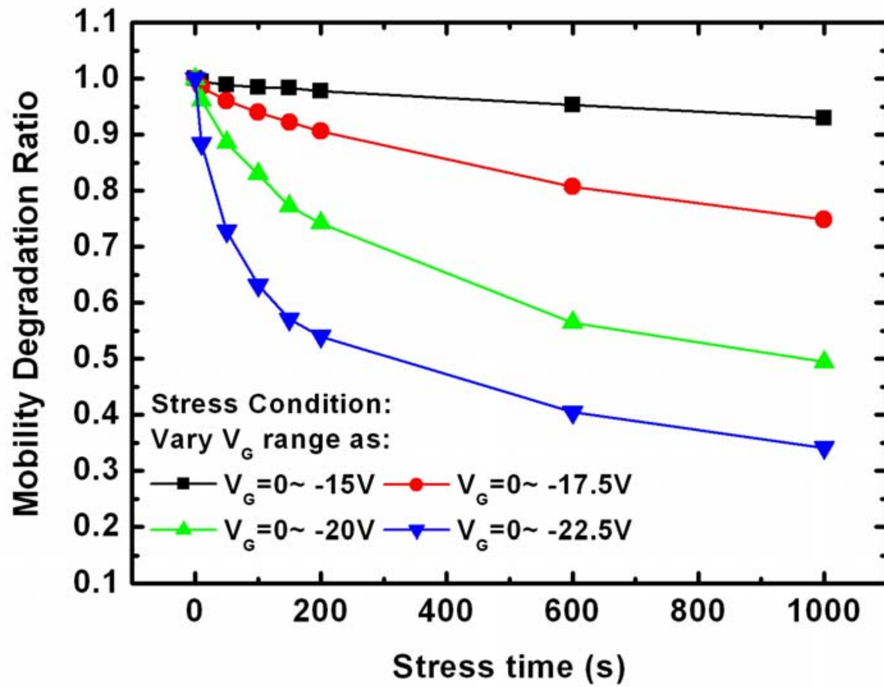
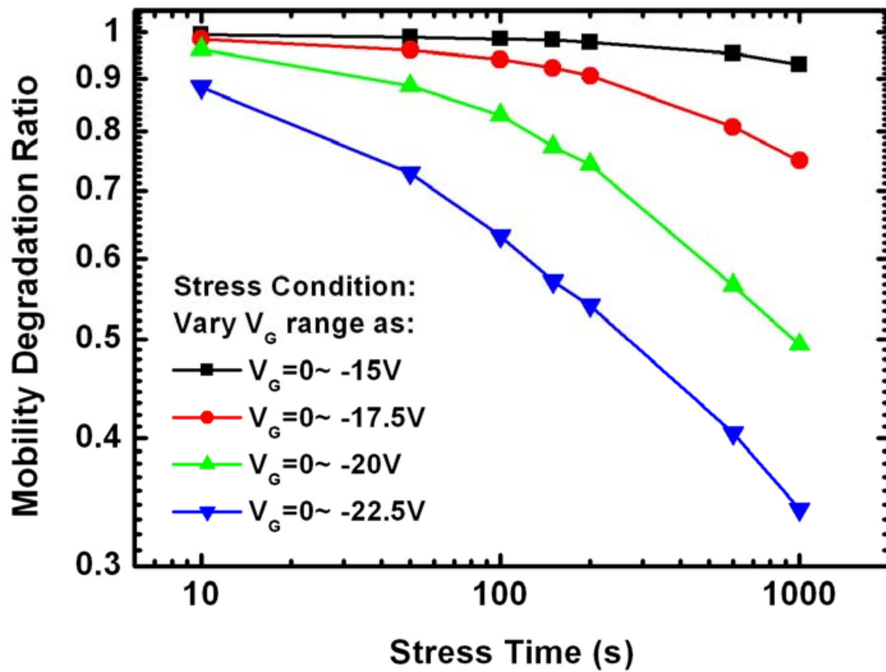
Figure 5-11 Normalized capacitance C_{GD} for the n-type device after – 20 V gate DC stress



(a)



(b)

Figure 5-12 Mobility degradation for the n-type device after gate dynamic stress with different voltage range in (a) linear scale and (b) logarithmic scale

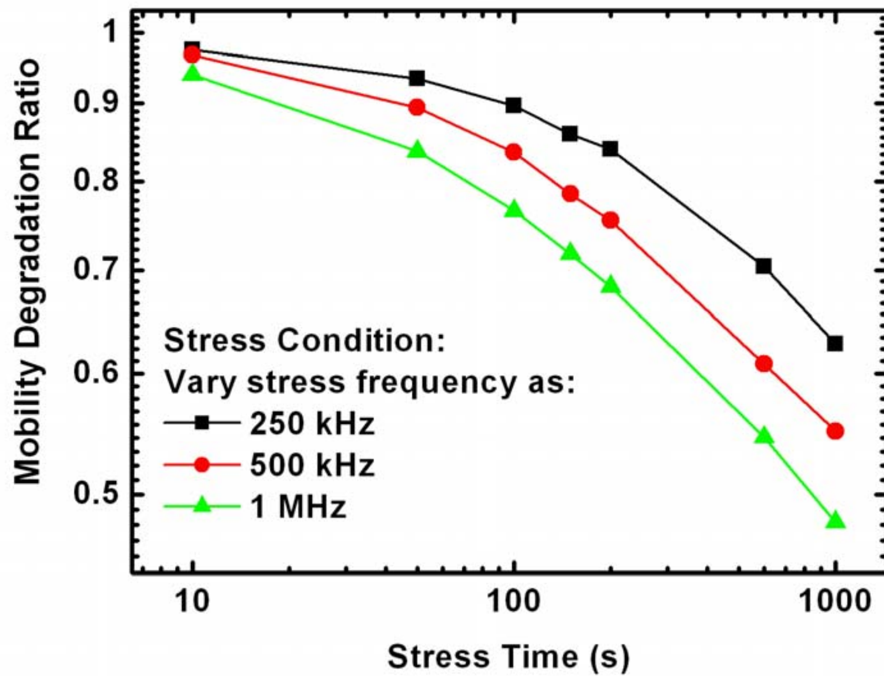
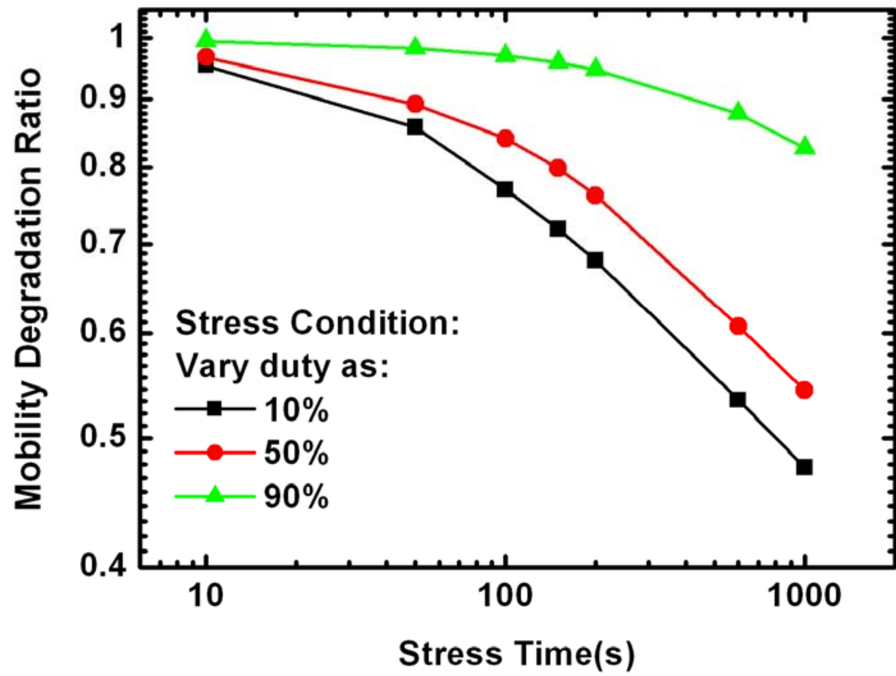


Figure 5-13 Mobility degradation for the n-type device after gate dynamic stress with different pulse frequencies



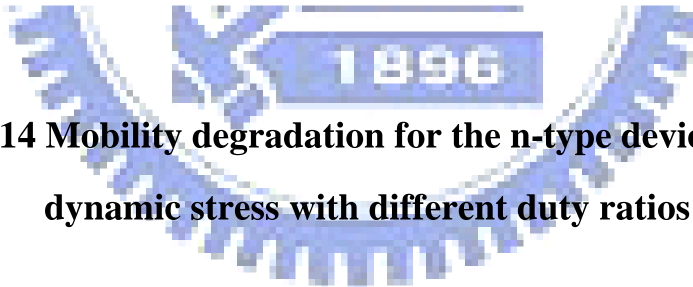

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Figure 5-14 Mobility degradation for the n-type device after gate dynamic stress with different duty ratios

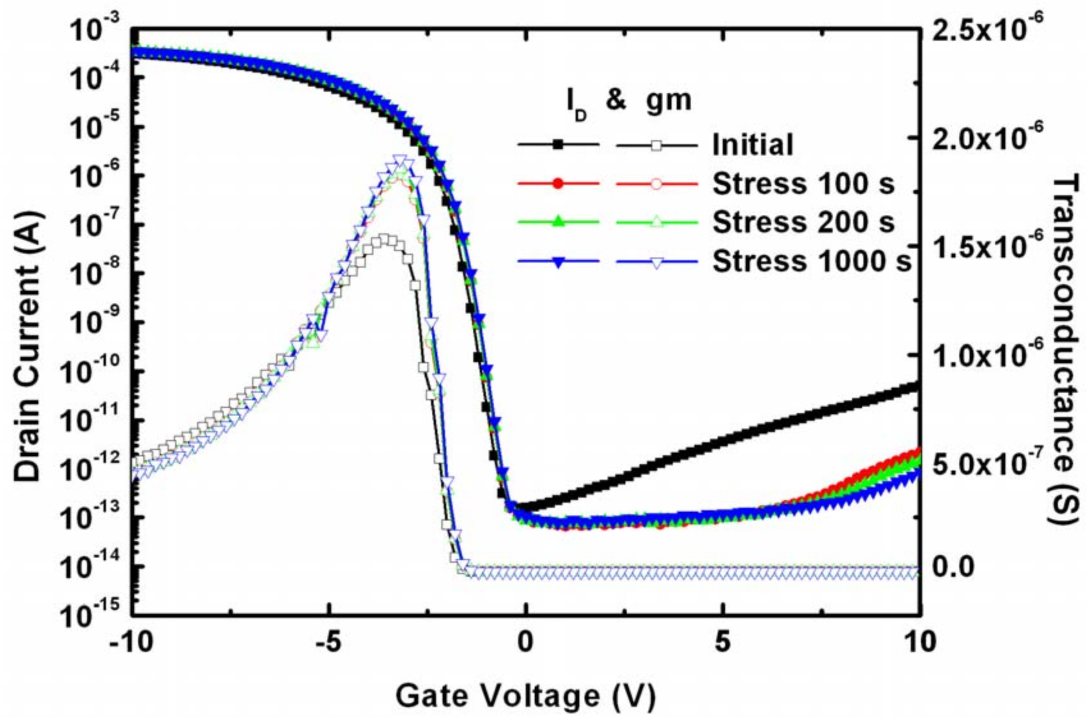

Figure 5-15 Transfer characteristics and device mobility for the p-type device under the gate dynamic stress ranging between 0 V and + 20 V with the grounded source and drain electrodes

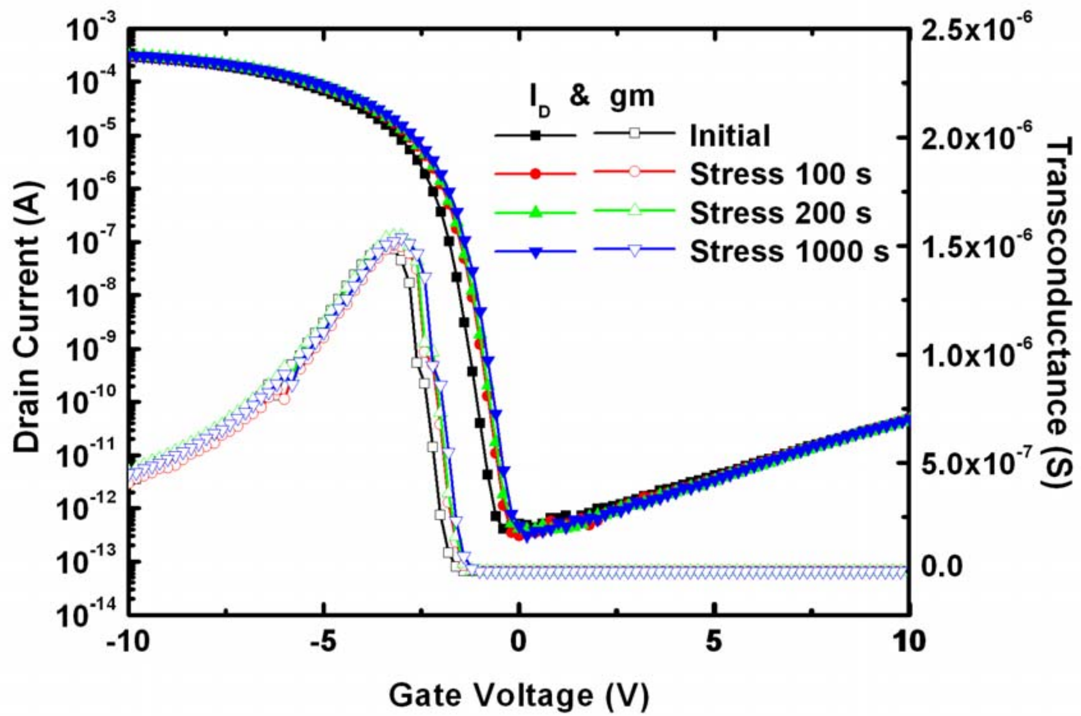

Figure 5-16 Transfer characteristics and device mobility for the p-type device under the gate DC stress + 20 V with source and drain electrodes are grounded

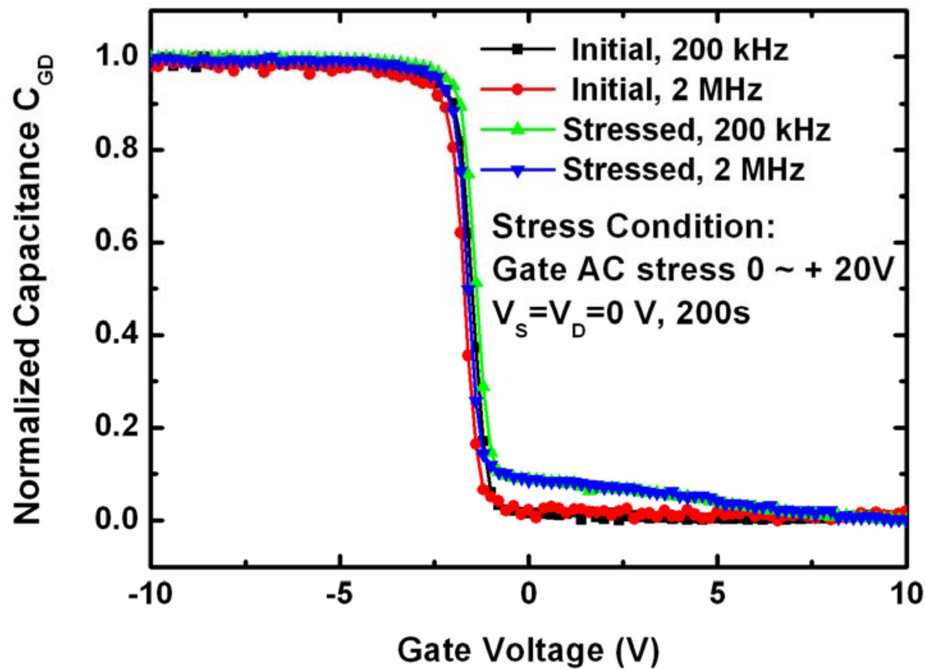

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Figure 5-17 Normalized capacitance C_{GD} for the p-type device after gate dynamic stress ranging between 0 V and + 20 V

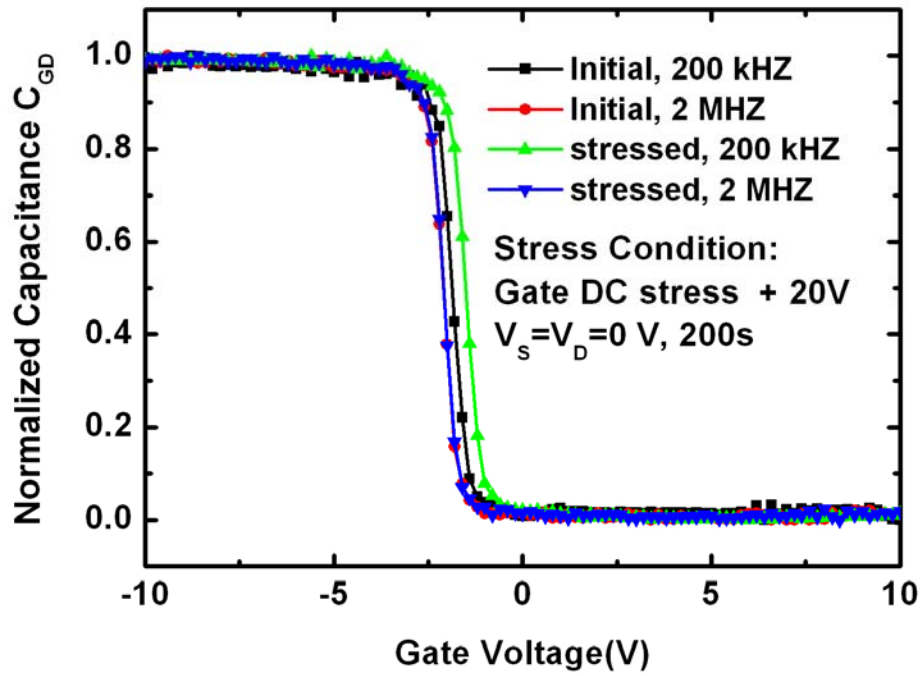
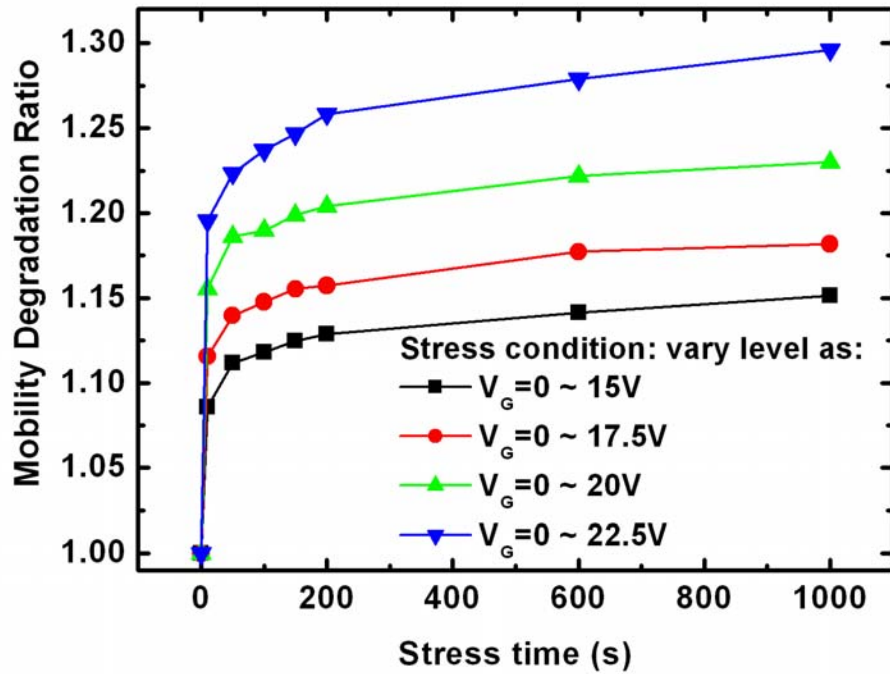
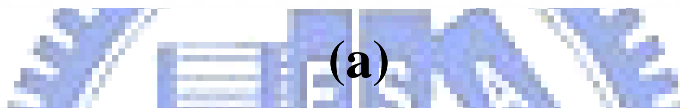
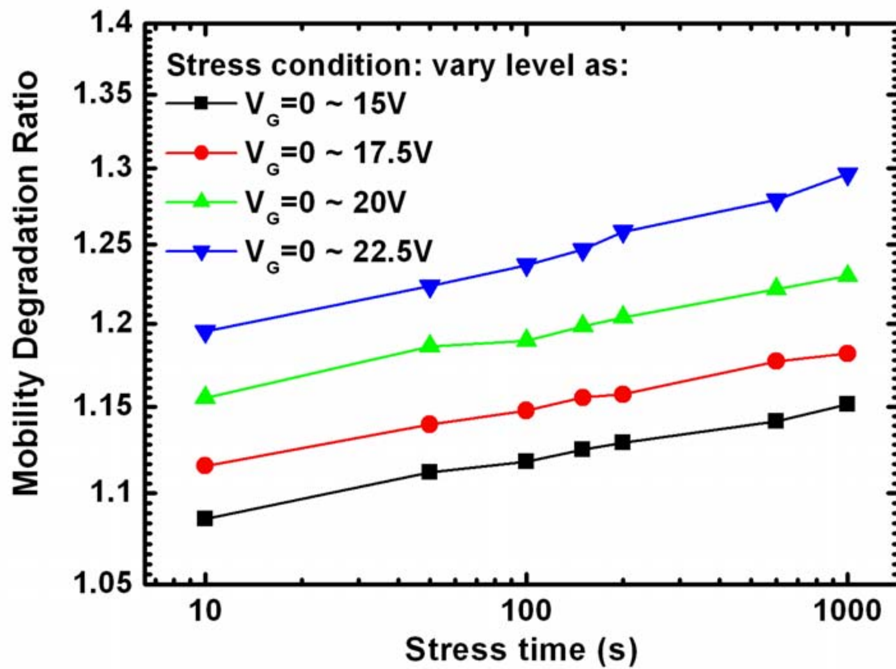


Figure 5-18 Normalized capacitance C_{GD} for the p-type device after the gate DC stress + 20 V





(a)



(b)

Figure 5-19 Mobility degradation for the p-type device after gate dynamic stress with different voltage range shown in (a) linear scale and (b) logarithmic scale

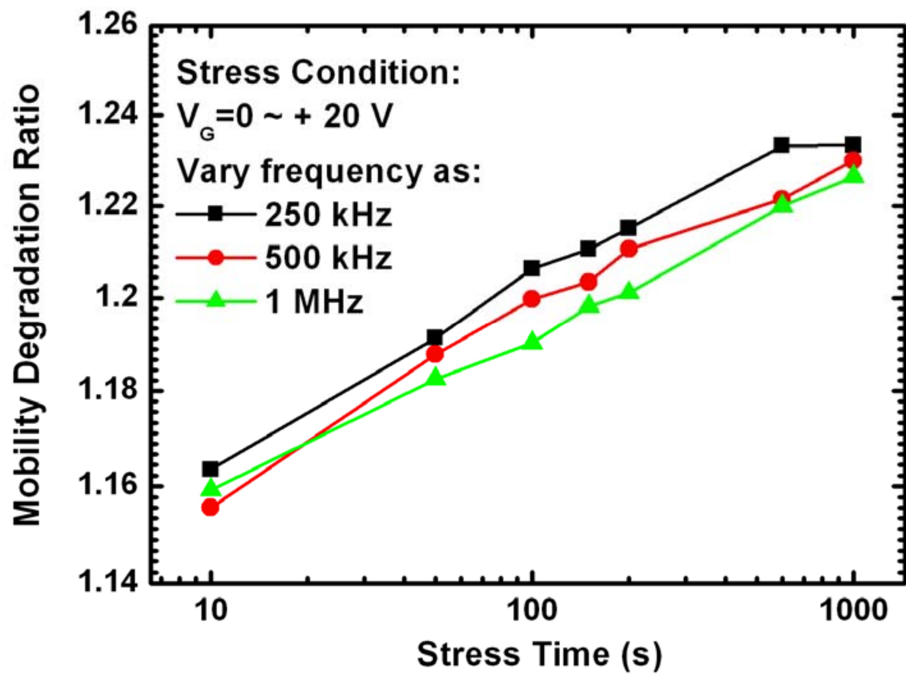


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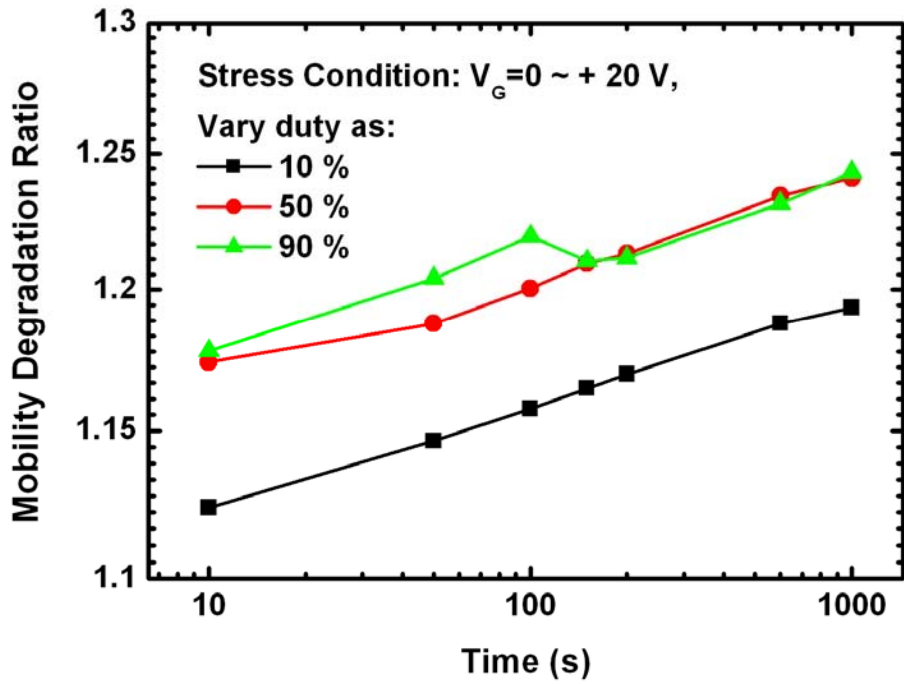
Figure 5-20 Mobility degradation for the p-type device after gate dynamic stress with different pulse frequencies



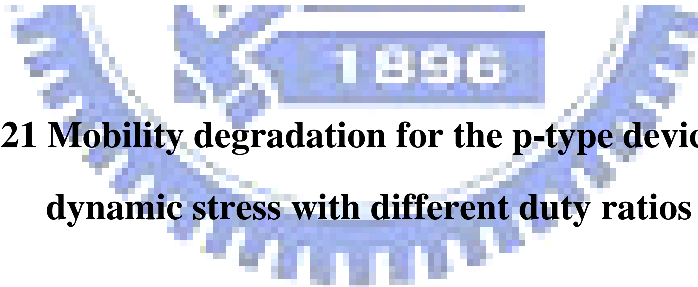


Figure 5-21 Mobility degradation for the p-type device after gate dynamic stress with different duty ratios

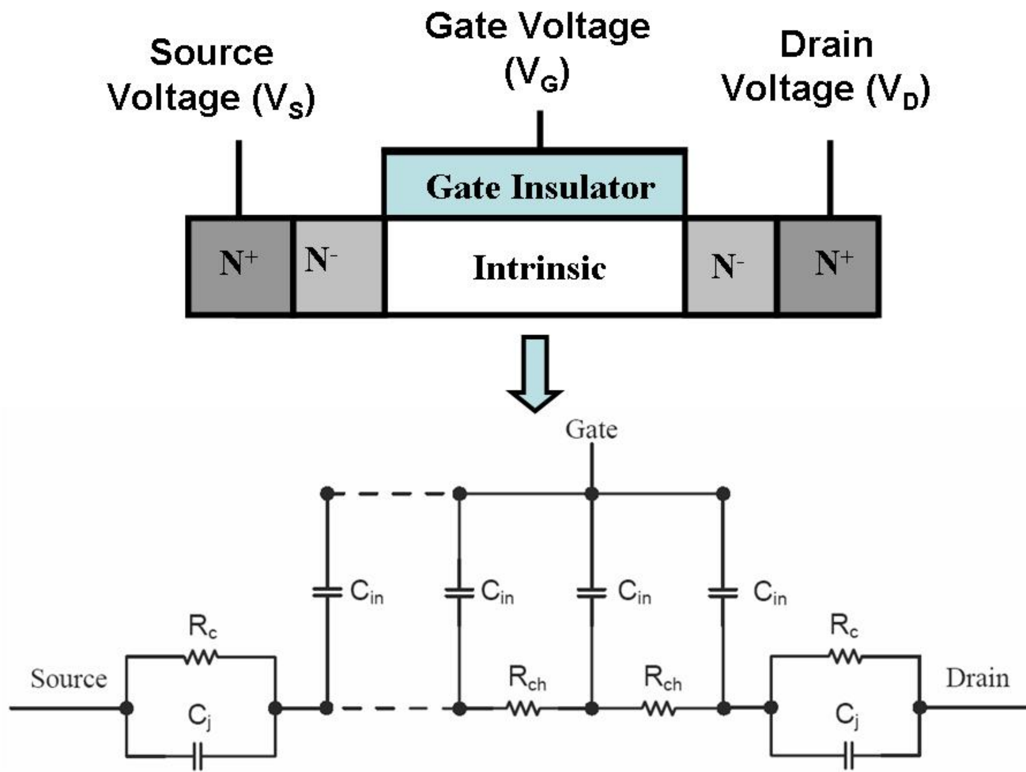


Figure 5-22 Device cross section view and an equivalent circuit model for an n-type poly-Si TFT

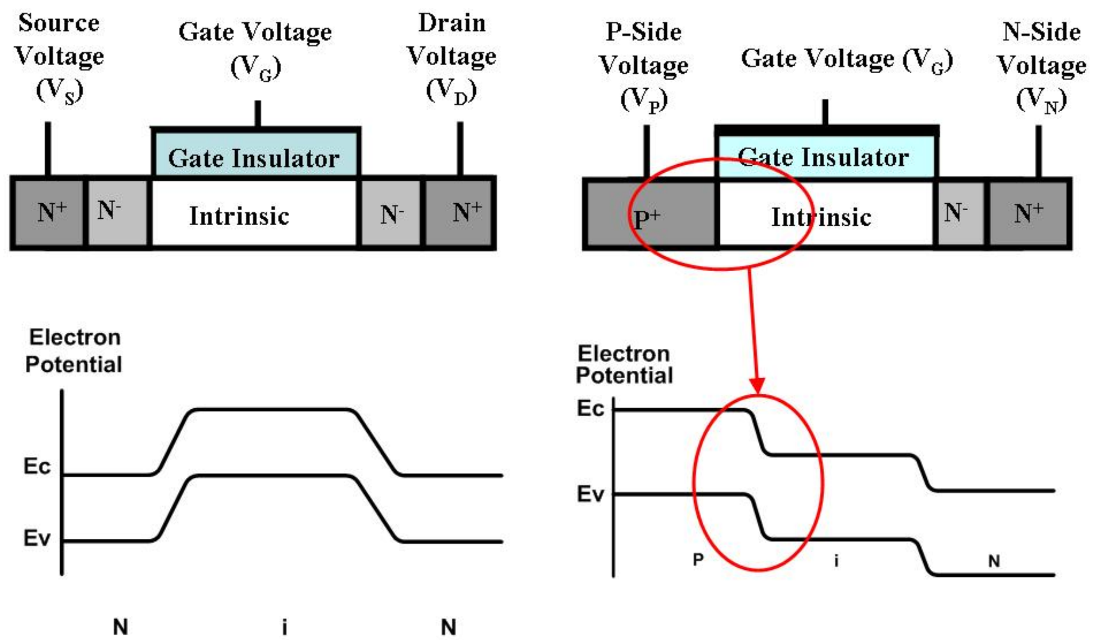


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Figure 5-23 Device cross section view and the band diagram for the gated p-i-n device

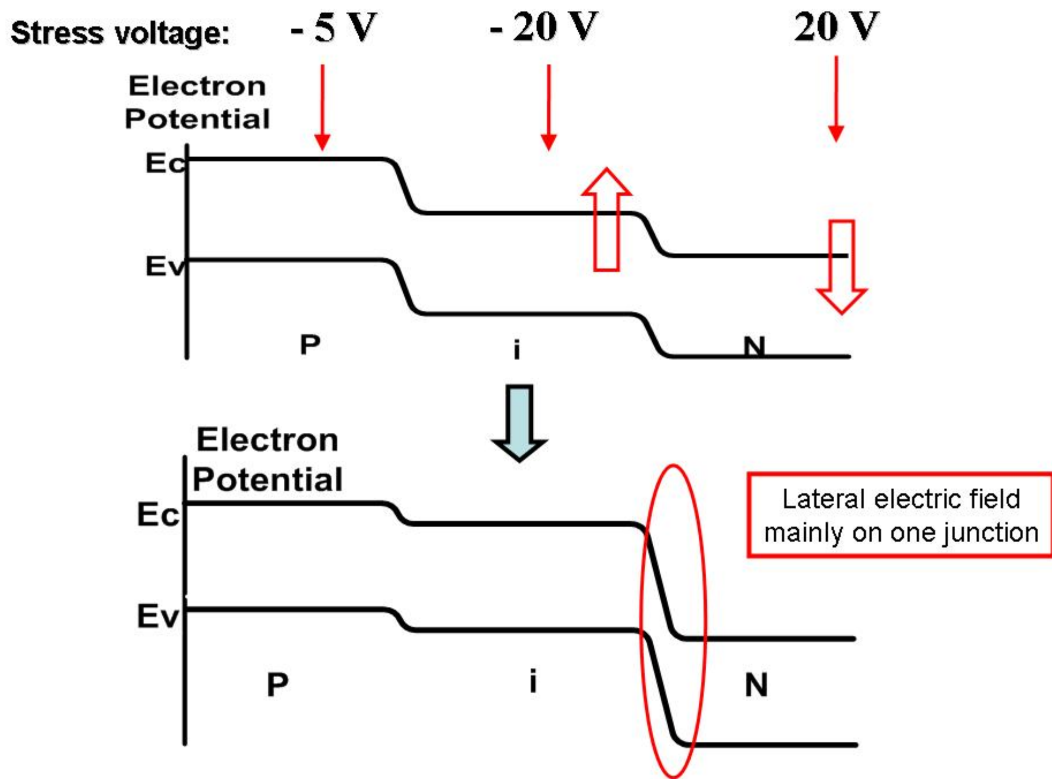


Figure 5-24 The figure showing how the voltage is picked to have only the N-side junction with large electric field

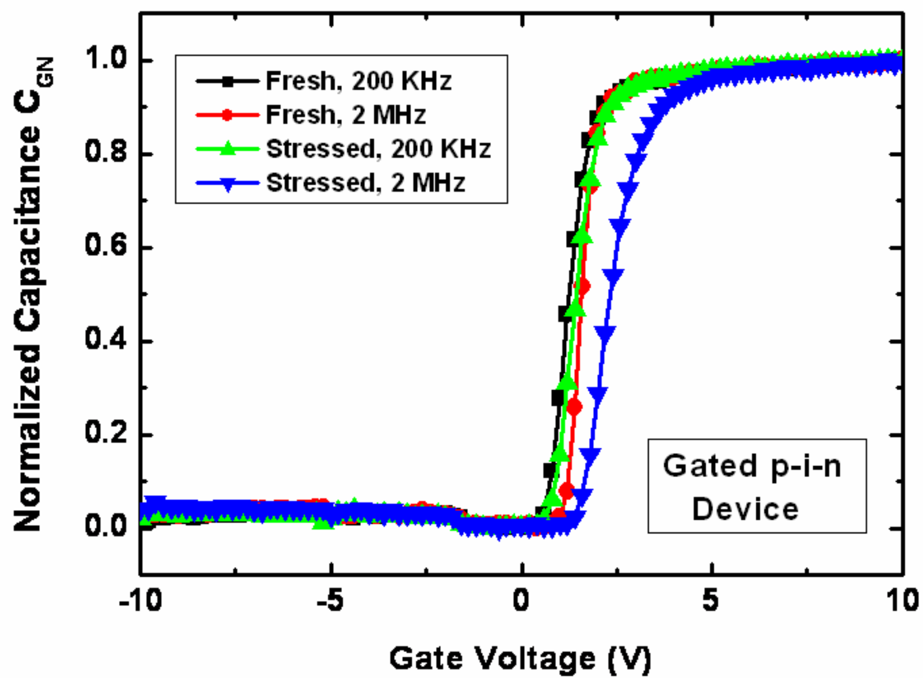


Figure 5-25 Normalized capacitance C_{GD} for the gated p-i-n device after 200 second DC stress

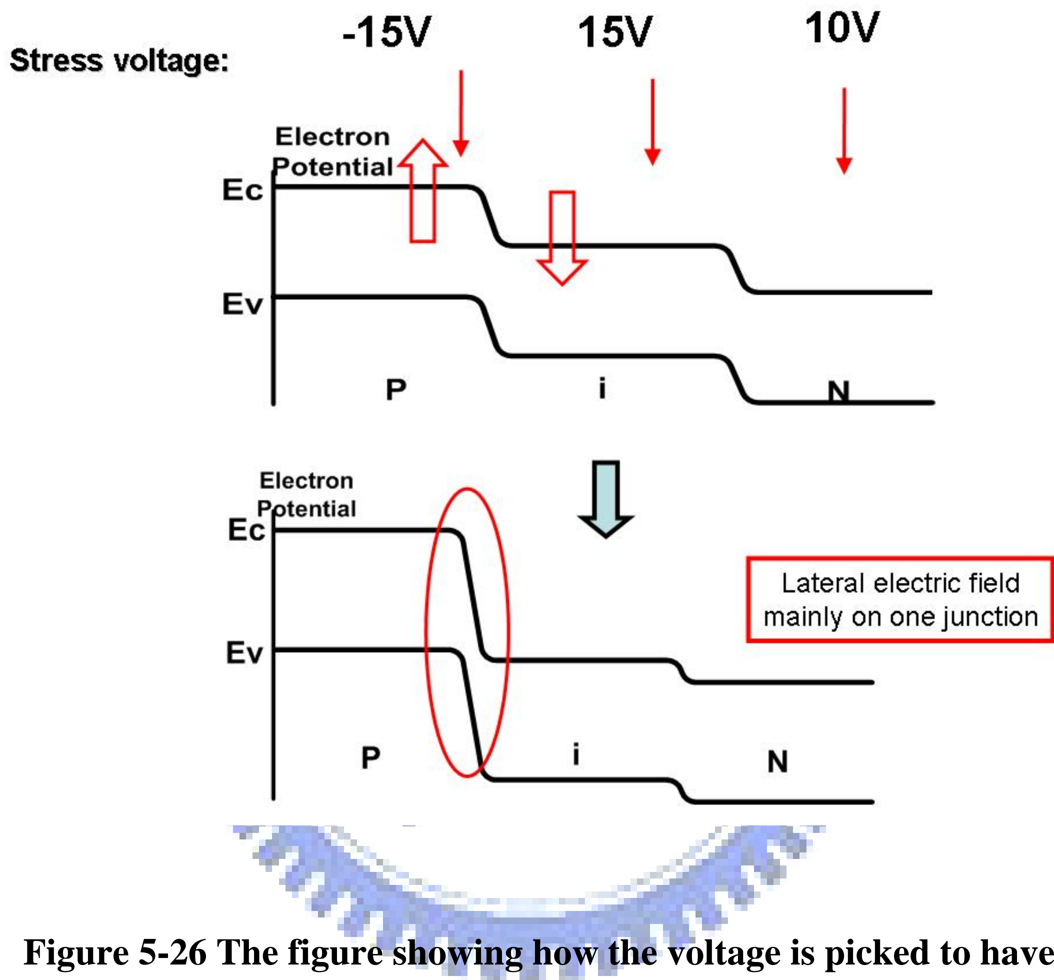
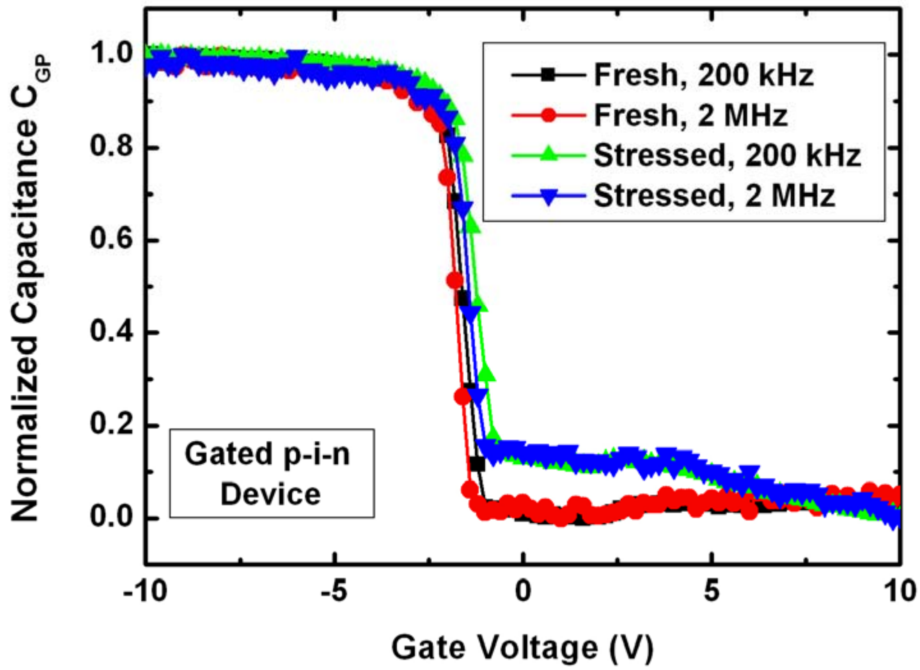


Figure 5-26 The figure showing how the voltage is picked to have only the P-side junction with large electric field



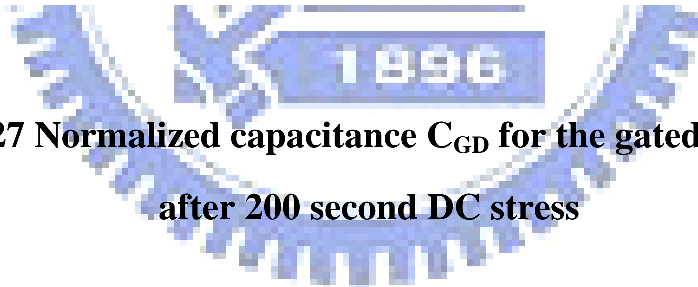


Figure 5-27 Normalized capacitance C_{GD} for the gated p-i-n device after 200 second DC stress

Large E-field on junctions

Carrier source: thermal activated electrons

N-type TFT

Collision near the junction

Creating Defect States

P-type TFT

Carrier source: electrons in leakage current

Electrons get trapped in oxide near source/drain junction

Channel Shortening Effect

Ec
Ef
Ev
P-side
e-
$\vec{E}$
0→-20V
Ec
Ef
Ev

Gate
Drain
Gate Insulator
P^+
Potential near junction
E_c
E_F
E_v

Figure 5-28 The figure discussing how the large electric field over the junctions could lead to the degradation

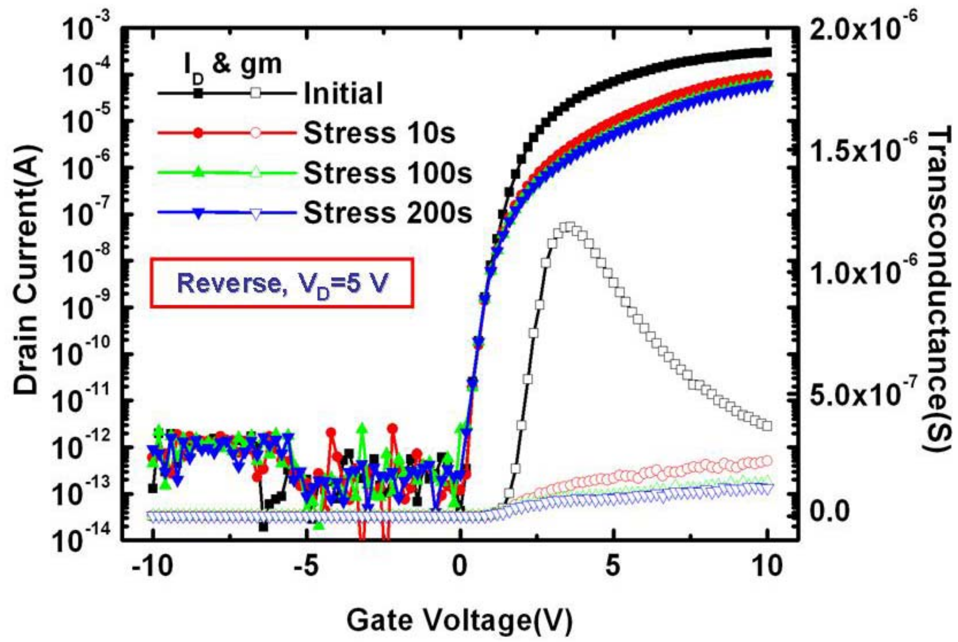


Figure 5-29 Transfer characteristics and device mobility for the n-type device before and after the DC hot carrier stress with stress duration 200 seconds

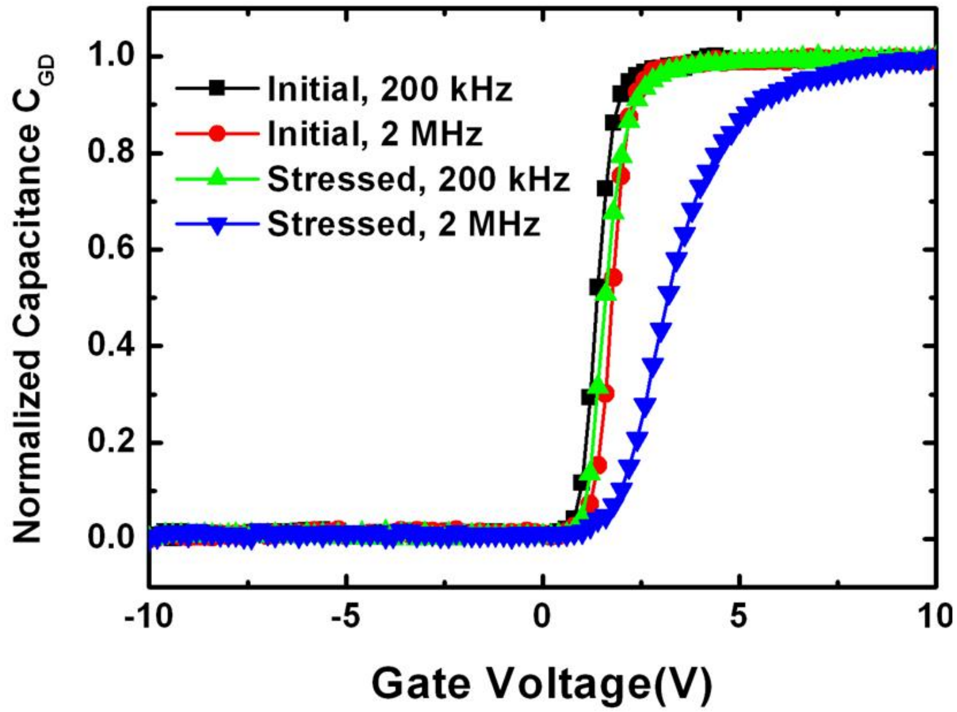


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Figure 5-30 Normalized capacitance C_{GD} for the n-type device before and after DC hot carrier stress

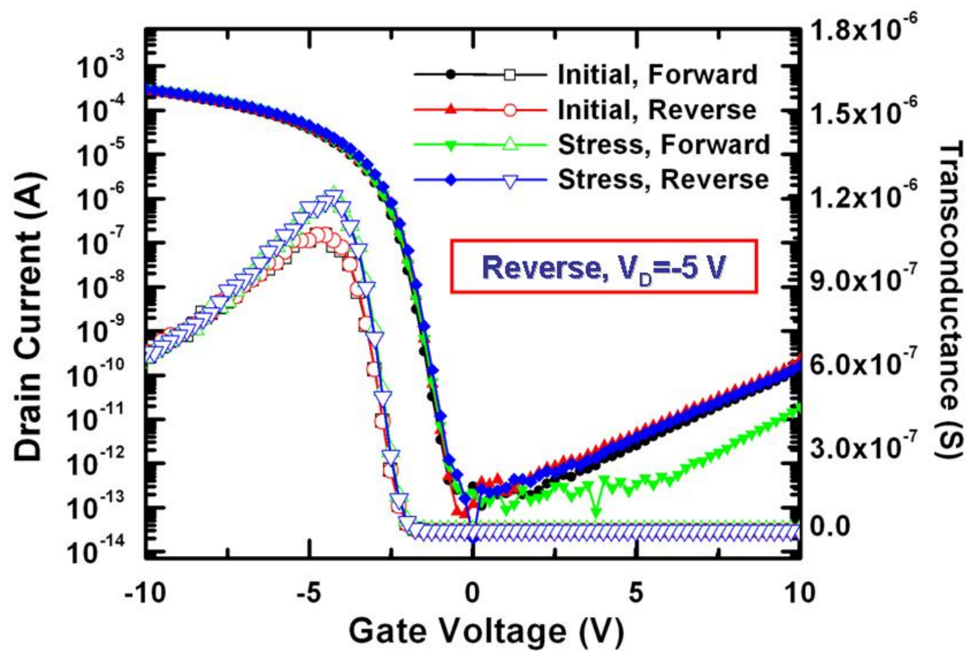
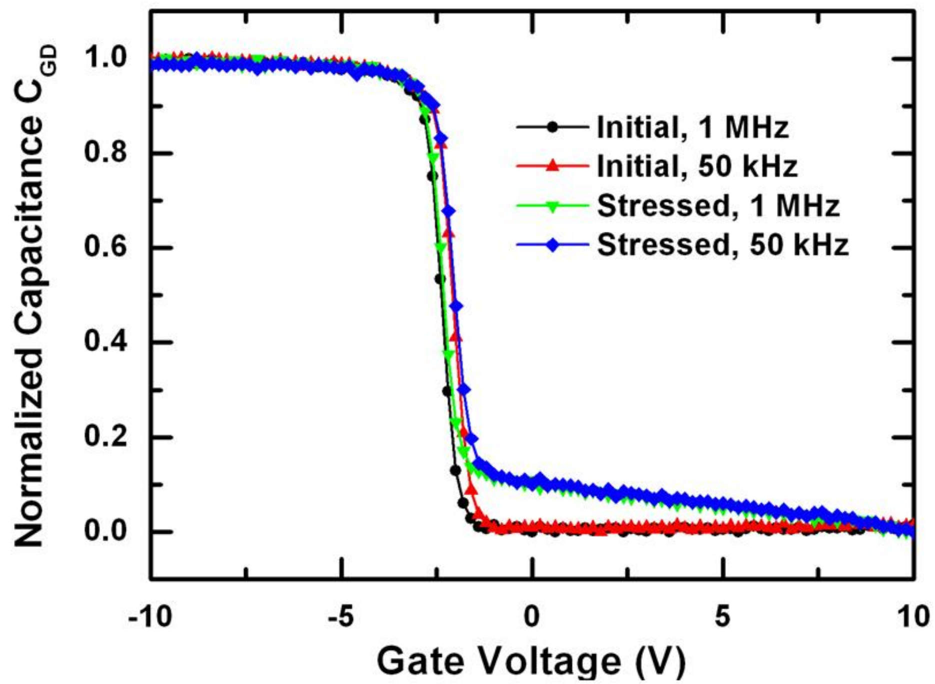


Figure 5-31 Transfer characteristics and device mobility for the p-type device after the DC hot carrier stress with stress duration 200 seconds



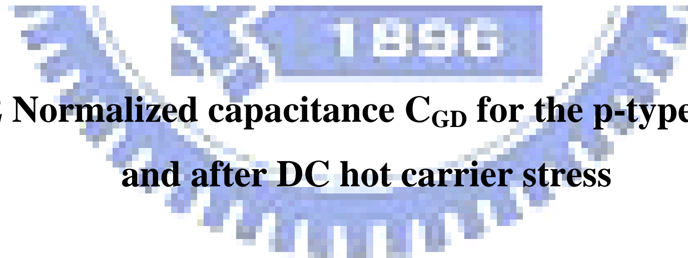

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Figure 5-32 Normalized capacitance C_{GD} for the p-type device before and after DC hot carrier stress

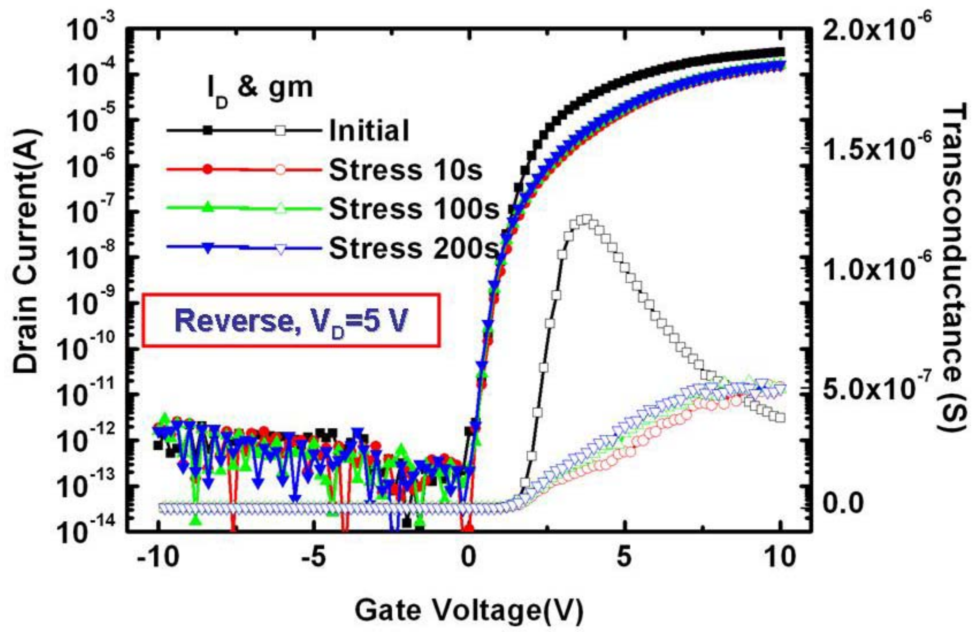


Figure 5-33 Transfer characteristics and device mobility for the n-type device before and after the drain DC stress with stress duration 200 seconds

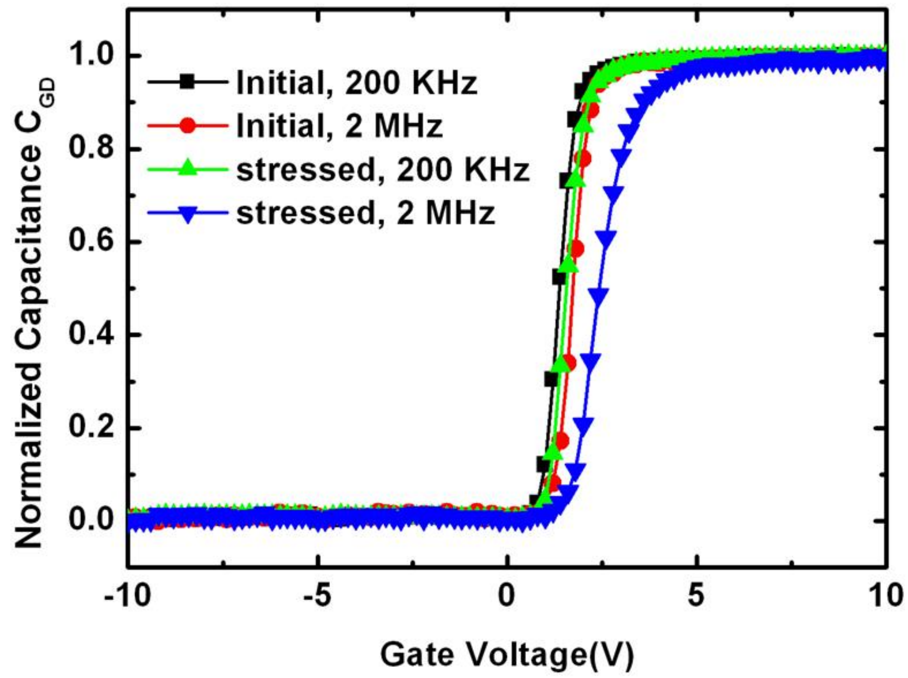


Figure 5-34 Normalized capacitance C_{GD} for the n-type device before and after drain DC stress

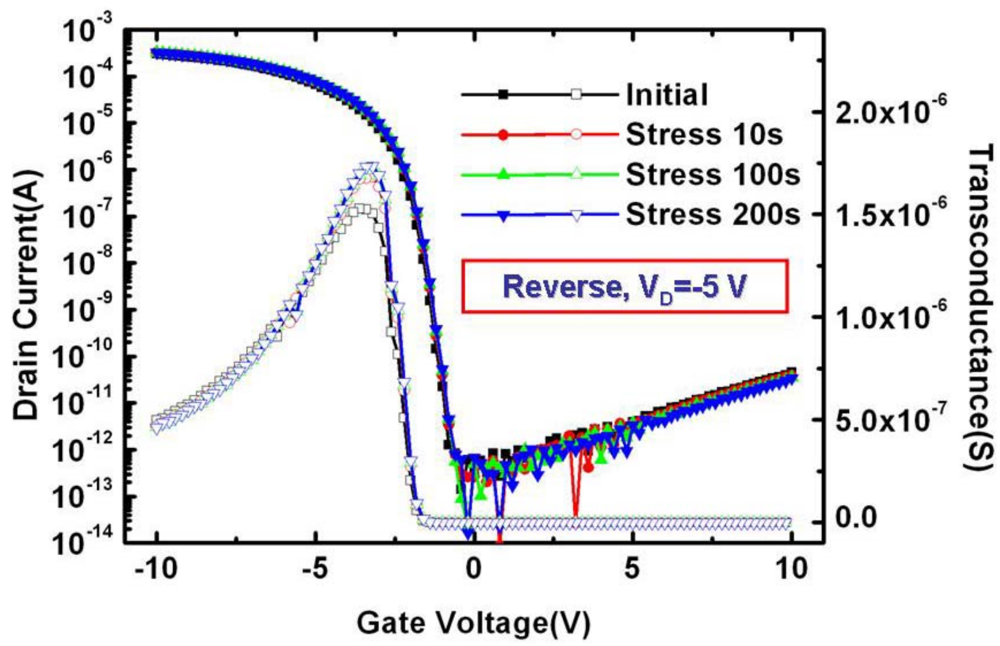
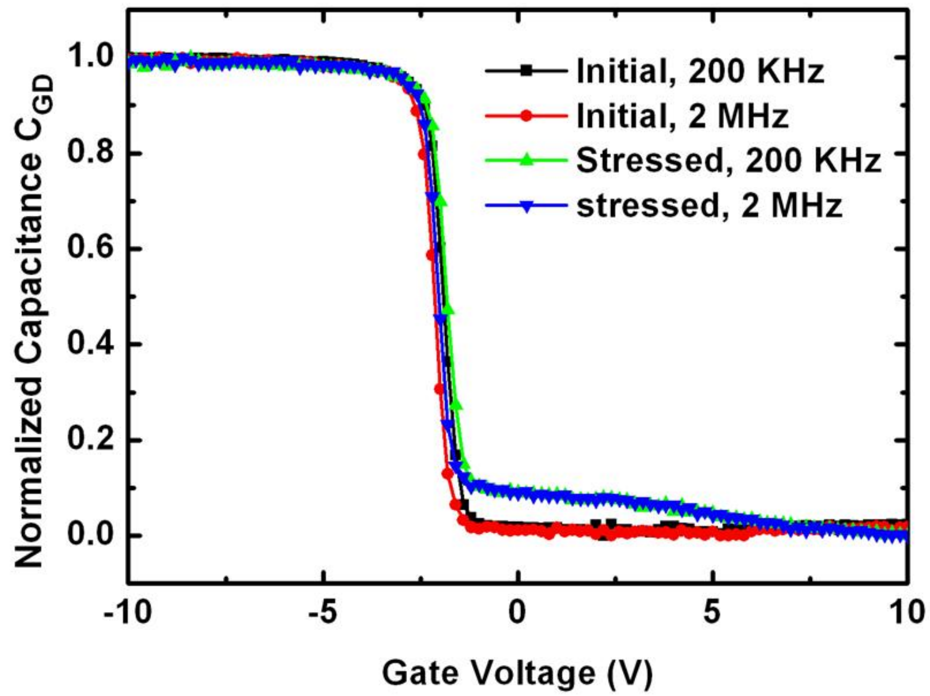


Figure 5-35 Transfer characteristics and device mobility for the p-type device before and after the drain DC stress with stress duration 200 seconds



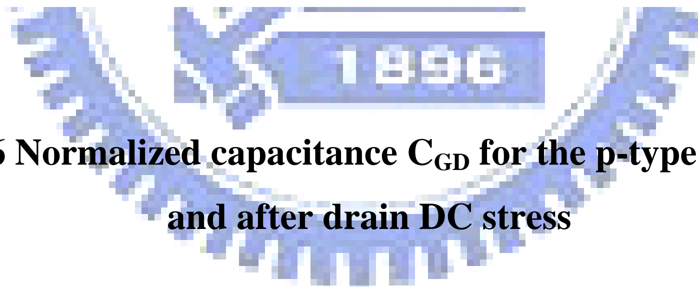


Figure 5-36 Normalized capacitance C_{GD} for the p-type device before and after drain DC stress

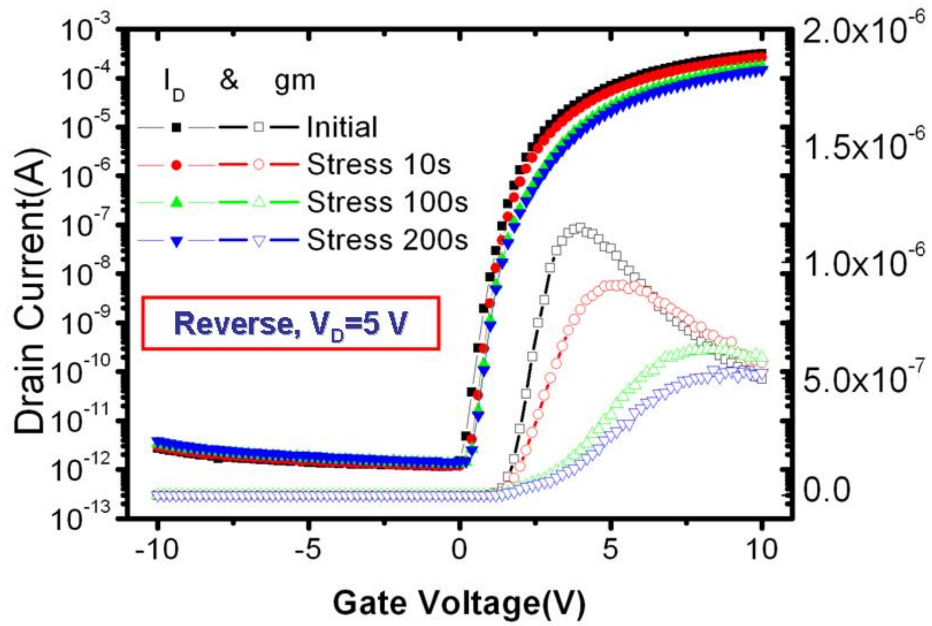
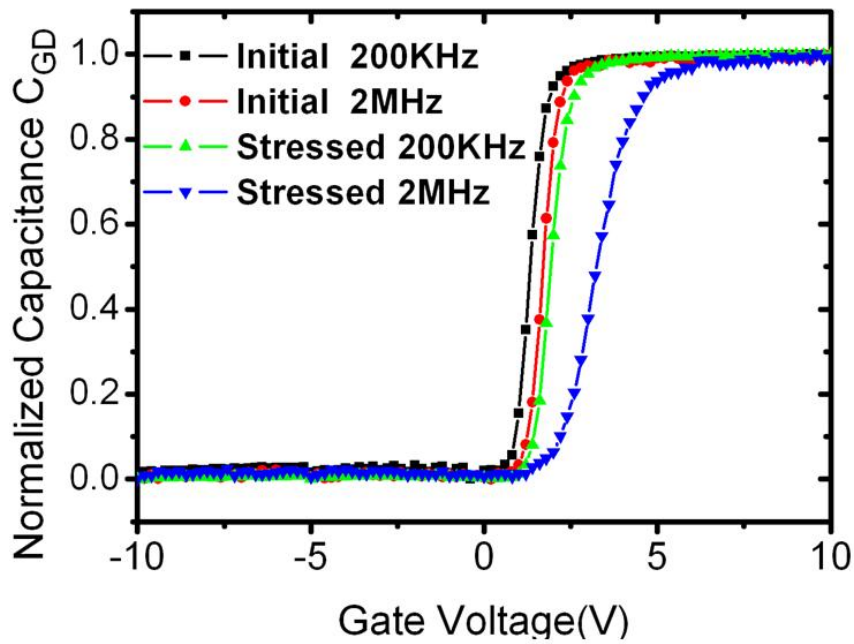


Figure 5-37 Transfer characteristics and device mobility for the n-type device before and after the gate AC stress toggling between ON/OFF regions



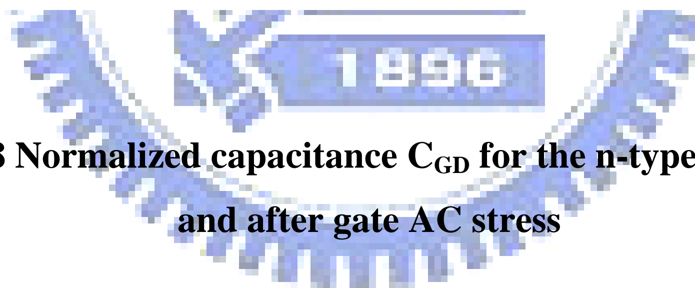


Figure 5-38 Normalized capacitance C_{GD} for the n-type device before and after gate AC stress

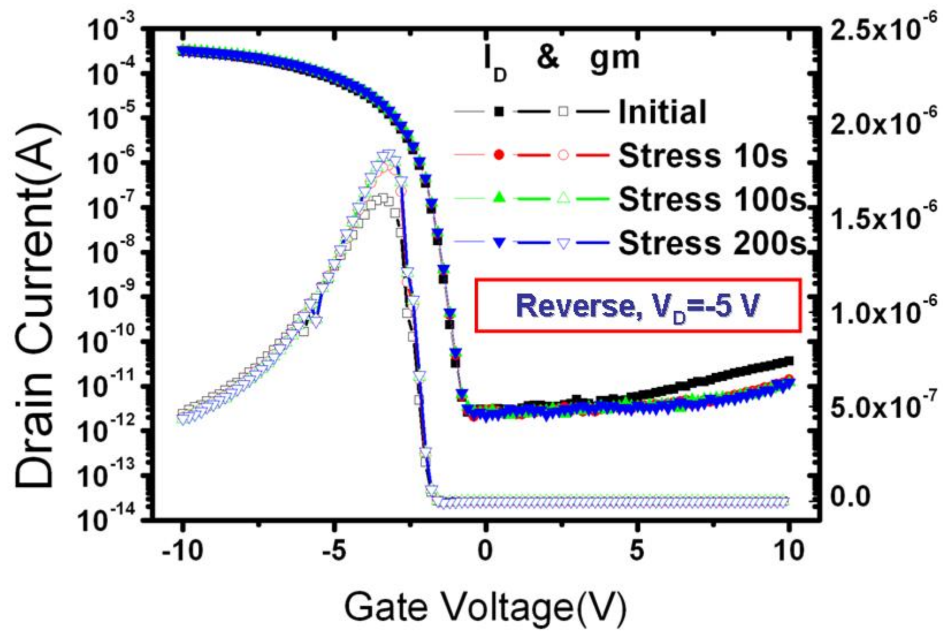


Figure 5-39 Transfer characteristics and device mobility for the p-type device before and after the gate AC stress toggling between ON/OFF regions

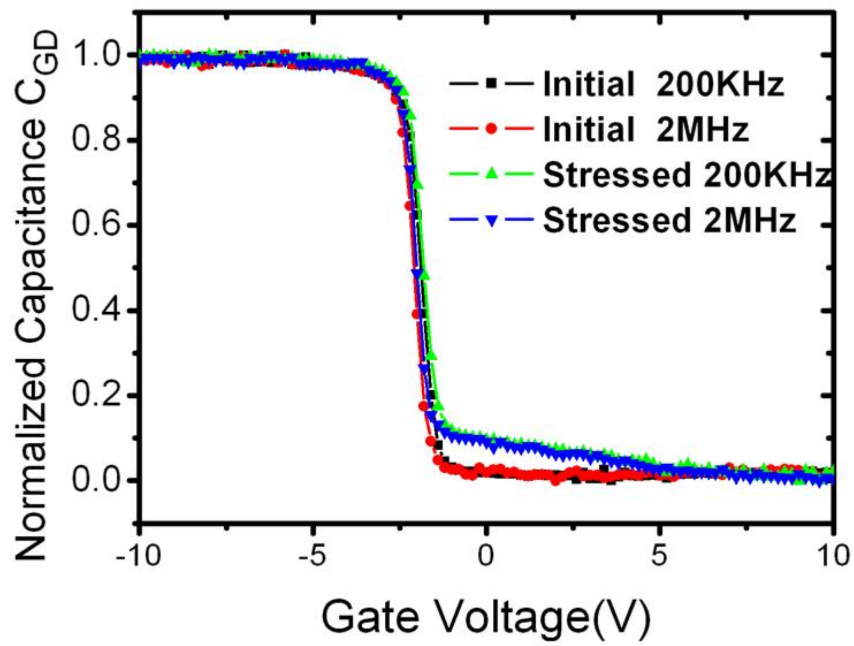


Figure 5-40 Normalized capacitance C_{GD} for the p-type device before and after gate AC stress

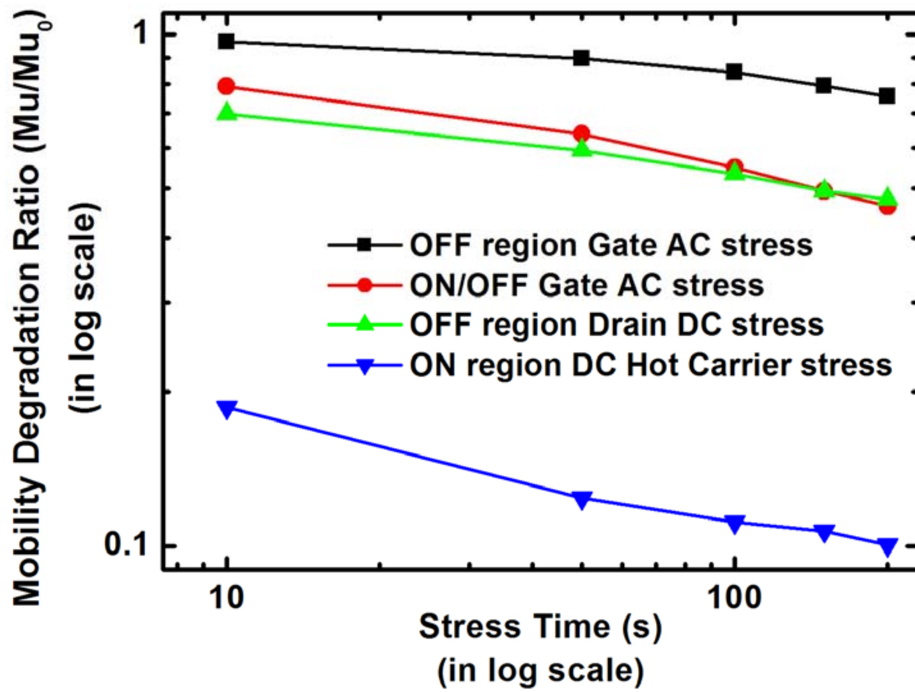
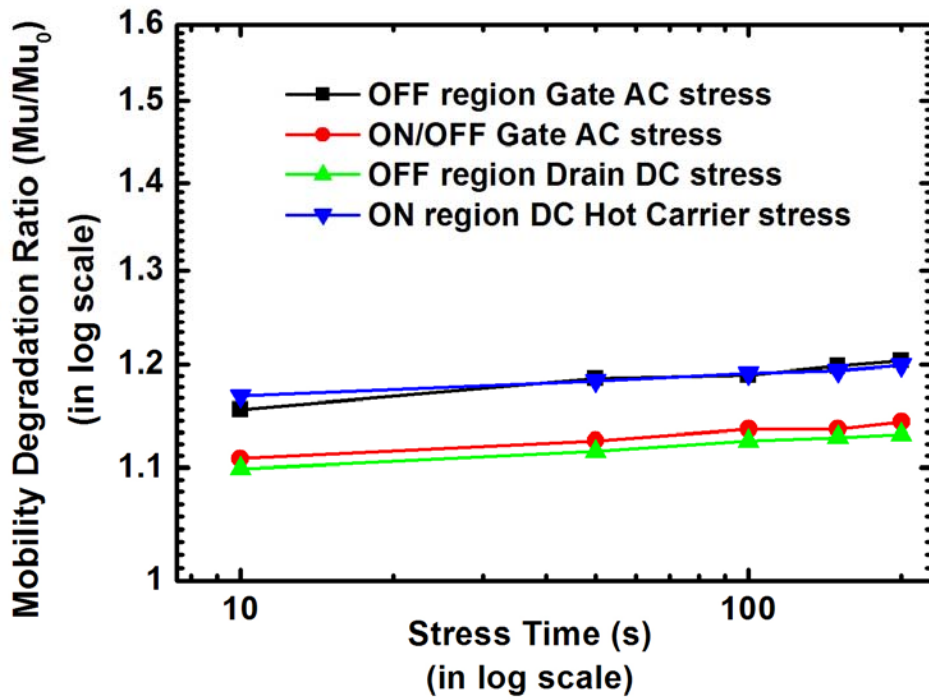


Figure 5-41 Mobility degradation comparison for the n-type devices under various "generalized hot carrier stress" conditions



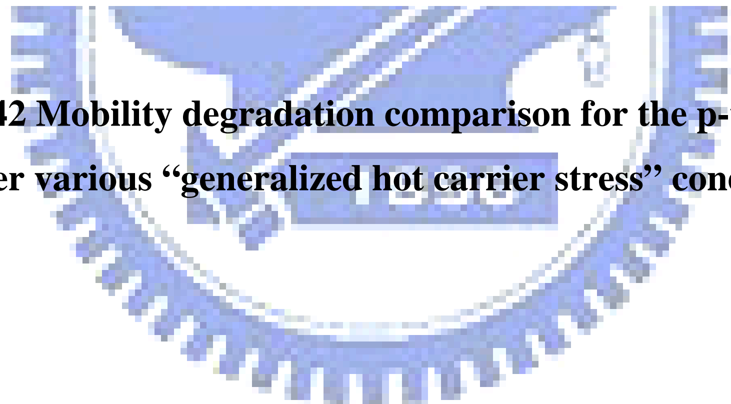


Figure 5-42 Mobility degradation comparison for the p-type devices under various "generalized hot carrier stress" conditions

	For N-type poly-Si TFTs	For P-type poly-Si TFTs
I-V curves	Decreased Mobility and ON current	Increased Mobility and decreased OFF current
C-V curves	Shift and frequency-dependent distortion	Anomalous increase for $\lvert V_G \rvert < \lvert V_{FB} \rvert$
Leveling dependence	Mobility deteriorates more with larger V_G range	Mobility increase more with larger V_G range
Frequency dependence	Mobility deteriorates more with higher frequency	No apparent trend
Duty dependence	Mobility degrades more with smaller V_G duty ratio	Mobility increases more with smaller V_G duty ratio (only for the small duty cycle value)

Table 5-1 The table summarizing the degradation behavior and dependency for the device under gate dynamic operation in the OFF region

Chapter 6

Summaries and Future Work

In previous chapters, the spatial and temporal variation behaviors for the poly-Si TFTs are respectively studied. In chapter 3, the spatial variation is classified and studied from a statistical approach and we utilized the special layout to study to examine the micro variation behavior. The two equations proposed to describe the variation behavior are then put to simulate the effect of device variation on circuit performance and in addition the projected variation behavior for the devices with different device dimension is also discussed. The two equations should be of great help in evaluating the variation behavior since usually in real applications the TFTs in the circuits would be located within several hundred micron meters and thus in this case the micro variation may play an important role in affecting the whole circuit performance. From the viewpoint for the circuit designers, the equations as well as the behaviors about the device variation would be very helpful since after all the over-design may still be required in dealing the variation issue and the designers can at least have a rough picture on how the variation could be and thus the equation discussed in this work should facilitate the design. A possible future work which should also be helpful in designing is the profile of the long-range variation. However, this may required some more help from the production line since in this case the variation may involve some more complicated factors. Besides, it would also be of practical interest to discuss the micro variation behavior with different grain size in the active region.

In chapter 4 the reliability behavior for the device under DC operation is studied and the circuit model is proposed to describe the frequency –dependent distortion for the C-V behavior. Though the model can fairly describe the O. C. region and the S. C.

region, or equivalently the OFF and ON region, there are still some incompleteness for the method. Beside the one drawback mentioned in section 4.4, from the viewpoint of further understanding of the mechanism and the validity of the method, the C-V behavior under the quasi measurement is also of interest. However, the equipment is not so far feasible in our research group and is thus such study may not be applicable. From the viewpoint of device physics, the so-called "high frequency" or "low frequency" should just be one aspect of the trap behavior such as the surface recombination rate and the midgap generation-recombination rate. It would be of practical interest to see if the method can be applied to describe the capacitance behavior for the frequency down to the quasi level.

On the other hand, the device reliability under gate AC operation is studied in chapter 5. The similar model proposed in chapter 4 is again utilized and the junction degradation is found to be responsible for the reliability behavior for the gate AC operation in the OFF region. For the panel designers, it would be of practical importance since the stress condition is actually happening for the real TFT LCD panels. The drain engineering could thus be applied for the reinforcement of the reliability and some kind of the tradeoff could be required between the higher device performance (short LDD length) and the reliability consideration (profiling of the LDD region). One future work for this study is the dependence of the gate pulse parameter, namely the rising time and the falling time, and the device degradation. For the gate and drain signal, some other waveforms of the pulses could also be of practical interest since poly-Si TFTs are expected to form various kinds of circuits and thus the device may need to face some even more complicated operation conditions. Nevertheless, the model and the understanding proposed in this work should still be of great help in the further studying and the future work mentioned above.

References

Chapter 1

[1-1] Yue Kuo, "Thin Film Transistors: materials and processes, volume 1: amorphous silicon thin film transistors," pp.53-56, Springer, 2004

[1-2] Yue Kuo, "Thin Film Transistors: materials and processes, volume 1: amorphous silicon thin film transistors," pp.203-239, Springer, 2004

[1-3] Yue Kuo, "Thin-Film Transistor and Ultra-Large Scale Integrated Circuit: Competition or Collaboration," Japanese Journal of Applied Physics, Vol. 47, No. 3, 2008, pp. 1845–1852

[1-4] David J. R. Cristaldi, Salvatore Pennisi, Francesco Pulvirenti, "Liquid Crystal Display Drivers: techniques and circuits," Springer Science, pp. 149-151, 2009

[1-5] Tohru Nishibe and Hiroki Nakamura "Value-Added Circuit and Function Integration for SOG (System-on Glass) Based on LTPS Technology," SID Symposium Digest of Technical Papers, Volume 37, Issue 1, pp. 1091-1094, 2006

[1-6] Buyeol Lee, Yasuhiro Hirayama, Yasushi Kubota, Shigeki Imai, Akihiko Imaya, Mikio Katayama, Kiyoshi Kato, Akira Ishikawa, Takayuki Ikeda, Yoshiyuki Kurokawa, Tadafumi Ozaki, Kohei Mutaguch, Shumpei Yamazaki, "A CPU on a Glass Substrate Using CG-Silicon TFTs," IEEE International Solid-State Circuits Conference, Vol. 1, pp. 164-165, Feb., 2003.

[1-7] Ya-Hsiang Tai, “Device Variation and Its Influences on the LTPS TFT Circuits,” International TFT Conference (2005).

[1-8] Chein-Wen Lin, "Study on the C-V characteristics for LTPS TFTs under DC stress," master thesis, National Chiao Tung University, 2007

[1-9] Hsiao-Hsien Lin, "Study of LTPS TFTs Degradation under Gate Pulse Stress in OFF Region with Drain Bias," master thesis, National Chiao Tung University, 2007

[1-10] Yukiharu Uraoka, Noboyuki Hirai, Hiroshi Yano, Tomoaki Hatayama, Takashi Fuyuki, "Hot carrier analysis in low-temperature poly-Si TFTs using picosecond emission microscope," IEEE Transactions on Electron Devices, v 51, n 1, p 28-35, January 2004

Chapter 3

[3-1] Yoshiharu Nakajima, Yoshitoshi Kida, Masaki Murase, Yoshihiko Toyoshima, and Yasuhito Maki, "Latest Development of "System-on-Glass" Display with Low Temperature Poly-Si TFT," SID Symposium Digest of Technical Papers, May 2004 , Volume 35, Issue 1, pp. 864-867

[3-2] K. Yoshiyuki, T. Shuichi, and S. Nobuyuki, “A new grain boundary model for drift-diffusion device simulations in polycrystalline silicon thin-film transistors,” Jpn. J. Appl. Phys., Part 2: Lett., vol. 42, no. 6 B, pp. L634–L636, Jun. 2003.

[3-3] A. W. Wang and K. C. Saraswat, “Modeling of grain size variation effects in polycrystalline thin film transistors,” in IEDM Tech. Dig.,1998, pp. 277–280.

[3-4] A. W.Wang and K. C. Saraswat, “A strategy for modeling of variations due to grain size in polycrystalline thin-film transistors,” IEEE Trans. Electron Devices, vol. 47, no. 5, pp. 1035–1043, May 2000.

[3-5] Hye-Hyang Park,Ki-Yong Lee,Kyoung-Bo Kim,Hye-Dong Kim,Ho-Kyoon Chung,"Uniformity improvement of SLS poly-Si TFT AMOLED," Digest of Technical Papers - Proceedings of the 5th International Meeting on Information Display, 2006, p 790-792

[3-6] Chih-Lung Lin,Chun-Da Tu,Tsung-Ting Tsai,"Novel pixel circuit for AMOLED with compensating threshold voltage variation of poly-Si TFTs," International Display Manufacturing Conference and FPD Expo - Proceedings, 2007, p 573-574

[3-7] Cheng-Chiu Pai,Ya-Hsiang Tai, "A new analogue buffer using poly-Si TFTs

with deviation less dependent on the gray level for active matrix displays," Digest of Technical Papers - SID International Symposium, v 36, n 1, AAAI Mobile Robot Competition and Exhibition - Papers from the AAAI-04 Workshop, Technical Report, 2005, p 438-441

[3-8] Ya-Hsiang Tai, Bo-Ting Chen, Yu-Ju Kuo, Chun-Chien Tsai, Ko-Yu Chiang, Ying-Jyun Wei, Huang-Chung Cheng, “A new pixel circuit for driving organic light-emitting diode with low temperature polycrystalline silicon thin-film transistors,” IEEE Journal of Display Technology, v 1, n 1, September, 2005, p 100-103

[3-9] C. Michael and M. Ismail, “Statistical Modeling for Computer-Aided Design of MOS VLSI Circuits,” Amsterdam, The Netherlands: Kluwer Academic, 1993, pp. 8–10.

[3-10] Shih Che Huang, “Statistical Study on the Uniformity Issue of Low Temperature Polycrystalline Silicon Thin Film Transistor,” Master's thesis on Electro-Optical Engineering, National Chiao Tung University, 2005, page 29-30.

[3-11] J. Yamashita, K. Uchino, T. Yamamoto, T. Sasaoka and T. Urabe, "New Driving Method with Current Subtraction Pixel Circuit for AM-OLED Displays", SID Tech. Dig., pp. 1452-1455, 2005.

[3-12] S. J. Ashtiani, P. Servati, D. Striakhilev and A. Nathan, "A 3-TFT Current-Programmed Pixel Circuit for AMOLEDs", IEEE Transactions on Electron Devices, pp. 1514-1518, 2005.

[3-13] Cheng-Ho Yu, Ya-Hsiang Tai, Te-Hung Teng, "Diverse Instability Behaviors for N-Channel Low-Temperature Polycrystalline Silicon Thin Film Transistors," Proceedings of the International Display Manufacturing Conference and Exhibition 2005 (IDMC'05), pp. 503-506

[3-14] J. L. Devore, Probability and Statistics For Engineering and the Sciences, 3rd

ed. Toronto, Canada: Thomson Inf./Publ. Group, 1991, pp.466–468, 489–490.

[3-15] Bastos, J. Steyaert, M. Graindourze, B. Sansen, W, "Matching of MOS transistors with different layout styles," Proceedings of IEEE International Conference on Microelectronic Test Structures, pp.17-18, 1996

[3-16] Ta-Hsun Yeh, Jason C. H. Lin, Shyh-Chyi Wong, Honda Huang and Jack Y. C. Sun, "Mis-match Characterization of 1.8V and 3.3V Devices in 0.18pm Mixed Signal CMOS Technology," Proc. IEEE 2001 Int. Conference on Microelectronic Test Structures, pp.77-82, VoI 14, March 2001.

[3-17] S. M. Sze, "Semiconductor devices: physics andtechnology," John Wiley & Sons, inc., second edition, page 38.

[3-18] Kadaba R. Lakshmikumar, Robert A. Hadaway,Miles A. Copeland, "Characterization and Modeling of Mismatch in MOS Transistors for Precision Analog Design", IEEE Journal of Solid State Circuits, pp. 1057-1066, Vol.SC-21, No.6, December 1986.

[3-19] Chee-Lin Yum, "Statistical evaluation of layout techniques and device size for characterizing the matching behavior of N- and P-channel differential pairs," Bachelor's thesis on Electrical Engineering, University of Southern Maine; 1996.

[3-18] J. H. Park, W. J. Nam, J. H. Lee and M. K. Han, K. Y. Lee, B.D. Choi, K. J. Yoo and H. H. Park, "A Short Channel Effect in Low Temperature Poly-Si Thin Film Transistor for Active Matrix Display," Digest of Technical Papers - SID International Symposium, v 37, n 1, Society for Information Display - 44th International Symposium, Seminar, and Exhibition, SID 2006 - International Symposium Digest of Technical Papers, 2006, p 254-257

Chapter 4

[4-1] Satoshi Inoue, Hiroyuki Ohshima and Tatsuya Shimoda, "Analysis of

Degradation Phenomenon Caused by Self-Heating in Low-Temperature-Processed Polycrystalline Silicon Thin Film Transistors," Jpn. J. Appl. Phys. Vol. 41 (2002) pp. 6313–6319

[4-2] Satoshi Inoue, Mutsumi Kimura and Tatsuya Shimoda, "Analysis and Classification of Degradation Phenomena in Polycrystalline-Silicon Thin Film Transistors Fabricated by a Low-Temperature Process Using Emission Light Microscopy," Jpn. J. Appl. Phys. Vol. 42 (2003) pp. 1168–1172

[4-3] Seok-Woo Lee, HoChul Kang, Kum Mi Oh, Eugene Kim, Soo-Jeong Park, Kyoung Moon Lim, Chang-Dong Kim, and In-Jae Chung, "Analysis of Poly-Si TFTs' Degradation Behavior Induced by DC Stress," Digest of Technical Papers - SID International Symposium, v 36, n 1, AAAI Mobile Robot Competition and Exhibition - Papers from the AAAI-04 Workshop, Technical Report, 2005, p 232-235

[4-4] Glenn O. Workman, Jerry G. Fossum, Srinath Krishnan, and Mario M. Pelella, Jr., "Physical Modeling of Temperature Dependences of SOI CMOS Devices and Circuits Including Self-Heating," IEEE Transactions on Electron Devices, VOL. 45, NO. 1, pp. 125-133, JANUARY 1998

[4-5] Y. Uraoka, K. Kitajima, H. Yano, T. Hatayama, T. Fuyuki, S. Hashimoto and Y. Morita, "Degradation of Low Temperature Poly-Si TFTs by Joule Heating," IEIC Technical Report (Institute of Electronics, Information and Communication Engineers), vol. 104, no 510, pp. 71-76, 2004

[4-6] Julian J . Sanchez, Kelvin K. Hsueh, and Thomas A. Demassa, "Drain-Engineered Hot-Electron-Resistant Device Structures: A Review," IEEE Transactions on Electron Devices. Vol. 36. No. 6. pp. 1125-1132, 1989

[4-7] Yukiharu Uraoka, Tomoaki Hatayama, Takashi Fuyuki, Tetsuya Kawamura and Yuji Tsuchihashi, "Hot Carrier Effects in Low-Temperature Polysilicon Thin-Film Transistors," Jpn. J. Appl. Phys. vol. 40 pp. 2833-2836, 2001

[4-8] Chenming Hu, Simon C. Tam, Fu-Chieh Hsu, Ping-Keung Ko, Tung-Yi Chan, Terrill, K.W., "Hot-electron-induced MOSFET degradation—Model, monitor, and improvement," IEEE Transactions on Electron Devices, Vol. ED-32, No. 2, pp. 375-385, 1985

[4-9] Mitsumasa Koyanagi, Alan G. Lewis, Russel A. Martin, Tiao-Yuan Huang, John Y. Chen, "Hot-electron-induced punchthrough (HEIP) effect in submicrometer PMOSFET's," IEEE Transactions on Electron Devices, Vol. ED-34, No. 4, p 839-844, 1987

[4-10] Kook Chul Moon, Jae-Hoon Lee, Moon-Young Shin and Min-Koo Han, "Observation of electron trapping in p-type polycrystalline silicon thin film transistors due to hot carrier stress employing C-V measurement," 2003 International Workshop on Active Matrix Liquid Crystal Displays (AMLCD '03), pp. 181-184

[4-11] David J. R. Cristaldi, Salvatore Pennisi, Francesco Pulvirenti, "Liquid Crystal Display Drivers: techniques and circuits," Springer Science, pp. 157-158, 2009

[4-12] Ya-Hsiang Tai, Shih-Che Huang, Hao Lin Chiu, "Degradation of capacitance-voltage characteristics induced by self-heating effect in poly-Si TFTs," Electrochemical and Solid-State Letters, Vol. 9, No. 6, p G208-G210, 2006

[4-13] Ya-Hsiang Tai, Shih-Che Huang, Chien Wen Lin, Hao Lin Chiu, "Degradation of the capacitance-voltage behaviors of the low-temperature polysilicon TFTs under DC stress" Journal of the Electrochemical Society, Vol. 154, No. 7, p H611-H618, 2007

[4-14] Tor A. Fjedly, Trond Ytterdal, Michael Shur, "Introduction to device modeling and circuit simulation" p. 165 , John Wiley &Sons, New York (1998).

[4-15] Kook Chul Moon, Jae-Hoon Lee, and Min-Koo Han, "The study of hot-carrier stress on poly-Si TFT employing C-V measurement", IEEE Transactions on Electron Devices, v 52, n 4, April, pp. 512-517, 2005.

[4-16] Ouisse Thierry, Cristoloveanu Sorin, Borel Gerard, “Hot-carrier-induced degradation of the back interface in short-channel silicon-on-insulator MOSFETs”, IEEE Electron Device Letters, v 12, n 6, Jun, pp. 290-292, 1991.

Chapter 5

[5-1] T. Nishibe, H. Nakamura, "Future development of SOG technologies for advanced displays," Proceedings of the 14th International Display Workshops (IDW '07), vol. 2, pp. 495-498, 2007

[5-2] Tohru Nishibe, Hiroki Nakamura, "Value-added integration of functions for silicon-on-glass (SOG) based on LTPS technologies," Journal of the Society for Information Display, vol 15, no. 2, pp. 151-156, February 2007

[5-3] Yoshiharu Nakajima, Yoshitoshi Kida, Masaki Murase, Yoshihiko Toyoshima, Yasuhito Maki, "Latest developments for 'system-on-glass' displays using low-temperature poly-Si TFTs," Journal of the Society for Information Display, vol. 12, no. 4, pp. 361-365, 2004

[5-4] Chun-sung CHIANG, Jerzy KANICKI, and Kazushige TAKECHI, "Electrical Instability of Hydrogenated Amorphous Silicon Thin-Film Transistors for Active-Matrix Liquid-Crystal Displays," Jpn. J. Appl. Phys. Vol. 37 (1998) pp. 4704-4710, September 1998

[5-5] Yukiharu Uraoka, Noboyuki Hirai, Hiroshi Yano, Tomoaki Hatayama, Takashi Fuyuki, "Hot carrier analysis in low-temperature poly-Si TFTs using picosecond emission microscope," IEEE Transactions on Electron Devices, v 51, n 1, p 28-35, January 2004

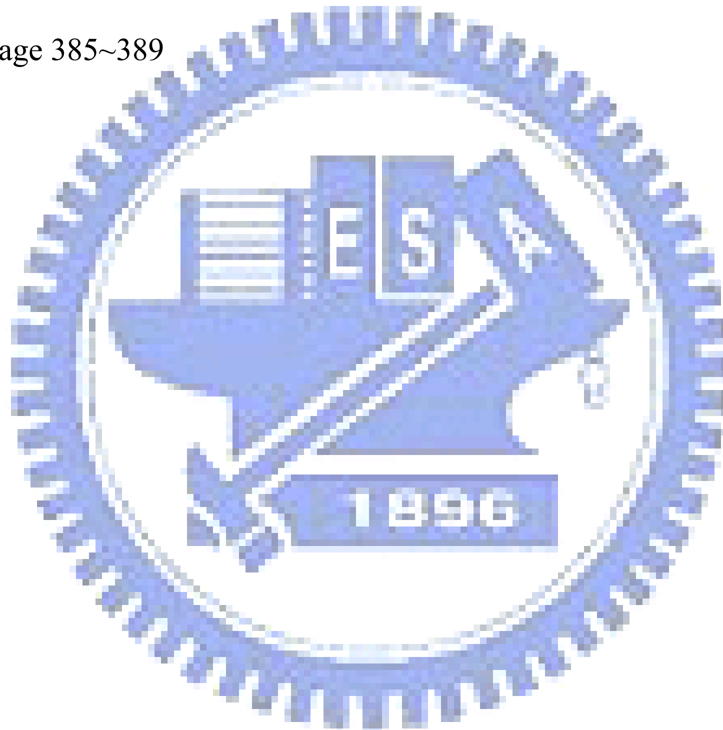
[5-6] Y. Uraoka, N. Hirai, H.Yano, T. Hatayama, T. Fuyuki, "Hot carrier analysis in low-temperature poly-Si thin-film transistors using pico-second time-resolved emission microscope," IEEE Electron Device Letters, v 24, n 4, p 236-238, April

2003

[5-7] Kaoru Kusafuka, Hidehisa Shimizu, Shinichi Kimura, “Driving method of liquid crystal display device,” US patent 5995074, 1999

[5-8] Mitsumasa1 Koyanagi, Alan G. Lewis, Russel A. Martin, Tiao-Yuan Huang, John Y. Chen, "Hot-electron-induced punchthrough (HEIP) effect in submicrometer pMOSFET's," IEEE Transactions on Electron Devices, vol. 34, no. 4, pp. 839-844, April 1987

[5-9] Ben Streetman, Sanjay Banerjee, "Solid State Electronic Devices," Prentice Hall; 5th edition, page 385~389



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多晶矽薄膜電晶體的空間與時間變動性探討

Characterization of the Spatial and Temporal Variation of Poly-Si TFTs

Publication List

1. International Journals

[1] Ya-Hsiang Tai, **Shih Che Huang**, and Hao Lin Chiu, “Degradation of Capacitance -Voltage Characteristics Induced by Self-Heating Effect in Poly-Si TFTs,” *Electrochemical and Solid-State Letters*, vol. 9, num. 6, pp. 208-210, 2006.

[2] **Shih-Che Huang**, Yu-Han Kao, Ya-Hsiang Tai, “Study on electrical degradation of p-type low-temperature polycrystalline silicon thin film transistors with C–V measurement analysis,” *Thin Solid Film*, 515 (2006) 1206–1209

[3] **Shih-Che Huang**, Yen-Pang Chou, Ya-Hsiang Tai, “Statistical study on the states in the low-temperature poly-silicon films with thin film transistors,” *Thin Solid Film,* 515 (2006) 1210–1213

[4] Ya-Hsiang Tai, **Shih-Che Huang**, Chien-Kwen Chen, “Analysis of Poly-Si TFT Degradation Under Gate Pulse Stress Using the Slicing Model,” *IEEE Electron Device Letters*, Vol. 27, No. 12, December 2006, pp. 981-983

[5] Ya-Hsiang Tai, **Shih-Che Huang**, Chien Wen Lin, and Hao Lin Chiu, “Degradation of the Capacitance-Voltage Behaviors of the LTPS TFTs Under DC Stress,” *Journal of The Electrochemical Society,* vol.154, num7, page H611-H618 ,2007.

[6] Ya-Hsiang Tai, **Shih-Che Huang**, Wan-Ping Chen, Yu-Te Chao, "A Statistical Model for Simulating the Effect of LTPS TFT Device Variation for SOP Applications," *Journal of Display Technology,* VOL. 3, NO. 4, page 426-433, 2007.

[7] **Shih-Che Huang**, Ya-Hsiang Tai, "Characterization of poly-Si TFT variation using interdigitated method," *Solid-State Electronics,* vol. 52 (2008) page 1170–1176

[8] Ya-Hsiang Tai, **Shih-Che Huang**, Ko-Ching Su, Chen-Yeh Tseng, "Variation and mismatch effects of the low-temperature poly-Si TFTs on the circuit for the X-ray

active matrix sensor," *Solid-State Electronics*, vol. 52 (2008) page 649–656

[9] Ya- Hsiang Tai, Ming-Hsien Tsai, and **Shih-Che Huang**, "The Linear Combination Model for the Degradation of Amorphous Silicon Thin Film Transistors under Drain AC Stress," *Japanese Journal of Applied Physics*, Vol. 47, No. 8, 2008, pp. 6228–6235

[10] Ya-Hsiang Tai, **Shih-Che Huang**, and Po-Ting Chen, "Degradation Mechanism of Poly-Si TFTs Dynamically Operated in OFF Region," IEEE Electron Device Letters, Vol. 30, No. 3, MARCH 2009, pp.231-233

[11] Ya-Hsiang Tai, **Shih-Che Huang**, and Po-Ting Chen, "Characterization of the Channel Shortening Effect on P-type Poly-Si TFTs," *submitted to IEEE Transactions on Device and Materials Reliability.*

2. International Conferences

1. **Shih-Che Huang**, Guo-Feng Peng, Jyh-Long Chern, Ya-Hsiang Tai, "Statistical Investigation on the Variation Behavior of Low-Temperature Poly- Si TFTs for Circuit Simulation ," *Society for Information Display symposium (SID)*, 2006, pp.329-332

2. **Shih-Che Huang**, Yu-Han Kao, Ya-Hsiang Tai, "Study on electrical degradation of p-type low-temperature polycrystalline silicon thin film transistors with C–V measurement analysis," *International Conference on Metallurgical Coatings and Thin Films, (ICMCTF)*, 2006, pp.108

3. **Shih-Che Huang**, Yen-Pang Chou, Ya-Hsiang Tai, "Statistical study on the states in the low-temperature poly-silicon films with thin film transistors," *International Conference on Metallurgical Coatings and Thin Films (ICMCTF)*, 2006, pp.109

4. Fu-Chi Chang, **Shih-Che Huang**, Ya-Hsiang Tai, "Verification on the Range Effect of the Device Variation on LTPS TFT Circuit Performance Using Ring

Oscillator," *International Electron Devices and Materials Symposia (IEDMS)*, 2006, pp.463-464

5. **Shih-Che Huang**, Hung-Chuan Tsao, Ya-Hsiang Tai, "Analysis of P-type Poly-Si TFT Degradation Under Dynamic Gate Voltage Stress Using the Slicing Model," *Asia Display,* 2007, pp.557-561. (Oral)

6. Yan-Fu Kuo, **Shih-Che Huang**, Wei-Lun Shih, Ya-Hsiang Tai, "Dynamic stress effects on the reliability of Poly-Si TFT," *International Display Manufacturing Conference and Exhibition (IDMC) 2007*, pp.497-499.

7. Yan-Fu Kuo, **Shih-Che Huang**, Yu-Te Chao, Ya-Hsiang Tai, " Capacitance-Voltage Behaviors of the LTPS TFTs Before and After DC Stress Explained by the Slicing Model," *International Display Manufacturing Conference and Exhibition (IDMC) 2007*, pp.523-525.

8. **Shih-Che Huang**, Hung-Chuan Tsao, and Ya-Hsiang Tai, "Estimation of the Effect of Channel Shortening for P-Type Poly-Si TFTs Under AC Stress," *International Display Manufacturing Conference and Exhibition (IDMC) 2007*, pp.134-137. (Oral)

9. Ya-Hsiang Tai, **Shih-Che Huang** and Chang-Lung Chan, "Characterization of Device Degradation of Poly-Si TFTs Under Dynamic Operation with Drain Biased," *IEEE International Reliability Physics Symposium (IRPS) 2008*, page 709-710

3. Domestic Journals

1. 黃士哲, "多晶矽薄膜電晶體在顯示器系統設計上的挑戰," 電子月刊, 2006 July.

2. 黃士哲, "低溫多晶矽薄膜電晶體的變動特性及其在OLED畫素驅動電路的影響," 化合物半導體&光電技術, 2007 Feb.

3. 黃士哲, "低溫多晶矽薄膜電晶體在顯示器系統的可靠度行為," 電子月刊, 2008 July