國立交通大學

光電工程研究所

博士論文

有機薄膜電晶體與非晶矽薄膜電晶體在偏壓與光照下之可靠度分析

Bias-Stress Effect and Photo-Irradiation Effects in Organic and a-Si:H Thin Film Transistors

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A Thesis Submitted to Institute of Electro-Optical Engineering National Chiao Tung University in partial Fulfillment of Requirements for the Degree of Ph.D. in Electro-Optical Engineering

January 2010

Hsinchu, Taiwan, Republic of China

中華民國九十九年三月

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國立交通大學光電工程研究所博士班

摘 要

在論文中,我們探討了低溫製程下有機薄膜電晶體和非晶矽薄膜電晶體的可靠度問題。首先在有機薄膜電晶體的部份,元件在偏壓下以及照光下的劣化機制被深入的探討。在直流偏壓的實驗中,我們首次發現利用汲極電壓調整通道載子濃度,元件臨界電壓漂移量和通道中累積的載子濃度成正比,我們並修改了舊有的偏壓壓力(Bias Stress)模型,使模型可以完整呈現閘極和汲極電壓對有機薄膜缺陷產生機制以及元件臨界電壓的影響。在交流偏壓的實驗中,我們發現臨界電壓漂移量會受施加偏壓的頻率所影響,負閘極偏壓的頻率效應可以用元件通道累積電洞的反應時間來解釋,等效電路模型和非晶矽薄膜電晶體使用的相同。在更進一步的研究中,我們探討絕緣層表面狀態以及環境對於元件可靠度的影響。從實驗結果中我們發現,利用具有氫氧基的絕緣層製作出來的元件在含水氣的環境中,元件劣化速度是較快的。另外,也發現五苯環素薄膜電晶體通道中可移動的電子,並非由汲極源極注入,而是由環境光或是因有機介電層中的氫氧基與水氣反應所提供。最後,我們探討元件照光的反應以及五苯環素光電晶體的光偵測能力。實驗中發現光引起的電子濃度是可以由電場來控制且也可以利用電場來增加有機薄膜中的光致電子電洞對,我們稱此效應為光電場效應。我們利用此光電場效應來增強元件對光的靈敏度,也詳細探討光強度、電場強度、元件尺寸等參數對光靈敏度以及測光時可偵測範圍(detectable range)的影響。利用光電場效應可以使五苯環素電晶體在藍光下的光響應高達 92 A/W。

在非晶矽薄膜電晶體的部份，我們量測並分析由工研院製作在軟板上的低溫非晶矽薄膜電晶體，元件是製作在聚亞醯胺薄膜上且製程溫度在 160 °C 之下。元件的基本電特性與傳統溫度下(300 ~ 350 °C)製作出來的元件並無太大差異，只有元件的可靠度受低溫沉積的影響而下降。在我們的研究中首度發現，同時施加長時間閘極和汲極偏壓後，元件的臨界電壓漂移會隨通道寬度變大而增加且會使可靠度模型失效。這是因為元件產生了自我加熱的效應，導致元件通道中的溫度上升，當使用導熱差的塑膠基板時，自我加熱效應比玻璃基板上更為嚴重，我們也延伸可靠度模型來萃取等效的通道溫度，並和傳統的自我加熱模型計算出的溫度比較，傳統的等效熱電阻模型並無法解釋臨界電壓漂移與通道寬度的關係，因為熱對流以及熱輻射等散熱方式並沒有被傳統的等效熱電阻模型考慮。因此，我們利用可靠度模型來推估元件通道溫度，此方法不需要建立複雜的等效電路與量測材料的熱特性，而且，此方法首度探討並解釋了自我加熱效應和偏壓壓力效應的交互影響。最後，我們首度將元件置放在彎曲的載台上進行量測並觀察其自我加熱效應，我們發現若沒有自我加熱效應產生，則元件可靠度不受彎曲影響；若有自我加熱效應產生時，可靠度會隨彎曲程度增強而劣化。這可能是因為薄膜內的矽氫鍵結在有應力情況下變得較脆弱，自我加熱效應會使這些較脆弱的鍵結斷裂，使缺陷態更容易產生。

Bias-Stress Effect and Photo-Irradiation Effects in Organic and a-Si:H Thin Film Transistors

Student: Shih-Chin Kao Advisor: Hsiao-Wen Zan

Degree of Ph.D. in Electro-Optical Engineering

Abstract

In this thesis, the reliability issues of low-temperature process organic-based TFTs and a-Si:H TFTs are discussed. Firstly, for organic-based TFTs, the degradation mechanisms of device under bias stress or under prolonged illumination are carefully investigated. In the steady-state bias stress experiment, we use drain bias to adjust the carrier concentration in the channel and find that the accumulated carrier concentration is proportional to the threshold voltage shift. This verifies the relationship between the defect generation and the accumulated carrier concentration in organic thin film for the first time. In the pulsed bias stress experiment, under positive and negative bias, the threshold voltage shifts have the different pulse width dependence. These results show that there is obvious difference in hole and electron accumulation rates. On the other hand, the influences of dielectric surface states and environmental conditions on the reliability of device are studied. Based on the experimental result, the device fabricated on the dielectric with hydroxyl groups in the moisture environment has more serious reliability issues. Additionally, since electron injection from Au to pentacene is difficult, it is found that the accumulated electrons are provided from light-induced electrons or from the negative-charge states produced when OH groups react with moisture. Finally, the influence of illumination on OTFT and pentacene-based organic phototransistors (OPTs) are studied. Using bias to adjust the channel carriers can control the light-induced threshold voltage shift. Also, electric field is found to enhance the dissociation of light-induced excitons. This is named as

the photoelectric field effect in this dissertation. We use the photoelectric field effect to enhance the sensitivity of OPTs for the first time. We also investigate the influence of light intensity, wavelength, bias, channel dimension, and illumination time on the light-induced threshold voltage shift. Under blue light illumination, the photoresponsivity of pentacene-based TFTs reaches 92 A/W using the photoelectric field effect.

For a-Si:H TFTs, we analyze devices fabricated by Industrial Technology Research Institute, Taiwan. Devices are fabricated on polyimide substrate and process temperature is kept at 160 ^{o}C. The basic device parameters such as mobility, threshold voltage and threshold slope do not differ from device fabricated in the conventional process temperature but the reliability issue becomes more serious. In our studies, after applying simultaneous gate and drain bias stress, it is found that the threshold voltage shift has the channel width dependence and can not accurately predicted by the original reliability model due to the self-heating effect. According to the equivalent thermal resistant circuit, when changing glass substrate to polyimide substrate, the smaller thermal conductivity of polyimide substrate cause the low cooling capacity to accumulate higher channel temperature. We also firstly observe a relationship between the self-heating effect and the bias-stress effect, particularly when devices have wide channel width. Conventional thermal resistant circuit can not explain the channel width dependence. Therefore, we use the reliability model to fit the experimental data and extract the effective channel temperature. This is a new methodology to discuss the self-heating effect without calculate detailed thermal resistance model or simulate thermal flow of devices. Finally, we also firstly find that tensile stress may further accelerate the generation of defects when self-heating effect occurs.

誌謝

從 2003 年暑假尾聲中，敲下門的那一刻起到現在，我的研究生活已經到達尾聲即將要進入另一個人生旅程中的新階段。在這研究生活的時光中，有歡樂也有難過的事情，雖然不是精采與充滿掌聲的旅程，但我的內心卻是充實的且在這期間所發生的種種事情都已深刻地烙印在我的回憶中。在此感謝我的指導教授–冉曉雯老師，在她細心的教導中學習如何做研究，且以嚴謹的態度來求證假設和不厭其煩的指導我論文上的缺失。因此在這一個這麼好的研究環境下，我的論文才得以完成。也要感謝孟心飛老師能夠提供許多的寶貴見解，使得此論文能夠更為完整。另外要特別感謝顏國錫學長，他以認真且嚴謹的態度努力地從事研究工作是在我博士班中學習的典範。

在博士班的生涯中，感謝學弟鄭庭軒，在我還是博士新生時與我辛苦地建立研究方向。也要謝謝學弟：潘皇維、歐陽祥睿和孟繁琦與我一起努力從事研究。以及還要感謝博士班同學陳蔚宗，周政偉，黃士哲，盧贊文，鄒一德，陸亭州，黃彥棠和蔡武衛給予我許多研究上的建議以及實驗上的幫助。在這四年半的時間中，要謝謝邵而康、王志宏、邱育敏、吳文馨、王光明、涂廷遠、高德倫、顏睿志、梁芸嘉、方俊傑、吳權陵、顏志宇、姜鈞銘、姜淑鈴、許庭毓、薛琇文、羅世益、古明哲和陳家新等學弟，讓原本苦悶的研究生活轉變為充滿歡樂與活力。此外，我也要感謝工研院的學長們黃俊杰和胡國仁等，提供我許多不管是製程技術上或是學業上的幫助，得以豐富了我的論文內容。

在這漫長的求學過程中，感謝我的父母提供我一個無後顧之憂的生活，讓我專心地讀書以及做研究，也謝謝我的弟弟和妹妹在此期間常常到新竹來陪伴我，讓我深深感受到家人的關懷。在這裡，我想對我的家人、老師們和學長學弟們說，要是沒有妳們的幫忙與協助就沒有現在的我，真是謝謝你們。

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Chapter 1

INTRUDUCTION

1-1 Introduction

In resent years, flexible displays are of great interest especially for mobile applications. Because flexible substrates can not sustain high temperature process temperature, the development of low-temperature process of electronic transistor is necessary. Amorphous silicon (a-Si) and organic materials are promising to fabricate electronics on flexible substrates. The flexible displays have been demonstrated that a-Si thin film transistor (TFT) and organic-based thin film transistor (OTFT) arrays combine with OLEDs, LCDs, and EPDs as shown in Fig. 1-1 (a), (b) and (c) [1-3]. Flexibility can render the display to have new properties such as bendable, rollable, and elastically stretchable. However, lowering temperature process usually affects the stability of electronics. And, the solution process used in OTFT fabrication usually cause residual hydroxyl groups or water molecule in the electrons to lower the lifetime of product.

In this thesis, the reliability issues of OTFTs are studied in steady-state and dynamic operation bias and in different environments. Finally, the self-heating effect of a-Si TFT fabricated on the polyimide substrate is studied.

1-2 Overviews of Organic-Based Thin Film Transistors

Organic thin-film transistors (OTFTs) have received great attention due to their low-cost and large-area array application. In 1960, using small-molecule organic material, condensed hydro-carbons and dyes, successfully fabricated the field effect transistor. However, their semiconductor characteristics were poor and their reproducibility very low, which caused large difficult to develop any real devices. A relatively minor fundamental interest was maintained in organic materials until the 1970s, when the first world energy crisis launched a renewed interest in organic-based semiconductor, aimed at the development of cheap, flexible, large-area organic-based solar cells. However, after a decade of intense research, both in universities and in private enterprise, results showed that organic semiconductors suffer from severe limitations, linked to the existence of a very high density of defects and traps, as well as to very low carrier mobility. Although significant experimental effort was invested during the 1980s, the inability to increase significantly the carrier mobility above this low value of about 10^{-4} cm^2/Vs led many research groups to question the real potential of organic-based semiconductors for use as active layers in electronic devices. Until 1990s, short conjugated oligmoer and sexithiophene showed the mobility of the order of 10^{-1} cm^2/Vs, almost matching that of a-Si:H TFTs.

To date, the performance of organic thin-film transistors (OTFTs) has been obviously improved by the application of new organic channel compounds and advanced fabrication process. In 2000, field-effect mobility and I_{on}/I_{off} of pentacene-based TFTs had reached 3.2 $cm^2V^{-1}s^{-1}$ ratio and $>10^9$ were demonstrated. Because the large barrier between Au and pentacene blocks electron injection from contact into the channel, the channel of OTFT is usually P-type. Fig. 1-2 (a) Pentacene is made up of five benzene rings (b) a single pentacene molecule ($C_{22}H_{14}$) consists of 5 benzene rings. In each molecule 14 of the 22 C atoms are bonded to two other C atoms and to one hydrogen atom. The four inequivalent H atoms are numbered 1–4. Other H atoms are related by symmetry. (c) A single $C_{22}H_{16}$ molecule (dihydropentacene) is shown here. The two C-H_2 units are positioned on sites 1 and 8 [4].

More recently, displays have been made on OTFT backplanes on flexible polymeric substrates. OTFT arrays to drive liquid crystal (LC) [2] [5] or organic light emitting diode (OLED) [6] which showed full-color moving pictures had been demonstrated. In these reports, OTFTs are encapsulated by passivation layer to avoid exposing to oxygen or moisture in air, and to avoid damage from the subsequent LC or OLED process. When flexible substrates are substituted for conventional glass substrate, the general products can have new application and for different usage as rollable light-weight displays or environmental sensor integrated into clothing or irregular surface of consumer electronics. In particular, organic materials can be deposited at room temperature by spin coating, or by roll-to-roll technology compatible with ink-jet printing. Compared with conventional instruments for fabricating inorganic electric devices, spin coating and roll-to-roll technology can provide low-cost fabrication process due to the lower requirements in vacuum. Because the roll-to-roll technology has high-throughput, the fabrication cost of organic electronic devices on flexible substrates can be further reduced. Here, a roll of thin plastic or metal foil used as the substrate can be kilometers long and meters compared to the glass size of 10 generation about 3 m × 3 m in a flat-panel display (FPD) manufacturing process.

Although the field-effect mobility of organic electric device is already comparable to that of hydrogenated amorphous silicon (a-Si:H), the carrier transport in organic semiconductors, such as pentacene, is sensitive to contamination and is strongly interface-dependent. However, there is difficult to fabricate the very smooth morphology of gate dielectric surface and the uniform of surface state for the large substrate. In the other hand, these organic materials are still sensitive to moisture in ambient air and need superior passivation to cover the organic active layer. Thus, inorganic and organic passivation thin-film technology still has to be further studied.

In previous reports, OTFTs are encapsulated by passivation layer to avoid exposing to oxygen or moisture in air, and to avoid damage from the subsequent LC or OLED process. However, even when devices are encapsulated or operated in an inert environment, OTFTs are known to suffer from bias stress effect (BSE) that causes significant threshold voltage shift.

The bias-stress effect in OTFTs had been studied by using different organic active materials or different gate insulators on different device structures [7]. It was found that, for p-type OTFTs under steady-state bias stress, positive gate bias stress caused a positively-shifted threshold voltage (V_{th}) and negative gate bias stress caused a negatively-shifted V_{th}. The BSE was reversible by removing gate bias or by applying opposite polarity gate bias. Light irradiation also enhanced the reversal process. However, the prolong illumination causes a positively-shifted V_{th}. due to trapping light-induced electrons.

Charge trapping, ion migration, charged-state creation and the formation of bound hole pairs (bipolaron) are several proposed mechanisms to explain the BSE [8]. Charge trapping and ion migration were found to be dominant mechanisms in OTFTs with an organic dielectric [9]. When using thermally-grown SiO_2 as the gate dielectric to study OTFTs reliability, charged-state creation is usually believed to be responsible for the threshold voltage shift (ΔV_{th}). John E. Northrup and Michael L. Chabinyc used density functional calculation to simulate defect states generation in pentacene film and found that it was due to the formation of oxygen- and hydrogen-related defects such as $C\text{-}H_2$, OH, and C-HOH in organic semiconductors [10]. Gu *et al.* also studied the response time of the defect states in pentacene. Long-lifetime deep electron traps were proposed to explain the hysteresis effect in pentacene-based OTFTs.

In this thesis, the reliability issues of pentacene-based OTFTs are studied and discussed in the following separated chapters.

1-2-1 Fundamental Transport Mechanism of OTFTs

Band transport mechanism in disordered organic semiconductors dominated by hopping between localized states and carriers are scattered at every step. Hopping is assisted by phonons and mobility increases with temperature, although it is very low overall ($\mu_{EF} << 1$ cm^{2}V^{-1}s^{-1}). The boundary between band transport and hopping is defined by materials having mobilities between 0.1 and 1 cm^{2}V^{-1}s^{-1} [11, 12, 13]. Highly ordered organic semiconductors, such as several members of the acene series including anthracene and pentacene have room temperature mobilities in this intermediate range, and in some cases temperature-independent mobility has been observed [12], even in polycrystalline thin films of pentacene [13]. That observation was used to argue that a simple temperature-activated hopping mechanism can be excluded as a transport mechanism in high-quality thin films of pentacene [13]. At low temperatures (below approximately 250 K), band transport becomes the mechanism that takes control of carrier transport in single crystals of pentacene and other acenes. Very high mobility values (from 400 cm^{2}V^{-1}s^{-1} [14] to more than 1000 cm^{2}V^{-1}s^{-1} [15]) have been reported. At these temperatures, the vibrational energy is much lower than the intermolecular bonding energy and phonon scattering is very low; thus, high mobility is exhibited. At or close to room temperature, phonon scattering becomes so high that the contribution of the band mechanism to transport becomes too small. At these same temperatures, hopping begins to contribute to carrier transport. Hopping of carriers from site to site becomes easier as the temperature rises. The combination of these two mechanisms explains the fact that the mobility decreases as temperature rises from a few degrees K to about 250 K, and after that the mobility begins to rise slowly [14].

1-2-2 Parameters in Transfer Characteristics of OTFTs

A thin film transistor is composed of three basic elements: (1) a thin semiconductor film; (2) an insulating layer; and (3) three electrodes (source, drain and gate). Fig.1-3 show two kinds of standard OTFT device structure Fig. 1-3(a) is the top-contact device and Fig. 1-3(b) is the bottom-contact device, respectively. The general operation concepts are originated from MOSFET theory. But there is a slight difference, traditional MOSFET are usually operated in inversion mode while the OTFTs are generally operating in accumulation mode. Since the pentacene thin film is a p-type semiconductor due to the characteristic of Au/pentacene contact barrier, the pentacene-based channel is turned on when negative gate bias is applied. The bias-drop across gate dielectric causes the downward energy band bending in the pentacene film near the gate electrode and additional positive charge carriers will accumulate at the interfaces. The gate dielectric is served as a capacitance and can store charges. Applying a drain bias causes a voltage potential difference in the channel and drives the accumulated free carriers to form the drain current.

As shown in Fig. 1-4, the LUMO level of pentacene is quite far away from the Fermi level of gold, so there is a substantial energy barrier for electrons and electron injection is very unlikely. Accordingly, no current passes through the pentacene layer. in contrast, when the gate voltage is reversed to negative, holes are easily injected because the Fermi level is close to the HOMO level and the barrier is low. a conducting channel forms at insulator-semiconductor interface and charge-carriers can be driven from source to drain by applying a second, independent, bias to the drain. Because holes are more easily injected than electrons, pentacene is said to be p-type. Symmetrically, an organic semiconductor is said to be n-type when electron injection is easier than hole injection, which occurs when the LUMO is closer to the Fermi level than the HOMO.

In order to comparing the performance of different organic-based TFTs, the field-effect mobility (μ_{EF}), threshold voltage (V_{th}) and subthreshold slope ($S.S.$) are usually served as metric units.

Field-Effect Mobility (μ_{EF}):

The μ_{EF} can be extracted from the device drain current by using the general MOSFET drain-current equation.

In linear region ($V_{GS} - V_{th} > V_{DS}$):

$$I_{DS} = \frac{W}{L}\mu_{FE}C_{ox}\left[\left(V_{GS}\text{-}V_{th}\right)V_{DS}\text{-}\frac{V_{DS}{}^{2}}{2}\right] \tag{1-1}$$

when V_{DS} is small ($V_{GS} - V_{th} >> V_{DS}$), Eq. (1-1) can be reduced to

$$I_{DS} = \frac{W}{L}\mu_{FE}C_{ox}\left(V_{GS}\text{-}V_{th}\right)V_{DS} \tag{1-2}$$

In saturation region ($V_{GS} - V_{th} < V_{DS}$)

$$I_{DS} = \frac{W}{L}\frac{\mu_{FE}C_{ox}}{2}\left(V_{GS}\text{-}V_{th}\right)^{2} \tag{1-3}$$

where V_{th}, W, L and C_{ox} are the threshold voltage, the channel width, the channel length and the gate dielectric capacitance per unit area.

In linear region, mobility is defined as

$$\mu_{FE,\ linear} = \frac{L}{WC_{ox}V_{DS}}\frac{\partial I_{DS}}{\partial V_{GS}} \tag{1-4}$$

In saturation region, mobility is defined as

$$\mu_{FE,\ sat} = \frac{2L}{WC_{ox}}\left[\frac{\partial\sqrt{I_{DS}}}{\partial V_{GS}}\right]^{2} \tag{1-5}$$

The field-effect mobility (μ_{EF}) is distinct from the more physically fundamental carrier mobility (μ), which has the same units but relates average carrier velocity v to applied electric field E. The field-effect mobility (μ_{EF}) is easily affected by additional effects such as parasitic resistant, carrier scattering and current crowding. However, the field-effect mobility (μ_{EF}) can be immediately and simply extracted from the transfer characteristic when sweeping a range of gate bias at a specified drain bias.

Therefore, using μ_{EF} as metric unit is convenient than extracting (μ).

Threshold Voltage (V_{th}):

The threshold voltage can be extracted from the transfer characteristic in the linear region by plotting I_{DS} versus V_{GS} for small drain voltages ($V_{GS} - V_{th} > V_{DS}$), and extrapolating the line to I_{DS} =0. Fig. 1-5 shows the transfer characteristic in the linear region. Similarly, the threshold voltage can be extracted from measurements in the saturation region by plotting $\sqrt{I_{DS}}$ versus V_{GS} and extrapolating to I_{DS} =0.

Threshold voltage of pentacene-based TFTs is usually large and uncontrolled, and values as high as tens of volts. Until now, the large V_{th} can not be clearly explained. However, it is believed that the high density of trapped charge consists at the interface between pentacene film and gate dielectric. For electronic applications, a large threshold voltage causes the power waste and needs larger drive bias to lead to the bias stress effect. To date, some groups successfully use self-assembled monolayer to modify or lower the defect density on the dielectric surface and obtain lower V_{th}. Using higher dielectric constant material as gate insulator also can reduce the threshold voltage.

Subthreshold Slope (*S.S.*):

Based on the simplified physical models underlying Eq. 1-1 and 1-3, the drain current is zero when applied gate bias (V_{GS}) is smaller than threshold voltage (V_{th}). Actually, these two equations can not correctly represent the drain current in the subthreshold region. When device is switched from off-state to on-state in the subthreshold region, the power-law dependence between the drain current increase and the gate bias is found. The general current equation in the subthreshold region can be expressed as:

$$I_{DS} = \frac{W}{L} K \mu_{FE} C_{ox} \left(1\text{-}e^{\frac{-qV_{DS}}{kT}} \right) e^{\frac{qV_{GS}}{nkT}} \tag{1-6}$$

Fig. 1-6 shows that the subthreshold region of the transfer characteristic and a straight line through the subthreshold region. The slop of a straight line is relative to the interface state between pentacene film and gate dielectric. Therefore, the inverse of the subthreshold slope usually represents the behavior of subthreshold region. The inverse of the subthreshold slope also is named as the subthreshold swing and expressed as

$$S.S. = \left(\frac{\partial log I_{DS}}{\partial V_{GS}} \right)^{-1}$$

where the units used for subthreshold slope (*S.S.*) are volts/decade that represents the increment in gate voltage needed to change the drain current by a factor of 10.

1-2-3 Hysteresis of OTFTs

Hysteresis, or memory effects is often observed in the transfer characteristics of organic-based TFTs. Hysteresis refers to short-term reversible shifts that lead to looping in the measured characteristics, depending on which direction the bias voltages are swept in. There are usually three mechanisms to explain the hysteresis in p-type organic-based TFT: (1) slow polarization of the gate dielectric, (2) charge storage in the dielectric, and (3) electron trapping in the semiconductor. (1) and (2) mechanisms are dominated by the gate dielectric quality. Mechanism (1) describes that when dipolar groups or molecules consists in a polymer gate dielectric, applied gate electric field cause slow reorientation in dipolar groups or molecule. In this case, hole carriers can not be immediately accumulated in the channel after changing gate bias. The slow accumulation rate leads to hysteresis in the transfer curves. If mechanism (2) dominates the hysteresis, the loop direction can be clockwise and anticlockwise depending on the sign and location of the injected and stored charge. Therefore, using the loop direction is difficult to differentiate between mechanism (1) and (2). However, when the injected and stored charge existed in the gate dielectric, the gate leakage current is usually affected and the abnormal gate leakage current can represent the mechanism (2). When organic thin film is deposited on the thermally grown silicon dioxide (SiO_2) gate dielectric, mechanism (1) and (2) can be excluded to lead to hysteresis. The hysteresis is induced by trapping electrons in the organic thin film. The electron trap states in the semiconductor are quickly filled and slowly released. When sweeping gate bias from positive to negative bias, initial positive gate bias attracts electron accumulated in the channel and the electron traps are filled. Then, when changing positive gate bias to negative, from off to on, hole carriers are accumulated in the channel and trapped electrons with slow release rate induce extra holes. Extra hole carriers lead to extra drain current during the off-to-on sweep. If changing gate bias sweep direction, on-to-off, there are no trapped electrons to cause extra hole carriers. Therefore, the field-effect mobility (μ_{EF}) and threshold voltage (V_{th}) are dependent on the direction of sweeping gate bias.

1-2-4 Threshold Voltage Shift Mechanism of OTFTs

The ΔV_{th} of OTFTs is believed due to the carrier trapping by the defect states. However, there are only a few explanations on the micro process of the defect creation, which can be observed in bias stress experiment. Bias tress experiment can be divided into two kinds: negative bias stress and positive bias stress.

Firstly, micro process of defect creation under negative bias stress is introduced. The formation of bipolaron proposed by R. A. Street et al. [8] is one of the plausible mechanisms. The deep states slowly trap holes to form bipolarons. The formation of bipolarons would cause the ΔV_{th} due to the reduction of mobile holes. The reaction can be expressed as:

$$h + h \rightarrow (hh)_{BP}$$

The other possible mechanism was proposed by John John E. Northrup et al. [10] They studied the formation of hydrogen- and oxygen-related defects (C-H_2, OH, and C-HOH) in pentacene film based on the density functional calculation. The defect creation reactions were given as follows:

$$2h^{+} + C_{22}H_{16} + C_{22}H_{14} \rightarrow 2(C_{22}H_{15})^{+}$$

and

$$2h^{+} + C_{22}H_{16}O + C_{22}H_{14} \rightarrow (C_{22}H_{15}O)^{+} + (C_{22}H_{15})^{+}$$

When the pentacene film is in a hole-rich environment, both these two reactions tend react to the right-hand side and produce positive-charged states that cause ΔV_{th}. Either bipolaron formation or hydrogen-, oxygen-related defect creation, these studies need more experimental results to support their theories. Both mechanisms assume that the reaction rate is proportional to the carrier concentration.

However, compare with negative bias stress effect, there are fewer studies focused on positive bias stress effect. Applying a prolonged positive bias to the device usually causes electrons trapping in the channel and a threshold voltage shift forward positive bias. After removing the negative bias, the recovery of trapped electrons can be observed and the device threshold voltage comes back to the original value. Until now, the micro process of electron trap generation under the positive bias stress is not discussed in detail.

The reversible positive ΔV_{th} not only caused by positive bias stress but also can be induced by H_2O and O_2 in ambient air. When there are lots of OH groups on the SiO_2 surface, SiOH is generated. H_2O and O_2 are easily absorbed by SiOH to cause electron traps at the pentacene/dielectric interface. This generation process can be shown as chemical reaction:

$$SiOH + H_2O \Leftrightarrow SiO^- + H_3O^+$$

and

$$SiOH + e^- + \frac{1}{4}O_2 \rightarrow SiO^- + \frac{1}{2}H_2O$$

We can see H_2O and O_2 contained in air promote the reaction to the right-hand side and produce negative-charged states that cause the ΔV_{th}. Therefore, if we perform the measure in vacuum or eliminating OH groups on the dielectric surface, the prolonged positive bias influence on device V_{th} may be drastically reduced.

1-2-5 Originals of Trapped Carriers

In the above section, the most of reliability studies focus on the defect generation and a few studies discuss the original of trapped carriers. The efficiency of injection of carriers from the metal contact into the HOMO or LUMO of the pentacene thin film depends on the energy barrier ϕ_B that carrier has to overcome at the metal/organic semiconductor interface. At the metal/organic semiconductor interface, $\phi_{B,e}$ and $\phi_{B,h}$ depend, respectively, on the position of the LUMO and HOMO relative to the Fermi level of the metal. Fig. 1-7 shows that the Energy-band diagrams of pentacene-based thin film transistor with Au contact metal. Obviously, the work function of Au contact is near the HOMO of pentacene film, The $\phi_{B,h}$ is smaller than $\phi_{B,e}$. Therefore, the hole carriers are main transport carriers. For originals of trapped hole carriers in the device channel, it is believed that the hole carrier injection from contact is the main mechanism. Because the large $\phi_{B,e}$ seriously lower the efficiency of electron injection, the electron injection is excluded to provide free electrons in the channel. To date, originals of trapped electrons are fully understood and observed phenomena can not be satisfactorily explained. There are two plausible mechanisms to explain originals of trapped electrons: (1) light-induced electron traps and (2) hydroxyl groups induced electron traps.

(1) Light-induced electron traps:

When irradiating the device, photons enter the pentacene film to generate the excitions. Then, light-induced excitons dissociate into hole-electron pairs. Some papers report that the dissociation process of light-induced excitons can be enhanced under electric field. High vertical field (higher than 2×10^4 V/cm [16]) may be effective in dissociating excitons.

(2) Hydroxyl groups induced electron traps

Based on the above Sec. 1-2-3, the generation process of electron traps has been explained. Hydroxyl groups on gate dielectric or in pentacene film combine with moisture in air to generate electron traps. The originals of hydroxyl groups may come from fabrication process that causes residual hydroxyl groups due to incomplete cross-linking or incomplete baking.

In following chapter 4, the influences of light-induced electrons and hydroxyl groups on gate dielectric are studied and discussed.

1-2-6 Gate Dielectric Surface Treatment

The transfer characteristic of organic-based TFTs strongly depends on the gate dielectric states. There are usually high density of traps consisted on the gate dielectric surface to lower the field-effect mobility, cause the hysteresis and increase the leakage current. Therefore, it is proposed that using various kinds of organic compound treats gate dielectric surfaces of organic-based TFTs to improve the transistor performance. For the first time, Lin *et. al.* demonstrated that using OTS to treat the dielectric surface improve the mobility of pentacene-based TFTs due to the lower density of trap states at the interface between the semiconductor and the gate dielectric [17]. To date, many chemical compounds have been used for the surface treatment of gate dielectrics. These chemical compounds are classified into (1) trichlorosilane [18], (2) alkoxysilane [19], (3) phosphonic acid [20] and (4) silazane [21] according to the reaction group. The surface treatment can improve the mobility, threshold voltage and subthreshold slope.

1-3 Overviews of a-Si:H TFTs on Flexible Substrate

Electronic devices fabricated on flexible substrates have been attracted great attention and expected to realize electric books. The advantages of the electric book are portable, low-power, and inexpensive electronics even including wireless. Furthermore, the fabrication cost of a-Si:H TFTs on flexible substrates can be lowered compared to conventional technology due to substrate cost. The cost of glass substrate is usually higher than the polyimide substrate. Therefore, the fabrication cost in a-Si:H TFTs can be lowered and power consumption also can be reduced when process temperature is lower. Although organic based TFTs are attractive due to room-temperature and large-area fabrication process compatibility, these organic materials easily degrade in air and the superior encapsulation are necessary. Furthermore, the transfer characteristic of organic based TFT is very sensitive to the surface states of gate dielectric. The very smooth surface of substrate or gate dielectric is basic requirements to fabricate the uniform characteristic of devices on the large or long substrates.

In the other hand, in order to obtain stable and superior characteristic, process temperature of a-Si:H TFTs is usually higher than 150 ^{o}C. However, many polyimide substrates can sustain the temperature varied from 150 ^{o}C to 200 ^{o}C and the cost is still kept at low. More recently, there have been reports of TFT fabrication at 150◦C on Kapton E and at 110◦C on polyethylene terephthalate (PET), showing performance characteristics close to those fabricated at 250–300◦C. The gate dielectrics in a-Si:H TFTs and passivation dielectrics are usually based on plasma deposited amorphous silicon nitride (a-SiN$_x$). The basic requirements of a good gate dielectric have to sustain electric fields of about 2 MV/cm without breakdown and low charge-trapping rate at lower electric fields. When PECVD a-SiN$_x$ gate dielectric fabricated at 150^{o}C for compatibility with flexible plastic substrates, a-SiN$_x$ thin film usually have high hydrogen concentration, poor dielectric performance and the high leakage current. The fabrication process follow is shown in below:

1-3-1 Reliability Issues of a-Si:H TFTs on plastic substrates

Compared with crystalline silicon transistors, a-Si:H TFTs exhibit threshold voltage shift (ΔV_{th}) under bias stress that causes the drain current to decrease with time. There are two main mechanisms are responsible for the device ΔV_{th}: (1) the creation of dangling bonds in a-Si:H film and (2) charge trapped inside the dielectric layer (silicon nitride). In that case (1), the device ΔV_{th} is temperature- and bias-dependent and irreversible after stress removal. When the ΔV_{th} is induced by charge trapped, the ΔV_{th} is independent on temperature and dielectric-trapped charges emitted from defective gate dielectric to a-Si:H layer increase gate leakage current. When decreasing deposition temperature down to the highest working temperature of low-cost polyimide substrate, this low process temperature leads to poorer electronic properties in a-Si:H and in higher charge-trapping rate in the gate dielectric. It was reported that in a-Si:H TFTs fabricated at the substrate temperature of 110 ^{o}C, a-Si:H defect generation increased fivefold, whereas the charge trapping in the nitride gate dielectric went up by one order of magnitude.

When applying the general operation bias to stress the device, the ΔV_{th} of a-Si:H

TFTs is attributed state creation in the a-Si:H thin film. After prolonged bias stress, the ΔV_{th} of a-Si:H TFT is obvious while the field effect mobility and subthreshold slope remain unchanged. When reaching adequate stress bias, defect state creation in a-Si:H TFTs is no longer dominant and the ΔV_{th} is controlled primarily by charge injection from the channel into the gate dielectric interface. In our experiment, when process temperature is kept at 160 °C, the device ΔV_{th} is strongly dependent on the substrate temperature. It means that the SiN_x thin film is more stable than thin film at low process temperature and state creation mechanism is the major mechanism. ΔV_{th} as a function of stressed gate bias and stress time can be expressed by the stretched-exponential equation [22]:

$$V_{th} - V_{th}^{ini} = \Delta V_{th} = (V_G - V_{th}^{ini})\left\{1 - \exp\left[-\left(\frac{t}{\tau_t}\right)^{\beta}\right]\right\} \tag{1-7}$$

where V_{th}^{ini} is the initial threshold voltage. β is a weakly temperature-dependent dispersion parameter. τ_t can be expressed as $\tau_t = \nu^{-1}\exp\left(\frac{E_A}{kT}\right)$, where ν is an attempt to escape frequency and E_A is the mean activation energy for the defect generation.

1-3-2 Self-Heating Effect

Recently, gate driver circuits of TFT-LCD panel have been successfully fabricated by using conventional a-Si:H TFTs on glass substrates [23]-[25]. The a-Si:H based circuits can lower the amount of driver ICs and simplify the IC bonding process. Because a-Si:H TFTs exhibit low field effect mobility, the enormous channel width such as using the finger structure as shown in Fig. 1-8 or increasing drain bias are usually designed to provide adequate current to drive the pixel array. However, a-Si:H TFTs have the serious reliability issues compared with poly-Si TFTs. The instability of threshold voltage easily causes the fail on the function of circuits.

Unfortunately, in recent studies, it is found that the enormous channel width and large drain bias enhance the ΔV_{th} and cause the damage in the channel by burning. Fig. 1-8 (a) shows that increasing channel width increases the normalized device current and serious degradation generated in a-Si:H TFT with large channel width when reaching adequate operation bias. Fig. 1-9 (b) shows that large current cause damage in the channel by burning [26]. Based on the state creation mechanism; the ΔV_{th} is proportional to the carrier concentration in the channel. The threshold voltage shift should be independent on the channel width and increasing drain bias can lower the ΔV_{th}, when gate bias stress is applied. The abnormal ΔV_{th} is attributed to the self-heating effect. According to the study on self-heating effect in a-Si:H TFTs reported by Wang *et al.* [27], heat dissipation to the ambient are primarily through the gate, the source and the drain contacts. The path through the gate contact via the gate insulator is the most effective. When heat dissipates through gate contact, the thermal resistance of the substrate dominates the thermal dissipation from gate contact to the ambient. The temperature of device can be estimated by the power consumption equation and the thermal resistance of the substrate. Although the device temperature can be estimated, the accurate device temperature and critical operation bias induced the self-heating effect are still difficult to predicted due to complicated thermal dispersive routes. For example, the gate metal pattern also can affect the self-heating effect. Fig. 1-10 shows the surface temperature distribution of a-Si:H TFT when operated at different bias conditions [26].

1-4 Comparisons between Organic TFTs and a-Si:H TFTs

For the development of devices on flexible substrates, organic TFTs have several advantages compared with a-Si:H TFT :

1. Compared with existing a-Si:H TFTs, organic TFTs can offer a greater performance

advantage.

2. Because of the high processing temperature used in a-Si:H thin film deposition, a few of the flexible substrate materials are suitable and these materials are usually expensive. However, the processing temperature of organic TFTs can be lowered to room temperature and are compatible with transparent flexible substrates.
3. Using low-cost processes such as roll-to-roll to manufacture organic TFTs on a large area substrate can significantly reduce cost.

Although the performance of organic TFTs is already better than that of a-Si:H TFT, some drawbacks are still waited for solving :

1. Organic materials are very sensitive to the surface state of gate dielectric. Therefore, for industrial manufacture, the uniformity of OTFTs is a serious issue.
2. These organic materials easily degrade in air and the superior encapsulation technology is needed.

Therefore, there are many groups still use the existing a-Si:H TFT process to develop the device on flexible substrates and have some advantages :

1. For display corporations, the device can be manufactured by using the original instruments.
2. The reliability of a-Si:H TFTs is better than organic TFTs.

Fig. 1-1 (a) Pentacene-based array combined with light emitting diode [Sony, 2007] (b) Pentacene-based array combined with liquid crystal [Hitachi, Ltd., 2006] (c) Pentacene-based array combined with electrophoresis [National Academy of Sciences, 2001].

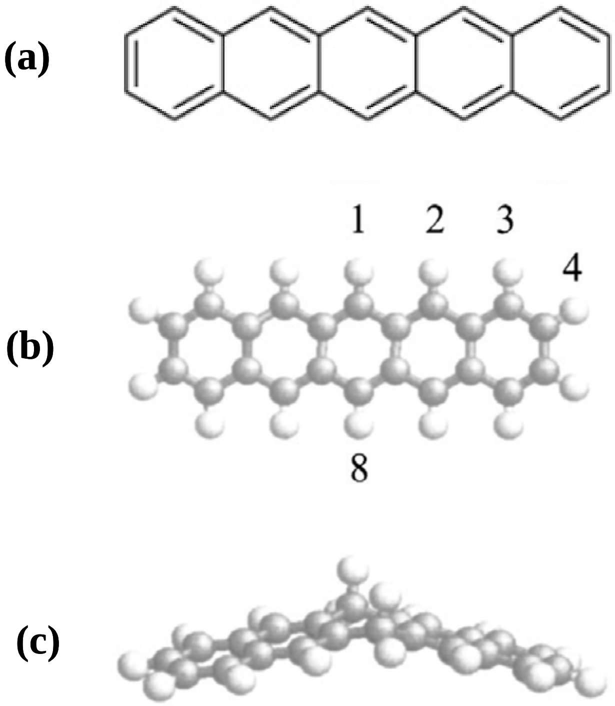


Fig. 1-2 (a) Pentacene is made up of five benzene rings (b) a single pentacene molecule ($C_{22}H_{14}$) consists of 5 benzene rings. In each molecule 14 of the 22 C atoms are bonded to two other C atoms and to one hydrogen atom. The four inequivalent H atoms are numbered 1–4. Other H atoms are related by symmetry. (c) A single $C_{22}H_{16}$ molecule (dihydropentacene) is shown here. The two C-H_2 units are positioned on sites 1 and 8.

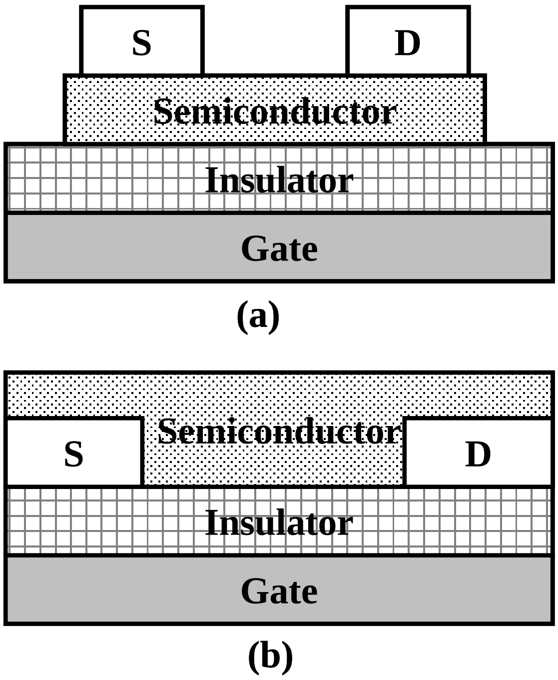


Fig. 1-3 OTFT device configurations: (a) Top-contact device, with source and drain electrodes evaporated onto the organic semiconducting layer. (b) Bottom-contact device, with the organic semiconductor deposited onto the gate insulator and the previously fabricated source and drain electrodes.

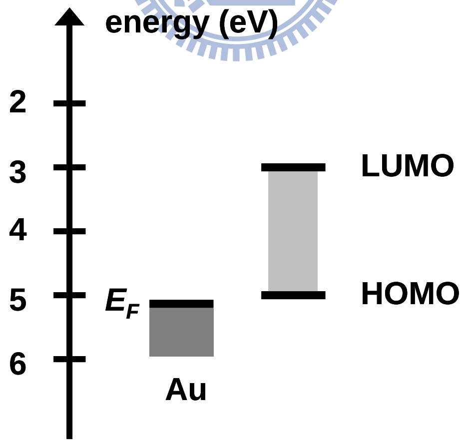


Fig. 1-4 Energy scheme of the gold-pentacene interface.

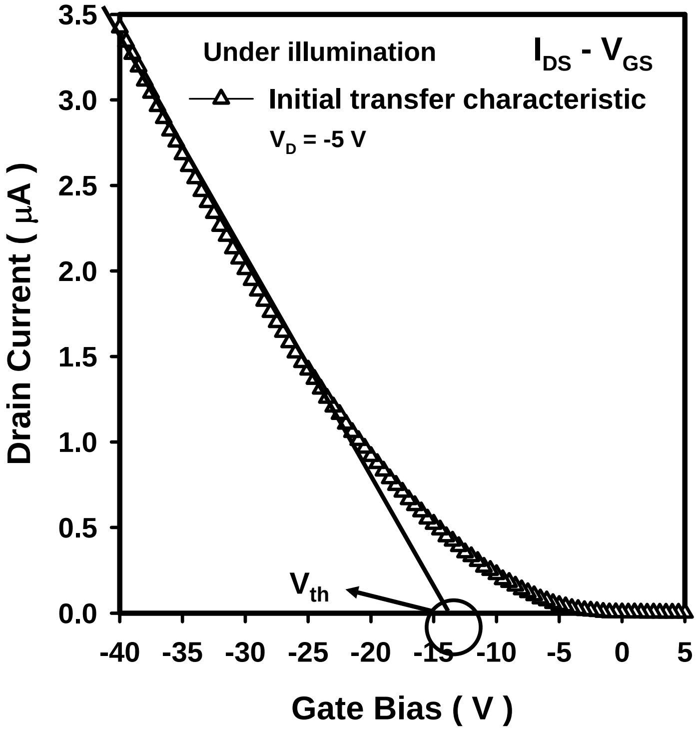


Fig. 1-5 Plot of drain current (I_{DS}) as a function of gate voltage for OTFT to obtain the threshold voltage (V_{th}).

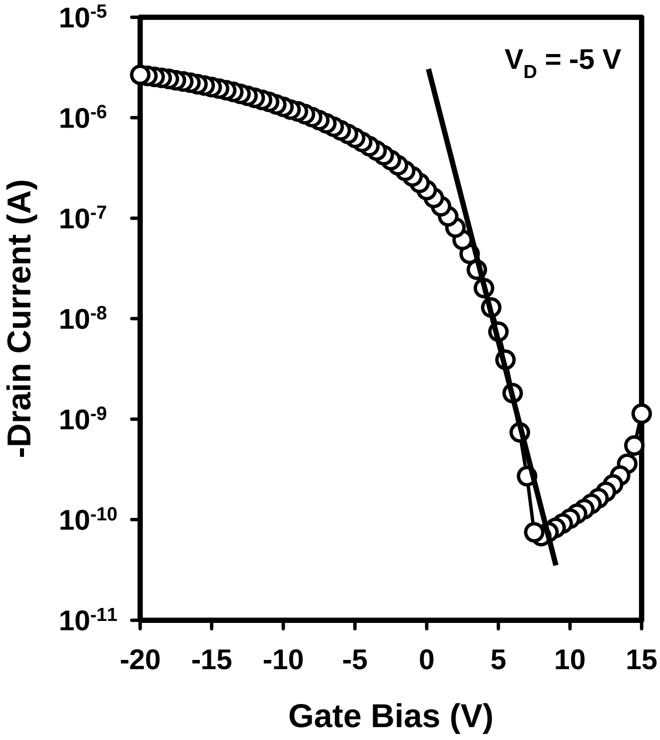


Fig. 1-6 OTFT transfer characteristics and fitting used for extraction of the subthreshold slope.

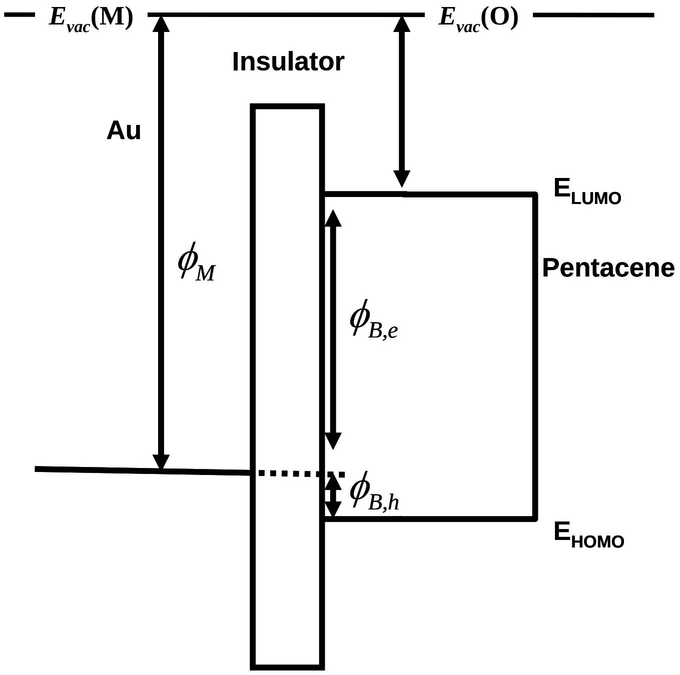


Fig. 1-7 Schematic of an organic-metal interface energy diagram. $\phi_{B,e}$ **and** $\phi_{B,h}$ **are the electron and hole barriers and** E_{vac}**(O) and** E_{vac}**(M) are the organic and metal vacuum levels, respectively.**

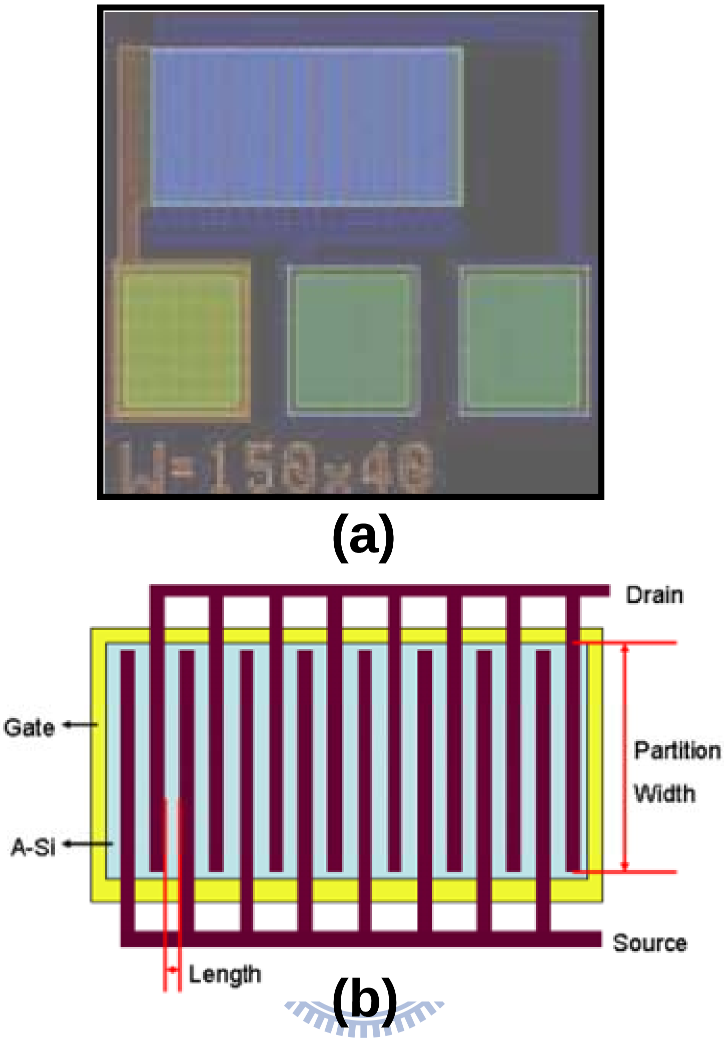


Fig. 1-8 (a) Top view and (b) Schematic diagram of the partitioned a-Si:H TFT named as finger structure.

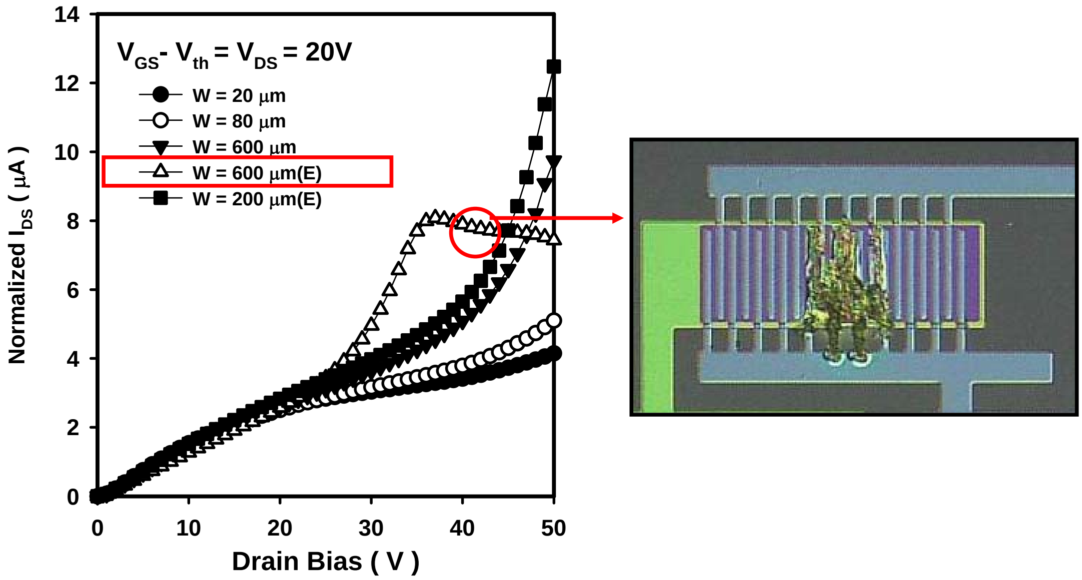
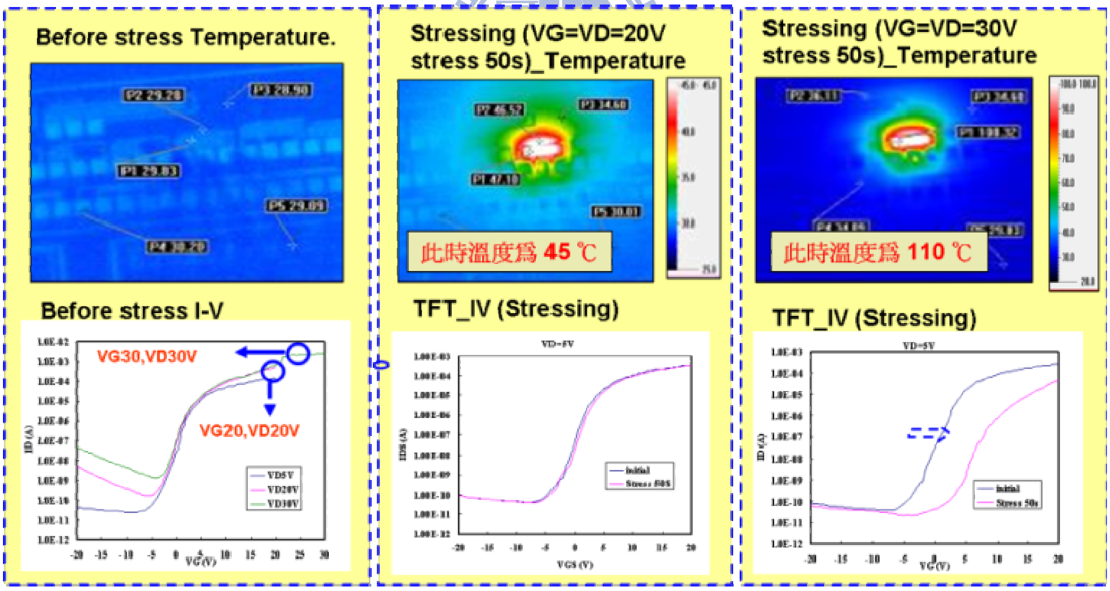


Fig. 1-9 (a) shows that increasing channel width increases the normalized device current and serious degradation generated in a-Si:H TFT with 600 μm when reaching adequate operation bias. (b) large current causes damage in the channel by burning.



Initial

V_G=V_D=20V

V_G=V_D=30V

Fig. 1-10 The surface temperature distributions of a-Si:H TFT when devices are applied different operation bias [21].

Chapter 2

FABRICATION PROCESS TECHNOLOGY

2-1 Vapor Deposition Process in Pentacene Thin-Film Fabrication

Small molecule organic semiconductor films can be deposited by sublimation in a variety of vacuum deposition systems utilizing various methods. The deposition parameters can vary widely from method to method. And OTFTs with good charge carrier transport characteristics have been fabricated using most versions of vacuum sublimation and deposition. The based pressure of the deposition system and the pressure during deposition are important process parameters, since they determine, among other things the mean path of the sublimed organic semiconductor molecules and the presence of impurity atoms and molecules in the vicinity of the substrate surface during film formation. Substrate temperature and deposition rate are two other deposition parameters that can dramatically influence thin-film morphology and thus the transport characteristics of OTFTs.

2-2 PECVD Process in a-Si:H Thin-Film Fabrication

PECVD is widely used in the fabrication of VLSI processes. Its influences to thin film properties, semiconductor device reliability, production yield, etc. are thoroughly examined and published in documents. The conventional capacitively coupled PECVD reactor is widely used in the deposition of non-metal thin films for a-Si:H TFTs. The reactor is composed of two parallel plates enclosed in a vacuum chamber. The loading plate on which the substrate is loaded is grounded and heated. The other plate is connected to an RF generator with a matching network. Although 13.56 MHz is the most popular frequency, other higher or lower frequencies, from 50

KHz to 2.45 GHz, have also been used in commercial reactors. In this kind of reactor, plasma is generated between the two electrodes under vacuum. There are other types of PECVD reactors of which the plasma is generated through an inductive process. For example, an inductive coil can be applied near the electrode or surrounding the chamber to generate an additional plasma reaction path. The plasma density of this kind of reactor can be higher than that in a conventional capacitively coupled reactor. In another case, the plasma can be generated in a chamber remote from the deposition chamber, the remote reactor. This arrangement can minimize plasma damages to the film or the device.

Because the a-Si:H film is full of defects that are charge-trapping centers, dangling bonds ate the major contributor of these defects. Hydrogen is the most effective passivation agent for dangling bonds. It is readily available in the PECVD process because hydrogen is a major component in the feed gas stream. Therefore, in the TFT preparation procedure, an important issue is how to effectively retain a large amount of hydrogen in the film. The film’s hydrogen content can be varied by process parameters, such as temperature, power and feed gases.

2-3 Polyimide Substrates

Polymer foil substrates are highly flexible, can be inexpensive, and permit roll-to-roll processing. However, they are thermally and dimensionally less stable than glass substrates and are easily permeated by oxygen and water. A glass transition temperature, Tg, compatible with the device process temperature is essential. However, a high Tg alone is not sufficient. Dimensional stability and a low coefficient of thermal expansion (CTE) are also important factors. Typical polymer films are shrunk by heating and cooling cycles. They shrink less if prestabilized by prolonged annealing. Because the elastic modulus of polymer substrates is a factor of 10–50 lower than that of inorganic device materials, a small thermal mismatch stress can make the free-standing workpiece curve and cause misalignment during the overlay registration of the flattened piece. A large CTE mismatch coupled with a large temperature excursion during processing can break a device film [1]. Polymers substrates with CTE below 20 ppm/◦C are preferred as substrates for silicon-based device materials.

Candidate polymers for flexible substrates include (1) the thermoplastic semicrystalline polymers: polyethylene terephthalate (PET) and polyethylene naphthalate (PEN), (2) the thermoplastic noncrystalline polymers: polycarbonate (PC) and polyethersulphone (PES), and (3) high-Tg materials: polyarylates (PAR), polycyclic olefin (PCO), and polyimide (PI). PC, PES, PAR, and PCO are optically clear and have relatively high Tg compared to PET and PEN, but their CTEs are 50 ppm/◦C or higher, and their resistance to process chemicals is poor. Much research has been conducted with PET, PEN, and PI, with their relatively small CTEs of 15, 13, and 16 ppm/◦C (Kapton E), respectively, relatively high elastic moduli, and acceptable resistance to process chemicals. Both PET and PEN are optically clear with transmittance of >85% in the visible. They absorb relatively little water (~0.14%), but their process temperatures are only ~150 and ~200◦C, even after prestabilization by annealing. In contrast, PI has a high glass transition temperature of 350◦C, but it is yellow because it absorbs in the blue, and it absorbs as much as 1.8% moisture [2]. No polymer meets the extremely demanding requirement for low permeability in OLED applications. The typical water and oxygen permeation rates of flexible plastic substrates are 1–10 $g/m^2/day$ and 1–10 $cm^3/m^2/day$, respectively, instead of the required 10^{-6} $g/m^2/day$ and 10^{-5} $cm^3/m^2/day$. Barrier layer coatings can reduce absorption and permeability by gas, raise resistance to process chemicals, strengthen adhesion of device films, and reduce surface roughness.

2-4 Measurement Platforms

2-4-1 Current-Voltage Measurement Instrument

Two measurement systems are used in this study. In ambient air, using semiconductor parameter analyzers (HP4156 or Keithley 5270) measure the current-voltage characteristic of pentacene-based TFTs and a-Si:H TFTs in metal box. The temperature of sample stage can be adjusted from room temperature to 200 ^{o}C. Another measurement system includes semiconductor parameter analyzer Keithley 4200 and vacuum chamber. The chamber pump can lower the pressure in chamber from 760 Torr to 0.5 Torr. Therefore, measurements can be performed in vacuum at room temperature to compare H_2O and O_2 influences on the device stability. Fig. 2-1 shows that the measurement system includes semiconductor parameter analyzer Keithley 4200 and vacuum chamber.

2-4-2 Light Sources

There are four different light sources used to irradiate the device in this thesis. The white light source comes from light-emitting diode (LED) backlight with a broad wavelength range. Blue, green and red light sources are light-emitting diodes with 467 nm, 536 and 631 nm wavelengths. The light source is set up above the device to irradiate the sample from the top. The light power is controlled by the power supply (PPT3615). Changing the applied voltage can adjust the light intensity.

2-5 Material Analysis Instruments

2-5-1 Contact Angle System

Contact angle system is used to estimate wetting ability of a localized region on a solid surface. The angle between the baseline of the drop and drop boundary is measured. The measured result shows that the material surface is hydrophile or hydrophobic. Because the contact angle strongly depends on the chemical bonding of the material surface, the magnitude of contact angle also represent the proportion of hydroxyl groups on the material surface. In chapter 4, measuring the water contact angle compares the proportion of hydroxyl groups on the dielectric surfaces of PVP and PMMA. Fig. 2-2 is the picture of contact angle system used in this experiment.

2-5-2Fourier Transform Infrared Spectroscopy

FTIR is powerful tool for identifying types of chemical bonds (function groups) in organic molecular. The absorbed wavelength of incident light represents the characteristic of the chemical bond, by analyzing the infrared absorption spectrum, the chemical bonds in a molecule can be determined. In chapter 4, because the absorption spectrum of OH groups is well know and easily searched in many previous papers, using FTIR can accurately observe the proportion of OH group on the material surface. Fig. 2-3 shows some absorption spectrum of common function groups.

2-5-3 X-Ray Diffraction

X-ray diffraction (XRD) is a non-destructive technique that reveals detailed information about the chemical composition and crystal structure of materials. The crystal lattice is a regular three-dimensional distribution of atoms in space. Atoms are arranged and form a series of parallel planes separated from one another by a distance d, which varies according to the nature of the material. When monochromatic X-ray project onto a crystalline material at particular angle (Θ), diffraction will occurs because the ray traveled distances reflected from successive planes differs by a complete number n of wavelength. Plotting the angular positions and intensities of the diffracted peaks produces a pattern, which is characteristic of the sample. Fig. 2-4 is the picture of Shimadzu XRD-6000.

2-5-4 Atomic force microscope (AFM)

Atomic force microscope (AFM) is used to measure surface morphology on a scale from angstroms to 30 microns. It scans samples through a probe or tip, with radius about 20 nm. The tip is held several nanometers above the surface and using feedback mechanism that measured interactions between tip and surface on the scale of nanoNewtons. Variations in tip height are recorded when the tip is scanned repeatedly across the sample, then producing morphology image of the surface. In this experiment, the used equipment is Digital Instruments D3100 as shown in Fig. 2-5 and the used active mode is tapping mode.

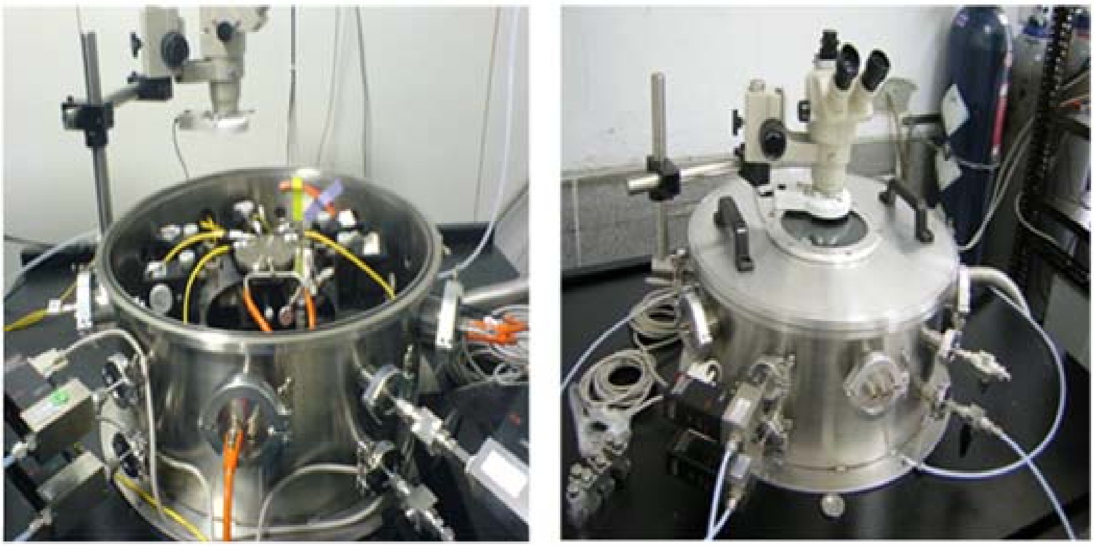


Fig. 2-1 The vacuum measurement system includes semiconductor parameter analyzer Keithley 4200 and vacuum chamber. The pressure of vacuum chamber ranges from 760 Torr to 0.5 Torr.

Fig. 2-2 Water contact angle system

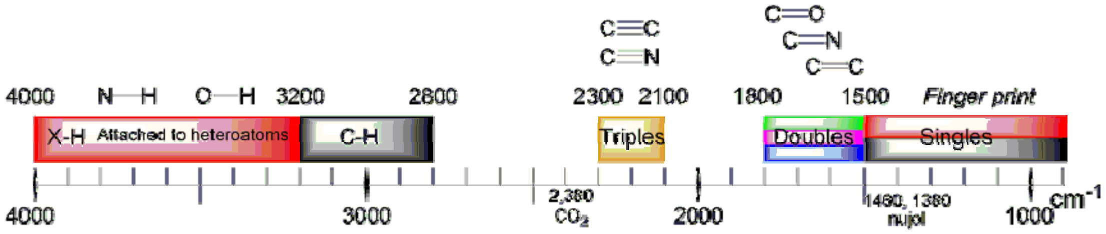


Fig. 2-3 Absorbance spectrums of different function groups

Fig. 2-4 Shimadzu XRD-6000

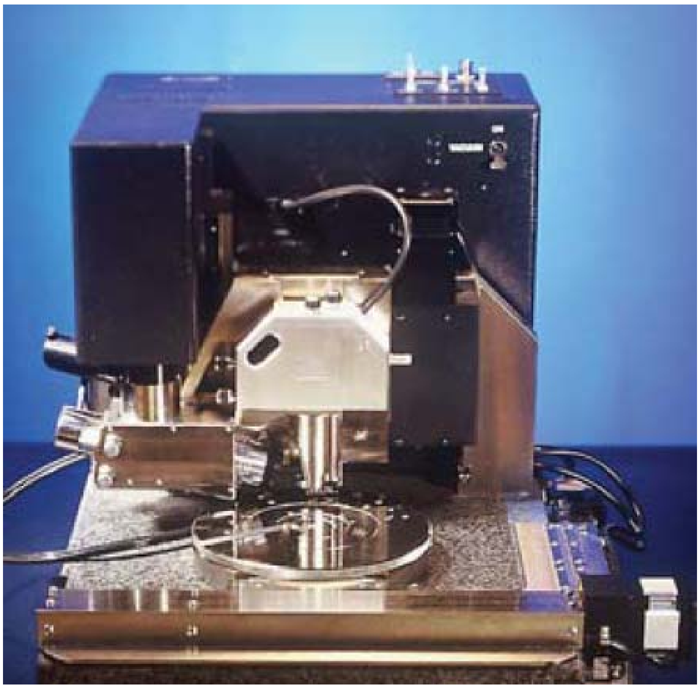


Fig. 2-5 Digital Instruments D3100

Chapter 3

RELIABILITY ISSUES OF PENTACENE-BASED OTFT

3-1 Introduction

Recently, organic thin-film transistors (OTFTs) have received great attention due to their low-cost and large-area array application. Field-effect mobility comparable to that of a-Si:H TFTs can be obtained under a low operation voltage. OTFT arrays to drive liquid crystal (LC) [1, 2] or organic light emitting diode (OLED) [3] which showed full-color moving pictures had been demonstrated. In these reports, OTFTs were encapsulated by passivation layer to avoid exposing to oxygen or moisture in air, and to avoid damaging from the subsequent LC or OLED process. However, even when devices are encapsulated or operated in an inert environment, OTFTs are known to suffer from bias stress effect (BSE) that causes significant threshold voltage shift (V_{th} shift). The BSE in OTFTs had been studied by using different organic active materials or different gate insulators on different device structures [4]. It was found that, for p-type OTFTs under steady-state gate bias stress, positive gate bias stress caused a positively-shifted V_{th} and negative gate bias stress caused a negatively-shifted V_{th}. The BSE was reversible by removing gate bias or by applying opposite polarity gate bias. Light irradiation also enhanced the reversal process.

Several mechanisms have been proposed to explain the BSE, including charge trapping, ion migration, charged-state creation and the formation of bound hole pairs (bipolaron) [5]. For OTFTs with organic dielectric, charge trapping and ion migration were found to be dominant [6]. For OTFTs with thermally-grown SiO_2 as the gate dielectric, charged-state creation or bipolaron formation within the organic semiconductor film, near the dielectric interface, is usually believed to be responsible for V_{th} shifts. More specifically, J. E. Northrup [7] had proposed that the state creation was due to the formation of oxygen- or hydrogen-related defects such as C-H_2, O_H, and C-HOH in organic semiconductors [8]. The bipolaron, proposed by Salleo and Street et al. [5], are the less mobile bound hole pairs that deplete the accumulation channel of mobile holes and cause an increase in the V_{th}. Both the state creation and the bipolaron formation suggest that the reaction rate should be proportional to the carrier concentration. Thus, the gate-bias stress effect can be explained. However, to the best of our limited knowledge, there is no other observation directly validating the proportionate relationship between the reaction rate and the carrier concentration. When device is operated in linear model, using drain bias can effectively adjust the carrier concentration. Thus its influence on the BSE of OTFTs is worth investigating. Although the drain bias effect in OTFTs with organic dielectric had been studied to discuss its influence on ion migration, the effect on OTFTs with stable dielectric had not been carefully investigated before.

Based on above studies, OTFTs stressed by steady-state bias were intensively characterized and analyzed. The bias stress effect under pulsed bias stress, however, was not clearly addressed. Since there are many defect states distributed in organic materials and the interface between organic film and insulator layer. The time-dependent charging and releasing behaviors of these defect states will influence channel carrier density when gate bias is suddenly changed. Therefore, using steady-state bias stress is difficult to discuss the trapping and detrapping of defect states and their influences on device threshold voltage during pulsed operation. Following the discussion of drain bias influence on OTFT instability, dynamic bias reliability for pentacene-based OTFTs with thermally grown oxide was studied. The influence of trapping and releasing effect on dynamic bias reliability was also discussed. The results are useful and important for investigating trap effect and for designing pentacene-based OTFT circuit.

Finally, the one of the reliability issues of OTFT is induced by prolonged illumination when OTFTs were applied on display. When illuminating organic film, excitons are generated, a fraction of which are dissociated in electron-hole pairs. Light-induced electrons close to the gate dielectric are trapped by the interface states and the device threshold voltage shifts toward positive [8-10].

Therefore, in this chapter, drain bias influence, dynamic bias reliability and light-induced instability are studied and discussed, sequentially. These three issue results are very important for reliability of organic TFTs on display application.

3-2 Experiment

3-2-1 Device Fabrication Process

In this study, conventional top-contact pentacene-based OTFTs were used. 100-nm-thick thermal oxide is grown on heavily doped Si wafers to serve as the gate dielectric. The fabrication processes follow are shown in below.

Step1. Clean the oxide surface

Before fabricating device on wafer, the native oxide on the back of wafer must be etched by using BOE (NH_4F : HF = 10 : 1) solution. Then, the oxide surface of wafer was cleaned by 5 mins DI water, 5 mins acetone and 5 mins DI water, sequentially. Using hot plate bakes the wafer to remove the moisture on the oxide surface.

Step2. Pentacene film deposition through shadow mask

Pentacene obtained from Aldrich (purity: 99.9%) without purification was evaporated through a shadow mask onto thermal oxide to form the active layer. The deposition rate was set at 0.5 Å/s while the substrate temperature was kept at 70 °C. The pressure was kept at room temperature and at around 3×10^{-6} Torr during deposition process. The thickness of pentacene film is 100-nm.

Step3. Depositing Au to form source and drain contact

After depositing a 100-nm-thick pentacene, 100-nm-thick gold was deposited through the shadow mask to form source/drain contacts. The thickness of Au layer was 100 nm. The device channel length varied from 100 μm to 600 μm while channel width was fixed as 1000 μm. The structure scheme of pentacene-based TFTs is shown in Fig. 3-1.

3-2-2 Definition of Device Threshold Voltage

The device was measured at room temperature in ambient air. The threshold voltage (V_{th}) is extracted by using the linear region equation. The ΔV_{th} is defined as $V_{th} - V_{th}^{ini}$ where V_{th}^{ini} is the initial threshold voltage before bias stress.

3-3 Steady-State Bias Stress

3-3-1 Gate Bias Stress Effect

Before performing further OTFT reliability study, the gate bias stress effect of pentacene-based TFTs used in this study was characterized. The initial device transfer characteristic before stress is shown in Fig.3-2. Field effect mobility, threshold voltage and subthreshold slope are 0.32 cm^2/Vs, -6.5~8 V and 1.05 V/decade, respectively. Threshold voltage was extracted by using the linear region equation and mobility was extracted by using maximum linear-region transconductance (G_M). With source and drain connected to ground, various gate biases were used as the stress conditions (V_{DS} = 0 V, $V_G - V_{th}^{ini}$ = -5 V, -10 V, and -15 V, where V_{th}^{ini} is the initial threshold voltage). The linear-region transfer characteristics of the devices before stress and after 2000-sec stress are depicted in Fig. 3-3. All the devices exhibit similar original characteristics, so only one curve is shown to represent the characteristics before stress. Fig. 3-4 (a) and (b) show the evolution of linear-region transfer characteristics during a 2000-sec stress time under $V_G - V_{th}^{ini}$ = -15 V. Obviously the gate-bias stress causes a shift of the transfer characteristics while the subthreshold swing keeps almost unchanged. The shift of threshold voltage V_{th} and the shift of field-effect mobility μ_{FE} as a function of stress time are shown in Fig. 3-5 (a) and (b), respectively. μ_{FE} is not affected by the stress, while V_{th} is drastically changed. Such a phenomenon is often believed to be caused by the generation of deep states with long discharge time that degrade V_{th}. The shallow traps that would affect μ_{FE} may not be changed by the gate bias stress [11]. The power-law dependence between the threshold voltage shift and the stress time is also found in Fig. 3-6. Clearly, the steady-state gate bias stress influenced only the threshold voltage. Similar results have also been reported by other researchers [11, 12]. State creation was the primary mechanism to explain the BSE of pentacene-based TFTs with thermally-grown SiO_2 dielectric [4]. The time dependence of ΔV_{th} can be described by using the stretched exponential equation as [13]:

$$V_{th} - V_{th}^{ini} = \Delta V_{th} = (V_G - V_{th}^{ini})\left\{1 - \exp\left[-\left(\frac{t}{\tau_t}\right)^{\beta}\right]\right\} \tag{3-1}$$

where V_{th}^{ini} is the initial threshold voltage. β is a weak temperature-dependent dispersion parameter. τ_t represents the effective trapping time that can be expressed using $\tau_t = \nu^{-1}\exp\left(\frac{E_A}{kT}\right)$, where ν is an attempt to escape frequency. E_A is the mean activation energy for defect generation. Parameters of the stretched exponential equation can be extracted by fitting the simulated ΔV_{th} curve to the experimental data as shown in Fig. 3-7. When the stretched exponential function is used, the dispersion parameter β can be obtained by plotting $log\left\{-ln\left[1 - \Delta V_{TD}(Q_{G0}/Q_G)/(V_{GS} - V_{th}^{ini})\right]\right\}$ as a function of log(t) in the inset of Fig. 3-7. After applying a 2000-sec gate bias stress under V_G - V_{th}^{ini} = 15V, extracted E_A, β and τ_t are 0.57 eV, 0.283 and 3.61×10^4 sec, respectively. These extracted parameter values were similar to those obtained in other studies [11, 12].

3-3-2 Drain Bias Stress Effect on the Threshold Voltage Shift

Different drain biases (V_{DS} = 0 V, 5 V, 10 V, and 15 V) were added to the bias-stress measurement while the gate bias was fixed as V_G - V_{th}^{ini} = -15 V. The linear-region transfer characteristics of the devices before stress and after bias stress are depicted in Fig. 3-8 (a) and (b). When increasing drain bias under gate bias stress, the shifts of transfer characteristics are suppressed. The shift of μ_{FE} is plotted as a function of stress time in Fig. 3-9. Unchanged μ_{FE} is observed, and consequently the influence of drain-bias stress on the shallow traps can be excluded. The influence of drain-bias stress on the V_{th}, however, is significant. As shown in Fig. 3-10, the shift of V_{th} is suppressed when the drain bias becomes more negative. All the relationships depicted in Fig. 3-11 follow the power-law dependence with identical slope. According to the BSE model, the slope represents the dispersion parameter β that influences the relaxation and the dispersive transport of disorder system. Identical β value implies that the microscopic processes of the state creation such as the impurity diffusion or the defect creation kinetics should be independent of the drain bias. The influence of drain bias on the carrier concentration is believed, as in a-Si:H TFTs, to be the dominant reason that causes the shift of threshold voltage to be dependent on V_{DS}.

To quantitatively discuss this relationship, for a given V_{GS}, we define the threshold voltage shift ratio ($\Delta V_{th,D}/\Delta V_{th,0}$) as the ratio between the threshold voltage shift with various V_{DS} stress ($\Delta V_{th,D}$) and the threshold voltage shift with zero drain-bias stress ($\Delta V_{th,0}$). Then, we plot $\Delta V_{th,D} / \Delta V_{th,0}$ as a function of drain bias in Fig. 3-12. The calculated normalized channel charge defined as Q_G / Q_{G0} is also shown in Fig. 3-12, where Q_G is the channel charge when V_{DS} is varied and Q_{G0} is the channel charge when $V_{\mathrm{DS}} = 0$. The equations used to calculate Q_{G} and Q_{G0} are expressed in Ref [14]. Good agreement can be observed between $\Delta V_{th,D} / \Delta V_{th,0}$ and the calculated Q_G / Q_{G0} curve. The result verifies the proportionate relationship between the defect creation rate and the carrier concentration. Also, the result suggests that convergent data can be obtained by plotting the restored threshold voltage shift $\Delta V_{th,D}$ (Q_{G0} / Q_G) as a function of stress time as shown in Fig. 3-13. The restored threshold voltage shift excludes the drain bias effect and can be simulated by using the stretched exponential function with same parameters.

3-4 Dynamic-State Bias Stress

3-4-1 Steady-State Bias Stress

Before analyzing dynamic-state bias stress effect, the basic steady-state bias stress effect of pentacene-based TFTs used in this study was characterized. The initial device transfer characteristic before stress is shown in Fig. 3-14. Field effect mobility, threshold voltage and subthreshold slope are 0.47 cm^2/Vs, -13 V and 1.05 V/decade, respectively. Threshold voltage was extracted by using the linear region equation and mobility was extracted by using maximum linear-region transconductance (G_M). Then, gate-bias stress was applied on devices when $V_G = V_{th}^{ini}$ -20 V and $V_D = V_S = 0$ V, where V_{th}^{ini} was the initial threshold voltage. The linear-region transfer characteristics of the devices before stress and after 2000-sec stress are depicted in Fig. 3-15. In the Fig. 3-16, field-effect mobility and subthreshold slope are plotted as a function of stress time. The stress caused a shift in device transfer characteristics while field-effect mobility and subthreshold slope were nearly unchanged. The threshold voltage shift (ΔV_{th}) of pentacene-based TFTs plotted as a function of stress time is shown in Fig. 3-17. After applying negative gate-bias stress to pentacene-based TFTs, using the stretched exponential equation extracted E_A, β and τ_t are 0.56 eV, 0.363 and 2.26×10^4 sec, respectively. The dispersion parameter β can be obtained by plotting $log\left\{-ln\left[1-\Delta V_{th,D}(Q_{G0}/Q_G)/(V_{GS}-V_{th}^{ini})\right]\right\}$ as a function of log(t) in the inset of Fig. 3-17.

3-4-2 Pulsed Gate Bias Waveform

Under pulsed bias stress, pulsed voltage was applied to the gate electrode while source and drain electrodes were grounded, as shown in Fig. 3-18. A rectangular pulse with varying pulse widths was used to observe device degradation. The pulse swing region was separated into two parts: the peak voltage region and the base voltage region, as shown in Fig. 3-19. The peak voltage was defined as V_p. The base voltage region was defined as V_b. The pulse period was defined as ($t_\mathrm{p}+t_\mathrm{b}$) and the duty ratio was defined as $t_\mathrm{p}/(t_\mathrm{p}+t_\mathrm{b})$. The effective stress time was defined as the accumulated peak voltage time of pulse periods during stress time.

3-4-3 Negative Pulsed Gate Bias Stress

Under pulsed bias stress conditions, the signal pulse width ranges from 2.5 ms to 3 μs, and the duty-cycle is 50% of the pulse period. Device drain and source electrodes were grounded and pulsed bias was applied to the gate electrode. Peak voltage was set at V_{th}^{ini} -20 V and base voltage was kept at 0 V. Following pulsed bias stress, mobility and subthreshold slope were unchanged when ΔV_{th} was dependent on pulse width as shown in Fig. 3-20.

Similar pulse width effect on ΔV_{th} was observed in a-Si:H TFTs while devices were stressed by negative pulsed bias stress [13]. However, a-Si:H TFTs in those reports were made to be n-type devices, not p-type. When a-Si:H TFTs were stressed by positive pulsed bias stress and the accumulated carriers were majority carriers (electrons), no pulse width effect was observed. For pentacene-based OTFTs, obvious pulse width effect was obtained when the accumulated carriers were majority carriers (holes). A larger response time of holes in OTFTs than that of electrons in a-Si:H TFTs is expected.

To analyze the response time, Chiang et al. simplified the structure of a-Si:H TFTs to an equivalent circuit as shown in Fig. 3-21. The equivalent circuit includes the gate insulator capacitance C_i, a-Si:H capacitance C_s and effective a-Si:H resistance R_s for hole conduction. Like a-Si:H TFTs, OTFTs possess charge trapping and state creation which are two main defect generation mechanisms describing ΔV_{th} in OTFTs during bias stress. The charge trapping mechanism is dependent on the electrical field created by gate bias. Calculating the gate bias distribution between the gate insulator and a-Si:H layers determines the influence of charge trapping. The equation can be expressed as：

$$V_i\left(t^*\right) = V_{ST}\left[1 - \frac{C_i}{C_i + C_s} exp\left(-\frac{t^*}{\tau_{RC}}\right)\right] \tag{3-2}$$

where $V_i(t^*)$ is the voltage drop across the insulator and pentacene film at time t^*. $\tau_{RC} = R_S C_S$, and V_{ST} is the amplitude of the gate pulse. t^* is defined as accumulated peak voltage time. However, in our experiment, using Eq. (3-2) to evaluate ΔV_{th} is difficult. When pulse width is decreasing, V_i gradually reaches its saturation value $\frac{C_S}{C_S + C_i} V_{ST}$, which is not near zero. ΔV_{th}, on the contrary, decreases to be near zero under small pulse width. Therefore, V_i derived from the charge trapping mechanism is not suitable to describe pulse width dependence of OTFTs. State creation was the other main mechanism dependent on carrier concentration in the device channel. Chiang et al. also proposed the effective carrier model to calculate accumulated carrier concentration on the a-Si:H/a-SiN$_x$ interface [13]. The equation included pulse width (PW) is expressed as:

$$\frac{N_{AC}}{N_{DC}}=\left[1-\frac{\tau_{RC}}{PW}+\frac{\tau_{RC}}{PW}exp\left(-\frac{PW}{\tau_{RC}}\right)\right] \qquad (3\text{-}3)$$

where $N_{DC} = -C_iV_{ST}/q$ is the accumulated carrier concentration under steady-state gate bias conditions. N_{AC} is the accumulated carrier concentration under pulsed gate bias conditions.

In our experiment, the negative dynamic gate bias stress with three fixed effective stress times (2000 sec, 1500 sec and 1000 sec) and pulse width ranges from 2.5 ms to 3 μs was used. ΔV_{th} ratio was defined as the ratio between ΔV_{th} under pulsed negative gate bias stress (ΔV_{th}^{AC-}) and ΔV_{th} under steady-state negative gate bias stress (ΔV_{th}^{AC-}). Based on the state creation mechanism, the concentration ratio (N_{AC}/N_{DC}) is equal to the ΔV_{th} ratio ($\Delta V_{th}^{AC-}/\Delta V_{th}^{DC-}$). Then, $\Delta V_{th}^{AC-}/\Delta V_{th}^{DC-}$ was plotted as a function of pulse width in Fig. 3-22. The simulation curve with pulse width dependence can be calculated by using Eq. (3-3). Good agreement can be found between the experimental data and the simulation curve when τ_{RC} was set as 13-μs. Since τ_{RC} describes the accumulation rate of positive charge in device channel, carrier transit time and hole trapping time may account for the 13-μs response time. In next section, we also revealed that the releasing of trapped holes during relaxation has no influence on dynamic bias reliability when relaxing duration was shorter than 17.5 ms.

The (N_{AC}/N_{DC}) factor was then used to modify the original stretched exponential equation as：

$$V_{th}\text{-}V_{th}^{ini}=\Delta V_{th}=(V_G\text{-}V_{th}^{ini})\left\{1\text{-}exp\left[\text{-}\left(\frac{t}{\tau_t}\right)^{\beta}\right]\right\}\times\frac{N_{AC}}{N_{DC}} \qquad (3\text{-}4)$$

Fig. 3-23 shows that simulation curves can fit the experimental data well. The behavior of ΔV_{th} under negative pulsed bias stress can be predicted by the modified stretched exponential equation. For 160×120 pixel display with 140 μs on-state duration, τ_{RC} as 13-μs does not affect pixel operation. However, for high resolution displays or organic electronic circuits, the device current significantly decreases when operating duration is less than τ_{RC}.

3-4-4 Trapped Charge Releasing or Compensation Effects

Although Eq. (3-4) precisely describes the pulse width dependence of ΔV_{th} under negative dynamic gate bias stress, the releasing of the trapped charges during base voltage duration when gate bias is 0 V is not considered. When OTFTs array is applied on display, each pixel has longer off-state duration than its on-state duration in a frame time. The trap releasing effect during base voltage duration is uncertain and requires further study. To observe the trap releasing effect, waveforms of pulse bias formed by the fixed peak voltage duration (t_p) and various base voltage durations (t_b) were used. As shown in Fig. 3-24, the base voltage duration ranged from 0.625 ms to 17.5 ms when the peak voltage duration was fixed as 2.5 ms. Peak voltage was set at V_{th}^{ini} -15 V and base voltage was kept at 0 V. The largest base voltage duration (17.5 ms) is larger than frame duration (16.67 ms). Then, ΔV_{th} curves at fixed effective stress times (2000 sec, 1500 sec and 1000 sec) were plotted as a function of base voltage duration as shown in Fig. 3-25. Obviously, ΔV_{th} curves were not affected by increasing base voltage duration, implying that the trapped holes are difficult to be released from trapped states in frame duration. In previous reports, Gu *et al.* [8] found that time constants of electron detrapping were the order of second or more, time constants of hole detrapping were not accurately estimated. In our study, it is expected that time constants of hole detrapping may be larger than the order of millisecond. Therefore, it is acceptable to ignore trap releasing effect in Eq. (3-4).

Although trapped hole releasing effect is not observed in this study, electron compensation effect is a noteworthy issue. Many reports have found that ΔV_{th} recovery rate can be enhanced by applying opposite gate bias [4, 15]. The recombination of trapped holes with free electrons or the compensation between positive-charged states and negative-charged states are plausible reasons.

The ΔV_{th} recovery behavior under various positive gate biases is observed in Fig. 3-26. Devices firstly received a negative steady-state gate bias stress ($V_G = V_{th}^{ini}$ -20 V) for 1000 sec. When stress time reached 1000 sec, stress bias was removed and various positive gate biases (V_G = 0 V, 3 V and 6 V) were applied to the gate electrode during recovery time. When V_G = 0 V, gate-bias-induced positive states gradually became neutral states and mobility and subthreshold slope remained uncharged. When V_G = 3 V and 6 V, ΔV_{th} recovery rate was enhanced and ΔV_{th} became negative, implying that the enhanced recovery was due to the compensation of positive and negative gate-bias-induced charged states.

Under dynamic gate bias stress, however, positive V_G has only little influence on ΔV_{th} and the enhanced recovery behavior is not pronounced. As shown in Fig. 3-27, ΔV_{th} under dynamic bias stress with different base voltages (V_b = 0 V, 6 V, 8 V and 10 V) and fixed peak voltage ($V_p = V_G = V_{th}^{ini}$ - 20 V) was depicted as a function of effective stress time. The bipolar pulse width was fixed at 5 ms, duty cycle was 50 % which meant that peak voltage duration was equal to base voltage duration. When increasing base voltage from 0 V to 10 V, only a slight decrease of ΔV_{th} can be observed. Unlike steady-state bias as shown in Fig. 3-26, positive gate bias has only weak influence on ΔV_{th} under pulsed operation. This behavior can be observed more clearly in the following experiment when devices were stressed by positive pulsed gate bias.

3-4-5 Positive Pulsed Gate Bias Stress

In this section, the positive pulsed bias stress effect on pentacene-based TFTs was discussed. The positive pulsed bias stress was applied to device gate electrode with peak voltage as 6 V and base voltage as 0 V. The signal pulse width ranged from 2.5 ms to 3 μs, and the duty-cycle was 50% of the pulse period. ΔV_{th} under positive pulsed gate bias stress (ΔV_{th}^{AC+}) was plotted as a function of effective stress time as shown in Fig. 3-28. ΔV_{th} under positive steady-state gate bias stress (ΔV_{th}^{DC+}) was also plotted for comparison. Obviously, ΔV_{th}^{AC+} was much smaller than ΔV_{th}^{DC+} and has almost no frequency dependence. When ΔV_{th} ratio ($\Delta V_{th}^{AC+}/\Delta V_{th}^{DC+}$) versus pulse width was depicted in Fig. 3-29, no pulse width dependence was found. This result differs from that of negative pulsed bias stress as shown in Fig. 3-20 and Fig. 3-22. Under positive gate bias stress, a response time constant larger than 2.5 ms is expected.

Even though the electron injection has a large barrier from gold to pentacene, such a phenomenon should not be a limitation factor since ΔV_{th}^{DC+} is significant. The drastically suppressed ΔV_{th}^{AC+} may reflect a long response time of the electron traps. Gu *et al.*, proposed acceptor-like defects with long trap time in their studies, not excluding the existence of short trap time traps [15]. From our experiment results, it is evident that acceptor-like defects with long trap time dominate the ΔV_{th} under positive gate bias stress. As a result, when pulse width of dynamic gate bias stress is shorter than 2.5 ms, ΔV_{th} decreases to be almost 15% of its value under steady-state bias stress. It was not concluded that the electron trap response time is 2.5 ms. Pulsed signal with pulse width larger than 2.5 ms should be used to probe the trap response time. However, due to the noise limitation of the function generator in our experiment, dynamic gate bias stress effect with signal frequency lower than 200 Hz was not addressed in this paper.

3-5 Prolonged Light Irradiation Effect

3-5-1 Illumination System Setup

The light-emitting diode (LED) backlight was used as the light source to irradiate the sample from the top with a fixed brightness as 500 nits. The device was measured at room temperature in ambient air. The Fig. 3-30 shows the illumination system and the device structure. The threshold voltage (V_{th}) was extracted by using the linear region equation. The ΔV_{th} is defined as $V_{th} - V_{th}^{ini}$ where V_{th}^{ini} is the initial threshold voltage before illumination or bias stress.

3-5-2 Gate Bias Suppressed Light-Induced Threshold Voltage Shift

Firstly, the suppression of light-induced ΔV_{th} by applying negative gate-bias stress is demonstrated. As shown in Fig. 3-31, the initial transfer characteristics (line) and those after a 500-sec illumination (symbols) are compared. Without bias stress, the transfer characteristics obviously shift +2.04 V after a 500-sec illumination. When a gate bias of -10 V is applied during illumination, the transfer characteristic shift is significantly suppressed. Threshold voltage and mobility (in the inset) extracted from the transfer characteristics after a 500-sec illumination are plotted as a function of gate-bias stress voltage in Fig. 3-32. Before and after a 500–sec illumination with different gate bias, unchanged mobility indicates a constant device temperature since the field-effect mobility is expected to increase with temperature in organic semiconductors [16]. Obviously, ΔV_{th} is effectively suppressed by increasing the gate bias from 0 V to -15 V. ΔV_{th} in dark under negative gate bias stress is also shown by the dash line in Fig. 3-32. The gate-bias influence on light-induced ΔV_{th} is due to the compensation between the bias-induced positive charged states and the light-induced negative charged states. A similar compensation phenomenon was proposed by Gu *et al.* when studying ΔV_{th} recovery behavior [15].

3-5-2 Drain Bias Modulation on Light-Induced Threshold Voltage Shift

Then, the drain-bias influence on the light-induced ΔV_{th} was studied when source and gate electrodes were grounded. As shown in Fig. 3-33, initial transfer characteristics and those after a 500-sec illumination with and without drain-bias stress are compared. The shift of the transfer characteristics was suppressed by applying positive drain bias. Figure 3-34 shows the extracted threshold voltage and the mobility (in the inset) as a function of drain-bias stress voltage after a 500-sec illumination. The results are similar to those in Fig. 3-34. However, the mechanism should not be the compensation effect as described above because the drain-bias stress in dark only causes slight threshold voltage shift as shown by the dash line in Fig. 3-34.

Under illumination, the electron trapping effect competes with the electron-hole recombination effect. It is plausible that when light-induced holes are removed from pentacene through the drain contact, less recombination probability gives rise to more electron trapping and hence larger ΔV_{th}. A band diagram from source to drain is depicted to explain the proposed mechanism. As shown by case A in Fig. 3-35(a), when a positive drain bias is applied, the lowered Fermi energy (E_F) in the drain electrode leads to a downward band bending of pentacene near the drain side. The band bending confines light-induced holes in the channel to recombine with light-induced electrons. As a result, the electron trapping is suppressed and the ΔV_{th} is reduced.

If the proposed mechanism is correct, the following three cases will also exist. As shown by case B in Fig. 3-35(b), the negative drain bias creates upward band bending in pentacene and helps light-induced holes to flow out from pentacene into the drain electrode. Enlarged light-induced ΔV_{th} is expected. For case C in Fig. 3-35(c), applying positive source and drain bias simultaneously should further confine the light-induced holes and reduce ΔV_{th} when comparing with case A. Applying negative source and drain biases as shown by case D in Fig. 3-35(d), on the contrary, leads to a more significant ΔV_{th} when comparing with case B. These expected phenomena are successfully observed in Fig. 3-36 when the light-induced ΔV_{th} is plotted as a function of applied bias (V_{app}) in case A to case D.

3-5-3 Bias Enhanced Memory Effect

After removing irradiation, the source and drain biases also help sustain the light-induced ΔV_{th}. The recovery behavior of the light-induced ΔV_{th} is depicted in Fig. 3-37. With almost identical initial light-induced ΔV_{th}, the recovery of ΔV_{th} after light removal is plotted as a function of recovery time with different bias conditions. It is known that after light removal, the equilibrium condition in pentacene is rebuilt. For devices recover with $V_D = V_S = V_G = 0$ V, holes produced by thermal generation or by source and drain injection recombine with trapped electrons in pentacene. Light-induced ΔV_{th} is eliminated with recovery time as shown by the white circle symbols in Fig. 3-37. For devices recover with $V_D = V_S = -15$ V and $V_G = 0$ V, however, the negative drain and source bias impede the injection of holes. The trapped electrons in pentacene are mostly kept and the light-induced ΔV_{th} is sustained. In our experiment, the light-induced ΔV_{th} is sustained for over 5000 seconds and is erased by removing the drain and source biases or by applying positive drain and source biases. The measurement of the device transfer characteristics every 500 seconds does not affect the ΔV_{th} signal.

3-6 Conclusions

In this chapter, the usual reliability issues of OTFT in bias stress measurement or under prolonged illumination are discussed. Based on the drain bias influence on V_{th} of OTFTs, the shift of V_{th} of OTFTs with SiO_2 dielectric is proportional to the channel charge amount as in a-Si:H TFTs. For threshold voltage shift of OTFT under positive and negative pulsed gate bias stress, influences of pulse width, relaxing duration, and trap response time on threshold voltage shift was investigated. For negative pulsed bias stress, the pulse width effect on device ΔV_{th} can be well explained by using RC equivalent circuit and simulated with an equation (Eq. (3-4)) derived from state creation mechanism. For positive pulsed bias stress, drastically suppressed ΔV_{th} without pulse width dependence was obtained. Since devices under positive gate bias were operated in off-state, a slow accumulation of electron carriers or a slow response of acceptor-like traps were plausible reasons for the long response time (> 2.5 ms). Finally, threshold voltage shift affected by light-induced electron concentration was studied. It demonstrated that the threshold voltage shift obviously depends on light-induced electrons. Using drain bias and source bias can effectively adjust the amount of accumulated electrons in channel even when the gate electrode was connected to ground.

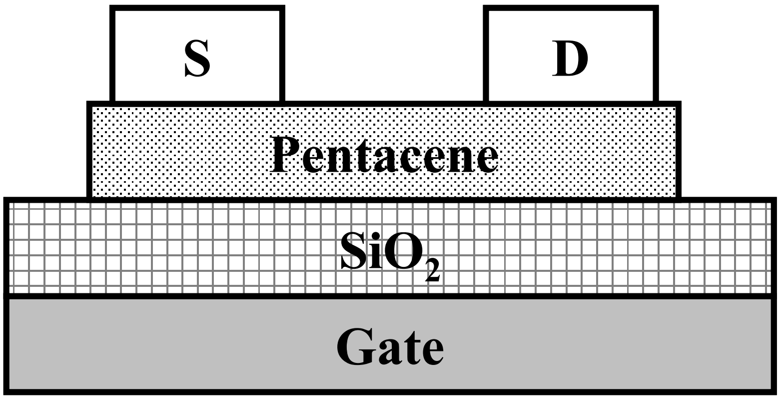


Fig. 3-1 Schematic structure of top-contact pentacene-based thin film transistor. A 100-nm-thick thermal oxide is used as gate dielectric.

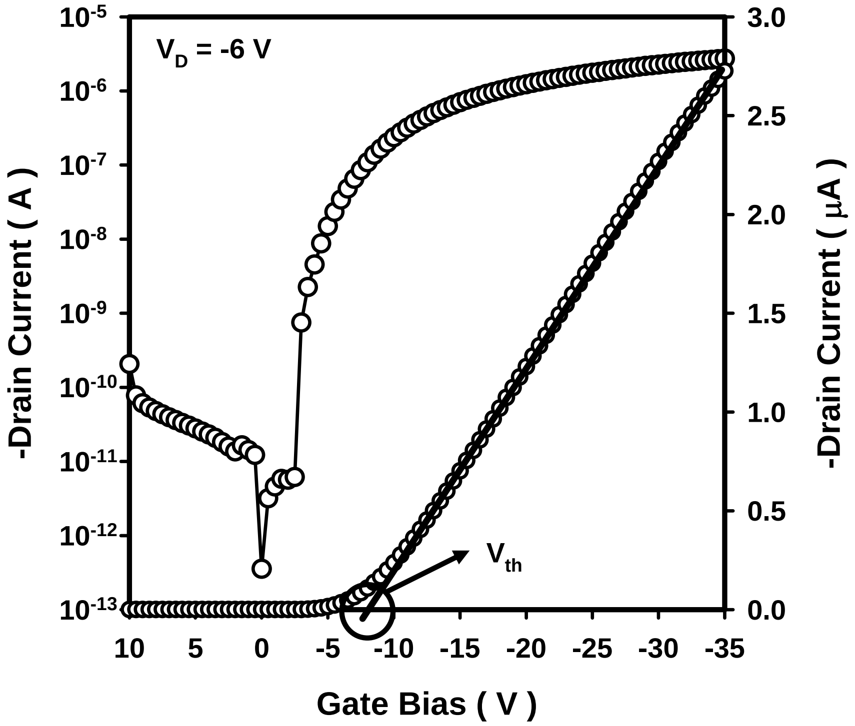


Fig. 3-2 The linear-region initial transfer characteristic of OTFT. The gate bias is swept from 10 V to -35 V when drain bias is kept at -6 V. The threshold voltage (V_{th}) is extracted by using the linear region equation.

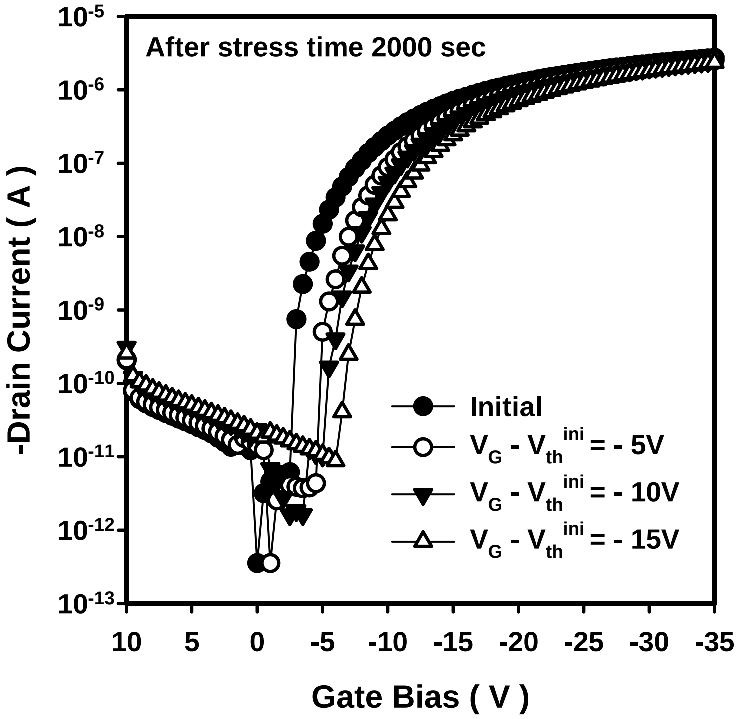


Fig. 3-3 The linear-region transfer characteristics of OTFTs before and after 2000-sec gate bias stress. The stress conditions are: $V_G - V_{th}^{ini}$ = -5 V, -10 V, and -15 V, V_{DS} = 0 V.

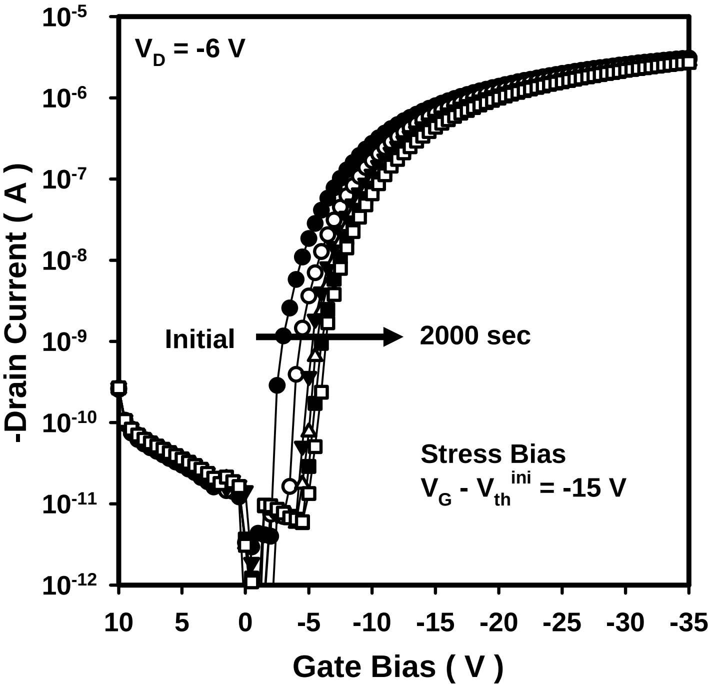


Fig. 3-4 (a) The evolution of linear-region transfer characteristics when y-axis is in logarithm scale during a 2000-sec gate bias stress. The stress conditions are: $V_G - V_{th}^{ini}$ = -5 V, -10 V, and -15 V, V_{DS} = 0 V.

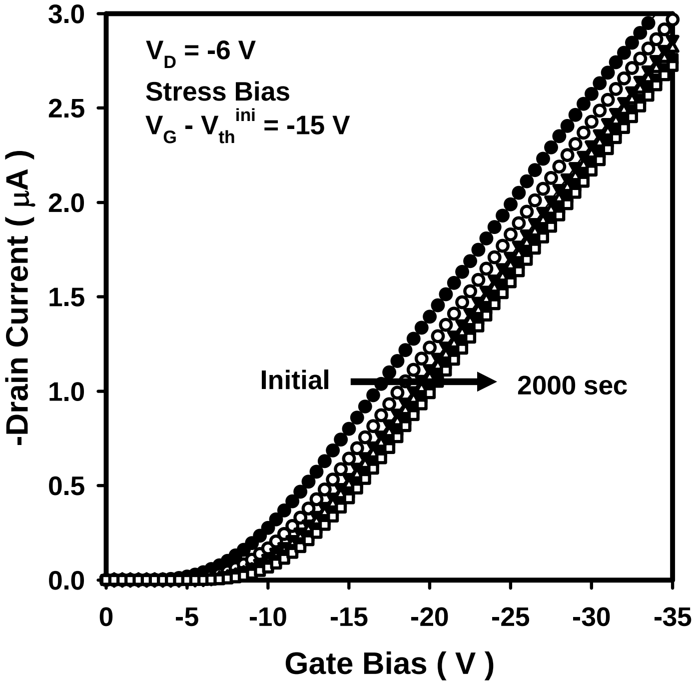


Fig. 3-4 (b) The evolution of linear-region transfer characteristics when y-axis is in linear scale during a 2000-sec gate bias stress. The stress conditions are: $V_G - V_{th}^{ini}$ = -5 V, -10 V, and -15 V, V_{DS} = 0 V.

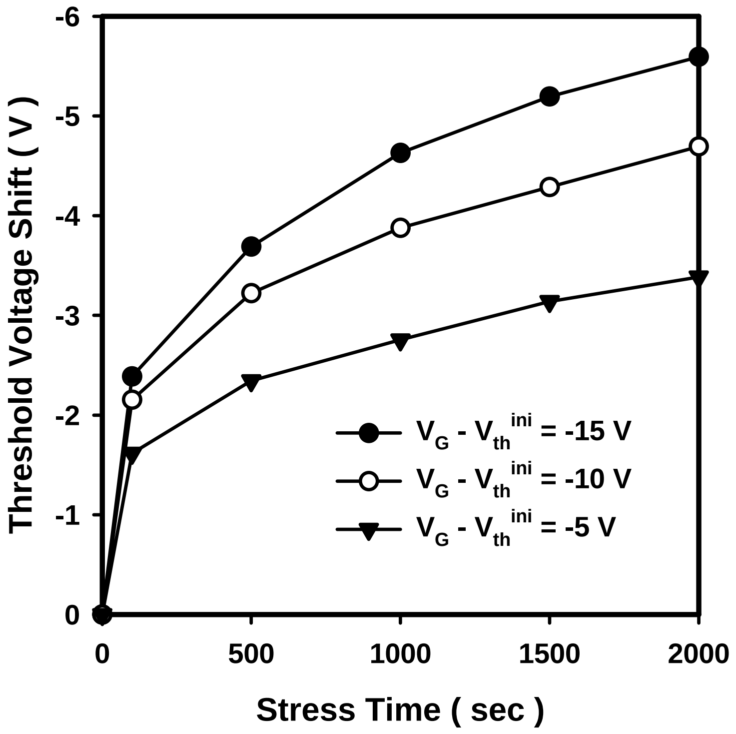


Fig. 3-5 (a) the shift of threshold voltage as a function of stress time when gate stress bias ($V_G - V_{th}^{ini}$) are -5 V, -10 V, and -15 V while V_{DS} is 0 V.

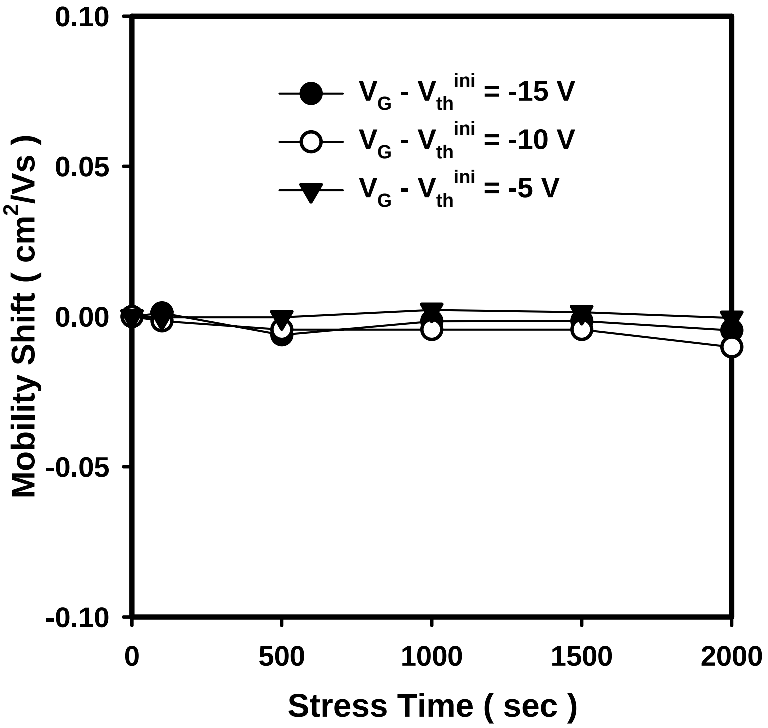


Fig. 3-5 (b) the shift of field-effect mobility as a function of stress time when gate stress bias ($V_G - V_{th}^{ini}$) are -5 V, -10 V, and -15 V while V_{DS} is 0 V.

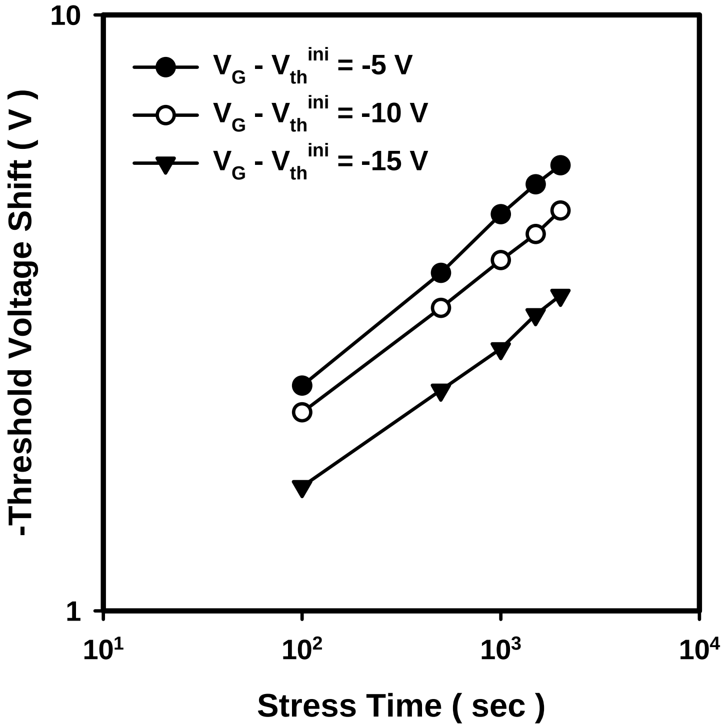


Fig. 3-6 The shift of threshold voltage as a function of stress time in logarithm scale when gate stress bias ($V_G - V_{th}^{ini}$) are -5 V, -10 V, and -15 V while V_{DS} is 0 V.

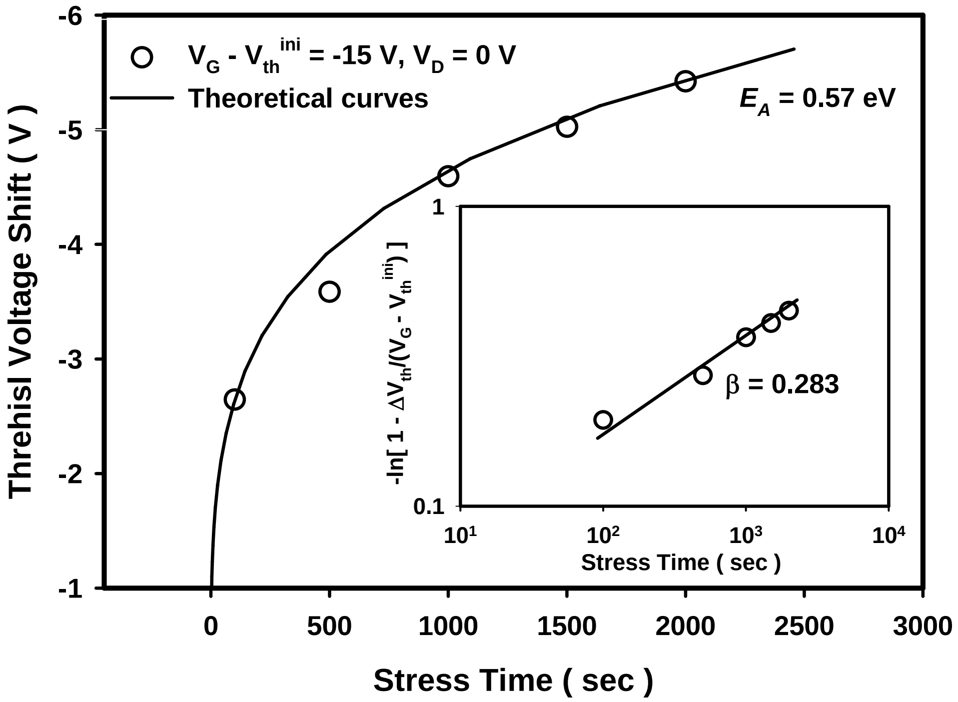


Fig. 3-7 The threshold voltage shift as a function of stress time. The simulated curve given by Eq.(1) is plotted with the parameters (β = 0.363, E_A = 0.56 eV and τ_t = 3.61×10^4 sec). The dispersion parameter β can be obtained by plotting $\log\left\{-\ln\left[1-\Delta V_{th,D}(Q_{G0}/Q_G)/(V_{GS}-V_{th}^{ini})\right]\right\}$ as a function of log(t) as shown in the inset. Stress bias condition: gate stress bias ($V_G - V_{th}^{ini}$) is -15 V while drain bias (V_{DS}) is 0 V

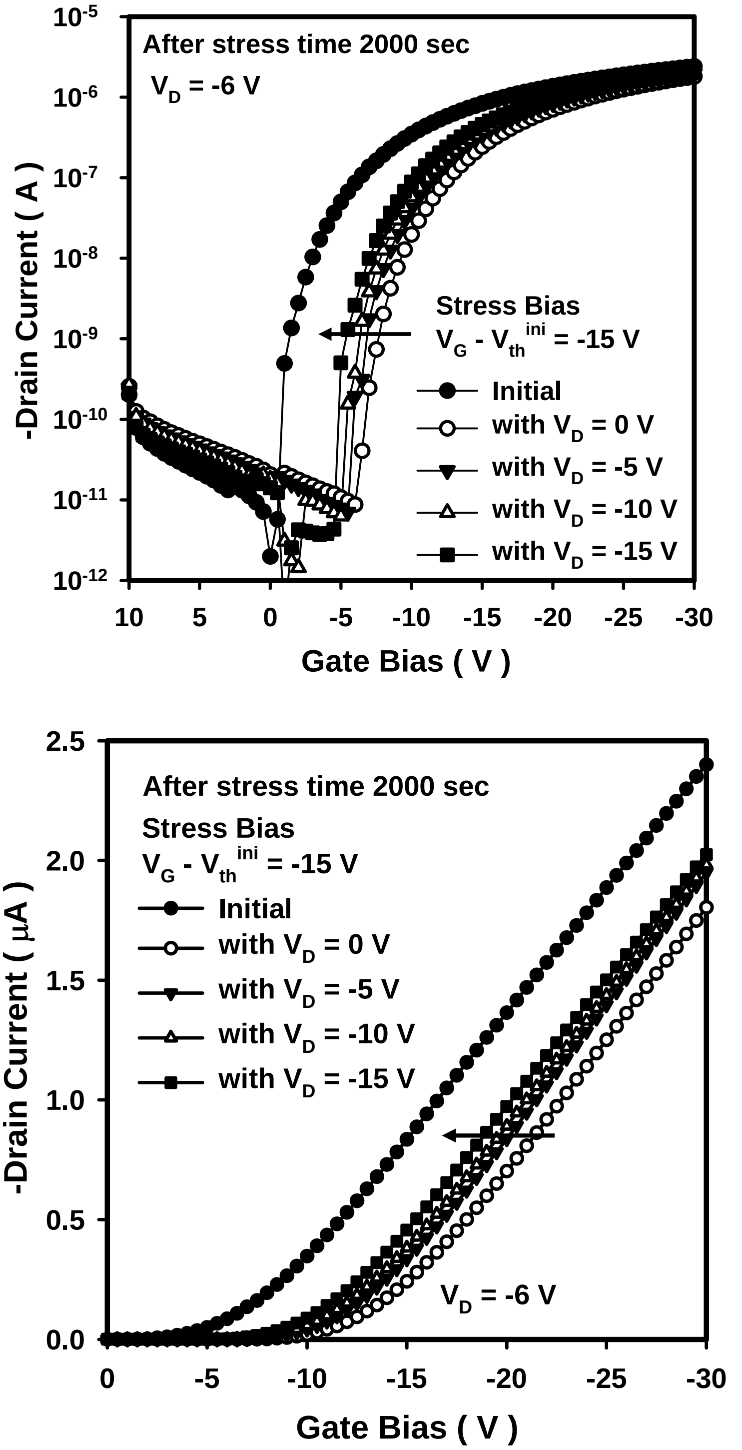


Fig. 3-8 (a) and (b) The linear-region transfer characteristics of OTFT before and after 2000-sec gate bias stress when different drain biases (V_{DS} = 0 V, 5 V, 10 V, and 15 V) are applied to devices while gate bias ($V_G - V_{th}^{ini}$) is fixed at -15 V.

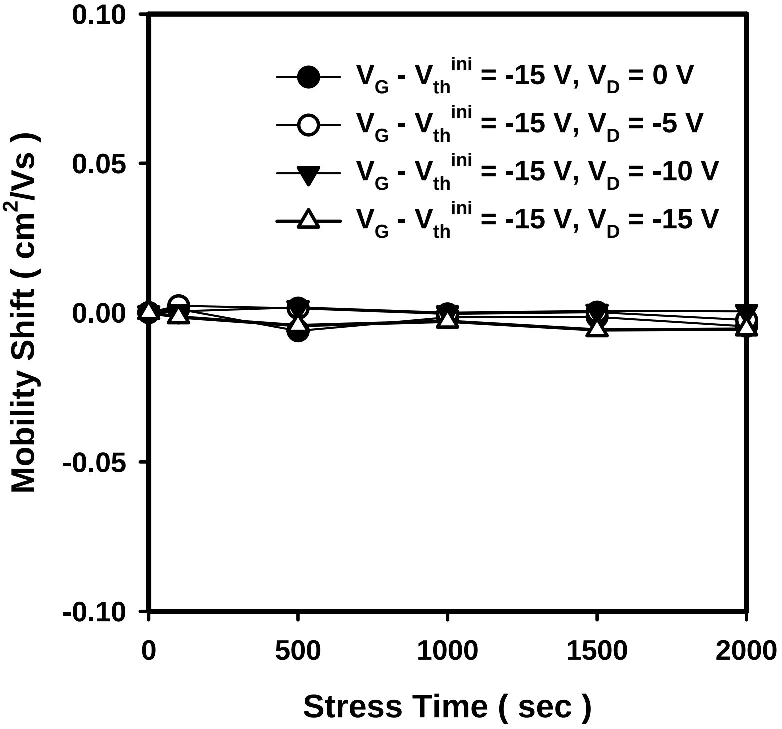


Fig. 3-9 The shift of mobility as a function of stress time when different drain biases (V_{DS} = 0 V, 5 V, 10 V, and 15 V) were added to the bias-stress measurement while the gate bias was fixed as $V_G - V_{th}^{ini}$ = -15 V.

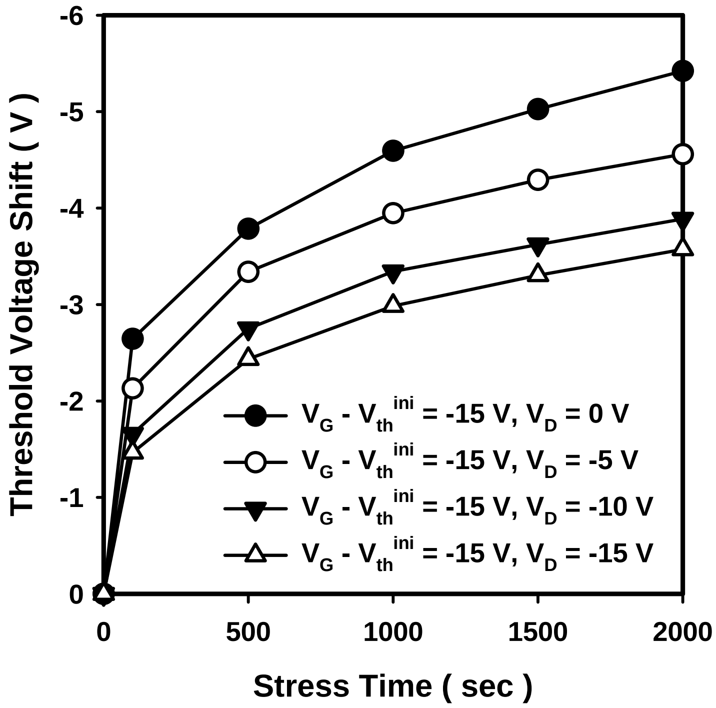


Fig. 3-10 The shift of threshold voltage as a function of stress time when different drain biases (V_{DS} = 0 V, 5 V, 10 V, and 15 V) were added to the bias-stress measurement while the gate bias was fixed as $V_G - V_{th}^{ini}$ = -15 V.

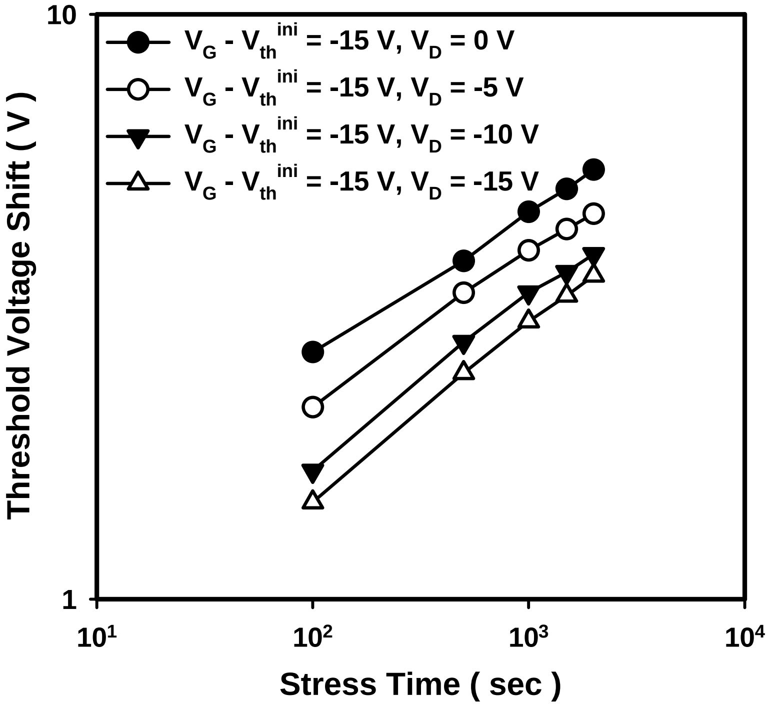


Fig. 3-11 The shift of threshold voltage as a function of stress time in logarithm scale when different drain biases (V_{DS} = 0 V, 5 V, 10 V, and 15 V) were added to the bias-stress measurement while the gate bias was fixed as $V_G - V_{th}^{ini} = -15$ V.

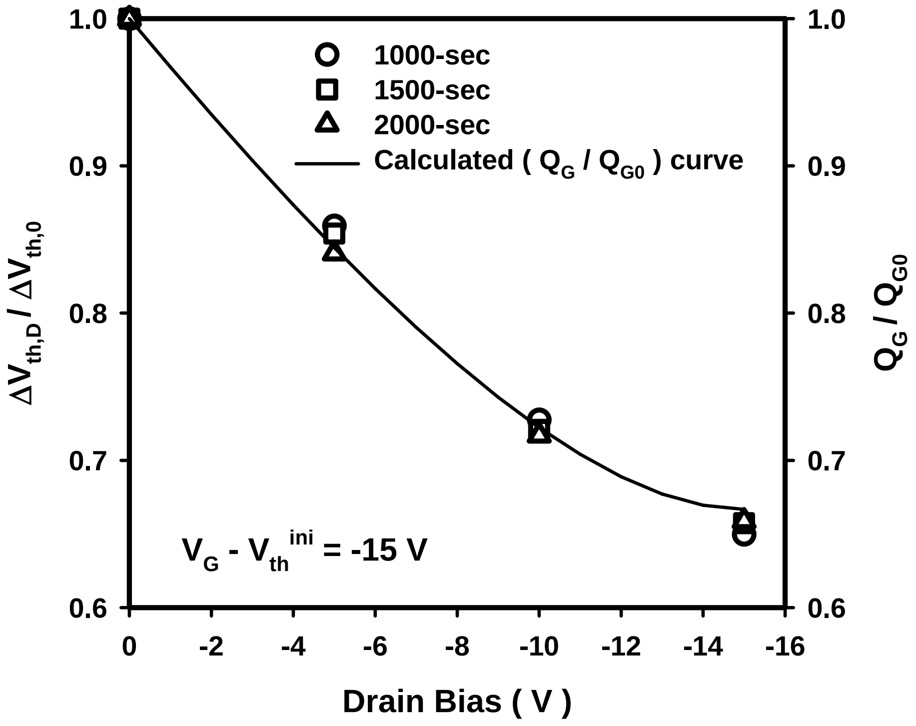


Fig. 3-12 The threshold voltage shift ratio ($\Delta V_{th,D}/\Delta V_{th,0}$) and the normalized channel charge (Q_G / Q_{G0}) as a function of stressed drain bias.

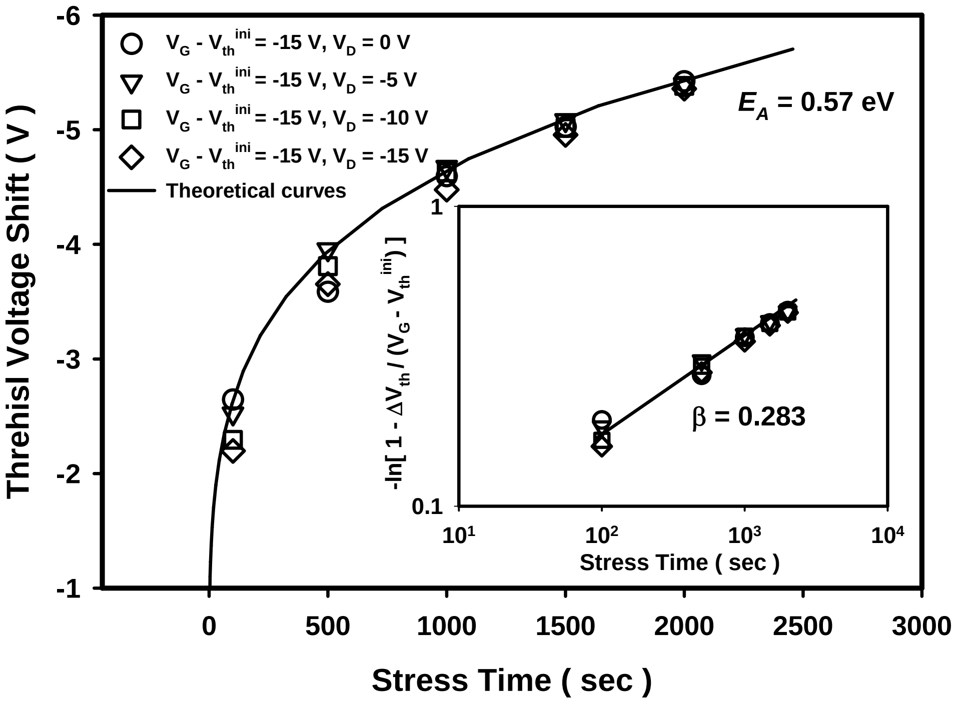


Fig. 3-13 The restored threshold voltage shift as a function of stress time. The theoretical curve given by $\Delta V_{th,D} \times (Q_{G0}/Q_G) = (V_G - V_{th}^{ini})\left\{1-\exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]\right\}$ is also plotted with the parameters given in Ref. [10]. The dispersion parameter β can be obtained by plotting $\log\left\{-\ln\left[1-\Delta V_{th,D}(Q_{G0}/Q_G)/(V_{GS}-V_{th}^{ini})\right]\right\}$ as a function of log(t) as shown in the inset.

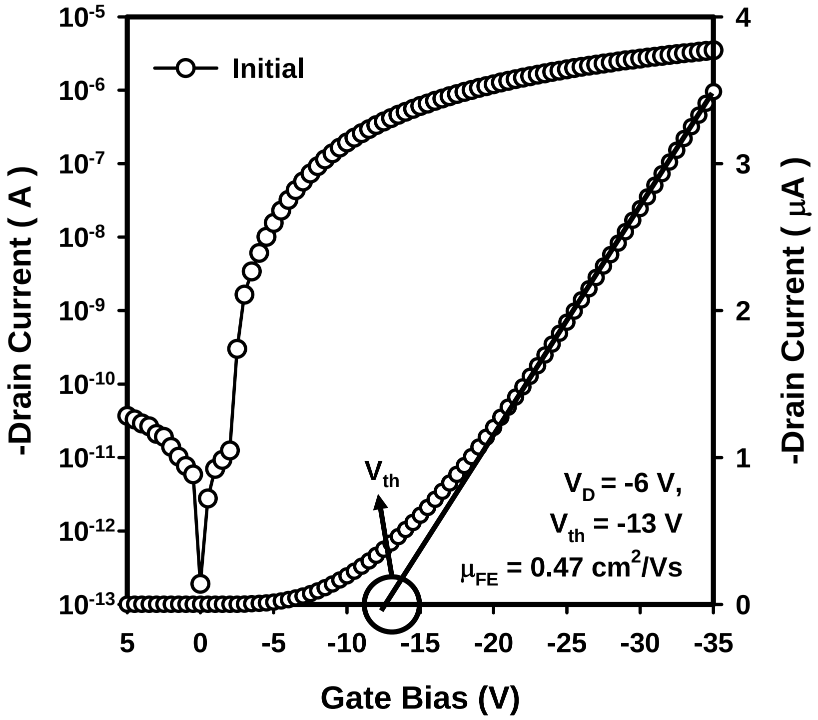


Fig. 3-14 The linear-region initial transfer characteristic of OTFT. The gate bias is swept from 10 V to -35 V when drain bias is kept at -6 V. The threshold voltage (V_{th}) is extracted by using the linear region equation.

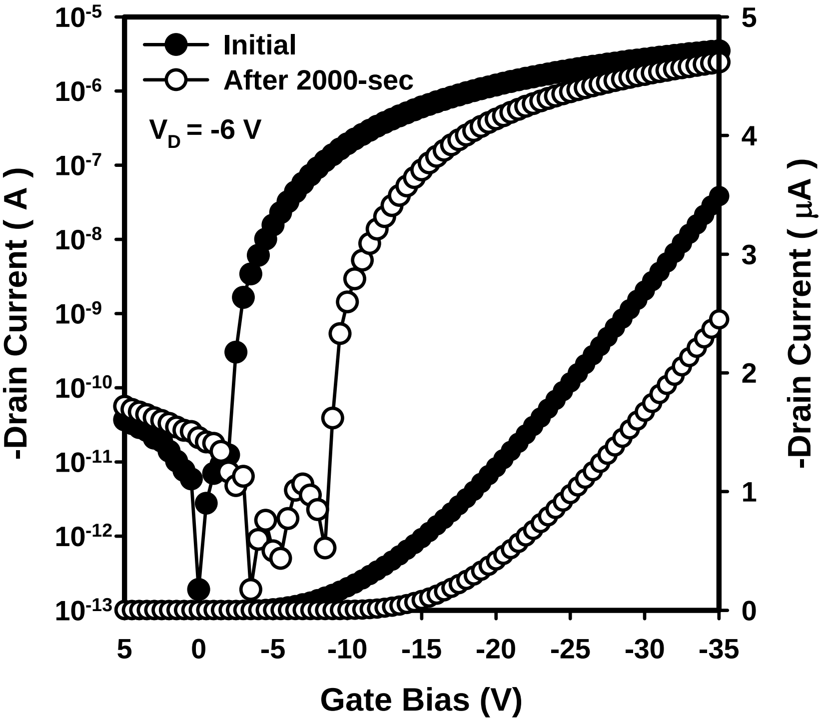


Fig. 3-15 The linear-region transfer characteristics of OTFTs before and after 2000-sec gate bias stress. The stress conditions are: $V_G - V_{th}^{ini} = -20$ V, $V_{DS} = 0$ V.

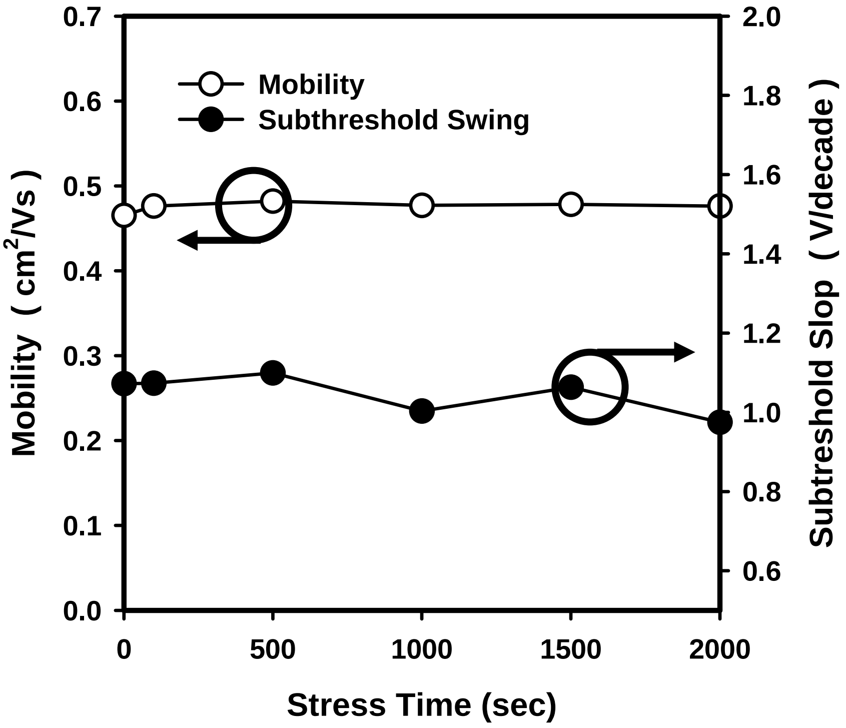


Fig. 3-16 The shift of mobility and the shift of subthreshold slopes as a function of stress time during gate bias stress. The stress conditions are: $V_G - V_{th}^{ini}$ = -20 V, V_{DS} = 0 V.

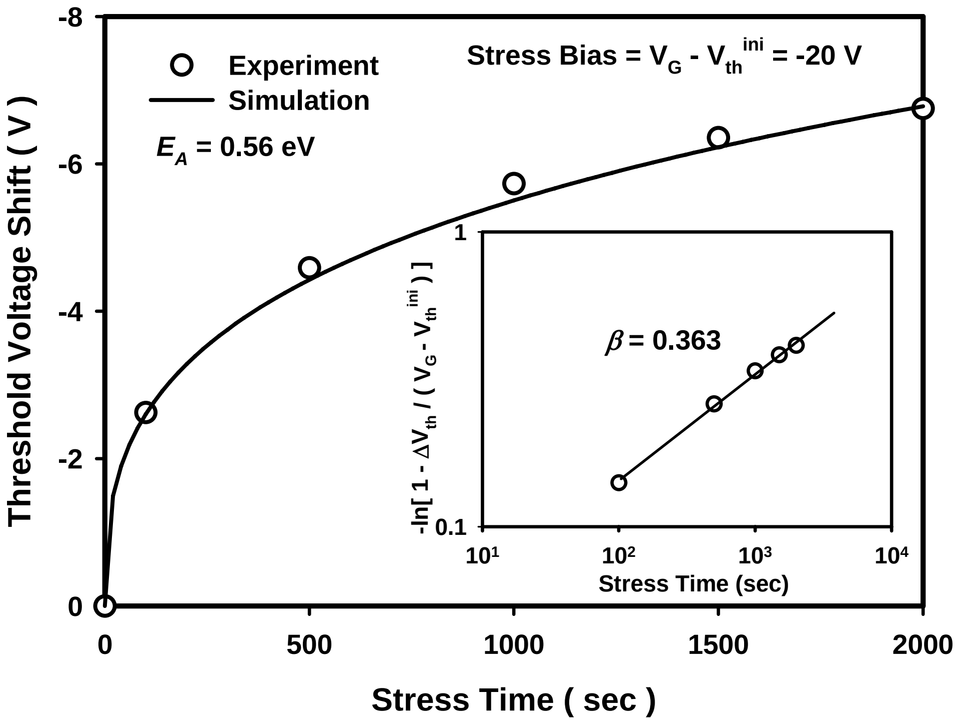


Fig. 3-17 The threshold voltage shift as a function of stress time. The simulated curve given by Eq.(1) is also plotted with the parameters (β = 0.363, E_A = 0.56 eV). The dispersion parameter β can be obtained by plotting $log\left\{-ln\left[1-\Delta V_{th}(Q_{G0}/Q_G)/(V_{GS}-V_{th}^{ini})\right]\right\}$ as a function of log(t) as shown in the inset.

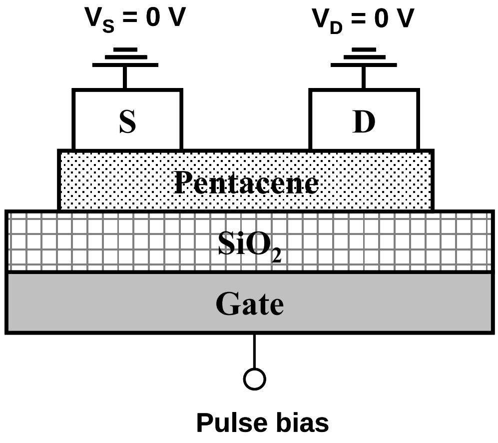


Fig. 3-18 The cross-section of pentacene-based TFTs; pulsed voltage is applied to the gate electrode and source and drain were grounded.

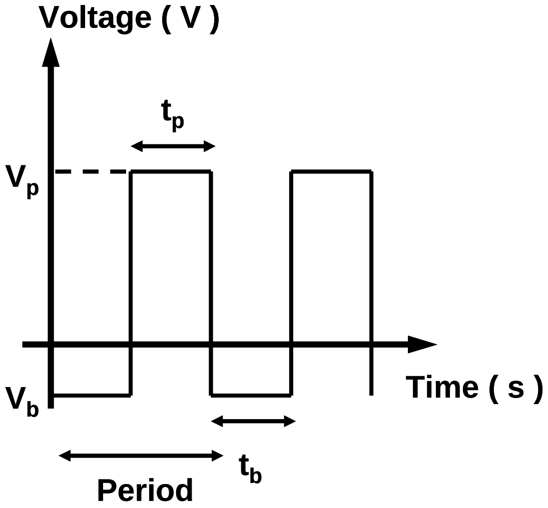


Fig. 3-19 The scheme of pulse bias function.

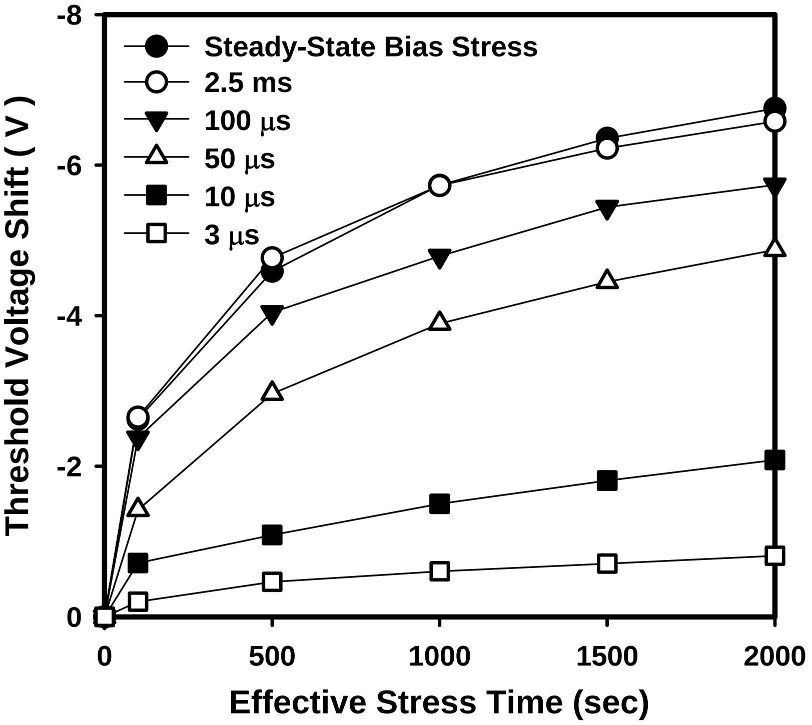


Fig. 3-20 The threshold voltage shift curves under steady-state gate bias stress and negative pulsed gate bias stress are plotted as a function of effective stress time. Pulsed gate bias conditions: the pulse width ranges from 2.5 ms to 3 µs, the duty-cycle is 50% of the pulse period, peak voltage = $V_G = V_{th}^{ini}$ - 20 V, V_{DS} = 0 V, and based voltage = 0 V. Steady state bias stress condition: $V_G = V_{th}^{ini}$ - 20 V, V_{DS} = 0 V.

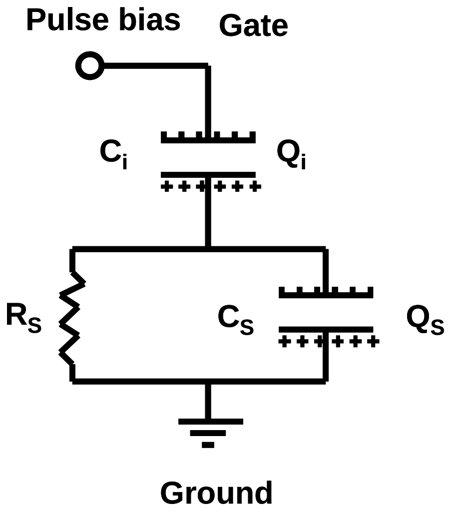


Fig. 3-21 The equivalent circuit of pentacene-based TFTs is used to simulate the negative pulsed gate bias stress effect.

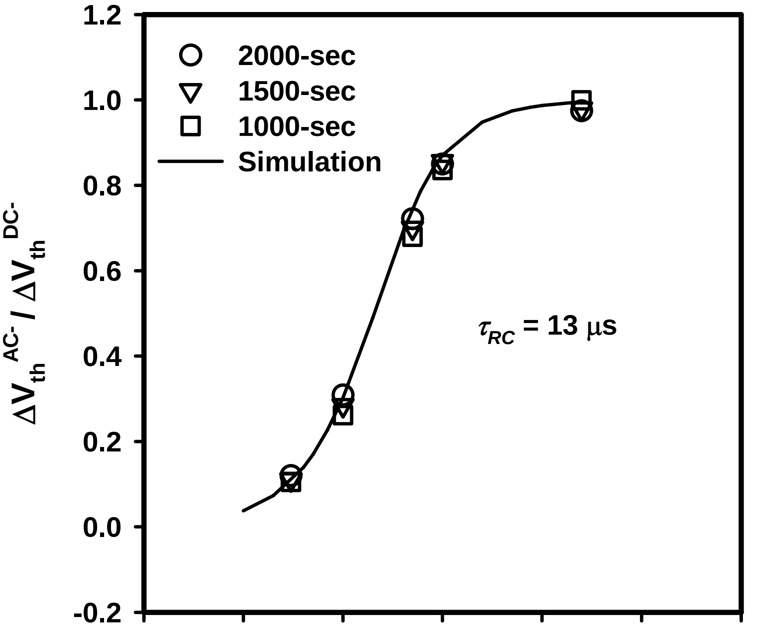


Fig. 3-22 The ΔV_{th} ratio ($\Delta V_{th}^{AC-}/\Delta V_{th}^{DC-}$) as a function of pulse width. Response time τ_{RC} can be extracted by fitting the experimental data with the simulated curve calculated from Eq. (3).

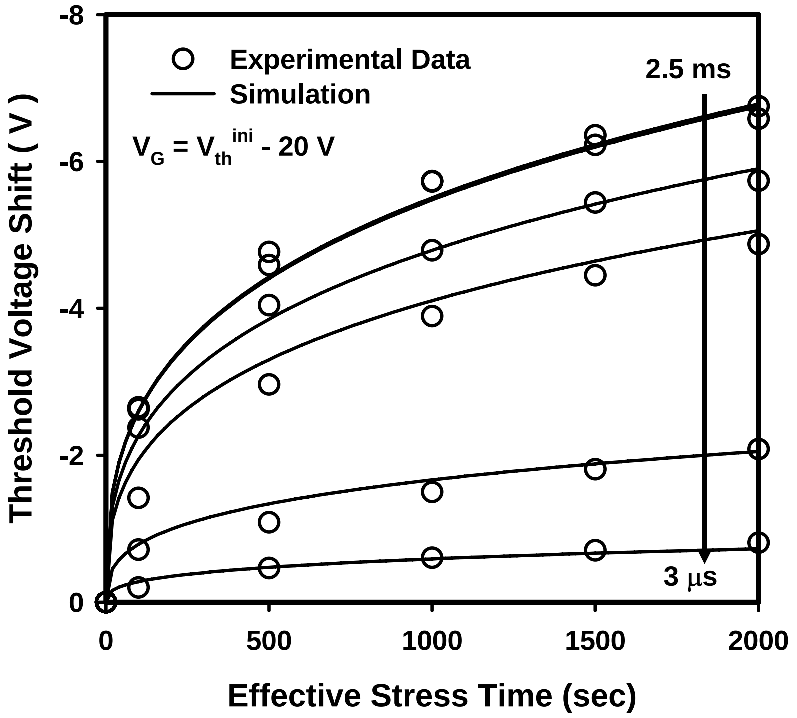


Fig. 3-23 The calculated curves obtained from Eq.(4) and the experimental data. The parameters of modified model are $\beta = 0.363$, $E_A = 0.56$ eV and $\tau_{RC} = 13$ µs.

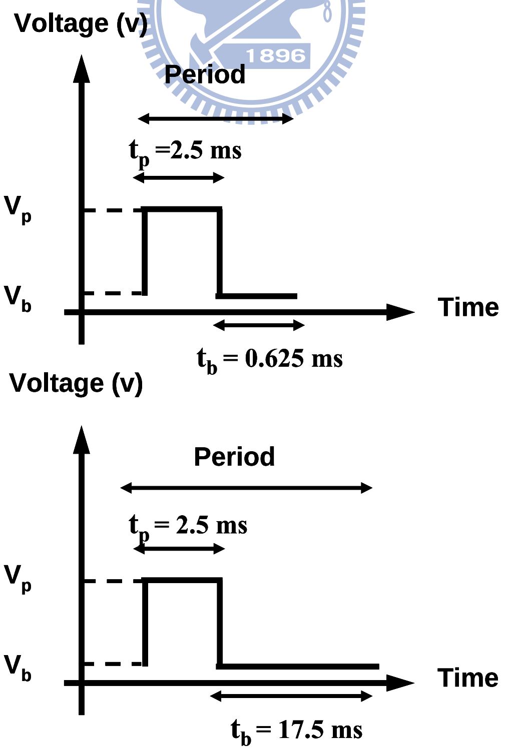


Fig. 3-24 The waveforms of pulsed bias are formed by fixed peak voltage duration (t_p = 2.5 ms) and various base voltage duration (t_b = 0.625 ms to 17.5 ms).

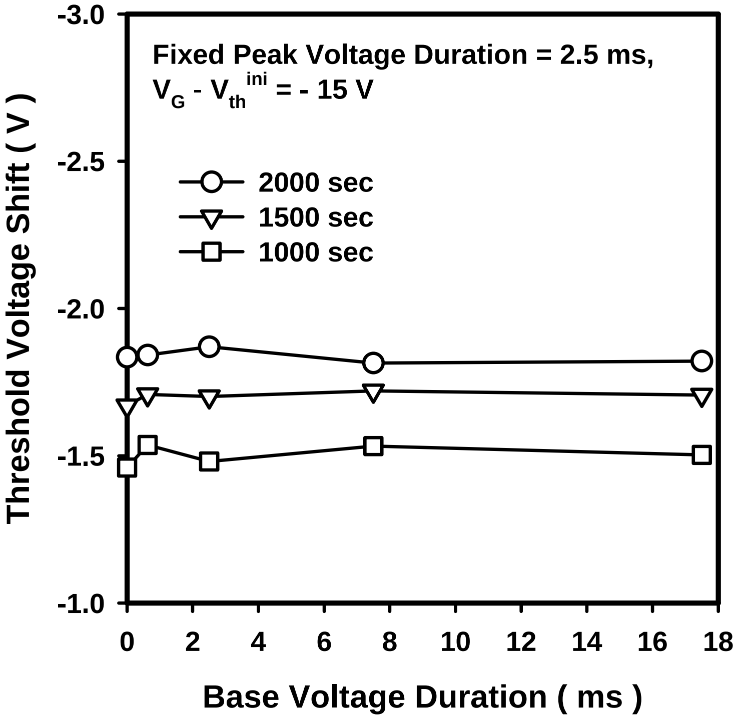


Fig. 3-25 ΔV_{th} curves with effective stress time as 2000 sec, 1500 sec and 1000 sec are plotted as a function of base voltage duration. The bias stress conditions: $V_G - V_{th}^{ini} = -15$ V, $V_D = V_S = 0$ V.

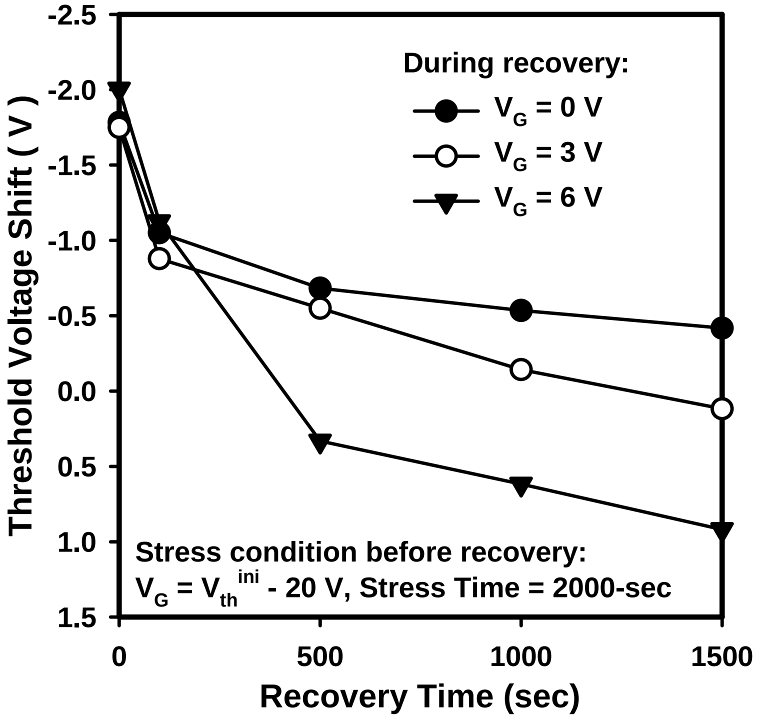


Fig. 3-26 After 2000-sec stress with $V_G = V_{th}^{ini} - 20$ V, the ΔV_{th} plotted as a function of recovery time when $V_G = 0, 3, 6$ V during recovery.

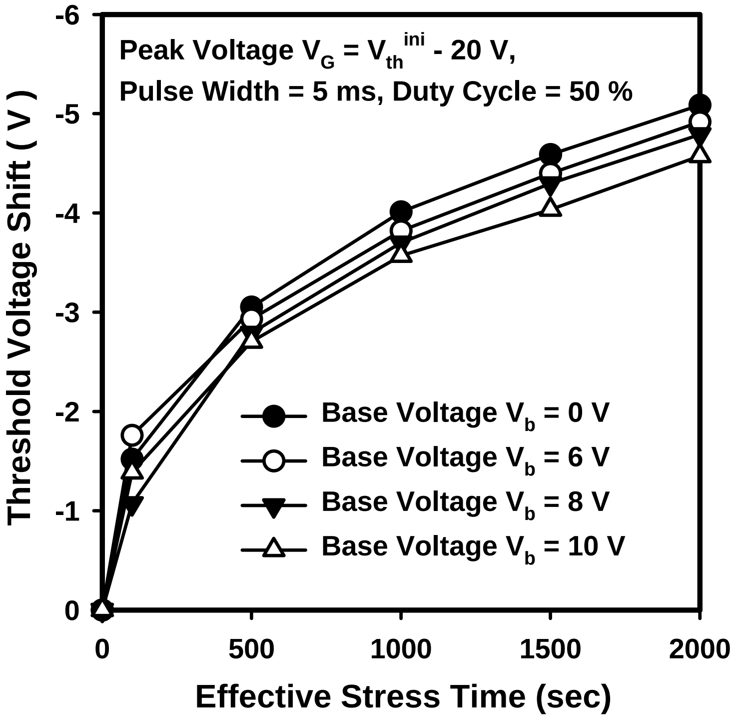


Fig. 3-27 ΔV_{th} curves under bipolar pulsed bias stress as a function of effective stress time. The stress conditions: Peak voltage = $V_G = V_{th}^{ini}$ - 20 V, V_{DS} = 0 V, Based voltage = 0, 6, 8, and 10 V. The duty cycle is 50 % of the pulse period. Pulse width was fixed at 5 ms.

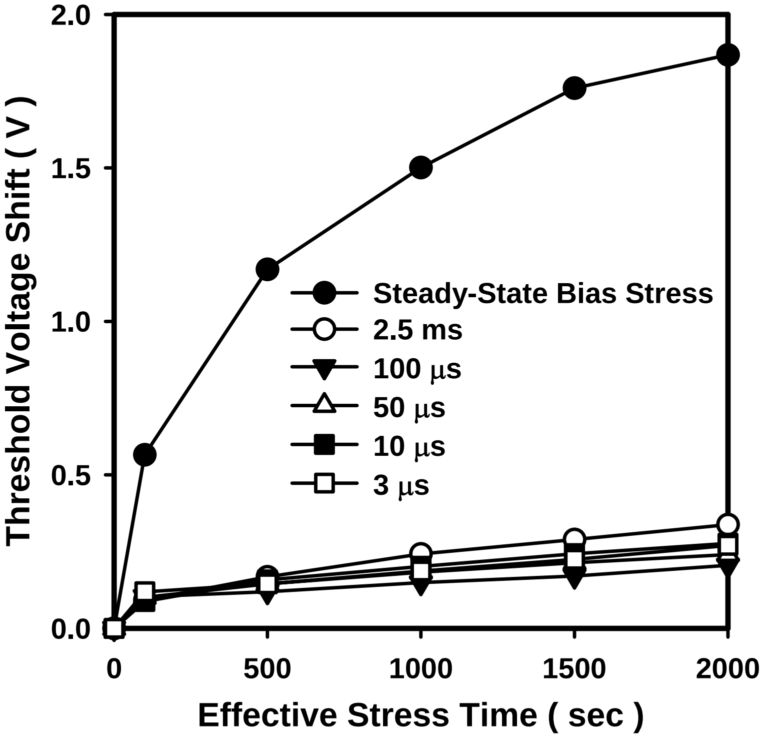


Fig. 3-28 The threshold voltage shift curves under steady-state gate bias stress and positive pulsed gate bias stress as a function of stress time are shown. The pulsed gate bias stress conditions: the pulse width ranges from 2.5 ms to 3 µs, the duty-cycle is 50% of the pulse period, peak voltage = V_G = 6 V, V_{DS} = 0 V, and based voltage = 0 V. Steady-state bias stress condition: V_G = 6 V, V_{DS} = 0 V.

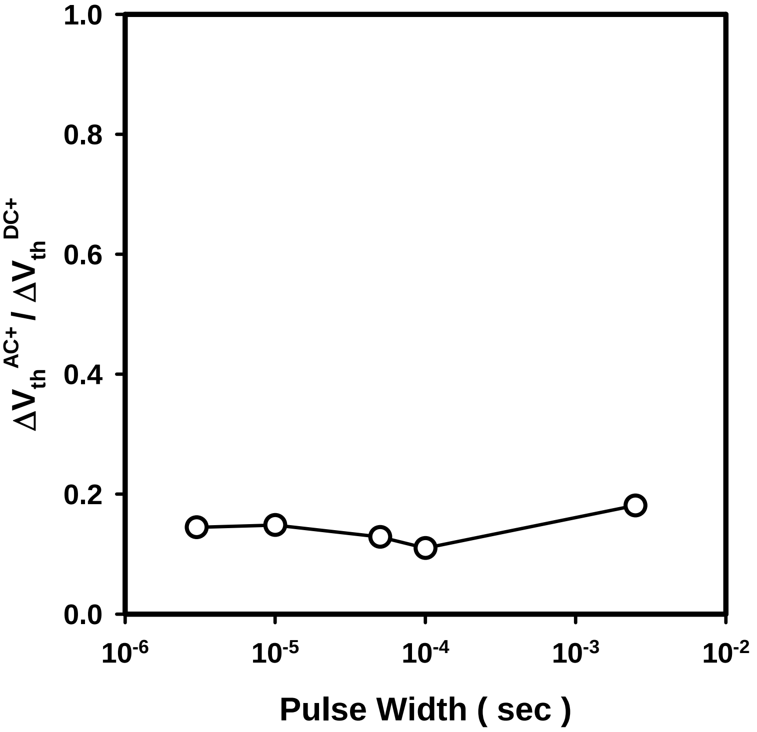


Fig. 3-29 ΔV_{th} ratio ($\Delta V_{th}^{AC+}/\Delta V_{th}^{DC+}$) as a function of pulse width.

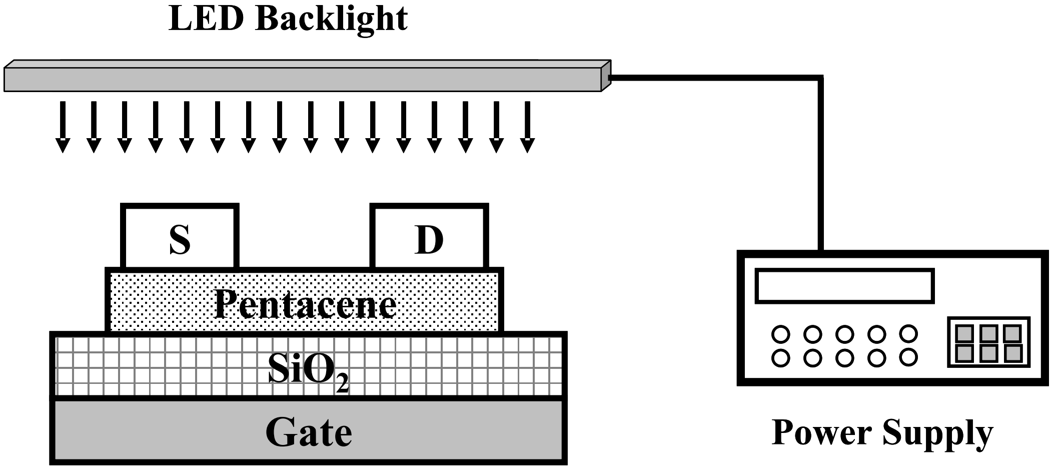


Fig. 3-30 The illumination system and conventional top-contact bottom-gate pentacene-based TFT. A 100-nm thickness of SiO_2 is served as gate dielectric.

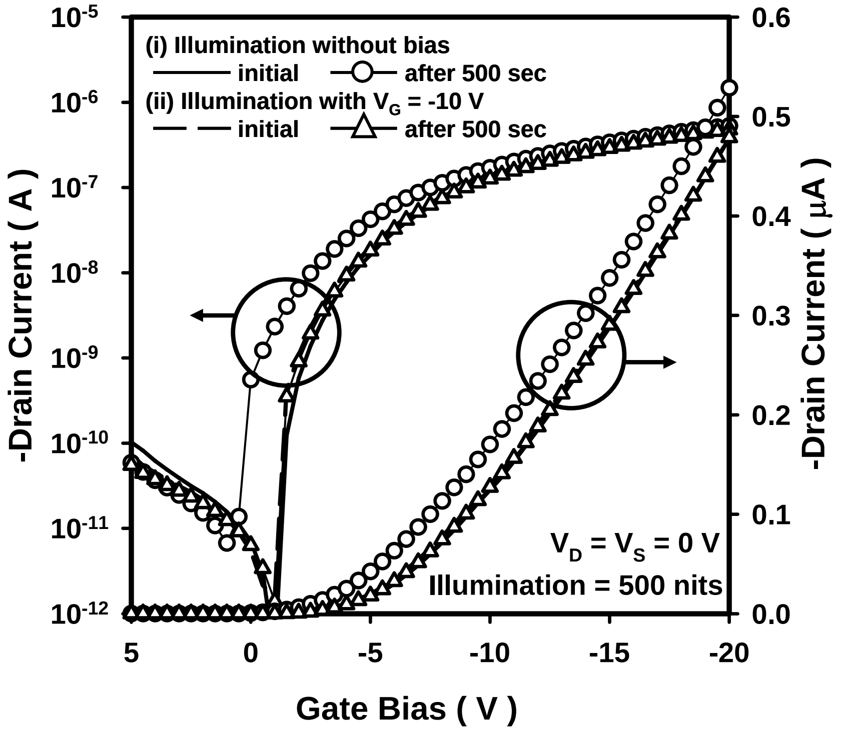


Fig. 3-31 The transfer characteristics of OTFTs before and after a 500-sec illumination with gate bias. The stress conditions are: V_G = 0 V and -10 V, V_{DS} = 0 V.

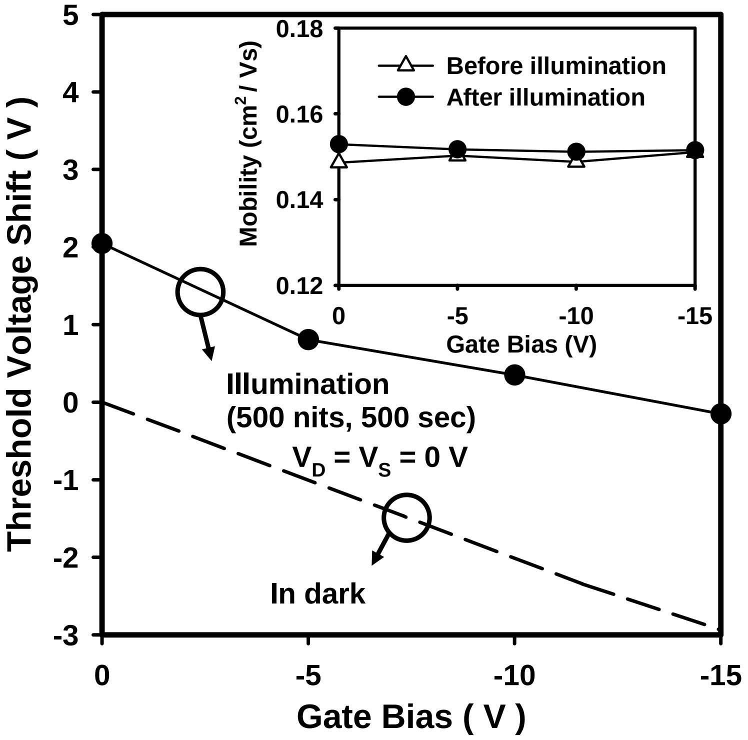


Fig. 3-32 Threshold voltage shift and mobility (in the inset) under illumination as a function of negative gate bias. The threshold voltage shift under gate-bias stress in dark is shown by the dash line.

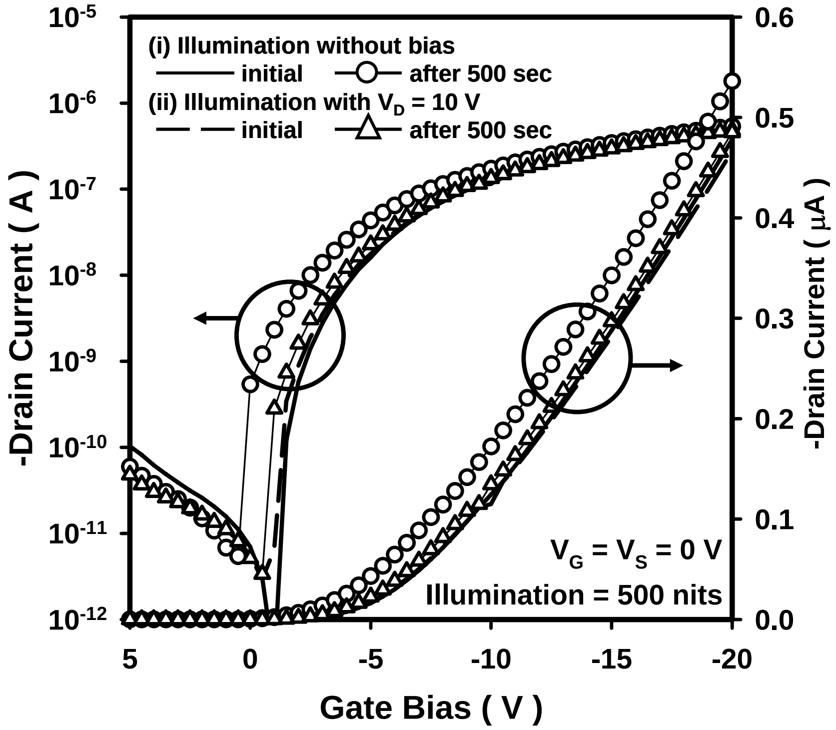


Fig. 3-33 The transfer characteristics of OTFTs before and after a 500-sec illumination with drain bias. The stress conditions are: $V_D = 0$ V and 10 V, $V_{GS} =$ 0 V.

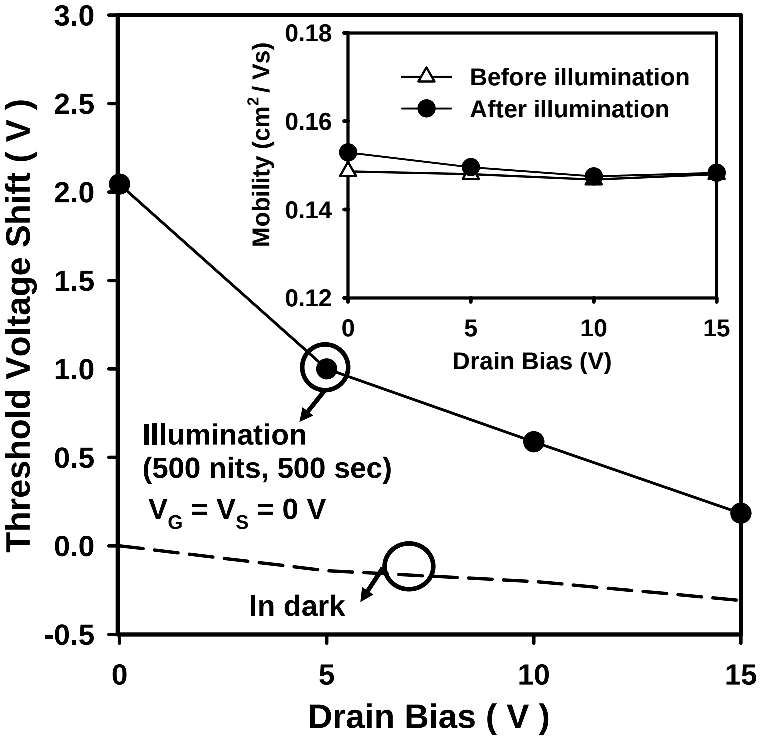
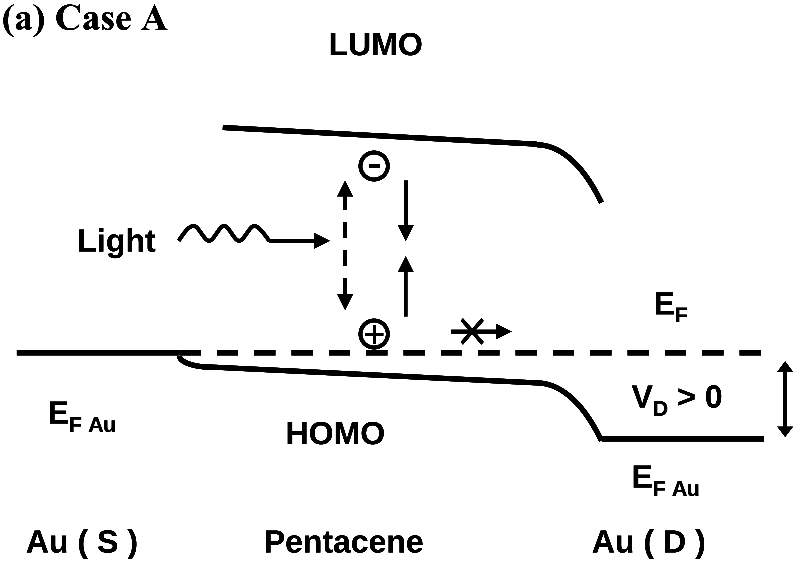
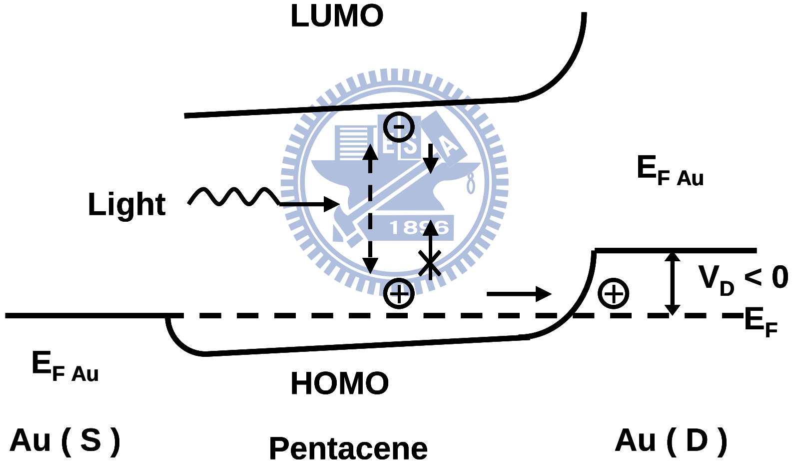


Fig. 3-34 Threshold voltage and mobility (in the inset) as a function of positive drain bias. The threshold voltage shift under drain-bias stress in dark is shown by the dash line.

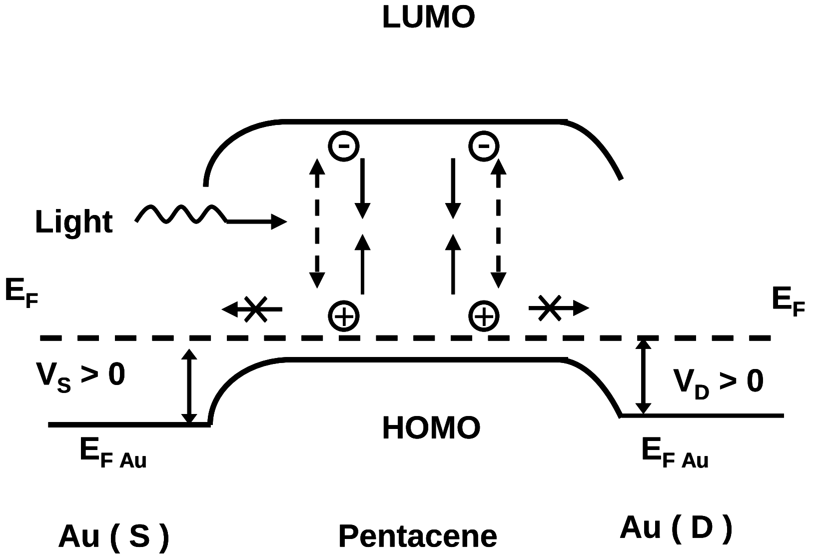
(a) Case A



(b) Case B



(c) Case C



(d) Case D

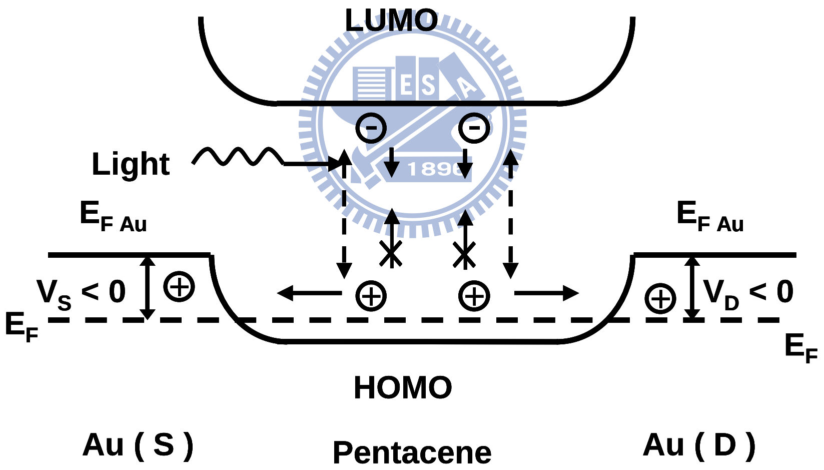


Fig. 3-35 Energy band diagram of organic TFTs from source to drain when devices are under illumination and bias conditions as (a) case A: positive drain bias with grounded source and gate, (b) case B: negative drain bias with grounded source and gate, (c) case C: positive source and drain biases with grounded gate, and (d) case D: negative source and drain biases with grounded gate.

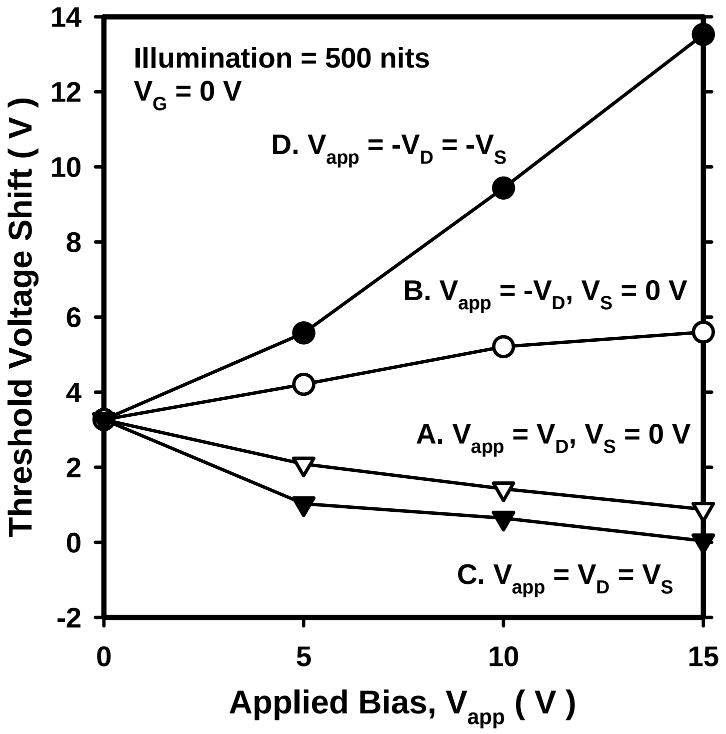


Fig. 3-36 The light-induced ΔV_{th} as a function of applied bias (V_{app}) after a 500-sec illumination. V_{app} can be only V_D or both V_D and V_S. Cases A, B, C and D correspond to the four band diagrams in Fig. 3-38.

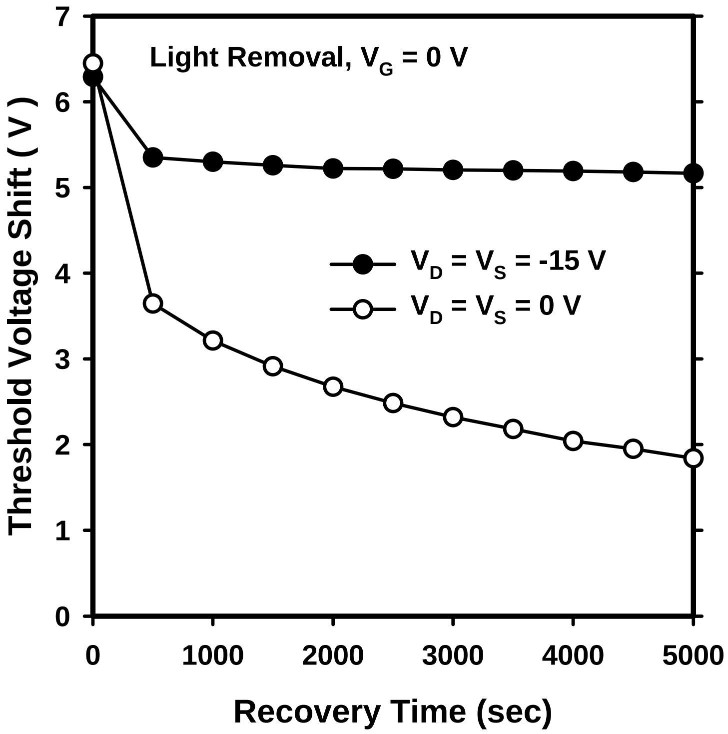


Fig. 3-37 After light removal, the light-induced ΔV_{th} as a function of recovery time under various drain and source biases ($V_D = V_S = 0$ V, or $V_D = V_S = -15$ V) with grounded gate.

Chapter 4

DIELECTRIC HYDROXYL GROUPS EFFECTS IN OTFT

4-1 Introduction

Organic thin film transistors (OTFTs) compared with the conventional amorphous silicon thin film transistors have many advantages, such as low-temperature process, low cost, flexible and light weight. However, poor reliability of OTFTs is a serious issue for waiting to solve [1]. Hole or electron trapping in the interface between active layer and gate dielectric are responsible for the pronounced threshold voltage shift (ΔV_{th}) of OTFTs. Compare with negative bias stress, a few studies discussed the electron trapping mechanism under positive bias stress in detail due to p-type channel. When trapping electron in active layer, the hysteresis are usually observed in the electric transfer characteristic of OTFTs [2]. If using OTFTs as photo-sensors, the device photoresponsivity dependent on the light-induced ΔV_{th} shifted forward positive due to electron trap states. Therefore, it is necessary further studying the electron trapping mechanism to control the device ΔV_{th}.

To date, electron trap origins of OTFTs are not clearly explained. Injected electrons and light-induced electrons are possible electron origins to induce electron trap states. In previous studies, it was found that the OH group density on dielectric surface also dominate the electron trapping [3]. Therefore, different surface states of dielectrics are prepared to stress in air and vacuum with and without illumination in this study. These results would reasonably explain electron origins and electron trap generation mechanism.

4-2 Device Fabrication Process

In this study, conventional top-contact pentacene-based TFTs with dual dielectric layers were used. 100-nm-thick thermal oxide was grown on heavily doped Si wafers to serve as the first layer of gate dielectric. The back of heavily doped Si wafer is served as the gate electrode. Poly(methyl methacrylate) (PMMA) and poly(4-vinyl phenol) (PVP) are separately used as second dielectric layers to provide different surface states.

Step1. Clean the oxide surface

Before fabricating device on wafer, the native oxide on the back of wafer must be etched by using BOE (NH_4F : HF = 10 : 1) solution. Then, the oxide surface of wafer was cleaned by 5 mins DI water, 5 mins acetone and 5 mins DI water, sequentially. Using hot plate bakes the wafer to remove the moisture on the oxide surface.

Step2. Organic dielectric layer fabrication

***PMMA fabrication condition*:** PMMA was obtained from MicroChem. Corp. with molecular weight of 95000 and was dissolved in anisole at 10 wt%. Fig. 4-1 is the molecular structure of PMMA. The spin speed was accelerated from 0 to 1000 rpm during the first 10 sec and further increased the spin speed from 1000 rpm to 6000 rpm in following 10 sec. After keeping 6000 rpm of the spin speed for 40 sec, the spin speed was decreased from 6000 rpm to 0 rpm in following 10 sec. Then, using hot plate baked the sample for 30 mins at 70°C.

***PVP fabrication condition*:** PVP was obtained from Aldrich with molecular weight about 20000. PVP have OH function groups on its molecule structure as shown in Fig. 4-2, poly (melamine-co-formaldehyde) MMF was used as cross-linker and dissolved in PGMEA (propylene glycol 1-monomethyl ether 2-acetate, $C_6H_{12}O_3$). Fig. 4-3 is schematic picture of MMF cross-link with PVP. Most of PVP spin conditions were similar to above PMMA fabrication process except the initial acceleration from 0 to 1000 rpm was finished in 5 seconds. Then, PVP was cross-linked by thermal curing through a hot plate in air. At temperatures of 100 °C for 10 min and 200 °C for 50 min to remove PGMEA in the PVP film [4-6]. The spin conditions of PMMA and PVP was organized in Table 4-1

Step3. Pentacene film deposition through shadow mask

Pentacene obtained from Aldrich (purity: 99.9%) without purification was evaporated through a shadow mask onto organic insulator to form the active layer. The deposition rate was set at 0.5 Å/s. The substrate temperature and the pressure were kept at room temperature and at around 3×10^{-6} Torr during deposition process.

Step4. Depositing Au to form source and drain contact

After depositing a 100-nm-thick pentacene, 100-nm-thick gold was deposited through the shadow mask to form source/drain contacts. The thickness of Au layer was 100 nm. The device channel length varied from 100 μm to 600 μm while channel width was fixed as 1000 μm. The structure scheme of pentacene-based TFTs with PMMA or PVP dielectric layers are shown in Fig. 4-4.

4-3 Illumination System Setup

There are four different light sources to illuminate the device in this experiment. The white light source comes from light-emitting diode (LED) backlight with a broad wavelength range. Blue, green and red light sources are light-emitting diodes with 467 nm, 536 and 631 nm wavelengths. These spectrums of four light sources are shown in Fig. 4-5. The light source was set up above the device to irradiate the sample from the top. The light power was controlled by the power supply (PPT3615). The light intensity was adjusted by changing the applied voltage.

4-4 Material Analysis of PVP and PMMA Thin Film

4-4-1 Wettability of PVP and PMMA Dielectrics

Using spin-coating process fabricates PMMA and PVP thin films on clean heavily doped Si wafer with 100-nm-thick silicon dioxide thin film. Water contact angles of PMMA and PVP dielectric surfaces are $61.7^{\mathbf{o}}$ and $51.8^{\mathbf{o}}$ as shown in Fig. 4-6. Previous researches mentioned that the water contact angle strongly dependents the chemical composition of dielectric surface [7]. The larger water contact angle indicates that PVP dielectric surface is more hydrophilic than PMMA dielectric surface because OH groups consist in PVP molecule structure.

4-4-2 Fourier Transform Infrared Spectroscope

Using Fourier Transform Infrared Spectroscope (FTIR) observes the surface characteristic of organic dielectrics. The FTIR absorption spectra of PVP and PMMA dielectric layers were shown in Fig. 4-7. For PVP absorption curve, there are two stretching bands at 3355 cm^{-1} and 3000 cm^{-1}, which were attributed to the OH groups and C–H groups, respectively [8-9]. However, there is no obvious stretching band at 3355 cm^{-1} in PMMA absorption curve. This result shows that there are obvious amount differences of OH groups on PVP and PMMA dielectric surfaces.

4-5 Hydroxyl Group Influence on the Transfer Characteristic of OPT

4-5-1 Electric Transfer Characteristics

Based on above results, pentacene thin films are deposited on organic dielectric with and without OH groups to form thin film transistors. The transfer characteristics of pentacene-based TFTs with PVP and PMMA dielectrics are shown in Fig. 4-8. Subthreshold swing and on/off ratio of PVP-OTFTs are similar to PMMA-OTFTs. The threshold voltage of PVP-OTFTs and PMMA-OTFTs are about -3 ~ -6 V and -14 V. The field effect mobility of PVP-OTFTs and PMMA-OTFTs are about 0.6

$cm^2/V*s$ and 0.36 $cm^2/V*s$. In our experiment, the field effect mobility of PVP-OTFT is larger than that of PMMA-OTFTs.

It had been reported that the device mobility is affected by the pentacene grain size [10-12]. Some groups proposed that the larger grain size helps to enlarge the device mobility. If pentacene grain size is small, there are many grain boundaries in the device channel which include many trap sites to block the free carrier transportation.

However, other groups found the opposite result [13] and proposed that the device mobility was mainly dominated by pentacene growth mode. If Stranski - Krastanov growth mode (two dimensional growth modes) is observed at the beginning of pentacene deposition, the molecules near substrate will strongly bind to substrate than bind with other molecules. This kind of growth mode will leave lots of voids in the first layer of pentacene and cause lower carrier mobility. In contrast, if Volmer-Weber growth mode (three dimensional growth modes) is observed, pentacene molecule will highly interconnect with one another and have fewer voids, the mobility then become higher.

Although many superior groups tried to clarify the relationship between pentacene grain size and field effect mobility, the grain size is still difficult to use to estimate the field effect mobility. Therefore, in following section, the morphology and phase composition of the pentacene films grown on PVP and PMMA gate dielectrics which greatly influence the device performance will be discussed in detail.

4-5-2 X-Ray Diffraction

Using x-ray diffraction (XRD) studies the structural order difference between pentacene films grown on PVP and PMMA dielectrics. XRD pattern of the pentacene film consist of the thin-film phase and the single-crystal (bulk) phase [14]. Thin-film phase is defined when reflection plane spaces (d_{00l}) are 15.66 Å, 7.78 Å, and 5.17 Å (l = 1, 2, and 3, respectively). It is usually found in vapor deposited thin film and is kinetically favored phase. On the other hand, single-crystal phase is observed when reflection plane space (d_{00l}) is 14.61 Å, 7.26 Å, and 4.82 Å (l = 1, 2, and 3, respectively), single-crystal phase is thermodynamically stable phase. Fig. 4-9 shows that XRD patterns of 100nm-thick pentacene films deposited on PVP and PMMA gate dielectrics. Both PVP and PMMA samples have series of (d_{00l}) reflections which shows the formation of "thin-film" phase. Next we can find both two samples have obvious peak fractions from (d_{001}) to (d_{003}) in the XRD pattern. These features suggest that molecules in the pentacene film are well-oriented perpendicular to the dielectric interface [18]. Finally, the XRD intensity of first peak for pentacene film on PMMA gate dielectric was almost two times larger than on PVP gate dielectric. This result indicates that pentacene thin film is more highly ordered grown on PMMA gate dielectric than on PVP gate dielectric.

4-5-3 Morphology of PMMA, PVP and Pentacene Films

Before and after depositing pentacene thin film on organic gate dielectric, using atomic force microscope (AFM) observes the morphology of PMMA, PVP and pentacene thin films. Surface roughness is one of factors which affect pentacene crystallization. Pentacene grow on smooth surface usually have better morphology and mobility than that grow on rough surface. Fig. 4-10 (a) and (b) are atomic microscopy images of PMMA and PVP dielectrics surfaces before depositing pentacene thin films. Fig. 4-11 (a) and (b) are atomic microscopy images of pentacene thin film surface on PMMA and PVP dielectrics. There are not obvious difference in pentacene grain size between deposited on PVP and PMMA dielectric. Based on these results of AFM and XRD, it is difficult to explain that PVP-OTFTs have higher field effect mobility. In previous study, Sangyun Lee et al. proposed that OH-terminated interface may increase the mobility by supplying the hopping sites, the carriers then can easily move through the channel [15]. In following experiments, the OH group influences on the electric characteristics of OTFTs are further studied and discussed.

4-5-4 Hysteresis of Electrical Transfer Characteristic

Hysteresis is widely observed in the transfer characteristic of pentacene-based TFTs and used to explain the dielectric interface states. Using the semiconductor parameter analyzer HP4156 measures the device transfer characteristic. Firstly, the devices are measured at room temperature in ambient air and under dark. The transfer characteristic curves are obtained by sweeping gate bias from positive to negative and back to positive. Because the transfer characteristic curve of PVP-OTFT obviously towards positive, sweep gate bias of PVP-OTFT is extended from 10 V to 15 V. The transfer characteristics of PVP-OTFT and PMMA-OTFT swept in both directions are shown in Fig. 4-12 and Fig. 4-13. There is no hysteresis observed in these two transfer characteristic curves measured in air and under dark. However, when light source is turned on, these two devices are measured again. The light intensity is 16.9 mW/cm^2. Fig. 4-14 and Fig. 4-15 show that the transfer characteristics of these two device. Compared with PMMA-OTFT, there is hysteresis observed in PVP-OTFT. In previous studies, defect states or dipoles on dielectric surface are used to explain the hysteresis generation mechanism. Defect states help trapping electron and electron trap usually have longer lifetime than hole trap. The dipolar groups on the organic dielectric can be reoriented under large electrical. OH groups are main origins to provide the trapping sites and dipoles. When fabricating device, incomplete cross-linking or incomplete baking cause residual hydroxyl OH groups. When exposing device to ambient air, thin film may be also adsorb water molecules.

However, when these two devices are measured under dark, hysteresis is not observed. Therefore, OH groups on the PVP dielectric surface are not affected and reoriented by gate electrical field. Gu *et al*. proposed that trapped electrons in the semiconductor have very long lifetimes. It was found that time constants of electron detrapping were the order of second or more. Therefore, trapped electrons can not be released in time and stored in the semiconductor to induce extra drain current. The illumination and the ambient air also dominated the hysteresis in transfer characteristic [16-18].

In our experiment, it was found that dielectric interface needed OH groups to cause hysteresis even if device was measured in ambient air under illumination compare with Fig. 4-14 and Fig.4-15.

4-5-5 Wavelength Absorption Spectrum of Pentacene Thin Film

The relationship between different light wavelengths and the device ΔV_{th} is discussed. According to the study proposed by Yong-Young Noh *et al* [19], the influence of wavelength on the irradiation effect of pentacene-based OTFTs had been discussed. A smaller light-induced ΔV_{th} is found when the incident light had larger wavelength due to the internal filter effect. When illuminating the pentacene-based TFTs, the device threshold voltage shifted toward positive because that the light-induced electrons close to the gate dielectric are trapped by the interface states. If the certain wavelength has high absorption in pentacene thin film, it is not able to arrive at the gate dielectric interface. In this experiment, red, green and blue light-emitting diodes (LEDs) are used as light sources to discuss the light wavelength influence on the device ΔV_{th}. During illumination, stressed gate bias V_{GS}^{st} 15 V is applied while drain and source are grounded. Light power of all light sources is 0.05 mW/cm^2. Fig. 4-16 shows that the light-induced ΔV_{th} increased with decreasing light wavelength and the ΔV_{th} of PVP-OTFT is larger than that of PMMA-OTFT. Based on the internal filter effect, the light-induced ΔV_{th} is dominated by light absorption spectrum. The light absorption spectrum of pentacene thin film deposited on PVP and PMMA dielectrics are shown in Fig. 4-17. Two light absorption curves are parallel. Obviously, OH groups on dielectric surface do not affect the light absorption of pentacene thin film. OH groups on dielectric surface only enhance the light-induced ΔV_{th}.

4-6 Bias Stress Effect on OPTs with and without Hydroxyl Groups

As above description, pentacene thin film deposited on organic dielectrics with and without OH groups have different interface states between gate dielectric and pentacene thin film [20-21]. In this section, the OH group influences on the reliability, the photoresponsivity and the defect generation mechanism are discussed. In previous researches, they proposed that increasing OH groups at the interface can enhance the device photoresponsivity. However, OH group consisted in the interface between dielectric and pentacene thin film is one of main degradation mechanisms. In the chapter 3, it demonstrates that adjusting the electrical field can control the photoresponsivity of pentacene-based TFTs. Therefore, combining bias stress and illumination is applied to devices with different interface states to discuss carrier generation and transport mechanisms and the defect generation mechanism.

4-6-1 Bias Stress in Air and under Dark

Firstly, OH group influence on the device reliability is discussed in ambient air and under dark. Because Au/pentacene contact barrier is prefer to hole transport, pentacene thin film is p-type channel. The positive gate bias is applied to stress the device at off-state region and the negative gate bias is applied to stress the device at on-state region. For positive gate-bias stress, gate stress bias V_{GS}^{st} was kept at 15 V and $V_D = V_S$ were 0 V for 1000 sec. The linear-region transfer characteristics of PVP-OTFT and PMMA-OTFT before and after a 1000-sec bias stress are depicted in Fig. 4-18. Then, threshold voltage shift (ΔV_{th}) curves of PVP-OTFT and PMMA-OTFT are plotted as a function of bias stress time as shown in Fig. 4-19. It is found that positive gate bias stress influences on PVP-OTFT and PMMA-OTFT are differing. The transfer characteristic of PMMA-OTFT is nearly unchanged after bias stress. Obviously, the bias stress only causes a parallel shift of the transfer characteristic of PVP-OTFT while the subthreshold swing keeps almost unchanged. The field-effect mobility μ_{FE} as a function of stress time is shown in Fig. 4-20. μ_{FE} is not affected by the bias stress while V_{th} is drastically changed. Under positive electric field, electron carriers should be accumulated in the channel and trapped in the interface between pentacene and dielectric. However, the V_{th} of PMMA-OTFT kept unchanged. The ΔV_{th} is only observed in PVP-OTFT. Therefore, it is supposed that OH groups can provide electron traps or electron carriers in the channel under bias stress.

For the negative gate bias stress, a 1000-sec gate bias stress is applied and V_{GS}^{st} is kept at -15+V_{th} V while $V_{\mathrm{D}} = V_{\mathrm{S}}$ are grounded. The transfer characteristics of both devices before and after a 1000-sec bias stress are depicted in Fig. 4-21. Then, the ΔV_{th} curves of both devices are plotted as a function of bias stress time as shown in Fig. 4-22. The negative bias stress causes obvious ΔV_{th} in both devices while their subthreshold swing kept almost unchanged. The field-effect mobility μ_{FE} as a function of stress time is shown in Fig. 4-23. Obviously, μ_{FE} is not affected by the bias stress. Compared with the positive gate bias stress, the negative gate bias stress causes the obvious ΔV_{th} in PMMA-OTFT but ΔV_{th} is still smaller than that of PVP-OTFT.

When applying negative gate bias, hole carrier are accumulated in the channel and trapped in the interface between pentacene and dielectric. Compared with positive gate bias stress effect, there is obvious ΔV_{th} observed in PMMA-OTFT and the ΔV_{th} difference between both devices is reduced. It is proposed that hole injection from Au contact dominates hole carriers accumulated in the channel. Therefore, OH group influence on the device ΔV_{th} may be lowered.

4-6-2 Bias Stress in Air and under Illumination

When devices are operated under illumination, many researches found that the device threshold voltage shifts forward the positive voltage. The light-induced ΔV_{th} is attributed to light-induced carriers accumulated in the channel and dependent on carrier concentration. In the chapter 3, the light-induced carrier concentration can be controlled by the drain bias while illuminating the devices.

In this experiment, the light power is setup at 2.95 mW/cm^2 and a 1000-sec gate bias stress is applied. Transfer characteristics of PMMA-OTFT and PVP-OTFT are measured in ambient air. Firstly, the prolonged illumination influence on the threshold voltage of pentacene-based TFT with and without OH groups is studied. After applying a 1000-sec illumination to both devices, the ΔV_{th} of PVP-OTFT shifts forward positive and is larger than that of PMMA-OTFT as shown in Fig. 4-24. Although the prolonged illumination causes slightly ΔV_{th} in both devices, it is found that OH groups on dielectric surface can enhance the light-induced ΔV_{th}.

In following experiments, PMMA-OTFT and PVP-OTFT are stressed under illumination. The V_{GS}^{st} is setup at 15 V and $V_D = V_S$ are grounded and devices are measured in ambient air. The linear-region transfer characteristics of devices before and after a 1000-sec bias stress are depicted in Fig. 4-25. Then, the ΔV_{th} curves of both devices with and without illumination are plotted as a function of bias stress time as shown in Fig. 4-26. Compared with results of section 4-6-1, the ΔV_{th} of PMMA-OTFT is significantly enhanced by illumination. However, when applying positive gate bias stress under illumination, the ΔV_{th} of PVP-OTFT is slightly enhanced due to reaching the saturation in the shorter stress time. Recently, many reports found that light-induced ΔV_{th} can be significantly enlarged by applying an electric field during light irradiation (named as the photoelectric field effect in this study). The gate electric field effectively enhances dissociating light-induced excitons into hole-electron pairs and a large numbers of light-induced electrons are accumulated in the channel. However, the maximum of light-induced ΔV_{th} is limited by the applied gate bias. A band diagram from gate to drain is depicted to explain the proposed mechanism as shown in Fig. 4-27. When a positive gate bias is applied, the lowered Fermi energy (E_F) in the gate electrode leads to a downward band bending of pentacene near the gate dielectric. The number of electron trapping states below the Fermi energy is increased. This allows more photogenerated electrons to be trapped. More trapped electrons caused larger light-induced ΔV_{th}. When the trapping states are fully occupied, the light-induced ΔV_{th} reaches the saturation and is independent on the stress time. The additional photogenerated electrons recombine with photogenerated hole.

For PMMA-OTFT, it is interesting that there is obvious difference in the threshold voltage shift when applying positive gate bias under dark and illumination. This result is reasonable and can be explained by the carrier transport mechanism of pentacene-based TFT. Because the Fermi level of Au contact is near the LOMO of pentacene, electrons are difficult to inject into the pentacene film from Au contact. After applying positive gate bias stress under dark, the unchanged threshold voltage verifies that the injection electron can be ignored. Therefore, the original of free electron carrier in the channel of PMMA-OTFT only depends on the light-induced electrons. When illuminating device during positive gate bias stress, light-induced excitons provide free electrons accumulated in the channel to cause the ΔV_{th}.

For PVP-OTFT, there are many OH groups on dielectric surface. Therefore, two plausible mechanisms were proposed. 1. Thermal generation: OH groups between dielectric and pentacene film form a lot of carrier generation center to generate hole-electron pairs. 2. Reacted with moisture: OH groups between dielectric and pentacene film capture moisture to generate negative defects [22-26].

When extending gate bias stress time, the ΔV_{th} of PVP-OTFT under illumination reached a larger saturation value than under dark, as shown in Fig. 4-28. The increment between ΔV_{th} curves stressed by gate bias with and without illumination is difficult to explain by the thermal generation mechanism. In previous discussion on energy band of pentacene film, the saturation value of device ΔV_{th} should be limited by the gate bias. Therefore, it represents that OH groups at dielectric surface and moisture in air contribute a lot defects to cause the device ΔV_{th}. In following experiment, devices were measured in vacuum to compare with that in air and discussed moisture influence on the defect generation mechanism.

4-6-3 Bias Stress in Vacuum

This measurement system includes semiconductor parameter analyzer Keithley 4200 and vacuum chamber. The chamber pump can lower the pressure in chamber from 760 Torr to 0.5 Torr. Devices are measured in the chamber under dark. Then, threshold voltage shift (ΔV_{th}) curves of PMMA-OTFT and PVP-OTFT are plotted as a function of bias stress time as shown in Fig. 4-29. As expected, the threshold voltage of device with PMMA dielectric is near unchanged. Obviously, the ΔV_{th} of device with PVP dielectric is significantly suppressed while stressing the device at vacuum.

Therefore, when stressing devices in air, the combination of moisture in ambient air and OH groups on the dielectric surface contributes electron traps.

The previous study proposed that SiOH at the dielectric interface react with H_2O and O_2 in ambient air to cause the device ΔV_{th} forward positive bias [27]. The chemical reaction equation is shown in below.

$$SiOH + H_2O \Leftrightarrow SiO^- + H_3O^+$$

$$SiOH + e^- + \frac{1}{4}O_2 \rightarrow SiO^- + \frac{1}{2}H_2O$$

In previous discussion, the maximum of light-induced ΔV_{th} dominated by the gate bias is discussed. Although the saturated light-induced ΔV_{th} of PVP-OTFT and PMMA-OTFT are different, the OH group influence is believed to be responsible for the difference between two ΔV_{th} curves. If the proposed mechanism is correct, both ΔV_{th} curves should reach the same saturation when excluding the OH group influence. After applying a 1000-sec positive gate bias stress in vacuum and under illumination, it is found that the ΔV_{th} curves of both devices are similar as shown in Fig. 30.

Therefore, this result also demonstrates that when applying positive gate bias to PVP-OTFT in ambient air and under illumination, different originals of electron traps are simultaneously contributed from illumination and moisture in air.

4.8 Conclusion

In this chapter, using PVP and PMMA organic thin film as gate dielectric fabricates pentacene-based OTFTs with different interface states between dielectric and pentacene. Incomplete cross-linking causes OH groups consisted on the PVP dielectric surface. Measuring the contact angle and FTIR spectrum of PVP dielectric demonstrates that OH groups actually consist on the PVP dielectric surface. Because molecular structure of PMMA does not contain the hydroxyl groups, there are no OH groups consisted on the PVP dielectric surface. Using these two different surface states of dielectrics discusses OH group influence on the transfer characteristics and stability of pentacene-based TFTs.

Compared with PMMA-OTFT, the transfer characteristic of PVP-OTFT has higher field-effect mobility. However, based on the XRD and AFM results of pentacene deposited on two dielectrics, it is difficult to explain that the field-effect mobility of PVP-OTFT is higher than that PMMA-OTFT. A plausible mechanism is that the OH-terminated interface supplies hopping sites to enhance free carrier transport in the channel. On the other hand, OH groups cause hysteresis in the transfer characteristic of PVP-OTFT when exposed to the light.

In the reliability studies, the OH group influence and originals of electron traps are discussed in detail. OH groups in the interface between pentacene and dielectric can react with moisture to form defect traps under bias stress when exposing devices to ambient air. When applying positive gate bias to device in vacuum, the light-induced ΔV_{th} is not affected by OH groups. These results demonstrate that light-induced electron and OH groups reacted with moisture are main originals of electron traps and injection electrons can be ignored.

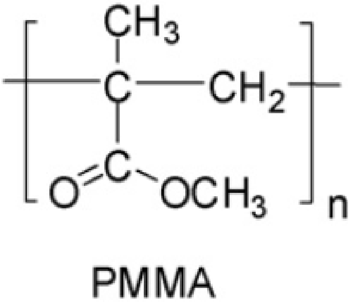


Fig. 4-1 Molecular structure of PMMA

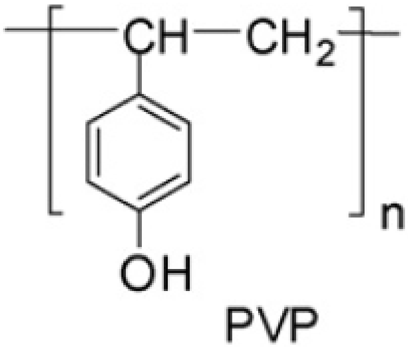


Fig. 4-2 Molecular structure of PVP

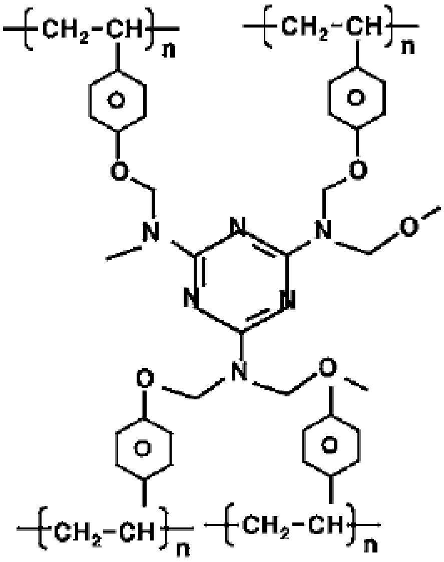


Fig. 4-3 Schematic structure of MMF cross-link with PVP

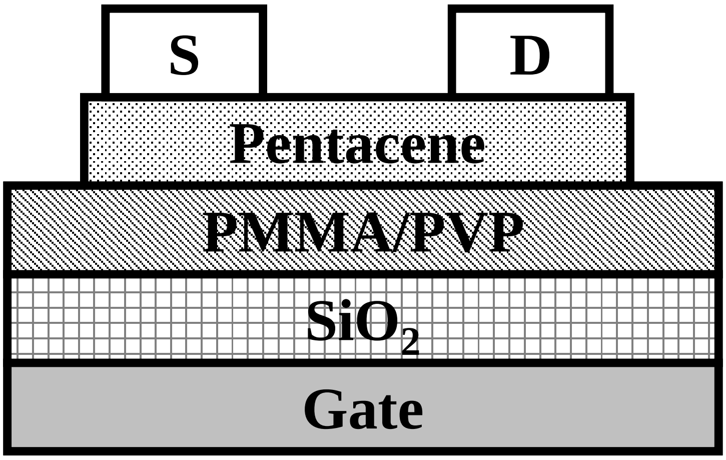


Fig. 4-4 Schematic structure of PVP-OTFTs and PMMA-OTFTs

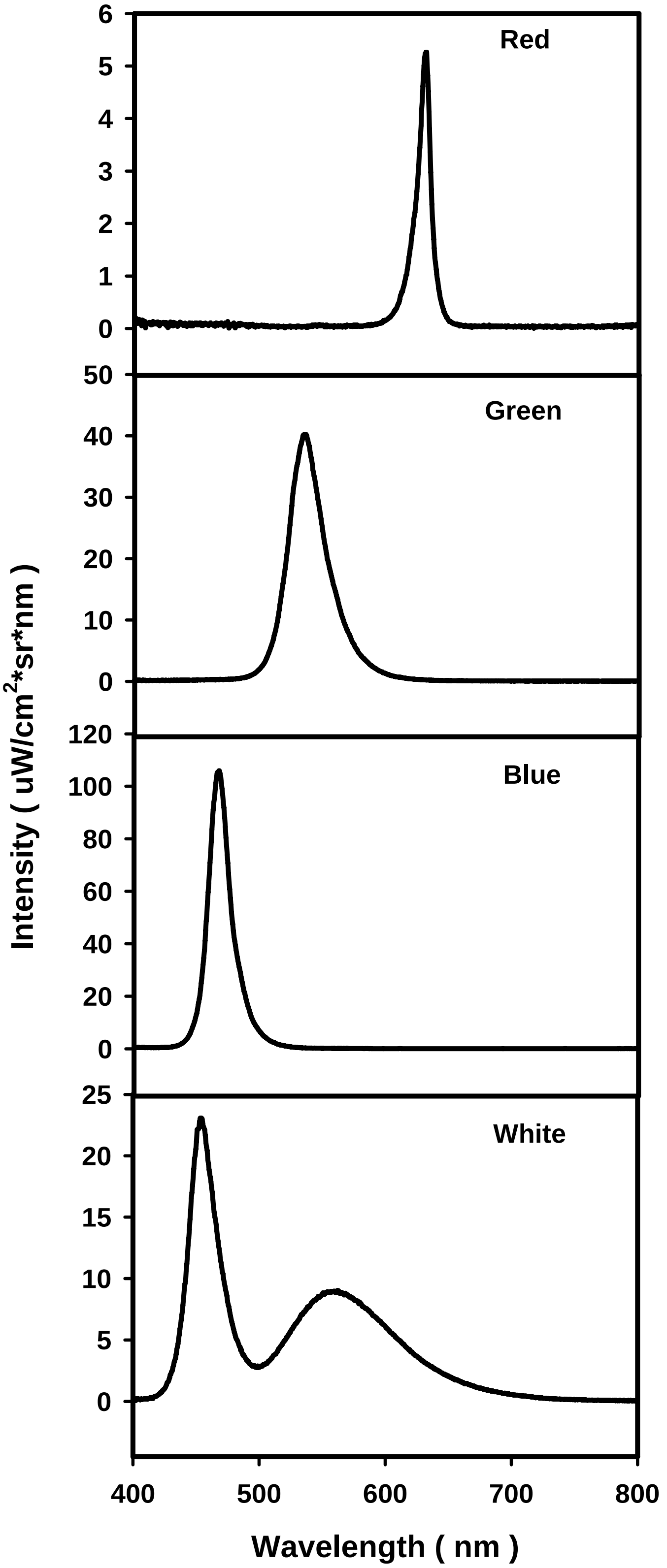


Fig. 4-5 Wavelength spectrum of light sources (Red, Green, Blue and White).

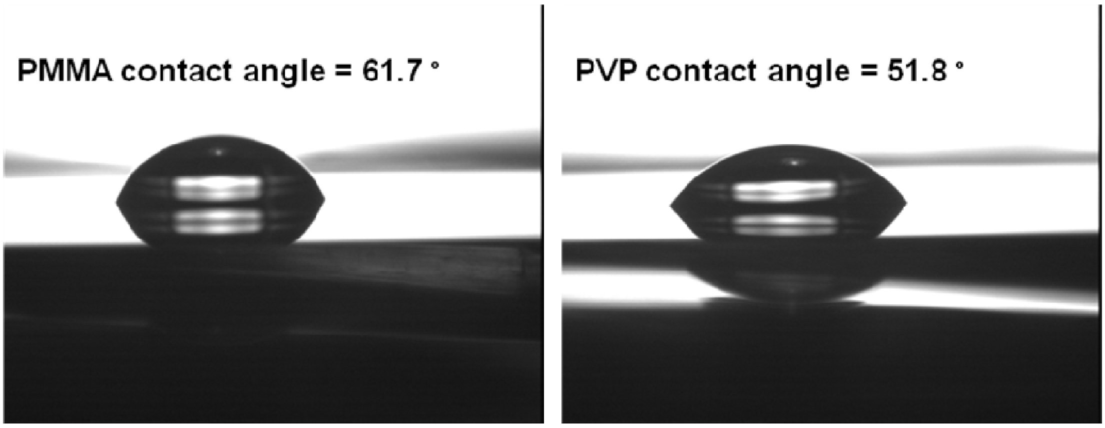


Fig. 4-6 Water contact angle of PVP and PMMA dielectric surfaces.

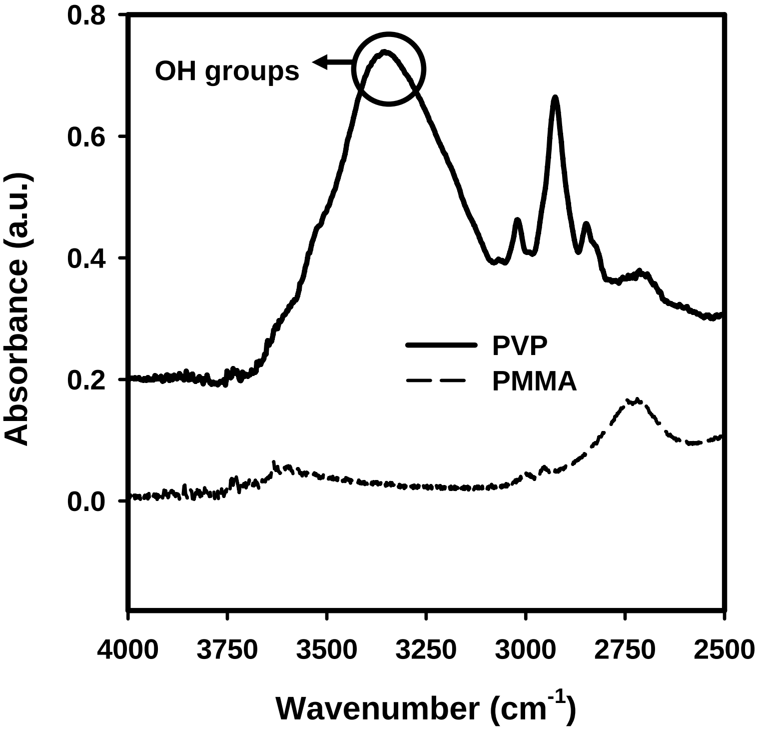


Fig. 4-7 FTIR spectra of PVP and PMMA film.

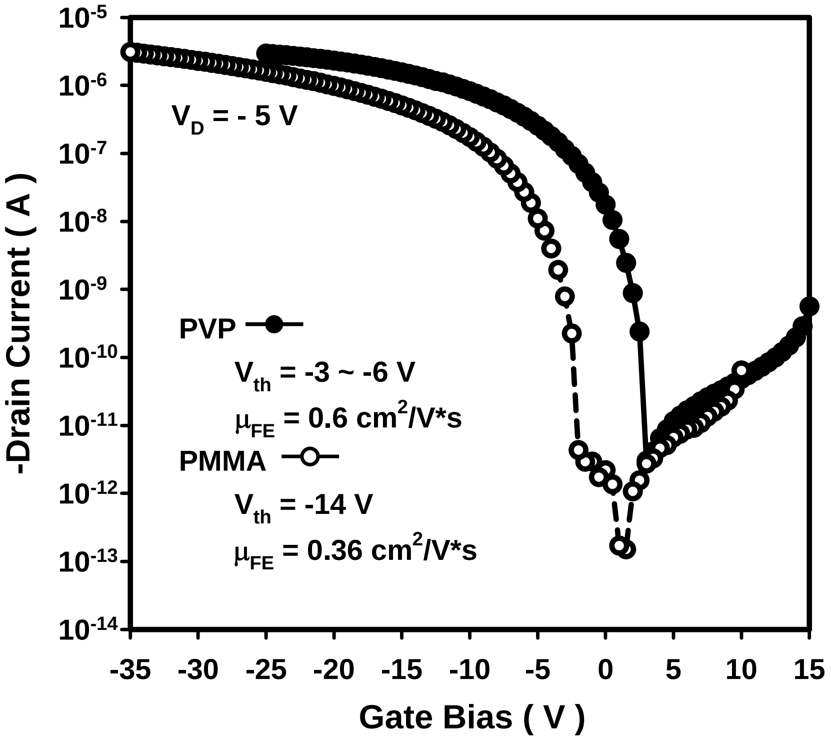


Fig. 4-8 The linear-region initial transfer characteristic of PVP-OTFT and PMMA-OTFT. The gate bias is swept from positive bias to negative bias. The threshold voltage (V_{th}) is extracted by using the linear region equation.

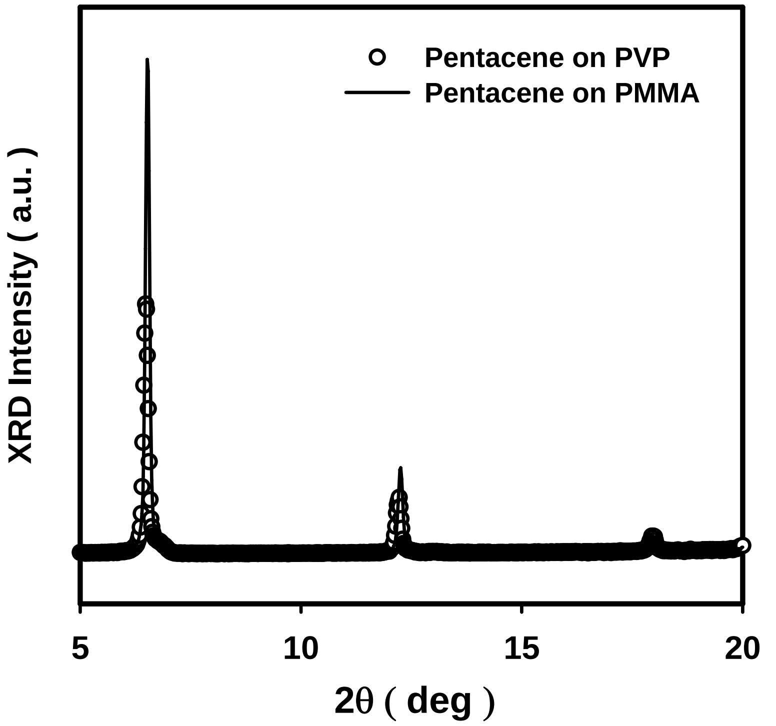


Fig. 4-9 X-ray diffraction (XRD) pattern of pentacene deposited on PVP and PMMA dielectrics. The thickness of pentacene films deposited on PVP and PMMA dielectric are 100nm.

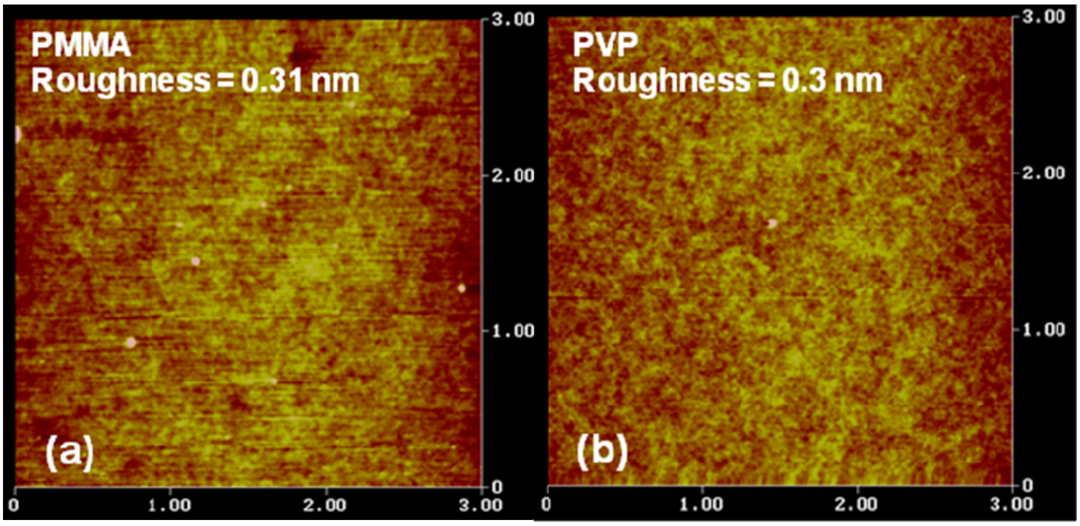


Fig. 4-10 Atomic force microscope (AFM) image of (a) PMMA and (b) PVP dielectric surfaces before depositing pentacene.

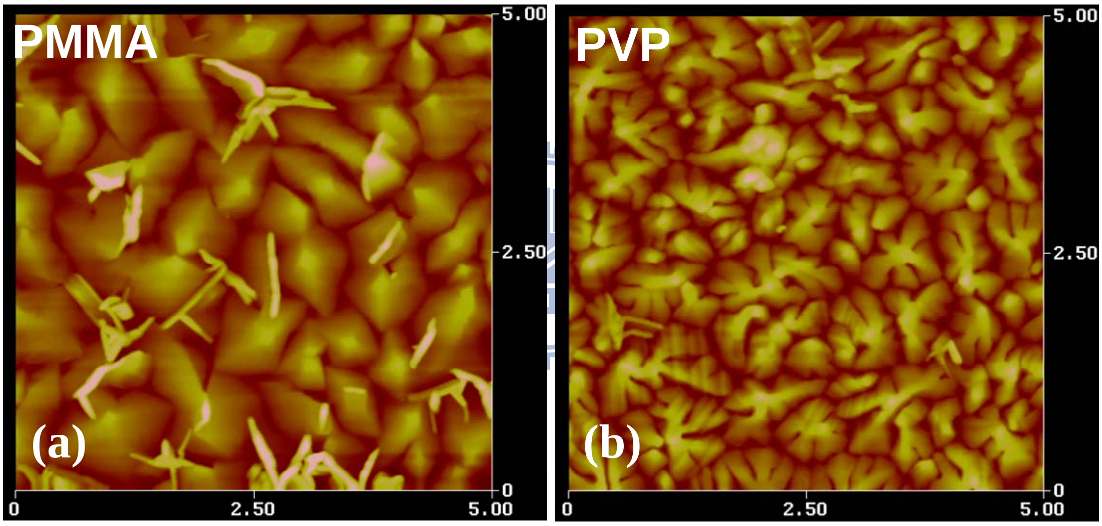


Fig. 4-11 Atomic force microscope (AFM) image of pentacene thin film surfaces deposited on (a) PMMA and (b) PVP dielectrics.

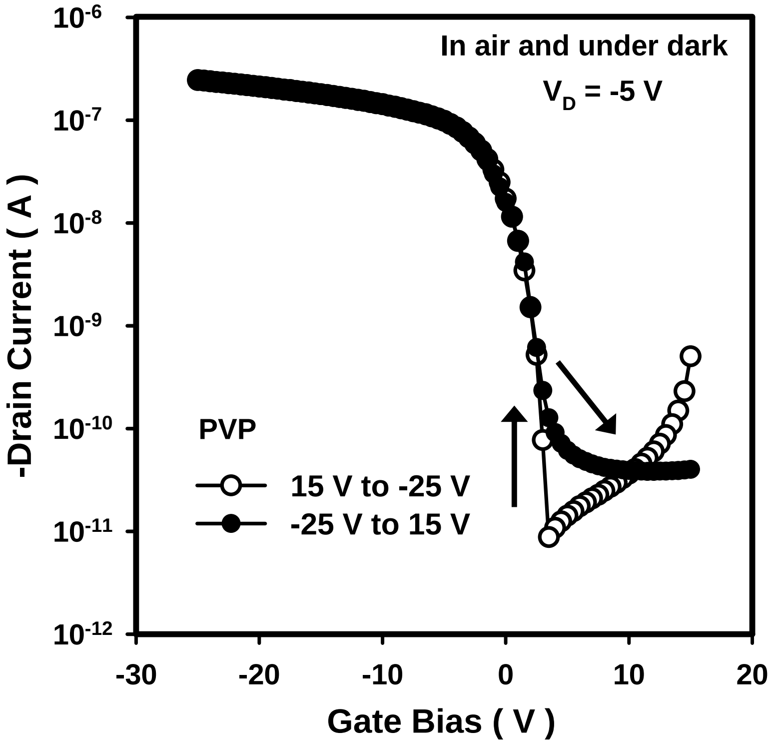


Fig. 4-12 The linear-region transfer characteristic of PVP-OTFT swept form 15 V to -25 V and back to 15 V in ambient air and under dark while drain bias is kept at -5 V.

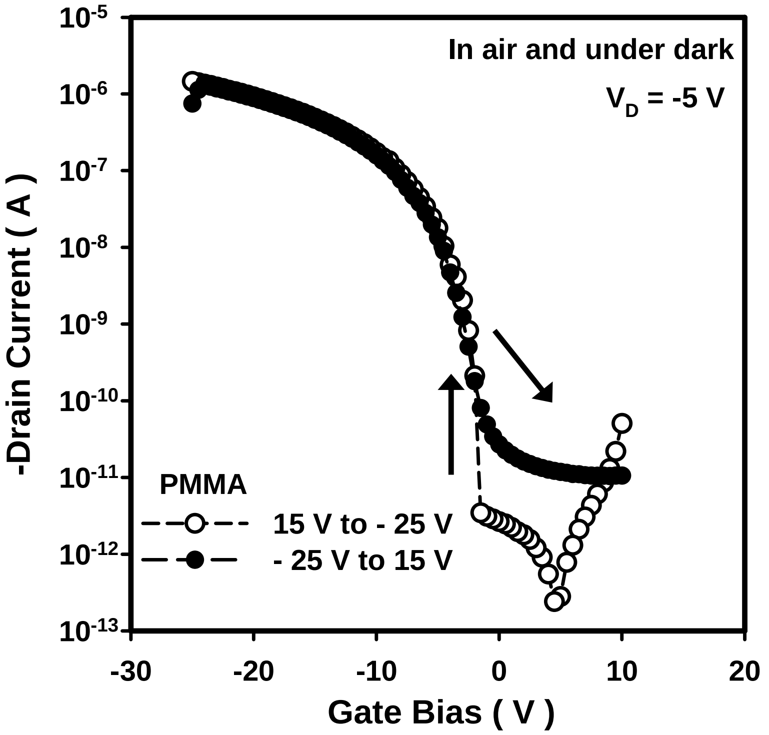


Fig. 4-13 The linear-region transfer characteristic of PMMA-OTFT swept form 10 V to -25 V and back to 10 V in ambient air and under dark while drain bias is kept at -5 V.

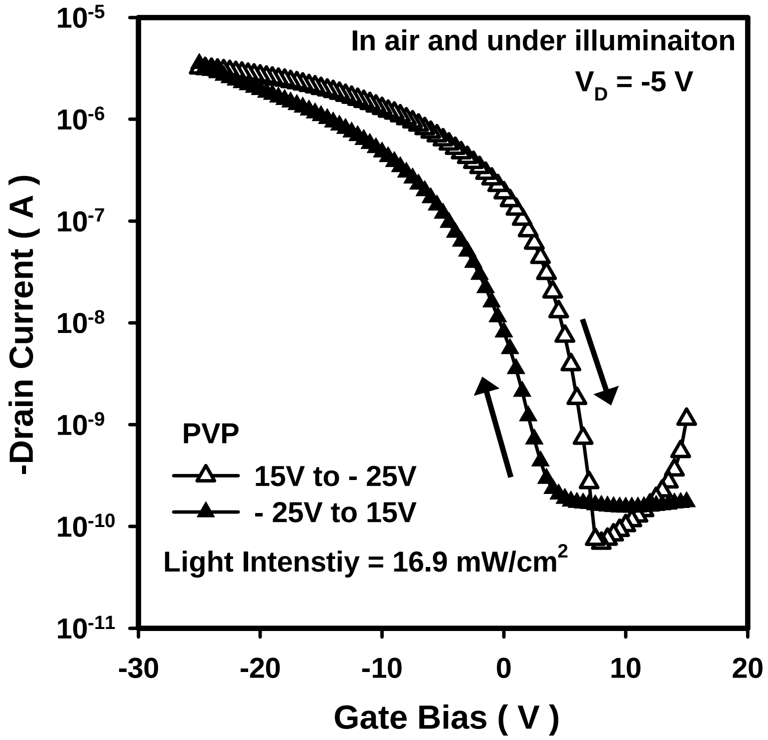


Fig. 4-14 The linear-region transfer characteristic of PVP-OTFT swept form 15 V to -25 V and back to 15 V in ambient air and under illumination while drain bias and light intenstiy are kept at -5 V and 16.9 mW/cm^2.

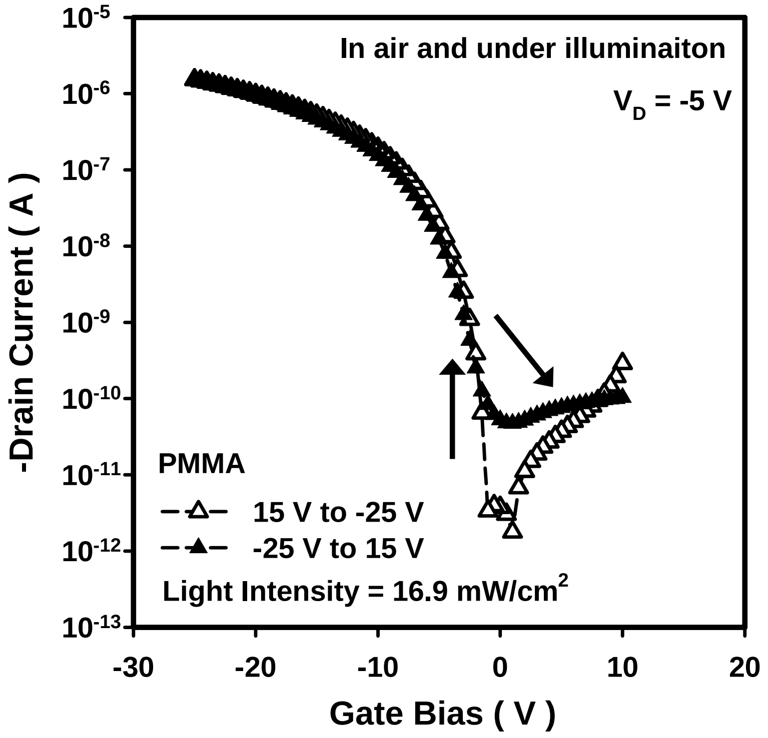


Fig. 4-15 The linear-region transfer characteristic of PMMA-OTFT swept form 10 V to -25 V and back to 10 V in ambient air and under illumination while drain bias and light intenstiy are kept at -5 V and 16.9 mW/cm^2.

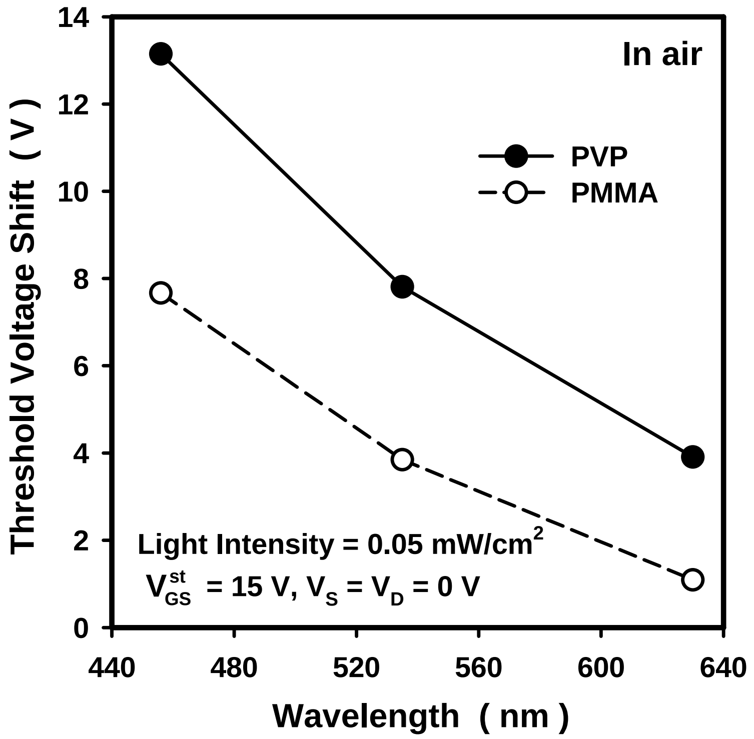


Fig. 4-16 Threshold voltage shift (ΔV_{th}) of PMMA-OTFT and PVP-OTFT after bias stress under illumination with different wavelength. The bias stress conditions: $V_G - V_{th}^{ini} = 15$ V, $V_D = V_S = 0$ V and light intensity is 0.05 mW/cm^2.

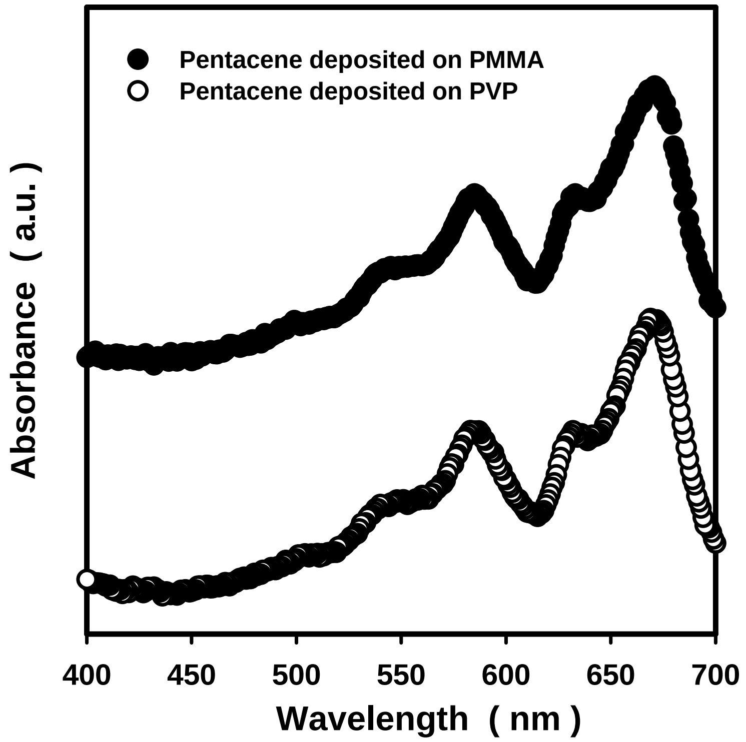


Fig. 4-17 The absorption spectra of pentacene thin films deposited on PVP and PMMA dielectric. The thicknesses of both pentacene thin films are 100 nm.

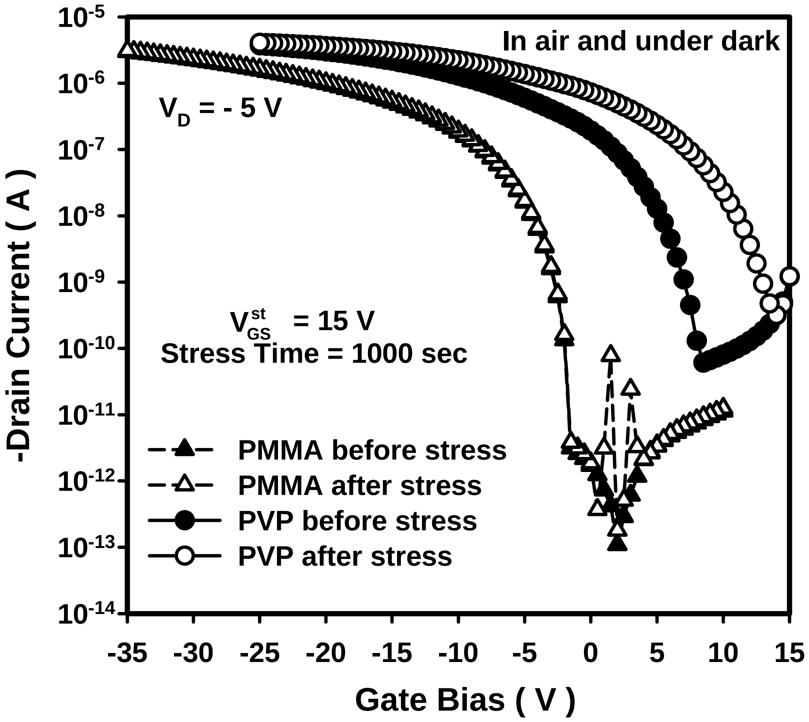


Fig. 4-18 The transfer characteristics of PVP-OTFT and PMMA-OTFT before and after a 1000-second positive gate bias stress in ambient air and under dark. The bias stress conditions: $V_G - V_{th}^{ini} = 15$ V, $V_D = V_S = 0$ V.

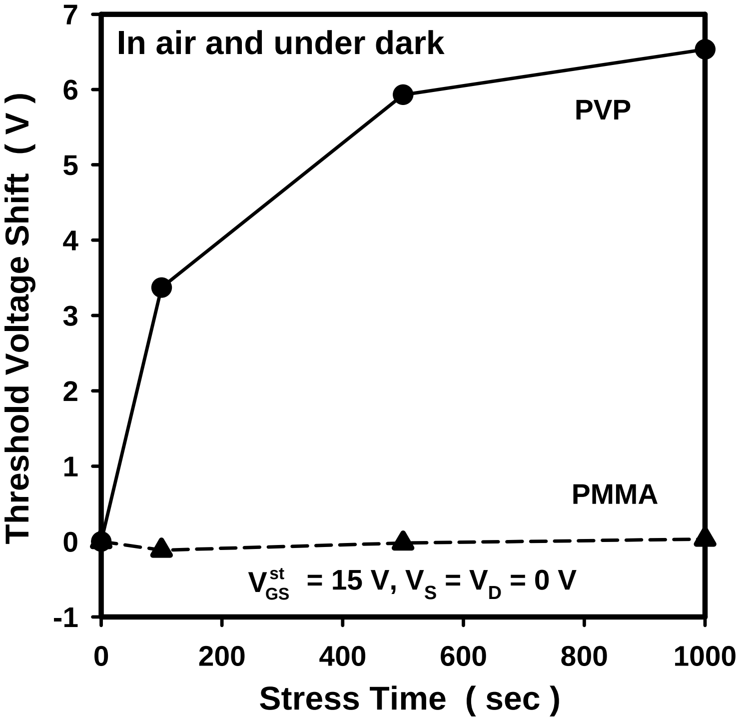


Fig. 4-19 Threshold voltage shift (ΔV_{th}) of PVP-OTFT and PMMA-OTFT during positive gate bias stress in ambient air and under dark. The bias stress conditions: $V_G - V_{th}^{ini} = 15$ V, $V_D = V_S = 0$ V.

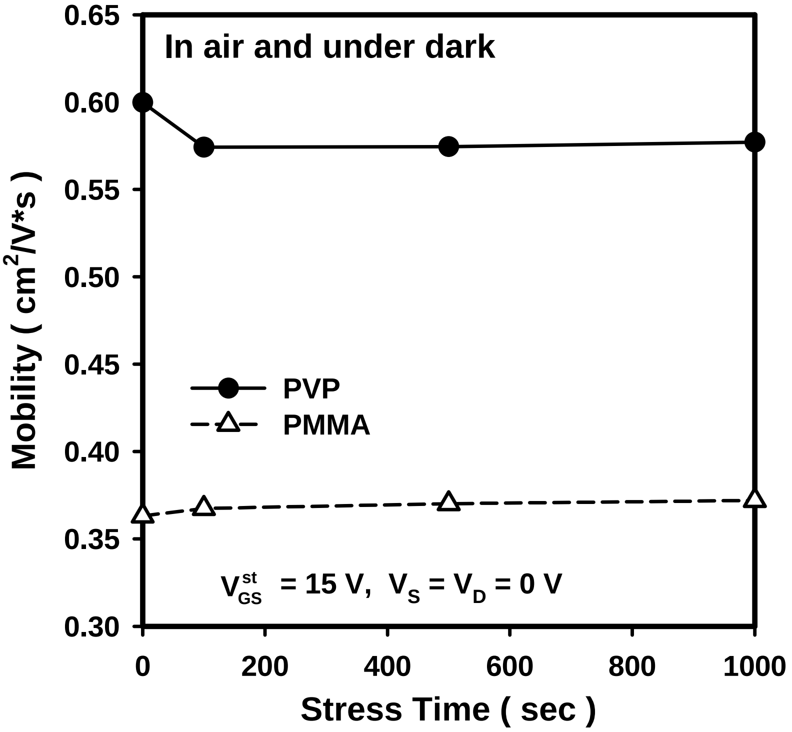


Fig. 4-20 The field-effect mobility of both devices plotted as a function of positive bias stress time in ambient air and under dark. The bias stress condition: $V_G - V_{th}^{ini}$ = 15 V, $V_D = V_S$ = 0 V.

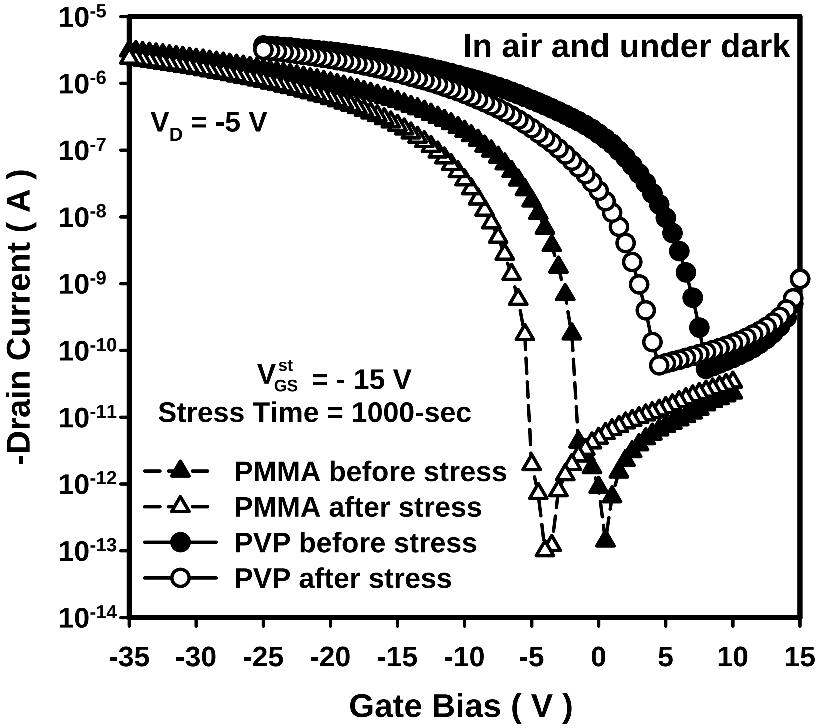


Fig. 4-21 The transfer characteristics of PVP-OTFT and PMMA-OTFT before and after a 1000-second negative bias stress in ambient air and under dark. The bias stress condition: $V_G - V_{th}^{ini}$ = -15 V, $V_D = V_S$ = 0 V.

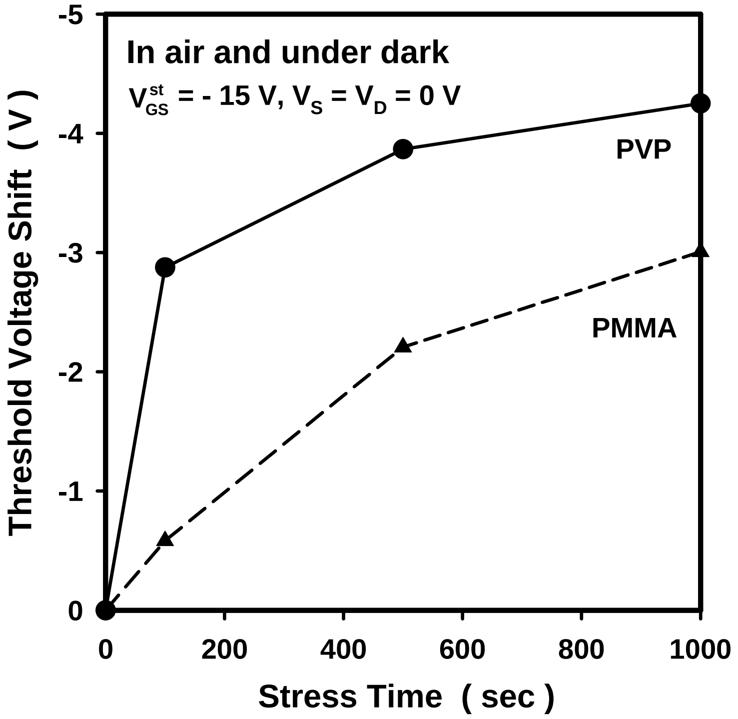


Fig. 4-22 Threshold voltage shifts (ΔV_{th}) of PVP-OTFT and PMMA-OTFT during positive gate bias stress in ambient air and under dark. The bias stress conditions: $V_G - V_{th}^{ini}$ = -15 V, $V_D = V_S$ = 0 V.

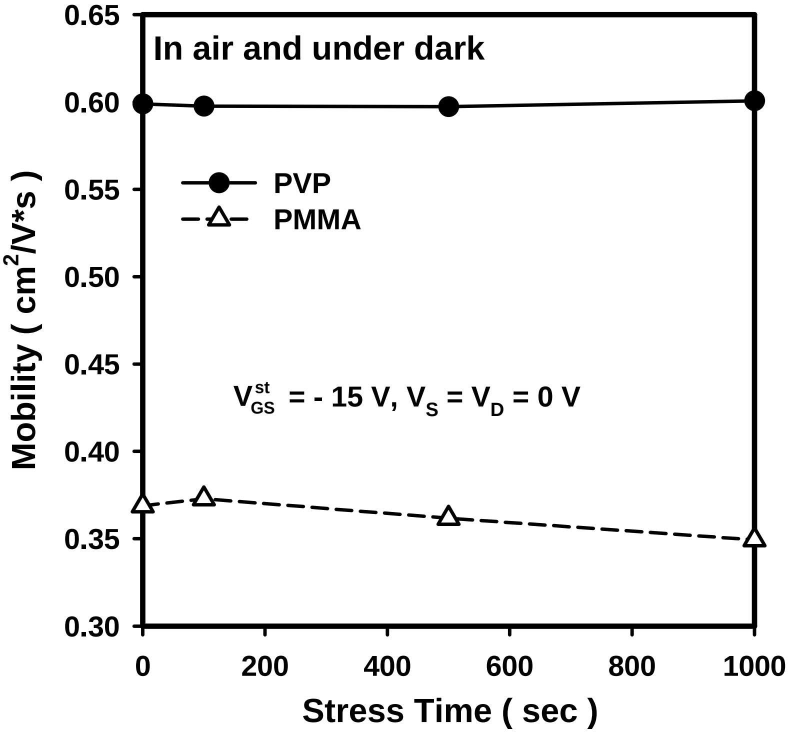


Fig. 4-23 The field-effect mobility of both devices plotted as a function of positive bias stress time in ambient air and under dark. The bias stress condition: $V_G - V_{th}^{ini}$ = -15 V, $V_D = V_S$ = 0 V.

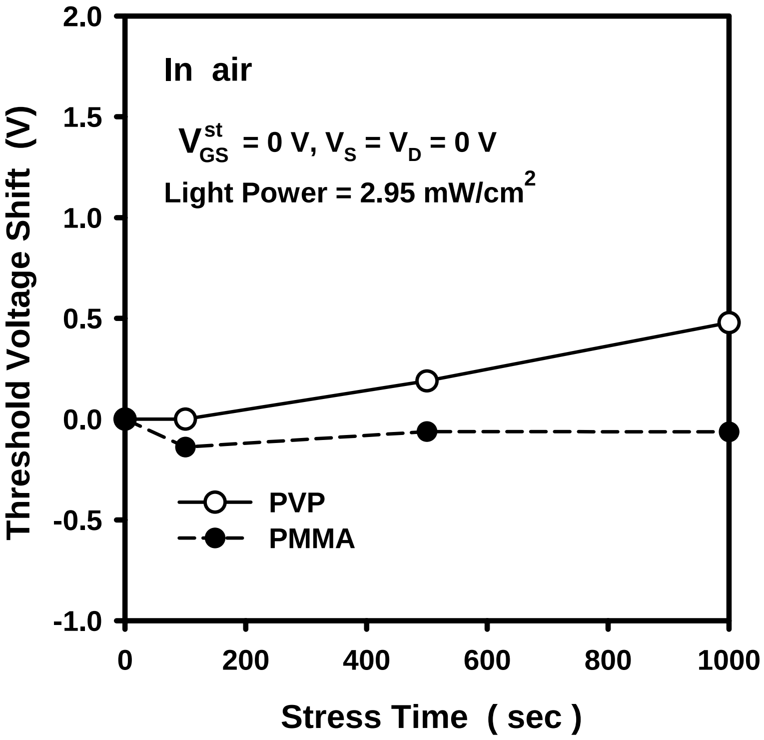


Fig. 4-24 Threshold voltage shift (ΔV_{th}) of PVP-OTFT and PMMA-OTFT during illumination. The light intensity is 2.95 mW/cm^2.

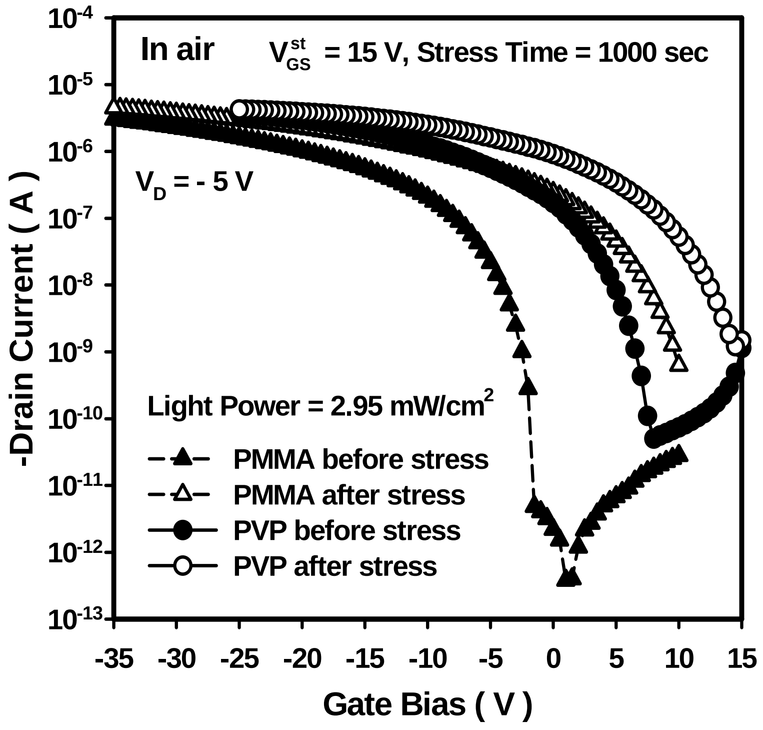


Fig. 4-25 The transfer characteristics of PVP-OTFT and PMMA-OTFT before and after a 1000-second positive bias stress under illumination. The bias stress conditions: $V_G - V_{th}^{ini}$ = 15 V, $V_D = V_S$ = 0 V. The light intensity is 2.95 mW/cm^2.

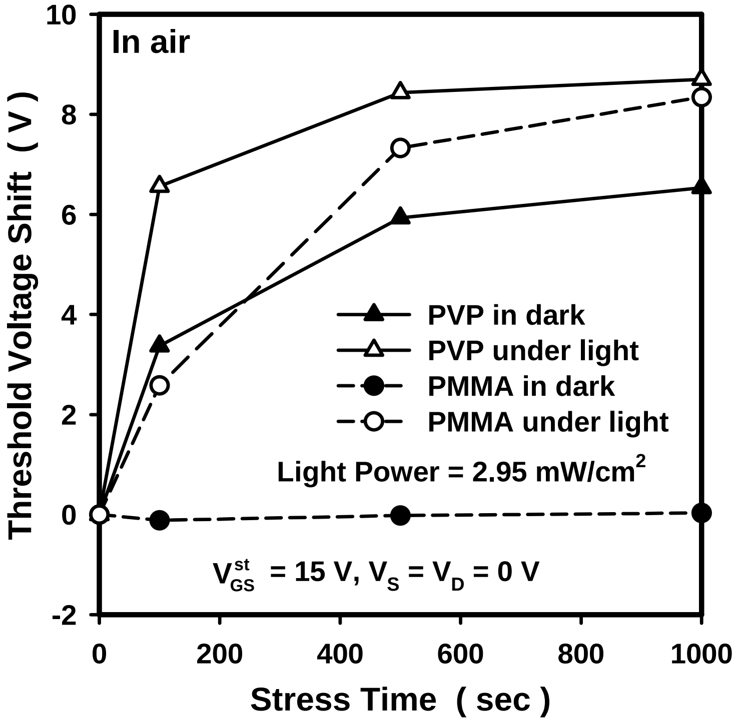


Fig. 4-26 Threshold voltage shift (ΔV_{th}) of PVP-OTFT and PMMA-OTFT during positive gate bias stress under dark and illumination. The bias stress condition: $V_G - V_{th}^{ini}$ = 15 V, V_D = V_S = 0 V. The light intensity is 2.95mW/cm^2.

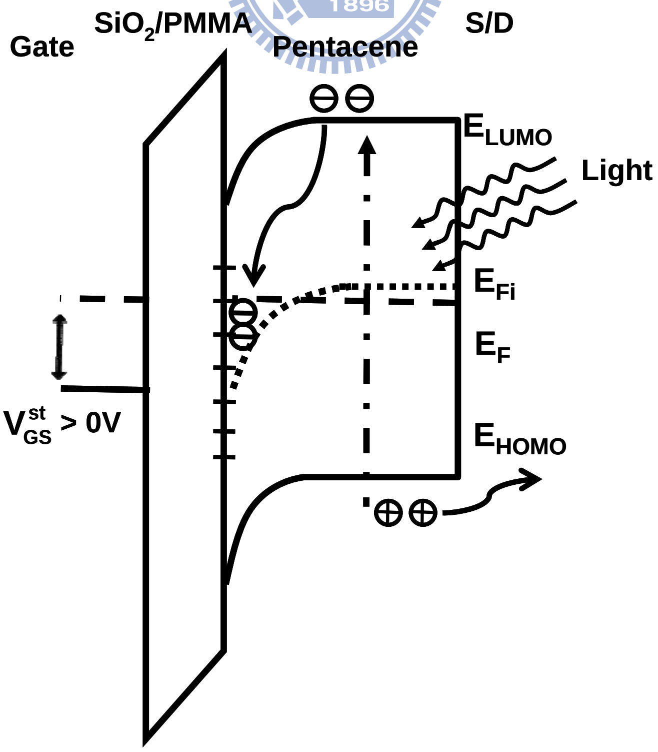


Fig. 4-27 Energy-band diagram of OTFT from gate to drain/source when devices are under illumination with positive gate bias.

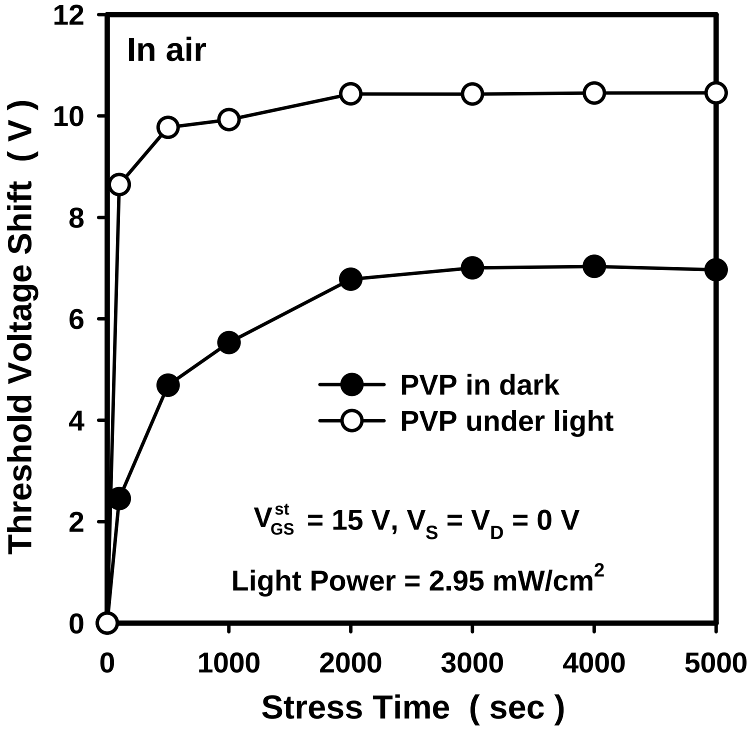


Fig. 4-28 Threshold voltage shift (ΔV_{th}) of PVP-OTFT during positive gate bias stress under dark and illumination when extending stress time. The bias stress conditions: $V_G - V_{th}^{ini}$ = 15 V, V_D = V_S = 0 V. The light intensity is 2.95 mW/cm^2.

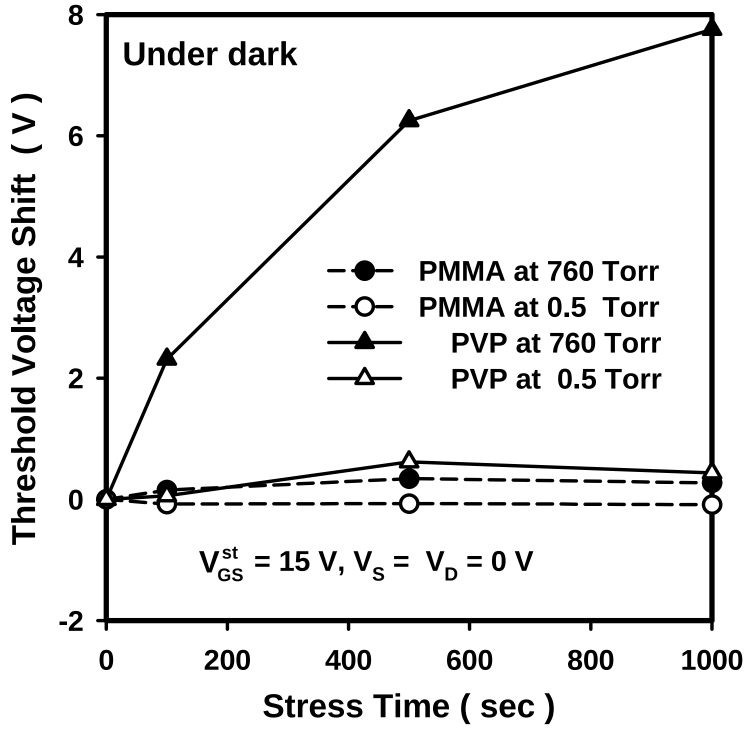


Fig. 4-29 Threshold voltage shifts (ΔV_{th}) of PMMA-OTFT and PVP-OTFT under dark and in air and in vacuum. The bias stress conditions: $V_G - V_{th}^{ini}$ = 15 V, V_D = V_S = 0 V.

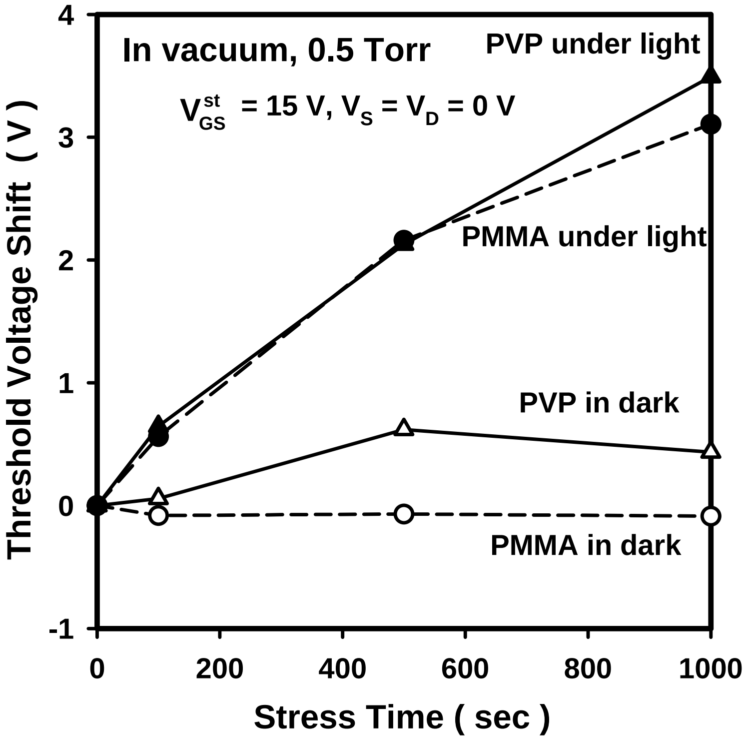


Fig. 4-30 Threshold voltage shifts (ΔV_{th}) of PMMA-OTFT and PVP-OTFT in vacuum under dark and illumination. The bias stress conditions: $V_G - V_{th}^{ini} = 15$ V, $V_D = V_S = 0$ V.

PMMA	Time (second)	Spin speed (rpm)
	0 ~ 10	0
	10 ~ 20	0 ~ 1000
	20 ~ 30	1000 ~ 6000
	30 ~ 70	6000
	70 ~ 80	6000 ~ 0
PVP	**Time (second)**	**Spin speed (rpm)**
	0 ~ 10	0
	10 ~ 15	0 ~ 1000
	15 ~ 25	1000 ~ 6000
	25 ~ 65	6000
	65 ~ 75	6000 ~ 0

Table 4-1 Spin coating parameters of PMMA and PVP dielectric fabrication process.

Chapter 5

ELECTRICAL FIELD ENHANCED OPTs

5-1 Introduction

Organic thin-film transistors (OTFTs) have attracted much attention because of their low-temperature processing, flexibility, and light weight [1, 2]. Besides serving as a switch in display, an OTFT exhibits high photoresponsivity (R_{ph}) and can be used as an organic phototransistor (OPT) [3, 4, 5]. Under illumination, excitons generated in pentacene film dissociate into electrons and holes. Holes can be well conducted without being significantly trapped. Light-induced electrons, on the contrary, are easily trapped by deep electron trapping states in a pentacene film [6]. When electrons are trapped close to organic/dielectric interface, OPT exhibits pronounced light-induced threshold voltage shift (ΔV_{th}) [3, 7]. The light-induced ΔV_{th} increases the photocurrent at a fixed gate bias and thus enhances R_{ph}. Recently, many reports found that R_{ph} or the light-induced ΔV_{th} of OPT can be significantly enlarged by applying an electric field during light irradiation (named as the photoelectric field effect in this study) [4, 7]. However, the influences of electric field and channel length on electron trapping have not been studied under illumination. When OPT is used to detect light signals with various intensities, the dynamic detecting range is also not investigated. In this paper, pentacene-based OPTs with different channel lengths are used to detect light signals with various intensities. Electric field effect, channel length effect, and dynamic detecting range under repeated operation are discussed.

5-2 Device Fabrication Process

In this experiment, conventional top-contact pentacene-based TFTs with dual dielectric layers were used. 100-nm-thick thermal oxide was grown on heavily doped Si wafers to serve as the first layer of gate dielectric. The back of heavily doped Si wafer is served as the gate electrode. Poly (methyl methacrylate) (PMMA) and PVP (poly-4-vinyl phenol) were separately used as second dielectric layers to provide different surface states.

Step1. Clean the oxide surface

Before fabricating device on wafer, the native oxide on the back of wafer must be etched by using BOE (NH_4F : HF = 10 : 1) solution. Then, the oxide surface of wafer was cleaned by 5 mins DI water, 5 mins acetone and 5 mins DI water, sequentially. Using hot plate bakes the wafer to remove the moisture on the oxide surface.

Step2. Organic dielectric layer fabrication

PMMA fabrication condition: PMMA was obtained from MicroChem. Corp. with molecular weight of 95000 and was dissolved in anisole at 10 wt%. Fig. 2.1 is the molecular structure of PMMA. The spin speed was accelerated from 0 to 1000 rpm during the first 10 sec and further increased the spin speed from 1000 rpm to 6000 rpm in following 10 sec. After keeping 6000 rpm of the spin speed for 40 sec, the spin speed was decreased from 6000 rpm to 0 rpm in following 10 sec. Then, using hot plate baked the sample for 30 mins at 70 °C.

Step3. Pentacene film deposition through shadow mask

Pentacene obtained from Aldrich (purity: 99.9%) without purification was evaporated through a shadow mask onto organic insulator to form the active layer. The deposition rate was set at 0.5 Å/s. The substrate temperature and the pressure were kept at room temperature and at around 3×10^{-6} Torr during deposition process.

Step4. Depositing Au to form source and drain contact

After depositing a 100-nm-thick pentacene, 100-nm-thick gold was deposited through the shadow mask to form source/drain contacts. The thickness of Au layer was 100 nm. The device channel length varied from 100 μm to 600 μm while channel width was fixed as 1000 μm.

5-3 Illumination System Setup

There are four different light sources to illuminate the device in this experiment. The white light source comes from light-emitting diode (LED) backlight with a broad wavelength range. Blue, green and red light sources are light-emitting diodes with 467 nm, 536 and 631 nm wavelengths. These spectrums of four light sources are shown in Fig. 4-5. The light source was set up above the device to irradiate the sample from the top. The light power was controlled by the power supply (PPT3615). The light intensity was adjusted by changing the applied voltage. The light intensity range was from 50 μW/cm^2 to 8.5 mW/cm^2. The Fig. 5-1 shows the illumination system and the device structure.

5-4 Characteristics of Pentacene-based OPTs

Electrical transfer characteristics of pentacene-based thin film transistor (OTFT) with PMMA dielectric are shown in the Fig. 5-2. The device channel length varied from 100 μm to 600 μm while channel width was fixed as 1000 μm. Field effect mobility and threshold voltage are near 0.36 cm^2/Vs and -14.5 V extracted from transfer characteristics of devices with different channel widths. The effective capacitance of dual gate dielectric included PMMA and SiO_2 dielectrics is near 23.4 nF/cm^2. I_{on}/I_{off} ratio of devices with channel length varied from 200 μm to 600 μm are near 10^6 but I_{on}/I_{off} ratio of device with 100 μm channel length was reduced to 10^3 due to the large leakage current. In other studies, it was also found that increasing leakage current caused by the short channel effect is a serious problem when improving the device process to short channel.

5-5 Electrical Field Modulation on the Photoresponsivity of OPT

When pentacene-based thin-film transistors (TFTs) are used as switching elements or circuit components, however, the light-induced ΔV_{th} causes serious reliability problems. If pentacene-based TFTs are applied to photodetector, the pronounced threshold voltage shift (ΔV_{th}) under light illumination becomes a good reference. The light-induced ΔV_{th} can be attributed to electron trapping in the interface between gate dielectric and active layer. As a result, increasing the interface state density leads to a more significant light-induced ΔV_{th}. Gate-bias stress and drain-bias was also found to enhance the ΔV_{th} under illumination because that the positive gate-bias stress produces extra negative-charged defects. As shown in Fig. 5-3, the initial transfer characteristics (line) and those after a 100-sec illumination (symbols) are compared. Without gate bias stress, the transfer characteristic slightly shifts forward positive after a 100-sec illumination. When a gate bias of 15 V is applied during illumination, the transfer characteristic shift is significantly enhanced.

5-5-1 Gate and Drain Bias Effect

First, the light-induced ΔV_{th} is investigated using bias stress to control the light-induced threshold voltage shift. The light-induced ΔV_{th} is defined as $V_{th} - V_{th}^{ini}$, where V_{th}^{ini} and V_{th} are threshold voltages under illumination before and after bias stress. The white light source is used to illuminate the device (W/L = 1000 μm/200 μm) with an intensity 600 μW/cm^2 for 100 sec. During illumination, bias stress is also applied using different stressed gate bias (V_{GS}^{st}). Stressed drain bias (V_{DS}^{st}) is 0 V or equal to V_{GS}^{st}. Source electrode is grounded. Before and after the 100-sec illumination with different stress conditions, transfer characteristics are measured promptly under illumination. Then, the light-induced ΔV_{th} is plotted as a function of V_{GS}^{st} in Fig. 5-4. White circles represent the light-induced ΔV_{th} for grounded drain while black circles represent the light-induced ΔV_{th} for $V_{DS}^{st} = V_{GS}^{st}$. When $V_{GS}^{st} = 0$ V, the light-induced ΔV_{th} is a small positive value because of the electron trapping. When a negative gate bias is applied during illumination, light-induced ΔV_{th} shifts to become negative owing to the compensation between the light-induced electron trapping and the bias-induced hole trapping. Applying positive gate bias obviously enhances the light-induced ΔV_{th} owing to electron trapping. Effective electron trapping results from the separation of light-generated excitons and the equilibrium of trapping and recombination. The separation of excitons can be enhanced by an electric field through field-induced dissociation [4, 6, 7]. In our study, the electric field across the channel film close to source/drain electrodes (vertical field) is usually much higher than the electric field along the channel length from source to drain electrodes (lateral field). High vertical field (higher than 2×10^4 V/cm [9]) may be effective in dissociating excitons. Additionally, vertical electric field causes downward band bending at organic/dielectric interface to provide empty trapping states [10]. Lateral field, on the other hand, may facilitate the removal of holes through source electrode to prevent recombination [11]. As shown in Fig. 5-3, when V_{DS}^{st} changes from 0 V to be equal to V_{GS}^{st}, the vertical electric field is reduced and the lateral electric field is increased. The light-induced ΔV_{th} is significantly reduced when $V_{DS}^{st} = V_{GS}^{st}$, implying that the light-induced ΔV_{th} is dominated by vertical field rather than by lateral field.

5-5-2 Channel Length Effect

The removal of holes, however, is still found to be essential when we compare light-induced ΔV_{th} for devices with L varying from 600 µm to 100 µm, as shown in Fig. 5-5. Reducing L significantly increases the light-induced ΔV_{th}. Since the removal of light-induced holes is more effective near the source/drain electrodes than in the center of the channel, increasing L reduces the portion of source/drain-affected areas and suppresses the light-induced ΔV_{th}. The channel length effect reveals that the removal of light-induced holes through source/drain electrodes is necessary to allow light-induced electrons to be effectively trapped by deep states.

5-5-3 Gate Bias Stress under Dark

Although using drain bias stress and gate bias stress can modulate the device responsivity, the bias stress effect on light-induced ΔV_{th} should be considered. In this experiment, 1000-sec positive and negative gate bias were applied to pentacene-based TFT with PMMA dielectric. After 1000-sec bias stress, ΔV_{th} curves are plotted as a function of the stress time. Obviously, the positive gate bias stress caused slight the device ΔV_{th}. Compare with previous light-induced ΔV_{th} under bias stress, the bias-induced ΔV_{th} can be neglected as shown in Fig. 5-6. However, for the negative gate bias stress, the pronounced ΔV_{th} is observed as shown in Fig. 5-7. Because the hole carriers can easily enter the pentacene from gold contact, the high hole concentration induces the large threshold voltage shift.

5-5-4 Recovery of Light-Induced Threshold Voltage Shift

In previous studies, it was found that the light-induced threshold shift can be recovered after removing illumination. But we found that the source and drain biases help sustain the light-induced ΔV_{th} after removing irradiation. In this experiment, it was found that applying gate bias also can sustain the light-induced ΔV_{th} after removing irradiation compared.

In further study, different cases were discussed to sustain the light-induced ΔV_{th} of pentacene-based TFT with PMMA dielectric after removing light. Following three cases are used to compare the retention ability after the light-induced ΔV_{th} reaches saturation. Case (1) keep V_{GS}^{st} = 15 V in dark, case (2) keep V_{GS}^{st} = 0 V under illumination and case (3) keep V_{GS}^{st} = 0 V in dark. With almost identical initial light-induced ΔV_{th}, before comparing different conditions, devices are applied by a 500-sec white light illumination with gate bias stress. The gate bias and light intensity are 15V and 600 μW/cm^2. When (2) and (3) conditions were performed, the recovery of light-induced ΔV_{th} was observed as shown in Fig. 3.8. However, for the condition (1), the light-induced ΔV_{th} is sustained for over 2100 seconds. Fig. 5-9 shows that only applying illumination or stressing device in dark, the device ΔV_{th} is slight compared with combining illumination and positive gate bias.

5-6 Photoresponsivity of Pentacene-Based OPT

5-6-1 Wavelength Effect on Photoresponsivity of OPTs

According to the study proposed by Yong-Young Noh, Dong-Yu Kim and Kiyoshi Yase [8], the influence of wavelength on the irradiation effect of pentacene-based OTFTs had been discussed. A smaller light-induced ΔVth was found when the incident light had larger wavelength due to the internal filter effect. When illuminating the pentacene-based TFTs, the device threshold voltage shifted toward positive because that the light-induced electrons close to the gate dielectric were trapped by the interface states. If the wavelength had high absorption in pentacene, it was not able to arrive at the gate dielectric interface effectively. In this experiment, red, green and blue light-emitting diodes (LEDs) were used as light sources to discuss light wavelength influence on the device ΔV_{th}. Fig. 5-10 shows that the device ΔV_{th} increased with decreasing light wavelength. Based on the internal filter effect, the light-induced ΔV_{th} was dominated by light absorption spectrum.

5-6-2 Photoresponsivity Variation for Different Light Intensity

Using different light intensity to illuminate the device studies the gate bias dependence of OPTs Photoresponsivity. The linear-region transfer characteristics of the devices before stress and after 100-sec illumination with various gate bias stresses while varying light intensity 50 μW/cm^2 to 400 μW/cm^2 are depicted in Fig. 5-11, 5-12 and 5-13. All the devices exhibit similar original characteristics, so only one curve is shown to represent the characteristics before stress. Fig. 5-11, 5-12 and 5-13 show the evolution of linear-region transfer characteristics during a 100-sec illumination time under different light intensity. Obviously, increasing the gate-bias stress increases the shift of the transfer characteristics.

The light-induced ΔV_{th} with 100-sec illumination is plotted as a function of light intensity (P_L) under various gate biases in Fig. 5-14. When V_{GS} = 5 V, the light-induced ΔV_{th} is small and saturates when P_L reaches 200 μW/cm^2. Increasing V_{GS} from 5 V to 15 V, the light-induced ΔV_{th} is enlarged and the saturation points moves to higher P_L. However, when extending illumination time from 100-sec to 3000-sec, the light-induced ΔV_{th} reaches the similar saturation value under different light intensity illumination as shown in Fig. 5-15. As aforementioned, vertical electric field helps separate excitons as well as cause downward band bending. Increasing P_L increases the number of excitons inside the organic active layer. With a fixed vertical electric field, it is presumed that a fixed ratio of excitons can be separated. However, a saturated light-induced ΔV_{th} is observed under high P_L, implying that the exciton separation may not be the bottleneck reaction for the generation of light-induced ΔV_{th}. The downward band bending controlled by gate bias, on the other hand, plays an important role.

A band diagram from gate to drain/source is depicted to explain the proposed mechanism. Fig. 5-16 shows the energy band diagram under illumination without applying V_{GS}^{st}. When applying a positive gate bias V_{GS}^{st} = 5 V, the lowered Fermi energy (E_F) in the gate electrode leads to a downward band bending of pentacene near the gate side as shown in Fig. 5-17. A fixed amount of trap states moves to be below the Fermi energy and tends to trap free electrons. When P_L increases from 50 μW/cm^2 to 200 μW/cm^2, increased photo-generated electrons fill into the trap states to enhance light-induced ΔV_{th}. After the states are fully occupied, increasing P_L can no longer enhance electron trapping and the light-induced ΔV_{th} saturates under high P_L as shown in Fig. 5-18. When gate bias is changed from 5 V to 15 V, downward band bending is enhanced and the amount of empty trapping states is increased as shown in Fig 5-19. This allows more photo-generated electrons to be trapped and provide a larger response window to different P_L. Also, for a very weak light such as P_L = 50 μW/cm^2, increasing V_{GS} can effectively enlarge the light-induced ΔV_{th} as well as R_{ph} as shown in Fig. 5-20. If no bias is applied on OPT, it is almost impossible to detect the weak light with P_L = 50 μW/cm^2. Under while LED irradiation, increasing V_{GS} to be 30 V enlarges R_{ph} to be 10 A/W and 40 A/W for OPTs with L as 200 μm and 100 μm, respectively. R_{ph} reaches 92 A/W when OPT with L as 100 μm is biased by 30-V V_{GS} and irradiated under blue LED with a wavelength as 465 nm and a power density as 50 μW/cm^2. It is summarized that increasing gate bias during illumination can effectively increase detection dynamic range and also enhance the sensing ability to very weak light intensity in the range of μW/cm^2.

5-7 Operation Method of Pentacene-Based Phototransistors

Finally, repeated sensing behavior is confirmed by applying periodic gate bias onto devices during illumination. As shown in Fig. 5-21, the V_{GS}^{st} waveform consists of four sequential potential steps (15 V, 0 V, -20 V, and 0 V). Every potential step has a 50-sec duration. V_{GS}^{st} as +15 V determines the sensing period. V_{GS}^{st} as -20 V is used to accelerate the recovery of the sensing signal. The light-induced ΔV_{th} and photocurrent variations (ΔI_{ph}) are plotted as a function of time. ΔI_{ph} is defined as $I_{\mathrm{ph}} - I_{\mathrm{ph}}^{\mathrm{ini}}$ where $I_{\mathrm{ph}}^{\mathrm{ini}}$ is the drain current measured promptly under irradiation. Though long-time integration (several tens of seconds) is needed to obtain significant ΔI_{ph} and ΔV_{th}, its application on a large-area flexible scanner is possible. During scanning, OPTs are turned off (with a positive gate bias). They are turned on only in the signal reading cycles. This is beneficial for power saving. During recovery period, incomplete recovery is due to an incomplete compensation between electron and hole trapping, and can be treated as noise. The noise can be eliminated if the variation of ΔV_{th} and ΔI_{ph} in sensing period is used as sensing index, as shown by the black symbols in Fig. 5-17.

5-8 Conclusions

Light-induced threshold voltage shift ΔV_{th} and photosensitivity R_{ph} of pentacene-based OPT are greatly improved by applying positive gate bias during illumination or by reducing the channel length. It is verified that even when vertical electric field plays a dominant role in enhancing the light-induced ΔV_{th}, the removal of light-induced holes through source/drain electrodes is necessary to allow light-induced electrons to be effectively trapped by interface states. When increasing

P_L, the maximum light-induced ΔV_{th} of OPT was restricted owing to the fixed amount of interface trap states under a constant gate bias. Increasing the positive gate bias extends the response window to larger P_L and improves R_{ph} to very weak light. Finally, the repeated OPT response to different P_L is confirmed by applying periodic voltage signal cycle. These results are useful to design OPT in image sensor array.

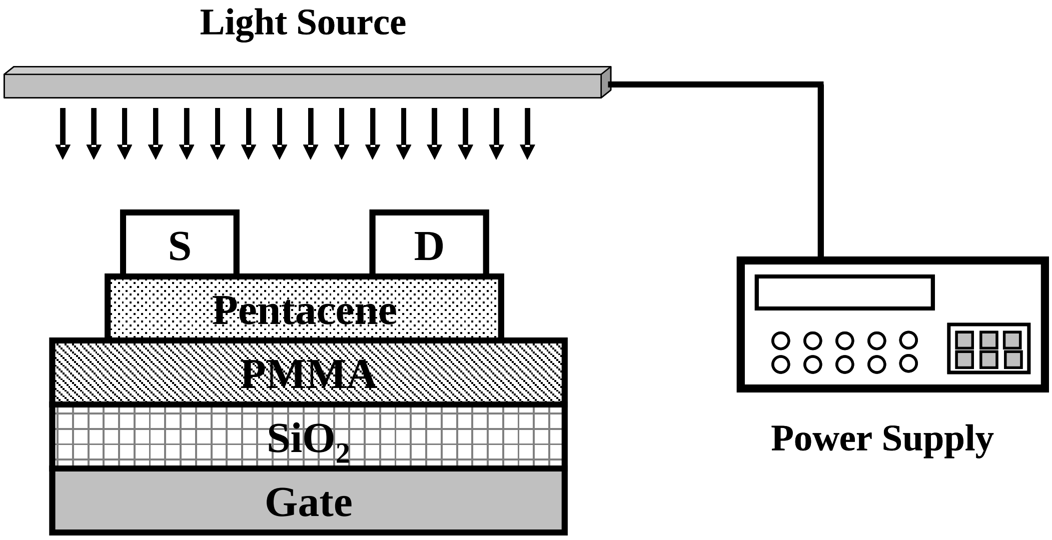


Fig. 5-1 The illumination system and conventional top-contact bottom-gate pentacene-based TFT. A 100-nm thickness of SiO_2 and PMMA are served as dual gate dielectric.

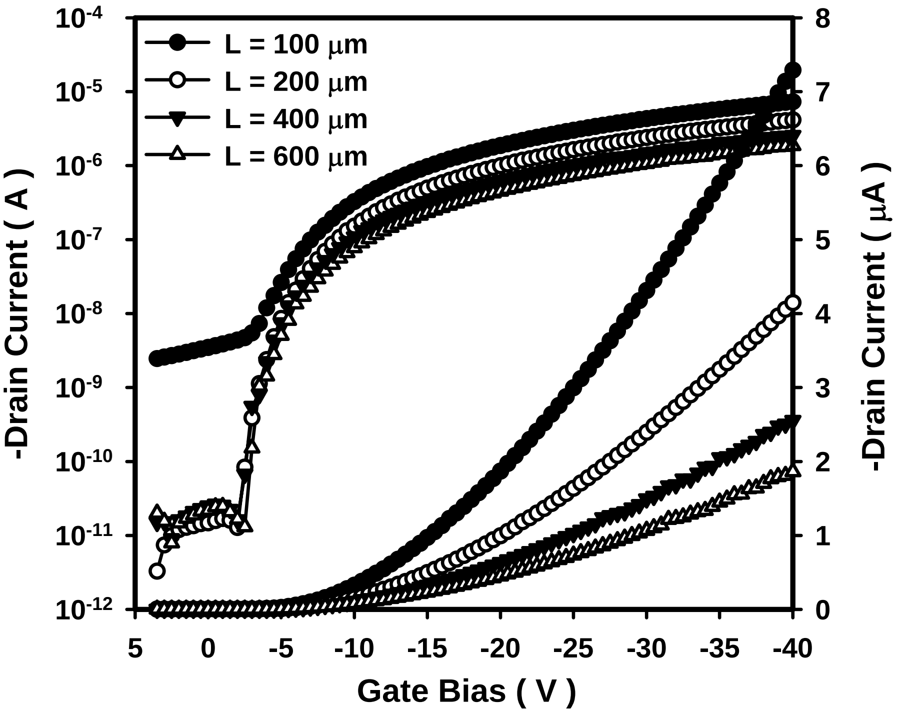


Fig. 5-2 The initial transfer characteristics of OTFTs with different channel length. Channel length is varied from 100 μm to 600 μm

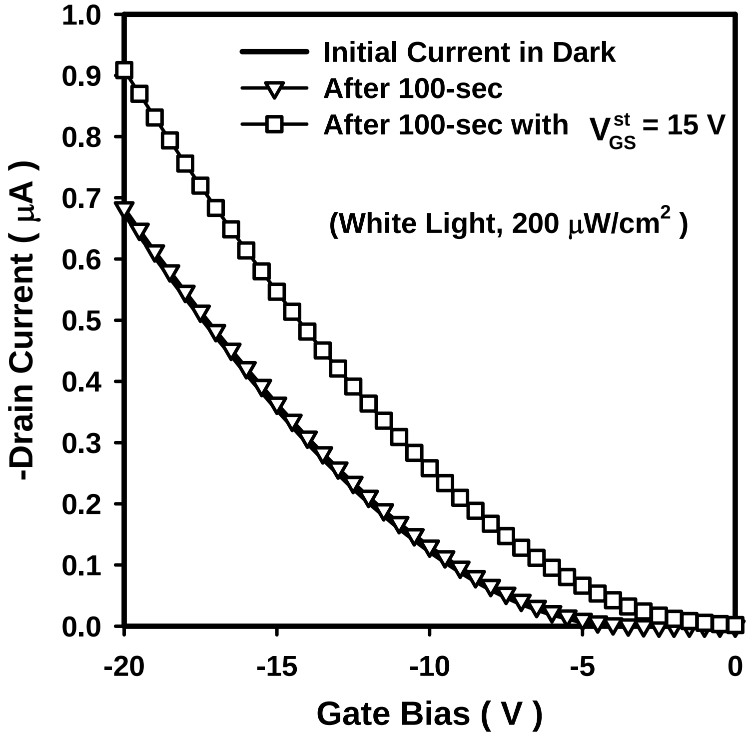


Fig. 5-3 Transfer characteristics of OTFTs before and after a 100-sec illumination with and without gate bias. The stress conditions are: V_G = 0 V and 10 V, $V_D = V_S$ = 0 V.

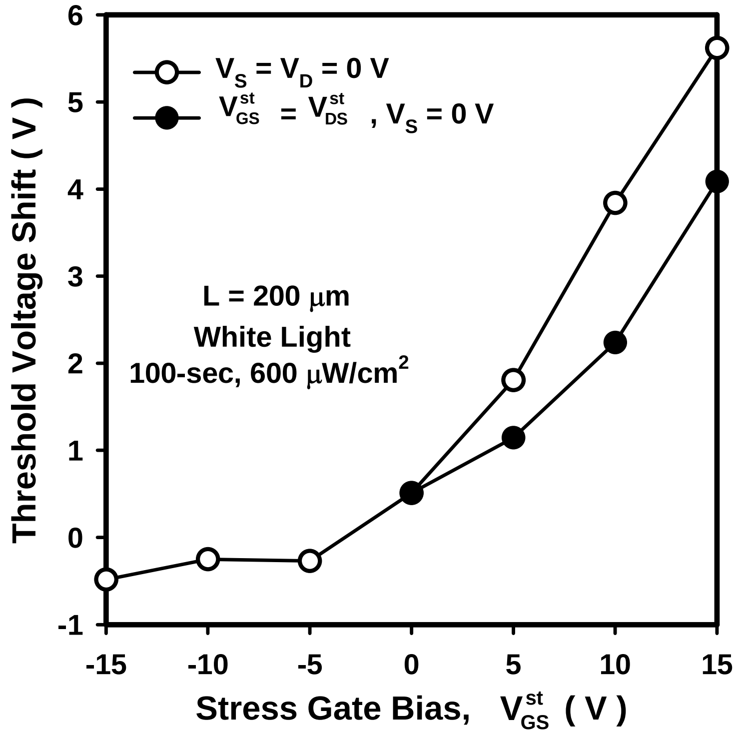


Fig. 5-4 The light-induced threshold voltage shifts ΔV_{th}^{Light} as a function of gate bias. The bias conditions are: $V_D = V_S$ = 0 V and V_{DS}^{st} = V_{GS}^{st}, V_S = 0 V.

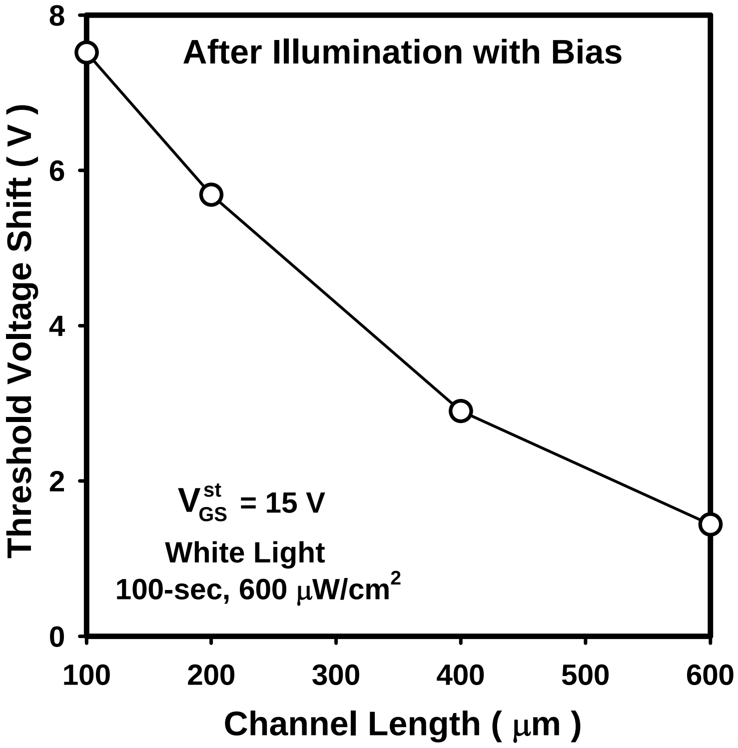


Fig. 5-5 The light-induced threshold voltage shifts ΔV_{th}^{Light} as a function of the channel length.

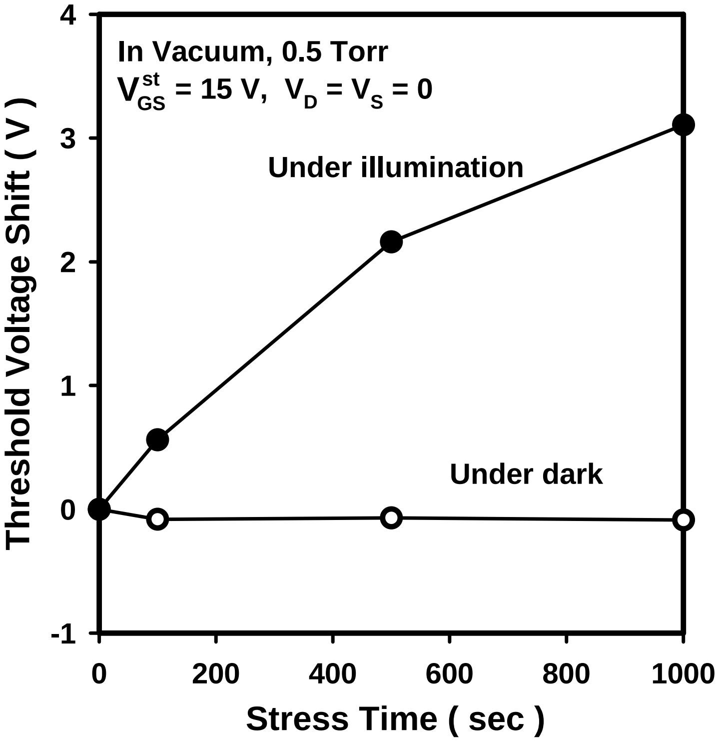


Fig. 5-6 Threshold voltage shift (ΔV_{th}) of PMMA-OTFT during positive gate bias stress in ambient air when under dark and illumination. The bias stress conditions: $V_G - V_{th}^{ini}$ = 15 V, $V_D = V_S$ = 0 V.

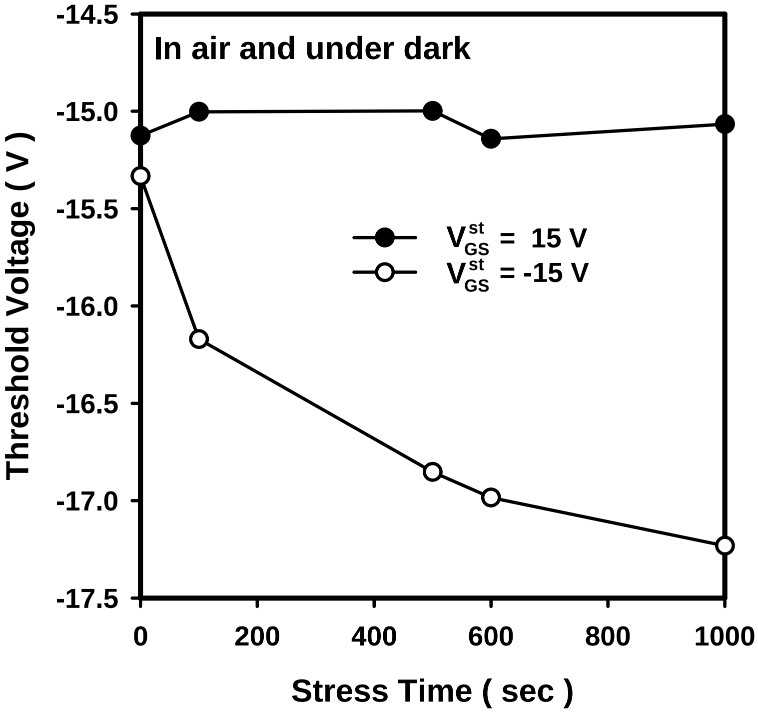


Fig. 5-7 Threshold voltage shift (ΔV_{th}) of PMMA-OTFT during positive and negative gate bias stress in ambient air and under dark. The bias stress conditions: $V_G - V_{th}^{ini}$ = 15 V and -15 V, $V_D = V_S$ = 0 V.

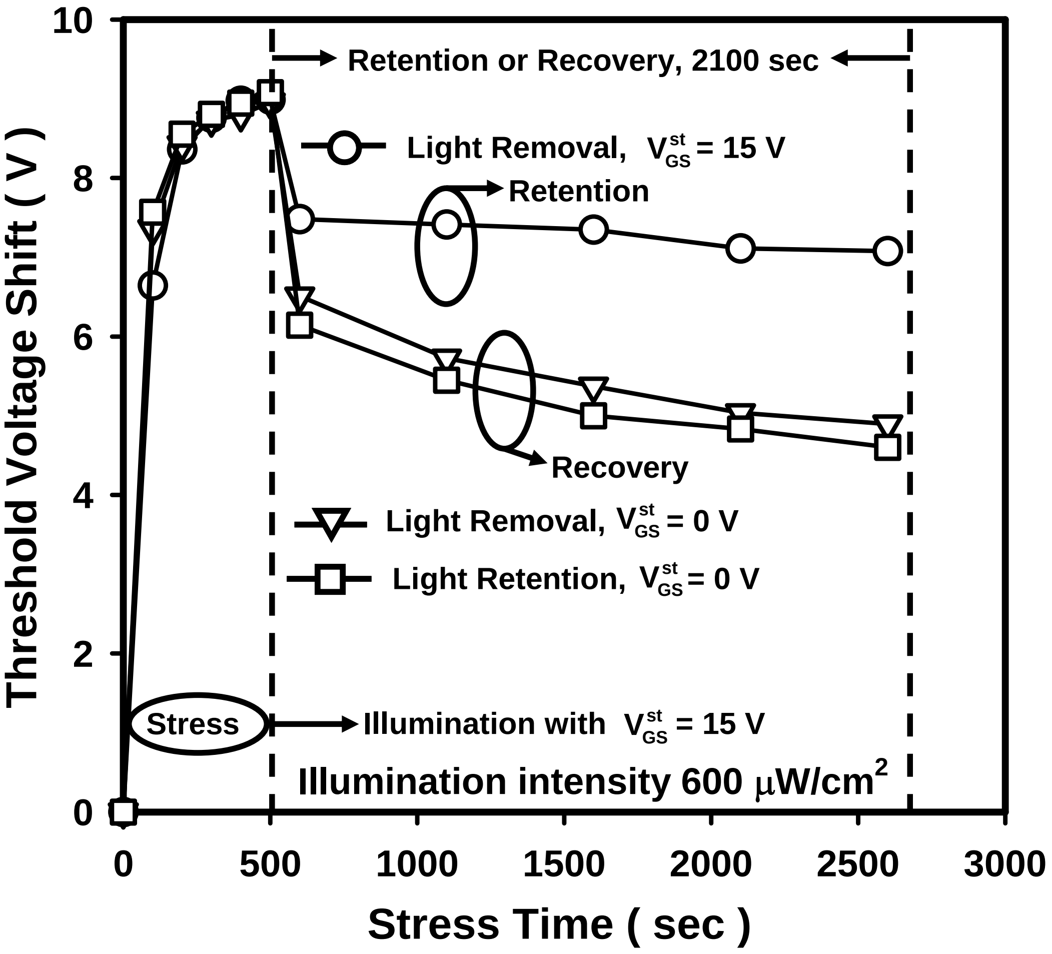


Fig. 5-8 After trap states are fully occupied, the light-induced ΔV_{th} as a function of recovery time under various gate bias (V_G = 0 V, or V_G = 15 V) while drain and source are grounded with and without light removal. The bias stress conditions: $V_G - V_{th}^{ini}$ = 15 V, $V_D = V_S$ = 0 V and light intensity is 600 μW/cm^2.

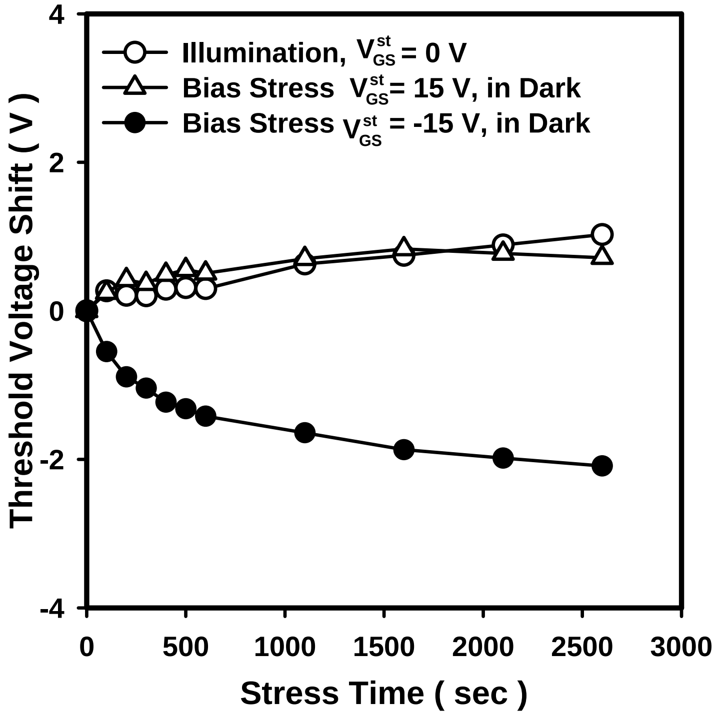


Fig. 5-9 Threshold voltage shift (ΔV_{th}) of PMMA-OTFT during various bias stress under dark or during prolonged illumination. The bias stress conditions: $V_G - V_{th}^{ini}$ = 15 or -15 V, $V_D = V_S$ = 0 V and light intensity is 600 μW/cm^2.

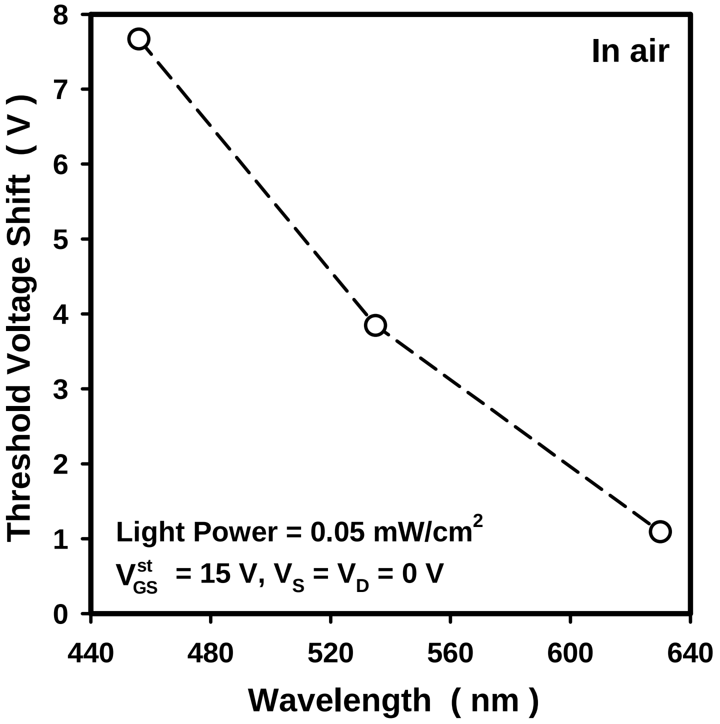


Fig. 5-10 Threshold voltage shift (ΔV_{th}) of PMMA-OTFT after bias stress under illumination with different light wavelength. The bias stress conditions: $V_G - V_{th}^{ini}$ = 15 V, $V_D = V_S$ = 0 V and light intensity is 0.05 mW/cm^2.

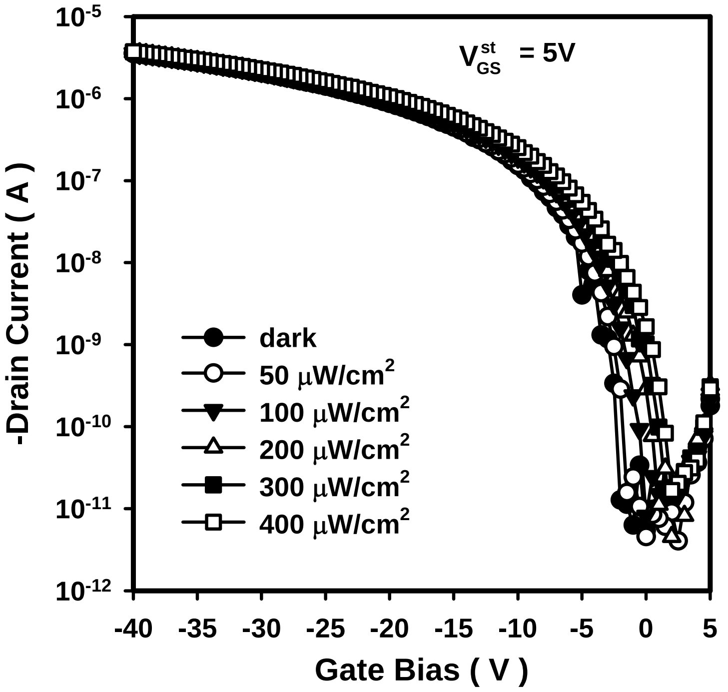


Fig. 5-11 Transfer characteristics of OTFT before and after 100-sec illumination. The light intensity is varied from 50 μW/cm^2 to 400 μW/cm^2. The gate bias stress conditions: $V_G - V_{th}^{ini}$ = 5 V and V_{DS} = 0 V.

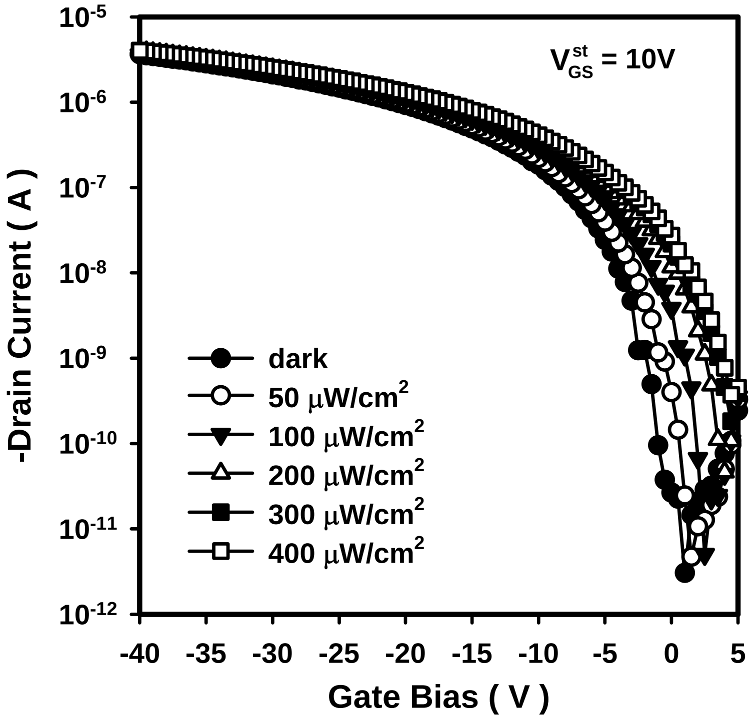


Fig. 5-12 Transfer characteristics of OTFT before and after 100-sec illumination. The light intensity is varied from 50 μW/cm^2 to 400 μW/cm^2. The gate bias stress conditions: $V_G - V_{th}^{ini}$ = 10 V and V_{DS} = 0 V.

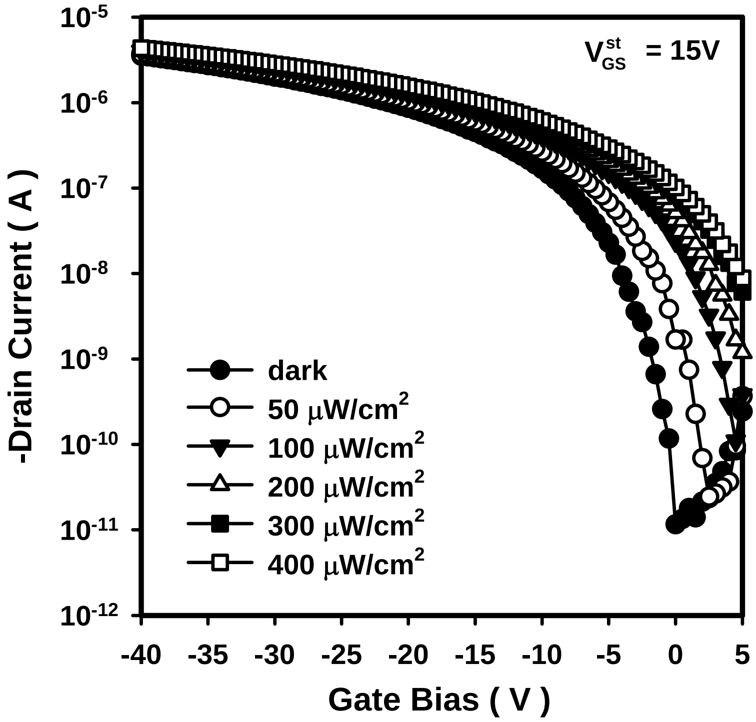


Fig. 5-13 Transfer characteristics of OTFT before and after 100-sec illumination. The light intensity is varied from 50 μW/cm^2 to 400 μW/cm^2. The gate bias stress conditions: $V_G - V_{th}^{ini}$ = 15 V and V_{DS} = 0 V.

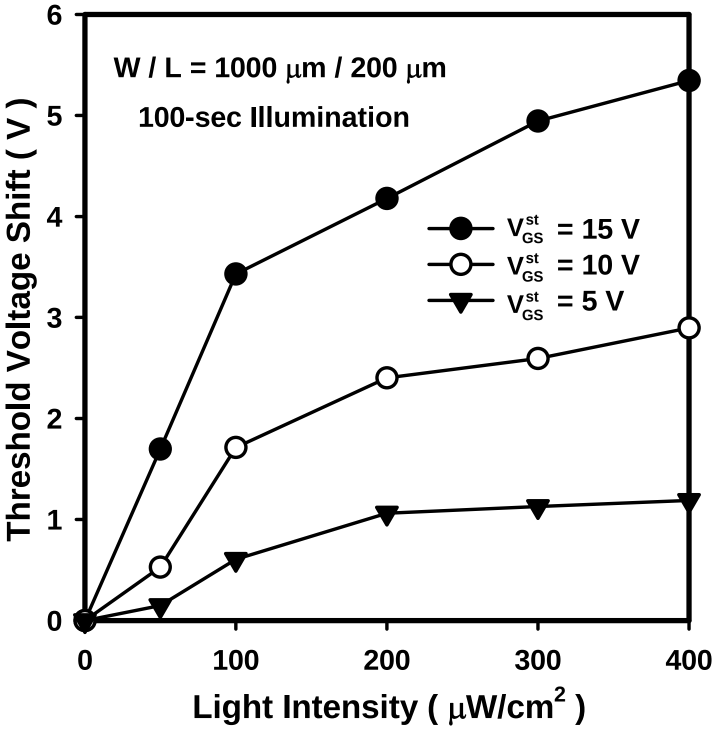


Fig. 5-14 ΔV_{th}^{Light} as a function of light intensity under various gate biases. The gate stress bias conditions: V_{GS}^{st} = 5, 10 and 15 V while $V_S = V_D$ = 0V.

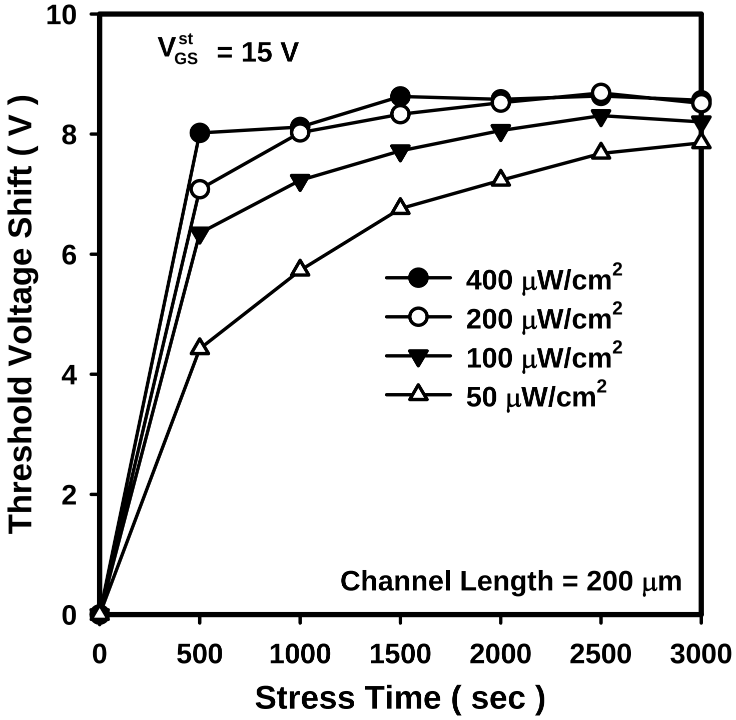


Fig. 5-15 ΔV_{th}^{Light} as a function of stress time under various light intensity. The gate stress bias conditions: V_{GS}^{st} = 15 V while $V_S = V_D$ = 0V.

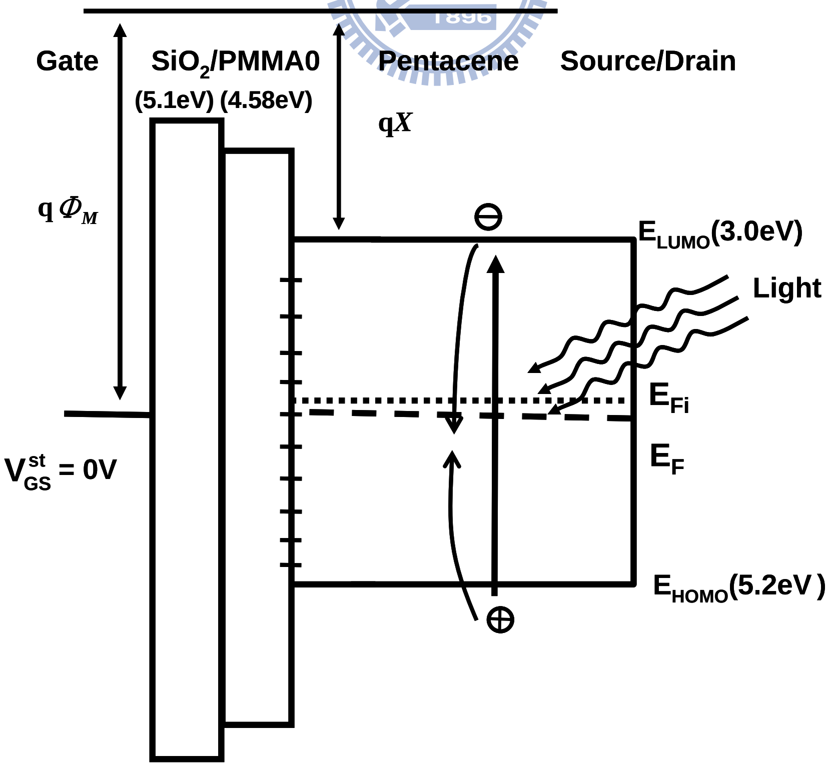


Fig. 5-16 Energy-band diagram of OPT from gate to drain/source when devices are under illumination without gate bias.

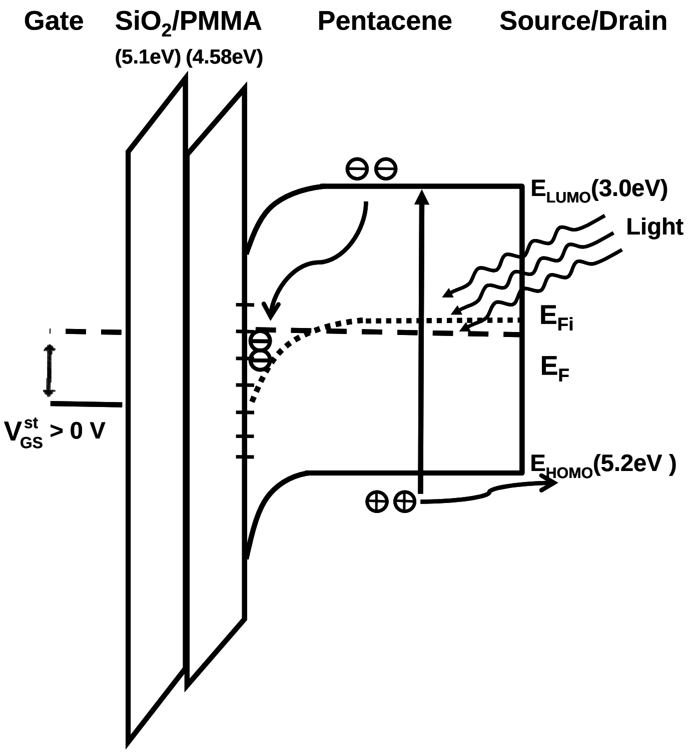


Fig. 5-17 Energy-band diagram of OPT from gate to drain/source when devices are under illumination with gate bias (5V) before trap states are fully occupied.

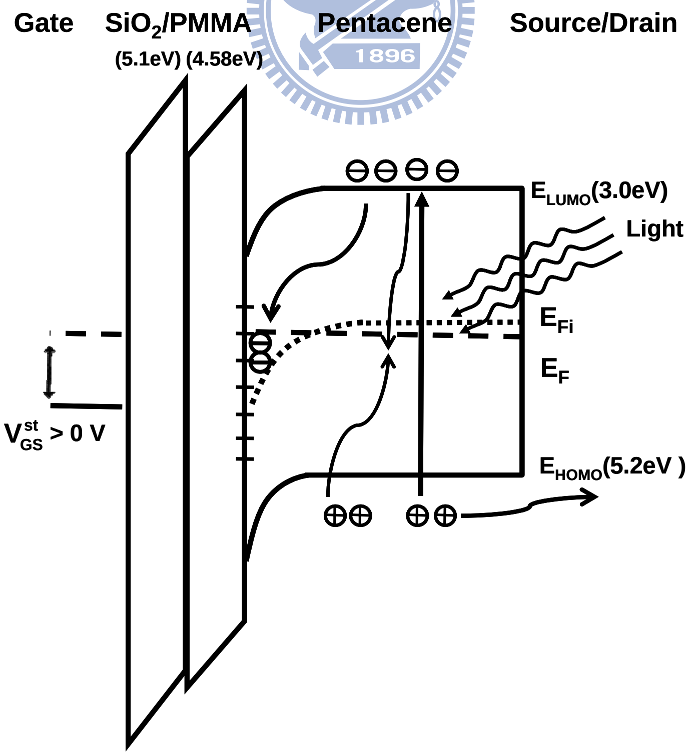


Fig. 5-18 Energy-band diagram of OPT from gate to drain/source when devices are under illumination with gate bias (5V) after trap states are fully occupied.

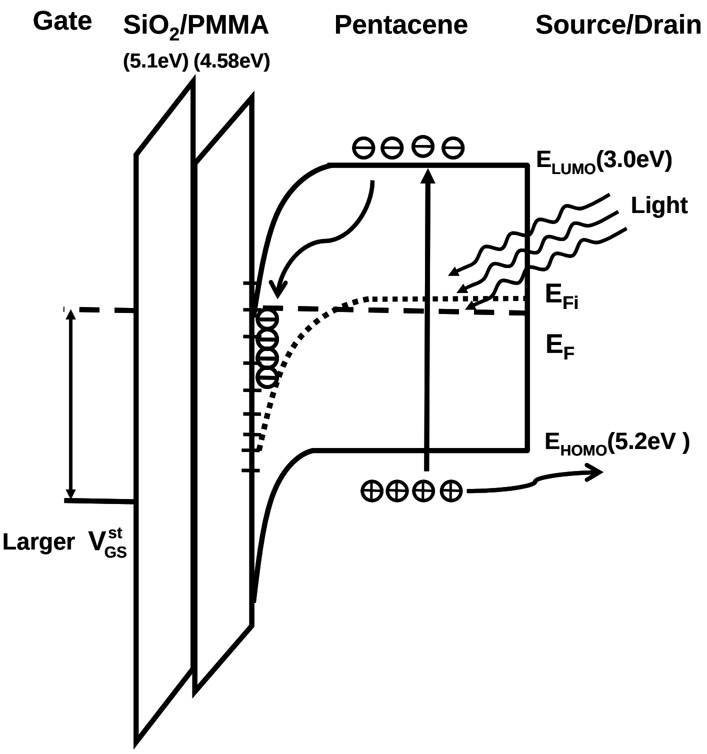


Fig. 5-19 Energy-band diagram of OPT from gate to drain/source when devices are under illumination with gate bias (15V) before trap states are fully occupied.

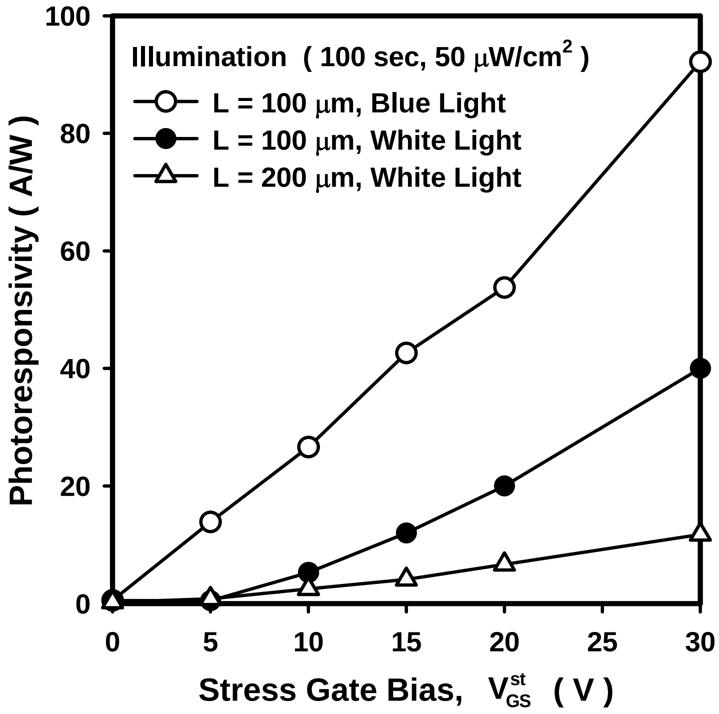


Fig. 5-20 R_{ph} as a function of gate stress bias under blue light and white light illumination. Channel length are 100 μm or 200 μm. The illumination time is 100 sec and light intensity is 50 μW/cm^2.

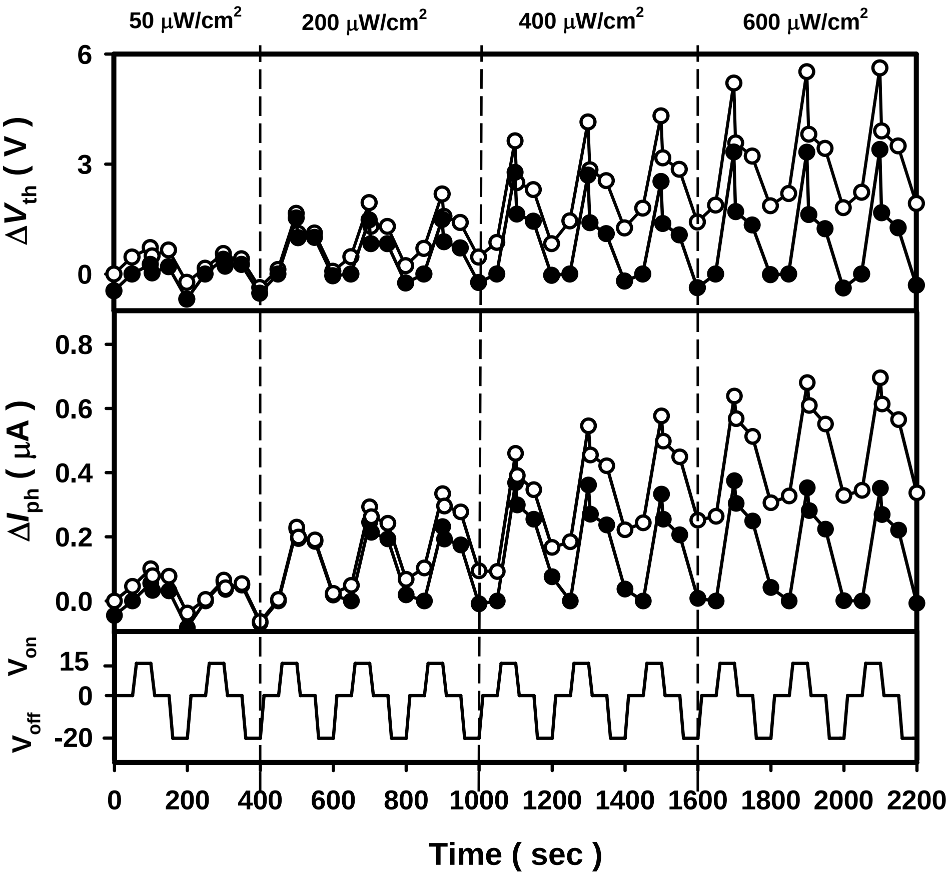


Fig. 5-21 ΔV_{th}^{Light} and photo current difference ΔI_{ph} measured by applying periodical gate bias under various light intensities. V_{GS}^{st} waveform consists of sequential four potential steps (15V, 0V, -20V, 0V). ΔV_{th}^{Light} and ΔI_{ph} normalized to the initial value of every cycle is also shown by black circles.

Chapter 6

a-Si:H TFTs on Polyimide Substrate

6-1 Introduction

Hydrogenated amorphous silicon thin-film transistors (a-Si:H TFTs) fabricated on plastic substrates have drawn a lot of attention in the past decade [1,2]. Compared with glass substrates, plastic substrates have advantages such as flexible, light, thin and reduced incidences of breakage. Many reports have successfully demonstrated the fabrication of a-Si:H TFTs on plastic substrate [3,4]. However, when plastic substrates are used, the process temperature usually has to be lower than 180 °C. Depositing low-leakage dielectric layer and low-defect a-Si:H layer at such a low temperature is a great challenge. Low-temperature a-Si:H TFTs on plastic substrates also exhibit more significant bias-stress induced reliability issues than a-Si:H TFTs fabricated at standard temperature (250 °C ~ 300 °C) on glass substrates [5]. After prolonged gate bias stress, pronounced threshold voltage shift (ΔV_{th}) was observed. Charge trapped inside the dielectric layer (silicon nitride) and the creation of dangling bonds in a-Si:H film are two major reasons for ΔV_{th}. Some also reported that, when gate bias stress is applied under high temperature, dielectric-trapped charges emitted from defective gate dielectric to a-Si:H layer increase gate leakage current and generate abnormal ΔV_{th}[6].

Using plastic substrates not only limits the process temperature but also causes serious self-heating effect. As will be discussed later in this paper, a-Si:H TFTs on plastic substrate can exhibit more pronounced self-heating effect than those on glass substrate can since plastic substrate usually has larger thermal resistance than glass substrate does. According to the study on self-heating effect in a-Si:H TFTs reported by Wang *et al.* [7], heat dissipation to the ambient are primarily through the gate, the source and the drain contacts. The path through the gate contact via the gate insulator is the most effective. When heat dissipates through gate contact, the thermal resistance of the substrate dominates the thermal dissipation from gate contact to the ambient. We propose that using plastic substrate instead of glass substrate increases the thermal resistance of the substrate and hence enhances self-heating effect in a-Si:H TFTs. In this paper, it is found that the heat dissipation problem together with the defective a-Si:H film deposited at low temperature causes serious self-heating enhanced bias-stress effect for a-Si:H TFTs on plastic substrate.

In this study, we use a colorless 18 × 18 cm^2 and 40-μm-thick polyimide (PI) substrate with transmittance of visible light (λ = 400 nm ~ 700 nm) nearly 90 % [2]. With process temperature lower than 160 °C, mobility, threshold voltage and subthreshold swing of a-Si:H TFTs are 0.42 cm^2/V.s , 7 volts and 0.77 V/decade, respectively. With various kinds of bias stress (gate-bias stress and two-terminal bias stress in which gate and drain bias stress are applied simultaneously) at temperature ranging from 25 °C to 60 °C, stable gate dielectric property is verified when the gate leakage current keeps as low as 10^{-13} $\mathrm{A/cm}^2$. When different drain bias stress is applied on devices with different channel widths, influences of channel carrier concentration and self-heating effect on ΔV_{th} are investigated. Finally, the substrate bending effect on the self-heating enhanced ΔV_{th} is also discussed.

6-2 Experimental

6-2-1 Device Fabrication

Bottom-gate a-Si:H TFTs with a back-channel-etch (BCE) structure were fabricated on clear polyimide substrates.

Step1. Gate metal fabrication

A Ti/Al/Ti tri-metal layer with a total thickness of 200 nm was deposited by RF sputtering and then patterned by dry etching to form the gate electrodes. Opposing internal stresses of Ti and Al is compensated, preventing the cracking of the polyimide substrate.

Step2. *SiN_x, a-Si:H and n^+ a-Si:H deposition*

SiN_x, a-Si:H and n+ a-Si:H films were deposited sequentially by the parallel electrode 13.56MHz RF-PECVD at 160 °C. Thicknesses of SiN_x, a-Si:H, and n^+ a-Si:H layers were 300, 200, and 50 nm, respectively. An active island was then formed by the island etching process.

Silicon nitride films were deposited from a mixture of $SiH_4/NH_3/N_2/H_2$ gases (40/148/650/700 sccm), and the RF power was 340W. Hydrogenated amorphous silicon films were deposited from a mixture of SiH_4/H_2 gases (50/450 sccm), and the RF power was 30 W. The lower RF power was used to avoid the plasma damage to the active layer. Moreover, phosphine was used as a dopant source during n^+ layer deposition.

Step3. *Contact metal and passivation fabrication*

The source/drain metals were deposited and defined by dry etching to form the source/drain electrodes. Then, the n^+ layer region between the source and drain electrodes was etched away. Finally, a 300 nm thickness of SiN_x was deposited as the passivation layer.

The schematic diagram of the bottom-gate a-Si:H TFT on polyimide substrate is shown in Fig. 6-1.

6-2-2 Measurement and Bias Stress Conditions

Electrical characteristics of devices were measured using a HP 4156A electrical analyzer to extract V_{th}^{ini}, threshold voltage (ΔV_{th}), field-effect mobility (μ_{FE}) and subthreshold slope (*S.S.*).

Gate-bias stress and two-terminal bias stress were applied to devices with channel width varied from 10 μm to 80 μm while channel length was fixed as 8 μm. When gate-bias stress was applied, source and drain were connected to ground. When two-terminal bias stress was used, gate bias minus threshold voltage was equal to drain bias ($V_D = V_G - V_{th}^{ini}$) while source was grounded, where V_{th}^{ini} is the initial threshold voltage before bias stress. The device enters the saturation region and causes the depletion region near the drain electrode. The electron concentration in the channel is not uniform and electron carriers pass through the device channel.

6-3 a-Si:H TFTs on Polyimide Substrate

6-3-1 Transfer Characteristics of a-Si:H TFTs on Polyimide Substrate

Figure 6-2 and 6-3 are transfer characteristics and output characteristics of the fabricated devices, respectively. The on/off current ratio at V_D = 10 V is greater than 10^7. The gate-to-source leakage current (I_{GS}) is approximately 10^{-13} A. μ_{FE} and $S.S.$ are 0.42 cm^2 V^{-1}s^{-1} and 0.77 V/decade, respectively. μ_{FE} was extracted by using maximum linear-region transconductance (G_M). In Fig. 1(c), normalized drain current ($I_{DSN} = I_{DS} \times \mathrm{L/W}$) of devices with channel width as 10 μm and 80 μm are compared. Under small drain bias, I_{DSN} of these two devices are similar. Under large drain bias, however, devices with large channel width exhibit much larger I_{DSN} than those with small channel width do. When gate bias and drain bias are increased, devices with large channel width lose saturation characteristics. Self-heating was proposed by Wang *et al.* to explain the observed non-saturated drain current [7].

6-3-2 Bias-Temperature Stress Effect

Then, gate-bias stress effects at different temperatures are studied. Figure 6-4 and 6-5 show the transfer characteristics for devices before and after stress (stress condition: V_G - V_{th}^{ini} = 25 V, V_D = V_S = 0 V) at 25°C and at 60 °C, respectively. Gate-bias stress causes a threshold voltage shift while I_{GS}, μ_{FE}, and *S.S.* are almost unchanged. When temperature increases, the threshold voltage shift becomes more pronounced. Gate leakage current keeps as low as 10^{-13} A, indicating almost unchanged gate dielectric quality.

With identical gate leakage current, larger ΔV_{th}^{ini} produced at higher temperature may be due to the increased defect generation rate. According to the charged-state creation mechanism in a-Si:H film, the defect generation rate is proportional to carrier concentration and the effective carrier trapping time τ_t. τ_t can be expressed as $\tau_t = \nu^{-1} \exp\left(\frac{E_A}{kT}\right)$, where ν is an attempt to escape frequency and E_A is the mean activation energy for the defect generation. ΔV_{th} as a function of stressed gate bias and stress time can be expressed by the stretched-exponential equation [8]:

$$V_{th} - V_{th}^{ini} = \Delta V_{th} = (V_G - V_{th}^{ini})\left\{1 - \exp\left[-\left(\frac{t}{\tau_t}\right)^{\beta}\right]\right\} \tag{1}$$

where V_{th}^{ini} is the initial threshold voltage. β is a weakly temperature-dependent dispersion parameter.

Figure 6-6 depicts ΔV_{th} as a function of stress time at 25°C, 30°C, 40°C, 50°C and 60°C when $V_{Stress} = V_G - V_{th}^{ini} = 25$ V. Also, ΔV_{th}^{ini} under different stress bias V_{Stress} after 1500 sec at 25°C is plotted as a function of V_{Stress} in Fig. 3(b). The experimental data in Fig. 6-6 and Fig. 6-7 can be well explained by Eq. (1) with E_A and β as 0.57 eV and 0.355, respectively. The constant value of β suggests that the weak temperature dependence of β can be neglected in our study. Increasing channel widths from 10 μm to 80 μm does not influence ΔV_{th}.

It is also known that, when ΔV_{th} is dominated by the state creation mechanism, drain bias modulates the average carrier concentration and influences ΔV_{th} [9]. If

$V_{stress} = V_D = V_G - V_{th}^{ini}$, ΔV_{th}^{ini} can be expressed as :

$$V_{th} - V_{th}^{ini} = \Delta V_{th} = \frac{2}{3} \times (V_G - V_{th}^{ini}) \left\{ 1 - \exp\left[-\left(\frac{t}{\tau_t} \right)^{\beta} \right] \right\} \tag{2}$$

This two-terminal stress effect is observed in Fig. 6-8 by plotting ΔV_{th} as a function of stress bias V_{Stress} after 1500-sec stress at 25°C, where $V_{Stress} = V_D = V_G - V_{th}^{ini}$. For small V_{Stress}, ΔV_{th} can be well explained by Eq. (2), verifying the influence of drain-bias modulated carrier concentration as in previous reports [9]. For large V_{Stress}, however, significant deviation of ΔV_T from the theoretical curve is observed. The deviation is more pronounced when devices exhibit larger channel width. This channel width enhanced ΔV_{th} is clearly observed when ΔV_{th} is plotted as a function of different channel widths as shown in the Fig. 6-9.

The above results can be explained by two possible reasons: hot-carrier enhanced charge trapping and self-heating effects. However, the generation of hot carriers usually accompany with significant kink effect. In our experiment, no obvious kink effect is observed from the device output characteristics. Also, when $V_{Stress} = V_D = V_G - V_{th}^{ini}$, devices are biased close to saturation points where the kink effect seldom appears. On the contrary, according to previous reports [7], self-heating is pronounced in a-Si:H TFTs due to the high resistive intrinsic a-Si:H film. Joule heat produced in a-Si:H film close to drain side increases device temperature and enlarges channel current. It is reported that heat dissipation is more effective at channel edge than in the center region. As a result, devices with wider channel width suffer from severer self-heating effect [10].

6-3-3 Self-Heating Effect

To further characterize the self-heating effect, characteristic temperature (T_{ch}) is extracted by fitting the measured ΔV_{th} with those calculated from Eq. (2) when we set different temperatures as shown in Fig. 6-10. E_A and β are 0.57 eV and 0.355. In Fig. 5(b), T_{ch} is plotted as a function of V_{Stress} ($=V_D = V_G - V_{th}^{ini}$) for devices with channel width as 10 μm and 80 μm. The extraction steps of T_{ch} are shown in Fig. 6-11. Obviously, T_{ch} for both devices is 25°C (room temperature) under low V_{Stress}. When V_{Stress} is 40V, T_{ch} rises up to 40°C and 60°C for devices with channel width 10 μm and 80 μm, respectively.

To justify the physical meaning of the characteristics temperature T_{ch}, we calculate the increased temperature due to self-heating effect according to the physical model proposed by Wang et al. [7]. The thermal equivalent circuit is shown in Fig. 6-12. In their model, the temperature increase induced by self-heating effect (ΔT_{SHE}) can be calculated by using the thermal equivalent circuit and can be described by Eq. (3) [11].

$$\Delta T_{SHE} = I_D \times V_{DS} \times R_{th} \qquad (3)$$

where R_{total} is the total thermal resistance that includes the thermal resistances of different heat dissipation paths and the thermal resistance of the substrate. As aforementioned, heat dissipation is dominated by the path through gate contact and substrate. Also, the thermal resistance of the substrate can be given as [7]:

$$R_{sub} = \frac{1}{\pi k W} \ln\left(\frac{16 D_{glass}}{\pi L_g}\right) \qquad (4)$$

where k and D are the thermal conductivity and the thickness of the substrate, respectively. W and L are the channel width and length of a-Si:H TFT. Thermal conductivity of polyimide substrate is about 0.2 $Wm^{-1}K^{-1}$ [11]. By using Eq. (4), the thermal resistance of polyimide substrate is calculated to be 6.4×10^4 K/W when channel width as 80 μm and channel length as 8 μm are considered. The calculation is shown in below:

$$R_{sub} = \frac{1}{3.14\times0.2\times80\times10^{-6}}\ln\left(\frac{16\times4\times10^{-5}}{3.14\times8\times10^{-6}}\right) = 6.4\times10^{4}(\frac{K}{W})$$

The thermal resistance of polyimide substrate is about two times higher that that of conventional glass substrate. The thickness of conventional glass substrate is 1.1 mm. The calculation is shown in below:

$$R_{sub} = \frac{1}{3.14\times0.81\times80\times10^{-6}}\ln\left(\frac{16\times1.1\times10^{-3}}{3.14\times8\times10^{-6}}\right) = 3.22\times10^{4}(\frac{K}{W})$$

After calculating R_{sub}, R_{total} can be obtained according to Ref. [7]. Then, ΔT_{SHE} can be estimated. As shown by Eq. (3), ΔT_{SHE} is proportional to the drain current. When constant bias is applied during stress, drain current decreases as a function of time due to the threshold voltage shift. As a result, Eq. (3) can be modified as Eq. (5) to include the bias-stress effect in self-heating effect.

$$\Delta T_{SHE} = \left(\frac{V_{GS}-V_{th}}{V_{GS}-V_{th}^{ini}}\right)^{2}\left(I_D V_{DS} R_{total}\right) \qquad (5)$$

In Eq. (5), ΔT_{SHE} becomes a function of stress time due to the bias stress effect. With increasing stress time, threshold voltage increases and ΔT_{SHE} decreases. The device temperature due to self-heating effect (T_{SHE}) can then be represented by adding the calculated ΔT_{SHE} with the original environmental temperature (e.g., 25°C). In our study, T_{SHE} for devices with channel width as 80 μm and for 1500-sec stress time is plotted in Fig. 6-13 by triangular symbols. Obviously, T_{SHE} increases with stress bias. The reason to explain the higher value of T_{SHE} when compared with T_{ch} may be because the model above neglects the heat dissipation by heat convention and radiation [10, 13]. As a result, the model overestimates the self-heating effect. The calculated T_{SHE} verifies the existence of significant self-heating effect. It is noted, though, T_{SHE} does not have the channel width effect since R_{sub} does not consider the heat dissipation at channel edge.

6-3-4 Self-Heating Effect on the Bend Substrate

Finally, ΔV_{th} for wide channel device on flat substrate and bent substrate are studied. When stress bias is small, ΔV_{th} for wide channel device on flat substrate and bent substrate are compared in Fig. 6-14 and 6-15. Obviously, ΔV_{th} keeps unchanged for bent substrate with a curvature radius as 15 mm or 7.5 mm. When stress bias is large and self-heating effect appears, ΔV_{th} for wide channel device on flat substrate and bent substrate are compared in Fig. 6-15. Interestingly, ΔV_{th} increases significantly on bent substrate. It is known that outward bending causes tensile stress in the a-Si:H film [14]. When film temperature increases due to self-heating effect, tensile stress accompanies with the elevated temperature may further accelerate the generation of defects and enlarge ΔV_{th}.

6-4 Conclusion

In this study, a-Si:H TFTs are successfully fabricated on colorless polyimide substrates at low process temperature as 160 °C. Device reliability after bias-temperature stress are investigated. Unchanged gate leakage current as 10^{-13} A indicates that the SiN_x layer fabricated at 160 ℃ is stable. Using gate bias stress and two–terminal bias stress at different temperature on devices with various channel widths, threshold voltage shift (ΔV_{th}) due to charged-state creation is well defined. Moreover, self-heating enhanced ΔV_{th} is firstly observed and investigated. Increasing channel width, drain bias, or substrate temperature enhances self-heating effect. The increased temperature facilitates the generation of defect states and therefore enhances ΔV_{th}. Influence of substrate curvature on the self-heating enhanced ΔV_{th} is also firstly demonstrated.

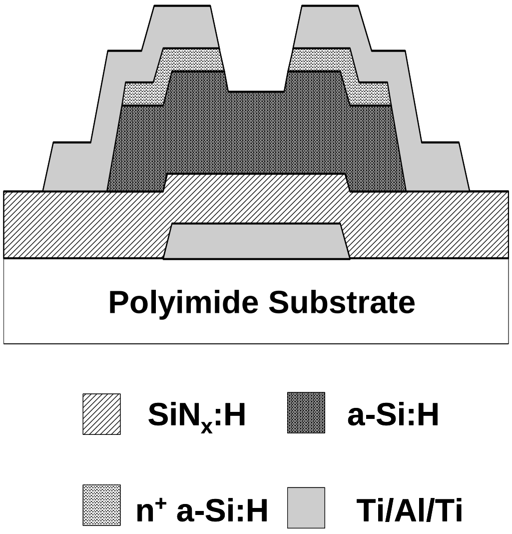


Fig. 6-1 Schematic diagram of the bottom-gate a-Si:H TFT on polyimide substrate.

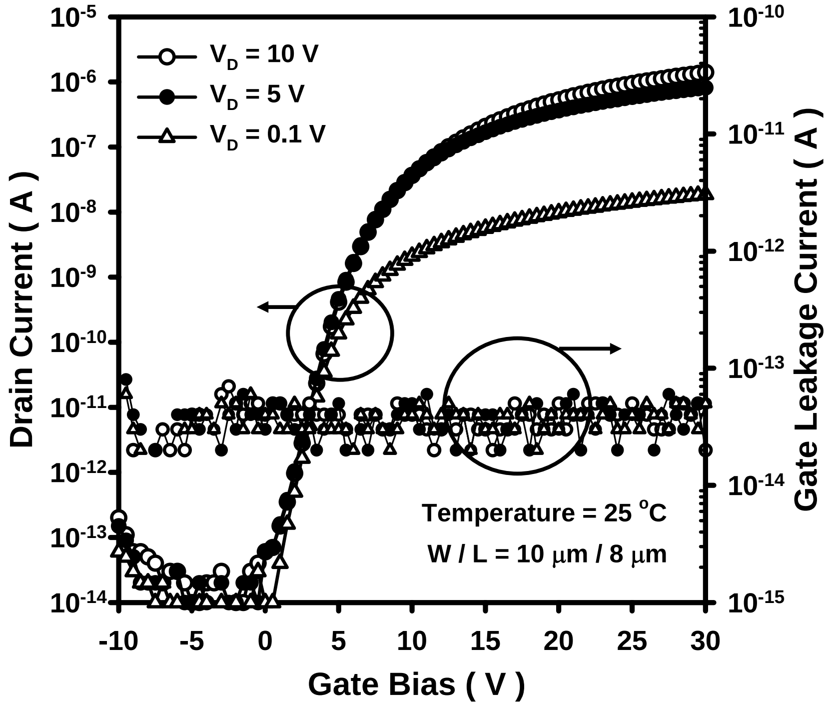


Fig. 6-2 Transfer characteristics of the bottom-gate a-Si:H TFT fabricated at 160°C on polyimide substrate.

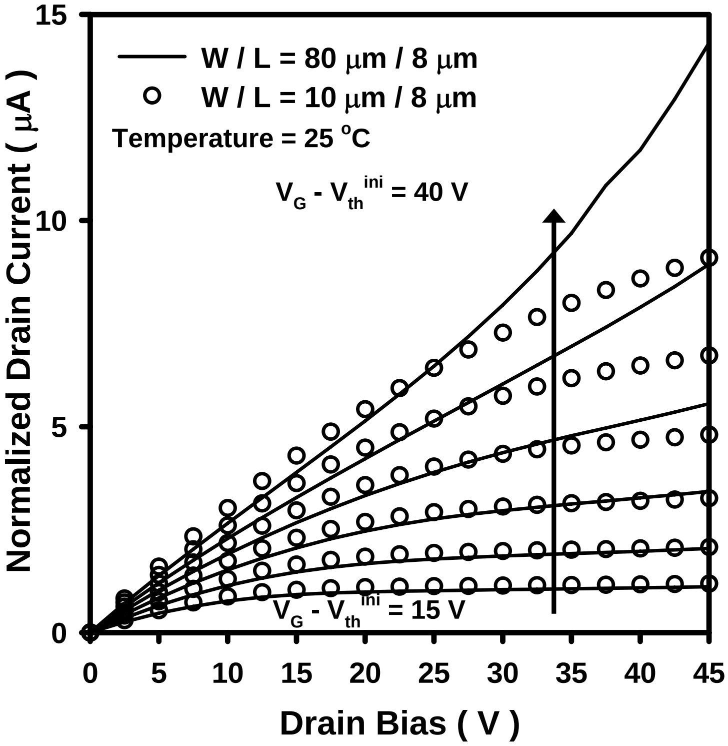


Fig. 6-3 Output characteristics of the bottom-gate a-Si:H TFT fabricated at 160°C on polyimide substrate.

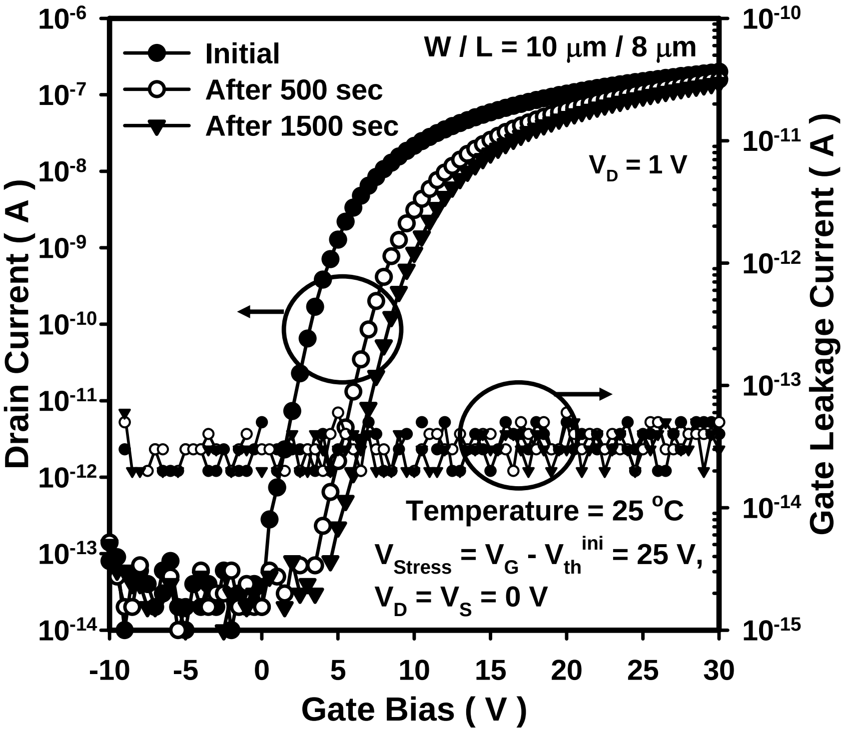


Fig. 6-4 Transfer characteristics of the bottom-gate a-Si:H TFT before and after applying 500 sec and 15000 sec gate-bias stress transfer characteristics at 25 °C substrate temperature. Gate leakage current keeps as low as 10^{-13} A.

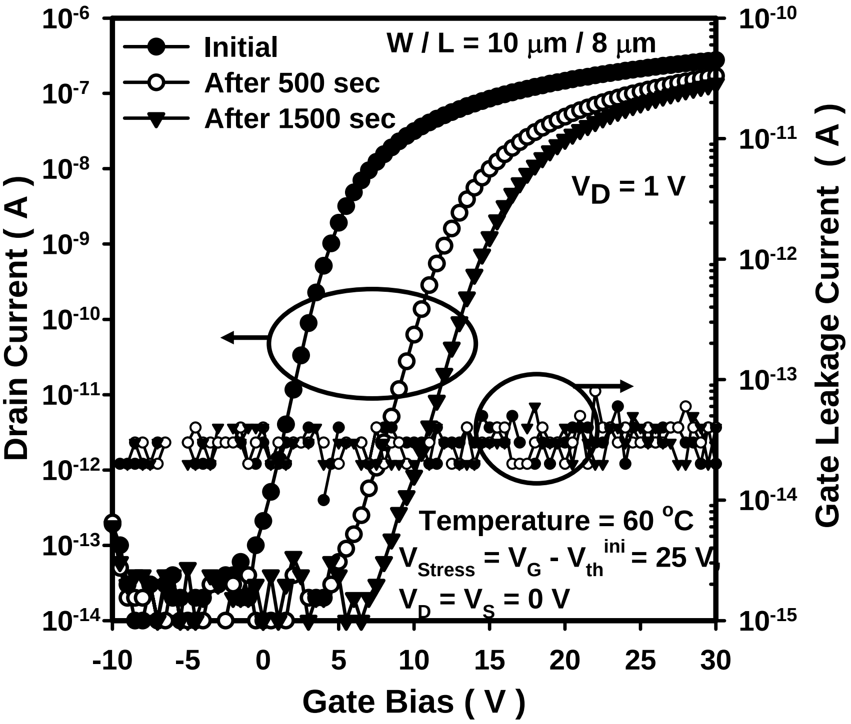


Fig. 6-5 Transfer characteristics of the bottom-gate a-Si:H TFT before and after applying 500 sec and 15000 sec gate-bias stress at 60 °C substrate temperature. Gate leakage current keeps as low as 10^{-13} A.

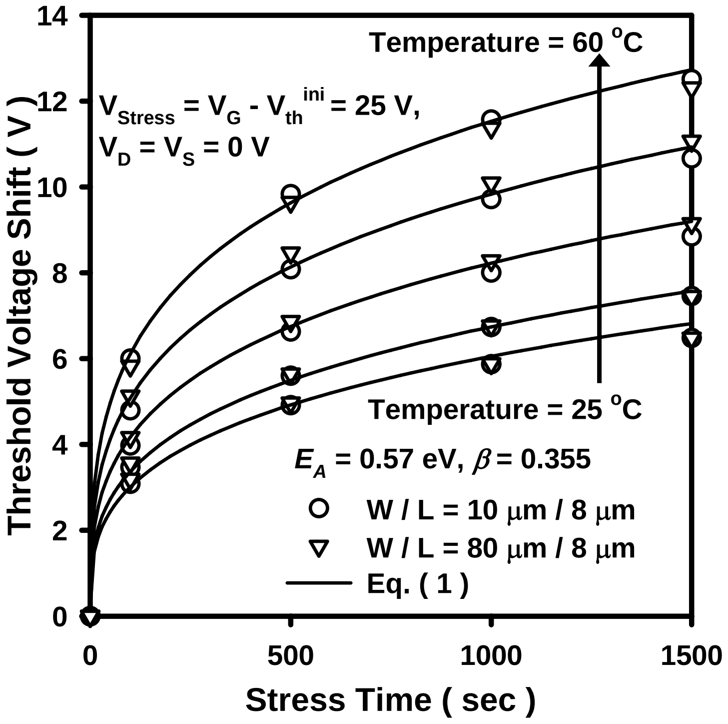


Fig. 6-6 ΔV_{th} as a function of stress time at 25°C, 30°C, 40°C, 50°C and 60°C when $V_{Stress} = V_G - V_{th}^{ini}$ = 25 V. The experimental data can be well explained by Eq. (1).

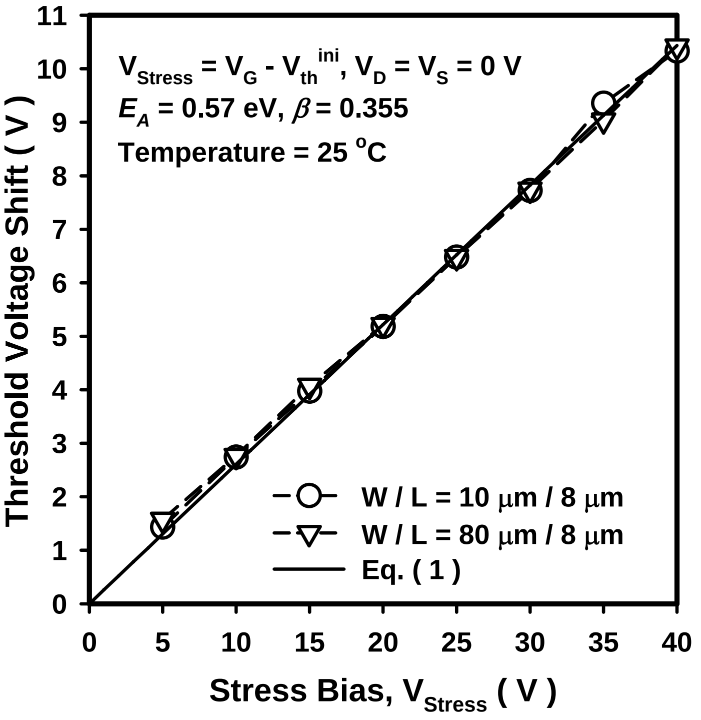


Fig. 6-7 ΔV_{th} under different stress bias V_{Stress} after 1500 sec at 25°C is plotted as a function of V_{Stress}. The experimental data can be well explained by Eq. (1).

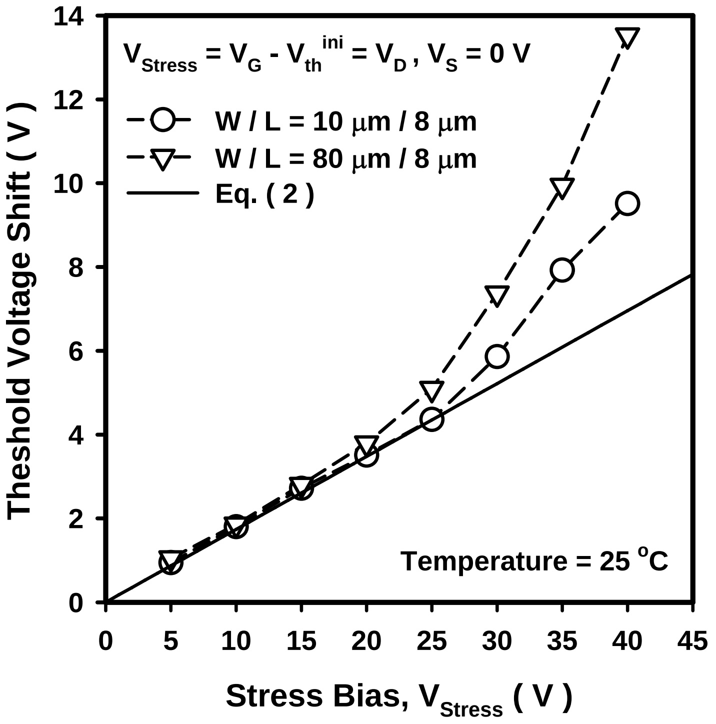


Fig. 6-8 ΔV_{th} as a function of stress bias where $V_{Stress} = V_D = V_G - V_{th}^{ini}$, stress time is 1500 sec and substrate temperature is 25°C

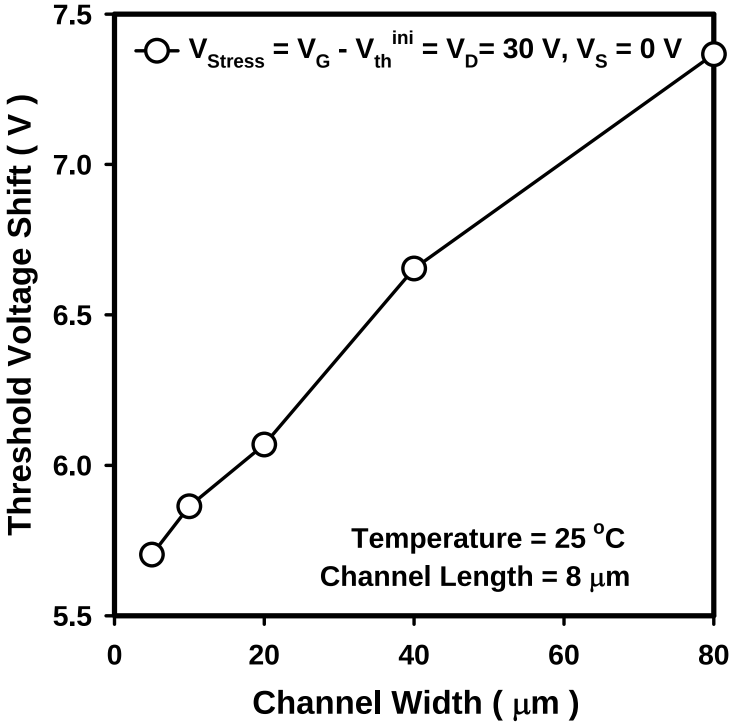


Fig. 6-9 ΔV_{th} is plotted as a function of different channel widths where $V_{Stress} = V_D = V_G - V_{th}^{ini}$, stress time is 1500 sec and substrate temperature is 25°C.

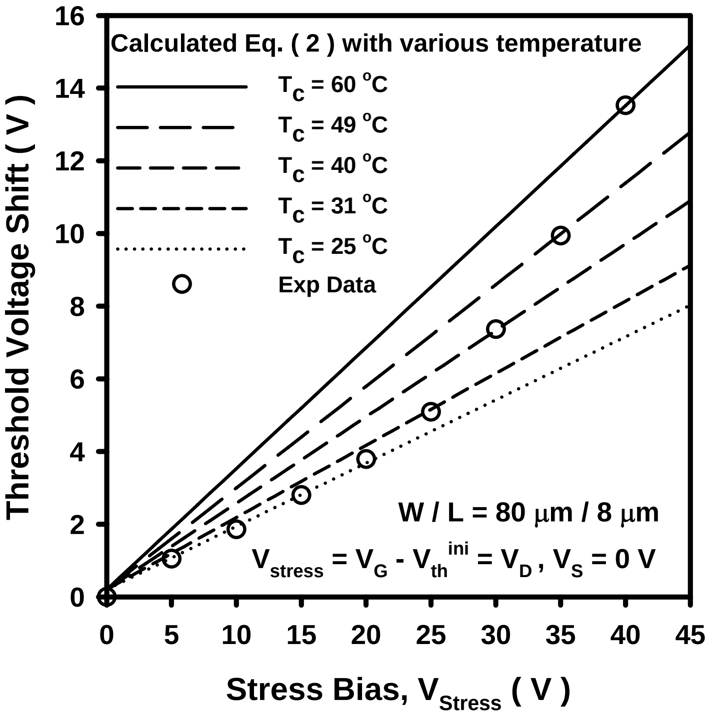


Fig. 6-10 Characteristic temperature (T_{ch}) extraction by fitting the measured ΔV_T with those calculated from Eq. (2). Temperature calculated by the modified self-heating effect model (T_{SHE}) for devices with channel width as 80 μm after 1500-sec stress time is also plotted by triangular symbols. Stress bias $V_{Stress} = V_D = V_G - V_{th}^{ini}$. Channel length is fixed as 8 μm.

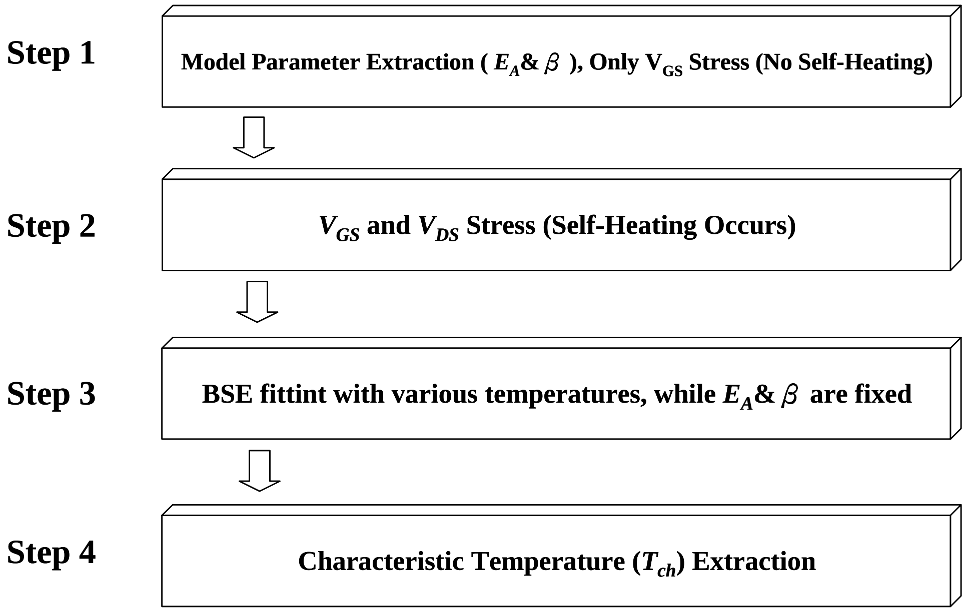


Fig. 6-11 Steps of extracting the channel temperature from the reliability model.

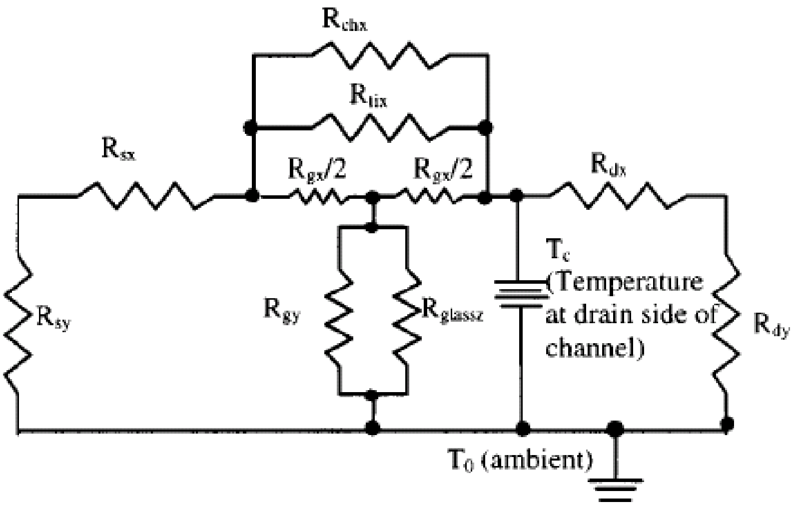


Fig. 6-12 Schematic diagram of the a-Si:H TFT thermal equivalent circuit. T_C is the temperature at the drain side of the channel and T_0 is the temperature of the contact pads, which is assumed to be the ambient temperature of the substrate.

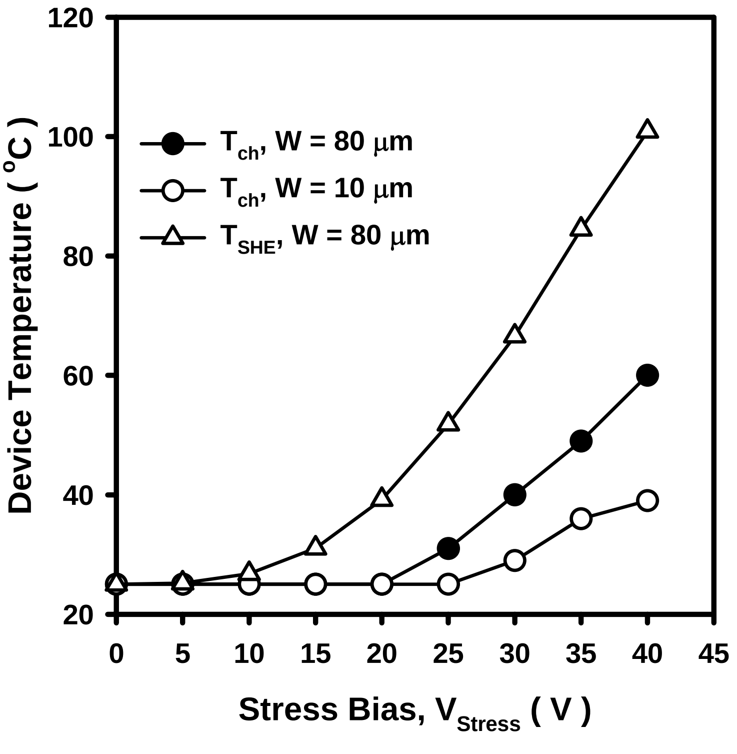


Fig. 6-13 Extracted T_{ch} as a function of stress bias for devices with channel width as 10 μm and 80 μm, respectively. Temperature calculated by the modified self-heating effect model (T_{SHE}) for devices with channel width as 80 μm after 1500-sec stress time is also plotted by triangular symbols. Stress bias $V_{Stress} = V_D = V_G - V_{th}^{ini}$. Channel length is fixed as 8 μm.

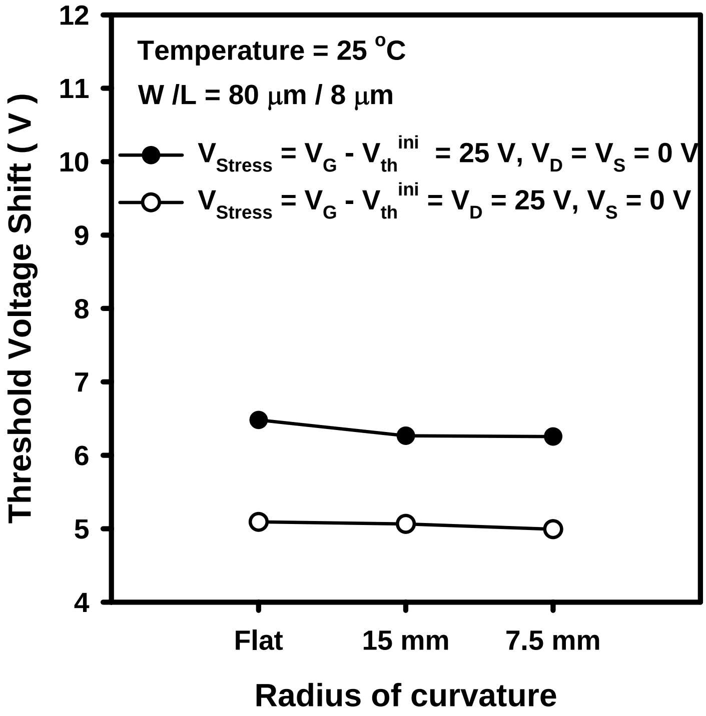


Fig. 6-14 Comparison of ΔV_{th} for wide channel device on flat substrate and on bended substrate when $V_{Stress} = V_D = V_G - V_{th}^{ini} = 25V$ or $V_{Stress} = V_G - V_{th}^{ini} = 25V$.

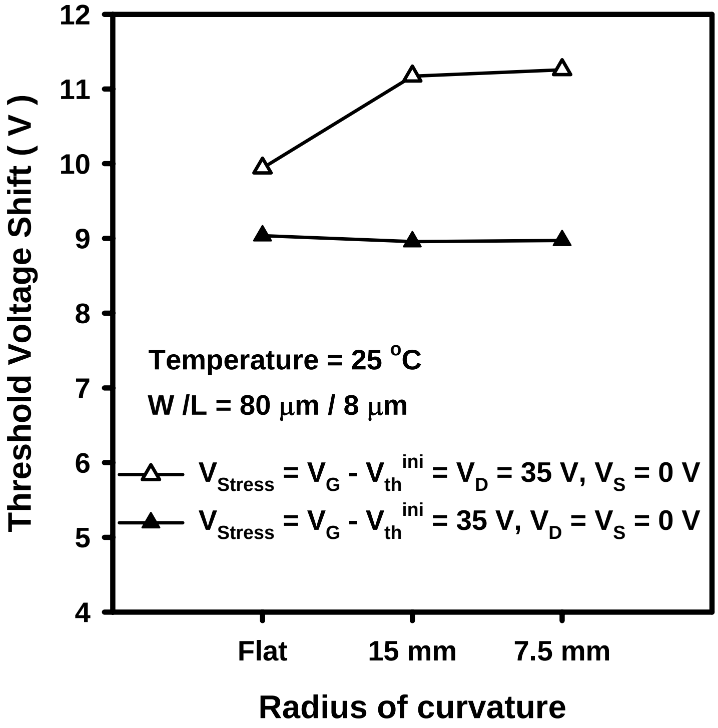


Fig. 6-15 Comparison of ΔV_{th} for wide channel device on flat substrate and on bended substrate when $V_{Stress} = V_D = V_G - V_{th}^{ini} = 35V$ or $V_{Stress} = V_G - V_{th}^{ini} = 35V$.

Chapter 7

CONCLUSION

In this thesis, the reliability issues of low-temperature organic thin film transistor and low-temperature a-Si:H thin film transistor are investigated.

For organic TFTs:

Pentacene thin film is used as the active layer. We discuss the bias stress issues and the light-induced threshold voltage shift of OTFTs. We also investigate the electric field effect of organic phototransistor. Finally, a new sensitive OPT with memory ability and with a large detectable range is proposed.

Bias Stress Effect:

Under steady-state bias stress condition, we firstly investigate the drain bias effect on bias-stress effect (BSE) in pentacene-based OTFTs with SiO_2 dielectric. It is found that the shift of V_{th} is proportional to the channel charge amount while the channel charge amount is adjusted by drain bias. When using pulse bias to stress OTFTs, the ΔV_{th} of OTFTs under positive and negative pulsed bias stress are studied. Influence of pulse width, relaxing duration, and trap response time on threshold voltage shift is investigated. For negative pulsed bias stress, the pulse width effect on device ΔV_{th} can be well explained by using RC equivalent circuit and simulated with an equation (Eq. (3-4)) derived from state creation mechanism. The RC delay time as 13 μs may be account for hole transit time or hole trapping time. Additionally, trap release effect on ΔV_{th} during base voltage duration were discussed. When increasing base voltage duration from 3 μs to 17.5 ms with fixed peak voltage duration, ΔV_{th} was unchanged. As a result, Eq. (3-4) is sufficiently accurate without considering trap release effect. For positive pulsed bias stress, drastically suppressed ΔV_{th} without pulse width dependence was obtained. Since devices under positive gate bias are operated in off-state, a slow accumulation of electron carriers or a slow response of acceptor-like traps were plausible reasons for the long response time (> 2.5 ms). When devices are stressed by bipolar pulsed bias (with negative bias as peak voltage and positive bias as base voltage), ΔV_{th} was dominated by negative pulsed bias stress. Different positive base voltages only slightly decrease ΔV_{th}.

In further study, we spin-coat Poly(methyl methacrylate) (PMMA) and poly(4-vinyl phenol) (PVP) thin film to modify the surface of SiO_2 gate insulator. For devices with PVP-modified gate insulator, incomplete cross-linking produce hydroxyl (OH) groups on dielectric surface. OH groups cause hysteresis in the transfer characteristic of PVP-OTFT when exposed to the light. Then, under positive gate bias stress, significant negative-charged states appears at pentacene/dielectric interface because OH groups react with moisture to cause electron trapping. When applying positive gate bias to device in vacuum, it is found that light-induced threshold voltage shift is not affected by OH groups. Since light-induced threshold voltage shift (ΔV_{th}^{Light}) is caused by light-induced electron trapping at pentacene/dielectric interface, it is found that electron trapping may have two independent sources. One is from light irradiation, the other is from the reaction between OH groups and moisture.

Photo–Irradiation Effect:

In Ch. 3 and Ch. 5, the light-induce electrons and the photoelectric field effect are discussed. Firstly, it is found that the light-induce electrons can be adjusted by varying the electric field distribution of the device channel. In the further study, it is verified that even when vertical electric field plays a dominant role in enhancing ΔV_{th}^{Light}, the removal of light-induced holes through source/drain electrodes is necessary to allow light-induced electrons to be effectively trapped by interface states as discussion in Ch. 5. When increasing P_L, the maximum ΔV_{th}^{Light} of OPT is restricted owing to the fixed amount of interface trap states under a constant gate bias. Increasing the positive gate bias extends the response window to larger P_L and improves R_{ph} to very weak light. Finally, the repeated OPT response to different P_L is confirmed by applying periodic voltage signal cycle. These results are useful to design OPT in image sensor array. To date, the origin of electron trapping states is not clear. We had measured the devices in vacuum to suppress the influence of oxygen and water. Significant photoelectric field effect was still observed. Further studies need to be conducted to explore the mechanism in depth.

For a-Si:H TFTs on the Polyimide Substrate:

In this study, we measure and analyze a-Si:H TFTs fabricated by Industrial Technology Research Institute, Taiwan. Devices are successfully fabricated on colorless polyimide substrates at low process temperature as 160 °C. With process temperature lower than 160°C, mobility, threshold voltage and subthreshold slope of a-Si:H TFTs are 0.42 cm^2/Vs , 7 volts and 0.77 V/decade, respectively. These parameters of transfer characteristic of low-temperature process device are comparable for the conventional process device. However, low-temperature process still causes more serious reliability issue. There reliability issues have been discussed in the Ch. 6.

Device reliability after bias-temperature stress is investigated. Unchanged gate leakage current as 10^{-13} A indicates that the SiN_x layer fabricated at 160 ℃ is stable. Using gate bias stress and two–terminal bias stress at different temperature on devices with various channel widths, threshold voltage shift (ΔV_{th}) due to charged-state creation is well defined. Moreover, self-heating enhanced ΔV_{th} is firstly observed and investigated. Increasing channel width, drain bias, or substrate temperature enhances self-heating effect. The increased temperature facilitates the generation of defect states and therefore enhances ΔV_{th}. In this study, the thermal the thermal equivalent circuit is used to estimate the variation of the temperature increase induced by self-heating effect when changing glass substrate to polyimide substrate. Additionally, the reliability model is used to calculate the channel temperature. The result verifies that device on the PI substrate has more serious self-heating effect. Influence of substrate curvature on the self-heating enhanced ΔV_{th} is also firstly demonstrated.

Summary

In pentacene-based OTFT experiments, the defect generation process of OTFT is sensitive to ambient light and air. Therefore, the stability of OTFT is needed to over the superior passivation layer. To date, there are many groups to continuously research and develop the suitable material. However, these features can be applied on the sensor field. For light detector application, the pentacene-based phototransistor shows the superior photosensivity. Therefore, the pentacene-based phototransistor has potential to develop low-cost scanner on flexible substrates.

Although the transfer characteristic of a-Si:H TFTs fabricated at 150 ^{o}C process temperature is comparable to that fabricated at 350 ^{o}C, the reliability of device is degraded by lowering the process temperature. Compare with pentacene-based OTFT, a-Si:H TFTs fabricated at 150 ^{o}C process temperature is still more stable in ambient air. In Ch. 6, the self-heating effect is observed in the a-Si:H TFTs and it is also found that the low thermal conductivity of polyimide substrate enhances the self-heating effect. However, the relative self-heating effect is never observed in OTFTs and this part needs more experiments to study.

Appendix

REILABILITY MODEL

In twenty years ago, the reliability model of amorphous silicon thin film transistors had been studied. W. B. Jackson *et al.* (Phys. Rev. B, vol.39 p.1164, 1989) had described the defect creation by using the stretched-exponential behavior in detail. The change of the defect density from equilibrium, ΔN_s, is given by

$$\frac{d\Delta N_s}{dt} = -AD(t)\Delta N_s \tag{1}$$

where A is a constant of proportionality, and $D(t)$ is the time-dependent hydrogen diffusion coefficient. The time dependence is due to the trapping and detrapping of the hydrogen with an anomalously wide range of dwell times as it diffuses through the network. In the theory of multiple trapping for trap-limited band transport in approximately exponential distribution of trap energies, the dispersive diffusion coefficient is given by

$$D(t) = D_{00}(\omega t)^{-\alpha} \tag{2}$$

where D_{00} is a microscopic diffusion, ω is a hydrogen attempt frequency, and α is the temperature-dependent dispersion parameter which is given by $\alpha = 1-\beta = 1-T/T_0$. the quantity kT_0 is the characteristic energy of the exponential distribution of trapping sites, and T is the measurement temperature. Solving Eq. (1) using Eq.(2) yields the characteristic stretched exponential

$$\Delta N_s(t)=\Delta N_s(0)\,exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right] \tag{3}$$

Where $\beta = T/T_0$ as before, and

$$\tau=\tau_0\,exp\left(\frac{E_\tau}{kT}\right) \tag{4}$$

where

$$\tau_0 = \frac{1}{\omega} \tag{5}$$

and E_τ is given by

$$E_\tau = kT_0 \, ln\left(\frac{\beta}{A\tau_0 \mathrm{D}_{00}}\right) \tag{6}$$

Equations (3)-(6) relate the time dependence of defect densities to hydrogen diffusion and have a number of importance consequences which can be tested and verified by experiment.

In the MIS structure, the carrier density and hence the induced defect density depends on the distance x form the insulator. Inserting the x dependence explicitly, Eq.(1) becomes

$$\frac{\mathrm{d}\Delta N_S(x,t)}{dt} = -AD(t)\Delta N_S(x,t) \tag{7}$$

Equation (8) can be integrated over x through the thickness of the film. Defining ΔNs according to the relation

$$\Delta N_{\mathrm{S}} = \Delta N_{\mathrm{S}}(t) \equiv \int_0^\infty N_S(0) exp\left[-\left(\frac{t}{\tau}\right)^\beta\right] \tag{8}$$

It becomes an areal charge density. In the rest of the paper, N_s, ΔN_s and n_{BT} (the density of band-tail carriers) refer to areal charge densities defined in a manner si,ilar to Eq.(8). Equation (1) and all other equations in the paper hold for these areal chare densities. Accordingly, the time dependence of areal defect densities in amorphous silicon should follow a stretched exponential behavior indicated in Eq.(3). Since the threshold-voltage shift, $\Delta V_{th} = V_{th}(\mathrm{t}) - V_{th}(\infty) = \Delta N_s/C_i$, where $V_{th}(0)$ is the threshold voltage in the virgin state, $V_{th}(\infty)$ is the threshold voltage when equilibrium has been reached at $t \to \infty$, C_i is the insulator capacitance per unit area, the time dependence of the threshold voltage shift is given by

$$\frac{V_{th}(t)-V_{th}(\infty)}{V_{th}(0)-V_{th}(\infty)}=\frac{\Delta N_s(t)}{\Delta N_s(0)}=exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right] \tag{9}$$

According to Eq.(9), the threshold-voltage shift should exhibit stretched exponential behavior with t given by Eq.(4) and $\beta = T/T_0$. Eq.(9) can be transformed to a typical stretched exponential function.

$$V_{th}(t)-V_{th}(\infty)=\left(V_{th}(0)-V_{th}(\infty)\right)exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]$$

$$V_{th}(t)=V_{th}(\infty)+\left(V_{th}(0)-V_{th}(\infty)\right)exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]$$

$$V_{th}(t)-V_{th}(0)=\left(V_{th}(\infty)-V_{th}(0)\right)-\left(V_{th}(\infty)-V_{th}(0)\right)exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]$$

$$V_{th}(t)-V_{th}(0)=\left(V_{th}(\infty)-V_{th}(0)\right)\left\{1-exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]\right\} \tag{10}$$

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Bias-Stress Effect and Photo-Irradiation Effects in Organic and a-Si:H Thin Film Transistors

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