A Monolithic CMOS Autocompensated Sensor Transducer for Capacitive Measuring Systems

Cheng-Ta Chiang, *Member, IEEE*, Chi-Shen Wang, and Yu-Chung Huang

***Abstract*—In this paper, a monolithic complimentary metal–oxide–semiconductor (CMOS) autocompensated sensor transducer for capacitive measuring systems is newly presented. The proposed converter is compact and robust to integrate in capacitive measuring systems. The proposed autocompensated sensor transducer is attractive due to the fact that a digitized signal is produced without realizing the analog-to-digital converter. Hence, the hardware cost could be reduced. Furthermore, the output signal of the proposed transducer is a pulse stream; it could be easily sent over a wide range of transmission media, such as package switch networks (PSNs), radios, and optical, infrared (IR), and ultrasonic media. Another innovation is that the proposed automatic compensation circuits enhance and compensate the linear relation between the variable capacitance of the detected sensor and the output digital frequency over a wide dynamic frequency range. Measurement results have successfully verified the functions and the performance of the proposed autocompensated sensor transducer and confirmed that it is possible to apply it to the air pressure sensor. The area of this chip is $940 \times 1080\ \mu m^2$, and the power consumption is 6.4 mW. The proposed transducer is not only suitable for capacitive measuring systems but also practical for application in the front-end systems of the wireless sensor network.**

***Index Terms*—Capacitive sensor, complimentary metal–oxide–semiconductor (CMOS), sensor interface, sensor transducer, signal conditioning.**

I. Introduction

RECENTLY, sensor transducers have been an attractive topic of research for sensor measuring instruments and automotive and medical systems. For example, these transducers have been suitably used in pressure transducers [1], [2], humidity sensing systems [3], [4], etc. To fit the demands of the commercial market on sensor transducers, the proposed autocompensated sensor transducer, which is implemented as a capacitance-to-frequency converter (CFC), has the feature of being low cost. The proposed autocompensated sensor transducer is attractive due to the fact that a digitized signal is produced without realizing the analog-to-digital converter. Thus, the hardware cost could be reduced. Furthermore, the output signal of the proposed transducer is a pulse stream; it could be easily sent over a wide range of transmission media, such as package switch networks, radios, and optical, infrared, and ultrasonic media. Hence, the output signal could easily be received and processed by the receiver terminal, such as the receiver in the systems of a wireless sensor network. Until now, several achievements [5]–[8] had been realized. However, the output frequency of these transducers could not be higher than a 100-kHz frequency band, as listed in Table I. Hence, they are not suitable for present applications, such as demanding a wide dynamic frequency range. To satisfy such sensor requirements, a novel design with digitized compensation circuits is, thus, investigated first [9].

TABLE I
COMPARISONS TO PREVIOUS INTEGRATED SENSOR TRANSDUCERS

	[7]	[8]	This work
Technology	NMOS 5μm	CMOS 4μm	CMOS 0.35μm
Power supply	10 V	±1.5 V	3.2 V
Input Capacitance range	20-50 pF	2-20 pF	4-24 pF
Maximum Frequency range	1.2 kHz	1 kHz	500 kHz
Chip area	2.4 mm^2	1.1 mm^2	1.01 mm^2

In this paper, a monolithic CMOS autocompensated sensor transducer for capacitive measuring systems is newly proposed. The proposed converter is compact and robust for integration into capacitive measuring systems. Based on the 0.35-μm 2P4M CMOS technology with a 3.2-V power supply, all the functions and the performance of the proposed converter are tested and proven through Simulation Program with Integrated Circuit Emphasis (SPICE) simulations. Measurement results have successfully verified the functions and the performance of the proposed autocompensated sensor transducer and confirmed that it is possible to apply them to the air pressure sensor. The output frequency range is from 0.5 to 500 kHz, and the variable capacitance of the detected sensor ranges from 4 to 24 pF. The area of this chip is $940 \times 1080\ \mu m^2$, and the power consumption is 6.4 mW. The proposed transducer is not only suitable for capacitive measuring systems but is also practical for application in the front-end systems of the wireless sensor network.

In Section II, the capacitive sensing principle of the air pressure sensor is addressed. The system architecture and

Manuscript received May 30, 2007; revised November 3, 2007. First published June 10, 2008; current version published October 10, 2008. This work was supported by the National Science Council of Taiwan, R.O.C., under Contract NSC92-2218-E-009-011.

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Digital Object Identifier 10.1109/TIM.2008.925020

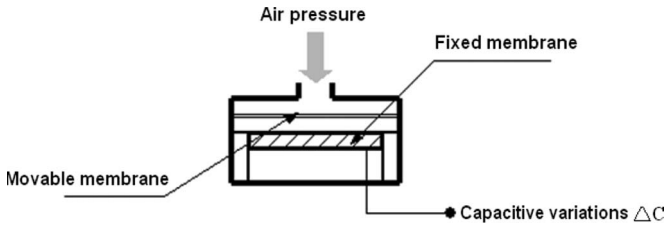


Fig. 1. Structure of the air pressure sensor.

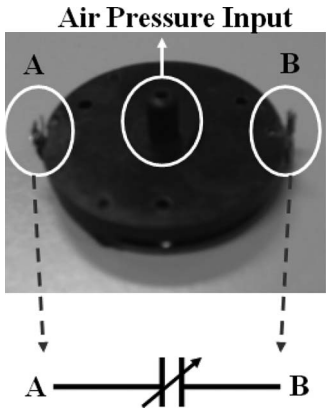


Fig. 2. Physical structure of the air pressure sensor.

simulation results are described in Section III. Section IV displays the measurement results. Last, Section V provides the conclusions and future works.

II. Capacitive Sensing Principle of the Air Pressure Sensor

First, the capacitive sensing principle of the air pressure sensor is addressed. The structure of the air pressure sensor is shown in Fig. 1. The controlled air pressure passes through a channel and pushes the movable membrane. When the movable membrane starts to shift, the distance between the fixed and movable membranes is changed. Thus, the capacitive variations ΔC can be derived as

$$C = \varepsilon \frac{A}{d} \tag{1}$$

$$\Delta C = \frac{A}{d}\Delta\varepsilon - \frac{\varepsilon A}{d^2}\Delta d + \frac{\varepsilon}{d}\Delta A. \tag{2}$$

Combining (1) and (2)

$$\frac{\Delta C}{C} = \frac{\Delta\varepsilon}{\varepsilon} - \frac{\Delta d}{d} + \frac{\Delta A}{A} \tag{3}$$

where ε is the dielectric constant, A is the area of two metal plates, and d is the gap distance. In the air pressure sensor, the parameters of ε and A will not be changed. Thus, the capacitive variations ΔC will be directly affected by the gap distance Δd. By controlling the air pressure, the capacitive variations of the air pressure sensor can be obtained by (3). Fig. 2 shows the physical structure of the air pressure sensor, and the experimental characteristics are measured in Fig. 3. In Section IV, the air pressure sensor will be applied and experimented on within the proposed autocompensated sensor transducer.

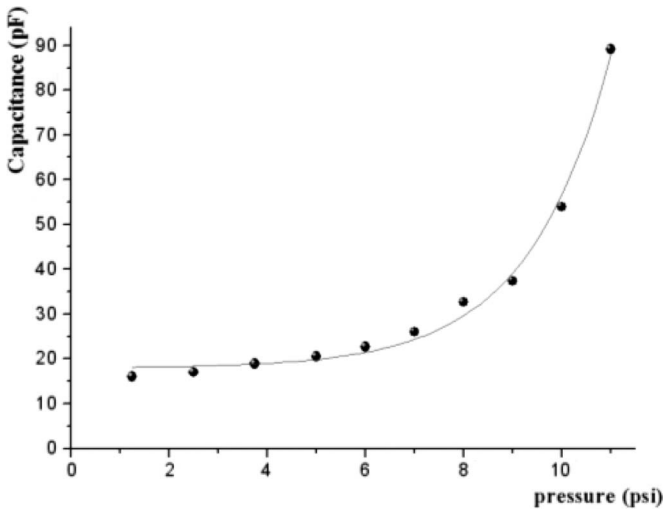


Fig. 3. Experimental characteristic of the air pressure sensor.

III. System Architecture and Simulation Results

Now, the system architecture and circuits are analyzed. Fig. 4 shows the schematic of the proposed autocompensated sensor transducer, which consists of the capacitance-to-voltage converter (CVC), the voltage-to-frequency converter (VFC), and the automatic compensation circuits. By following Section III, the configurations, the operation principles of all the function blocks, and the compensation algorithm of the automatic compensation circuits will be described in detail.

A. CVC

Among the proposed CFC, the CVC needs to be particularly taken care of. That is because this interfacing circuit is first contacted to the detected sensor. Furthermore, the offset voltage of the operational amplifier (OP) and the charge injection error of a switch should be particularly considered. The schematics of the CVC with the OP offset and switch charge injection insensitive properties are shown in Fig. 5. C_x is the capacitor of the detected sensor, and C_R and C_F are the designed capacitors. V_{R1} is the common-mode voltage (1.6 V), and V_{R2} is the reference voltage (2.1 V). The signals ck_1 and ck_2 are two nonoverlapping phase clocks. When the signal ck_2 is logic high, the voltage V_{R2} will charge the capacitor C_x, whereas the capacitor C_F stores the offset voltage of the OP. The MOS M_5 is switched on, and the output voltage is V_{R1}. When the signal ck_1 is logic high, the capacitor C_F is connected to the output. The voltage V_{R2} charges the capacitor C_R. Thus, by following the principle of charge conservation, the output voltage V_o will be derived as follows:

$$\begin{aligned} &C_x(V_{R2} - V_{R1} - V_{os}) + C_R(0 - V_{os}) + C_F(0 - V_{os}) \\ &\quad = C_x(0 - V_{os}) + C_R(V_{R2} - V_{R1} - V_{os}) + C_F(V_o - V_{os}). \end{aligned} \tag{4}$$

Therefore

$$V_o = \frac{C_x - C_R}{C_F}(V_{R2} - V_{R1}). \tag{5}$$

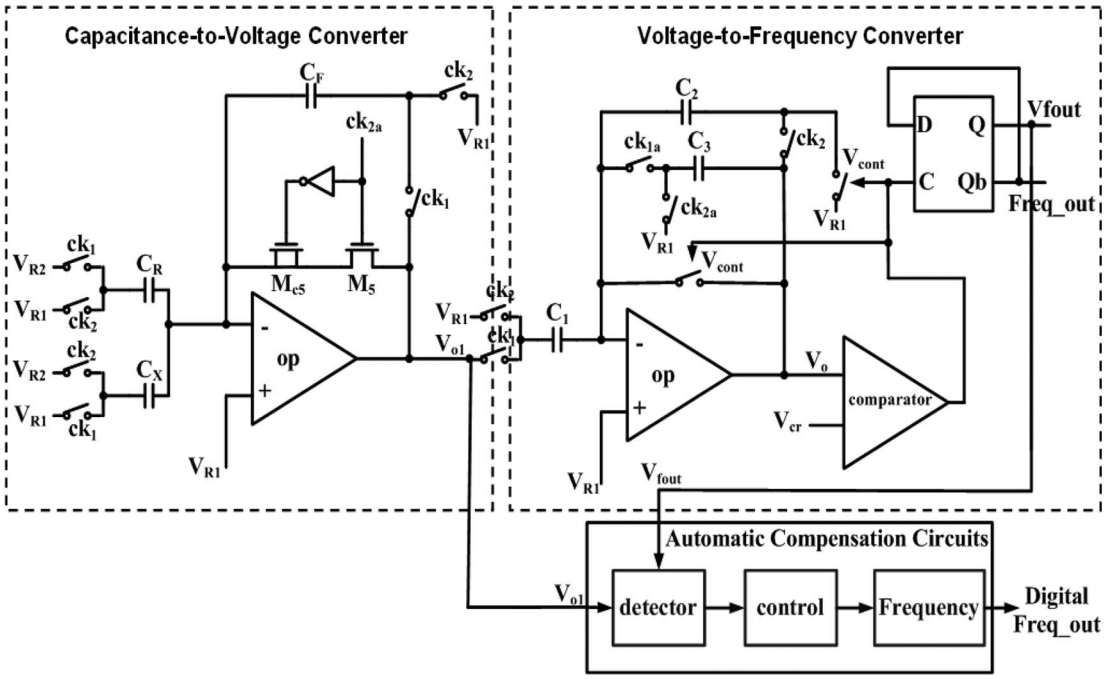


Fig. 4. Schematic of the proposed autocompensated sensor transducer.

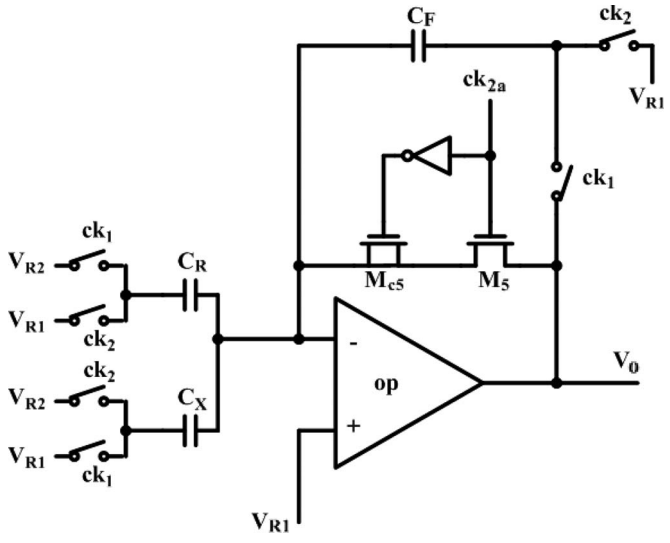


Fig. 5. Schematic of the CVC with the OP offset and switch charge injection insensitive properties.

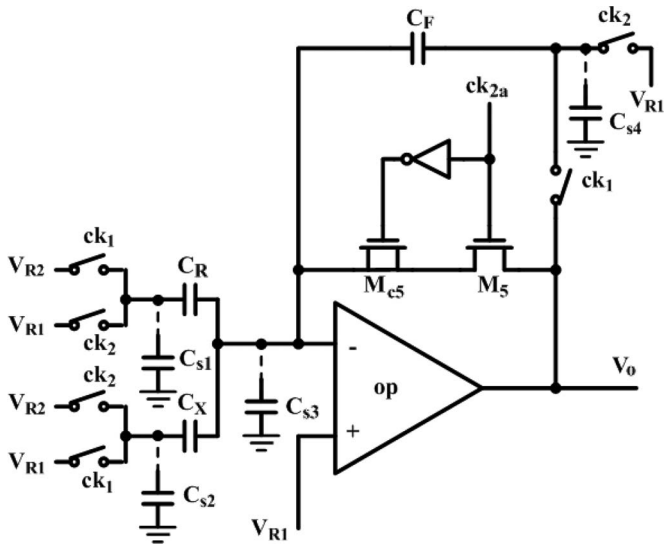


Fig. 6. Schematic of the CVC with parasitic capacitors C_{s1} to C_{s4}.

By following (5), the OP offset can be removed. Thus, the CVC with the OP offset insensitive property is verified. Next, the charge injection error of a switch is to be discussed. The voltage error is generated when the MOS M_5 is turned off. The produced charge injection error ΔV_e that is contributed to the output node will be given as follows:

$$\Delta V_e = \frac{C_{gs5} * V_{ck2a}}{C_F}. \tag{6}$$

To solve this error, the MOS M_{c5} is designed to absorb the charge injection from the MOS M_5. ck_{2a} is the clock signal that is raised slightly before the signal ck_2. When the signal ck_{2a} goes from logic high to logic low, the MOS M_5 will be turned off. When the signal ck_{2a} is from logic high to logic low, the MOS M_{c5} turns on and absorbs the charge from the MOS M_5. Thus, the problem of the charge injection error can be overcome.

Moreover, the OP plays an important role in the converter. Therefore, to discuss the effect of the OP nonideality, the OP specification must be addressed. The setting time and the resolution are all dependent on the OP gain and bandwidth. All the OP considerations are discussed below. At the beginning, the OP gain is derived as

$$C_x(V_{R2} - V_{R1}) = C_x(V_{R1} - \text{OP}_-) + C_R(V_{R2} - \text{OP}_-) + C_F(V_o - \text{OP}_-) \tag{7}$$

$$V_{R1} - \text{OP}_- = \frac{V_o}{A}, \qquad A : \text{Gain}. \tag{8}$$

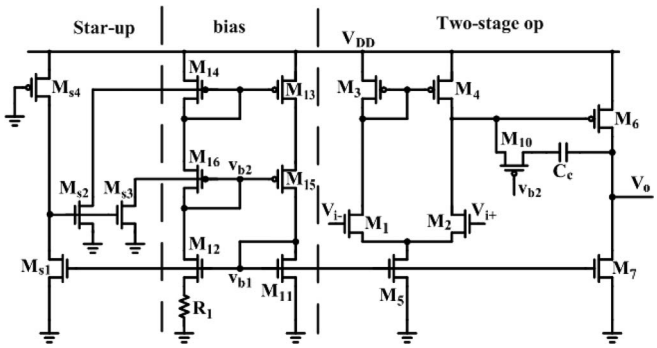


Fig. 7. Schematic of the OP.

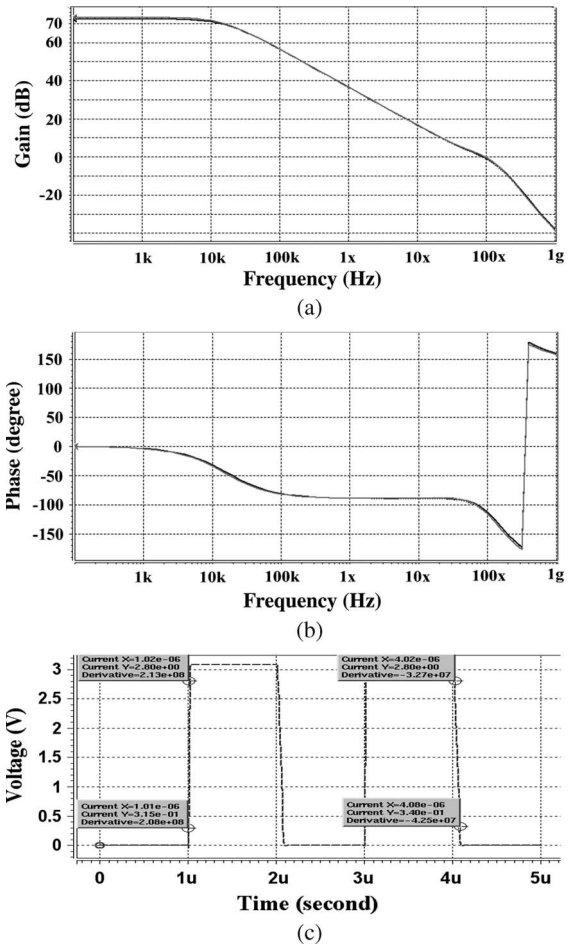


Fig. 8. SPICE simulation results of the OP under frequency sweeping from 0.1 Hz to 1 GHz. (a) Gain. (b) Phase. (c) SR response.

Therefore

$$V_o = \frac{(C_x - C_R)}{C_F}(V_{R2} - V_{R1}) * \left(\frac{1}{1 + \frac{1}{A}\left(\frac{C_F + C_R + C_x}{C_F}\right)} \right)$$
$$= \frac{(C_x - C_R)}{C_F}(V_{R2} - V_{R1}) * \left(1 - \frac{1}{A\left(\frac{C_F}{C_F + C_R + C_x}\right)} \right) \quad (9)$$

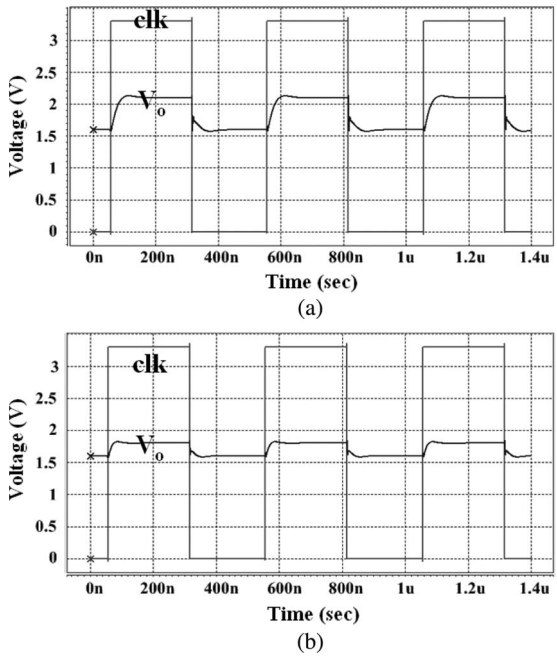


Fig. 9. SPICE output waveforms under the capacitance $C_F = 20$ pF and $C_R = 4$ pF, the voltages $V_{R1} = 1.6$ V and $V_{R2} = 2.1$ V, and the capacitance C_x of (a) 24 pF and (b) 12 pF.

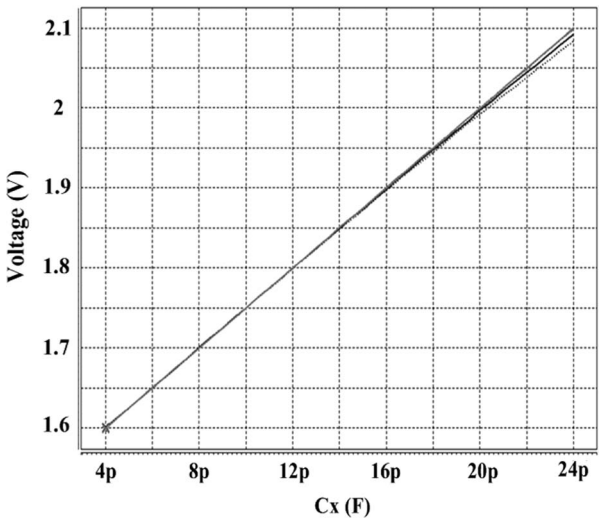


Fig. 10. SPICE simulation results of the CVC under the SPICE design corner (TT, SS, SF, FS, FF).

where the term

$$\frac{\frac{(C_F + C_R)}{C_F}(V_{R2} - V_{R1})}{A\left(\frac{C_F}{C_F + C_R + C_x}\right)}$$

is the voltage error ΔV_o, and $C_F/(C_F + C_R + C_x)$ is the feedback factor β. In the specification, the resolution of the CVC is designed to be 10 bits. Therefore, the voltage error ΔV_o could be given as follows:

$$\frac{V_i}{2^{10}} \geq \left(\frac{C_x - C_R}{C_F}\right)\frac{(V_{R2} - V_{R1})}{A\beta}. \quad (10)$$

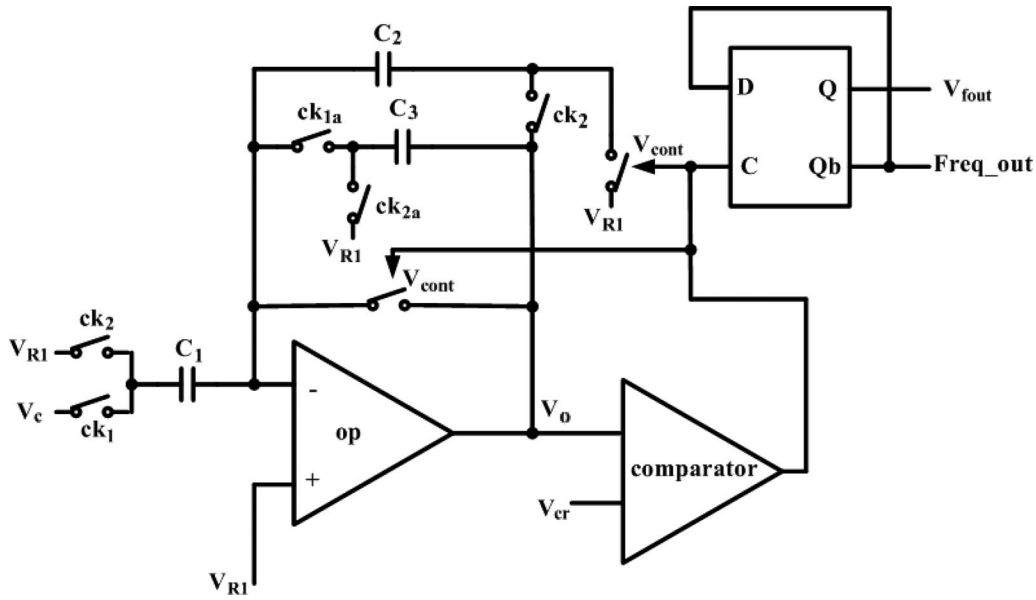


Fig. 11. Schematic of the VFC.

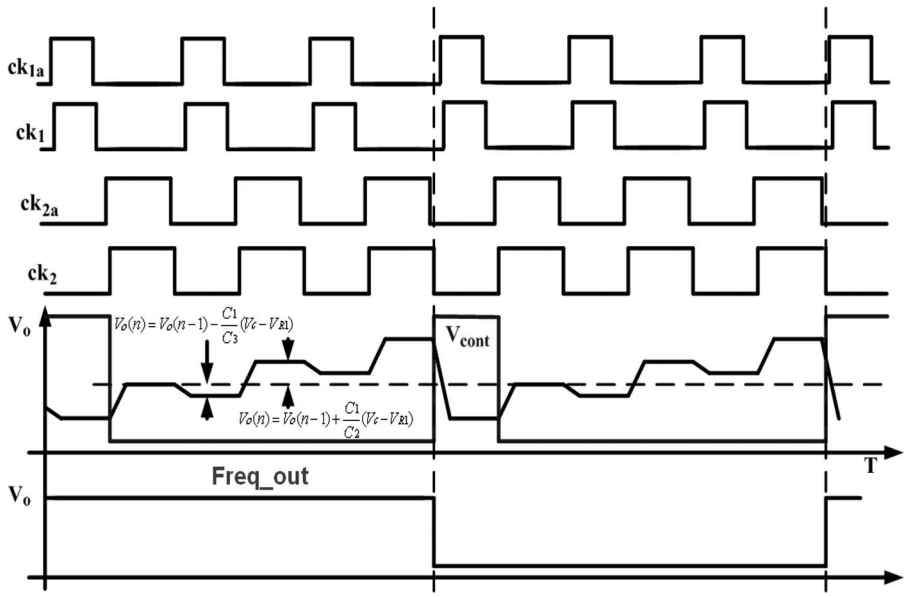


Fig. 12. Timing diagram of the VFC.

Thus, by performing (10), the OP gain should be higher than 67.82 dB. Next, considering the bandwidth, the time constant is given by

$$\tau = \frac{1}{\beta * W_t} = \frac{1}{2\pi\beta * f_t}. \tag{11}$$

To reserve the time for settling the circuit, the settling time T_{set} is designed in the three-fourths clock period. Therefore, the settling time T_{set} is given by

$$T_{\text{set}} = \frac{3}{4} \cdot \frac{1}{2} T_c \approx 180 \text{ ns} \tag{12}$$

where the system clock period T_c is 500 ns. The voltage error needs to be less than 1 least significant bit. Therefore

$$\varepsilon = (V_{R2} - V_{R1}) \cdot e^{-T_{\text{set}}/\tau} \leq \frac{V_i}{2^{10}}. \tag{13}$$

Thus, by performing (13), the minimum unit-gain bandwidth f_t is 15.3 MHz. Last, the consideration of the slew rate (SR) is given by

$$\text{SR} = \frac{I}{C_L} = \frac{V_{p\text{-}p}}{\frac{1}{4} * \frac{1}{2} * T_c}$$
$$V_{p\text{-}p} = 0.5 \text{ V}. \tag{14}$$

By performing (14), the SR should be larger than 8 V/μs. However, the parasitic capacitance of the detected capacitor C_x

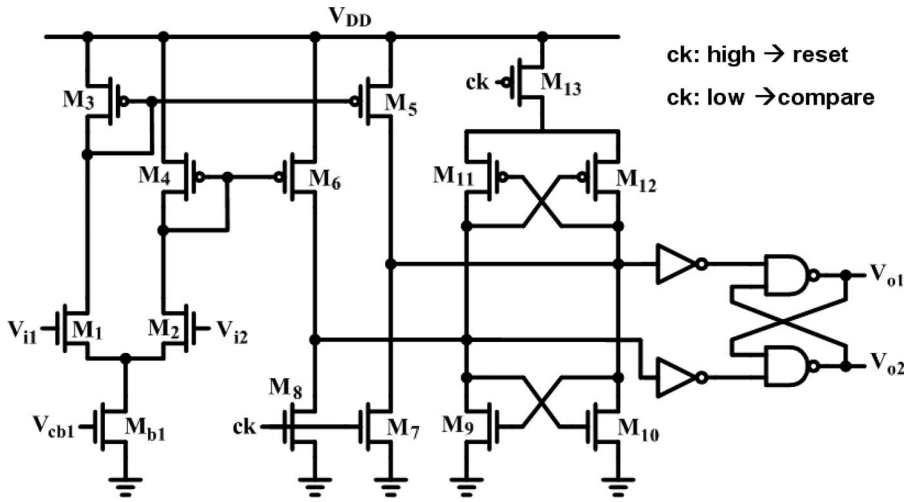


Fig. 13. Schematic of the comparator.

should be also considered. In Fig. 6, the parasitic capacitors C_{s1}, C_{s2}, and C_{s4} are connected to fixed biases; thus, they will not affect the charge transfer of the CVC. However, the parasitic capacitor C_{s3} in the negative input node of the OP will affect the charge transfer of the CVC. Let the parasitic capacitance of C_{s3} be equal to 5 pF. Therefore, (7) should be modified as follows:

$$C_x(V_{R2}-V_{R1})+C_{s3}V_{R1}=C_x(V_{R1}-\mathrm{OP}_-) +C_R(V_{R2}-\mathrm{OP}_-)+C_F(V_o-\mathrm{OP}_-)+C_{s3}\mathrm{OP}_-. \quad (15)$$

Therefore

$$V_o=\frac{(C_x-C_R)}{C_F}(V_{R2}-V_{R1})*\left(1-\frac{1}{A\left(\frac{C_F}{C_F+C_R+C_x+C_{s3}}\right)}\right). \quad (16)$$

By following (9)–(14) mentioned above, the OP gain should be 68.67 dB, and the minimum unit-gain bandwidth f_t is 16.9 MHz. The SR is the same, i.e., 8 V/μs. According to such specifications, the OP is designed and is shown in Fig. 7. The two-stage OP consists of the startup circuit ($M_{s1}-M_{s4}$), the biasing circuit ($M_{11}-M_{16}$), the first-stage amplifier (M_1-M_5), the second-stage amplifier (M_6 and M_7), and the compensation circuit (M_{10} used as a null resistor and a Miller compensation capacitor C_c). The OP under the frequency sweeping from 0.1 Hz to 1 GHz is verified as shown in Fig. 8. The dc gain is 72 dB, the unit gain bandwidth is 95 MHz, and the phase margin is 68°. The positive and negative SRs under the output loading 5 pF are 248.5 and 41 V/μs, respectively. Fig. 9(a) and (b) presents the SPICE output waveforms under the capacitance C_x of 24 and 12 pF, respectively. All the output voltages of the CVC circuit are plotted in Fig. 10. These results are simulated under the SPICE design corner (TT, SS, SF, FS, FF). All these results have rather linear relations between the capacitance and the voltage. These linear relations are obtained by considering the OP offset and switch charge injection insensitive properties. The SPICE simulation results and the characteristic of the CVC circuit are successfully verified and matched each other.

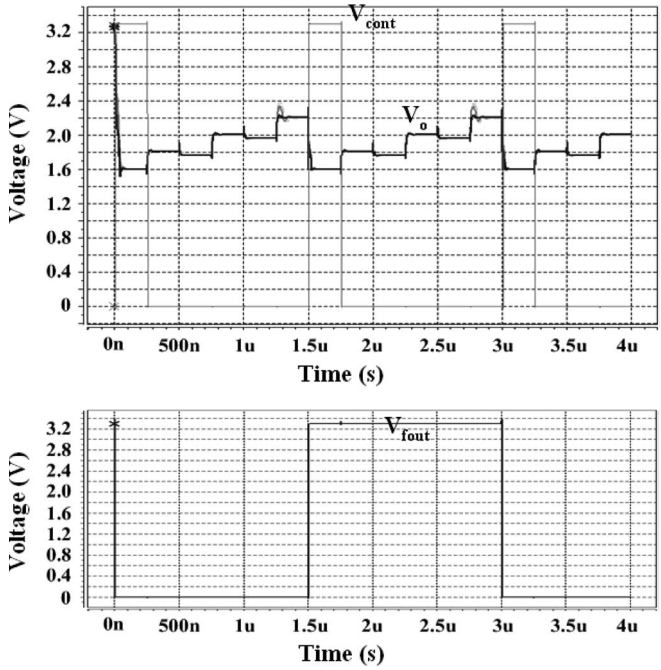


Fig. 14. SPICE output waveforms of the voltages V_{cont}, V_o, and V_{fout} under the capacitance $C_F = 20$ pF, $C_R = 4$ pF, $C_1 = 1.5$ pF, $C_2 = 3$ pF, and $C_3 = 15$ pF, the voltages $V_{R1} = 1.6$ V and $V_{R2} = 2.1$ V, and the capacitance $C_x = 20$ pF.

B. VFC

The schematic of the VFC is shown in Fig. 11. It consists of the switch-capacitor integrator, a comparator, and a D flip-flop. Following the SC techniques, this circuit applies the charge redistribution method. These circuit operations could be written as follows:

$$V_o(n)=V_o(n-1)+\frac{C_1}{C_2}(V_c-V_{R1}) \text{ when the signal } ck_2 \text{ is high} \quad (17)$$

$$V_o(n)=V_o(n-1)-\frac{C_1}{C_3}(V_c-V_{R1}) \text{ when the signal } ck_1 \text{ is high} \quad (18)$$

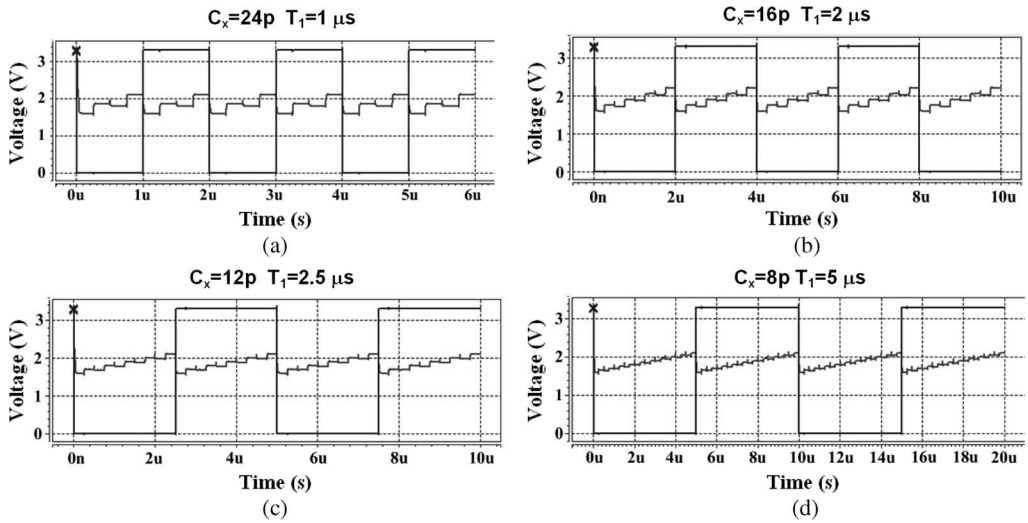


Fig. 15. SPICE output waveforms of the time period $T_1 = 1$, 2, 2.5, and 5 μs under the capacitance C_x of (a) 24 pF, (b) 16 pF, (c) 12 pF, and (d) 8 pF.

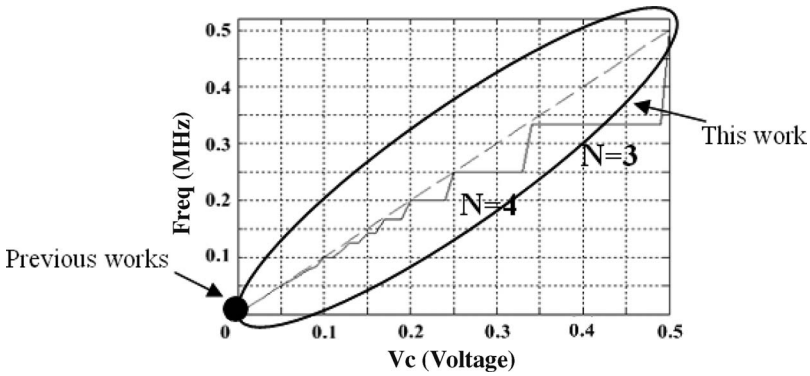


Fig. 16. Relation between the voltage and the frequency of the VFC (without automatic compensation circuits).

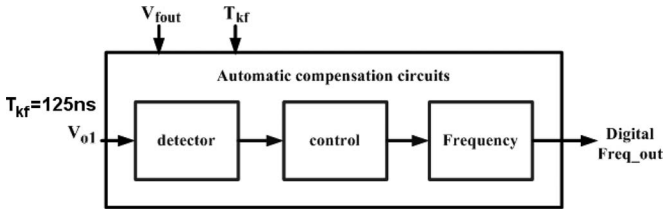


Fig. 17. Block diagram of the automatic compensation circuits.

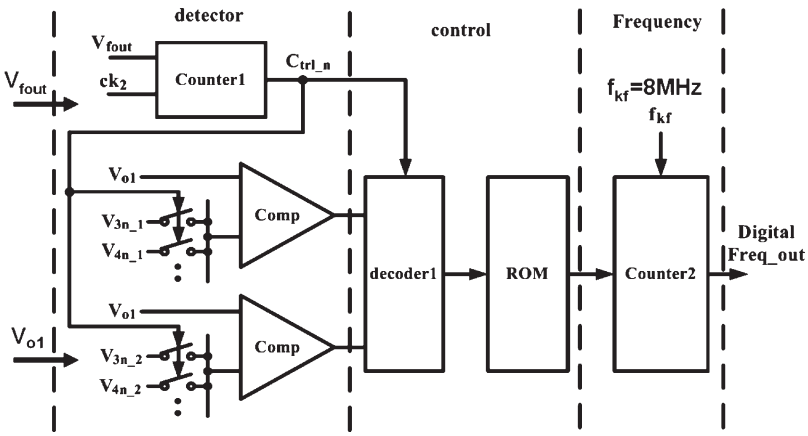


Fig. 18. Schematic of the automatic compensation circuits.

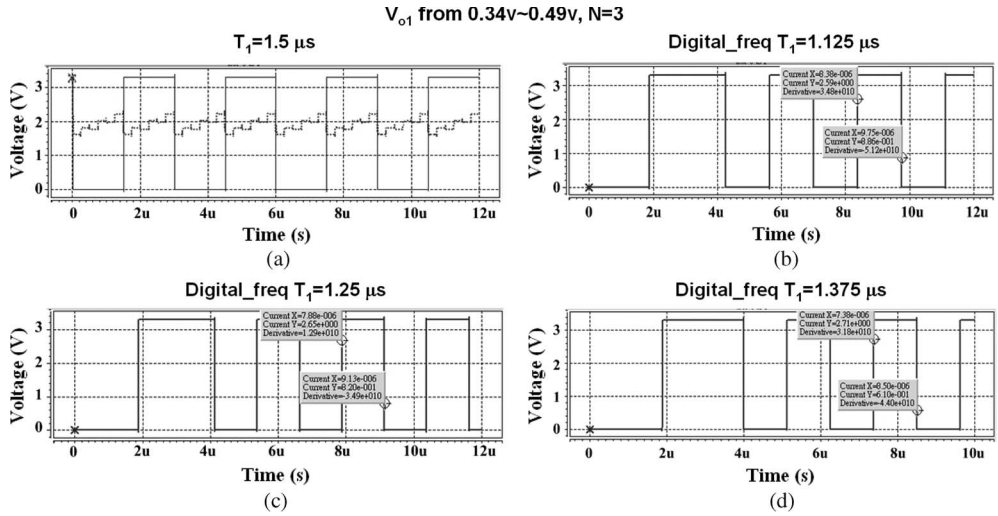


Fig. 19. SPICE output waveforms of the automatic compensation circuits under step number $N = 3$. The time periods T_1 are (a) 1.5 μs, (b) 1.125 μs, (c) 1.25 μs, and (d) 1.375 μs.

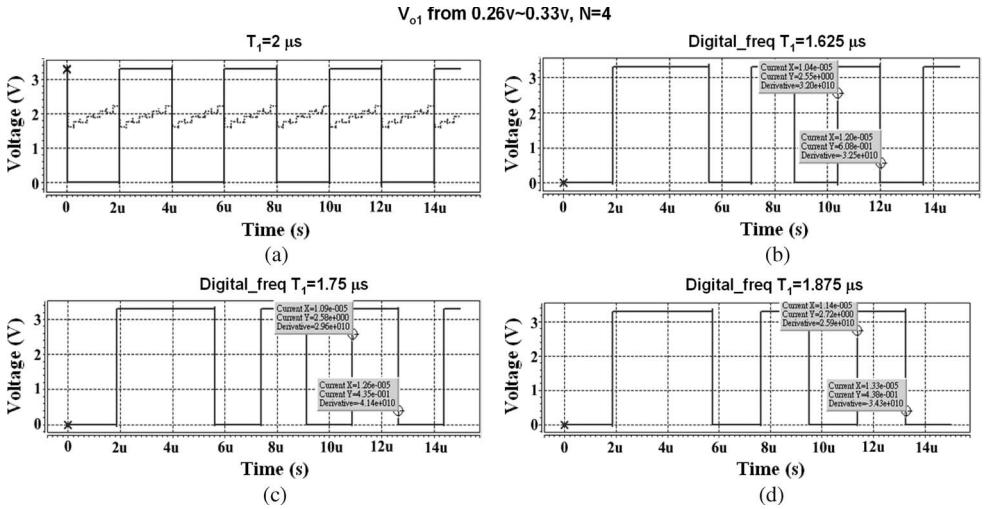


Fig. 20. SPICE output waveforms of the automatic compensation circuits under step number $N = 4$. The time periods T_1 are (a) 2 μs, (b) 1.625 μs, (c) 1.75 μs, and (d) 1.875 μs.

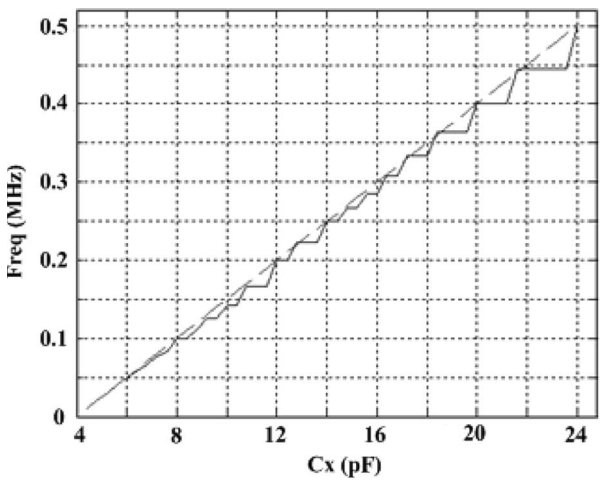


Fig. 21. Relation between the capacitance and the frequency of the proposed autocompensated sensor transducer.

TABLE II
DEVICE PARAMETERS USED ON THE PROPOSED AUTOCOMPENSATED SENSOR TRANSDUCER

C_x	C_R	C_F	C_1	C_2	C_3	f_c	f_{kf}	V_{cr}	F
4~24p	4p	20p	1.5p	3p	15p	2MHz	8MHz	2.1V	0.5~500kHz

where n is defined as the nth cycle of the switch-capacitor integrator, and V_c is the output voltage of the CVC circuit. The capacitor ratio C_1/C_2 is five to ten times the ratio of C_1/C_3. Therefore, the voltage V_o can step up until it exceeds the threshold voltage V_{cr} of the comparator. When the voltage V_o is higher than the voltage V_{cr}, the voltage V_{cont} will go to logic high and reset the voltage V_o. The D flip-flop is also triggered. Moreover, when the voltage V_{cont} is logic high, the capacitor C_2 will store the OP offset voltage and perform the circuit operation of the offset cancellation. All the timing

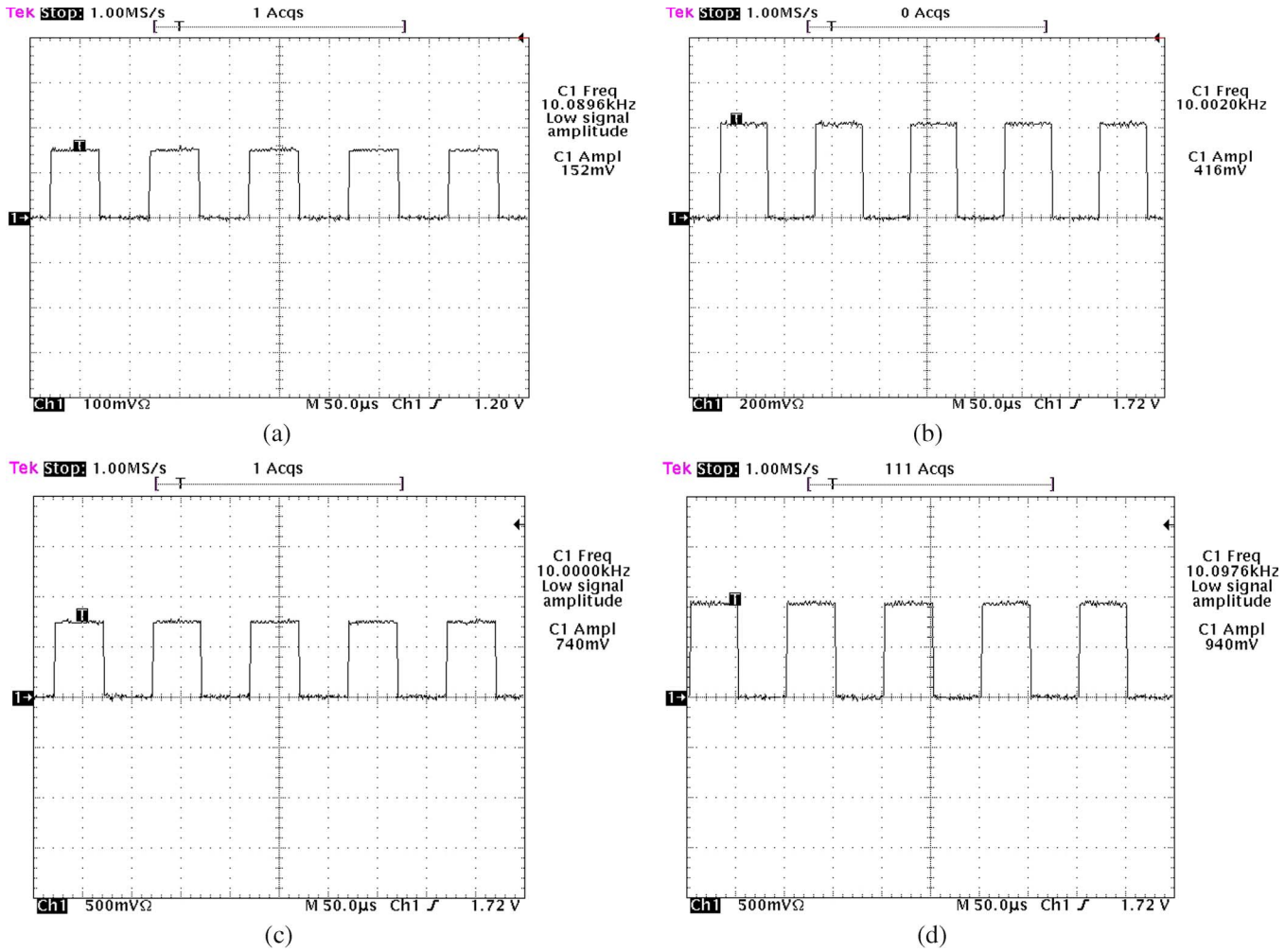


Fig. 22. Measured results of the CVC under the capacitance C_x of (a) 6.8 pF, (b) 12 pF, (c) 18 pF, and (d) 22 pF.

signals discussed above are plotted in Fig. 12. The output frequency F of the VFC circuit is derived as

$$F = \frac{1}{T} = \frac{1}{2T_1} = \frac{1}{2*N*T_c} = \frac{1}{2*\left(\frac{V_{cr}-V_{R1}}{V_c-V_{R1}} * \frac{C_2}{C_1}\right)*T_c} = \frac{1}{2} * \frac{C_1}{C_2}\frac{V_c - V_{R1}}{V_{cr} - V_{R1}} f_c \tag{19}$$

where N is the step number, and f_c is the reciprocal of the system clock period T_c. Hence, combining (5) and (19), the output frequency F could be modified as

$$F = \frac{1}{2} * \frac{C_1}{C_2} * \frac{C_x - C_R}{C_F} * \frac{V_{R2} - V_{R1}}{V_{cr} - V_{R1}} f_c. \tag{20}$$

Fig. 13 shows the schematic of the comparator circuit. When the signal ck goes to logic low, the comparison of the two input differential pairs is performed. The SPICE output waveforms of the voltages V_{cont}, V_o, and V_{fout} are presented in Fig. 14. Last, the output frequency of the VFC circuit is simulated in Fig. 15(a)–(d). In Fig. 15(b), by performing (20), the output time period T_1 should be 5/3 μs. However, it does not match the simulation result of 2 μs. Moreover, the nonlinearity on the high-frequency range is shown in Fig. 16. The reason for this nonlinearity is that the step number N must be an integer

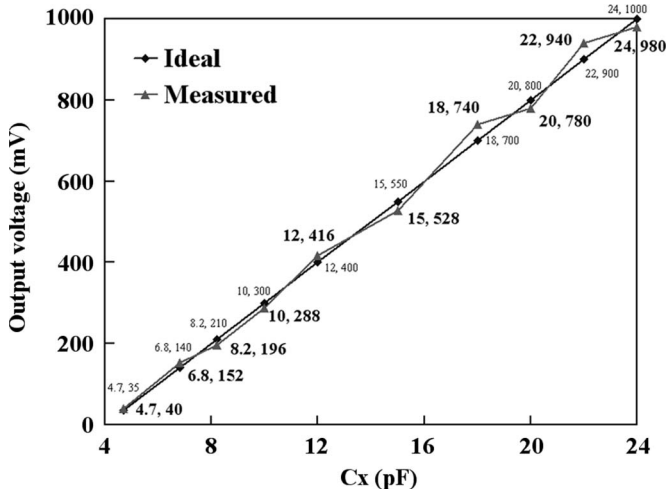


Fig. 23. Measured results of the CVC under the varied capacitance of C_x, which ranges from 4.7 to 24 pF. The boldface-type numbers are the measured values, and the fine-type numbers are the ideal values.

number. Hence, this effect will produce the quantized error. The previous works [5]–[8] do not meet this problem because their frequency band is lower. To solve this problem of obtaining the wide dynamic frequency range, the digitized compensation circuits are, thus, newly investigated [9].

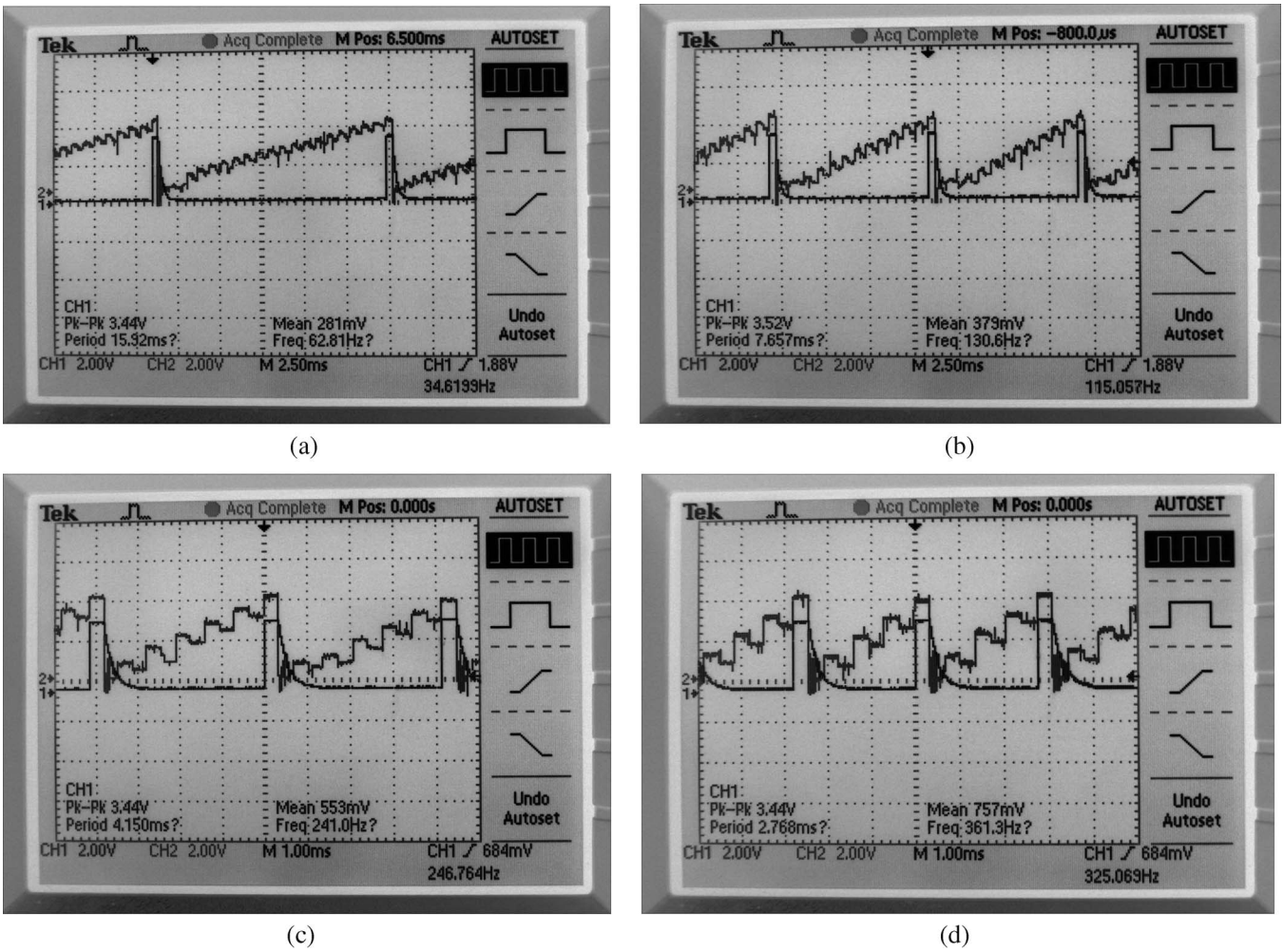


Fig. 24. Measured results of the VFC under the voltage V_c of (a) 0.44 V, (b) 0.74 V, (c) 1.35 V, and (d) 2 V.

C. Automatic Compensation Circuits

In Fig. 17, the nonlinearity is obviously observed on $N = 3$ $(0.34 < V_c < 0.49$ V) and $N = 4$ $(0.25 < V_c < 0.34$ V). Therefore, to obtain a wide dynamic frequency range, the automatic compensation circuits are proposed to compensate the nonlinearity of the VFC on the range of step numbers 3 and 4. The design concept of the automatic compensation circuits is the performance of the interpolation method. In the circuit implementation, the automatic compensation circuits include the detector, control, and frequency circuits, as shown in Fig. 18. Depending on the two voltages V_{font} and V_{o1}, which are the output signals of the VFC and CVC circuits, the detector will decide the step number N. Then, the control circuit will perform the compensation algorithm and send the decision signals to the frequency circuit. Last, the frequency circuit generates the desired compensation frequency and outputs the frequency signal through the digital buffer. The compensation algorithm is performed as follows, where T_{kf} is the sampling period (125 ns), and V_{ref1} and V_{ref2} are the threshold voltages of the comparators. Now, the circuit operations to perform the compensation algorithm are described in Fig. 18. First, in the detector block, counter1 counts and determines the step number N. Then, the control signal C_{trl_n} will be used to turn on the switches, and comparators will use the reference voltages V_{3n_1} and V_{3n_2}, which belonged to $N = 3$, or the reference voltages V_{4n_1} and V_{4n_2}, which belonged to $N = 4$. The outputs of the comparators are thermometer codes. By using these codes, decoder1 can grab the stored data of the ROM in the control block. The stored data in the ROM, which are numbers 9–15,

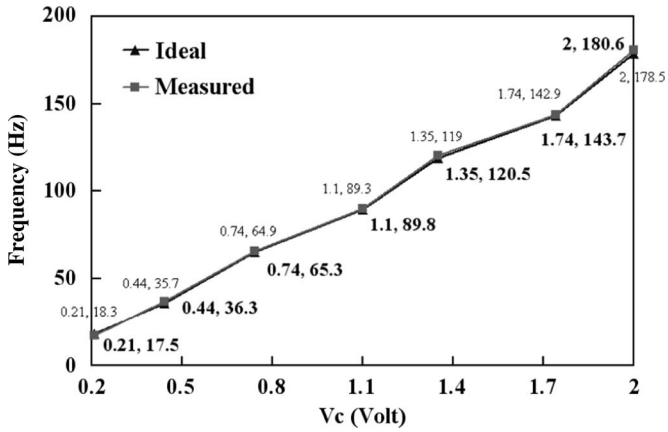


Fig. 25. Measured results of the VFC under the varied voltage V_c, which ranges from 0.21 to 2 V. The boldface-type numbers are the measured values, and the fine-type numbers are the ideal values.

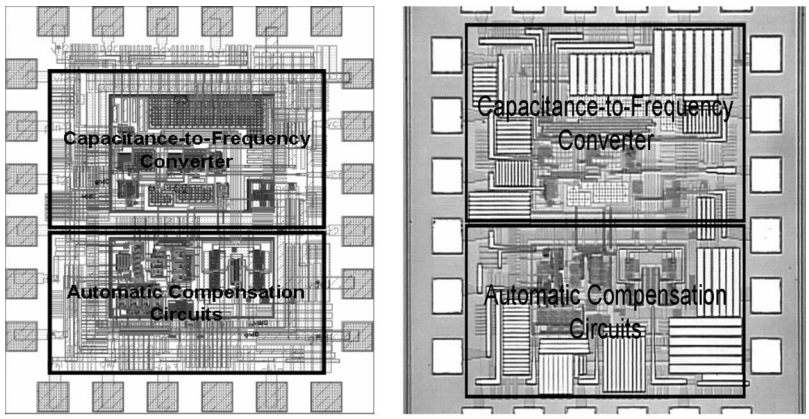


Fig. 26. (a) Physical layout and (b) photograph of the fabricated autocompensated sensor transducer. The area of this implemented chip is $940 \times 1080\ \mu\text{m}^2$.

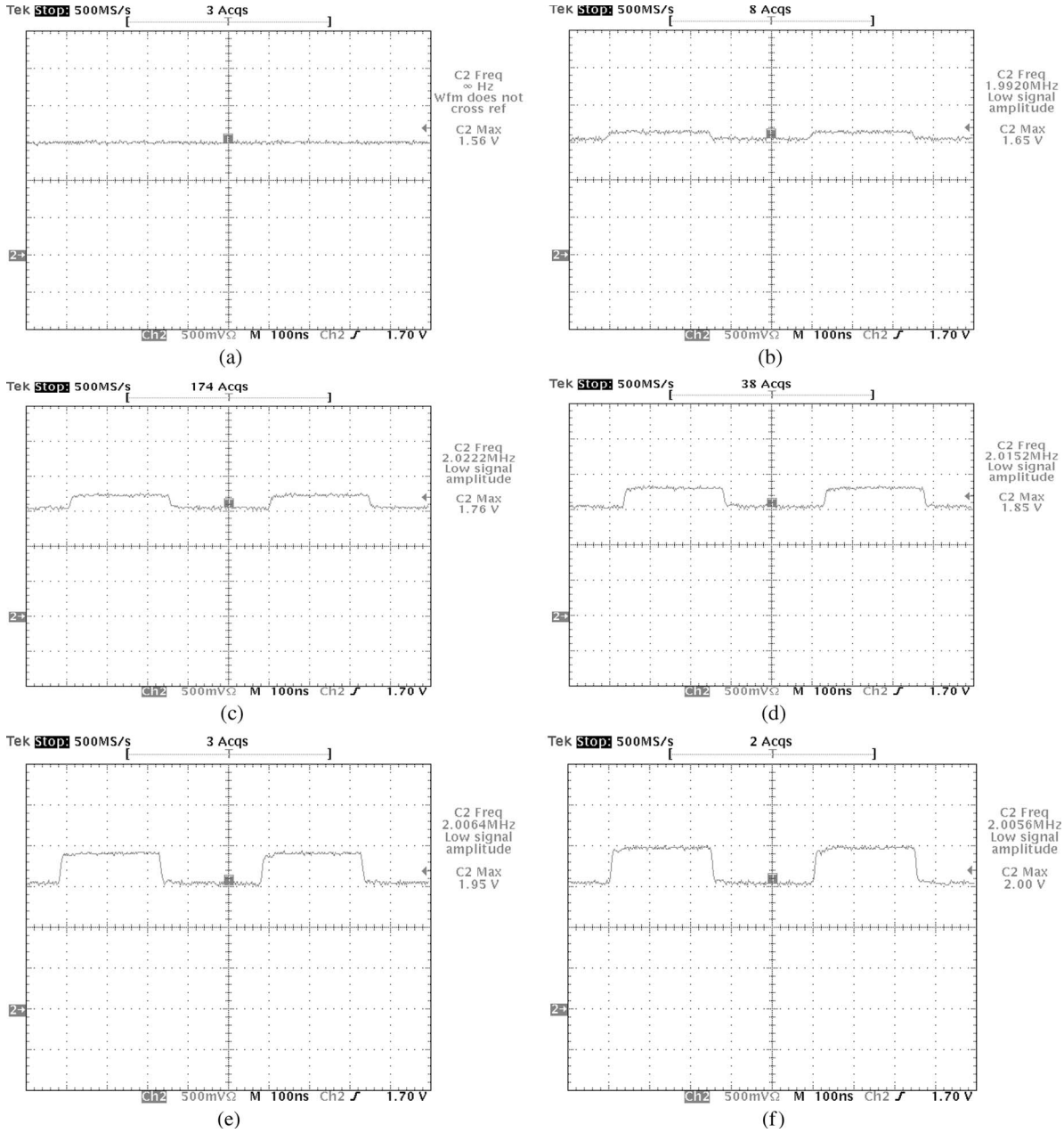


Fig. 27. Measured results of the integrated CVC under the capacitance C_x of (a) 4 pF, (b) 8 pF, (c) 12 pF, (d) 16 pF, (e) 20 pF, and (f) 22 pF.

will be sent to the next block. Last, counter2 will generate the compensated frequency. For example, if step number N is determined to be 3 and the chosen number from the ROM is 10, the output compensated time period T_1 will be 1250 ns. Thus, by performing the automatic compensation algorithm, the nonlinearity of the VFC on the range of step numbers 3 and 4 can be compensated. Last, the wide dynamic frequency range is obtained. Figs. 19 and 20 demonstrate the SPICE output waveforms of the automatic compensation circuits under step numbers 3 and 4, respectively. Fig. 21 shows the linear relation between the capacitance and the frequency of the autocompensated sensor transducer. Obviously, the quantized error has been decreased, and the automatic compensation circuits successfully function as well. Simulation results above have confirmed the correct functions and performance of the proposed autocompensated sensor transducer. All the device parameters that are used on the proposed autocompensated sensor transducer are listed in Table II.

When $N = 3$

if the voltage $V_{o1} > V_{ref1}$, then the compensated time period $T_1 = 9{*}T_{kf}$;
If the voltage $V_{ref1} > V_{o1} > V_{ref2}$, then the compensated time period $T_1 = 10{*}T_{kf}$;
if the voltage $V_{ref2} > V_{o1}$, then the compensated time period $T_1 = 11{*}T_{kf}$.

When $N = 4$

if the voltage $V_{o1} > V_{ref1}$, then the compensated time period $T_1 = 13{*}T_{kf}$;
if the voltage $V_{ref1} > V_{o1} > V_{ref2}$, then the compensated time period $T_1 = 14{*}T_{kf}$;
if the voltage $V_{ref2} > V_{o1}$, then the compensated time period $T_1 = 15{*}T_{kf}$.

IV. Measurement Results

First, the circuits of the CVC and the VFC are built by discrete components to verify circuit operations. The switches, an OP, and a comparator are implemented with analog bilateral switches CD4066, LF411, and LM311, respectively. The capacitance values of C_R, C_F, C_1, C_2, and C_3 are 4, 40, 5, 10, and 45 pF, respectively. The system clock frequency f_c is 1.45 kHz, and the reference voltages V_{R1}, V_{R2}, and V_{cr} are 0, 2, and 4 V, respectively. First, by performing the circuit operation of the CVC, the measured results are demonstrated in Fig. 22 under the capacitance C_x of 6.8, 12, 18, and 22 pF [for Fig. 22(a)–(d), respectively]. The output voltages are 152, 416, 740, and 940 mV, respectively. All the results are plotted in Fig. 23, and the accuracy is within $\pm 8.57\%$. Fig. 24 shows the measured results of the VFC under the voltage V_c of 0.44, 0.74, 1.35, and 2 V [for Fig. 24(a)–(d), respectively]. Taking Fig. 24(a) as an analysis example, when the voltage V_c is 0.44 V, the step-up voltage is 0.22 V. The voltage V_o, as shown in Fig. 12, will continue to go up until it exceeds the reference voltage V_{cr} of the comparator. The step number N is 20. The time period T_1 is equal to 14 ms $(20{*}0.7$ ms$)$. To verify the time period T_1 in Fig. 24(a), each timescale is 2.5 ms, and the time period between two V_{cont} signals is around five to six timescales. Thus, the time period is about 13.75 ms. This measured result matched the calculation result of 14 ms. By the same way, in Fig. 24(b), the voltage V_c is 0.74 V, and the step-up voltage is 0.37 V. The step number N is 11. The time period T_1 is equal to 7.7 ms $(11{*}0.7$ ms$)$, which matched the measured result of 7.657 ms. The time periods T_1 of Fig. 21(c) and (d) are 4.2 $(6{*}0.7)$ and 2.8 $(4{*}0.7)$ ms, respectively. They are also successfully proven to match the measured results, which are 4.15 and 2.768 ms. All the results are plotted in Fig. 25, and the accuracy is within $\pm 4.37\%$. Thus, all the circuit operations of the CVC and the VFC are successfully verified.

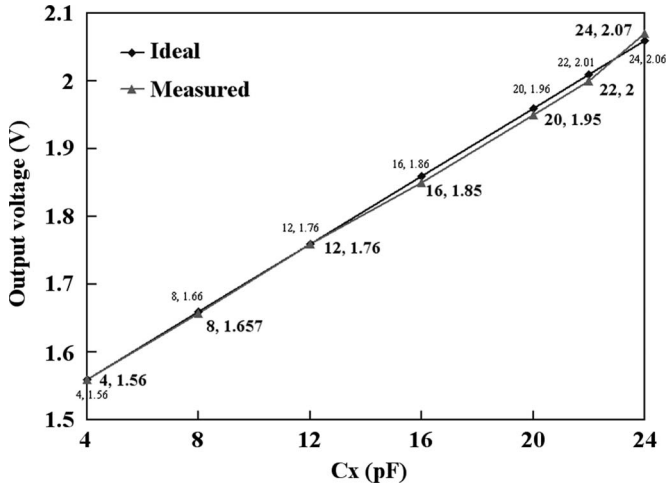


Fig. 28. Measured results of the integrated CVC under the varied capacitance of C_x, which ranges from 4 to 24 pF. The boldface-type numbers are the measured values, and the fine-type numbers are the ideal values.

Last, the monolithic CMOS autocompensated sensor transducer for capacitive measuring systems has been implemented. Fig. 26(a) and (b) demonstrates the physical layout and the photograph of the fabricated autocompensated sensor transducer, respectively. The area of this implemented chip is 940×1080 μm^2, and the power consumption is 6.4 mW. The system clock frequency f_c is 2 MHz, and the reference voltages V_{R1}, V_{R2}, and V_{cr} are 1.6, 2.1, and 2.1 V, respectively. First, by performing the circuit operation of the integrated CVC, the measured results under the capacitance C_x of 4, 8, 12, 16, 20, and 22 pF are demonstrated in Fig. 27(a)–(f), respectively. All the results are plotted in Fig. 28, and the accuracy is within $\pm 3.33\%$. Fig. 29 shows the measured results of the integrated CFC under the capacitance C_x of 6.6, 8, 12, 16, 20, 22, and 24 pF [for Fig. 29(a)–(g), respectively]. As discussed in Section III, the nonlinearity produced by the quantized error on the high-frequency range is also measured and is shown in Fig. 30. However, after performing the automatic compensation circuits, the nonlinearity has been greatly reduced, and the compensated output frequency is shown in Fig. 29(h)–(j). The accuracy is improved and promoted from $\pm 25.77\%$ (without compensation) to $\pm 5.14\%$. Thus, as in Section III, the automatic compensation circuits enhance and compensate the linear relation between the variable capacitance of the detected sensor and the output digital frequency. Last, Fig. 31(a) and (b) displays the measurement setup and the measured results of

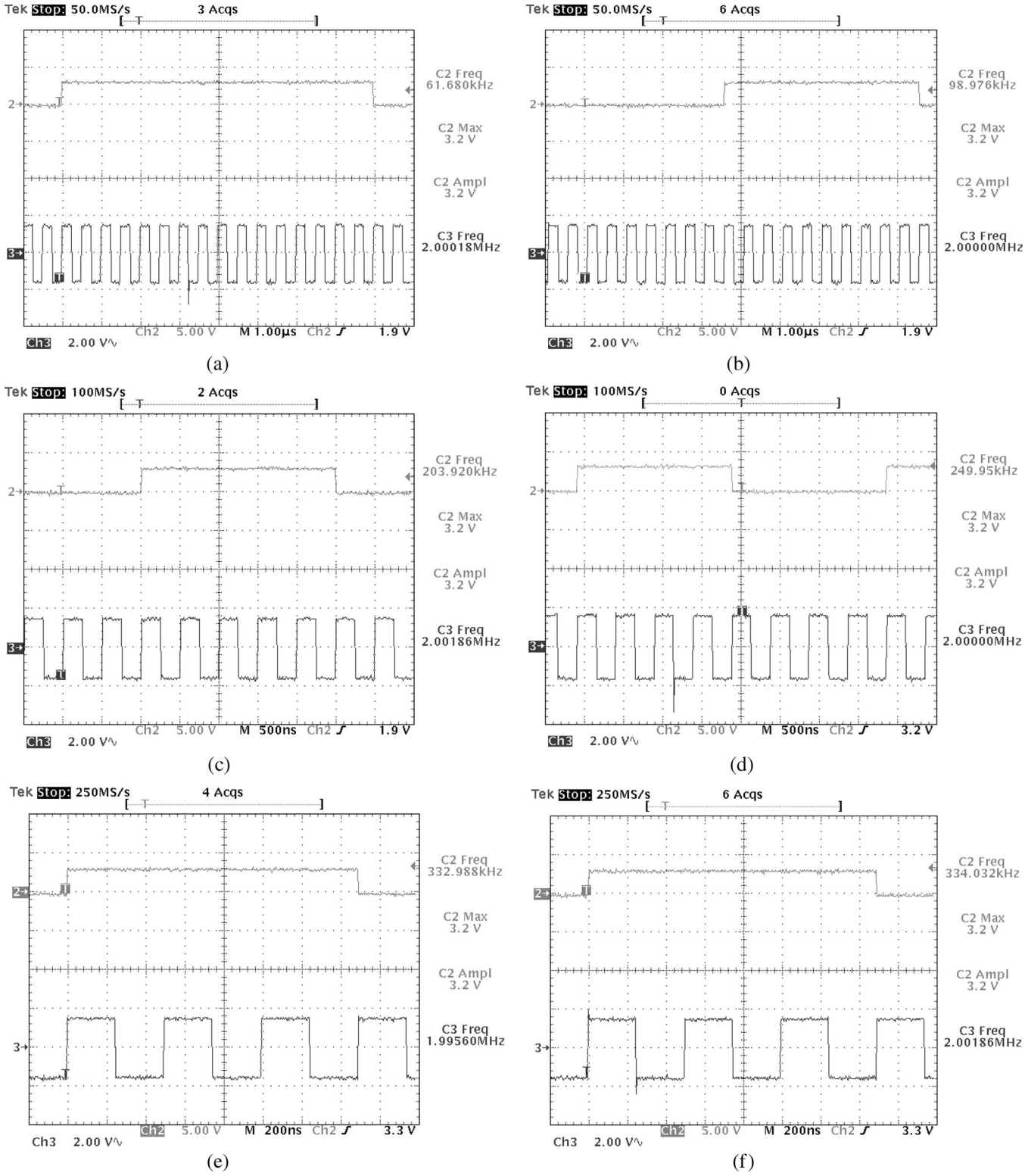


Fig. 29. Measured results of the proposed autocompensated sensor transducer under the capacitance C_x of (a) 6.6 pF, (b) 8 pF, (c) 12 pF, (d) 16 pF, (e) 20 pF, and (f) 22 pF.

the proposed autocompensated sensor transducer applied on the air pressure sensor. The applied scale of the air pressure ranges from 0.5 to 6 lb/in^2. Although some specific applications need the larger operating range of the air pressure, the applied scale of 6 lb/in^2 is still suitable in the wireless microsystem, such as the system specification in [3]. Measurement results have successfully verified the functions and the performance of the proposed autocompensated sensor transducer and confirmed that it is possible to apply it to the air pressure sensor. The characteristics of the proposed autocompensated sensor converter for capacitive measuring systems are summarized in Table III.

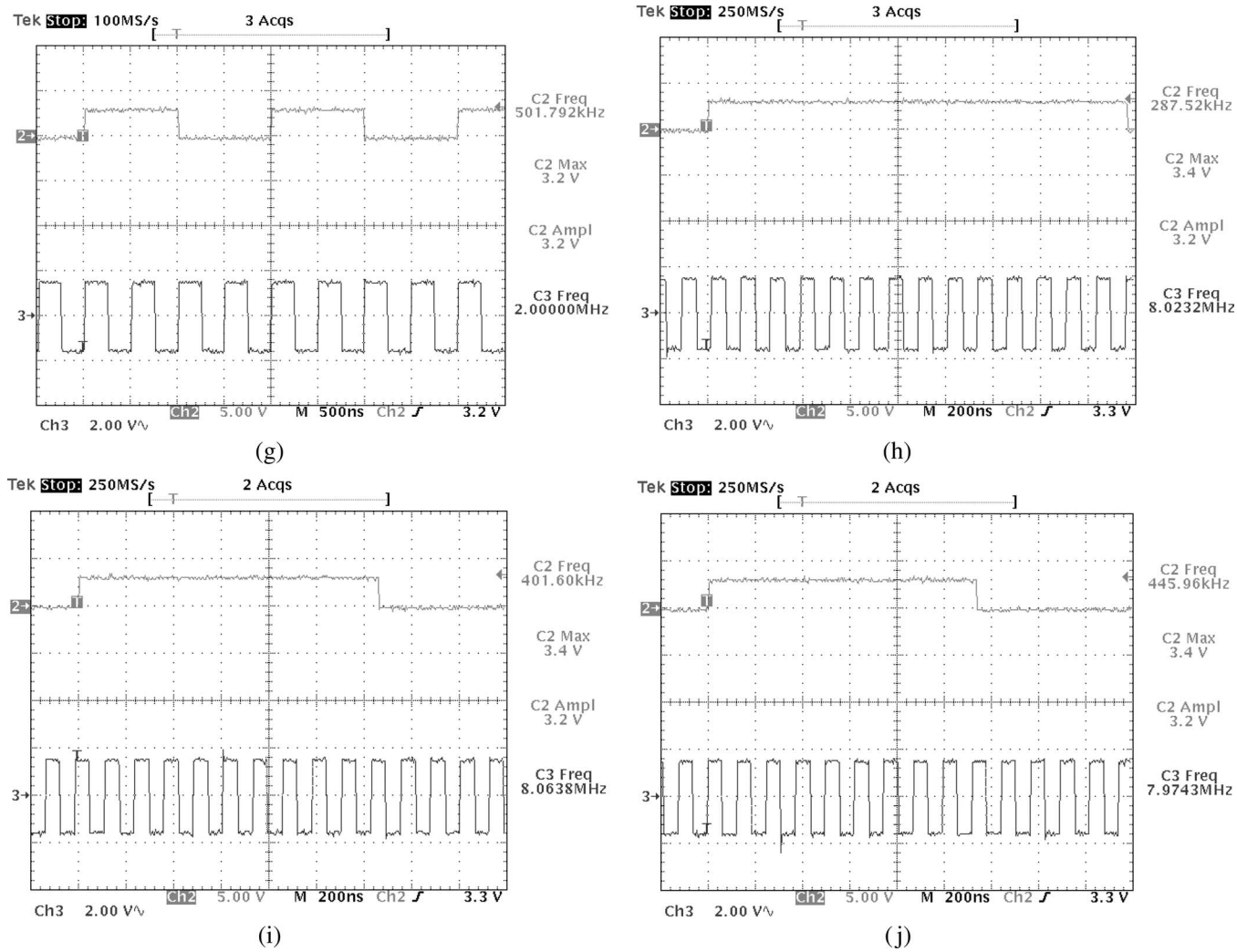


Fig. 29. (*Continued.*) Measured results of the proposed autocompensated sensor transducer under the capacitance C_x of (g) 24 pF, (h) 16 pF with compensation, (i) 20 pF with compensation, and (j) 22 pF with compensation.

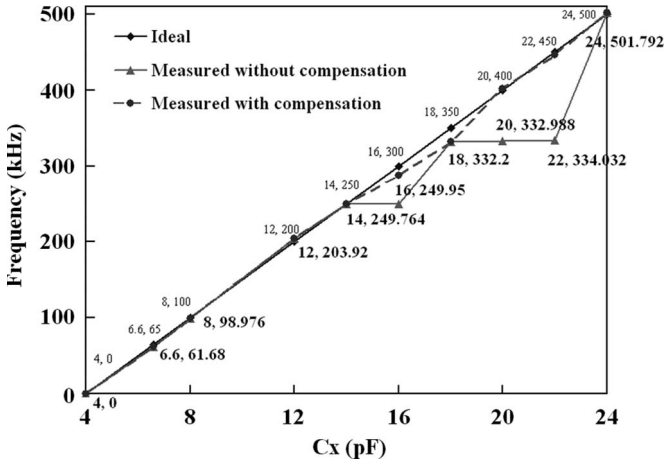


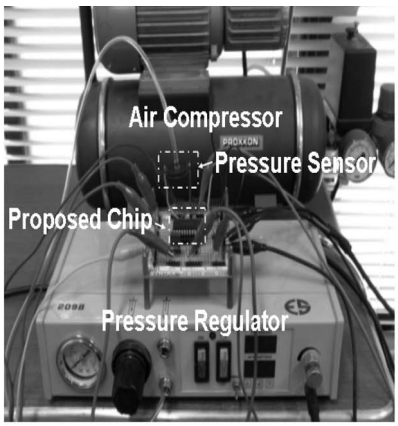
Fig. 30. Measured results of the proposed autocompensated sensor transducer under the varied capacitance of C_x, which ranges from 4 to 24 pF. The boldface-type numbers are the measured values without compensation, and the fine-type numbers are the ideal values.

V. Conclusion

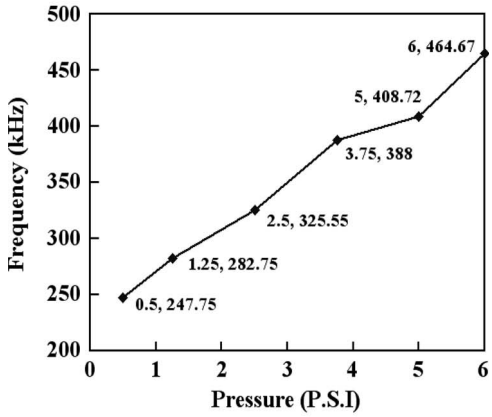
A monolithic CMOS autocompensated sensor transducer for capacitive measuring systems is newly proposed. The proposed autocompensated sensor transducer is attractive due to the fact that a digitized signal is produced without realizing the analog-to-digital converter. Hence, the hardware cost can be reduced. Moreover, the output signal of the proposed transducer can easily be received and processed by the receiver terminal. The automatic compensation circuits enhance and compensate the linear relation between the variable capacitance of the detected sensor and the output digital frequency over the wide dynamic frequency range. In the measurement results, all the functions and the performance of the proposed autocompensated sensor transducer have been successfully verified, and it has been confirmed that it is possible to apply the transducer on the air pressure sensor. In future research, the proposed autocompensated sensor transducer will be integrated with the tire pressure gauge to detect tire pressure, and the pressure information will then be transmitted through a wireless sensor network.

Acknowledgment

The authors would like to thank the SoC Technology Center, Industrial Technology Research Institute, Hsinchu, Taiwan,



(a)



(b)

Fig. 31. (a) Whole measurement setup. (b) Measured results of the proposed autocompensated sensor transducer applied on the air pressure sensors.

TABLE III
SUMMARY ON THE CHARACTERISTICS OF A MONOLITHIC CMOS AUTOCOMPENSATED SENSOR TRANSDUCER FOR CAPACITIVE MEASURING SYSTEMS

Technology	0.35 μm CMOS 2P4M
Methodology of the interface circuit	Switched-capacitor technique
Power supply	3.2 V
System clock rate	2 MHz
Input Capacitance range	4-24 pF
Output Frequency range	0.5-500 kHz
Power consumption	6.4 mW
Accuracy	±5.14%
Physical layout area	940 x 1080 μm^2
Application field	Sensor interface

R.O.C., for their support in chip fabrication and Sinopulsar Technology Inc., Hsinchu, for their support with the pressure sensor.

REFERENCES

[1] L. K. Baxter, *Capacitive Sensors Design and Applications*. New York: IEEE Press, 1997.
[2] S. Chatzandroulis, D. Tsoukalas, and P. A. Neukomm, "A miniature pressure system with a capacitive sensor and a passive telemetry link for use in implantable applications," *J. Microelectromech. Syst.*, vol. 9, no. 1, pp. 18–23, Mar. 2000.
[3] A. D. DeHennis and K. D. Wise, "A wireless microsystem for the remote sensing of pressure, temperature, and relative humidity," *J. Microelectromech. Syst.*, vol. 14, no. 1, pp. 12–22, Feb. 2005.
[4] Y. Wang, M. Nishikawa, R. Maeda, M. Fukunaga, and K. Watanabe, "A smart thermal environment monitor based on IEEE 1451.2 standard for global networking," *IEEE Trans. Instrum. Meas.*, vol. 54, no. 3, pp. 1321–1326, Jun. 2005.
[5] K. Watanabe, H. Matsumote, and K. Fujiwara, "Switched-capacitor frequency-to-voltage and voltage-to-frequency converters," *IEEE Trans. Circuits Syst.*, vol. CAS-33, no. 8, pp. 836–838, Aug. 1986.
[6] H. Matsumoto and K. Watanabe, "Switched-capacitor frequency-to-voltage and voltage-to-frequency converters based on charge balancing principle," in *Proc. IEEE Int. Symp. Circuits Syst.*, 1988, pp. 2221–2224.
[7] D. Yin, Z. Zhang, and J. Li, "A simple switched-capacitor-based capacitance-to-frequency converter," *Analog Integr. Circuits Signal Process.*, vol. 1, no. 4, pp. 353–361, Dec. 1991.
[8] F. Krummenacher, "A high-resolution capacitance-to-frequency converter," *IEEE J. Solid-State Circuits*, vol. SSC-20, no. 3, pp. 666–670, Jun. 1985.
[9] C.-T. Chiang, C.-S. Wang, and Y.-C. Huang, "A CMOS integrated capacitance-to-frequency converter with digital compensation circuit designed for sensor interface applications," in *Proc. IEEE Int. Conf. Sensors*, Oct. 2007, pp. 954–957.

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