An Active Guarding Circuit Design for Wideband Substrate Noise Suppression

Hao-Ming Chao, Wen-Shen Wuen, *Member, IEEE*, and Kuei-Ann Wen, *Member, IEEE*

***Abstract*—In this paper, an active guarding circuit is presented for wideband substrate noise suppression. A feed-forward compensation mechanism is proposed to extend the noise suppression bandwidth and to adjust the amplitude of phase-inversed noise cancellation current by introducing a zero and an amplitude controller. A noise decoupling mechanism is developed to provide a decoupling path and to sense the noise level for generating noise cancellation current. With substrate characterization, parameters of substrate network impedance, decoupling factor, and amplitude of noise cancellation current can be either obtained or determined. The active guarding circuit is implemented in a 90-nm CMOS process based on substrate characterization. The measured substrate noise suppression is better than −9 dB from dc to 250 MHz. The −3-dB suppression bandwidth is effectively extended to 1.2 GHz. The power consumption and circuit area are 2.5 mW and 20 μm × 41 μm, respectively.**

***Index Terms*—Analog circuits, CMOS integrated circuits (ICs), substrate coupling noise, substrate crosstalk, substrate isolation.**

I. Introduction

SUBSTRATE coupling noise is an important effect that can no longer be ignored with recently advancing deep-submicrometer CMOS technology. Lower supply voltage in combination with higher frequency operation in microwave telecommunication integrated circuits (ICs) results in more reactive and resistive impedance nodes in analog circuitry that are very sensitive to noise transients originated from the substrate. For the trend of system-on-chip (SoC) design, multifunctional chips of heterogeneous designs such as digital, analog, RF, embedded memory, microprocessor, and digital signal processing (DSP) are integrated at ever closer distances in a shared substrate to fulfill the requirement of various applications. However, such integration causes signal integrity degradation due to the insufficient isolation between noisy digital circuits and sensitive analog circuits. Fast switching signals generated by digital circuits introduce current spikes coupling through the shared substrate into the sensitive analog and RF circuits, and then adversely affect their performance.

Research of various respects have been performed to alleviate this problem including substrate coupling mechanism [1], [2], substrate coupling modeling [3], [4], substrate coupling effects on analog circuit performance [5]–[8], and substrate coupling reduction techniques [9]–[17]. Accurate modeling and analyzing of substrate coupling is a prerequisite to evaluate the impacts of substrate coupling noise; it also provides parameters for some substrate noise reduction circuits design [13], [16], [17]. Either passive or active methods are applied for substrate coupling noise reduction. For passive methods, different guard ring types are proposed [9], [10]. For active methods, noise signals can be either decoupled or counteracted as the references in [11]–[17]. Among those techniques, passive methods need no power consumption, but may not be effective enough in noisy situations. On the other hand, although active methods have a higher level of noise suppression, there are still several limitations and drawbacks. In [11], [14], and [15], CMOS amplifiers are used to invert the noise signals and inject them into the substrate for counteraction; but their performance are all limited by the tradeoff of power consumption and gain-bandwidth product of amplifiers. Hence, ranges of the effective operation frequency are less than few hundred megahertz. In [12], although a high noise suppression bandwidth as 400 MHz is achieved by employing a high-gain high-bandwidth SiGe HBT amplifier, the heterojunction bipolar technology is not suitable for the SoC design. A current mirror based method is employed in [13] for lower power consumption, but the effective noise suppression is less than 100 MHz due to the parasitic effects that dominate the frequency response. Finally, in [16], substrate noise is wideband suppressed by −1 dB in the frequency range from 40 MHz to 1 GHz, and is maximally −3.5 dB suppressed at 200 MHz by decoupling noise signals to ground via three large capacitors (10 pF each), where the capacitance values are equivalently increased by three power-consuming operational amplifiers (3.3 mW each) through the *Miller effect*.

Here we propose a new substrate noise suppression circuit that employs noise decoupling and feed-forward compensation mechanisms based on substrate characterization to reduce and to suppress the substrate coupling noise. The proposed circuit needs only several active devices of MOS transistors, and no power-consuming high-gain wideband amplifiers or area consuming passive components as capacitors are needed. Circuit design and implementation in 90-nm CMOS technology with performance analyses are also presented. Test keys of different isolation structures with distance variances are measured and

Manuscript received February 26, 2008; revised July 21, 2008. First published October 21, 2008; current version published November 07, 2008. This work was supported by the United Microelectronics Corporation and supported jointly by the Ministry of Education and the National Science Council, Taiwan, under Contract NSC96-2220-E-009-019.

H.-M. Chao and K.-A. Wen are with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: crystal.chao@gmail.com; stellawen@mail.nctu.edu.tw).

W.-S. Wuen is with the Microelectronics and Information Systems Research Center, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: vincent.wuen@gmail.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TMTT.2008.2004900

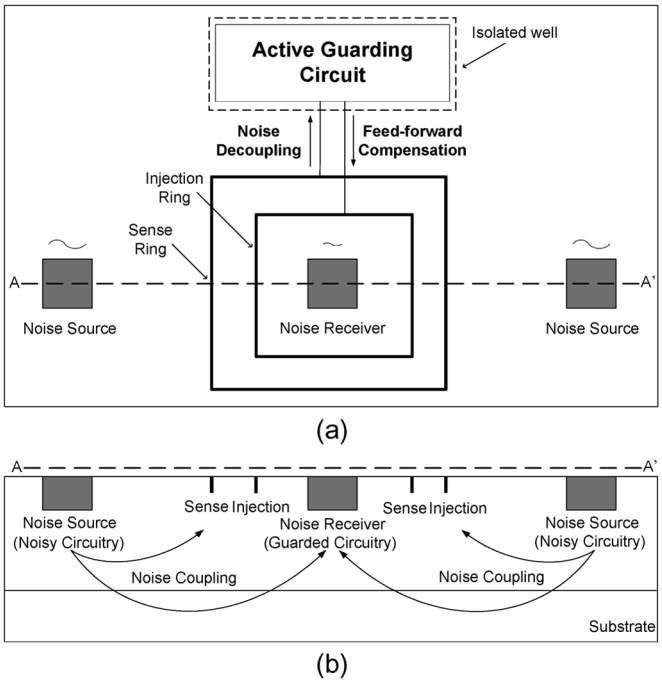


Fig. 1. (a) Top view and (b) cross section of the proposed active guarding circuit.

analyzed within the frequency range that is concerned for substrate characterization with Assura-RF.

This paper is organized as follows. Section II presents the design concepts of the proposed active guarding circuit. Section III describes the substrates characterization with Assura-RF verification. Section IV demonstrates the design and implementation of the active guarding circuit performance analyses. Measurement setup and experimental results are shown in Section V. Discussions and conclusions will be given in Section VI.

II. Design Concepts

As the proposed active guarding circuit shown in Fig. 1, an active guarding circuit with sense and injection rings is inserted between the noise source and guarded circuitry to suppress the substrate noise coupling. The sense ring is placed at the outer side to receive the substrate noise; the injection ring, on the contrary, surrounds the guarded circuitry at the inner side to inject the compensation current back to the substrate. In order to prevent self-induced noise from interfering the guarded circuitry through the common substrate, the active guarding circuit is placed in an isolated well.

As shown in Fig. 2, the proposed substrate noise suppression is achieved by two mechanisms: noise decoupling and feed-forward compensation. Noise current from any direction to the guarded circuitry is detected and averaged at the sense ring, and then decoupled to the active guarding circuit.

The compensation current is generated from the decoupled noise with its phase reversed and the amplitude adjusted. The bandwidth extension is further performed before the compensation current injected back to the substrate. The noise, which flows through the substrate other than the decoupling path at the branch point of the sense ring, can be cancelled by mixing the

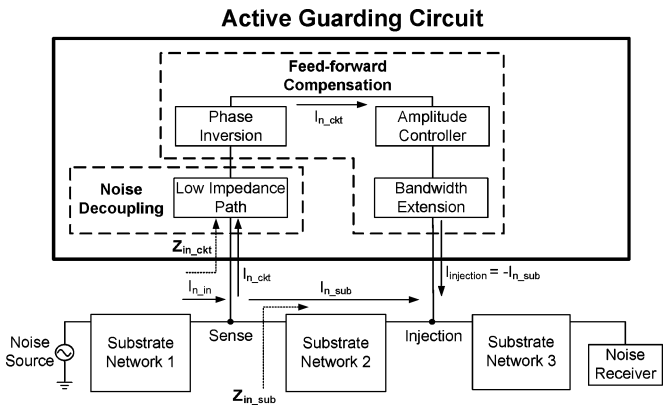


Fig. 2. Concepts of substrate noise suppression mechanisms of noise decoupling and feed-forward compensation.

compensation current via the injection ring. By implementing noise decoupling and feed-forward compensation with bandwidth extension, substrate noise received at the guarded circuitry can be effectively suppressed to ensure its performance.

A. Noise Decoupling

Noise decoupling is performed by creating a decoupling path connected to the sense ring. The decoupling path has an impedance value much lower than or at the same order as that of *substrate network 2*. Consequently, the input noise current flows through either the decoupling branch or *substrate network 2* at the sense point. Hence, the total substrate noise current flowing toward the guarded circuitry is reduced.

A decoupling factor F_D is defined to present the percentage of the input noise current I_{n_in} that is decoupled. As shown in Fig. 2, the decoupling branch connecting the active guarding circuit has an impedance of $Z_{\mathrm{in\_ckt}}$. The equivalent impedance of *substrate network 2* is defined as $Z_{\mathrm{in\_sub}}$. I_{n_in} is divided into two portions: the current being drained away by the active guarding circuit and the noise current continuing flowing through the substrate toward guarded circuitry I_{n_ckt} and I_{n_sub}. The substrate noise $(1F_D)$ is reduced at this stage as follows:

$$F_D(\%) = \frac{I_{n\_\mathrm{ckt}}}{I_{n\_\mathrm{in}}} = \left(\frac{1}{\dfrac{Z_{\mathrm{in\_ckt}}}{Z_{\mathrm{in\_sub}}} + 1} \right). \tag{1}$$

$Z_{\mathrm{in\_sub}}$ can be extracted from the substrate model and considered as a known parameter. The design parameter for decoupling factor F_D is $Z_{\mathrm{in\_ckt}}$.

The smaller $Z_{\mathrm{in\_ckt}}$ is, the larger F_D can be obtained, which means more noise current can be drained away from the substrate, and the smaller noise level will affect the guarded circuitry. However, in a circuit implementation using MOS transistors, $Z_{\mathrm{in\_ckt}}$ cannot be arbitrarily small. The smaller $Z_{\mathrm{in\_ckt}}$, the larger the MOS transistor size required, leading to higher power consumption and area.

B. Feed-Forward Compensation

The feed-forward compensation operation includes -180° phase inversion, amplitude adjustment, and bandwidth exten-

sion. A lot of well-known circuits can be used to perform phase inversion. Current mirror is herein chosen for its simplicity. The phase-inversed I_{n_ckt} is delivered to an amplitude controller with current gain $A_C(s)$ to adjust the magnitude of the compensation current $I_{\mathrm{injection}}$ to be identical to I_{n_sub}, as shown in (2). I_{n_sub} can flow through both the surface and bottom portions of substrate network 2. By designing the injection ring to be placed closely adjacent to the sense ring, the surface portion of substrate network 2 is a low impedance path and dominates the current flow of I_{n_sub}. Finally, the magnitude-matched and phase-inversed current $I_{\mathrm{injection}}$ is injected to the substrate through the injection ring and mixed with I_{n_sub} for cancellation of the total noise receiving at the guarded circuitry

$$I_{\mathrm{Injection}} = I_{n\_\mathrm{ckt}} \times A_C(s) = -I_{n\_\mathrm{sub}} = -I_{n\_\mathrm{in}} \times (1 - F_D). \tag{2}$$

The amplitude controller current gain $A_C(s)$ can be determined by the following equation:

$$|A_C(s)| = \frac{I_{n\_\mathrm{sub}}}{I_{n\_\mathrm{ckt}}} = \frac{Z_{\mathrm{in\_ckt}}}{Z_{\mathrm{in\_sub}}} = \frac{1}{F_D} - 1. \tag{3}$$

Tradeoffs between device mismatches and parasitic effects exist in the current mirror design, which is used to perform phase inversion. When noise frequencies are higher than the bandwidth of the current mirror, the losses and phase shifts will degrade the noise suppression performance. To release the bandwidth limitation, a zero is introduced.

In order to obtain the substrate network impedance, substrate characterization is prior to the design of the active guarding circuit and will be discussed in Section III.

III. Substrate Characterization

In order to characterize the substrate, structures of various isolation schemes composed of P+ guard ring (P+GR), Nwell guard ring (NWGR), and deep Nwell (DNW) of triple-well structures were fabricated in a 90-nm CMOS process and are characterized and analyzed [20]. The dependence of signal coupling on distance and frequency are extracted as substrate networks. Parameters in the extracted substrate networks are used for the design of the decoupling factor F_D and amplitude controller in the active guarding circuit. The characterized substrate networks also allow designers to utilize in their design process, and hence, choose the most suitable isolation scheme to meet the specification of substrate coupling noise tolerance and the budgets for the process costs.

A. Test Keys for Different Isolation Schemes

Five isolation schemes are designed based on three basic isolation structures, which include P+GR, NWGR, and DNW, compared to the reference (REF). Thus, six different structures of test keys include REF, P+GR, NWGR, DNW, NWGR with P+GR (NWGR/P+GR), and DNW with P+GR (DNW/P+GR) are implemented and measured in the frequency range from 100 MHz to 10 GHz with a distance variance from 10 to 100 μm. As shown in Figs. 3–8, schematics in the figures are designed structures corresponding to each measurement results, where the P+ region at the right is the noise sources and the one at the left is the receiver. The areas of the noise source and receiver are both 7.4 μm $\times$ 13 μm. The width of both P+GR and NWGR is 1.5 μm and the distance from P+GR and NWGR to noise receiver are 1.5 and 3 μm, respectively.

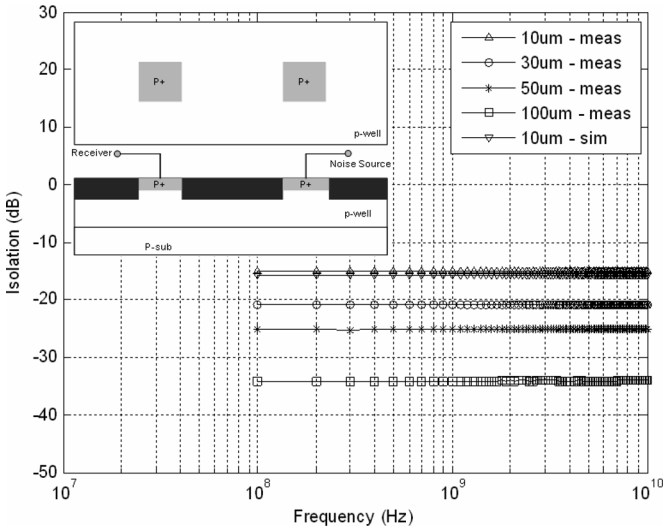


Fig. 3. Measurement and simulation results of the reference structure.

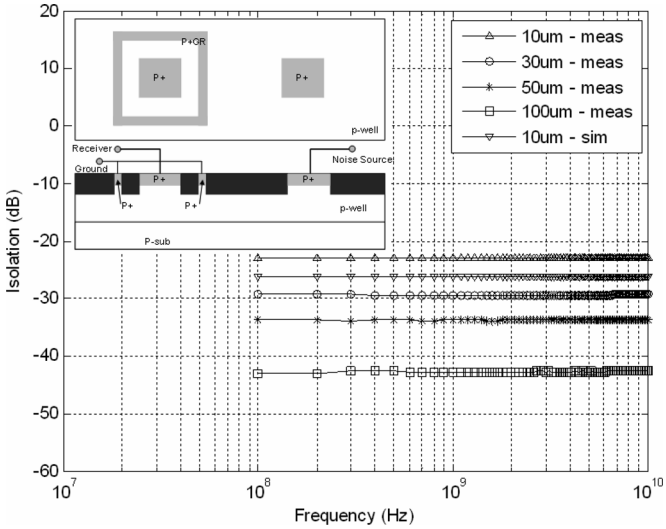


Fig. 4. Measurement and simulation results of the P+GR isolation scheme.

By comparing the isolation schemes of single guard ring structures in a frequency range below 10 GHz, the P+GR, NWGR, and DNW structures give approximately 8-, 25-, and 25–55-dB isolation improvement, compared to the reference structure at an isolation distance of 10 μm correspondingly. For the double guard ring designs of NWGR/P+GR and DNW/P+GR, they provide isolation performance of approximately 10 and 7 dB better than that of NWGR and DNW, respectively. The designs with the DNW structure give the most isolation, but require additional implant/mask processing steps, which increase the cost and the time of process cycle. Therefore, such designs cannot always be used.

The better isolation performances for NWGR and DNW and other double guard ring structures compared to P+GR is owing to the junction capacitances between NW/TW, DNW/TW,

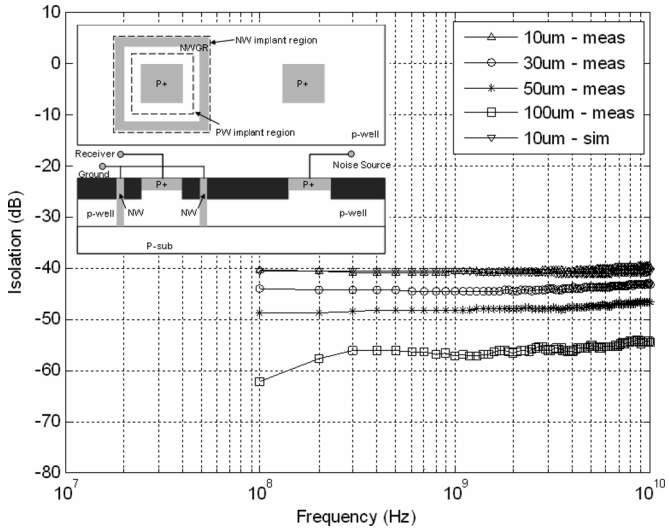


Fig. 5. Measurement and simulation results of the NWGR isolation scheme.

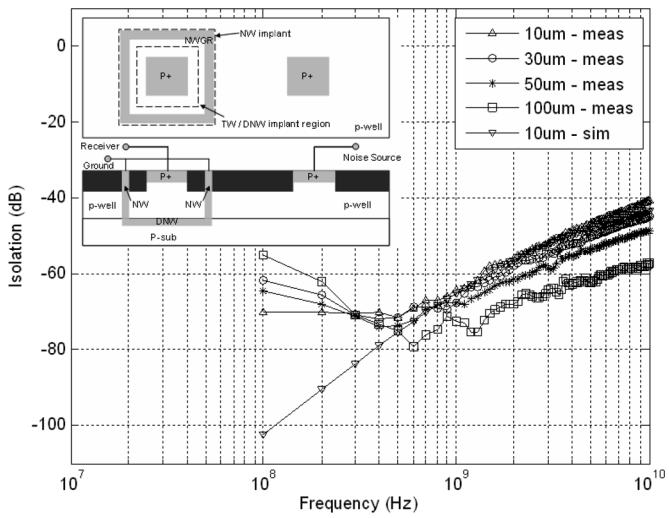


Fig. 6. Measurement and simulation result of the DNW isolation scheme.

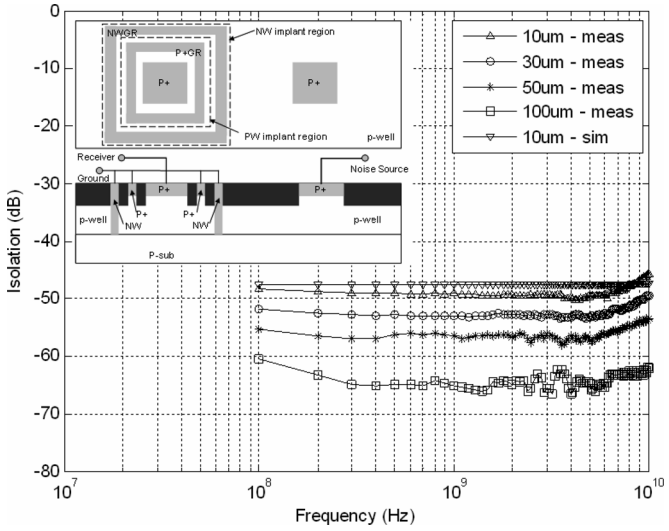


Fig. 7. Measurement and simulation results of the NWGR/P+GR isolation scheme.

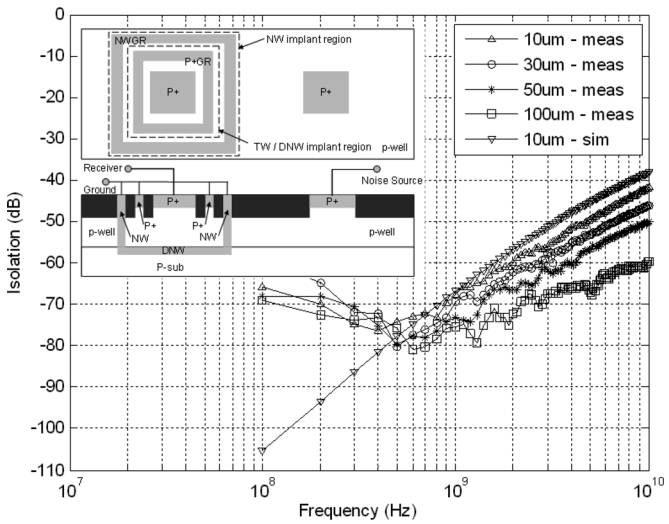


Fig. 8. Measurement and simulation results of the DNW/P+GR isolation scheme.

NW/PW, and DNW/PW, which formed a obstacle to block the substrate coupling noise. However, they start to lose this advantage when the frequency increases, as the higher frequency decreases the capacitive blocking capability of the junctions. For frequencies below several gigahertz, the DNW structure achieves better substrate isolation compared to the NWGR. Nevertheless, as the frequency reaches 10 GHz, the DNW structure shows almost the same isolation performance as NWGR.

To analyze the isolation character of the single guard ring structures, in the frequency below 10 GHz of interest, the isolation performance of P+GR shows a resistive behavior, which is independent of frequency, where NWGR shows both resistive and capacitive behaviors as the frequency gets higher than several gigahertz and DNW behaves mainly capacitive in the entire frequency range. These characterizations are verified with Assura-RF as the substrate networks shown in Fig. 9.

B. Substrate Characterization with Assura-RF

For substrate characterization, Assura-RF is used to extract the substrate network between devices with process information such as thickness of subdivisions, junction capacitances parameters, and material characteristics. The characterized substrate network is both resistive and capacitive considering high-frequency effects. Fig. 9 demonstrates two characterized networks between the noise source and the receiver for single guard ring test structures of REF, P+GR, NW, and DNW. The simulation results with each characterized substrate networks for the six test-key structures are shown in Figs. 3–8 compared to the measurement results in a 10-μm isolation distance. The average errors for each isolation scheme are shown in Table I.

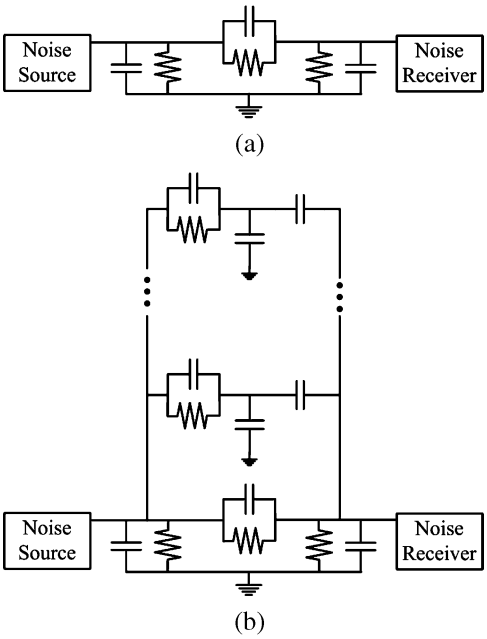


Fig. 9. Characterized substrate networks for: (a) REF and P+GR and (b) NWGR and DNW.

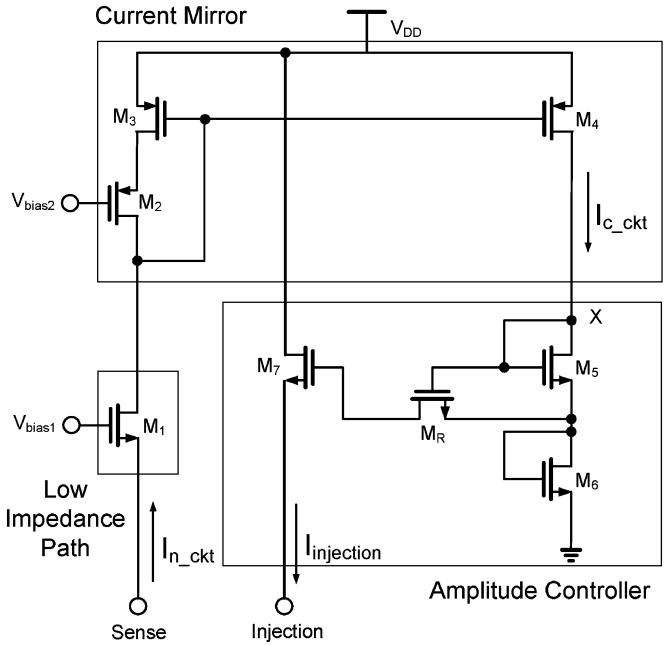


Fig. 10. Proposed active guarding circuit.

TABLE I
AVERAGE ERROR BETWEEN SIMULATION AND MEASUREMENT RESULTS

Isolation schemes	REF	P+GR	NWGR	DNW	NWGR/ P+GR	DNW/ P+GR
Average error	5%	14.5%	1.8%	4.2%	2.9%	8.2%

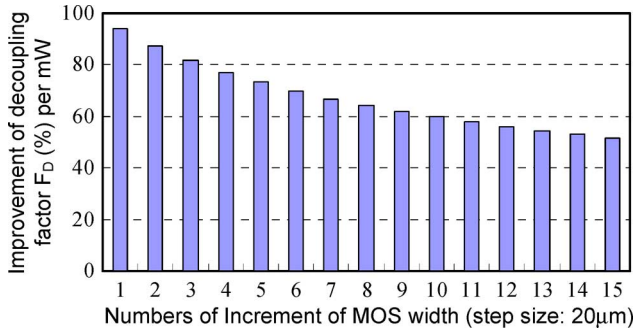


Fig. 11. Improvement of decoupling factor versus numbers of 20-μm width increment of M_1 from 150 μm.

IV. Active Guarding Circuit Design and Analyses

A. Noise Decoupling

Fig. 10 shows the schematic of the proposed active guarding circuit. The input common-gate transistor M_1 creates a low impedance path for the noise decoupling at the sense point with impedance value $1/g_{m1}$. Unlike other designs [12], [13], which use the common source configuration as the input stage to sense the substrate noise voltage from gate, M_1 not only senses the noise current, but also drains it away, leading to lower noise level for cancellation in the later stage.

For larger decoupling factor design, i.e., more noise current is drained away, the input impedance $1/g_{m1}$ should be designed as small as possible. However, smaller $1/g_{m1}$ indicates a larger transistor size $(W/L)_1$, which consumes large area and power. To optimize the design, improvement of decoupling factor F_D in percentage per milliwatt as the numbers of 20-μm-width increment of M_1 from 150 μm is studied.

Fig. 11 shows that less than 60% improvement of the decoupling factor F_D per milliwatt is achieved after the tenth increment of M_1 width of 350 μm when the noise frequency is 1 GHz. Therefore, the ninth increment of MOS width, i.e., 330 μm, is chosen as the width of M_1.

B. Feed-Forward Compensation

To realize the feed-forward compensation mechanism, MOS transistors from M_2 to M_7 and M_R are added to perform the phase inversion, amplitude control, and bandwidth extension.

The -180° phase inversion of the decoupled noise current I_{n_ckt} is accomplished by a current mirror composed from M_2 to M_4. The phase-inversed current I_{c_ckt} (which is identical to I_{n_ckt} for an ideal current mirror) is sent to the amplitude controller and bandwidth extension circuit composed from M_5 to M_7 and M_R. The current is converted to voltage via the diode-connected transistors M_5 and M_6. Finally, the transconductance stage M_7 adjusts the current gain together with M_5, M_6, and M_R then converts the voltage back into current $I_{\mathrm{injection}}$, which is injected into the substrate to cancel the noise current I_{n_sub}. A detailed design of the amplitude controller and bandwidth extension circuits are shown below.

C. Amplitude Control

Fig. 12 shows the equivalent circuit of the amplitude controller and bandwidth extension circuit. Transistor M_5 and M_6 are modeled as resistor $1/g_{m5}$ and $1/g_{m6}$ with their parasitic

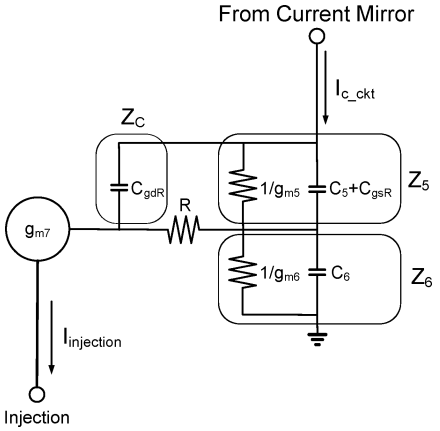


Fig. 12. Equivalent circuit of the amplitude controller and bandwidth extension circuit.

capacitance C_5 and C_6. M_R is modeled as a resistor R with its gate–drain parasitic capacitance $C_{\mathrm{gd}R}$ and gate–source parasitic capacitance $C_{\mathrm{gs}R}$, and M_7 performs as a transconductance stage.

Equation (4) shows the transfer function of $I_{\mathrm{injection}}/I_{c\_\mathrm{ckt}}$ as the small-signal current gain $A_A(s)$ of the amplitude controller

$$A_A(s) = \frac{I_{\mathrm{injection}}}{I_{c\_\mathrm{ckt}}} = \left(\frac{RZ_5}{R+Z_5+Z_C} + Z_6\right) \times g_{m7}. \quad (4)$$

Therefore, the low-frequency current gain, i.e., $A_C(0)$, can be approximated as

$$|A_A(0)| = \frac{I_{\mathrm{injection}}}{I_{c\_\mathrm{ckt}}} = \frac{g_{m7}}{g_{m6}}. \quad (5)$$

By referring to (3) and (5), the current gain can be determined as follows:

$$|A_A(0)| = \frac{I_{n\_\mathrm{sub}}}{I_{n\_\mathrm{ckt}}} = \frac{1/g_{m1}}{R_{\mathrm{in\_sub}}} = \frac{I_{\mathrm{injection}}}{I_{c\_\mathrm{ckt}}} = \frac{g_{m7}}{g_{m6}}. \quad (6)$$

As a result, given $R_{\mathrm{in\_sub}}$ from a substrate model and an optimal designed impedance $1/g_{m1}$, the ratio of g_{m7}/g_{m6} is determined to match the current of $I_{\mathrm{injection}}$ and I_{c_sub} for substrate noise cancellation.

D. Bandwidth Extension

To improve the noise suppression performance at high frequencies, a bandwidth extension circuit is applied by inserting a triode-region transistor M_R. The introduction of M_R creates a zero and a pole [18], which can be expressed as

$$Z_R = -\frac{g_{m6}}{g_{m5}+g_{m6}} \times \frac{1}{RC_{\mathrm{gd}R}}$$
$$P_R = -\frac{1}{RC_{\mathrm{gd}R}}. \quad (7)$$

Hence, the effective noise suppression bandwidth of the active guard circuit can be extended by designing the zero Z_R close to the original dominant pole P_D of the circuit without M_R to perform frequency compensation. The bandwidth is extended until P_R begins to affect the frequency response. The dominant pole P_D of the circuit without M_R can be approximated as

$$P_D \cong -\frac{1}{R_X(C_X||C_P)} \quad (8)$$

where $R_X = r_{o4}||[1/gm_5 + 1/gm_6]$, and r_{o4} is the output resistance of M_4. $C_X = C_5 + [C_6||(C_{\mathrm{gs7}} + C_{\mathrm{sub}})||C_{\mathrm{gd7}}]$, C_5, and C_6 are the parasitic capacitance of M_5 and M_6, and C_{sub} is the equivalent capacitance of substrate seen from the source of M_7. $C_P = C_{\mathrm{gd4}} + (C_{\mathrm{gs4}}||C_{\mathrm{gs3}})$.

E. Phase Estimation

For further analysis of the current subtraction error at the *injection* node due to phase mismatch, two parts of the phase shifts are analyzed: the phase shift of the remained noise current that flows from the *sense* node to the *injection* node through the substrate; and the phase shift of decoupled noise current that flows from the *sense* node to the *injection* node through the proposed active guarding circuit. As mentioned in Section II-B, since the injection ring is placed closely adjacent to the sense ring, the former phase shift from the *sense* node to the *injection* node through the substrate can be minimized, and thus, neglected. As for the latter, phase estimation is done to analyze the phase shifts from the *sense* node to the *injection* node through the proposed active guarding circuit as a function of frequency. Two portions of the phase shifts as $\angle A_C(j\omega)$ and $\angle A_A(j\omega)$, which express the phase shift from the *sense* node to the current mirror output node X (in Fig. 10) and the phase shift from node X to the amplitude controller output node (*injection*), respectively, are derived from the small-signal current gain of the current mirror $A_C(s)$ [which is shown in (9)] and current gain of the amplitude controller $A_A(s)$ [which is shown in (4)]

$$A_C(s) = \frac{I_{c\_\mathrm{ckt}}}{I_{n\_\mathrm{ckt}}} = -\frac{SC_{\mathrm{gs2}}g_{m4}+g_{m2}g_{m4}}{S^2C_{\mathrm{gs2}}(C_{\mathrm{gs3}}+C_{\mathrm{gs4}})+S(C_{\mathrm{gs3}}+C_{\mathrm{gs4}})+g_{m2}g_{m3}}. \quad (9)$$

For a transfer function $A(s)|_{s=j\omega} = (a+bj)/(c+dj)$, the phase shift can be expressed as $\angle A(j\omega) = \tan^{-1}(b/a) + \tan^{-1}(d/c)$. The phase response of the current mirror can be estimated as $\angle A_C(j\omega)$, as in (10). The effect of the bandwidth extension circuit in the phase domain can be revealed via $\angle A_A(j\omega)$, as shown in (11)

$$\angle A_C(j\omega) = -\pi + \tan^{-1}(b_1/a_1) - \tan^{-1}(d_1/c_1) \quad (10)$$

where $a_1 = g_{m2}g_{m4}$, $b_1 = \omega g_{m2}g_{m4}$, $c_1 = g_{m2}g_{m3} - \omega^2 C_{\mathrm{gs2}}(C_{\mathrm{gs3}} + C_{\mathrm{gs4}})$, and $d_1 = \omega(C_{\mathrm{gs3}} + C_{\mathrm{gs4}})$,

$$\angle A_A(j\omega) = \tan^{-1}(b_2/a_2) - \tan^{-1}(d_2/c_2) \quad (11)$$

where $a_2 = g_{m5} - \omega^2[RC_{\mathrm{gd}R}(C_5 + C_6 + C_{\mathrm{gd}R})]$, $b_2 = \omega[C_5 + C_{\mathrm{gs}R} + C_{\mathrm{gd}R} + RC_{\mathrm{gd}R}(g_{m5}+g_{m6})]$, $c_2 = g_{m5}g_{m6} - \omega^2[C_6(C_5+C_{\mathrm{gs}R}+C_{\mathrm{gd}R})+g_{m6}RC_{\mathrm{gd}R}(C_5+C_{\mathrm{gs}R})]$, and $d_2 = \omega[g_{m6}(C_5 + C_{\mathrm{gs}R} + C_{\mathrm{gd}R}) + g_{m5}C_6] - \omega^3 C_6 C_{\mathrm{gd}R}(C_5 + C_6)$.

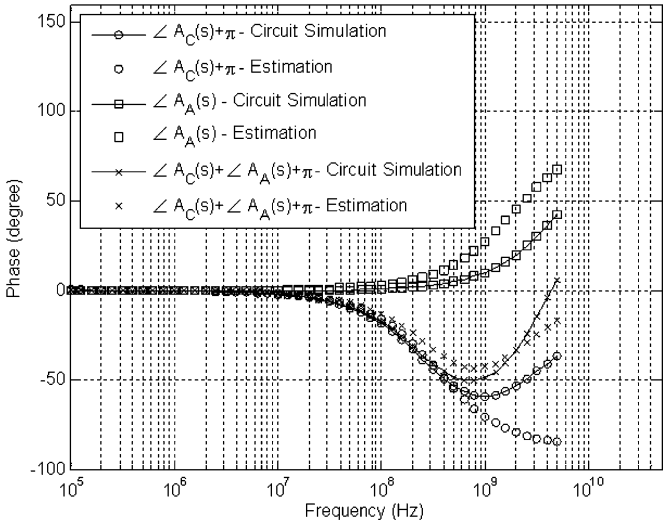


Fig. 13. Equivalent circuit of the amplitude controller and bandwidth extension circuits.

The estimated results are shown in Fig. 13 in comparison with circuit simulation results of $\angle A_C(j\omega)$ and $\angle A_A(j\omega)$ and their sum $\angle A_C(j\omega) + \angle A_A(j\omega) + \pi$, which indicates the total unwanted phase shifts for signals passing through the proposed active guarding circuit. Both estimated results and circuit simulation results show that the bandwidth extension circuit provides an opposite sign of phase shift that compensates the phase shift of the current mirror in a wide frequency range, and consequently reduces the total phase errors, which result in the subtraction error. However, although the phase errors are reduced, the magnitude of the injection current for substrate noise cancellation is still attenuated as the frequency gets higher. Therefore, in high frequency, the noise suppression performance of the proposed active guarding circuit is still degraded.

F. Circuit Injected Noise

Though the proposed active guarding circuit counteracts substrate coupling noise, it inevitably induces noises to the common substrate while performing suppression.

Unwanted noises induced by the circuit are classified into two parts; . The first part is the noise coupling through the common substrate from the transistor's bulk. The second part is the noises injecting directly to the substrate through the wires connected to the sense and injection ring.

For the first part, as described in Section II, the active guarding circuit is placed in an isolated well, and as shown in Fig. 5 for the NWGR isolation scheme, the isolated well provides at least 40-dB isolation performance for 10-μm isolation distance. Therefore, the noises injected from the circuit, which might transfer through the common substrate to the guarded circuit, will be mostly blocked by the well, and thus, can be neglected.

As for the second part, the total thermal noise at output node (*injection*) can be expressed as follows:

$$\overline{I_{\text{noise}}^2} = 4KT\gamma \times (g_{m1} + g_{m2} + g_{m3} - g_{m4} - g_{m5} + g_{m6}) \times \frac{g_{m7}}{g_{m6}} + 4KT\gamma \times g_{m7}. \quad (12)$$

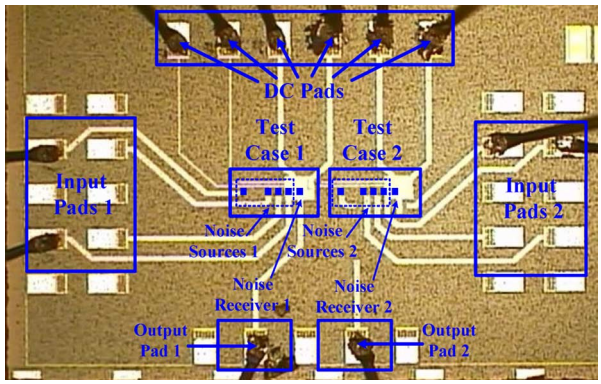


Fig. 14. Microphotograph of the proposed active guarding circuit.

In this study, I_{noise} is approximately 7.54×10^{-11} A in low frequency at room temperature. On the other hand, although the flicker noise might degrade the circuit performance, the degradation is only limited in low frequencies up to several megahertz. As a result, the total noise injected by the proposed circuit is much lower than the considered noise level in a wide frequency range.

V. Measurement Setup and Experimental Results

Based on the above design concepts with a characterized substrate model, the proposed active guarding circuit is implemented in 90-nm CMOS technology.

Fig. 14 shows a microphotograph of the fabricated chip. The area of the proposed active guarding circuit core is 20 μm $\times$ 41 μm. Two independent test cases of *Test Case 1* and *Test Case 2*, shown in Fig. 15, are implemented in the same chip with identical active guarding circuit designs. For each test case, four independent noise source inputs made of P+ diffusion pickups are placed with isolation distances of approximately 30, 50, 70, and 110 μm between the noise sources and receiver. Signal generators are used to send signals as noises with various input powers and frequencies from -30 to 15 dBm and from dc to 5 GHz, respectively. The noise signals are coupled through the P+ diffusion pickups to the substrate and the noise receiver, and then measured by a spectrum analyzer via the output pads.

The measurement results show similar suppression performance for isolation distances of 30 and 50 μm. For isolation distances of 70 and 110 μm, the suppression performance cannot be correctly measured due to the limitation of the instruments' sensitivity and the noise from the measurement environment since the noise level at output is lower then -80 dBm. As a result, the suppression performance for 30 μm is chosen to be presented in the following discussions.

A. Test Case 1

The setup for chip on-board measurement is shown in Fig. 15. *Test Case 1* evaluates the substrate coupling noise suppression performance by turning the active guarding circuit on/off and measures the isolation between the noise sources and receiver. Fig. 16 shows the measurement and simulation results in the frequency range from dc to 5 GHz with 30-μm isolation distance. The measurement and simulation data showed a 2–3-dB level

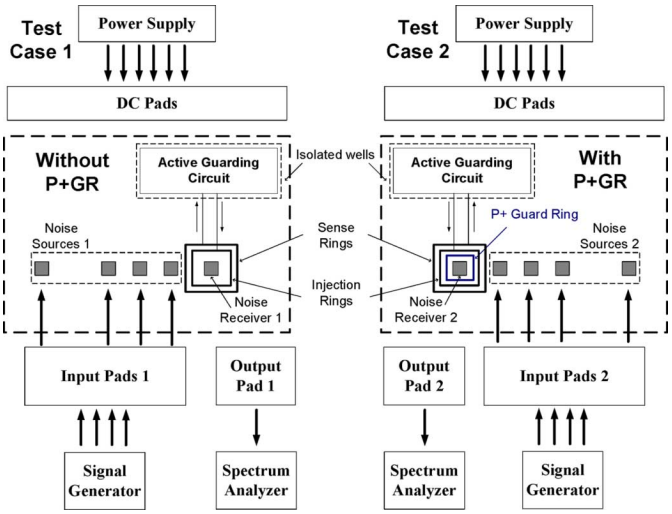


Fig. 15 Test plans and measurement setup for the fabricated chip.

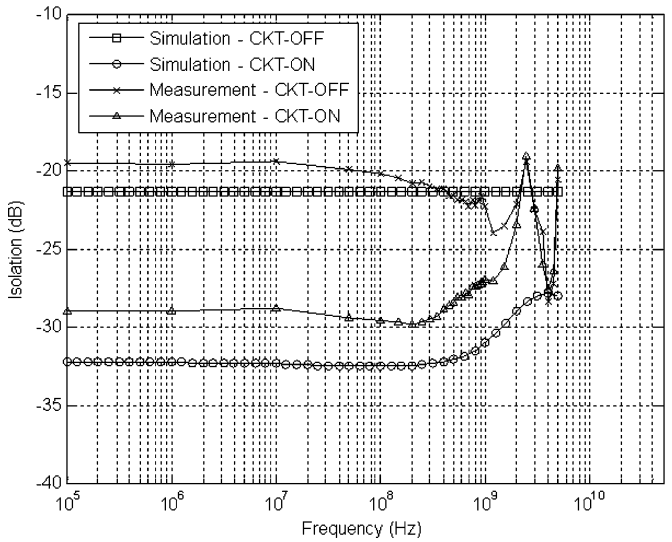


Fig. 16. Simulation and measurement results of the isolation performance versus frequency for *Test Case 1*.

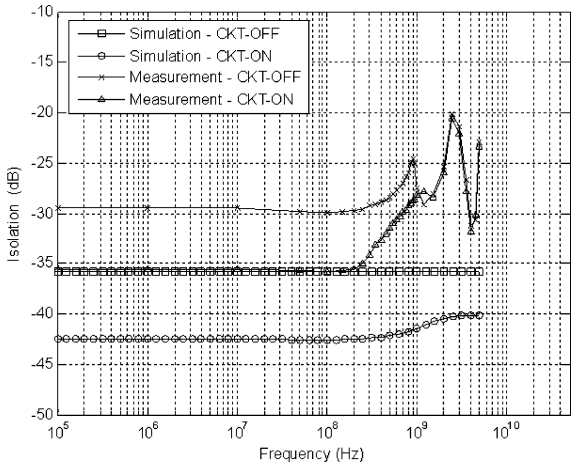


Fig. 17. Simulation and measurement results of the isolation performance versus frequency for *Test Case 2*.

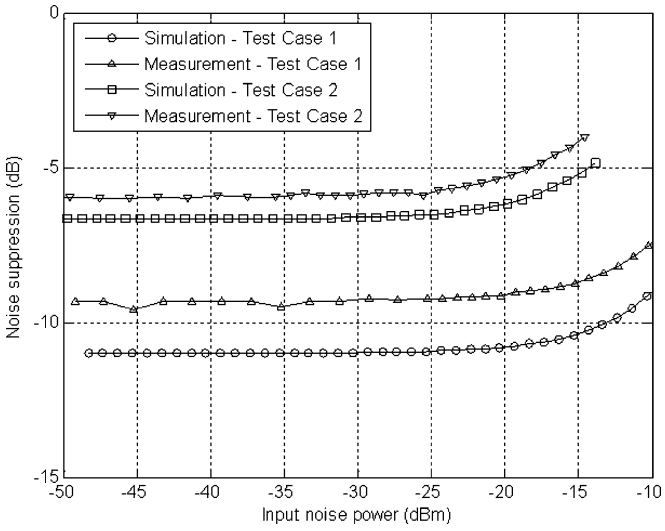


Fig. 18. Simulation and measurement results of circuit noise suppression performance versus input noise power.

shift due to the 5% inaccuracy of the substrate model for REF, as shown in Table I. The measurement results of circuit performance show an effective −3-dB noise suppression bandwidth from dc to 1.2 GHz and −1-dB bandwidth up to 2.2 GHz. The noise suppression, which is better than −9 dB, is obtained in the frequency range from dc to 250 MHz. The total power consumption is approximately 2.5 mW for 1-V supply voltage.

B. Test Case 2

Owing to the common use of P+GR, in *Test Case 2*, a P+GR is inserted to surround the noise receiver in *Test Case 1* to see the performance enhancement, as shown in Fig. 15. The substrate coupling noise suppression performance is obtained in the same manner as *Test Case 1*. Fig. 17 shows the measurement and simulation results of *Test Case 2* in the frequency range from dc to 5 GHz with 30-μm isolation distance. In comparison with *Test Case 1* when the circuit is off, P+GR contributes 10- and 14-dB isolation to measurement and simulation results, respectively. Owing to the 14.5% inaccuracy of the substrate model for P+GR, as shown in Table I, the data of measurement and simulation show a 5-dB level shift. The measurement result of circuit performance shows an effective −3-dB noise suppression bandwidth from dc to 650 MHz and −1-dB bandwidth up to 950 MHz. The noise suppression, which is better than −6 dB, is obtained in the frequency range from dc to 200 MHz. The total power consumption is approximately 3.5 mW for 1-V supply voltage.

For both *Test Case 1* and *Test Case 2* in frequencies higher than several hundred megahertz to gigahertz, the measured performance is degraded compared to the simulation results. This degradation is due to the poor ground plane resulting from the lack of parallel ground bonding wires on the test board and the loading effect of the output pads, which affect the high-frequency performances. Moreover, the bonding pads were too small in that only one wire bonding for each output pad is allowed, and thus cannot be corrected in this version. Nevertheless, the circuit performance can be evaluated for the wideband

TABLE II
PERFORMANCE SUMMARY

References	Technology	Noise Suppression Bandwidth			Power	Area
		-9dB Bandwidth	-3dB Bandwidth	-1dB Bandwidth		
This Work	90nm (CMOS)	DC – 250MHz	DC – 1.2GHz	DC – 2.1GHz	2.5mW	20μm × 41μm
JSSC'05 [16]	0.13μm (CMOS)	N/A	170MHz – 300MHz	60MHz – 1GHz	9.9mW	N/A
VLSI'05 [15]	0.35μm (CMOS)	N/A	500MHz – 600MHz	N/A	N/A	about 450μm x 500μm
CICC'00 [12]	0.8μm (SiGe)	DC – 150MHz	DC – 400MHz	DC – 500MHz	13.5mW	N/A

characteristic from dc to 1.2 GHz and 250 MHz for −3- and −9-dB noise suppression, respectively. In the next version of the test chip, the proposed circuit will be designed for on-wafer testing to avoid the unwanted effects of bond wires.

In addition, as shown in Fig. 17, the circuit performance in *Test Case 2* is not as good as that in *Test Case 1* because the inserting of P+GR decreases the input impedance $Z_{\text{in\_sub}}$ of the substrate at the branch point of noise decoupling, which also leads to the decrease of F_D. Therefore, for the identical active guarding circuit design, as in *Test Case 1*, the compensation current $I_{\text{injection}}$ that corresponded to F_D is smaller than the substrate noise current I_{n_sub}, and hence, results in the performance degrade. To get better performance in *Test Case 2*, the amplitude controller gain can be easily adjusted according to the decoupling factor F_D.

Fig. 18 shows the measured and simulated noise suppression performance as noise power at the noise receiver increases from −50 to −10 dBm at 10 MHz. The 1-dB degradation points of the measured noise suppression performance are approximately −13 and −19 dBm for *Test Case 1* and *Test Case 2*, respectively, which present the noise tolerance for the active guarding circuit inputs in these two test conditions.

The performance of the active guarding circuit is summarized in Table II with comparison to other recently published active substrate noise suppression circuits with measurement results. The proposed circuit has the widest noise suppression bandwidth with the smallest power and area consumption.

In view of the fact that the better performances shown in Table II may be due to the advanced technology of the 90-nm process, characteristics of the power consumption, circuit area, and suppression bandwidth of the proposed active guarding circuit are discussed as follows.

The power consumption of the proposed active guarding circuit can be expressed as follows in (13):

$$\begin{aligned} VDD \times I_{\text{Total}} &= VDD \times (I_{D1} + I_{D4} + I_{D7}) \\ &= VDD \times (2I_{D1} + I_{D7}) \\ &= VDD \times \Big(g_{m1} \times (V_{\text{GS1}} - V_t) \\ &\qquad + \frac{1}{2} g_{m7} \times (V_{\text{GS7}} - V_t) \Big) \end{aligned} \tag{13}$$

where I_{D1}, I_{D4}, and I_{D7} are the drain currents of transistor M_1, M_4, and M_7, and I_{D1} is identical to I_{D4} based on the characteristic of the current mirror. From (1), given the substrate impedance $Z_{\text{in\_sub}}$, the circuit input impedance $Z_{\text{in\_ckt}}$ $(1/g_{m1})$ can be chosen according to a designed decoupling factor F_D, and g_{m7} can be determined from (6). $(V_{\text{GS1}} - Vt)$ and $(V_{\text{GS7}} - Vt)$ can also be easily designed in the same value no matter what technology is chosen. Therefore, all these design parameters for power consumption can be equally designed in any technologies (given that $Z_{\text{in\_sub}}$ does not vary much in different technologies). Moreover, previous research on CMOS transistor scaling effects [19] had concluded that the transconductance-to-current ratio, i.e., g_m/I_D, is almost technology independent for saturated transistors. As a result, the current consumption of the proposed active guarding circuit is almost the same over different CMOS technologies and the power consumption is thus proportional to the supply voltage for different technologies. By comparing this work of the 90-nm process with 1.0-V supply voltage with the previous literature [16] of the 0.13-μm process with a 1.2-V supply voltage, the normalized power consumption of this study $(2.5\ \text{mW} \times 1.2 = 3\ \text{mW})$ is still much lower than that of [16] (9.9 mW). Since the chip area is highly related to the process, this study indeed gains some advantage owing to the down scaling of the 90-nm process. However, the main contribution of the small area comes from the architecture of the proposed active guarding circuit. In comparison to [16], which requires three high-gain amplifiers and three large capacitors, this study requires only eight active devices of MOS transistors, and no area-consuming high-gain wideband amplifiers or capacitors is needed. Therefore, to the best of the authors' knowledge, this study achieves an area of 20 μm × 41 μm that is much smaller than any previous design.

The noise suppression bandwidth could also be wider owing to the higher cutoff frequency of 90-nm technology compared to older generation technologies. Nevertheless, this study still requires the bandwidth extension technique to enhance noise suppression at gigahertz frequency.

To summarize, this study indeed gains some advantages in the advanced 90-nm technology, but the circuit architecture and technique in fact enhance the overall performance. Along with the continuous down scaling of the CMOS process and the trend of the SoC design, the substrate coupling noise issue becomes more and more important, the proposed circuit benefits from

better performance and lower power consumption as the technology scales down, and it is very suitable for future applications in industry.

VI. Discussions and Conclusions

An active guarding circuit design for wideband substrate noise suppression has been proposed with substrate characterization. The substrate noise is effectively suppressed by employing a noise decoupling mechanism and feed-forward compensation mechanism, which performs phase inversion, amplitude control, and bandwidth extension. Experimental results have demonstrated a wide -3-dB bandwidth as 1.2 GHz for noise suppression with noise-suppression performance better than -9 dB up to 250 MHz. The noise tolerance for the input of the proposed circuit is proven to be -13 dBm for 1-dB performance degradation.

The characterized substrate model provides simplified substrate networks for the common single guard ring structures, which can be utilized for further studies on substrate coupling issues. In addition, the experimental results of various isolation schemes provide useful information about choosing a proper one under different design considerations.

In conclusion, this is the first active substrate noise suppression circuit with wideband characteristics that has ever proposed with measurement results. The area requirement and power consumption are the smallest, compared to any other previous studies as referenced to the best of the authors' knowledge. Moreover, the proposed circuit benefits from better performance and lower power consumption as the technology scales down. Therefore, the proposed active guarding circuit is very suitable for future applications in the industry of highly integrated SoC designs with continuous down-scaling CMOS technology.

Acknowledgment

This research was conducted at the Trans.-Wireless Technology (TWT) Laboratory, National Chiao Tung University, Taiwan. The authors would like to thank Dr. M.-F. Chou, Taihan Precision Technology Company Ltd., Taipei, Taiwan, for valuable discussions and the RF team of the United Microelectronics Corporation, Hsinchu, Taiwan, for the support of substrate characterization.

References

[1] D. K. Su, M. J. Loinaz, S. Masui, and B. Wooley, "Experimental results and modeling techniques for substrate noise and mixed-signal integrated circuits," *IEEE J. Solid-State Circuits*, vol. 28, no. 4, pp. 420–430, Apr. 1993.

[2] M. van Heijninjen, J. Compiet, P. Wambacq, S. Donnay, M. G. E. Engels, and I. Bolsens, "Analysis and experimental verification of digital substrate noise generation for epi-type substrates," *IEEE J. Solid-State Circuits*, vol. 35, no. 7, pp. 1002–1008, Jul. 2000.

[3] A. Koukab, K. Banerjee, and M. Declercq, "Modeling techniques and verification methodologies for substrate coupling effects in mixed-signal system-on-chip designs," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 23, no. 6, pp. 823–836, Jun. 2004.

[4] N. K. Verghese and D. J. Allstot, "Verification of RF and mixed-signal integrated circuits for substrate coupling effects," in *Proc. IEEE Custom Integr. Circuits Conf.*, May 1997, pp. 363–370.

[5] M. Nagata, J. Nagai, K. Kijikata, T. Morie, and A. Iwata, "Physical design guides for substrate noise reduction in CMOS digital circuits," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 539–549, Mar. 2001.

[6] J. Catrysse, "Measured distortion of the output-waveform of an integrated opamp due to substrate noise," *IEEE Trans. Electromagn. Compat.*, vol. 37, no. 5, pp. 310–312, May 1995.

[7] M. Xu, D. K. Su, D. K. Shaeffer, T. H. Lee, and B. A. Wooley, "Measuring and modeling the effects of substrate noise on the LNA for a CMOS GPS receiver," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 473–485, Mar. 2001.

[8] C. Soens, G. Van der Plas, P. Wambacq, S. Donnay, and M. Kuijk, "Performance degradation of *LC*-tank VCOs by impact of digital switching noise in lightly doped substrates," *IEEE J. Solid-State Circuits*, vol. 40, no. 7, pp. 1472–1481, Jul. 2005.

[9] T. L. Hsu, Y. C. Chen, H. C. Tseng, V. Liang, and J. S. Jan, "psub guard ring design and modeling for the purpose of substrate noise isolation in the SOC era," *IEEE Electron Device Lett.*, vol. 26, no. 9, pp. 693–695, Sep. 2005.

[10] J. P. Z. Lee, F. Wang, A. Phanse, and L. C. Smith, "Substrate cross talk noise characterization and prevention in 0.35 μm CMOS technology," in *Proc. IEEE Custom Integr. Circuits Conf.*, May 1999, pp. 479–482.

[11] T. Liu, J. D. Carothers, and W. T. Holman, "A negative feedback based substrate coupling noise reduction method," in *Proc. ASIC/SOC Conf.*, Sep. 1999, pp. 49–53.

[12] W. Winkler and F. Herzel, "Active substrate noise suppression in mixed-signal circuits using on-chip driven guard rings," in *Proc. IEEE Custom Integr. Circuits Conf.*, May 2000, pp. 357–360.

[13] N. R. Agung, S. Takagi, and N. Fujii, "Improving the immunity to substrate noise using active noise cancellation circuit in mixed-signal integrated circuits," in *Proc. IEEE Asia–Pacific Circuits Syst. Conf.*, Oct. 2002, pp. 135–140.

[14] R. A. Nicodimus, S. Takagi, and K. Wada, "Active shield circuit for digital noise suppression in mixed-signal integrated circuits," *IEICE Trans. Fundamentals*, vol. E88-A, pp. 438–443, Feb. 2005.

[15] T. Nakura, M. Ikeda, and K. Asada, "Feedforward active substrate noise cancelling technique using power supply di/dt detector," in *VLSI Circuits Symp. Tech. Dig.*, Jun. 2005, pp. 284–287.

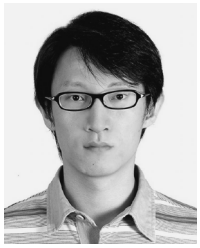
[16] T. Tsukada, Y. Hashimoto, K. Sakata, H. Okada, and K. Ishibashi, "An on-chip active decoupling circuit to suppress crosstalk in deep-submicron CMOS mixed-signal SoCs," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 67–79, Jan. 2005.

[17] H. M. Chao, C. L. Wang, W. S. Wuen, and K. A. Wen, "An active guarding circuit for giga-hertz substrate noise suppression," in *Proc. IEEE Eur. Microw. Integr. Circuits Conf.*, Oct. 2007, pp. 119–122.

[18] A. Rusznyak, "Filtering current mirror," *Proc. Inst. Elect. Eng.—Circuits, Devices, Syst.*, vol. 149, no. 4, pp. 218–220, Aug. 2002.

[19] C. Galup-Montoro, M. C. Schneider, and R. M. Coitinho, "Scaling rules allow the reuse of MOS analog design," in *Proc. IEEE Int. Microelectron. Syst. Educ. Conf.*, Jun. 2001, pp. 8–9.

[20] Y. C. Chen, "90 nm logic 1P9M substrate noise isolation characterization report," United Microelectron. Corporation (UMC), Hsinchu, Taiwan, TIC Doc., 2005.



Hao-Ming Chao was born in Taipei, Taiwan, in 1980. He received the B.S. degree in electrical control engineering and M.S. degree in electronics engineering from National Chiao Tung University, Taiwan, in 2003 and 2005, respectively, and is currently working toward the Ph.D. degree in electronics engineering from National Chiao Tung University.

His research interests include substrate noise in mixed-signal circuits and analog/mixed-signal circuit design.

Wen-Shen Wuen (M'98) was born in Hsinchu, Taiwan. He received the B.S., M.S. and Ph.D. degrees in electronics engineering from National Chiao Tung University (NCTU), Taiwan, in 1996, 1998 and 2004, respectively.

He is currently a Research Assistant Professor with the Microelectronics and Information Systems Research Center, NCTU. His research interests include CMOS RF IC and analog/mixed signal circuit design.

Kuei-Ann Wen (M'90) received the B.S., M.S., and Ph.D. degrees in electrical engineering from National Cheng-Kung University (NCKU), Taiwan, in 1983, 1985, and 1988, respectively.

She is currently a Full Professor with the Department of Electrical Engineering, National Chiao Tung University, Taiwan. His research interests are in the areas of SoC design and very large scale integration (VLSI) wireless communication circuits/systems, including RF circuits and baseband design. She covers and enhances the curriculum for SoC integration, VLSI computing and signal processing, and RF wireless communication. She has been involved in several key research projects including advanced IC/VLSI for academic excellence, and technology transfer for successful high-tech. She also set up the research cooperation laboratories with Agilent Technologies, Mentor Graphics, and Synopsys for the development of wireless SoC design automation, as well as the flow for industrial experts. She also leads the Trans. Wireless Technology (TWT) Laboratory, sponsored by the United Microelectronics Corporation (UMC), Hsinchu, Taiwan, for the development of advanced CMOS RF.