A Novel Planarization of Oxide-Filled Shallow-Trench Isolation

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ABSTRACT

Two planarization approaches of the oxide-filled trench isolation have been evaluated. Results show that the oxide-filled shallow-trench isolation technology based on a chemical-mechanical polishing (CMP) process is difficult to control and has a poor uniformity. It also results in a dishing effect in wide field regions. On the other hand, a new planarization process can achieve an excellent uniformity and fully planar surface by using a combination of a masking polysilicon layer based on a CMP process, selective wet etching for oxide refill on active regions, short-time CMP process for oxide refill, and reactive ion etching etchback. Results also show that the high breakdown yield of the gate oxide and the low leakage current of the n^+/p junction diodes with the novel planarization process demonstrates extremely low defect density from this process. This new process is a very promising candidate for oxide-filled shallow-trench isolation.

Introduction

To realize the scaled, high-density, and high-performance very large scale integrated (VLSI) devices and circuits, the isolation and planarization processes become more and more important. The local oxidation of silicon (LOCOS) isolation has been widely utilized in the high density dynamic ramdom access memory (DRAM) device.[1-3] Furthermore, to achieve lithography limited dimensions and multilevel interconnections with high-speed performance, the planarization process is another key processing step. The surface topography of integrated circuits is easy to planarize if the silicon wafer is planarized from the initial isolation process. However, the LOCOS-based isolation process results in a large encroachment of field oxide (bird's beak) into the devices' active regions, narrow width effect due to high-temperature oxidation, field oxide thinning effect,[4] and nonplanar surface topography.

Therefore, the oxide-filled trench isolation technology is the most promising candidate to circumvent these problems.[6,7] However, the conventional resist planarization and reactive ion etching (RIE) etchback process has cumulative tolerences associated with large film thickness and easily results in nonplanar surface topography.[8] The etchback and planarization of oxide-filled shallow trenches based on a chemical-mechanical polish (CMP) process has been proposed to solve these problems.[8,9] However, the CMP-only process shows problems with nonuniform polish and difficult control because there is no stopper for oxide etchback.[10] Also, the CMP-only process results in dishing effect in wide field regions.[9]

In order to overcome these problems and meet the stringent requirements mentioned above, an isolation and planarization technology which satisfies those requirements is required. This paper presents a novel planarization technique of oxide-filled shallow trenches to achieve an excellent uniformity and eliminate the dishing effect in wide field regions. It utilizes a combination of the formation of a masking polysilicon layer based on a CMP process with high etching selectivity,[11] selective wet etching for oxide refill on active regions, short-time CMP process for oxide refill, and RIE etchback.

Test structures of shallow trench isolation and the process sequence are described. The experimental results on the removal rate and the etching selectivity based on a CMP process are shown. The dishing effect in wide field regions and the global uniformity of shallow trench isolation is also discussed. Finally, the electrical characterization is evaluated.

Experimental

In order to evaluate the removal rate of polysilicon film, a 600 nm thick poplysilicon layer was deposited by low pressure chemical vapor deposition (LPCVD) at 620°C on a 100 nm thick silicon dioxide layer which was grown on 6 in. p-type (100) silicon wafers by wet oxidation at 980°C. For the determination of the removal rate of silicon nitride film, a 200 nm thick LPCVD silicon nitride (SiN) layer was directly deposited on p-type (100) silicon wafers at 780°C. Moreover, for the determination of the removal rate of CVD oxide film, a 500 nm thick LPCVD silicon dioxide was directly deposited on p-type (100) silicon wafers at 700°C. The polishing slurries (RODEL 2371 and SC-1) used in this experiment are colloidal silica in an aqueous KOH solution. Details on the slurries' properties are listed in Table I. The polishing pad is a microporous polyurethane material, and the hardness of pad is 52 ~ 62 Shore D. The flow rate of slurry was 200 ml/min and the platen temperature was set 98°F.

The novel planarization process of oxide-filled shallow trenches considered in this work is shown in Fig. 1. A new complete structure of the oxide-filled shallow trenches is shown in Fig. 1a. First, the trench hard mask was fabricated that consisted of 30 nm of thermally grown pad oxide and 200 nm of SiN. The hard mask and silicon trenches (400 nm) were etched by RIE. After the removal of photoresist, wafers were cleaned. A 30 nm thick silicon dioxide was grown by dry oxidation at 925°C. Next, 900 nm thick LPCVD oxide was deposited to refill the shallow trenches. Finally, a 300 nm thick LPCVD polysili-

Table I. The conditions of slurry A and slurry B.

	Slurry A	Slurry B
Type (Rodel)	SC-1	2371
PH	10.0 ~ 10.3	11.0 ~ 11.5
Particle size (nm)	30	70 ~ 90
Weight percent solids	30	28
Viscosity (cps)	<150	<25

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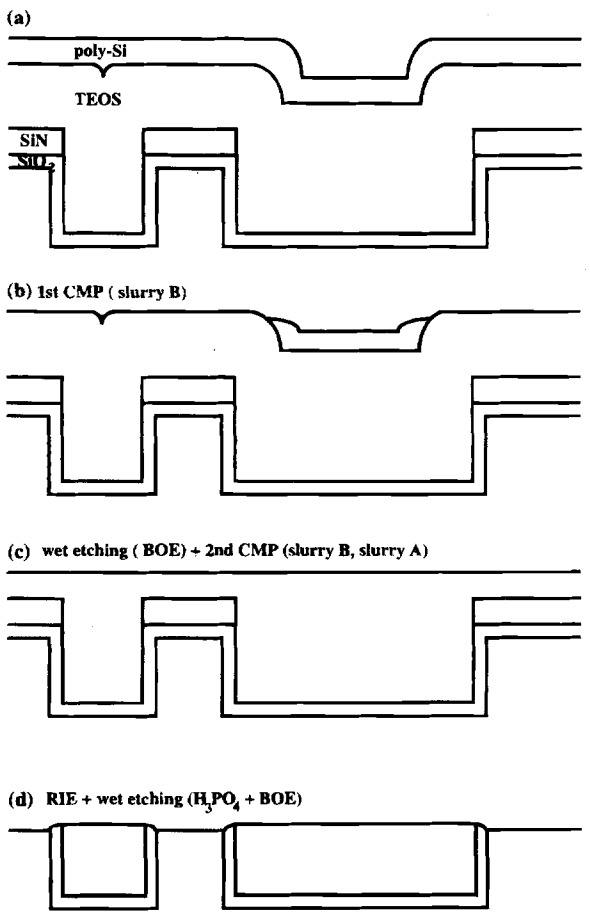

Fig. 1. The process sequence of the novel planarization.

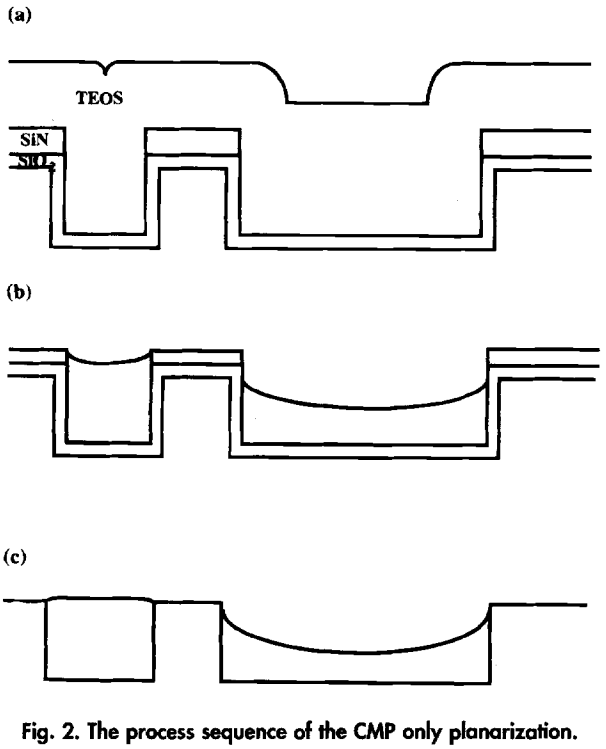

Fig. 2. The process sequence of the CMP only planarization.

con layer was deposited. The polysilicon layer was first polished at 4 psi with a dilute 3:1 slurry B listed in Table I until the polysilicon layer on the active regions was removed. However, the field regions were still capped by a polysilicon layer as shown in Fig. 1b. The oxide refill on active regions was then dipped to the level of the field oxide in the field regions with a buffer hydrofluoride acid. Next, the rest of polysilicon was polished at 4 psi with a dilute 3:1 slurry B. The oxide refill then underwent a short-time (1 min) CMP process at 7 psi with a dilute 2:1 slurry A as shown in Fig. 1c. The CMP process was followed by the RIE etchback. The RIE etchback process was stopped until the SiN layer remained at ~70 nm. Figure 2 shows the schematic process sequence of oxide-filled shallow trenches based on a CMP-only process. A complete structure of oxide-filled shallow trenches is shown in Fig. 2a. After the shallow trenches were refilled, the CVD-oxide layer was polished at 7 psi (47.6 kPa) with a dilute 2:1 slurry A as shown in Fig. 2b. After two planarization processes, wafers were cleaned and annealed in a N_2 ambient at 900°C for 30 min. Then, the SiN layer was stripped by a H_3PO_4 solution. Finally, the pad oxide was removed by a buffer HF solution.

After the planarizatrion processes, the wafers were cleaned. A 10 nm thick silicon dioxide was grown by dry oxidation at 900°C. Next, the screen oxide was stripped by a buffer HF solution.

To invesigate the creation of defects during the planarization process, the MOS capacitors and the n^+/p junction were performed. After the gate oxide (9.5 nm) was grown by dry oxidation at 900°C, a 300 nm LPCVD polysilicon gate was deposited at 620°C and doped by $POCl_3$ at 950°C. After the wafers were cleaned, Al was deposited and annealed at 350°C in N_2 ambient for 30 min to make capacitors. In addition, to form the n^+/p junction, arsenic implantation was performed through a 5 nm pad oxide at 60 keV with a dose of 5×10^{15} cm^{-2}. After the implantation process, wafers were cleaned, and a 550 nm LPCVD oxide was deposited at 700°C. Next, wafers were annealed in N_2 ambient at 900°C for 15 min to form the n^+/p junction. After the contact holes and aluminum contact were performed, wafers were sintered in a N_2 ambient at 350°C for 30 min.

Results and Discussion

Figure 3a and b shows the removal rates of polysilicon, CVD oxide, and SiN with pressures of 4 psi (27.2 kPa) and 7 psi (47.6 kPa). The various ratios of water/slurry A and water/slurry B were used as shown in Fig. 3a and b, respectively. The removal rate of polysilicon is 175.3 nm/min at 7 psi (47.6 kPa) with a dilute 2:1 slurry A as shown in Fig. 3a, while, the removal rate of CVD oxide is 116 nm/min and that of SiN is 50.5 nm/min at 7 psi (47.6 kPa) with a dilute 2:1 slurry A. However, the removal rate of polysilicon reaches 405 nm/min at 4 psi (27.2 kPa) and 560 nm/min at 7 psi (47.6 kPa) with a dilute 3:1 slurry B, while the removal rate of CVD oxide is only 4.5 nm/min at 4 psi (27.2 kPa) and 8.7 nm/min at 7 psi (47.6 kPa) with a dilute 3:1 slurry B. Moreover, the removal rate of SiN is also only 4.4 nm/min at 4 psi (27.2 kPa) and 8.65 nm/min at 7 psi (47.6 kPa) with a dilute 3:1 slurry B. Within the polishing process (Westech Model 372M wafer polisher), the film on the substrate will be removed. The removal rate, dT/dt, of a film of thickness, T, follows the Preston equation

$$dT/dt = Kpds/dt$$

where p is the applied pressure and ds/dt is the relative velocity between the film surface and the pad. K is the Preston coefficient.[12,13] Therefore, higher pressure results in a higher removal rate as shown in Fig. 3a and b. The removal rates of CVD oxide and SiN with slurry A are apparently higher than those of CVD oxide and SiN with slurry B. The reason is that smaller silica particles (slurry A) result in larger indentation stress.[13] This implies that the mechanical effect is the dominant factor of the removal process for CVD oxide and SiN. However, the significantly higher removal rate of polysilicon with slurry B is the high KOH concentration. Furthermore, the strength of the Si–Si bond is weaker than that of the Si–N or Si–O

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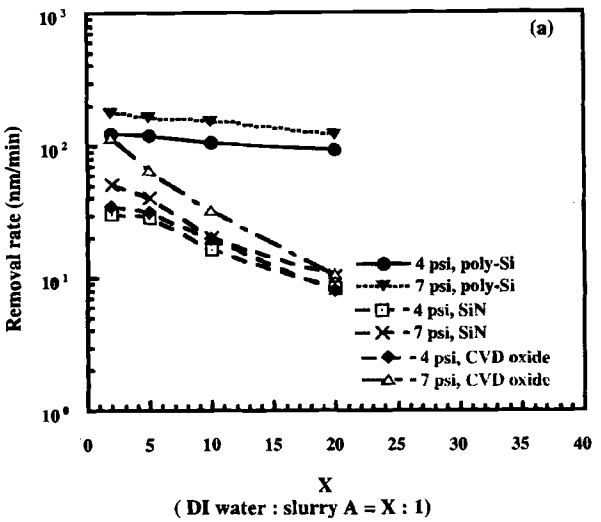


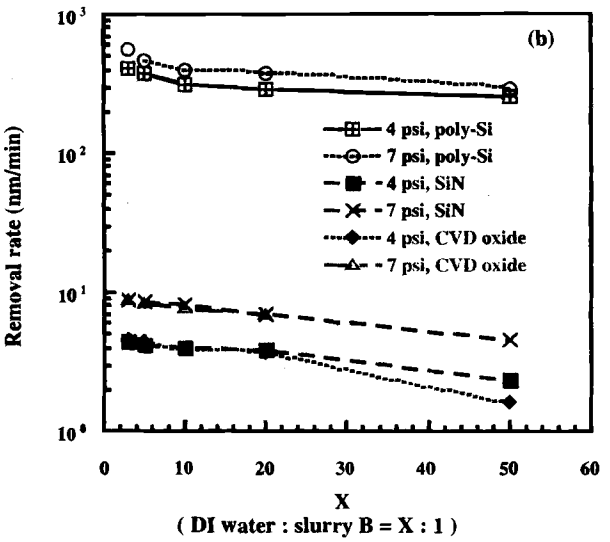
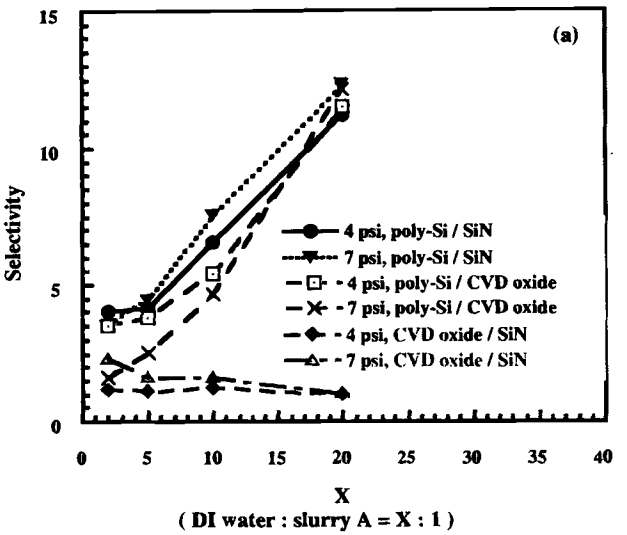


Fig. 3. The removal rates of polysilicon, CVD oxide, and SiN with (a) slurry A and (b) slurry B.



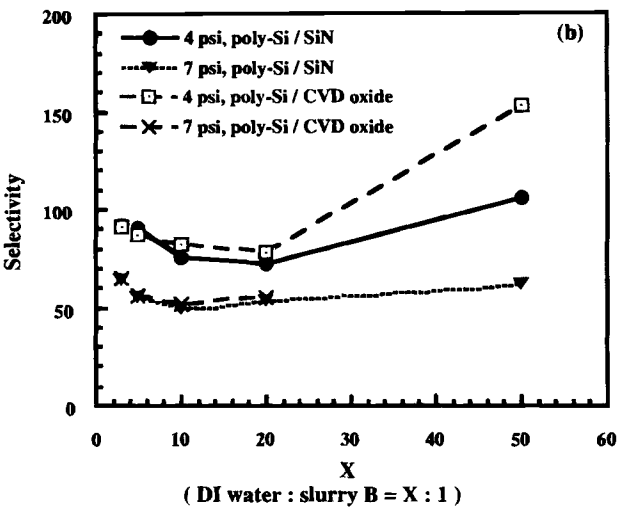


Fig. 4. The etch selectivity (a) polysilicon to oxide and SiN, and oxide to SiN (slurry A) and (b) polysilicon to oxide and SiN (slurry B).

bond. Within the polishing process, the temperature is elevated due to the friction of the slurry particle, pad, and wafer surface.[13] Therefore, the chemical-removal process of polysilicon becomes the dominant factor of the removal process.[14] The chemical reactions taking place in water separating silica surface molecules from the bulk are progressively as[12]

$$\equiv Si- + 4\ OH^- \rightarrow \equiv Si\text{–}OH + 3\ OH^- \rightarrow =Si(OH)_2$$

$$+ 2\ OH^- \rightarrow -Si(OH)_3 + OH^- \rightarrow Si(OH)_4$$

The etch selectivity of CVD oxide with respect to SiN is low (<3) as shown in Fig. 4a. Therefore, there is no way to stop the oxide etchback. The etch selectivity of polysilicon with respect to CVD oxide and SiN is shown in Fig. 4a and b. Comparing Fig. 4a and b, slurry B, with higher KOH concentration and larger silica particles, results in higher selectivity. The reason for this is that the large silica particles reduce the mechanical effect and the high KOH concentration enhances the chemical reactions. The etch selectivity of polysilicon to CVD oxide and SiN reaches 92 at 4 psi (27.2 kPa) with a dilute 3:1 slurry B. As a result, the CVD-oxide or SiN layer can serve as a stopper for polysilicon etchback. Moreover, lower pressure results in higher selectivity with slurry B.

Figure 5a shows the scanning electron microscope (SEM) micrograph of 1 μm wide field region of oxide-filled shallow trenches after the novel planarization process and the pad oxide/SiN layer stripped. According to Fig. 5, the novel planarization of oxide-filled shallow trenches considered in this work can achieve a planar surface in narrow field regions. Figure 5b shows the SEM micrograph of oxide-filled shallow trenches after a CMP process process at 7 psi (47.6 kPa) with a dilute 2:1 slurry A and the pad oxide/SiN layer stripped. Although this CMP process can achieve a planar surface in narrow field regions, it is difficult to control due to low etching selectivity of CVD oxide to SiN.

Figure 6 shows the SEM micrographs of 2 mm wide field regions of oxide-filled shallow trenches after the novel planarization process and the pad oxide/SiN layer stripped. No dishing of the field oxide in the adjacent active area is present as shown in Fig. 6a. Also, no dishing is observed 1 mm away from the edge of the large structure as shown in Fig. 6b. Therefore, the novel planarization of oxide-filled shallow trenches considered in this work can also achieve a planar surface in wide field regions. Figure 7 shows the SEM micrographs of 2 mm wide field region of oxide-filled shallow trenches after a CMP process and the pad oxide/SiN layer stripped. Slight dishing of the field oxide in the adjacent active area is present as shown in Fig. 7a. However, dishing (160 nm) is obviously observed 1 mm away from the edge of the large structure as shown in Fig. 7b.

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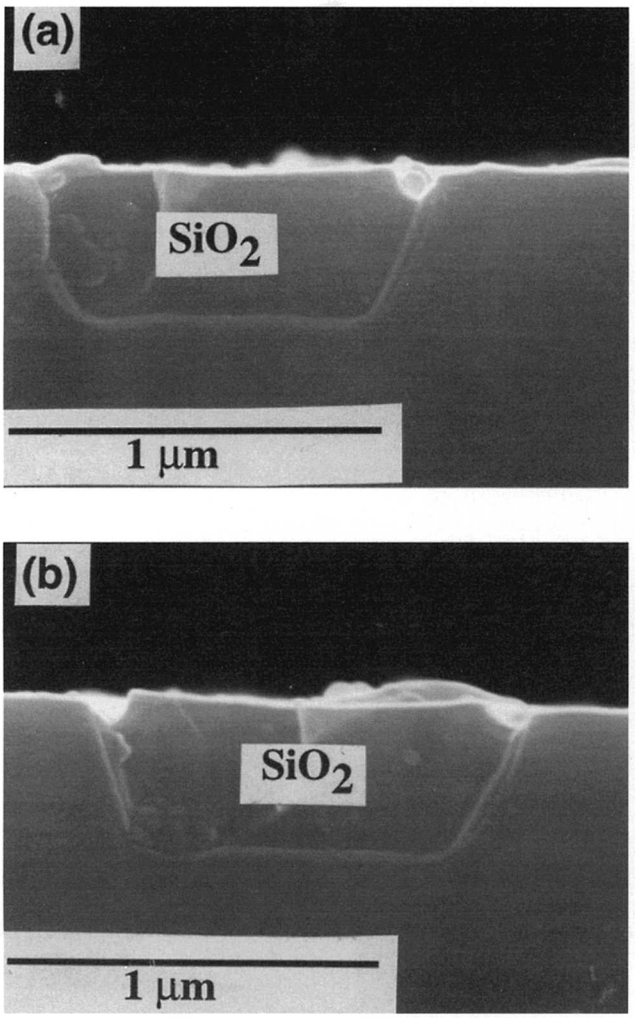

Fig. 5. SEM micrographs of oxide-filled shallow trenches (a) after the novel planarization and (b) after the CMP-only process.

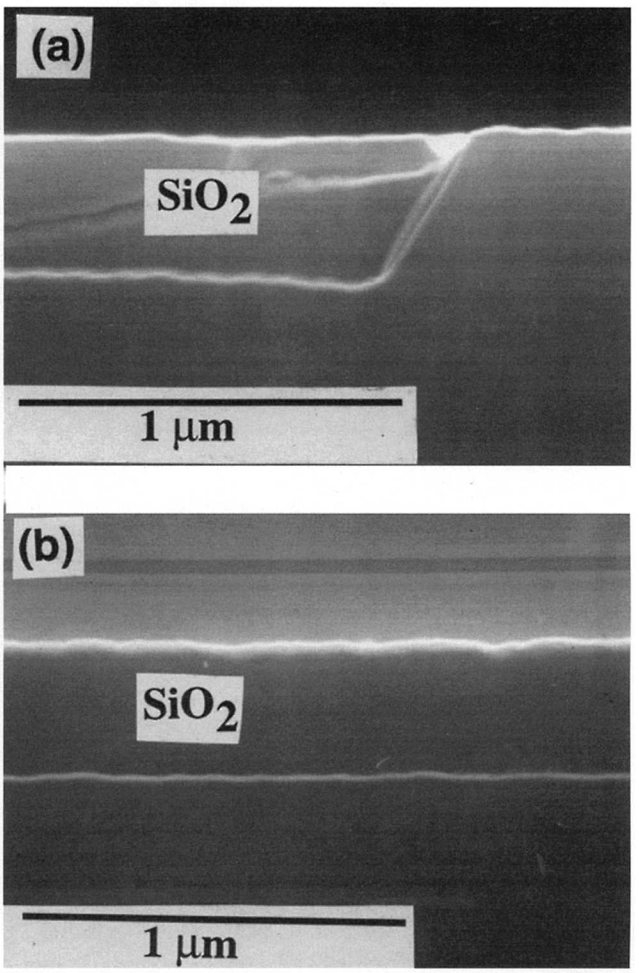

Fig. 6. SEM micrographs of 2 mm wide field region of oxide-filled shallow trenches using the novel planarization (a) in the adjacent active area and (b) 1 mm away from the edge of the large structure.

Figure 8 shows the dishing results using the CMP-only process and the novel process. Obviously, the CMP-only process results in dishing effect in wide field regions. This implies that in wide field regions, the reduction in the pressure is less significant due to the elasticity of the pad.[9] This results in a continued polishing of the oxide after the CVD oxide and SiN interface is reached. However, the novel planarization process of oxide-filled trench isolation with variable size and pattern factor can eliminate the dishing effect in wide field regions and achieve fully planar surface.

Figure 9 shows the dishing distribution for 1 and 100 μm wide field regions across 6 in. diameter silicon wafers. The measured points are shown in the inset of Fig. 8. The global deviation of dishing of the novel process is less than 10%. Therefore, the novel planarization process of oxide-filled shallow trenches considered in this work can achieve an excellent uniformity because the oxide refill underwent polishing only for a short time. Moreover, to form the masking polysilicon layer and remove it by the CMP processes is well controlled and will not influence the surface topography and uniformity due to high etching selectivity of polysilicon to oxide and SiN with slurry A.

Gate oxide breakdown field histograms of metal oxide semiconductor (MOS) capacitors with the novel planarization process considered in this work and the conventional CMP-only process are shown in Fig. 10. The high breakdown yield of the novel planarization process demonstrates extremely low defect density from this process.

Figure 11 shows the leakage current distribution of the n^+/p junction diodes (area = 0.01 cm^2). Compared to the CMP-only process, the lower leakage current of the n^+/p junction diodes at 3.3 V with the novel planarization process can be achieved. This also implies that low defect density results from the novel process considered in this work.

Conclusions

There is no way to stop oxide etchback. However, high etch selectivity of polysilicon to CVD oxide and SIN can be achieved by using a slurry with a high KOH concentration and large silica particles. Selectivity is pressure dependent. Two planarization approaches of the oxide-filled trench isolation have also been evaluated. The oxide-filled shallow-trench isolation technology based on a CMP-only process is difficult to control and has a poor uniformity. It also results in dishing effect in wide field regions. On the other hand, a novel planarization process is well controlled and can achieve an excellent uniformity and fully planar surface by using a combination of formation of a masking polysilicon layer based on a CMP process, selective wet etching for oxide refill on active regions, short-time CMP process for oxide refill, and RIE etchback. Results also show that the high breakdown yield of the gate oxide and the low leakage current of n^+/p junction diodes with the novel planarization process demonstrate extremely low defect density from this process. This new process is a very promising candidate for oxide-filled shallow-trench isolation.

Acknowledgment

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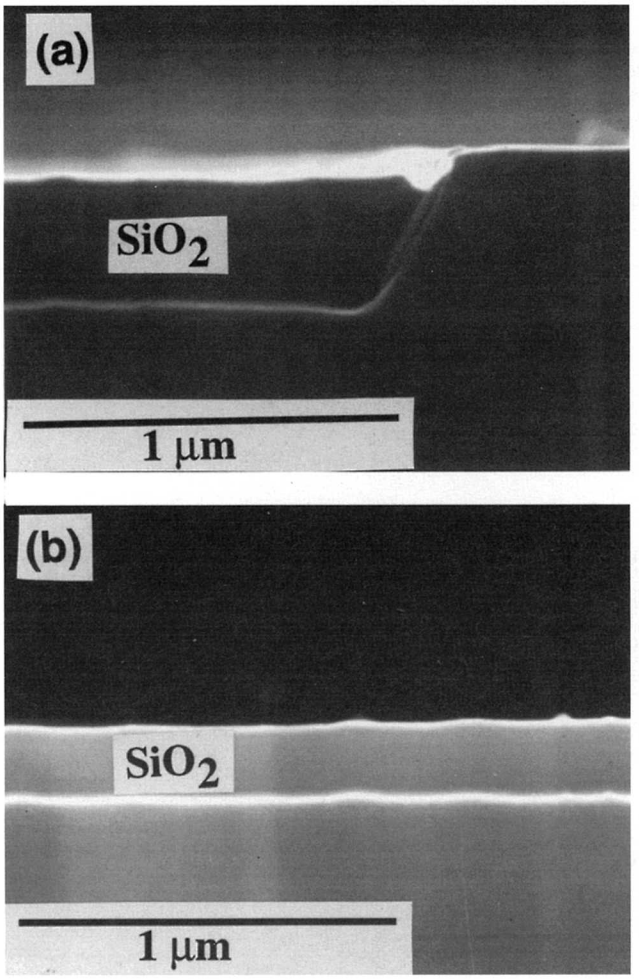

Fig. 7. SEM micrographs of 2 mm wide field region of oxide-filled shallow trenches after a CMP-only process (a) in the adjacent active area and (b) 1 mm away from the edge of the large structure.

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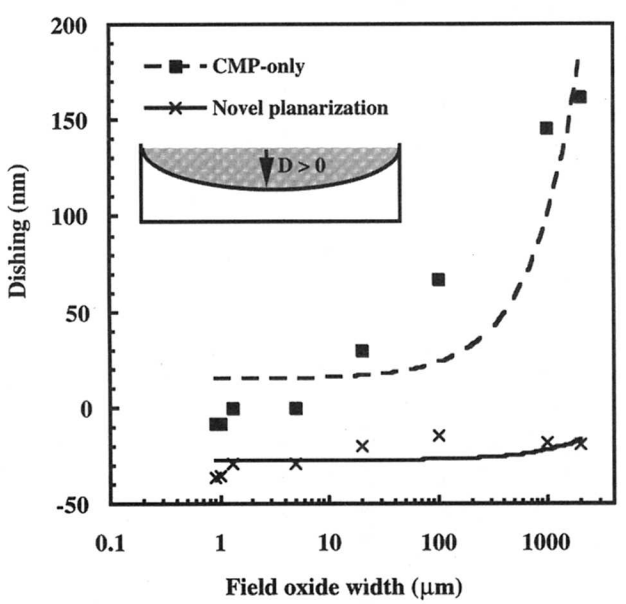

Fig. 8. The dishing results of the oxide-filled trenches after the CMP only process and the novel planarization process.

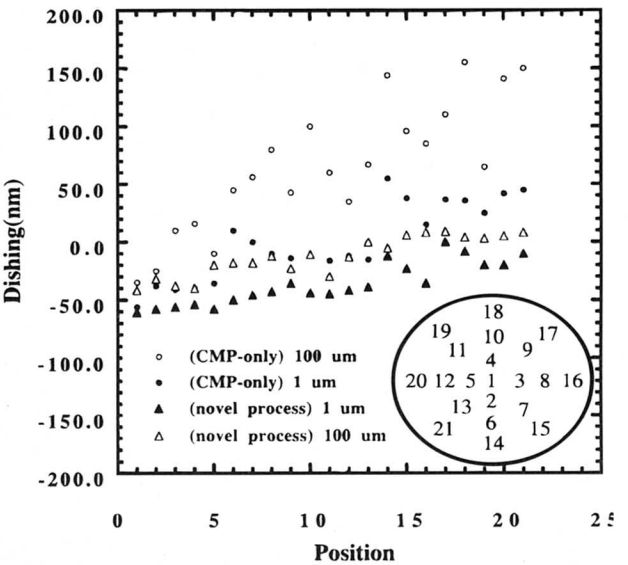

Fig. 9. The dishing distribution for 1 and 100 μm wide field region across 6 in. diam silicon wafers.

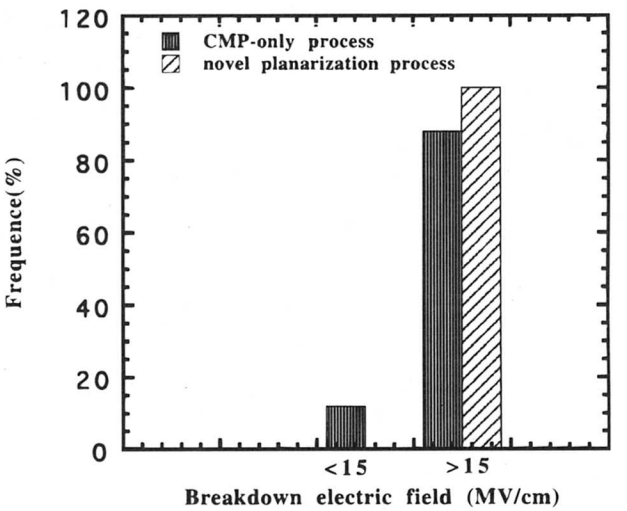

Fig. 10. Gate oxide breakdown field histograms of MOS capacitors with the novel planarization process considered in this work and the conventional CMP-only process.

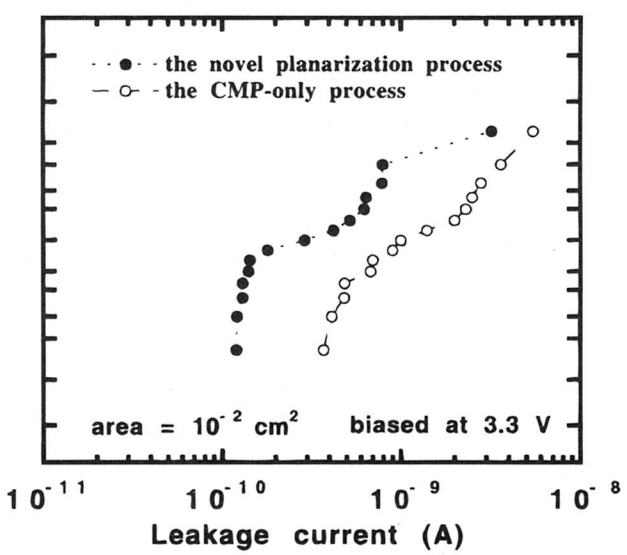

Fig. 11. The leakage current distribution of the n^+/p junction diodes.

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REFERENCES

1. N. Shimizu, Y. Naito, Y. Itoh, Y. Shibata, K. Hashimoto, M. Nishio, A. Asai, K. Ohe, H. Umimoto, and Y. Hirofuji, *IEDM Tech. Dig.*, 279 (1992).
2. D. H. Ahn, S. J. Ahn, P. B. Griffin, M. W. Hwang, W. S. Lee, S. T. Ahn, C. G. Hwang, and M. Y. Lee, *ibid.*, 679 (1994).
3. T. Park, S. J. Ahn, J. H. Ko, C. G. Hong, J. D. Kim, S. T. Ahn, and M. Y. Lee, *ibid.*, 675 (1994).
4. J. M. Sung, C. Y. Lu, L. B. Fritzinger, T. T. Sheng, and K. H. Lee, *IEEE Electron Device Lett.*, **EDL-11**, 549 (1990).
5. T. Kobayashi, S. Nakayama, M. Miyake, and Y. Okazaki, *IEDM Tech. Dig.*, 683 (1994).
6. P. C. Fazan and V. K. Mathews, *ibid.*, 57 (1993).
7. A. Bryant, W. Haensch, S. Geissler, J. Mandelman, D. Poindexter, and M. Steger, *IEEE Electron Device Lett.*, **EDL-14**, 412, (1993).
8. B. Davari, C. W. Koburger, R. Schulz, J. D. Warnock, T. Furukawa, M. Jost, Y. Taur, W. G. Schwittek, J. K. DeBrosse, M. L. Kerbaugh, and J. L. Mauer, *IEDM Tech. Dig.*, 61 (1989).
9. C. Yu, P. C. Fazan, V. K. Mathews, and T. T. Doan, *Appl. Phys. Lett.*, **61**, 14 (1992).
10. H. Inokawa, M. Miyake, S. Nakayama, and T. Kobayashi, *SSDM*, 989 (1994).
11. I. Ali, M. Rodder, S. R. Roy, G. Shinn, and M. I. Raja, *This Journal*, **142**, 3088 (1995).
12. S. Sivaram, H. Bath, R. Leggett, A. Maury, K. Monnig, and R. Tolles, *Solid State Technol.*, 87 (May 1992).
13. C. Fruitman, M. Desai, and D. Devlieger, *VMIC*, 218 (1994).
14. E. D. Palik, V. M. Bermudez, and O. J. Glembocki, *This Journal*, **132**, 135 (1985).

Anomalous Field-Oxide-Ungrowth Phenomenon in Recessed Local Oxidation of Silicon Isolation Structure

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ABSTRACT

An anomalous field-oxide-growth phenomenon in a recessed local oxidation of silicon (LOCOS) structure with a nitride spacer (R-LOCOS), in which the field oxide growth at the center of the opening area is suppressed when isolation spacing is small, is reported. The field-oxide-ungrowth (FOU) phenomenon was found to have strong structural dependence, on the aspect ratio of the opening area, active pattern density, and silicon recess depth. By changing process conditions, such as dry etching and wet cleaning conditions, however, the FOU was not affected. Since the tendency of the FOU occurrence was coincident with that of the microloading effect in reactive ion etching, the FOU was believed to originate from a residue on the exposed silicon surface after the etching process. When silicon was not recessed, the FOU was not observed at any of the structural variations. From a two-dimensional simulation of field oxidation, it has been found that in a nonrecessed LOCOS structure, a residue on the silicon surface does not significantly affect field oxide growth, but in the recessed LOCOS structure, field oxide growth is very sensitive to the existence of a residue on the recessed surface. Thus, to successfully use the recessed LOCOS structure with a subquarter micron design rule avoiding the occurrence of the FOU, structural factors that include an active pattern layout should be carefully chosen.

Introduction

The fast increase of packing density in recent ultralarge scale integration (ULSI) is demanding more tightly controlled device isolation technology. The requirements of the isolation technology at subquarter micron design rule are focused on minimized bird's beak length, planar surface, deep oxide depth, and less field oxide thinning.[1-3] Shallow trench isolation (STI) is the best solution in principle, but the practical problems, such as planarization and sidewall inversion prevent STI from receiving wide acceptance in production.[4,5] Since the recessed silicon in a LOCOS structure can similarly affect STI, it becomes a popular technique in recent isolation technology.[6-8] Although the recessed silicon in LOCOS improves the oxide volume ratio, field oxide thinning, and isolation ability due to deeper oxide depth, the simple addition of recessed silicon in conventional LOCOS structure causes larger bird's beak due to lateral oxidation through the sidewall of the recessed substrate. Thus, the use of spacers at the pad nitride edge to give offset and lateral sealing is inevitable to prevent bird's beak encroachment as long as the silicon substrate is recessed.[7,9] Polysilicon, chemical vapor deposition (CVD) oxide, and nitride have been examined as candidate material for the spacer, and many results showed that nitride was the most effective for the lateral sealing.[3,7,10,11] Thus, the recessed LOCOS structure with nitride spacer (which we call the R-LOCOS structure) is believed to be a strong candidate for subquarter micron design rule isolation structure.

In this study, our experiments are focused on field oxide growing at R-LOCOS structure, and we report an anomalous phenomenon which is found only at very small isolation spacing.

R-LOCOS Process

The process sequence of the R-LOCOS structure is illustrated in Fig. 1. A thin thermal oxide is first grown as the pad oxide and followed by LPCVD nitride deposition as the pad nitride. The nitride and oxide stack is etched down along the photoresist mask. After stripping the photoresist, wafers are immersed into dilute HF solution to etch off the pad oxide completely in the open areas. Subsequently, a thin low pressure CVD (LPCVD) nitride film is deposited to cover the entire surface. The nitride spacer is formed by reactive ion etching (RIE) etching the thin nitride film as shown in Fig. 1c using $CF_4/CHF_3/Ar$ chemistry with a pressure of 220 mTorr and an RF power of 1000 W. Afterward, the silicon substrate is "recessed" by etching in an inductively coupled plasma as shown in Fig. 1d using Cl_2/N_2 chemistry with a power of 50 mTorr, a bias power of 80 W, and a source power of 380 W. In this experiment, the thicknesses of the thin nitride film and the overetch target of the nitride spacer etch are in the range of 300 to 500 Å and 40 ~ 100%, respectively. The recess depth of silicon is in the range of 300 to 500 Å. After silicon etching, the remaining nitride thickness nonuniformity in the active area is less than 10% over 8 in. wafers (5% caused from nitride deposition and 5% from dry etching).

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