Sensitivity of Gate-All-Around Nanowire MOSFETs to Process Variations—A Comparison With Multigate MOSFETs

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***Abstract*—This paper investigates the sensitivity of gate-all-around (GAA) nanowire (NW) to process variations compared with multigate devices using analytical solutions of Poisson's equation verified with device simulation. GAA NW and multigate devices with both heavily doped and lightly doped channels have been examined regarding their immunity to process-induced variations and dopant number fluctuation. Our study indicates that the lightly doped GAA NW has the smallest threshold voltage ($V_{\rm th}$) dispersion caused by process variations and dopant number fluctuation. Specifically, the GAA NW shows better immunity to channel thickness variation than multigate devices because of its inherently superior surrounding gate structure. For heavily doped devices, dopant number fluctuation may become the dominant factor in the determination of overall $V_{\rm th}$ variation. The $V_{\rm th}$ dispersion of GAA NW may therefore be larger than that of multigate MOSFETs because of its larger surface-to-volume ratio.**

***Index Terms*—FinFET, gate-all-around (GAA), multigate MOSFETs, nanowire (NW), trigate, variation.**

I. Introduction

DUE TO their better gate control, the multigate structure [1]–[3] and gate-all-around (GAA) nanowire (NW) [4]–[6] are considered important candidates for future CMOS scaling. The GAA NW features the surrounding gate channel, which is an ideal structure to provide better gate control. However, with the scaling of device geometry, the impact of process variations has become a crucial issue to device design. Although the GAA NW is a promising alternative for future device scaling, its immunity to process variations remains an important question. Wang *et al.* [7] suggested that the NW structure may have larger performance variations than the double-gate FinFET structure. Wang *et al.* [8] also concluded that process fluctuations will severely impact NW device characteristics. However, Paul *et al.* [9] showed that the NW device is less sensitive to process-induced variations as compared with the FinFET device. Whether there is an optimum choice between the NW MOSFET and FinFET merits further examination. In this paper, we assess the sensitivity of GAA NW to process variations compared with multigate MOSFETs using theoretical calculation. A theoretical framework that can be used to assess the feasibility of GAA NW and multigate devices [10] by tackling their electrostatic integrities and sensitivities to process variations will be provided.

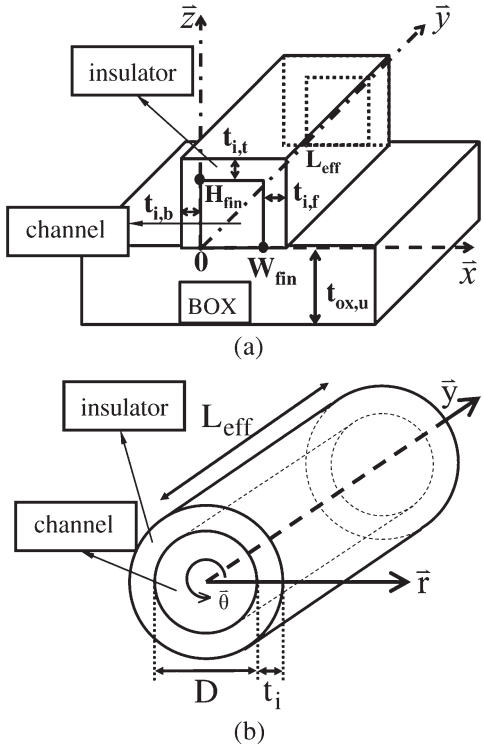

Fig. 1. Schematic sketch of the (a) multigate structure and (b) cylindrical GAA NW structure investigated in this paper. For the cylindrical GAA NW, the origin ($r = 0$ and $y = 0$) is defined at the center of the channel/source junction.

This paper is organized as follows. In Section II, we derive the subthreshold current model for the GAA NW and multigate structure, respectively. The threshold voltage ($V_{\rm th}$) can then be determined based on the calculated subthreshold current. In Section III, we investigate the $V_{\rm th}$ sensitivity to process variations for the GAA NW compared with that of multigate devices based on our theoretical calculation. The conclusions will be drawn in Section IV.

II. Subthreshold Current and $V_{\rm th}$ Calculation

Fig. 1(a) and (b) shows the schematic sketch of the multigate SOI structure and the cylindrical GAA NW, respectively. For

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the multigate structure, the Si-fin body covered by a gate insulator is a cuboid with six faces, and each face is connected to a voltage bias. For the cylindrical GAA NW, the cylindrical channel is wrapped by a gate insulator and is connected to the gate terminal. The front and back faces are connected to the source and drain.

An analytical potential solution is crucial to the derivation of subthreshold characteristics such as subthreshold current and $V_{\rm th}$. The channel potential solutions for the multigate structure and the cylindrical GAA NW are described as follows.

A. Potential Solution for the Multigate Structure

In the subthreshold regime, the Si-channel is fully depleted with negligible mobile carriers. Therefore, the potential distribution $\phi(x,y,z)$ satisfies Poisson's equation

$$\frac{\partial^2\phi(x,y,z)}{\partial x^2}+\frac{\partial^2\phi(x,y,z)}{\partial y^2}+\frac{\partial^2\phi(x,y,z)}{\partial z^2}=-\frac{qN_a}{\varepsilon_{\rm si}} \quad (1)$$

where N_a is the doping concentration of the Si-fin. Under the same boundary conditions as described in our previous work [10], the potential solution of the 3-D boundary value problem can be expressed as $\phi=\phi_1+\phi_2+\phi_3$

$$\phi_1(z) = -\frac{qN_a}{2\varepsilon_{\rm si}}z^2+az+b \quad (2a)$$

$$\phi_2(x,z) = \sum_i\left[c_i\sinh\left(\frac{i\pi}{H_{\rm eff}}\left(x+\frac{\varepsilon_{\rm si}}{\varepsilon_i}t_{i,b}\right)\right) + c_i'\sinh\left(\frac{i\pi}{H_{\rm eff}}\left(W_{\rm eff}-\left(x+\frac{\varepsilon_{\rm si}}{\varepsilon_i}t_{i,b}\right)\right)\right)\right] \cdot\sin\left(\frac{i\pi}{H_{\rm eff}}(z+t_{{\rm ox},u})\right) \quad (2b)$$

$$\phi_3(x,y,z) = \sum_m\sum_n\left[e_{m,n}\sinh(k_y y)+e'_{m,n}\sinh\left(k_y(L_{\rm eff}-y)\right)\right] \cdot\sin\left(\frac{m\pi}{W_{\rm eff}}\left(x+\frac{\varepsilon_{\rm si}}{\varepsilon_i}t_{i,b}\right)\right)\cdot\sin\left(\frac{n\pi}{H_{\rm eff}}(z+t_{{\rm ox},u})\right) \quad (2c)$$

where $\varepsilon_{\rm si}$, ε_i, and ε_{ox} are the dielectric constants of the Si-channel, gate dielectric, and buried oxide, respectively. $W_{\rm fin}$, $H_{\rm fin}$, and $L_{\rm eff}$ are defined as the fin width, fin height, and channel length, respectively. $t_{i,t}$, $t_{i,f}$, $t_{i,b}$, and $t_{{\rm ox},u}$ are the thicknesses of the top gate dielectric, front gate dielectric, back gate dielectric, and buried oxide, respectively.

B. Potential Solution for the Cylindrical GAA NW

For the cylindrical GAA NW, the device structure in this paper is symmetrical in the θ-direction [Fig. 1(b)], and the potential distribution $\phi(r,y)$ satisfies Poisson's equation

$$\frac{\partial^2\phi(r,y)}{\partial r^2}+\frac{1}{r}\frac{\partial\phi(r,y)}{\partial r}\frac{\partial^2\phi(r,y)}{\partial y^2}=-\frac{qN_a}{\varepsilon_{\rm si}} \quad (3)$$

$$\left.\frac{\partial^2\phi(r,y)}{\partial r}\right|_{r=0}=0 \quad (4a)$$

$$\varepsilon_{\rm si}\left.\frac{\partial\phi(r,y)}{\partial r}\right|_{r=D/2}=C_i\cdot[V_{\rm GS}-V_{\rm fb}-\phi(r=D/2,y)] \quad (4b)$$

$$C_i=2\varepsilon_i/(D\cdot\ln(1+2t_i/D)) \quad (4c)$$

$$\phi(r,y=0)=-\phi_{\rm ms} \quad (4d)$$

$$\phi(r,y=L_{\rm eff})=V_{\rm DS}-\phi_{\rm ms} \quad (4e)$$

where D and t_i are the channel diameter and thickness of the gate insulator, respectively. $V_{\rm GS}$ is the voltage bias of the gate terminal. Note that (4c) is the capacitance per unit length for an infinitely long cylindrical capacitor, which neglects the fringing effect of the field near the edges of the capacitor [11].

Similarly, this 2-D boundary value problem can be divided into two subproblems, including 1-D Poisson's equation and 2-D Laplace equation. Using the superposition principle, the complete potential solution is $\phi=\phi_1+\phi_2$, where ϕ_1 and ϕ_2 are solutions of the 1- and 2-D subproblems, respectively. Solving the boundary value problem in the cylindrical coordinate [12], the solution can be expressed as

$$\phi_1(r)=Ar^2+B \quad (5a)$$

where

$$A=-\frac{qN_a}{4\varepsilon_{\rm si}} \quad (5b)$$

$$B=V_{\rm GS}-V_{\rm fb}+\frac{qN_a}{\varepsilon_{\rm si}}\frac{D}{2}\left(\frac{D}{2}+2\frac{\varepsilon_{\rm si}}{C_i}\right) \quad (5c)$$

$$\phi_2(r,z)=\sum_n[k_n\cdot\sinh(\lambda_n\cdot y)+k'_n\cdot\sinh\left(\lambda_n(L_{\rm eff}-y)\right)]\cdot J_0(\lambda_n\cdot r) \quad (6)$$

where $J_\nu(x)$ is called the Bessel function of the first kind of order ν [12]. λ_n can be determined by

$$J_0\left(\lambda_n\frac{D}{2}\right)-\frac{\varepsilon_{\rm si}}{C_i}\lambda_n J_1\left(\lambda_n\frac{D}{2}\right)=0. \quad (7)$$

The coefficients k_n and k'_n can be expressed as

$$k_n=\frac{2}{\left[\left(\frac{C_i}{\lambda_n\varepsilon_{\rm si}}\right)^2+1\right]\cdot J_0^2\left(\lambda_n\frac{D}{2}\right)\cdot\sinh\left(\lambda_n L_{\rm eff}\right)} \cdot\left\{-A\cdot\left[\frac{1}{\lambda_n}\left(\frac{D}{2}\right)^3\cdot J_1\left(\lambda_n\frac{D}{2}\right) -2\left(\frac{1}{\lambda_n}\right)^2\left(\frac{D}{2}\right)^2\cdot J_2\left(\lambda_n\frac{D}{2}\right)\right] +(V_{\rm DS}-\phi_{\rm ms}-B)\frac{1}{\lambda_n}\frac{D}{2}\cdot J_1\left(\lambda_n\frac{D}{2}\right)\right\} \quad (8a)$$

$$k_n' = \frac{2}{\left[\left(\frac{C_i}{\lambda_n \varepsilon_{\rm si}}\right)^2 + 1\right] \cdot J_0^2\left(\lambda_n \frac{D}{2}\right) \cdot \sinh(\lambda_n L_{\rm eff}) \cdot \left\{ -A \cdot \left[\frac{1}{\lambda_n}\left(\frac{D}{2}\right)^3 \cdot J_1\left(\lambda_n \frac{D}{2}\right) - 2\left(\frac{1}{\lambda_n}\right)^2 \left(\frac{D}{2}\right)^2 \cdot J_2\left(\lambda_n \frac{D}{2}\right)\right] + (-\phi_{\rm ms} - B)\frac{1}{\lambda_n}\frac{D}{2} \cdot J_1\left(\lambda_n \frac{D}{2}\right)\right\}}. \quad (8b)$$

C. Subthreshold Current Calculation and Verification

Using the channel potential solution, the subthreshold current can be calculated by [13]

$$I_{\rm DS} = \frac{q\mu_n(kT/q)\left(n_i^2/N_a\right)\left[1-\exp\left(-V_{\rm DS}/(kT/q)\right)\right]}{P}. \quad (9a)$$

The denominator P in (9a) depends on the device structure and channel potential distribution. For multigate MOSFETs, P is calculated using the channel potential $\phi(x, y, z)$ for the multigate structure

$$P = \int_0^{L_{\rm eff}} \frac{dy}{\int_0^{H_{\rm fin}} \int_0^{W_{\rm fin}} \exp\left[q\phi(x, y, z)/(kT)\right] dxdz}. \quad (9b)$$

For the cylindrical GAA NW, P is calculated using the channel potential $\phi(r, y)$

$$P = \int_0^{L_{\rm eff}} \frac{dy}{2\pi \int_0^{D/2} r \cdot \exp\left[q\phi(r, y)/(kT)\right] dr}. \quad (9c)$$

The subthreshold current derived by (9) has been verified by 3-D device simulation [14]. Fig. 2(a) and (b) compares the derived subthreshold current with device simulation for heavily doped and lightly doped devices, respectively. Note that a smaller equivalent oxide thickness is used in the lightly doped case to sustain the electrostatic integrity [2]. In addition, we define the $V_{\rm th}$ as the gate voltage at which the calculated subthreshold current $I_{\rm DS} = 300\ {\rm nA} \times W_{\rm total}/L_{\rm eff}$ [15], where $W_{\rm total}$ is the total width. For the multigate structure, $W_{\rm total} = 2H_{\rm fin} + W_{\rm fin}$, and for the GAA NW, $W_{\rm total} = \pi \cdot D$. Since our calculated subthreshold current is applicable for the subthreshold regime, we focus on the accuracy for $V_{\rm GS}$ below $V_{\rm th}$. For heavily doped devices [Fig. 2(a)], the $V_{\rm th}$ is around 0.4 V, and for lightly doped devices [Fig. 2(b)], the $V_{\rm th}$ is around 0.2 V. It can be seen that our model shows satisfactory accuracy.

Compared with technology computer-aided design (TCAD) device simulation, our methodology shows higher efficiency in determining the subthreshold current and $V_{\rm th}$ of the multigate structure and GAA NW. In our calculation, the CPU time needed is less than 20% of that needed for TCAD simulation. More importantly, this theoretical framework provides more scalable and predictive results than experimental or TCAD simulation does.

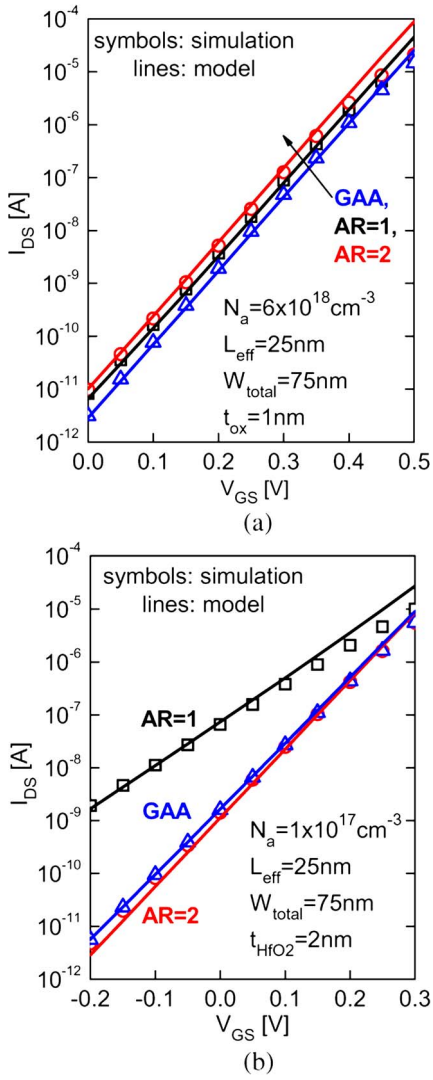

Fig. 2. Calculated subthreshold current compared with the result of 3-D device simulation. (a) Heavily doped channel. (b) Lightly doped channel with high-k dielectric (the dielectric constant of HfO_2 is 25). A midgap workfunction is given for both heavily and lightly doped devices (4.5 eV).

III. Sensitivity of GAA NW to Process Variations

To assess the sensitivity of GAA NW and multigate MOSFETs to process variations, we assume that the device parameters such as channel length $(L_{\rm eff})$, channel diameter (D) of GAA NW, and fin width $(W_{\rm fin})$ of multigate MOSFETs vary by ± 2.5 nm ($\pm 3\sigma$ value, with σ being the standard deviation) [16]. This 3σ value is estimated from the combination of process variations such as lithography variation, etch variation, and resist trim variation [16]. In addition, the impact of dopant number fluctuation is crucial to $V_{\rm th}$ variation of heavily doped devices. In this paper, we assess the $V_{\rm th}$ sensitivity to dopant number fluctuation using our analytical $V_{\rm th}$ model. We assume that the channel dopant number follows the Poisson distribution [17] and that the σ of the dopant number is $n_a^{1/2}$, where n_a is the average dopant number in the Si-channel. The corresponding $V_{\rm th}$ variation for process variations and dopant number fluctuation can be calculated as $\Delta V_{\rm th} = [V_{\rm th}(+3\sigma) - V_{\rm th}(-3\sigma)]/2$ [17].

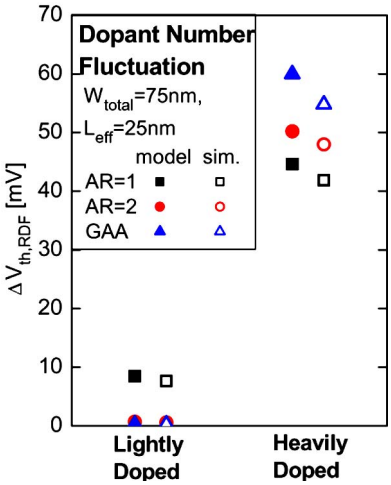

Fig. 3. Comparison of $\Delta V_{\rm th}$ caused by dopant number fluctuation ($\Delta V_{\rm th,RDF}$) between GAA NW and multigate MOSFETs (AR = 1 and 2). Both heavily doped and lightly doped channels are considered.

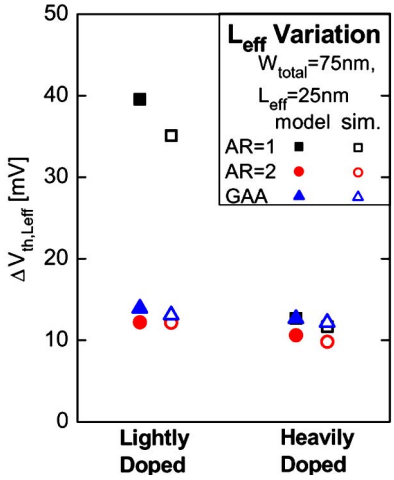

Fig. 4. Comparison of $\Delta V_{\rm th}$ caused by $L_{\rm eff}$ variation ($\Delta V_{\rm th,Leff}$) between GAA NW and multigate MOSFETs (AR = 1 and 2).

To compare the GAA NW with multigate MOSFETs, the total widths ($W_{\rm total}$) of GAA NW ($W_{\rm total} = \pi \cdot D$) and multigate MOSFETs ($W_{\rm total} = 2H_{\rm fin} + W_{\rm fin}$) are equal to make fair comparison. Multigate structures with various ARs ($\mathrm{AR} = H_{\rm fin}/W_{\rm fin}$) are considered, including FinFET (AR = 2) and trigate (AR = 1) [10]. Devices with various channel dopings are considered in this paper. For heavily doped devices, the channel doping is equal to 6×10^{18} cm^{-3}. For lightly doped devices, the channel doping is equal to 1×10^{17} cm^{-3}. Moreover, gate oxide ($t_{\rm ox} = 1$ nm) is used for heavily doped devices, while high-k dielectric ($t_{\rm HfO2} = 2$ nm, and the dielectric constant of HfO_2 is 25) is used for lightly doped ones to sustain the device electrostatics [2].

Fig. 3 shows the calculated $\Delta V_{\rm th}$ caused by dopant number fluctuation ($\Delta V_{\rm th,RDF}$) for $W_{\rm total} = 75$ nm and $L_{\rm eff} = 25$ nm, and the results are verified with device simulation [14]. The $\Delta V_{\rm th,RDF}$ for GAA NW MOSFETs is larger than that for multigate MOSFETs. This is because, for a given total width, the GAA NW possesses smaller channel volume than FinFET and trigate. Furthermore, it can be seen that for heavily doped channels, the $\Delta V_{\rm th,RDF}$ is significantly larger than that for lightly doped ones. The $V_{\rm th}$ dispersion due to dopant number fluctuation is a crucial concern for heavily doped device design.

Fig. 4 shows the calculated $\Delta V_{\rm th}$ caused by $L_{\rm eff}$ variation ($\Delta V_{\rm th,Leff}$) for $W_{\rm total} = 75$ nm and $L_{\rm eff} = 25$ nm. The discrepancies of $\Delta V_{\rm th,Leff}$ for heavily doped devices are not significant. For lightly doped channels, the $\Delta V_{\rm th,Leff}$ of GAA NW is also close to that of FinFET. However, the $\Delta V_{\rm th,Leff}$ of GAA NW is much smaller than that of trigate. The $\Delta V_{\rm th,Leff}$ is determined by $V_{\rm th}$ roll-off characteristics. Fig. 5(a) shows that for the heavily doped channel, the $V_{\rm th}$ roll-off characteristics of the three devices are similar because channel doping reduces the geometry dependence of electrostatic integrity. In Fig. 5(b), the $V_{\rm th}$ roll-off characteristic of the lightly doped GAA MOSFET is close to that of the lightly doped FinFET.

Fig. 6 shows the calculated $\Delta V_{\rm th}$ caused by channel thickness ($t_{\rm si}$) variation ($\Delta V_{\rm th,tsi}$) for $W_{\rm total} = 75$ nm and $L_{\rm eff} = 25$ nm. $W_{\rm fin}$ and diameter variations are considered for multigate MOSFETs and GAA NW, respectively. It can be seen that

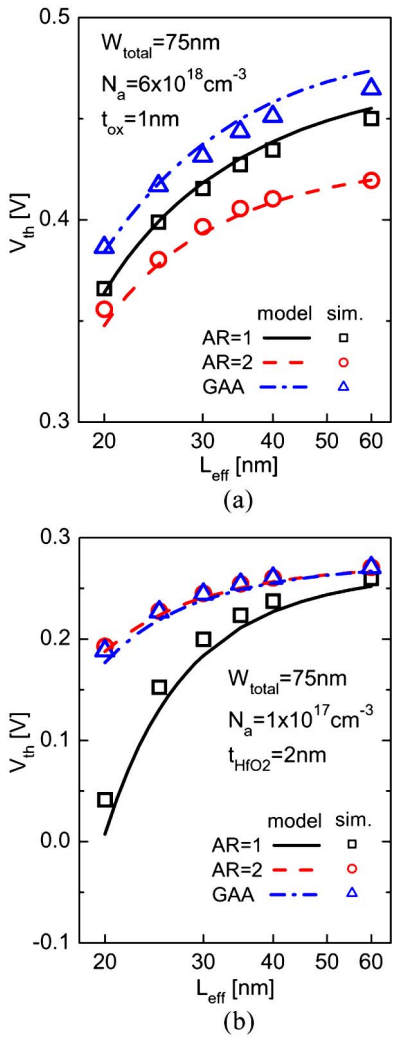

Fig. 5. $V_{\rm th}$ roll-off behaviors of GAA NW and multigate MOSFETs (AR = 1 and 2). (a) Heavily doped channel. (b) Lightly doped channel with high-k dielectric.

for the lightly doped channel, the $\Delta V_{\rm th,tsi}$ of GAA NW is smaller than that of multigate MOSFETs. This is because the surrounding gate structure of GAA NW reduces the channel

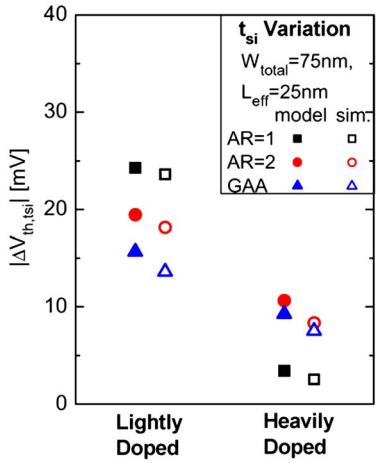

Fig. 6. Comparison of $\Delta V_{\rm th}$ caused by channel thickness ($t_{\rm si}$) variation ($\Delta V_{\rm th,tsi}$) between GAA NW and multigate MOSFETs (AR = 1 and 2). $W_{\rm fin}$ variation and diameter variation are considered for multigate MOSFETs and GAA NW, respectively.

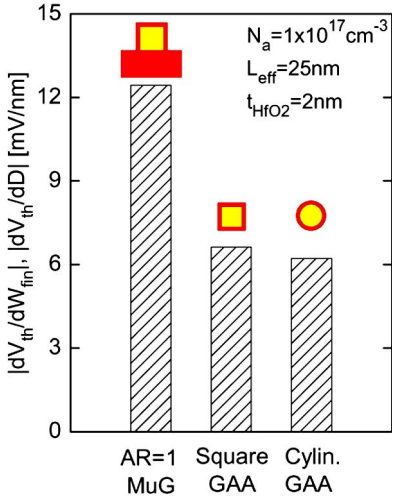

Fig. 7. Comparison of $V_{\rm th}$ sensitivity to channel thickness for trigate (AR = 1), GAA structure with a square cross section, and cylindrical GAA NW.

thickness dependence of $V_{\rm th}$. Fig. 7 shows that the GAA structure with a square cross section (which possesses the same channel volume as the cylindrical GAA structure) shows similar $V_{\rm th}$ sensitivity ($dV_{\rm th}/dW_{\rm fin}$) as that ($dV_{\rm th}/dD$) of the cylindrical GAA structure. Although multigate structures with higher AR can be used to improve the immunity to $W_{\rm fin}$ variation, Fig. 8 shows that with the scaling of $W_{\rm total}$, the $\Delta V_{\rm th,tsi}$ of GAA NW decreases more rapidly than that of FinFET.

To assess the overall $V_{\rm th}$ variation ($\Delta V_{\rm th,total}$) for GAA NW and multigate devices, we assume that variation sources such as dopant number fluctuation, $L_{\rm eff}$ variation, and channel thickness variation are independent. The overall $V_{\rm th}$ variation can then be calculated as $\Delta V^2_{\rm th,total} = \Delta V^2_{\rm th,RDF} + \Delta V^2_{\rm th,Leff} + \Delta V^2_{\rm th,tsi}$. Fig. 9 compares the calculated $\Delta V^2_{\rm th,total}$ of GAA NW and AR = 2 FinFET for $W_{\rm total}$ = 75 nm and $L_{\rm eff}$ = 25 nm. For the heavily doped channel, dopant number fluctuation dominates the overall $V_{\rm th}$ dispersion, and the $\Delta V_{\rm th,total}$ of GAA NW is larger than that of FinFET because of its smaller channel volume. For the lightly doped channel, process-induced

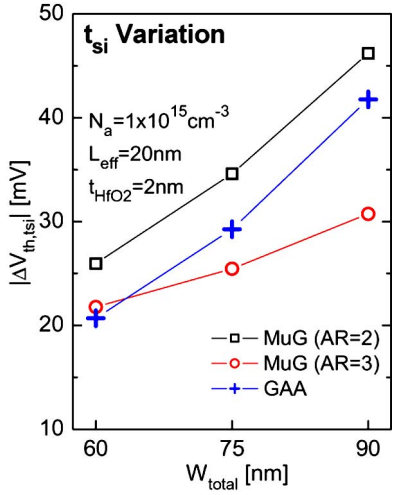

Fig. 8. Model prediction of $\Delta V_{\rm th,tsi}$ dependence on total width ($W_{\rm total}$) for lightly doped GAA NW and FinFET (AR = 2 and AR = 3).

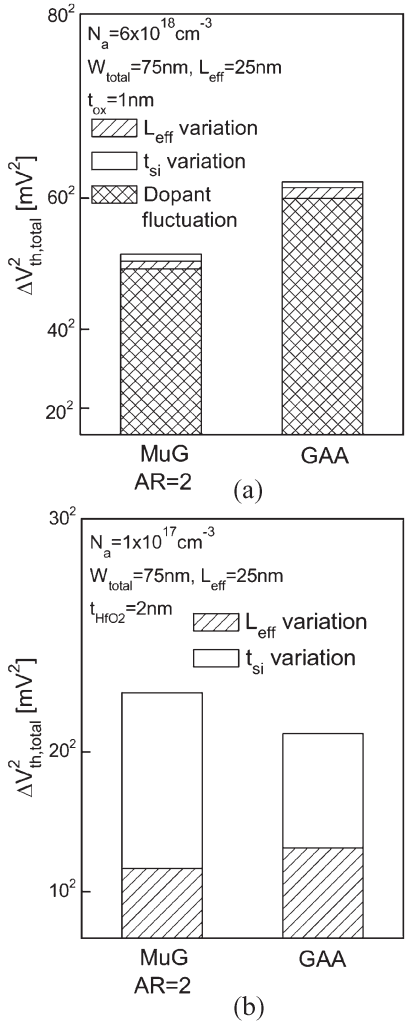

Fig. 9. Comparison of square of overall $V_{\rm th}$ variation ($\Delta V^2_{\rm th,total}$) between GAA NW and AR = 2 FinFET. (a) Heavily doped channel. (b) Lightly doped channel with high-k dielectric.

geometry variations dominate the overall $V_{\rm th}$ dispersion, and the $\Delta V_{\rm th,total}$ of GAA NW is smaller than that of FinFET because of its better immunity to channel thickness variation.

One key physical effect neglected in our analysis is the quantum–mechanical effect [18], [19]. Although the field confinement in the inversion layer may be significant for heavily doped devices, our comparison regarding $V_{\rm th}$ dispersion between GAA NW and multigate devices is basically valid. This is because the overall $V_{\rm th}$ dispersion for heavily doped devices is dominated by dopant number fluctuation, which is mainly determined by the channel volume. For lightly doped devices, the surface electric field is not strong in the subthreshold regime, and the field confinement may be neglected. However, when the channel thickness is below 10 nm, the structural confinement becomes significant for lightly doped devices [20], [21] and has to be considered by self-consistent solution of Poisson and Schrödinger equations.

IV. Conclusion

We have compared the sensitivity of GAA NW to process variations with multigate structures using analytical solutions of 3-D Poisson's equation verified with device simulation. The lightly doped GAA NW shows the smallest $V_{\rm th}$ variation caused by process variation and dopant number fluctuation. In particular, the GAA NW shows better immunity to channel thickness variation than the multigate structure because of its inherently superior surrounding gate structure. For heavily doped devices, dopant number fluctuation may become the dominant factor in the determination of overall $V_{\rm th}$ variation. The $V_{\rm th}$ dispersion of GAA NW may therefore be larger than that of multigate MOSFETs because of its larger surface-to-volume ratio.

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References

[1] O. Faynot, G. Barna, R. Ritzenthaler, and P. Gidon, "Scaling of multiple-gate fully depleted SOI transistors," in *Proc. Int. Conf. Solid State Devices Mater.*, Sep. 2004, pp. 764–765.

[2] J. Kavalieros, B. Doyle, S. Datta, G. Dewey, M. Doczy, B. Jin, D. Lionberger, M. Metz, W. Rachmady, M. Radosavljevic, U. Shah, N. Zelick, and R. Chau, "Tri-gate transistor architecture with high-k gate dielectrics, metal gates and strain engineering," in *VLSI Symp. Tech. Dig.*, Jun. 2006, pp. 50–51.

[3] M. J. H. van Dal, N. Collaert, G. Doombos, G. Vellianitis, G. Curatola, B. J. Pawlak, R. Duffy, C. Jonville, B. Degroote, E. Altamirano, E. Kunnen, M. Demand, S. Beckx, T. Vandeweyer, C. Delvaux, F. Leys, A. Hikavyy, R. Rooyackers, M. Kaiser, R. G. R. Weemaes, S. Biesemans, M. Jurczak, K. Anil, L. Witters, and R. J. P. Lander, "Highly manufacturable FinFETs with sub-10 nm fin width and high aspect ratio fabricated with immersion lithography," in *VLSI Symp. Tech. Dig.*, Jun. 2007, p. 7A-3.

[4] F. L. Yang, D. H. Lee, H. Y. Chen, C. Y. Chang, S. D. Liu, C.C. Huang, T. X. Chung, H. W. Chen, C. C. Huang, Y. H. Liu, C. C. Wu, C. C. Chen, S. C. Chen, Y. T. Chen, Y. H. Chen, C. J. Chen, B. W. Chan, P. F. Hsu, J. H. Shieh, H. J. Tao, Y. C. Yeo, Y. Li, J. W. Lee, P. Chen, M. S. Liang, and C. Hu, "5 nm-gate nanowire FinFET," in *VLSI Symp. Tech. Dig.*, Jun. 2004, pp. 196–197.

[5] S. D. Suk, S. Y. Lee, S. M. Kim, E. J. Yoon, M. S. Kim, M. Li, C. W. Oh, K. H. Yeo, S. H. Kim, D. S. Shin, and K. H. Lee, "High performance 5 nm radius twin silicon nanowire MOSFET (TSNWFET): Fabrication on bulk Si wafer, characteristics, and reliability," in *IEDM Tech. Dig.*, 2005, pp. 717–720.

[6] N. Singh, A. Agarwal, L. K. Bera, T. Y. Liow, R. Yang, S. C. Rustagi, C. H. Tung, R. Kumar, G. Q. Lo, N. Balasubramanian, and D. L. Kwong, "High-performance fully depleted silicon nanowire (diameter $\leq$ 5 nm) gate-all-around CMOS devices," *IEEE Electron Device Lett.*, vol. 27, no. 5, pp. 383–386, May 2006.

[7] J. Wang, E. Polizzi, and M. Lundstrom, "A computational study of ballistic silicon nanowire transistors," in *IEDM Tech. Dig.*, 2003, pp. 29.5.1–29.5.4.

[8] R. Wang, J. Zhuge, R. Huang, Y. Tian, H. Xiao, L. Zhang, C. Li, X. Zhang, and Y. Wang, "Analog/RF performance of Si nanowire MOSFETs and the impact of process variation," *IEEE Trans. Electron Devices*, vol. 54, no. 6, pp. 1288–1294, Jun. 2007.

[9] B. Paul, S. Fujita, M. Okajima, T. H. Lee, H. S. P. Wong, and Y. Nishi, "Impact of a process variation on nanowire and nanotube device performance," *IEEE Trans. Electron Devices*, vol. 54, no. 9, pp. 2369–2376, Sep. 2007.

[10] Y. S. Wu and P. Su, "Sensitivity of multigate MOSFETs to process variations—An assessment based on analytical solutions of 3-D Poisson's equation," *IEEE Trans. Nanotechnol.*, vol. 7, no. 3, pp. 299–304, May 2008.

[11] D. K. Cheng, *Field and Wave Electromagnetics*. Reading, MA: Addison-Wesley, 1992.

[12] D. G. Zill and M. R. Cullen, *Differential Equations With Boundary Value Problems*, 5th ed. Pacific Grove, CA: Brooks/Cole, 2001.

[13] X. Liang and Y. Taur, "A 2-D analytical solution for SCEs in DG MOSFETs," *IEEE Trans. Electron Devices*, vol. 51, no. 8, pp. 1385–1391, Aug. 2004.

[14] *ISE TCAD Rel. 10.0 Manual*, Zurich, Switzerland, 2004.

[15] G. Pei, J. Kedzierski, P. Oldiges, M. Ieong, and E. C. Kan, "FinFET design considerations based on 3-D simulation and analytical modeling," *IEEE Trans. Electron Devices*, vol. 49, no. 8, pp. 1411–1419, Aug. 2002.

[16] *International Technology Roadmap for Semiconductors*. [Online]. Available: http://www.itrs.net/

[17] T. Ohtou, N. Sugii, and T. Hiramoto, "Impact of parameter variations and random dopant fluctuations on short-channel fully-depleted SOI MOSFETs with extremely thin BOX," in *Proc. Silicon Nanoelectron. Workshop*, 2006, pp. 15–16. Workshop Abs.

[18] V. P. Trivedi and J. G. Fossum, "Quantum-mechanical effects on the threshold voltage of undoped double-gate MOSFETs," *IEEE Electron Device Lett.*, vol. 26, no. 8, pp. 579–582, Aug. 2005.

[19] M. Shoji and S. Horiguchi, "Electronic structures and phonon-limited electron mobility of double-gate silicon-on-insulator Si inversion layers," *J. Appl. Phys.*, vol. 85, no. 5, pp. 2722–2731, Mar. 1999.

[20] Y. Omura, S. Horiguchi, M. Tabe, and K. Kishi, "Quantum-mechanical effects on the threshold voltage of ultrathin-SOI nMOSFETs," *IEEE Electron Device Lett.*, vol. 14, no. 12, pp. 569–571, Dec. 1993.

[21] J. P. Colinge, J. C. Alderman, W. Xiong, and C. R. Cleavelin, "Quantum-mechanical effects in trigate SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 53, no. 5, pp. 1131–1136, May 2006.

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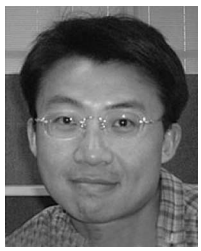

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