Chapter 1 Introduction

1.1 Overview of Thin Film Transistor Liquid Crystal Display (TFT-LCD)

Active matrix liquid crystal displays (AMLCDs) remain the most mature and prevalent technology among various flat panel display applications because of their practically excellent features such as the thinness, light weight, low operation voltage, and of their continuous technological development in full color displays. The technological progresses and applications of AMLCDs have rapid development in recent decades, such as portable computers, projection light valves, and miniature displays, owing to their characteristics including the brightness, viewing angle, low power consumption, and integrated circuit (IC) process compatibility. The cathode ray tubes (CRTs), which had ever played the leading role in display electronics due to their high information content, high resolution, and full color display features. However, CRTs have been completely replaced by LCDs. AMLCDs have penetrated into the desktop monitor market and even took possession of the market of television. Desktop monitor engineering specifications emphasize high visual performance, such as higher resolutions, higher pixel content, wider viewing angle, larger color gamut, higher brightness and a moderate price. Another large area display product, such as HDTV (high definition

television), would underscore lower cost while accepting a lower resolution and lower pixel content display. However, in order to quickly occupy the TV market, several AMLCD makers increase the size of LCD panels rapidly. Table 1-1 and Table 1-2 list the fabrication sizes for the maker's factories of all generation and their large area LCD-TV products.

Even the fabrication cost of passive-matrix is slightly lower than that of active-matrix arrays, it would be important to understand why an active-matrix array design is necessary. Figure 1-1 shows the electrical schematic of an active-matrix. Active-matrix addressing overcomes the half-select passive-matrix crosstalk limitation by integrating switching devices at the cross point of the row (scan or gate) and column (data or video signal) lines, as shown in Figure 1-2, and thereby isolating the off pixel from these select voltage lines. These switching devices consist of either two-terminal or three-terminal devices. The two-terminal device, which passes current one way, is usually a Schottky, *p-i-n* diode. The MIM (metal-insulator-metal) diode allows a bi-directional current passing, and usually composed of insulators like silicon nitride (SiN_x), diamond-like carbon (DLC), or tantalum pentoxide (Ta_2O_5), which deposited by PECVD (plasma-enhanced chemical vapor deposition). The three-terminal array switches are field-effect transistors (FETs), such as crystalline silicon metal oxide-semiconductor field-effect transistors (MOSFETs) or thin-film transistors (TFTs). A TFT is a MOSFET fabricated on an insulating substrate (preferably glass for low cost products) by employing all thin film components. It has all the advantages of a silicon-on-insulator (SOI) device: fabrication simplicity, strong latch-up immunity and possible high packing

density. When TFTs are used in AMLCDs, the semiconductor film of TFT channel is composed of either amorphous Si (a-Si), various degrees of recrystalized a-Si (poly-Si), or II-VI group semiconductors such as CdSe and ZnO, and most recently, even organic materials, such as pentacene, are being considered. The computer simulations are commonly used to optimize the TFT active-matrix array designs and analyze the electrical performance of the TFTs based on statistical extraction of the devices and fabrication process parameters. Since this approach is the most efficient way to predict the statistical mean and variance in display performance, it is more instructive to carry out a simple, physically based parameter analysis to identify functional dependencies, performance limits, and minimum requirements, and this analysis is applicable to any kind of TFT processing technologies. Table 1-3 [1-3] lists the major TFT and AMLCDs design factors. The pixel size, the TFT geometry, and the desired fill factor will determine the amount of parasitic capacitance to the adjacent rows and columns, while the display size and pixel content will dictate the resistance of the row and column lines. The number of rows and the frame time dominate the charging time of the pixel capacitance, including the liquid crystal capacitance and charge retention time. The minimum TFT on-state current determines the number of gray levels to accurately charge up the pixel. The LC mode will dictate the pixel voltage, and the allowable gray bit error rate, along with specifications for flicker, will determine the TFT and pixel off-state current.

TFTs have been intensively researched for possible electronic and display applications. In the early 1960's TFT technology was in

competition with single crystal silicon MOSFET for the integrated circuit field. Due to the rapid progress of the latter and the difficulty in consistently producing good quality devices of the former, TFTs were not successful at that time. However, the application of TFTs to displays was not given up. The first active matrix LCD (AMLCD) was realized in 1973. Figure 1-3 shows (a) the cross-sectional view of the whole panel, (b) the storage capacitor-on-gate line pixel design.

1.2 A Historical Perspective of Thin Film Transistors

The first TFT was demonstrated by P. K. Weimer at RCA Laboratory in 1961 [4] even the concept of a thin film FET was presented as early as 1935 [5]. P. K. Weimer represented the device which would now be called a staggered structure was composed of polycrystalline cadmium sulfide, similar to those developed for photodetectors, and monoxide as insulator films. The amorphous silicon was firstly utilized as active material in TFT reported by LeComber, Spear, and Ghaith in 1979 [6]. It had previously been investigated that the hydrogenated amorphous silicon could be doped with donors or acceptors to induce *n*- or *p*-type conductivity, in contrast to pure amorphous silicon [7]. This suggested that the hydrogenation compensated the dangling bonds in the silicon random networks so that a large density of mid gap states of silicon were passivated. LeComber *et al.* respectively employed Si_3N_4 and silicon deposited by glow-discharge as gate dielectric and active layer, and their devices exhibited on-state current of several microamperes and off-state current of about 1 nA. The TFTs

demonstrated by LeComber *et al.* fitted criteria for driving liquid crystal displays, as published by Brody [8]. From 1940s, device physicists have a preference for elemental materials, such as silicon or germanium. It has been considered that silicon have reproducible properties and is amenable for large area deposition. Besides applied to devices such as transistors and diodes, silicon was also being explored for use in solar cells [9]. Even amorphous silicon has no grain boundaries thus exhibits very low trap densities, and is self-passivating (against bulk silicon), its mobility is much lower than that of polycrystalline CdSe. The properties of polycrystalline CdSe will be influenced by grain size, grain boundary interface trap states, stoichiometry, and it could be sensitive to ambient such as oxygen and H_2O. The first polycrystalline silicon was proposed by Depp *et al.* [10] in IBM in 1980s. The polycrystalline silicon grown by chemical vapor deposition was employed to achieve good electrical performance. With mobility around 50 cm^2/Vs, they obtained ring oscillators with 2 μs delay per stage. These poly-Si TFTs reported by Depp *et al.* required high temperature process, since the gate insulator SiO_2 thermally grown at 1050°C. Therefore, quartz substrates were utilized instead of glass.

By 1982, both of the IBM [11] and Mitsubishi [12] groups used laser recrystallization approach to improve the mobility and threshold voltage of poly-Si TFTs, and an electron mobility of 400 cm^2/Vs was achieved. The motivation for elevating the mobility of the devices was to be able to integrate the driving circuits as well as providing pixel TFTs. In general, the a-Si TFT technology is more advanced and commercial products such as AMLCDs for portable computers are available. However, poly-Si TFTs

are superior to a-Si TFTs in many ways; one of the superiorities is that the former exhibits much higher mobility than that of the latter. As a result, the fabrication of pixel transistors and logic circuits with adequate speed on the same glass substrate become feasible. In addition, the lack of photo-sensitivity and higher stability of poly-Si mean that a light shield is not required. The fabrication process can thus be further simplified. Moreover, the working life of poly-Si devices is longer because of higher bias stress immunity. With all these advantages, poly-Si TFTs can find a much broader area of application than a-Si TFTs. Today TFTs have been intensively researched for possible electronic and display applications, such as static random access memories (SRAMs) [13], electrical erasable programming read only memories (EEPROMs) [14], photodetector amplifier [15], and active matrix liquid crystal displays (AMLCDs) [16-18]. In the more than six decades, TFTs have undergone extensive evolution, development, and refinement.

1.3 Physical Properties of ZnO

ZnO have been extensively investigated for applications to varistors, transparent high-power electronics, UV light emitting diodes, surface acoustic wave devices, and chemical and gas sensors [19-24] recently. Compared with GaN, ZnO has several advantages including larger excition binding energy (~60 meV in contrast to ~25 meV for GaN) [25] and commercial availability of bulk single crystals. The larger excition binding energy of ZnO brings about even bright light emission than that obtained

by GaN photonics. The optical properties of ZnO revealed the intrinsic direct wide band gap, band states arising from point defects, and a strongly bound exciton state by using photoconductivity, photoluminescence, and absorption. The excition binding energy of 60 meV led to the near-band-edge UV photoluminescence peak located at ~3.2 eV at room temperature. Furthermore, the visible emission observed by photoluminescence resulted from crystal defects such as interstitial zinc ions, oxygen vacancies or dislocations.

The single crystals of ZnO could be grown by a number of methods [20], and large size of ZnO substrates are also available [26-28]. High-quality of ZnO thin films could be obtained at a relative low temperature of less than 700°C. Since the exciton binding energy of ZnO is 2.4 times that of the room temperature (RT) thermal energy (k_BT = 25 meV). There have also been numbers of reports demonstrated the laser emission of ZnO-based structures at RT and beyond. The reasonable quality of ZnO could be obtained at much lower deposition temperatures than that of GaN by using techniques of pulsed laser deposition (PLD), molecular beam epitaxy (MBE), or reactive sputtering. This offers the possibility of realizing the ZnO-based devices mentioned above on cheap substrates such as glass. ZnO is a direct band gap semiconductor with E_g = 3.4 eV at room temperature. The band gap energy of ZnO could be tuned via substituting various cation ions into the ZnO lattice. Doping with magnesium could increase the band gap to as high as about 4.0 eV. On the other hand, cadmium doping could reduce the band gap energy. The crystal structure of ZnO is hexagonal (wurtzite), as shown in Figure 1-4, with lattice

parameters of a = 0.325 nm and c = 0.512 nm. The shallow donor levels related to the intrinsic defects laid approximately 0.01 to 0.05 eV below the conduction band which brought about *n*-type behaviors.

Table 1-4 [24] summarizes the basic physical properties of ZnO. In order to demonstrate all types of ZnO-based devices, it is important to control over the carrier concentration, which is strongly responsible for the electrical properties of ZnO. Unlike the single element semiconductors, the carrier concentration of ZnO was not only affected by the extrinsic impurities, called dopants, but also influenced by the intrinsic crystal defects, for instance the interstitial zinc ions and oxygen vacancies. The dopants and intrinsic defects determine whether the majority carriers of the ZnO were electrons and holes. Electron doping in ZnO has been attributed to Zn interstitials, oxygen vacancies, or hydrogen.

Besides the properties of ZnO mentioned above, there are several additional advantages of ZnO such as the compatibility of wet chemical etching photolithography and high energy radiation stability. It has been confirmed that ZnO is easily etched in all acid and alkalis so that it could be fabricated of small size devices. Moreover, ZnO is very resistive to high energy radiation [29-31], and make it a very suitable candidate for space applications. ZnO was also used as substrates for epitaxial growth of GaN films due to its identical crystal structure and close lattice parameters to that of GaN [32-33].

1.4 Motivation

Compared to the silicon-based TFTs mentioned above, ZnO-based TFTs exhibited much higher transparency in visible light wavelength and relative low process temperature, and thus have attracted much attention recently. Most of the ZnO-based TFTs were realized by radio frequency (rf) magnetron sputtering [34-53], ion beam sputtering [54], pulsed laser deposition [55-60], or laser molecular-beam epitaxy (LMBE) [61-62], and the mobility of devices demonstrated among the researches ranged from 0.05 to 70 cm^2/Vs. Besides the deposition methods of ZnO films involving vacuum facilities mentioned above, some studies [63-65] investigated another deposition method, chemical solution deposition (CSD), to fabricate ZnO active channel layers in TFTs. For the device deposition of the large area flat panel display, the CSD process may provide a more efficient way to fabricate device components than vacuum techniques. There are several printing techniques without using vacuum facilities, such as micro-contact printing [66], nano imprint [67], and ink-jet printing [68]. Table 1-5 summarizes the characteristics of these three direct pattern deposition methods. Even the ink-jet printing technique has the largest printing resolution (10~20 μm) among these three processes, its unrestricted printing area makes it become the most appropriate printing process for the large area flat panel display fabrication. Since the ink-jet printing technique requires the compatibility of solution process, the CSD process offers the opportunity to realize the fabrication of devices by ink-jet printing. In this thesis, we demonstrated the synthesis and characteristics of sol-gel-derived Mg and Zr doped thin film transistors, and the physical and material properties of the films were also investigated.

1.5 Thesis Organization

This thesis is organized as follows:

In chapter 1, the overview of thin film transistors, physical properties of ZnO, and motivations of this thesis were described.

In chapter 2, we introduced the experimental details of the sol-gel process and sputtering system. Furthermore, the analysis of material properties and measurement of electrical performances were also presented.

In chapter 3, sol-gel-derived *n*-type $Zn_{(1-x)}Mg_xO$ (x = 0－0.45) thin films and thin-film transistors (TFTs) with active channel layers made of the films were investigated. The films were prepared at 500℃. The effects of Mg doping on the crystallinity, optical transparency, grain size, and carrier concentration (n) of the films were examined. The Fermi level of the films, as derived from the temperature dependence of n, was ~0.12 eV below the conduction band. The donor concentration and donor level (E_d) were derived by a curve fitting method based on the electrical neutrality condition. E_d was found to be about 0.3 eV below the conduction band. The composition dependence of the TFT output characteristics was interpreted and correlated to the width of the depletion region adjacent to the grain boundaries. When the grains were almost depleted at x = 0.2, the TFT showed an enhancement mode and an on/off ratio of 10^6.

In chapter 4, sol-gel-derived $Zn_{(1-x)}Zr_xO$ films and thin film transistors (TFTs) were investigated, where x ranging from 0.00 to 0.10. The effects of Zr additive on the crystallinity, grain size and surface morphology of

$Zn_{(1-x)}Zr_xO$ films were discussed. $Zn_{(1-x)}Zr_xO$-TFTs exhibited much lower off-state current (I_{OFF}) and higher on/off ratio than pure ZnO-TFT. The behavior of I_{OFF} related to the carrier concentration (n) of $Zn_{(1-x)}Zr_xO$ films and the correlation between n and grain size were interpreted. The optimized I_{OFF} and on/off ratio of $Zn_{(1-x)}Zr_xO$-TFT were 3.24×10^{-13} A/μm and 8.89×10^{6} where $x = 0.03$, respectively.

In chapter 5, electrical performance improvements of sol-gel-derived $Zn_{0.97}Zr_{0.03}O$ thin-film transistors (TFTs) comprising $(Ba,Sr)TiO_3$ (BST) high-k gate insulators were investigated. The (110)-preferentially oriented BST synthesized on $BaRuO_3$ electrodes exhibited enhanced dielectric constants and suppressed leakage currents. Reduced operation voltage and improved electrical characteristics of $Zn_{0.97}Zr_{0.03}O$-TFTs correlated to higher gate capacitance and superior interface trap density (D_{it}) of BST gate dielectrics were interpreted. The optimized mobility (μ_{sat}), threshold voltage (V_{th}) and subthreshold slope (S) of $Zn_{0.97}Zr_{0.03}O$-TFTs incorporating BST gate insulators with a high dielectric constant of 151 were 1.40 cm^2/Vs, 1.45 V and 0.61 V/dec, respectively.

In chapter 6, conclusions of this thesis and further recommendations were given.

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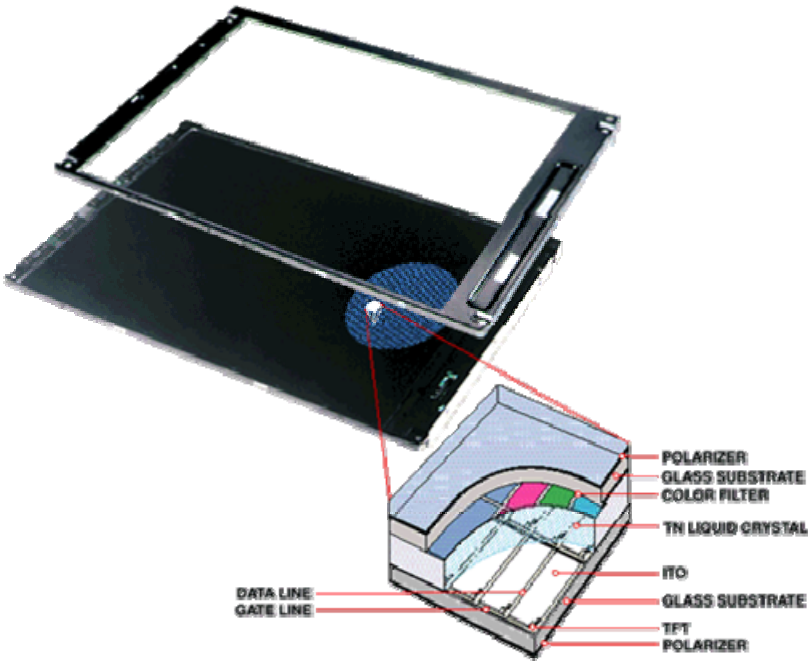

Figure 1-1 Electrical schematic of three-subpixel cross-section (bottom) of an active-matrix LCD.

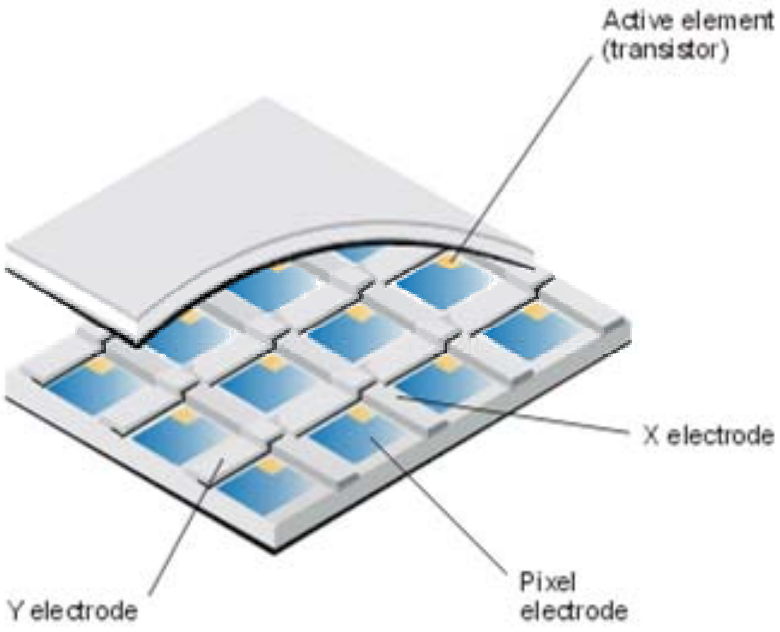

Figure 1-2 TFT switching devices at the cross point with the row and column lines.

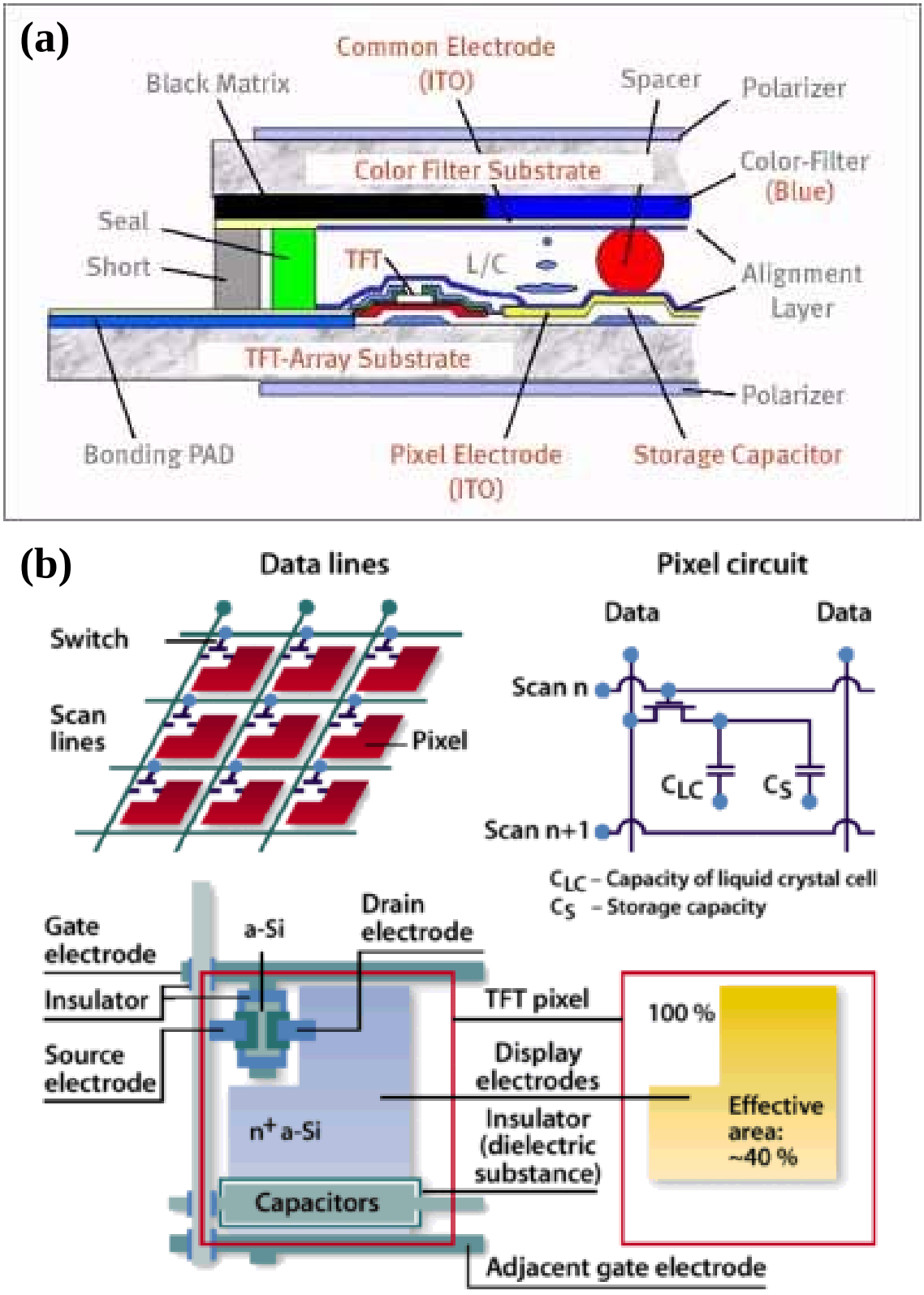

Figure 1-3 The TFT-LCD (a) cross-sectional view of panel, (b) storage capacitor-on-gate pixel.

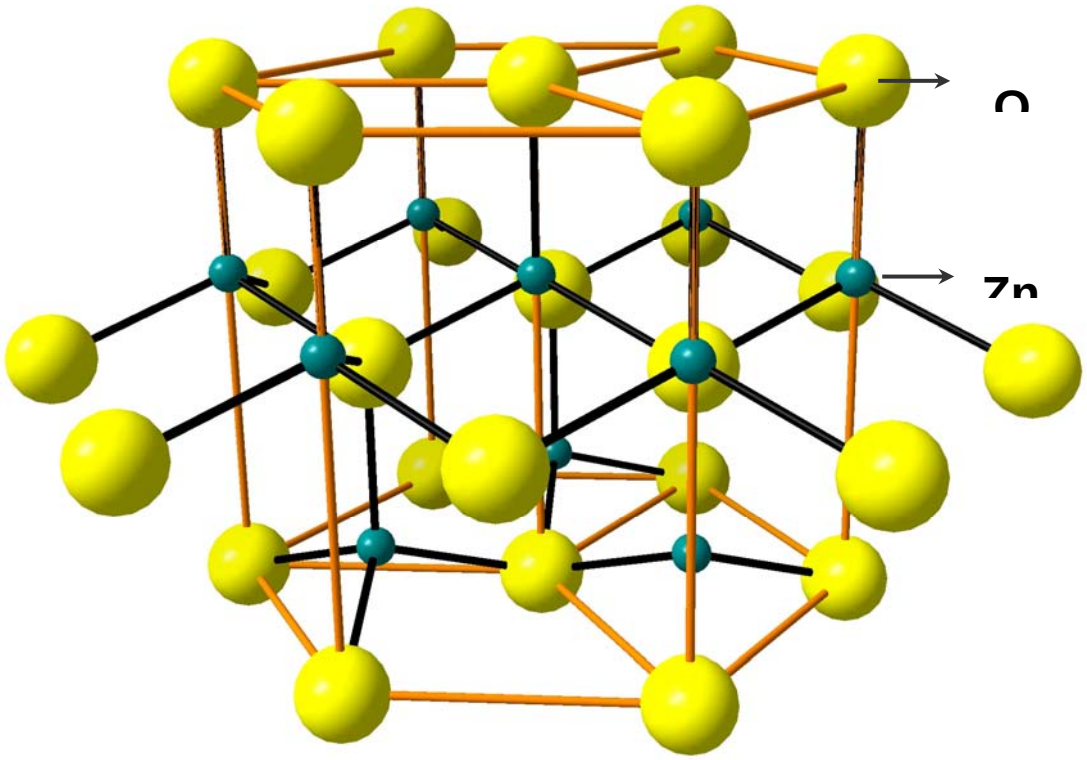

Figure 1-4 The hexagonal (wurtzite) crystal structure of ZnO.

Table 1-1 The fabrication sizes and cutting efficiency of all generation factories.

	Module Size (mm×mm)	26”	32”	37”	40”	42”	46”	47”
G5	1100×1300	6	3	2	2	2	2	2
G5.5	1300×1500	8	6	3	2	2	2	2
G6	1500×1850	12	8	6	4	3	3	2
G7	1870×2200	18	12	8	8	6	6	4
G7.5	1950×2250	18	12	8	8	8	6	6

Table 1-2 Comparison of large size LCD TVs by several makers.

Maker	Samsung	LG Philips	AUO	Chi Mei
Item				
Resolution	1920x1080	1920x1080	1920x1080	1920x1080
Module Size (mmxmm)	1323x765 (57″)	1264x738 (55″)	1020x573 (46″)	1043x856 (47″)
Aspect Ratio	16:9	16:9	16:9	16:9
Colors	16.7 M	16.7 M	16.7 M	16.7 M
Viewing Angle	170° (PVA)	176° (S-IPS)	170° (P-MVA)	170° (S-MVA)
Brightness (cd/m²)	500	550	600	600
Contrast Ratio	1000:1	550:1	800:1	800:1
Response Time (ms)	8	8	8	8
MP Schedule	Q3. '04	Q3. '04	Q2. '04	Q1. '05

Table 1-3 Major TFT/AMLCD Design Factors.

TFT AMLCD design factors	**Examples**
Display size	Diagonal (14”, 15”, 18”, 20”, 40”, etc.)
Light modulator/mode	(TNLC-NW, TNLC-NB, IPS, FELC, etc.)
Illumination conditions	Contrast ratio (2:1, 300:1, etc.) Maximum brightness (100 cd/m^2, 500 cd/m^2, etc.) Ambient illumination (dark room, room light, sunlight readable, etc.)
Display format (number of lines)	Content (VGA, SVGA, XGA, SXGA, UXGA, QUXGA-W, etc.)
Frame time	Film, 1/24 sec; video, 1/30 sec; data 1/60 sec; etc.
Number of gray levels	6-bits (262K colors), 8-bits (16.8M colors), etc.
TFT geometry	Bottom-gate staged BCE, I-stopper, top gate, etc.
Fill factor	30%, 60%, 75%, 100%

Table 1-4 Physical properties of wurtzite ZnO.

Property	Value
Lattice parameters at 300K:	
a_0	0.32495 nm
c_0	0.52069 nm
a_0/c_0	1.602 (1.633 for ideal hexagonal structure)
u	0.345
Density	5.606 g/cm^3
Stable phase at 300K	wurtzite
Melting point	1975°C
Thermal conductivity	0.6, 1-1.2
Linear expansion coefficient (/°C)	a_0: 6.5×10^{-6}, c_0: 3.0×10^{-6}
Static dielectric constant	8.656
Refractive index	2.008, 2.029
Energy gap	3.4 eV (direct)
Intrinsic carrier concentration	< 10^6 cm^{-3}
Exciton binding energy	60 meV
Electron effective mass	0.24
Electron Hall mobility at 300K for low n-type conductivity	200 cm^2/Vs
Hole effective mass	0.59
Hole Hall mobility at 300K for low p-type conductivity	5-50 cm^2/Vs

Table 1-5 Comparison of several printing techniques.

Classification	**Nano Imprint**	**Micro-Contact**	**Ink-jet**
Resolution	50 nm	3 μm	10~20 μm
Printing Area	100mm×100mm	100mm×100mm	> 2m×2m
Method	Contact	Contact	Non-contact
Deposition	Dry	Dry	Wet
Issue	Difficult for non-flat surface	Stability for printer	Drop volume <1f *l*