Chapter 5 Electrical Performance Improvements of Sol-Gel-Derived $Zn_{0.97}Zr_{0.03}O$ Thin-Film Transistors by Using $(Ba,Sr)TiO_3$ High-k Gate Insulators

5.0 Preface

Electrical performance improvements of sol-gel derived $Zn_{0.97}Zr_{0.03}O$ thin-film transistors (TFTs) comprising $(Ba,Sr)TiO_3$ (BST) high-*k* gate insulators were investigated in this study. The (110)-preferentially oriented BST synthesized on $BaRuO_3$ electrodes exhibited enhanced dielectric constants and suppressed leakage currents. Reduced operation voltage and improved electrical characteristics of $Zn_{0.97}Zr_{0.03}O$-TFTs correlated to higher gate capacitance and superior interface trap density (D_{it}) of BST gate dielectrics were interpreted. The optimized mobility (μ_{sat}), threshold voltage (V_{th}) and subthreshold slope (S) of $Zn_{0.97}Zr_{0.03}O$-TFTs incorporating BST gate insulators with a high dielectric constant of 151 were 1.40 cm^2/Vs, 1.45 V and 0.61 V/dec, respectively.

5.1 Introduction

ZnO is a normally *n*-type semiconductor with a wide band gap (3.2 eV) and large exciton binding energy (60 meV), which has been widely

exploited for applications in phosphors [1], transparent conducting oxides [2] and UV-laser-emitting diodes [3]. Owing to the high transparency and low processing temperature compared with amorphous and polycrystalline silicon thin-film transistors (a-Si and poly-Si TFTs), ZnO-TFTs have been intensively studied for the development of flat panel displays in the recent years. In our previous study [4], the chemical solution deposition of $Zn_{(1-x)}Zr_xO$-TFTs comprising silicon dioxide as gate dielectric has been demonstrated by sol-gel method. Even though $Zn_{(1-x)}Zr_xO$-TFTs represented a low off-state current of 3.24×10^{-13} A/μm and high on/off current ratio of 8.89×10^6 where $x = 0.03$ by doping Zr additives instead of annealing at high temperature, the devices have to operate at very high voltage and exhibited poor electrical characteristics such as mobility and subthreshold slope. Among ZnO-TFTs studies, SiO_2 was the most commonly used gate insulator due to its low gate leakage current and high breakdown field. Nevertheless, the low dielectric constant of SiO_2 ($\varepsilon_r = 3.9$) results in high operation voltage of ZnO-TFTs [5-8]. It has been reported that high mobility obtained at low operation voltage in organic thin-film transistors (OTFTs) by using high-*k* gate dielectrics [9]. In poly-Si [10] and SiGe TFTs [11], the high-*k* gate insulators were also used to improve the electrical characteristics including mobility, threshold voltage and subthreshold slope. Besides, it has also demonstrated that the high-*k* $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_7$ (BZN, $\varepsilon_r = 55$) gate insulator in ZnO-TFTs led to a very low operation voltage of 4V [12]. Another high-*k* candidate, Barium strontium titanate, $(Ba,Sr)TiO_3$ (BST), exhibits a very high dielectric constant of 725 deposited on Pt

electrodes at a temperature of 650℃ [13]. However, the BST films revealed large leakage currents at high deposition temperature. Even the leakage currents were suppressed at lower deposition temperature, the dielectric constants of BST have a dramatically degradation as a result of the high crystallization temperature of BST [14]. In order to resolve this problem, there are many reports emphasized that alternative conductive oxide electrodes, such as $LaNiO_3$ (LNO) [14], $SrRuO_3$ (SRO) [15] and $BaRuO_3$ (BRO) [16], would be desirable since these electrodes provide similar crystal structure and lattice constant with BST and thus decrease the crystallization temperature and raise the dielectric constant of BST due to the better lattice matching and structural compatibility between bottom electrodes and BST films. Therefore, the high dielectric constant and low leakage current of BST films could be obtained at a moderate deposition temperature incorporating conductive oxide electrodes mentioned above. In this work, we proposed the low operation voltage of $Zn_{0.97}Zr_{0.03}O$-TFTs comprising the high-*k* BST gate insulators with (110) preferred orientation given by BRO bottom gate electrodes. Moreover, the interpretation of electrical performance improvements of $Zn_{0.97}Zr_{0.03}O$-TFTs achieved by the higher gate capacitance and superior interface trap property of BST gate dielectric was also investigated.

5.2 Experiment

The BRO electrodes were grown on Si (100) substrates by rf

magnetron sputtering at a deposition temperature of 500℃, using a target made of packed $BaRuO_3$ powders. All BRO layers were prepared in an Ar/O_2 ratio of 19.5/0.5 and a total pressure of 10 mTorr at a power density of 2.3 W/cm^2. The BST films with a thickness of 3000 Å were deposited on the BRO bottom electrodes using a $(Ba_{0.5}Sr_{0.5})TiO_3$ powder target by rf sputtering. The BST layers were synthesized in an Ar/O_2 ratio of 1/1 at various deposition temperatures ranging from room temperature (RT) to 500℃, and the other conditions were the same as those of BRO electrodes. After depositing BST, the films were annealed at 400℃ for 30 min under oxygen atmosphere to eliminate the interface defects between BST and BRO. In order to investigate the dielectric constant and leakage current behaviors of BST films by means of metal-insulator-metal (MIM) structure, thermal evaporated aluminum films were deposited onto BST films as top electrodes with an area of 9.6×10^{-4} cm^2. The detailed synthesis of $Zn_{0.97}Zr_{0.03}O$ sol-gel precursor has been described in our previous study [4]. To identify the influences of high-*k* BST gate insulators on $Zn_{0.97}Zr_{0.03}O$-TFTs, the $Zn_{0.97}Zr_{0.03}O$ thin films utilized as active channel layers were both deposited on SiO_2/BRO and BST/BRO substrates with $Zn_{0.97}Zr_{0.03}O$ sol-gel solution by spin coating and annealed at 400℃ for 30 min under oxygen atmosphere, where SiO_2 with the same thickness of 3000Å as BST. Aluminum doped zinc oxide (AZO) films were deposited by rf sputtering onto $Zn_{0.97}Zr_{0.03}O$ active channel layers served as source and drain electrodes, and the channel width and length were 500 μm and 100 μm, respectively. The schematic diagram of the devices is shown in

Figure 5-1. The crystallinity of the BST films was examined by X-ray diffraction (XRD, Siemens D5000) with Cu $K\alpha$ radiation. The surface morphologies and microstructure of BST and $Zn_{0.97}Zr_{0.03}O$ films were observed by atomic-force microscope (AFM, Digital Instruments Nanoscope III) and scanning electron microscope (SEM, Hitachi S-4700). The leakage current of BST insulators and electrical performance of $Zn_{0.97}Zr_{0.03}O$-TFTs were measured by HP4156B precision semiconductor parameter analyzer. The dielectric constants of BST films were calculated by capacitance-voltage (C-V) measurement with HP4284A at a frequency of 100 kHz. The values of carrier concentration (n) of $Zn_{0.97}Zr_{0.03}O$ films were estimated by a metal-oxide-semiconductor (MOS) structures of AZO/$Zn_{0.97}Zr_{0.03}O$/BST/BRO with the same C-V measurement system. The MOS structures were also used to evaluate the interface trap density by quasistatic and high frequency (100 kHz) C-V characteristics.

5.3 Results and discussion

Figure 5-2 shows the XRD patterns of BST films deposited on BRO electrodes at various deposition temperatures ranging from 100 to 500℃. The (110) peak corresponding to BST phase appeared at a deposition temperature of 200℃ which was much lower than that grown on Pt electrodes [14]. The (110) orientation of BST films was further enhanced by increasing the deposition temperature up to 500℃. This result indicated that the low crystallization temperature of BST attributed to the preferred

orientation enhancement provided by (110)-oriented BRO bottom electrodes. The dielectric constant of BST films as a function of deposition temperature was shown in Figure 5-3. The ε_r values of BST films increased with higher deposition temperature due to the better crystallinity of BST films obtained at higher deposition temperature. It is noticed that the dielectric constant of BST grown on BRO at a moderate deposition temperature (T_d=300℃, ε_r=151) was much higher than that deposited on Pt electrodes (T_d~300℃, ε_r~50) [14] as a result of the reduction of crystallization temperature.

Figure 5-4 shows the variations of leakage current density with the electric field for the BST deposited on BRO with various deposition temperatures. The leakage currents of the BST deposited within room temperature to 300℃ were about 2×10^{-8} A/cm^2 at an applied field of 1 MV/cm and the similar leakage current behaviors could be observed. The leakage currents of BST were much lower than that grown on Pt electrodes at the same electric field [17]. On account of good lattice matching between BST and BRO layers, the interface defects located in BST/BRO were fewer than BST/Pt. Hence, the leakage current of BST deposited on BRO was lower than that grown on Pt electrodes. In contrast, the leakage currents of BST films deposited at 400 and 500℃ exhibited almost two orders of magnitude larger than that deposited below 300℃. The values of leakage current of BST deposited above 400℃ were too high to be appropriate gate insulators for transistors. Figure 5-5a-c show the surface morphologies

of BST deposited at 100 to 500℃ observed by using AFM over a scanning area of 3 × 3 μm, and the images depicted the effects of elevated deposition temperature on grain growth. This result was consistent with leakage current behaviors and XRD data. Since BST films grown at higher deposition temperature contained larger grain size, the grain boundary may supply shorter circuit paths to raise the leakage current when the bias was applied. The larger grain size also revealed better crystallinity obtained at higher T_d. The surface roughness (R_{rms}) of the BST films deposited at temperatures ranging from room temperature to 500℃ was shown in Figure 5-6. It is found that the values of surface roughness of BST films have a slightly increase with higher deposition temperature, but all of them were less than 3 nm which close to the value of SiO_2 (R_{rms}= 2.883 nm). This finding indicates that the leakage currents and surface roughnesses of the BST films grown at temperatures below 300℃ fill the requirements for their application as gate insulators in transistors. Figure 5-7a-c show the surface images of $Zn_{0.97}Zr_{0.03}O$ films deposited on SiO_2, BST (T_d = 100℃) and BST (T_d = 300℃), respectively. The same chain-like structure and small grain size as our previous study [4] could be observed. It could be also seen that the surface morphologies of $Zn_{0.97}Zr_{0.03}O$ films grown on SiO_2 and BST at different T_d had no significant variations.

The drain current-drain voltage (I_D-V_D) and drain current-gate voltage (I_D-V_G) characteristics of $Zn_{0.97}Zr_{0.03}O$-TFT utilizing SiO_2 as gate insulator are shown in Figure 5-8 and 5-9, respectively. From the slopes and

intercepts of $\sqrt{I_D}$ -V_G plots at V_D= 100 V, the mobility (μ_{sat}) and threshold voltage (V_{th}) of the device were estimated to be 0.24 cm^2/Vs and 3.92 V, respectively. The I_{ON}/I_{OFF} current ratio is 5.26×10^6 when V_G swept from –100 to 100 V, and the subthreshold slope (S) was about 10.3 V/dec. The device using SiO_2 as gate insulator represented similar device performances to our previous work [4].

Figure 5-10 shows the output characteristics of $Zn_{0.97}Zr_{0.03}O$-TFT consisted of BST (T_d= R. T.) gate insulator and a reduced operation voltage of 10 V was obtained. It has been reported that higher gate capacitance gave rise to more coupling between the gate electrode and semiconductor layer, and thus reduces the operation voltage of devices [12]. Hence, the reduction of operation voltage resulted from the higher gate capacitance of BST (T_d= R. T.) than SiO_2 since the former exhibited a ε_r of 25 larger than the later. Figure 5-11 shows the transfer characteristics of $Zn_{0.97}Zr_{0.03}O$-TFTs with V_D = 10 V incorporating BST as gate insulators deposited from room temperature to 300℃. It could be seen that the on-state currents increased with higher deposition temperature of BST gate insulators, and the off-state currents had no significant variations even compared with SiO_2 gate dielectric, which as shown in Figure 5-9. The electrical characteristics of $Zn_{0.97}Zr_{0.03}O$-TFTs comprising different gate insulators including SiO_2 and BST with T_d from R. T. to 300℃ were summarized in Table 5-1.

The *C-V* characteristics of MOS structure composed of $Zn_{0.97}Zr_{0.03}O$

semiconductor and BST (T_d= 300 ℃) insulator, which operated at frequencies from quasistatic to 100 kHz are shown in Figure 5-12. The *C-V* characteristics which performed at 100 kHz revealed the typical high-frequency *C-V* characteristics of MOS structure. However, the surface phenomenon did not appear even the *C-V* measurement was performed at 1 kHz. This should result from the low thermal generation rate of minority carriers (holes) caused by the wide band gap (~3.2 eV) of ZnO. Hence, we have tried lower frequency of 100 and 10 Hz, and the inversion capacitance is found to increase with lower frequency. It indicates that the thermal generation rate of minority carriers could keep up with the small-signal variation of lower frequency, and this result is in good agreement with the previous report [18]. Furthermore, this appearance was also observed in other wide band gap semiconductors such as GaN [19-21]. When a very low frequency of quasistatic measurement was applied, the inversion capacitance of $Zn_{0.97}Zr_{0.03}O$ MOS structure increased back up to the insulator capacitance, C_i. Therefore, it was considered that the inversion behaviors of wide band gap semiconductors such as $Zn_{0.97}Zr_{0.03}O$ could be only observed at very low frequency of *C-V* measurement. Since both of the high and low-frequency *C-V* curves were obtained, the interface trap densities (D_{it}) could be estimated by high and low frequency method. The high and low frequency method is one of the most common interface trapped charge measurement method, and the interface trap density D_{it} is given by

$$D_{it} = \frac{C_i}{q}\left(\frac{C_{lf}/C_i}{1 - C_{lf}/C_i} - \frac{C_{hf}/C_i}{1 - C_{hf}/C_i}\right) \quad (5\text{-}1)$$

where C_{lf} is the low frequency (quasistatic) capacitance, and C_{hf} the high frequency capacitance. Both of the C_{lf} and C_{hf} were measured as a function of gate voltage, and the relationship between surface potential ϕ_s and V_G is given by

$$\phi_s = \int_{V_{G1}}^{V_{G2}} \left(1 - \frac{C_{lf}}{C_i}\right) dV_G + \Delta \quad (5\text{-}2)$$

where Δ is an integration constant given by the surface potential at $V_G = V_{G1}$. Therefore, D_{it} could be determined and plotted as a function of ϕ_s. However, it is not always necessary to determine D_{it} as a function of surface potential. For instance, it is frequently sufficient to determine D_{it} at one point on the *C*-*V* curve and then compare device-to-device or run-to-run. A convenient choice is the minimum C_{lf} where the technique is most sensitive. This point also corresponds to a surface potential in the light inversion region near the midgap of the semiconductor. The values of D_{it} in our study were estimated by the high and low *C*-*V* method mentioned above.

For high-frequency curves, the measurement frequency must be sufficiently high that interface traps do not respond. The usual 1 MHz frequency may suffice, but for devices with high D_{it} there will be some response due to interface traps. If possible, one should use higher

frequencies. However, care must be used to ascertain that series resistance effects do not become important. The low frequency curve is usually obtained by measuring the current in response to a gate voltage ramp or by a charge voltage methos. It is easier to measure C_{lf} when sweeping from inversion to accumulation, because minority carrier need not be generated thermally since they already exist in the inversion layer. The lower limit of D_{it} that can be determined with the high and low frequency method lies around 10^{10} $cm^{-2}eV^{-1}$. The charge voltage method is well suited for MOS measurements since it has high noise immunity, because sizable voltages rather than low currents are measured, and since voltage steps rather than precisely linear voltage ramps are used. The method is also suitable to determine the additive constant Δ of Eq. (5-2) by comparing experimental and theoretical ϕ_s versus *W* curves, where ϕ_s is the surface potential and *W* is the space-charge region width obtained from the experimental high frequency *C*-*V* curves. A more detailed and extensive discussion was presented in the monograph "Semiconductor Material and Device Characterization" chapter 6, by Dieter K. Schroder 1998 John Wiley & Sons.

The dependence of D_{it} extracted from *C*-*V* measurements on different gate insulators including SiO_2 and BST with various T_d is shown in Figure 5-13. A large interface trap density of 8.14×10^{12} $cm^{-2}eV^{-1}$ was obtained by SiO_2, and the D_{it} were diminished by using BST insulators. The interface properties of BST were further improved with higher T_d and a low

D_{it} of 5.44 × 10^{11} $cm^{-2}eV^{-1}$ was obtained at T_d = 300℃. The improved $Zn_{0.97}Zr_{0.03}O$/BST interface characteristics may attribute to the superior surface properties provided by the better crystallinity of BST grown at higher T_d. Moreover, the values of carrier concentration n were also estimated from *C-V* characteristics with MOS structure. The n of $Zn_{0.97}Zr_{0.03}O$ semiconductor deposited on SiO_2 and BST with various T_d were around 3.97 to 4.04 × 10^{16} cm^{-3}. These values of n were in good agreement with our previous work [4] and revealed that the carrier concentrations of $Zn_{0.97}Zr_{0.03}O$ deposited on SiO_2 and BST insulators kept almost the same. Since it has been interpreted that the carrier concentration of ZnO depended on its grain size [22], the n of $Zn_{0.97}Zr_{0.03}O$ with minor fluctuation might result from the slightly variations of grain size deposited on SiO_2 and BST observed from Figure 5-7. Whereas different gate insulators did not affect the properties of $Zn_{0.97}Zr_{0.03}O$ semiconductor such as grain size and carrier concentration, the electrical performance improvements of $Zn_{0.97}Zr_{0.03}O$-TFTs could be referred to the higher gate capacitance and lower interface trap density of BST gate insulators. Since it has been indicated that the interface trap density plays an important role in device characteristics [23,24], the improved mobility, threshold voltage and subthreshold slope of $Zn_{0.97}Zr_{0.03}O$-TFTs by using BST gate insulators as shown in Table 5-1 could ascribe to the suppression of D_{it}.

5.4 Conclusion

In summary, we investigated the electrical performance improvements of sol-gel derived $Zn_{0.97}Zr_{0.03}O$-TFTs incorporating high-*k* BST as gate insulators. Due to the (110) preferred orientation provided by BRO bottom electrodes, the dielectric constant enhancement and leakage current restraint of BST films were observed. By using BST gate insulators in $Zn_{0.97}Zr_{0.03}O$-TFTs, the high gate capacitances reduced the operation voltage of the devices. Inasmuch as BST gate dielectrics represented superior interface trap density, the electrical performance including mobility, threshold voltage and subthreshold slope of $Zn_{0.97}Zr_{0.03}O$-TFTs were significantly improved. The optimized mobility, threshold voltage and subthreshold slope of $Zn_{0.97}Zr_{0.03}O$-TFTs consisted of BST gate insulator deposited at 300℃ with a ε_r of 151 were 1.40 cm^2/Vs, 1.45 V and 0.61 V/dec, respectively.

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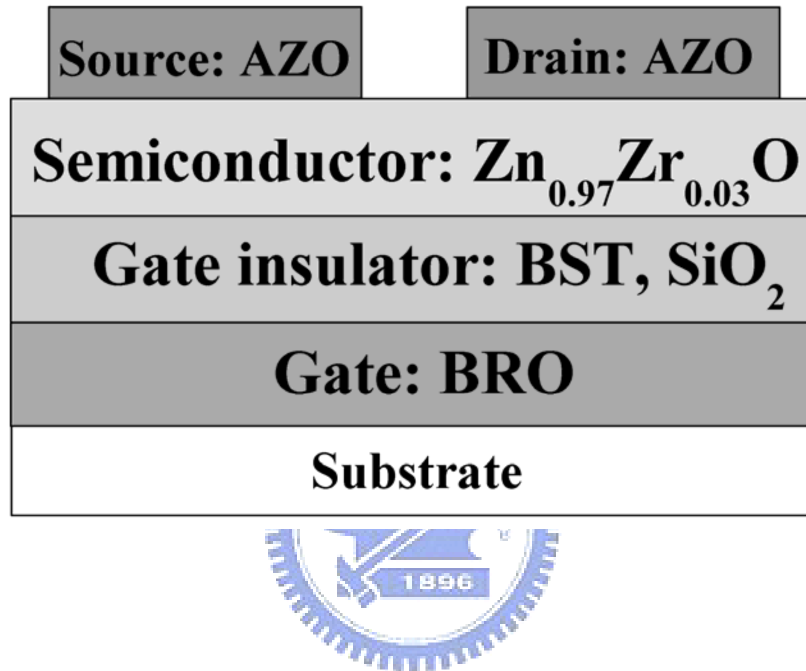

Figure 5-1 Schematic diagram the $Zn_{0.97}Zr_{0.03}O$ thin-film transistor.

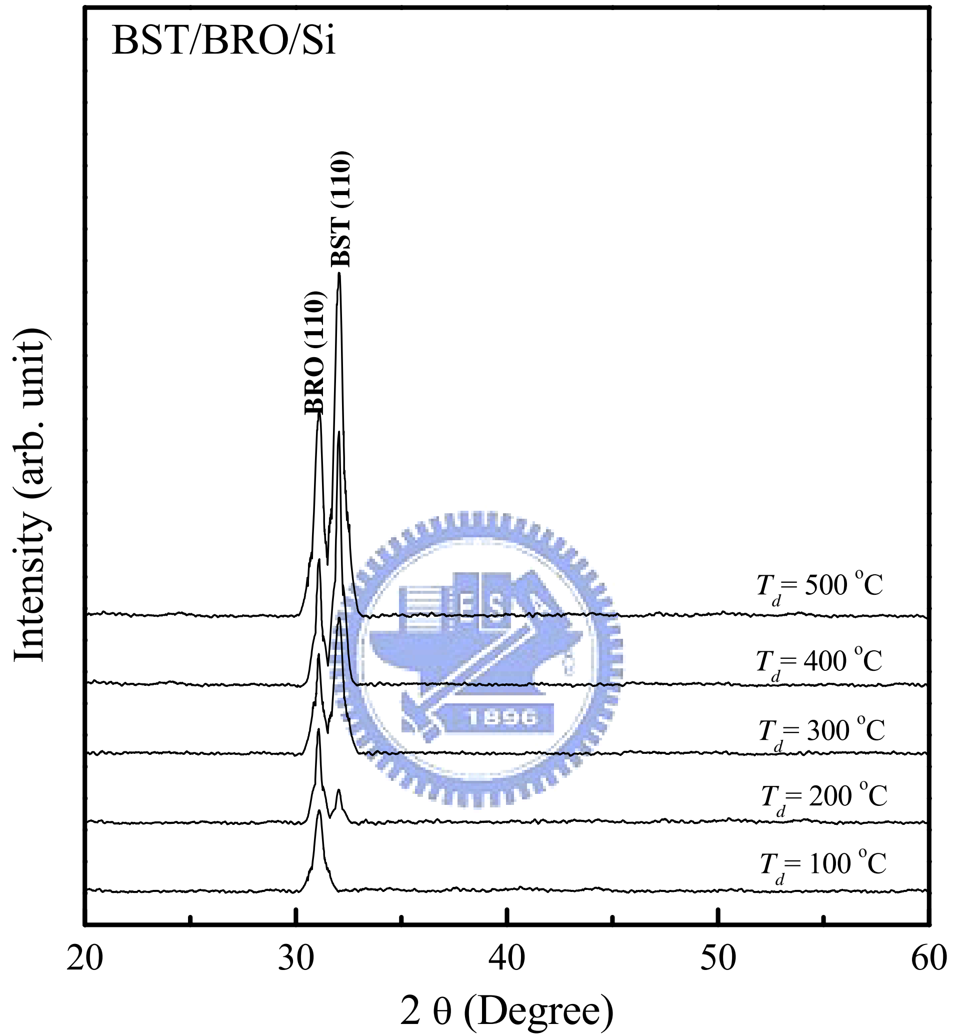

Figure 5-2 XRD spectra of BST films grown on $BaRuO_3$ at various deposition temperatures.

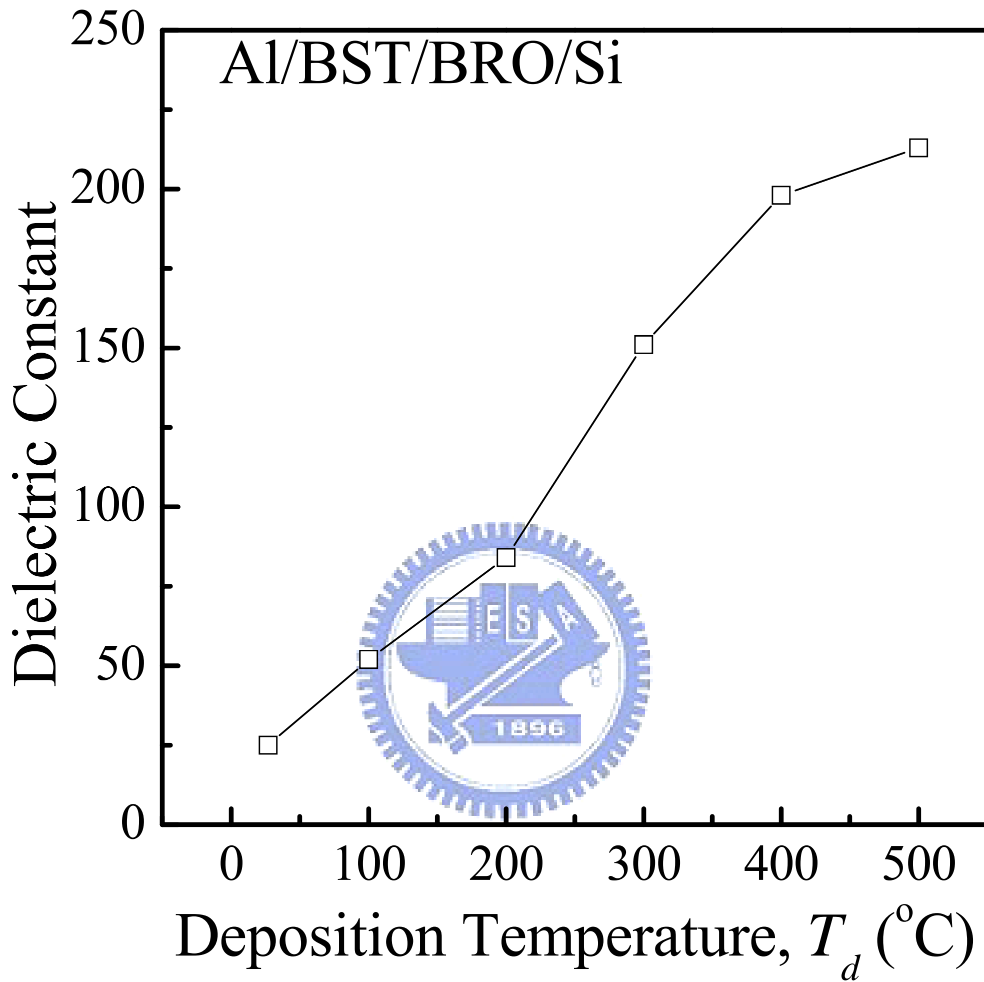

Figure 5-3 Dielectric constant of BST as a function of deposition temperatures.

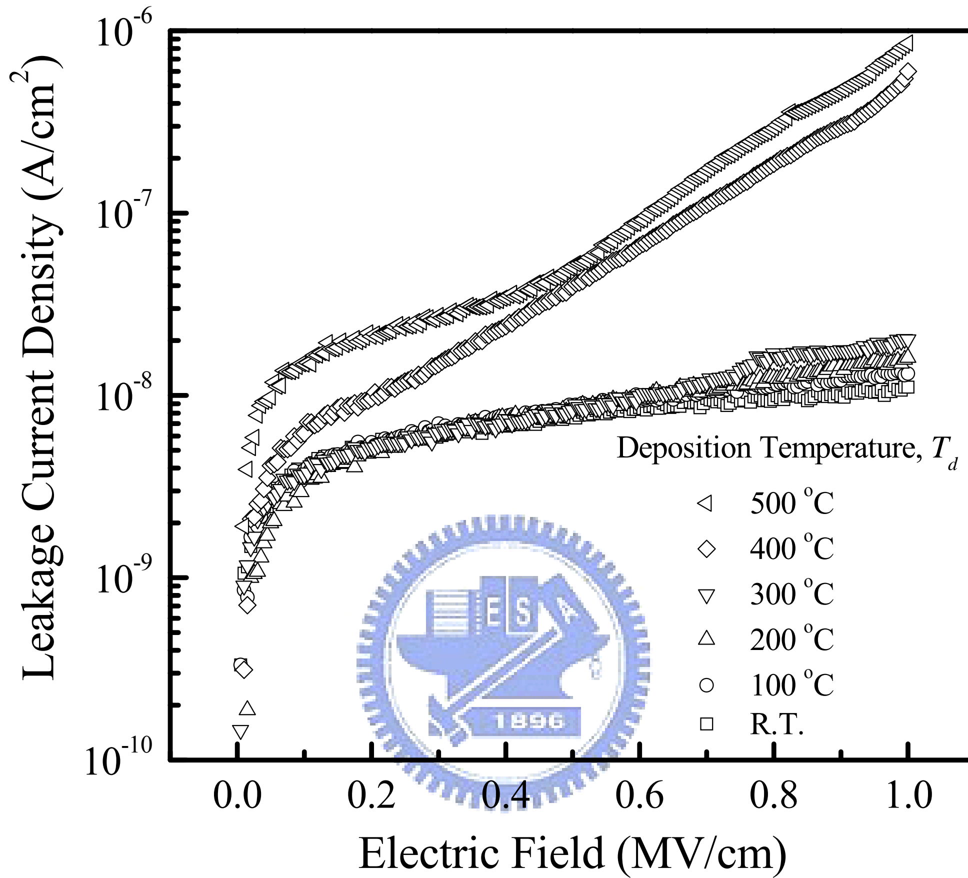

Figure 5-4 Leakage current density variation as a function of electric field for BST capacitors (Al/BST/BRO) with various deposition temperatures.

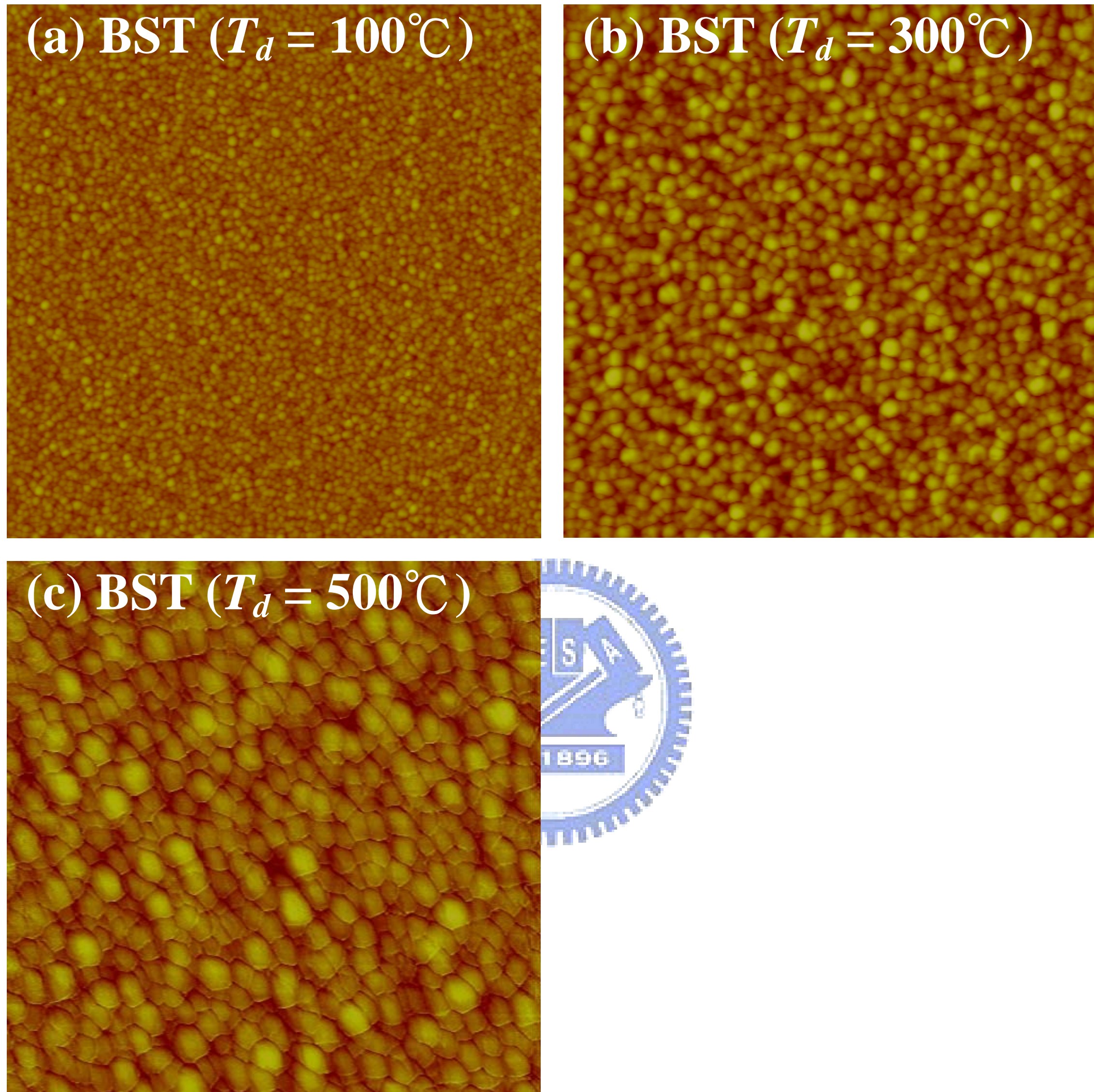

Figure 5-5 AFM surface observations of BST deposited at (a) 100 (b) 300 and (c) 500℃.

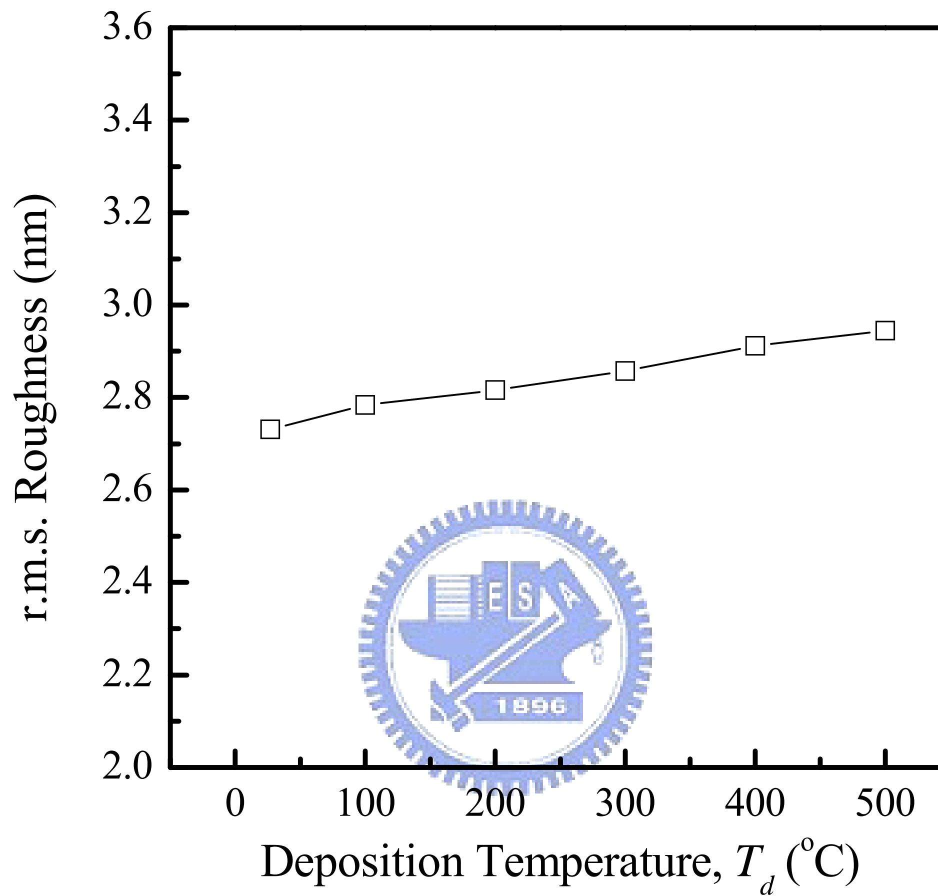

Figure 5-6 Roughness of BST films as a function of various deposition temperatures.

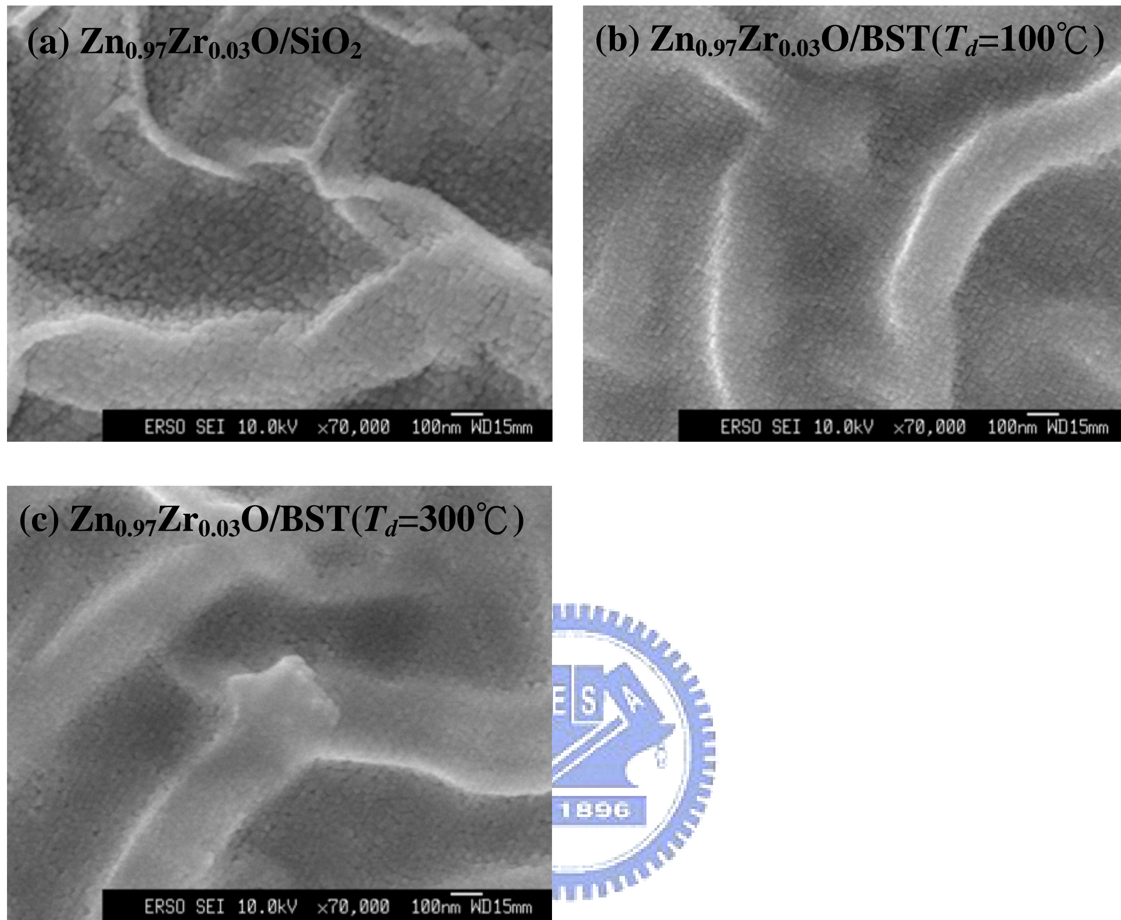

Figure 5-7 SEM surface images of $Zn_{0.97}Zr_{0.03}O$ films deposited on (a) SiO_2 (b) BST (T_d= 100℃) and (c) BST (T_d= 300℃).

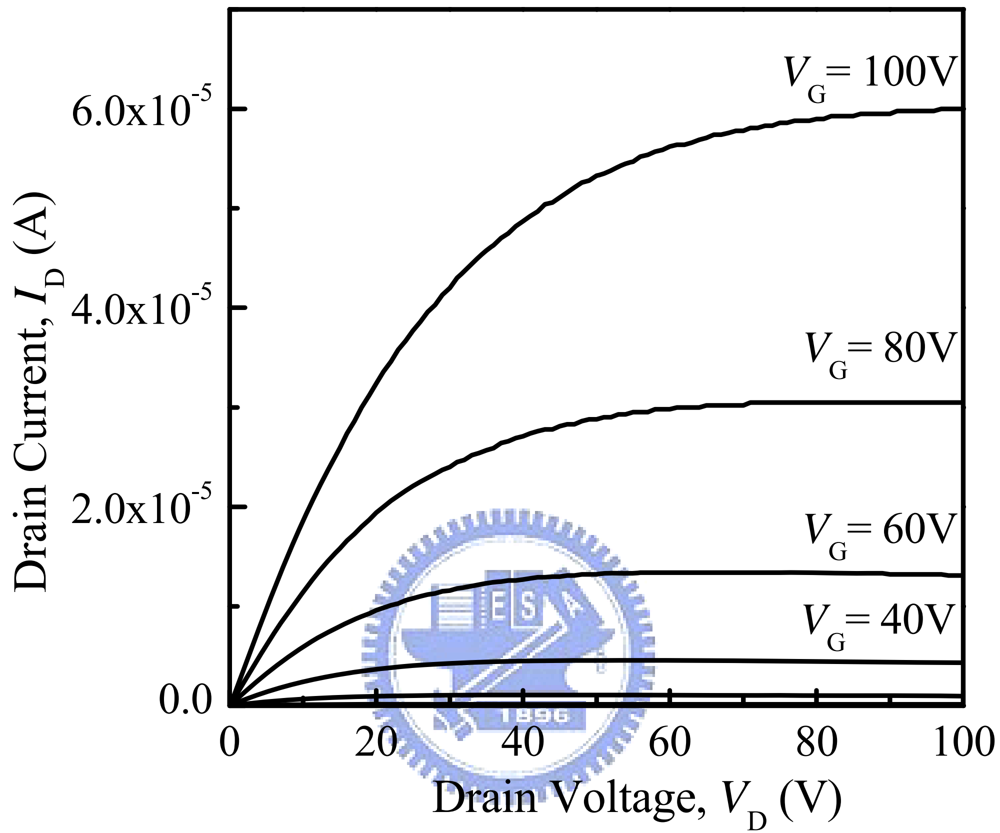

Figure 5-8 Output characteristics of $Zn_{0.97}Zr_{0.03}O$-TFTs by using SiO_2 as gate insulator at V_D = 100V.

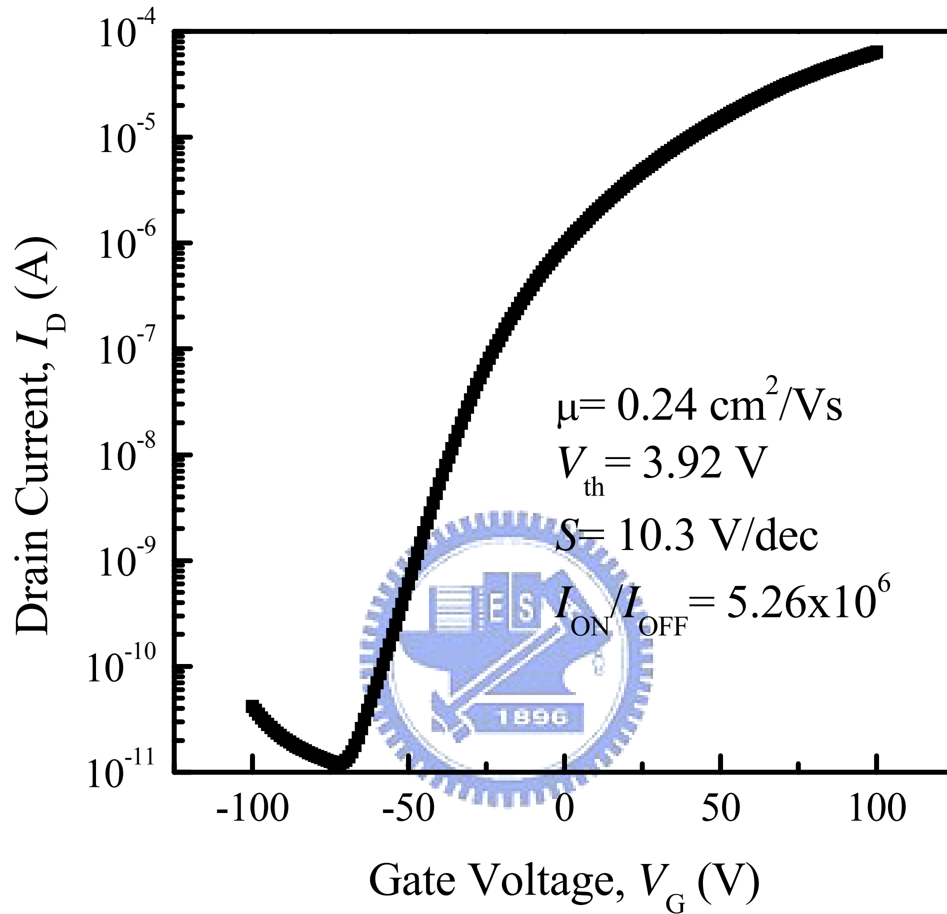

Figure 5-9 Transfer characteristics of $Zn_{0.97}Zr_{0.03}O$-TFTs by using SiO_2 as gate insulator at V_D = 100V.

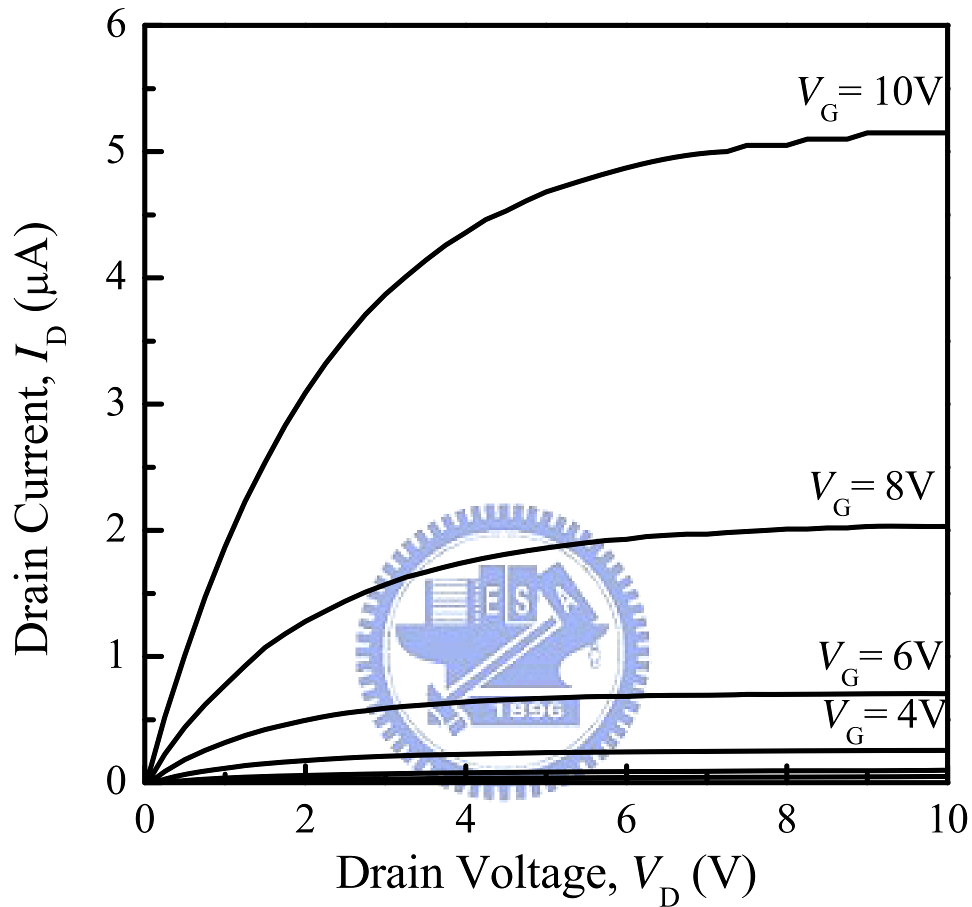

Figure 5-10 Drain current-drain voltage characteristics of the $Zn_{0.97}Zr_{0.03}O$-TFTs incorporating the BST gate insulator deposited at room temperature.

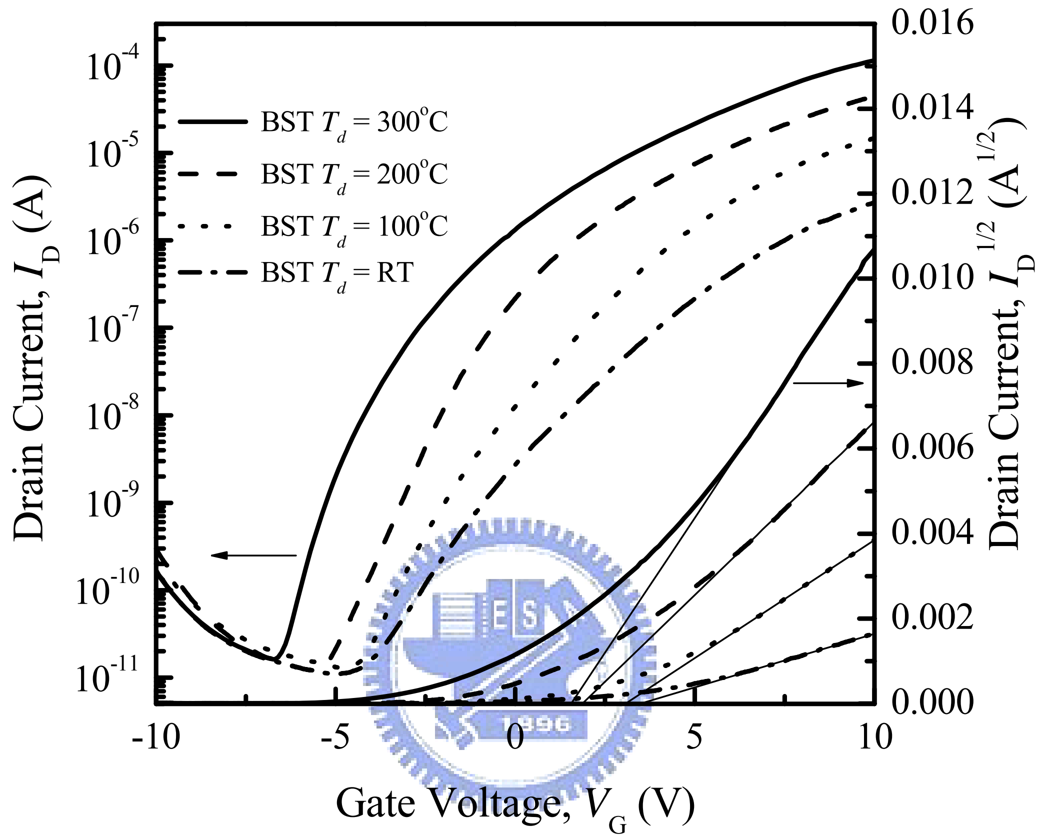

Figure 5-11 Log and square root of drain current as a function of gate voltage of the devices incorporating BST gate insulators, prepared at various values of T_d, recorded at a value of V_D of 10 V.

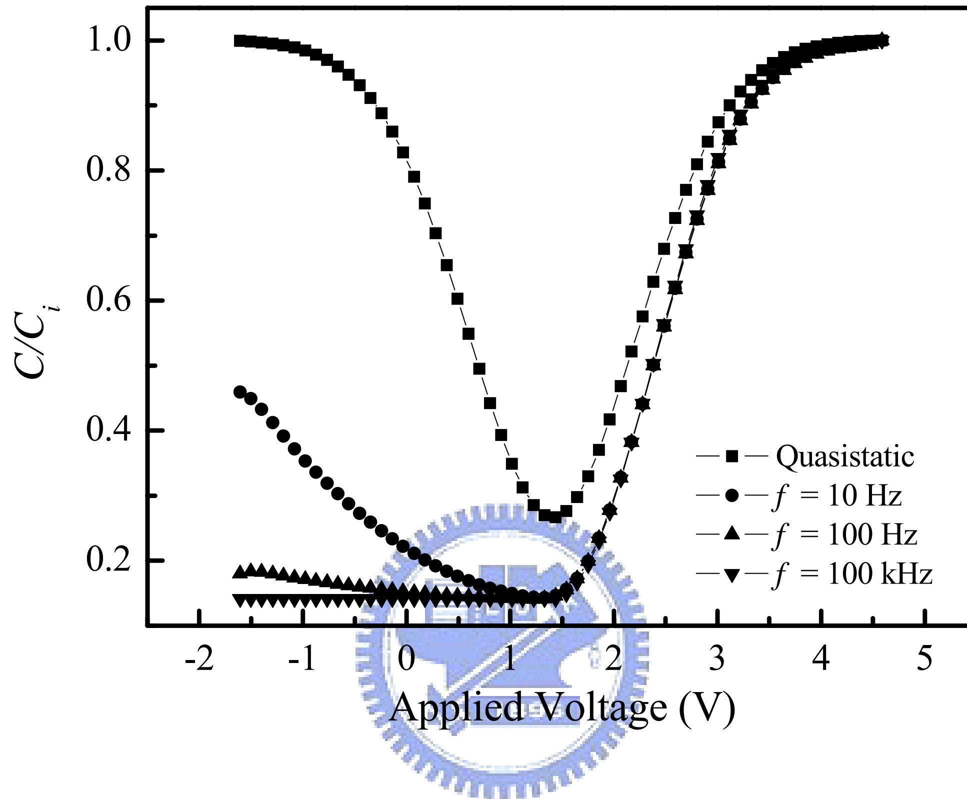

Figure 5-12 Frequency effects on the capacitance-voltage curves of the MOS structure composed of $Zn_{0.97}Zr_{0.03}O$ semiconductor and BST (T_d= 300℃) insulator.

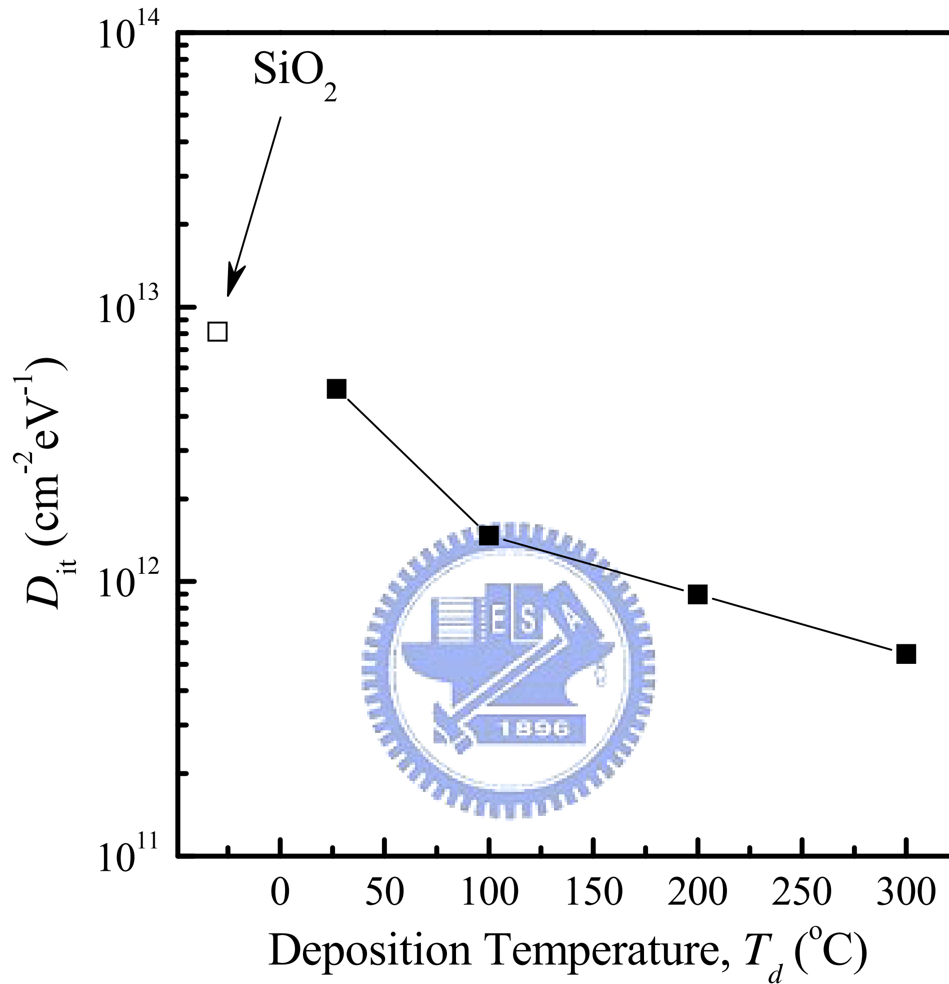

Figure 5-13 Dependence of interface trap density (D_{it}) on various gate insulators. Open and solid squares refer to SiO_2 and BST deposited at different T_d, respectively.

Table 5-1 Electrical characteristics of $Zn_{0.97}Zr_{0.03}O$-TFTs — including mobility (μ_{sat}), threshold voltage (V_{th}), subthreshold slope (S), and current modulation (I_{ON}/I_{OFF}) -incorporating SiO_2 and BST as gate insulators of various dielectric constants (ε_r) and interface trap densities (D_{it}); BST was deposited at various temperatures. The characteristics of the SiO_2-based devices were extracted using a value of V_D of 100 V; the characteristics of the devices incorporating the BST gate insulators were estimated at a value of V_D of 10 V.

Gate insulators	ε_r	D_{it} ($cm^{-2}eV^{-1}$)	μ_{sat} (cm^2/Vs)	V_{th} (V)	S (V/dec)	I_{ON}/I_{OFF}
SiO_2	3.9	8.14×10^{12}	0.24	3.92	10.3	5.26×10^{6}
BST (T_d= R. T.)	25	5.03×10^{12}	0.35	3.53	1.47	2.45×10^{5}
BST (T_d=100℃)	52	1.47×10^{12}	0.79	3.03	1.07	1.16×10^{6}
BST (T_d=200℃)	84	8.97×10^{11}	1.11	1.98	0.99	3.65×10^{6}
BST (T_d=300℃)	151	5.44×10^{11}	1.40	1.45	0.61	7.04×10^{6}