

# Impacts of N<sub>2</sub> and NH<sub>3</sub> Plasma Surface Treatments on High-Performance LTPS-TFT With High- $\kappa$ Gate Dielectric

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**Abstract**—Low-temperature polycrystalline-silicon thin-film transistors (LTPS-TFTs) with high- $\kappa$  gate dielectrics and plasma surface treatments are demonstrated for the first time. Significant field-effect mobility  $\mu_{FE}$  improvements of  $\sim 86.0\%$  and  $112.5\%$  are observed for LTPS-TFTs with HfO<sub>2</sub> gate dielectric after N<sub>2</sub> and NH<sub>3</sub> plasma surface treatments, respectively. In addition, the N<sub>2</sub> and NH<sub>3</sub> plasma surface treatments can also reduce surface roughness scattering to enhance the field-effect mobility  $\mu_{FE}$  at high gate bias voltage  $V_G$ , resulting in 217.0% and 219.6% improvements in driving current, respectively. As a result, high-performance LTPS-TFT with low threshold voltage  $V_{TH} \sim 0.33$  V, excellent subthreshold swing S.S.  $\sim 0.156$  V/decade, and high field-effect mobility  $\mu_{FE} \sim 62.02$  cm<sup>2</sup>/V · s would be suitable for the application of system-on-panel.

**Index Terms**—High- $\kappa$ , low-temperature polycrystalline-silicon thin-film transistors (LTPS-TFTs), NH<sub>3</sub> plasma, N<sub>2</sub> plasma.

## I. INTRODUCTION

HIGH-PERFORMANCE low-temperature polycrystalline-silicon thin-film transistors (LTPS-TFTs) with high- $\kappa$  gate dielectrics have been studied in recent years [1]–[5]. High- $\kappa$  gate dielectrics can provide higher gate capacitance density with the same physical thickness due to their high dielectric constant. A higher gate capacitance density can attract more carriers with a smaller gate voltage to fill up the traps that exist in the polycrystalline-silicon channel film. Therefore, the LTPS-TFT with high gate capacitance density could significantly reduce the operation voltage without any defect-passivation treatment [1]–[5]. The threshold voltage  $V_{TH}$  and the subthreshold swing (S.S.) can be significantly reduced by using high- $\kappa$  gate dielectrics instead of conventional thick SiO<sub>2</sub> gate dielectrics [1]–[5]. However, the trap states still exist among the polycrystalline silicon in spite of the employment of high- $\kappa$  gate dielectrics. The NH<sub>3</sub> plasma

Manuscript received July 23, 2008. First published September 16, 2008; current version published October 22, 2008. This work was supported by the National Science Council, Taiwan, under Contract NSC-96-2221-E-009-189. The review of this letter was arranged by Editor A. Nathan.

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Digital Object Identifier 10.1109/LED.2008.2004781

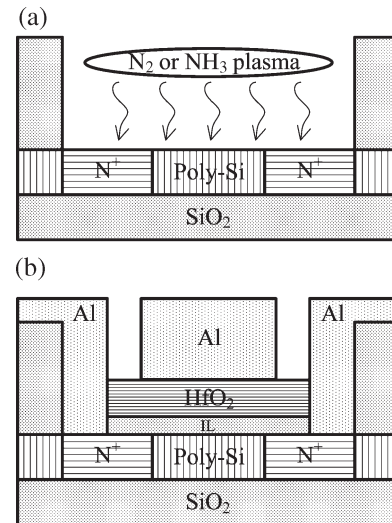


Fig. 1. Cross-sectional view of LTPS-TFT with plasma surface treatment and HfO<sub>2</sub> gate dielectric.

posttreatment is the most general method to passivate the trap states of the polycrystalline-silicon channel film for conventional TFTs [6], [7]. The impacts of NH<sub>3</sub> plasma treatment on the LTPS-TFT with high- $\kappa$  gate dielectric have not been reported yet.

In this letter, the LTPS-TFT with HfO<sub>2</sub> gate dielectric and NH<sub>3</sub> plasma surface treatment is demonstrated for the first time. In addition, N<sub>2</sub> plasma surface treatment is also used to distinguish the impacts of nitrogen and hydrogen species.

## II. EXPERIMENTAL PROCEDURE

The fabrication of devices started by depositing a 50-nm undoped amorphous-Si ( $\alpha$ -Si) layer at 550 °C in a low-pressure chemical vapor deposition system on Si wafers capped with a 500-nm thermal oxide layer. Then, the 50-nm  $\alpha$ -Si layer was recrystallized at 600 °C for 24 h. Then, a 500-nm silicon oxide was deposited by plasma-enhanced chemical vapor deposition at 300 °C for device isolation. The device active region was formed by patterning and etching the isolation oxide. The source and drain (S/D) regions in the active device region were implanted with phosphorus at 15 keV and  $5 \times 10^{15}$  cm<sup>-2</sup>. The S/D was activated at 600 °C for 24 h. Then, NH<sub>3</sub> or N<sub>2</sub> plasma surface treatment was performed for 0, 5, and 15 min at 300 °C with a power density of 1.6 mW/cm<sup>2</sup> in NH<sub>3</sub> or N<sub>2</sub> gas, as shown in Fig. 1(a). The flow rate was 100 sccm at pressure

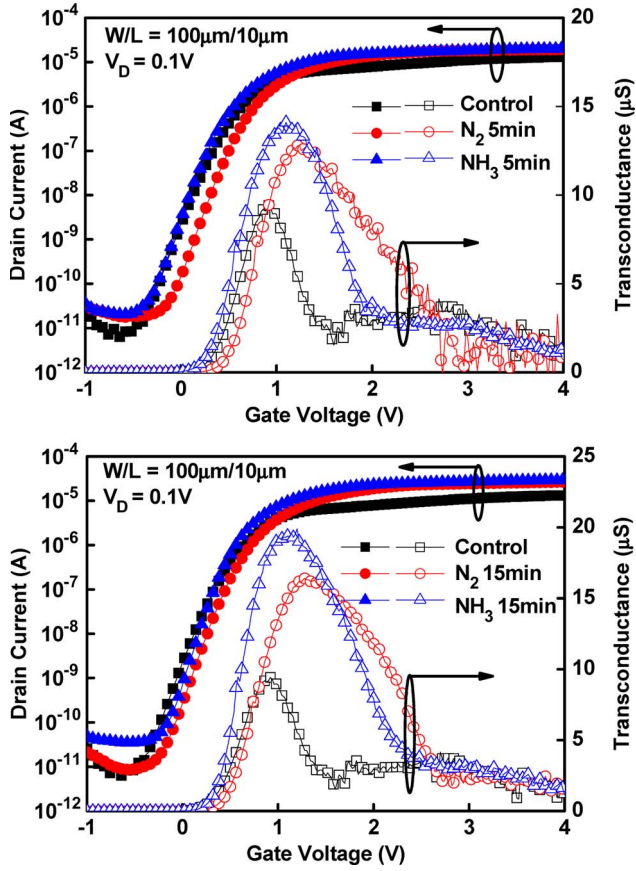


Fig. 2. Transfer characteristics ( $I_D$ - $V_G$  and transconductance  $G_m$ ) of LTPS-TFT with HfO<sub>2</sub> gate dielectric after N<sub>2</sub> and NH<sub>3</sub> plasma surface treatments for 5 and 15 min, respectively. The solid and hollow symbols represent the  $I_D$  and  $G_m$ , respectively.

of 67 Pa. A 50-nm HfO<sub>2</sub> with effective oxide thickness of  $\sim 10.7$  nm was deposited by an electron beam evaporation system at room temperature and pressure of  $5 \times 10^{-6}$  torr without gas flow. An O<sub>2</sub> treatment in furnace was applied to improve the HfO<sub>2</sub> quality at 400 °C for 30 min. The dielectric constant of HfO<sub>2</sub> is about 18.2. After the patterning of S/D contact holes, aluminum was deposited by thermal evaporation system as the gate electrode and S/D contact pad. Finally, the TFT devices were completed by the contact pad definition, as shown in Fig. 1(b). Devices with gate length ( $L$ ) and width ( $W$ ) of 10 and 100  $\mu\text{m}$ , respectively, were measured. The threshold voltage  $V_{TH}$  is defined as the gate voltage at which the drain current reaches  $10 \text{ nA} \times W/L$  and  $V_D = 0.1$  V. The field-effect mobility  $\mu_{FE}$  is extracted from the maximum transconductance ( $G_m$ ).

### III. RESULTS AND DISCUSSION

Fig. 2 shows the transfer characteristics ( $I_D$ - $V_G$  and transconductance  $G_m$ ) of the LTPS-TFT with HfO<sub>2</sub> gate dielectric after N<sub>2</sub> and NH<sub>3</sub> plasma surface treatments for 5 and 15 min, respectively. The important device parameters of LTPS-TFTs are listed in Table I. The S.S.'s of devices show improvements of 8.6% and 9.6% with N<sub>2</sub> plasma surface treatment for 5 and 15 min, respectively. Moreover, the  $\mu_{FE}$ 's

of devices also show increases of 43.7% and 86.0% with N<sub>2</sub> plasma surface treatment for 5 and 15 min, respectively. It is known that S.S. and  $\mu_{FE}$  are related to the dangling-bond deep trap states and the strain-bond tail trap states of the polycrystalline-silicon channel [8], respectively. The significant increase on  $\mu_{FE}$  indicates that nitrogen has better passivation effect on strain-bond tail trap states than on dangling-bond deep trap states. On the other hand, devices show 9.1% and 21.2% S.S. improvements with NH<sub>3</sub> plasma surface treatment for 5 and 15 min, respectively. In addition, the 5- and 15-min NH<sub>3</sub> plasma surface treatments show 51.4% and 112.5%  $\mu_{FE}$  improvements, respectively. It is found that the improvement of S.S. is on the same level by either 5-min N<sub>2</sub> or NH<sub>3</sub> plasma treatment. This implies that hydrogen from NH<sub>3</sub> has less significant contribution to the improvement of S.S. for such a short 5-min treatment. On the contrary, devices with a longer 15-min NH<sub>3</sub> plasma treatment exhibit more S.S. improvement, indicating more passivation effect on the dangling-bond deep trap states due to the contribution of hydrogen. Devices with either 15-min N<sub>2</sub> or NH<sub>3</sub> plasma treatment show significant  $\mu_{FE}$  improvement, indicating that good passivation on strain-bond tail states can be achieved by both plasma treatments. Fig. 3 shows the output characteristics ( $I_D$ - $V_D$ ) of the LTPS-TFT with HfO<sub>2</sub> gate dielectrics after N<sub>2</sub> and NH<sub>3</sub> plasma surface treatments for 5 and 15 min, respectively. For 5 min, N<sub>2</sub> and NH<sub>3</sub> plasma surface treatments show 165.0% and 91.3% driving saturation current  $I_{D\_sat}$  enhancements at  $V_G - V_{TH} = 4$  V and  $V_D = 5$  V, as shown in Table I and Fig. 3. The 5-min N<sub>2</sub> plasma surface treatment shows a smaller  $\mu_{FE}$  improvement and a higher  $I_{D\_sat}$  enhancement than the 5-min NH<sub>3</sub> plasma surface treatment. From Fig. 2, it is noted that the  $\mu_{EF}$  reduction rate after the peak is improved using plasma surface treatment at high  $V_G$ . This improvement is due to the reduced surface roughness scattering [9]. The N<sub>2</sub> plasma-treated device has more improvement on surface roughness scattering than the NH<sub>3</sub> plasma-treated device for 5-min treatment time, resulting in a higher driving saturation current  $I_{D\_sat}$  of the N<sub>2</sub> plasma-treated device. The surface roughness scattering is improved further, leading to 217.0% and 219.6% improvements in driving saturation current for the 15-min N<sub>2</sub> and NH<sub>3</sub> plasma surface treatments, respectively.

In addition to the performance improvement of the HfO<sub>2</sub> LTPS-TFT after plasma surface treatment, the gate capacitance density  $C_G$  also decreased due to the growth of interfacial layer (IL) during the plasma treatment. As shown in Table I, the HfO<sub>2</sub> LTPS-TFT after N<sub>2</sub> plasma surface treatment has lower  $C_G$  than after NH<sub>3</sub> plasma surface treatment, suggesting that the thickness of IL grown by N<sub>2</sub> plasma is thicker than the one grown by NH<sub>3</sub> plasma. The gate leakage current  $I_G$  of HfO<sub>2</sub> LTPS-TFTs after plasma surface treatment at  $V_G - V_{TH} = 2$  V and  $V_{DS} = 0.1$  V are also measured and listed in Table I. Much more  $I_G$  reduction of the N<sub>2</sub> plasma-treated device is observed to consist with the results of decreased  $C_G$ . The effective interface trap states  $N_{it}$ 's and effective grain boundary trap states  $N_{trap}$ 's of the poly-Si channel film were extracted from S.S. and  $I_D$ - $V_G$  curve [10]–[12]. These values are all listed in the Table I. The  $N_{it}$ 's of N<sub>2</sub> plasma-treated devices show a higher initial improvement due to the growth of IL by N<sub>2</sub>

TABLE I  
IMPORTANT DEVICE PARAMETERS OF LTPS-TFT WITH HfO<sub>2</sub> GATE DIELECTRIC AFTER N<sub>2</sub> AND NH<sub>3</sub> PLASMA SURFACE TREATMENTS FOR 5 AND 15 MIN, RESPECTIVELY

| HfO <sub>2</sub> -TFT | V <sub>TH</sub> (V) | S.S. (V/dec.) | I <sub>G</sub> (nA) | C <sub>G</sub> (fF/μm <sup>2</sup> ) | μ <sub>FE</sub> (cm <sup>2</sup> /V·s) | N <sub>trap</sub> (cm <sup>-2</sup> ) | N <sub>it</sub> (cm <sup>-2</sup> ) | I <sub>D,sat</sub> (mA) |
|-----------------------|---------------------|---------------|---------------------|--------------------------------------|--|---------------------------------------|-------------------------------------|-------------------------|
| Control               | 0.33                | 0.198         | 0.195               | 3.22                                 | 29.19                                  | 4.87x10 <sup>12</sup>                 | 4.67x10 <sup>12</sup>               | 0.311                   |
| N <sub>2</sub> 5min   | 0.5                 | 0.181         | 0.0333              | 3.05                                 | 41.96                                  | 4.85x10 <sup>12</sup>                 | 3.88x10 <sup>12</sup>               | 0.824                   |
| NH <sub>3</sub> 5min  | 0.28                | 0.180         | 0.193               | 3.19                                 | 44.20                                  | 3.96x10 <sup>12</sup>                 | 4.02x10 <sup>12</sup>               | 0.595                   |
| N <sub>2</sub> 15min  | 0.45                | 0.179         | 0.0233              | 3.02                                 | 54.30                                  | 4.55x10 <sup>12</sup>                 | 3.78x10 <sup>12</sup>               | 0.986                   |
| NH <sub>3</sub> 15min | 0.33                | 0.156         | 0.191               | 3.16                                 | 62.02                                  | 3.87x10 <sup>12</sup>                 | 3.19x10 <sup>12</sup>               | 0.994                   |

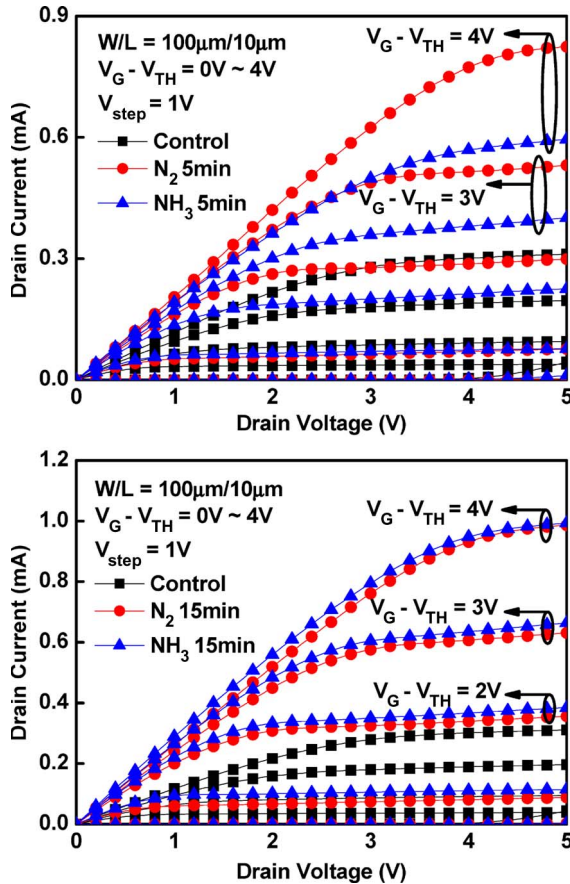


Fig. 3. Output characteristics ( $I_D$ - $V_D$ ) of LTPS-TFT with HfO<sub>2</sub> gate dielectric after N<sub>2</sub> and NH<sub>3</sub> plasma surface treatments for 5 and 15 min, respectively.

plasma treatment. However, for longer 15-min plasma treatment, the effect of NH<sub>3</sub> plasma on  $N_{it}$  is greater than that of N<sub>2</sub> plasma due to hydrogen incorporation. In addition, as shown in Table I, NH<sub>3</sub> plasma treatment shows greater passivation effect on grain boundary traps  $N_{trap}$ 's compared to N<sub>2</sub> plasma treatment.

High-performance LTPS-TFT with low threshold voltage  $V_{TH} \sim 0.45$  V, excellent S.S.  $\sim 0.179$  V/decade, and high field-effect mobility  $\mu_{FE} \sim 54.30$  cm<sup>2</sup>/V·s is obtained by using HfO<sub>2</sub> gate dielectric and 15-min N<sub>2</sub> plasma surface treatment. In addition, high-performance LTPS-TFT with low threshold voltage  $V_{TH} \sim 0.33$  V, excellent S.S.  $\sim 0.156$  V/decade, and high field-effect mobility  $\mu_{FE} \sim 62.02$  cm<sup>2</sup>/V·s is also obtained by using HfO<sub>2</sub> gate dielectric and 15-min NH<sub>3</sub> plasma surface treatment.

#### IV. CONCLUSION

In this letter, high-performance LTPS-TFT with HfO<sub>2</sub> gate dielectric has been fabricated. In order to enhance the performance of the LTPS-TFT with high- $\kappa$  gate dielectric, two kinds of plasma, N<sub>2</sub> and NH<sub>3</sub>, are employed. S.S., field-effect mobility  $\mu_{FE}$ , and driving saturation current are all significantly improved after N<sub>2</sub> and NH<sub>3</sub> plasma surface treatments.

#### ACKNOWLEDGMENT

The authors would like to thank the process support from National Nano Device Laboratories and the Nano Facility Center, National Chiao Tung University, Hsinchu, Taiwan, R.O.C.

#### REFERENCES

- [1] T.-M. Pan and T.-W. Wu, "High-performance polysilicon TFTs using stacked Pr<sub>2</sub>O<sub>3</sub>/oxynitride gate dielectric," *IEEE Electron Device Lett.*, vol. 29, no. 4, pp. 353–356, Apr. 2008.
- [2] C.-W. Chang, C.-K. Deng, J.-J. Huang, H.-R. Chang, and T.-F. Lei, "High-performance poly-Si TFTs with Pr<sub>2</sub>O<sub>3</sub> gate dielectric," *IEEE Electron Device Lett.*, vol. 29, no. 1, pp. 96–98, Jan. 2008.
- [3] M.-J. Yang, C.-H. Chien, Y.-H. Lu, G.-L. Luo, S.-C. Chiu, C.-C. Lou, and T.-Y. Huang, "High-performance and low-temperature-compatible p-channel polycrystalline-silicon TFTs using hafnium-silicate gate dielectric," *IEEE Electron Device Lett.*, vol. 28, no. 10, pp. 902–904, Oct. 2007.
- [4] C.-P. Lin, B.-Y. Tsui, M.-J. Yang, R.-H. Huang, and C. H. Chien, "High-performance poly-silicon TFTs using HfO<sub>2</sub> gate dielectric," *IEEE Electron Device Lett.*, vol. 27, no. 5, pp. 360–363, May 2006.
- [5] B. F. Hung, C. C. Chiang, C. C. Huang, A. Chin, and S. P. McAlister, "High-performance poly-silicon TFTs incorporating LaAlO<sub>3</sub> as the gate dielectric," *IEEE Electron Device Lett.*, vol. 26, no. 6, pp. 384–386, Jun. 2005.
- [6] H.-C. Cheng, F.-S. Wang, and C.-Y. Huang, "Effects of NH<sub>3</sub> plasma passivation on n-channel polycrystalline silicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 44, no. 1, pp. 64–68, Jan. 1997.
- [7] F.-S. Wang, M.-J. Tsai, and H.-C. Cheng, "The effects of NH<sub>3</sub> plasma passivation on polysilicon thin-film transistors," *IEEE Electron Device Lett.*, vol. 16, no. 11, pp. 503–505, Nov. 1995.
- [8] I.-W. Wu, T.-Y. Huang, W. B. Jackson, A. G. Lewis, and A. C. Chiang, "Passivation kinetics of two types of defects in polysilicon TFI by plasma hydrogenation," *IEEE Electron Device Lett.*, vol. 12, no. 4, pp. 181–183, Apr. 1991.
- [9] K. Onishi, C. S. Kang, R. Choi, H. J. Cho, S. Gopalan, R. E. Nieh, S. A. Krishnan, and J. C. Lee, "Improvement of surface carrier mobility of HfO<sub>2</sub> MOSFETs by high-temperature forming gas annealing," *IEEE Trans. Electron Devices*, vol. 50, no. 2, pp. 384–390, Feb. 2003.
- [10] C. A. Dimitriadis, P. A. Coxon, L. Dozsa, L. Papadimitriou, and N. Economou, "Performance of thin-film transistors on polysilicon films grown by low-pressure chemical vapor deposition at various pressures," *IEEE Trans. Electron Devices*, vol. 39, no. 3, pp. 598–606, Mar. 1992.
- [11] J. Levinson, F. R. Shepherd, P. J. Scanlon, W. D. Westwood, G. Este, and M. Rider, "Conductivity behavior in polycrystalline semiconductor thin film transistors," *J. Appl. Phys.*, vol. 53, no. 2, pp. 1193–1202, Feb. 1982.
- [12] R. E. Proano, R. S. Misage, and D. G. Ast, "Development and electrical properties of undoped polycrystalline silicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 36, no. 9, pp. 1915–1922, Sep. 1989.