規則化量子點成長及一維量子傳輸之研究

研究生：李晃銘　　　　　　　　　　　　指導教授：張翼 博士

國立交通大學材料科學與工程研究所

摘要

本論文致力於低維度半導體結構之研究，主要包含兩部份：規則化量子點成長及一維量子傳輸效應。在進入兩大主軸前，首先介紹電子束微影技術，並展示其結合熱回流光阻技術來製作奈米T形閘極。

在第一部份裡，我們展示自組鍺點受控制地排列在圖形化矽(001)基板上。而這些鍺點的尺寸估計為10奈米左右，並傾向沿著矽高台邊緣成長，且矽圖形排列能控制鍺點的分佈。另外，進一步以局部間接張力表面化學能模型來計算鍺點在圖形化矽高台上的成長及分佈情形，模擬的結果和實驗部份相當符合，顯示或許基材的表面形貌，能增進鍺點成長於矽基材上的規則化及均勻度。

在第二部份裡，以三閘極結構來研究一維狹窄制限的電子傳輸特性。元件種類包含單量子井及雙量子井砷化鎵/砷化鋁鎵異質結構兩種。一方面，著重於單量子井元件，發現固定表面模型，能合理描述對於不同通道寬度及長度在中央閘極電壓為零時的截止電壓。比較有無中央閘極的樣品，發現中央閘極即使為零偏壓時，也顯著地影響表面位能，從而促進在較深的二維電子氣體中的一維制限。非線性傳輸量測顯示出次能帶能量分離隨著中央閘極電壓呈線性變化，並在中央閘極為0.8V時可以提高70%。另外，以一個簡單的模型來計算最低的次能帶能量分離，模擬的結果和實驗整體行為相當一致。籍由加一正中央閘極電壓，可大大抑制偶然在長通道(寬度大於1μm)發現的雜質效應，由此提高最低的次能帶能量分離。此外，也呈現出所謂低於第一個傳導高原的0.7異常傳輸現象，顯示三閘極結構，在一維系統中，很適合來做電子密度相關的研究。另一方面，我們著重在雙量子井元件。利用各別歐姆接點製程技術，成功地製作垂直排列制限，並觀察到兩層各別的傳導特性，發現上量子井的次能帶能量分離比下量子井大。最後，也觀察到狹窄制限所造成的少量的拖拉訊號。

The Study of Regular Quantum Dots Growth and One-Dimensional Quantum Transport

Student: Huang-Ming Lee Advisor: Dr. Edward Yi Chang

Department of Materials Science and Engineering
National Chiao Tung University

Abstract

This dissertation is devoted to the study of low-dimensional semiconductor structures and mainly consists of two parts: regular quantum dots growth and one-dimensional (1D) quantum transport. Prior to getting into the two parts, the electron beam lithography incorporating thermally reflowed resist technique for fabricating nanometer T-shaped gate is introduced and demonstrated.

In the first part, the controlled placement of self-organized Ge dots on patterned Si (001) substrate is presented. The sizes of the Ge dots are characterized and estimated to be around 10 nm. The Ge dots tend to form along the Si mesa edge, and their distribution could be controlled by the pattern arrangement. In addition, the formation of Ge dots on patterned Si mesas was further calculated by a local strain-mediated surface chemical potential. The simulation results are quite consistent with the experimental data. It may be possible using substrate morphology to improve the ordering and uniformity of the Ge dots formed on Si substrate.

In the second part, the transport characteristics on 1D narrow constrictions defined by a triple-gate structure are investigated. The device structures include single quantum well (SQW) and double quantum well (DQW) GaAs/Al$_x$Ga$_{1-x}$As heterostructures. On one hand, we focus on SQW device. The pinch-off voltages at zero center gate voltage (V_{CG}) for various channel widths W (= 0.4-0.8 μm) and lengths L (= 0.2-2 μm) are well described by pinned-surface model. Comparison between samples with and without a center gate reveals that the center gate, even when zero-biased, significantly affects the surface potential and thereby facilitates the 1D confinement in a deep 2DEG. Nonlinear transport spectroscopy shows that subband energy separation (ΔE) changes linearly with V_{CG} and can be enhanced by 70% for $V_{\mathrm{CG}} = 0.8$ V. A simple model is used to calculate the lowest subband energy separation ($\Delta E_{1,2}$), which well reproduces the overall behavior of the measured $\Delta E_{1,2}$. In addition, effects of impurities, occasionally found for long-channel devices ($L \geq 1$ μm), are shown to be greatly suppressed by applying a positive V_{CG} and thereby enhancing $\Delta E_{1,2}$. We also present data for the transport anomaly below the first conductance plateau, the so-called '0.7 anomaly', to demonstrate that the triple-gate structure is useful for the study of density-dependent phenomena in a 1D system. On the other hand, we put emphasis on DQW device. The upper electron layer is supplied via modulation doping, while the lower one is induced through back gate. Vertically aligned constrictions in DQW with separate Ohmic contacts have been fabricated. Clear conductance plateaus for both layers were observed showing that ΔE of the upper quantum well is larger than that of the lower quantum well. Finally, the frictional drag signal caused by narrow constriction was observed.

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Fig. 4-31. Depletion characteristics of DQW sample as a function of V_{IG} with V_{BG} varied from 0 to 4 V at 4.2 K. A constant 10 mV is fed to small contact and the current is measured by another big ohimc contact.

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