Chapter 1

Introduction

1.1 Research Background of Low-Dimensional Semiconductor Structures

The definition of the low-dimensional (LD) semiconductor structures comes from considering the description of a wide range of artificial solid semiconductor structures, in which the physical properties differ significantly from those of bulk solids. In terms of dimensionality, at least in one spatial direction the length scale of the structure is made to be very small. The electrical and optical properties of these semiconductor structures are thus defined locally, and phenomena related to extremely small dimensions become more important than the actual chemical properties of the constituent materials. With the ongoing progress of sophisticated epitaxial growth techniques, such as molecular beam epitaxy (MBE) and metal-organic vapor phase epitaxy, the investigations of the exciting physical properties of these LD structures have become possible. The new epitaxial growth techniques mainly started in the late sixties and have now reached a level that the structural perfection and the spatial dimension of the artificial layers can be controlled on the atomic scale [1]-[3]. With the new growth technique, the first layered heterostructures were proposed at seventies [4], which is called quantum well. Typically, when a small bandgap material, with a layer thickness comparable with the carrier (electron or hole) de Broglie wavelength, is sandwiched between larger gap materials, either electrons or holes or both types of carrier find their motion confined in the direction of crystal growth, i.e. normal to the layers. Confinement of electrons

or holes thus leads to quantization of energy. Therefore, the conduction and valance bands split into a set of discrete energy states. The motion parallel to the layer remains unconfined, and so the system becomes two-, one- or even zero-dimensional depending on the reduction in the degrees of freedom for motion.

In two-dimensional (2D) system, during the seventies, the Si metal-oxide-semiconductor (MOS) field-effect transistor was the most extensively studied 2D system where the two dimensional electron gas (2DEG) is formed at the Si-SiO_2 interface, in the potential well arising from the creation of an inversion layer by applying a positive bias to the gate electrode. In the late seventies, research in 2D system has moved from Si to structures based on the heterojunctions of large and small gap semiconductors. Among them, the GaAs/$Al_xGa_{1-x}As$ system attracted most attention because it exhibits quantum confinement effects far superior to those in the Si MOS system due to the following advantages: (1) GaAs is a direct band gap material and as a result is suitable for manufacturing of very efficient light sources, such as light emitting diodes and laser diodes. (2) Due to its lower effective mass and also being separated from donor layer, the electron mobility in GaAs heterostructure is extremely high which makes it suitable for applications in high speed transistors and microwave devices such as high electron mobility transistors (HEMTs), heterojunction bipolar transistors, etc.

With further reduction of dimensions in the 2D GaAs/$Al_xGa_{1-x}As$ system, either by etching or evaporated surface metal gate techniques [5], [6], the quasi one-dimensional (1D) structure can be obtained. Instead of using etching methods, most of the reported works used split-gate structures to get quasi 1D due to the advantage of tunability of the quasi 1D channel and its electric subband energy. If the transport length scale is rather larger than both the length and the width of the

artificial quasi 1D channel, carriers can pass through the channel without any scattering, leading to ballistic transport. The most dramatic consequence in this regime is the quantized conductance observed in the units of $2e^2/h$. In addition, the zero-dimensional (0D) structure, quantum dot, can be made as well by using two-pairs of split-gate structures [7], in which the electron-electron interaction leads to Coulomb blockade and single-electron charging effects in electrical transport [8].

More recently, considerable efforts have been devoted to the realization of semiconductor quantum nanostructures on semiconductor surfaces [9]-[12], as a result of their potential applications for the electronic and optoelectronic device [13]-[15]. These nanostructures are very small three-dimensional (3D) systems whose dimension ranges from nanometers to tens of nanometers. The size is smaller than the de Broglie wavelength of slow electrons; therefore quantum effects are manifest in the structures. Among these nanostructures, the Ge-Si heterostructures promise wide applications in new micro- and opto-electronic devices due to its compatibility with Si-based electronics industry [16], which continuously follows an exponential progress based on scaling down silicon transistors. Since the first observations of Ge dots on Si (001) grown by MBE [17], many investigations [18]-[20] have been performed in order to study the growth mechanism and physical properties of these nanostructures. Actually, the deposition of pure Ge on Si is commonly described as a classic Stranski-Krastanow (SK) process [21]. In this growth mode, the 3D Ge dots are formed with defect-free, high-quality properties. However, this kind of growth usually generates a random formation of the Ge dots with a non-uniform and unpredictable spatial distribution, resulting in large inhomogeneous broadening in the energy spectrum. Thus, the greatest challenge in applying these dots is to control their lateral ordering and the uniformity of their sizes on a flat Si (001) substrate.

1.2 Overview of the Dissertation

This dissertation is devoted to the study of the LD semiconductor structures and is mainly classified into two subjects. The first subject is concerned with Ge dots on patterned Si substrates while the second one presents the characteristics of electronic transport in 1D constriction. Overall, the dissertation is divided into 5 chapters, including:

In chapter 2, before going through the main subjects, the EB lithography technique used in this dissertation is first introduced. We describe the typical process steps of the EB lithography in our laboratory. In addition, the standard EB lithography incorporating thermally reflowed resist technique to fabricate the nanometer T-shaped gate is demonstrated. A successful lift-off structure with 30-nm opening is achieved with a reflow temperature of 125 ℃ and the reflow time of 75 sec in this study.

In chapter 3, we get into the first subject concerning with the controlled placement of self-organized Ge dots on patterned Si (001) substrate. The Si templates include dot and anti-dot mesas, which are patterned by EB lithography and subsequent reactive ion etching (RIE). The sizes of the formed Ge dots are approximately estimated to be 10 nm, which was characterized by atomic force microscopy (AFM) and scanning electron microscopy (SEM). Due to the energetically favorable sites, the Ge dots tend to form along the Si mesa edge, and their distribution could be controlled by the pattern arrangement. In addition, the formation of Ge dots on patterned Si mesas was further calculated. The simulation results are quite consistent with the experimental data for Si dot and anti-dot mesas. Also, the calculated results clearly show that it may be possible using substrate morphology to improve the ordering and uniformity of the Ge dots formed on Si substrate.

In chapter 4, we investigate the transport characteristics on 1D narrow constriction. Two kinds of device structure were grown and studied including single quantum well (SQW) and double quantum well (DQW) GaAs/$Al_xGa_{1-x}As$ heterostructures. On one hand, we focus on SQW device and examine a simple triple-gate structure that incorporates an additional center gate in between the pair of split gates. Comparison between samples with and without a center gate reveals that the center gate, even when zero-biased, significantly affects the surface potential and thereby facilitates the 1D confinement in a deep 2DEG. Nonlinear transport spectroscopy shows that subband energy separation (ΔE) changes linearly with the center gate voltage (V_{CG}) and can be enhanced by 70% for V_{CG} = 0.8 V. A simple model is used to calculate the lowest subband energy separation ($\Delta E_{1,2}$), which well reproduces the overall behavior of the measured $\Delta E_{1,2}$. In addition, effects of impurities, occasionally found for long-channel devices, are shown to be greatly suppressed by applying a positive V_{CG} and thereby enhancing $\Delta E_{1,2}$. We also present data for the transport anomaly below the first conductance plateau, the so-called '0.7 anomaly', to demonstrate that the triple-gate structure is useful for the study of density-dependent phenomena in a 1D system. On the other hand, we put emphasis on the device equipped with DQW. In our DQW device, instead of having tunneling observed, two wells behave as isolated wells due to thicker barrier (~ 22 nm). The upper electron layer is supplied via conventional modulation doping, while the lower layer is induced through the field effect from a highly-doped Si-GaAs back gate. To observe Coulomb drag behavior, vertically aligned constrictions in DQW with separate ohmic contacts have been successfully fabricated. The 2DEG in both layers can be operated independently through isolation gate and focus ion beam (FIB) lithographic back gate. Clear conductance plateaus for both layers were observed

showing that ΔE of the upper quantum well is larger than that of the lower quantum well. The transconductance plot of the DQW sample shows that two layers can be simultaneously pinch-off when applying suitable biases to center gate and back gate and there is no tunneling observed in between. Finally, the frictional drag signal caused by narrow constriction was observed.

In chapter 5, important conclusions are drawn. Including: (1) The fabrication of the T-shaped gate with thermally reflowed resist technique is demonstrated. (2) The controlled placement of self-organized Ge dots on Si dot and anti-dot mesa is investigated both on experiment as well as numerical calculation. (3) Transport characteristics on 1D narrow constriction defined by a triple-gate structure is systematically studied including SQW and DQW device structures. Especially, we successfully achieve the vertically aligned constrictions in DQW with separate ohmic contacts and observe frictional drag signal caused by narrow constriction.

1.3 References

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Chapter 2

Electron Beam lithography Incorporating Reflowed Resist Technique

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In this chapter, the novel technique which combines EB lithography and thermally reflowed resist technique is presented. First, the EB lithography technique in our laboratory is introduced. Second, the standard EB lithography incorporating thermally reflowed resist technique to form the expected resist profile for nanometer T-gate formation is demonstrated.

2.1 Introduction to Electron Beam Lithography

Electron Beam (EB) Lithography refers to a lithographic process that uses a focused beam of electrons to create the extremely fine circuit patterns required by the modern electronic industry for integrated circuits as well as for fundamental research, in contrast with optical lithography which uses light for the same purpose. Due to the superiority of the shorter material wavelength (0.2-0.5 angstroms) of electrons, this technique is so far widely employed to perform a variety of scientific purposes that generally consist of the studies of bio-electronic devices, opto-electronic devices, quantum structures, semiconductor/superconductor interfaces, optical devices and so on. Derived from the early scanning electron microscopes, a conventional EB lithography system comprises a scanning EB across a substrate coated with a resist film, polymer (methyl methacrylate)(PMMA), which is sensitive to electrons, followed directly defining nanometer patters in the resist film through computer-aid

design and beam blacking system without any photo mask design in advance. Detailed functions of the EB lithography system are as shown in figure 2-1.

In comparison with optical lithography system, EB lithography has the following advantages, including improved resolution, great depth of field, excellent level-to-level overlay tolerance, easy pattern and absence of mask defects. Improved resolution leads to the ability to focus EB to spot sizes much smaller than optical resolutions, even to diameters below 10 nm. Spot size, however, is not the resolution determining factor. Instead, the electron scattering in the resist layer and backscattering from the substrate are the main limiting factors. Because the EB process does not use a photo mask, there are no mask defects to degrade the image. Also, the pattern is designed and stored in computer which can be changed or modified rapidly. On the other hand, it also takes some disadvantages that it is slow, being one or more orders of magnitude slower than optical lithography. Unlike a masking operation, each pattern must be individually drawn by the EB. Patterns comprising a large area will necessarily require a long writing time. Also, it is quite expensive and complicated that require frequent maintenance to keep its performance.

Typically, the process flowchart of this technique in our laboratory can be illustrated as can be seen in Fig. 2-2. First, the pre-etched wafer performed using conventional optical lithography was degreased with acetone (ACE) and isopropyl alcohol (IPA) and rinsed in the de-ionized water for 10 minutes, respectively. After blowing dry with nitrogen gas and baking in hotplate at 110 ℃ for 5 minutes, the wafer was spin-coated with a thickness of around 300 nm PMMA as EB resist and then baked in hotplate at 250 ℃ for 3 minutes. After exposing at Leica EBML300 EB direct writing system and developing in methyl isobutyl ketone (MIBK): IPA (1:3) for 100 sec and rinsing in an IPA for 30 sec, well-defined PMMA trenches were formed

on the pre-etched mesas for subsequent gate metal deposition. Just before metallization, the wafer should be treated with an oxygen based descum and dilute HCl dip to remove surface oxide to assure metal adhesion. Following an electron gun evaporation system was used to deposit metal film. After metallization, the metal patterns were transferred utilizing lift-off process in which we usually put the sample in ACE for over night to make sure that the unwanted metal films and residual resist can be easily and smoothly peeled off.

2.2 Nanometer T-Gate Fabricated by Thermally Reflowed Resist Technique

2.2.1 Introduction

Advances in nanofabrication tools, techniques and material growth methods, high performance devices such as GaAs and InP-based HEMTs are currently attracting great interests and investments. Actually, they are considered as the most promising candidates for active devices used both high-speed digital integrated circuit (ICs) and millimeter-wave and microwave analog ICs. In order to improve the device performance, submicron T-shaped gates, in addition to high mobility device structures, are usually used to achieve higher cut-off frequency (f_T) and higher maximum oscillation frequency (f_{max}) for the devices. Therefore, a well-controlled nanolithography technology is a strong requirement for the fabrication of high frequency devices. So far, a number of processes [1]-[5] have been reported. Yamashita et al. [1] succeeded in fabricating 25-nm-T-shaped gates by combining EB lithography and plasma chemical vapor deposition (CVD) with conventional RIE to define a multilayer resist and resulted in a device with f_T of 396 GHz. Suemitsu et al.

[2], [3] have demonstrated a fabrication technology utilizing a fullerene-incorporated nanocomposite resist for EB lithography and a two-step-recessed gate structure [4] and have succeeded in fabricating InAlAs/InGaAs HEMTs with an f_T of 352 GHz. However, the T-gate fabrication steps described above were too complicated. InP based HEMTs with gate length ranging from 0.06 to 0.2 μm [5] were fabricated by using triple resist layer structures, which consist of a bottom layer of PMMA, a middle layer of poly(dimethylglutarimide)(PMGI), and a top layer of PMMA. However, there were too many developers used to enable the fine gate formation for this process. Other nanometer gate processes that combined optical and EB lithography [6] have also been reported, however, all the processes require accurate alignment and highly sophisticated mask design.

In this study, a simple technique for the fabrication of the nanometer T-gate was developed. Standard EB lithography and thermally reflowed resist technique [7], [8] were employed to form the expected resist profile for nanometer T-gate formation. High-resolution scanning electron microscope (SEM) was then used to measure the dimension of the nanometer footprint. Ultra-short 30-nm T-shaped gate on GaAs substrate was realized, and the optimum conditions for the formation of smallest gaps of T-gate footprints were obtained.

2.2.2 Experimental method

Figure 2-3 summarizes the bilayer resist process steps for the fabrication of the nanometer T-gates. First, typical 160-nm-T-gate trenches were formed by exposing at the Leica EBML300 EB direct writing system at 40KeV with a thermionic LaB_6 filament emitter and using the bilayer EB resists which consist of a 250 nm bottom

high-resolution PMMA layer and a 720 nm top sensitive polymethyl methacrylate-methacrylic acid P(MMA-MAA) layer. Then, single center exposure and added sidewall exposure were used to define both the footprint and the head of the T-gate by modulating the exposure doses. After EB exposure, the samples were developed in a developer of MIBK and IPA (1:3) for 100 sec and then rinsed in an IPA for 30 sec and blown dry with nitrogen. In addition, all samples were descumed using inductively coupled plasma (ICP) in a 1:3 gas mixture of O_2 and Ar for 20 sec. The wafers were then sequentially cleaned with 1:10 HCl: H_2O solution for 60 sec and then rinsed in water for 60 sec and blown dry with nitrogen to ensure that the thin oxide layer on the GaAs surface were removed to assure metal adhesion. After development and descum, the photoresist was thermally reflowed using a hotplate on the bottom which ensures the uniform heat transform to the bottom resist, PMMA. Through optimal reflow temperature and heating time, the resist structures were reflowed to form the nanometer T-gate foot openings without any substantial change to the top P(MMA-MAA) layer and the desired lift-off structure for T-gate formation was maintained. Finally, Ti/Pt/Au Schottky layers were sequentially deposited on the GaAs substrate at a temperature below 50 ℃ by electron gun evaporation with a deposition distance of about 60 cm. After lift-off process, the nanometer T-gates with thickness of about 500 nm were formed on the GaAs substrate.

2.2.3 Results and Discussion

Figure 2-4 (a) to (c) are the cross-sectional SEM images of the photoresist and the T-gate formed during the process. Figure 2-4(a) shows the as-developed bilayer resist structure with gate length of about 160 nm and resist thickness of about 1000

nm after the resist was developed. Figure 2-4(b) exhibits the thermally reflowed resist configuration. Figure 2-4(c) is the T-gate formed after lift-off process with thickness of about 500 nm and the gate length at the bottom of the T-shaped gate is 30 nm. As can be seen from the SEM images in Fig. 2-4, the bottom resist PMMA was successfully shrunk to form the desired footprint opening of about 30 nm without any obvious change on the top P(MMA-MAA) layer.

Figure 2-5 shows the critical dimension (C.D.) of the observed gate length versus reflow time with different reflow temperatures. As can be seen in this figure, the gate length decreases with increasing thermal reflow time. Furthermore, the reflow temperature also influences the thermal reflow process. When the reflow temperature was 135 ℃, a highly sensitive relationship (~3.5 nm/sec) between gate length and reflow time is observed. However, the high sensitivity of the gate length on the reflow time leads to difficult process control and results in a small process window. As the reflow temperature was decreased to 115 ℃, the shrinking effect between gate length and the reflow time is not so significant. Consequently, an optimal reflow temperature of 125 ℃ was chosen for nanometer gate fabrication. In addition, the results of the distributions of the pattern-sizes with different reflow time at a fixed reflow temperature of 125 ℃ are shown in Fig. 2-6. For each reflow time, the sizes of the gate lengths were measured at different locations across the 3-inch GaAs wafer. When the reflow time reached 90 sec, the openings of the gate lengths on the GaAs substrate were covered with the reflowed resist which led to the failure in the following lift-off process. By combining the results indicated in Fig. 2-5 and Fig. 2-6, a lift-off structure with 30-nm opening was achieved with a reflow temperature of 125 ℃ and the reflow time was 75 sec in this study.

2.2.4 Summary

In summary, a novel method for fabricating ultra-short 30-nm T-gate on the GaAs substrate by combining advanced EB lithography and thermally reflowed resist technique has successfully been demonstrated. The effects of reflow temperature and reflow time on the gate length formed were illustrated. The typical as-developed 160-nm-T-gate patterns can be easily shrunk to nanometer scale in length ranging from 150nm to 30 nm after a simple thermal reflow procedure without any substantial change to the top layer resist structure of the T-gate. Finally, a 30 nm T-gate was demonstrated using this reflow technique which is the smallest T-gate with the thermally reflowed technique reported in the literature so far and can practically be used in the GaAs monolithic microwave integrated circuit (MMIC) fabrications.

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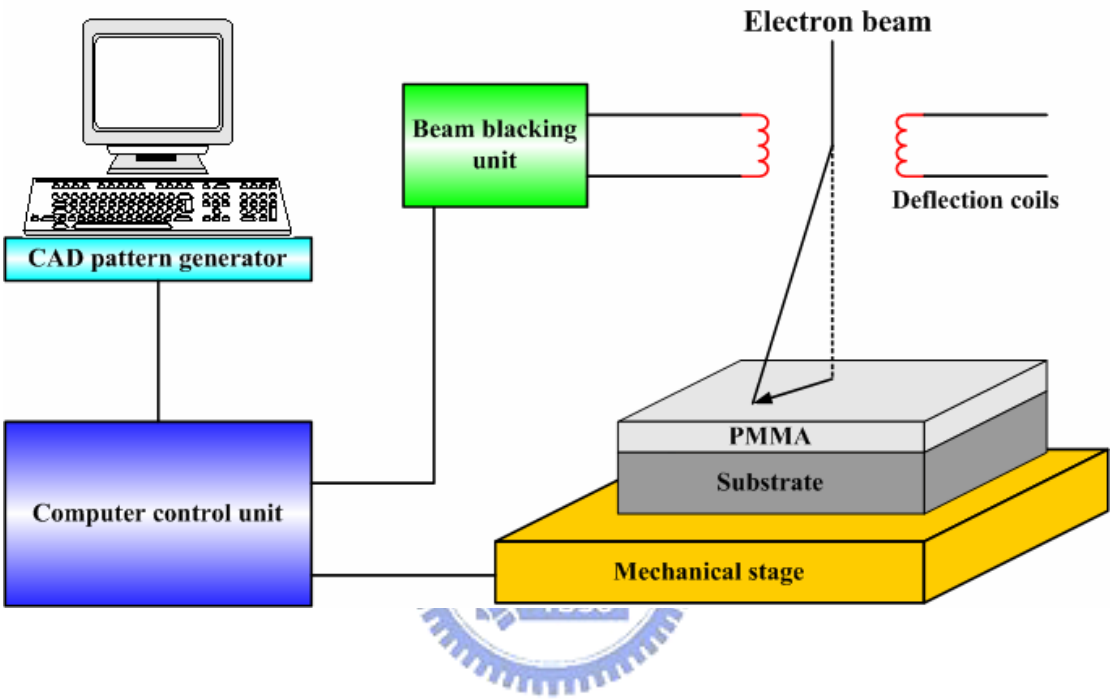


Fig. 2-1. Schematic diagram of the EB control system. First, a computer-aid design (CAD) pattern was generated using UNIX workstation and transferred to the computer control unit. Second, the CAD pattern was transformed to executable job file that accordingly control the beam blacking unit and mechanical stage to manipulate the EB to directly deposit energy on specific positions.

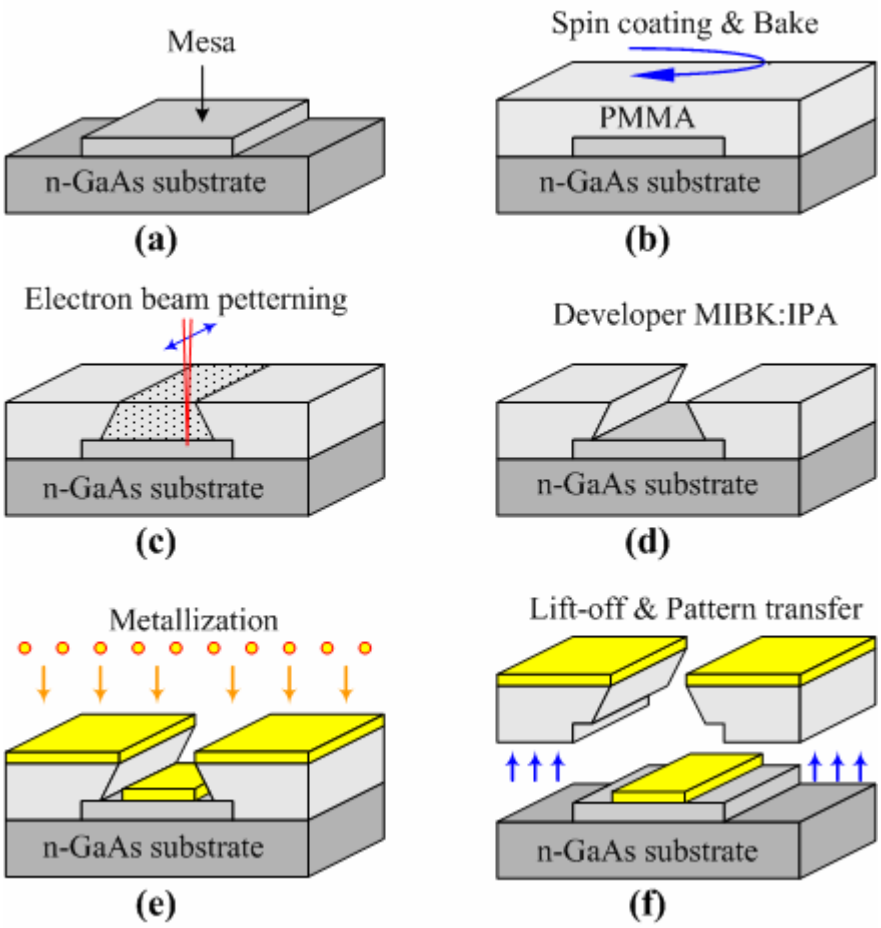


Fig. 2-2. Schematic process steps of the EB lithography in our laboratory. (a) The mesa formed using optical lithography process was chemically cleaned. (b) An EB resist, PMMA, was spin-coated and baked in hotplate. (c) The EB was used to define desired patterns. (d) A developer of MIBK and IPA (1:3) was prepared to etch the resist exposed by EB. (e) Ti/Au metals were deposited using electron gun evaporation. (f) The expected patterns were transferred by lift-off process.

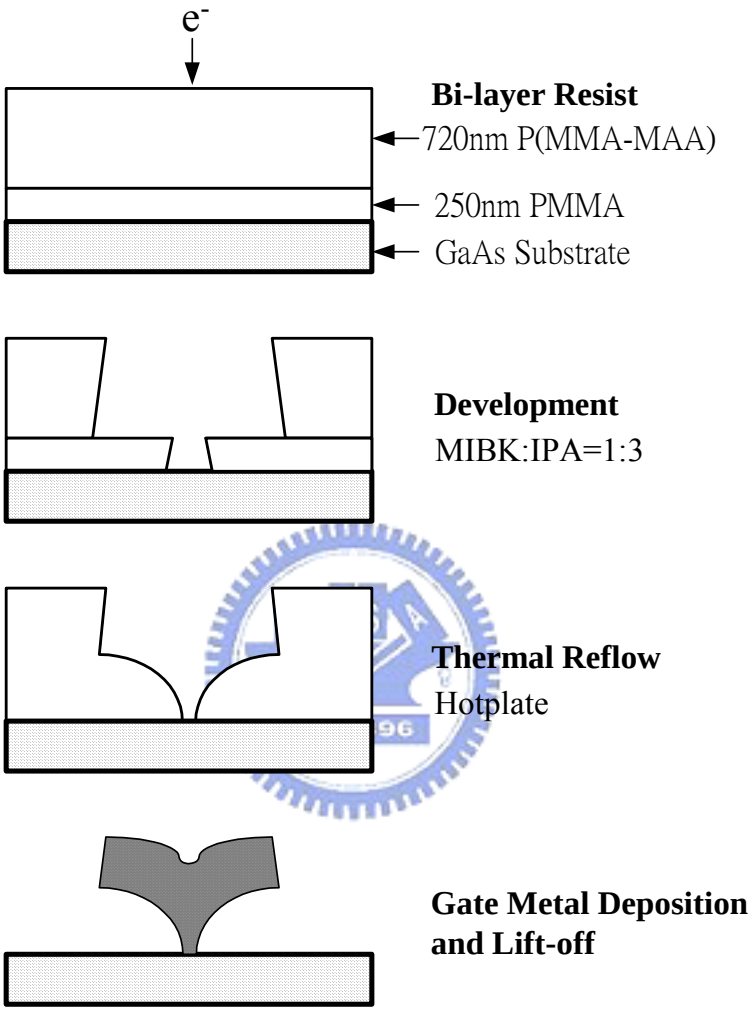
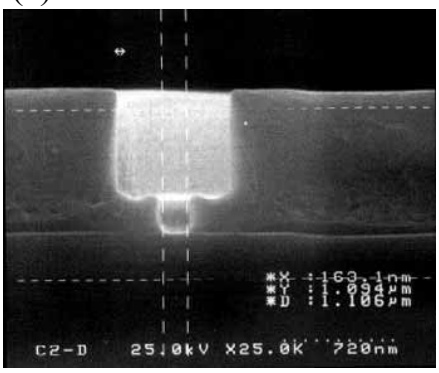
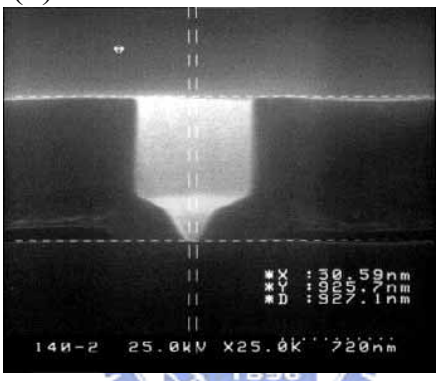


Fig. 2-3. Process flow of the thermally reflowed T-gate.

(a)



(b)



(c)

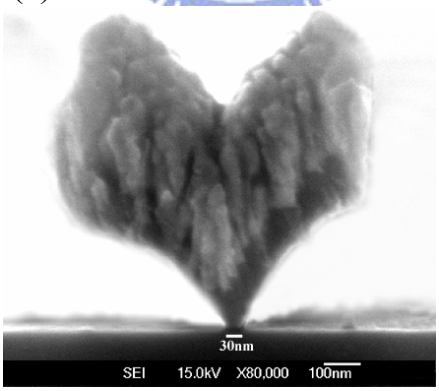


Fig. 2-4. SEM cross-sectional images of (a) as-developed resist structure, (b) thermally reflowed resist configuration and (c) 30-nm-T-gate after lift-off.

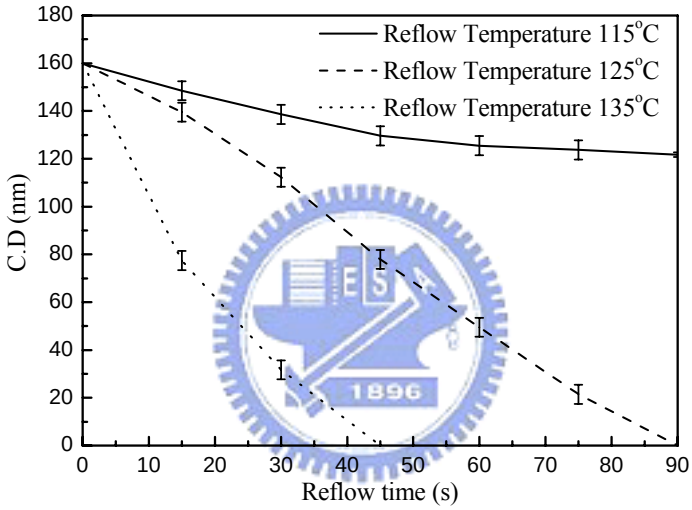


Fig. 2-5. Dependence of different reflow temperature and reflow time on critical dimension (C.D.) of gate length for thermal reflow technique.

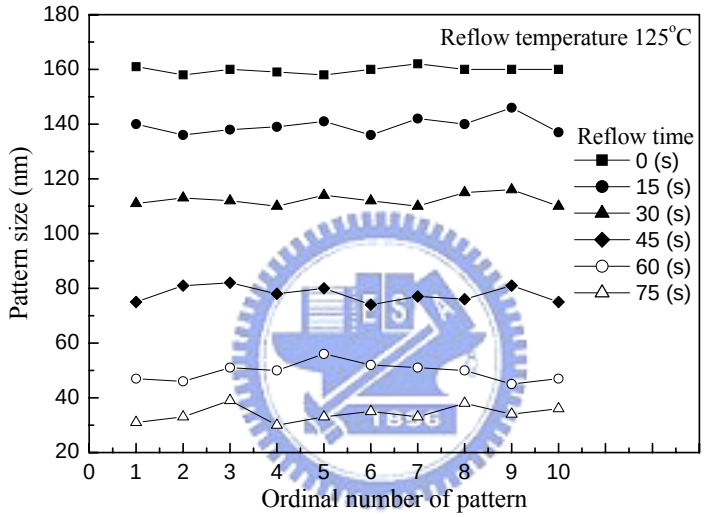


Fig. 2-6. Distributions of the pattern-sizes across the wafer with different reflow time at a fixed reflow temperature of 125 ℃ (Total 10 data points across the wafer for each reflow time).

Chapter 3

Controlled Placement of Self-Organized Ge Dots on Patterned Si (001) Substrate

3.1 Introduction

In recent decades, enormous studies have been dedicated to the realization of nanostructures based on semiconductors, such as Ge and InAs dots or islands on semiconductor surfaces [1]-[4], as a result of their prospective applications in the electronic and optoelectronic devices [5]-[7]. These nanoscale structures, so-called quantum dots (QDs), are very small quasi-zero-dimensional systems with spatially limited carriers in all three dimensions. Their sizes may range from nanometer to a few tens of nanometers, which are smaller than the de Broglie wavelength of slow electrons; thereby quantum effects are manifest in the QDs. Because of three-dimensional confinement, the energy states for electrons, holes and excitons (a pair composite of an electron and a hole interacting mutually via Coulomb force) change from continuous states into discrete quantized states like those revealed in real atoms. The electronic and optical properties of these dots are then governed by the discrete energy eigenstates of carriers. A typical quantum dot involves 10^3 to 10^6 atoms. This number of atoms is much smaller than that of constituting a bulk crystal, a quantum well, or a quantum wire, but is larger than atoms, molecules and clusters.

Lately, many different methods have been exploited to fabricate semiconductor QDs. In particular, self-organized technique is considered a promising alternative and has attracted a lot of attention in terms of the fact that self-organization provides a simple way to realize QDs without process-induced defects or damage, which is

frequently seen in the conventional method of fabricating QDs by lithographic patterning and wet or dry etching of quantum well structures. Among these self-organized semiconductor QDs, the Ge-Si system is becoming increasingly important due to its compatibility with the sophisticated Si-based ultra-large-scale integration technology [8], which continuously follows an exponential progress based on scaling down silicon transistors for the next few years.

The deposition of the Ge dots on Si is commonly described as a classic Stranski-Krastanow (SK) growth process [9]. Here, the Ge lattice parameter is about 4.2% larger than that of Si. The driving force of the dot formation in SK growth mode is a reduction of total energy by the local relaxation of lattice strain within strain-mismatched dots on a substrate material. In SK growth mode, the Ge dots are spontaneously self-organized on a 2D wetting layer as a result of the transition of the growth mode, namely, from 2D to 3D growth at a certain layer thickness, so-called critical thickness, which is typically reported to be between 4 and 5 monolayers. The advantage of exploiting this growth mode is to obtain nanometer-sized Ge dots with defect-free, high-quality properties and ease of fabrication. However, this kind of growth usually generates a random formation of the Ge dots with a non-uniform and unpredictable spatial distribution, resulting in large inhomogeneous broadening in the energy spectrum. Thus, the greatest challenge in applying these dots is to control their lateral ordering and the uniformity of their sizes on a flat Si substrate for both fundamental physics and practical applications for quantum devices.

So far, numerous reports on the self-organized QDs have been proposed to study the fundamental formation mechanism of the Ge dots [10], [11]. Their main purposes are to control the size uniformity and spatial arrangement of the self-organized Ge dots. On one hand, to improve the Ge dot density and size uniformity, carbon-induced

Ge dots [12] and boron-reconstructed surface [13] for the formation of Ge QDs have been proposed. On the other hand, to control the spatial distribution of the dots, a variety of growth methods were experimented. Kim et al. controlled the dimensions and positions of the Ge dots on the nanoscale by combining the SK growth mode with selective epitaxial growth (SEG) [14]. Jin et al. reported 1D self-alignment of the Ge islands on <110>-oriented ridges of the Si strip mesas, as well as the positioning of Ge islands at the corners of square Si mesas, using the SEG method [15]. Kitajima et al. demonstrated a 2D alignment of Ge islands on the lithographically patterned Si (001) surfaces, the smallest Si mesa was 140nm, resulting in a "one island on one mesa" relationship [16]. Zhong et al. successfully fabricated 2D periodic arrays of Ge islands on pre-patterned Si (001) substrates by combining solid-source MBE with holographic lithography [17]. However, most of the cited studies focused on the fabrication of a "single dot or island on one mesa or one pit" using SEG SiO_2 windows or patterned substrates. The feature sizes of these dots stated above are still larger than the desirable level. For effective quantum confinement, it is necessary to form smaller dots of about a few tens of nanometers. From previous theoretical simulations of heteroepitaxy on patterned substrates [18], [19], when the lateral dimensions of the substrate patterns are smaller than 100 nm, the strain energy in the epilayer can be significantly reduced, resulting in the vertical growth of Ge dots on top of the Si mesas. Still, there is no report on using Si mesa less than 100 nm for the formation of Ge dots to realize the spatial distribution of the Ge dots. On the other hand, regimented 2D arrays of self-organized Ge dots on the patterned substrates must be controlled in signal processing applications, such as quantum cellular automata [20]. Accordingly, Jin et al. presented the regimented placement of the self-organized Ge dots on Si mesas by SEG method [21]. However, the experimental results of

Kitajima et al. [16] suggest that the same results could be obtained using pre-patterned substrates without the SEG method. Recently, Capellini et al. achieved the ordered self-organized islands without a patterned substrate. Even though self-organized regimented arrays of Ge dots can be formed without a SEG window or a patterned substrate, the ordering of the distributions was limited [22].

In this chapter, we demonstrate the feasibility of the controlled ordering of self-organized Ge dots on the patterned Si (001) substrates without using the SEG method. These Si templates include both dot and anti-dot mesas, which were patterned by EB lithography incorporating with RIE technique. With the best growth condition, the sizes of the formed Ge dots are approximately estimated to be 10 nm, which was characterized by AFM and SEM. Due to the energetically favorable sites, the Ge dots tend to form homocentrically along the Si mesa edge, and their distribution could be controlled by the Si pattern arrangement. In addition, the formation of Ge dots on patterned Si mesas was further calculated by a local strain-mediated surface chemical potential [25] in a 3D model. The simulation results are quite consistent with the experimental data for Si dot and anti-dot mesas. Also, the calculated results clearly show that it may be possible using substrate morphology to improve the ordering and uniformity of the Ge dots formed on Si substrate. In the following sections, the details will be discussed.

3.2 Experimental Details

Figure 3-1 summarizes the entire process flow for the fabrication of the Ge dots on patterned Si substrates. First, a six inch p-type Si (001) blank wafer was degreased in ACE and IPA, and rinsed in de-ionized water. Typically, an additional ultrasonic

treatment is required to remove small unexpected particles which contaminated on the surface of the Si wafer. After it was blown dry with nitrogen and baked in air to get rid of water, the Si substrate was coated with a 120 nm thick PMMA as the EB resist and then baked at 180 ℃. The PMMA was then exposed at the Leica EBML300 EB direct writing system at 40 KeV and developed in MIBK: IPA (1:3) for 100 sec and rinsed in IPA for 30 sec. After the development, well-defined 100 nm PMMA trenches with 200 nm period were formed. The Si substrates with PMMA trenches were then etched using PMMA trenches as the etching mask. The Si etching process was performed in a TEL 5000 Oxide Etcher that contained a gaseous mixture of argon, methane and oxygen. After the plasma etching, the wafer was dipped in ACE to remove the residual PMMA. Before loading into the growth chamber, the wafers were chemically cleaned and dipped in a diluted HF solution (about 5 ~ 10 %) to form a hydrogen-terminated surface. Finally, the Ge dots were grown on the etched Si mesas using a ultra high vacuum chemical molecular epitaxy system at a growth temperature of 550 ℃ with a GeH_4 flow rate of 5 sccm. The growth period was 15 sec and the corresponding nominal thickness of the Ge layer was approximately 30 Å.

3.3 Ge Dots Grown on Si Dot Mesas

In this experiment, the EB dosage test run was first performed to get the exact PMMA profile for subsequent dry etching process. Figure 3-2(b) shows the well-defined 100 nm PMMA dots array with 200 nm period characterized by AFM. Usually, when the EB dosage is too large, the PMMA profile after development was all gone, leaving no patterns observed. On the contrary, as seen in Fig. 3-2(a), when the EB dosage is insufficient, the PMMA dots become connected with each other,

resulting in irregular patterns which are destructive for later dry etching procedure. By controlling the EB exposing dose and etching time, the formed Si dot mesas have dimensions of 65/23/200 nm in diameter/height/period as can be seen in Figs. 3-3(a) and (b). Compared to Fig. 3-2, the real profiles of etched Si dot mesas look like the mountain and become smaller, which is due to the lateral plasma etching.

Figure 3-4 presents several typical arrangements of self-organized Ge dots on patterned Si dot mesas. It has been predicted that for growth of Ge dots on small Si mesas with sizes of less than 100 nm, there will be some novel phenomenon occurred on the top of the mesas [18], [19]. In this work, we found that when the size of the mesa was 65 nm, the lateral growth of Ge dots seemed to be effectively suppressed and the size of the Ge dot became very small, leading to an average base width of 10 nm. Furthermore, the uniformity of these dots has also been improved and many Ge dots can be grown on the top of the small Si mesas to form the uniform distribution. From SEM image in Fig. 3-4(a), there is no "one dot on one mesa" relationship that was observed in Ref. [16]. Instead, approximate ten Ge dots were homocentrically grown along the Si mesa edges. The mesa edges are more favorable for dots nucleation than other sites. The mesa edges with reduced strain energy act as a barrier to diffusion of the adatoms [23], leading to a higher adatom density near the less strained region. In consequence, this will result in a higher probability of nucleation. Once dots nucleate in regions of the highest adatom density, subsequently arriving atoms within a diffusion length of the nuclei are more likely to join the existing nuclei, rather than forming additional nuclei [24]. This result is consistent with the previous works of Jin et al. [15] and Kitajima et al. [16]. In addition, the Ge dots initially formed at the mesa edge may change the strain distribution [15]. Furthermore, when the mesa sizes were less than 100 nm, the edge effect may take an important role on

the strain distribution of the mesa. By the above mechanism, we also found other arrangements of Ge dots on Si mesa as can be seen in Fig. 3-4(b) to (f). These dots tend to be symmetrically arranged on the top of these Si mesas. From SEM image of Fig. 3-4(f), the dot density of Ge on Si surface was estimated to be 3×10^{10} cm^{-2}.

In order to further investigate the Ge dots on Si surface, the phase-mode of AFM was used, which can differentiate areas with different properties such as viscoelasticity or mechanical properties on a sample. Figure 3-5 shows the AFM image of the distributed self-organized Ge dots on patterned Si dot mesa, which is similar to Fig. 3-4(b). From this figure, uniform Ge dots were indeed formed along the edge of the patterned Si dot mesa. Also, there is one Ge dot formed at the center of the mesa top. Its dimension is similar to those dots grown along the edge of the Si dot mesa. Further, with the best growth condition, we can obtain even dense Ge dots on Si dot mesas. Figure 3-6 presents the 3D AFM image of the uniformly distributed self-organized Ge dots on patterned Si dot arrays.

3.4 Ge Dots Grown on Si Anti-Dot Mesas

Similarly as described in section 3.3, the finished PMMA anti-dot array was first investigated. Figure 3-7 shows the AFM image of the 3D PMMA anti-dot array. With the exact EB exposing dose and development condition, the diameter and pitch of the holes are 100 nm and 200 nm, respectively.

Figure 3-8 shows the SEM images of the regimented arrays of the self-organized Ge dots on the patterned Si anti-dot mesas. Lateral plasma etching causes the diameter of the etched holes to be larger than those of the original PMMA resist patterns. As shown in Fig. 3-8(a), over-etching enlarged the etched holes, resulting in the narrowing of the spacing between the etched holes and even brought the edges of the

holes into contact with each other. The edge thus became rougher and long-range ordering was disrupted in these overlapped edge regions. However, continued over-etching caused the mesas between the holes to be discontinued and became isolated mesa islands with diameters less than 100 nm as region A shown in Figure 3-8(a), leading to the formation of the self-organized Ge dots on small isolated mesa islands. This result is consistent with the previous work for Ge dot growth on the etched Si dot mesas (see section 3.3) and this phenomenon is due to the energetically preferential nucleation [15], [16], [23], [24]. Controlling the EB dose for exposure and the etching time for the hole arrays can prevent the over exposure and over etching problems which are the main reasons for the enlargement of the dimension of the etched holes. In this experiment, anti-dot arrays with different etched depths were obtained and used for the growth of the 2D regimented arrays of the self-organized Ge dots. The depths of the holes in Figs. 3-8(b) and (c) are 23 nm and 13 nm, respectively. The size of the Ge dots formed in Fig. 3-8(b) is approximately the same as the size of the Ge dots in Fig. 3-8(c). Characterized by AFM, the average diameters of the Ge dots in both cases are approximately 10 nm. Compared these figures, the sharpness of the edge would increase the nucleation probability. The preferred positioning of the dots near the hole edges can be attributed to the reduced strain energy at the sharp edges. From Fig. 3-8(c), it can be seen that the Ge dots were formed around the edges of the holes and the dot distribution is quite uniform, the regularly spaced dots were caused by the balance between the strain energy of the dots and the repulsive interaction among the adjacent dots. Also comparing Fig. 3-8(b) and Fig. 3-8(c), it is clear that if the spacing between the holes is large and the edges are clean and smooth, more dots will form around the edges of the holes, if the hole is over etched and the edges of the holes are very close to each other and are rough due to over etch, the

number of the dots formed around the edges of the holes will be greatly reduced. Overall, the Ge nucleation sites decreased as the edges of the etched holes became rougher due to over etch.

3.5 Simulation on Si Dot Mesa

The simulation was performed by commercial multi-physics software (FEMLAB) incorporating with typical matrix manipulation tool (MATLAB) using a proposed concept of a local strain-mediated surface chemical potential [25]. The topography evolves via mass transport controlled by the chemical-potential., i.e. atoms diffuse from regions of high chemical potential to regions of lower chemical potential. The total surface chemical potential, μ, can be described by a simple continuum model [26], which assumes a linear dependence of the surface chemical potential on surface curvature [27] and a bent film treatment [28] as shown in the following equation

$$\mu = \mu_0 + \Omega\gamma\kappa(x,y,z) - \frac{\Omega C}{2}\left\{\frac{\kappa}{|\kappa|}\left[\kappa\left(z_s - z_0\right)\right]^2 - \varepsilon^2\right\} \qquad (3\text{-}1)$$

Where μ_0 is the chemical potential for the flat surface, Ω is the atomic volume, and γ is the surface free energy per unit area, κ(x,y,z) is the surface curvature, C is the elastic constant, and ε is the misfit strain between the bent film and the substrate. In this expression, the second term denotes the surface curvature contribution. In a curved surface, convex regions (positive curvature) have a higher chemical potential than concave regions (negative curvature). The Ge atoms diffuse from convex regions to concave regions. The third term determines the strain contribution to the total chemical potential. So, the total surface chemical potential is determined by the competition between the second term (surface curvature

contribution) and the third term (the strain-energy contribution). Instead of obtaining the real surface profiles taken by AFM, we numerically assumed an artificial Si dot mesa for simplicity in calculation.

Figure 3-9 shows the 3D profile of the Si dot mesa. Here, we assume that our Si dot mesa is an ideal convex surface with smooth edge. The convex surface is generated using Gauss function with diameter 100 nm and height 100 nm, respectively. Compared to the real sample, the height of the artificial Si dot mesa is much higher. Further, the effect from adjacent mesas is assumed to be very small for simplicity in calculation. Figure 3-10 displays the distribution of the total chemical potential calculated along the 3D Si dot mesa as shown in Fig. 3-9. From this figure, there are local minima occurred in the edge and the top of the Si dot mesa. This successfully explains the experimental result as shown in Figs. 3-4(b) and 3-5, where the formation of Ge dot occurred along the mesa edge and the center of the mesa top. However, in some samples, there is no Ge dot formed at the center of the mesa. This may be due to the imperfect edge of the Si dot mesa. This model proved that the edge is the energetically preferential nucleation sites for most cases. Figure 3-11 shows the 1D variation of the total local surface chemical potential along the Si dot mesa on x-axis. The blue curve and red empty circle curve are the cross-sectional surface profile of the Si dot mesa and the corresponding total chemical potential distribution along the mesa trace, respectively. In this figure, it clearly shows the positions of the local minima occurred at the edge and the center of the dot mesa.

3.6 Simulation on Si Anti-Dot Mesa

Figure 3-12 presents the 3D profile of the Si anti-dot mesa. Similarly as described in section 3.5, we assume that our Si anti-dot mesa is an ideal concave

surface with smooth edge. The concave surface is generated using Gauss function with diameter 100 nm and depth 50 nm, respectively. Compared to the real sample, the depth of the artificial Si anti-dot mesa is much deeper. Further, the effect from adjacent mesas is assumed to be very small for simplicity in calculation. Figure 3-13 displays the distribution of the total chemical potential calculated along the 3D Si anti-dot mesa as shown in Fig. 3-12. From this figure, there are local minima of the total surface chemical potential occurred at the edge of the Si anti-dot mesa. This successfully explains the experimental result as shown in Fig. 3-8, where the formation of Ge dot occurred along the mesa edge. This model proved that the edge is the energetically preferential nucleation sites for anti-dot case. Figure 3-14 shows the 1D variation of the total local surface chemical potential along the Si anti-dot mesa on x-axis. The blue curve and red empty circle curve are the cross-sectional surface profile of the Si anti-dot mesa and the corresponding total chemical potential distribution along the mesa trace, respectively. In this figure, it clearly reproduces the positions of the local minima occurred as shown in Fig. 3-8. From this model, we can calculate any surface profile of the Si mesa as expected, such as strip and square mesas as reported elsewhere.

3.7 Summary

In summary, the control of ordering of self-organized Ge QDs by the surface morphology of the patterned Si (001) substrate has been studied. We have observed the formation of the Ge dots on dot and anti-dot mesas. With the best growth condition, the sizes of the grown Ge dots are approximately 10 nm. The dot density of Ge on Si dot mesa was estimated to be 3×10^{10} cm^{-2}. The Ge dots tend to form along the Si mesa edge, and their distribution could be controlled by the pattern shape. In

some cases, in addition to the formation on the mesa edge, the Ge dots were also observed at the center of the mesa top. We also found that inhomogeneous mesa pattern may cause poor uniformity of the formation of the Ge dots. We also calculated the formation of Ge dots both on Si dot and anti-dot mesas by a local strain-mediated surface chemical potential in a 3D model. The simulation data clearly reproduce the positions of the local minima of the total surface chemical potential where the Ge dots tend to form. The overall behavior between simulation and experiment is quite consistent both on dot and anti-dot mesas. This study provides a possible picture to manipulate the self-organized nanostructures with expected places.

3.8 References

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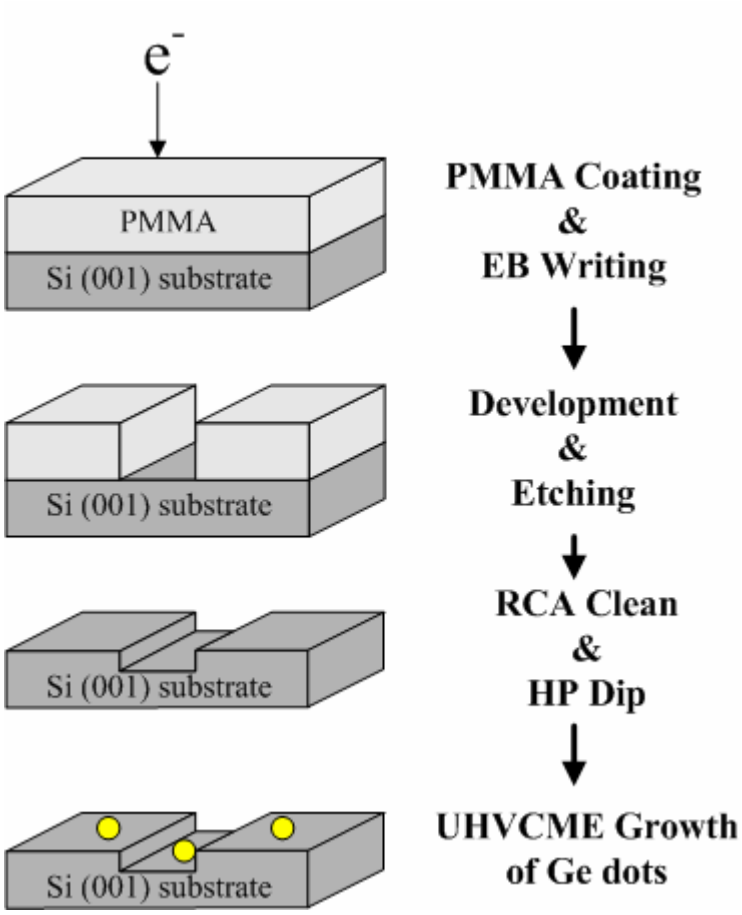


Fig. 3-1. Process flow for the fabrication of self-organized Ge dots on patterned Si (001) substrates. The Si templates include dot and anti-dot mesas.

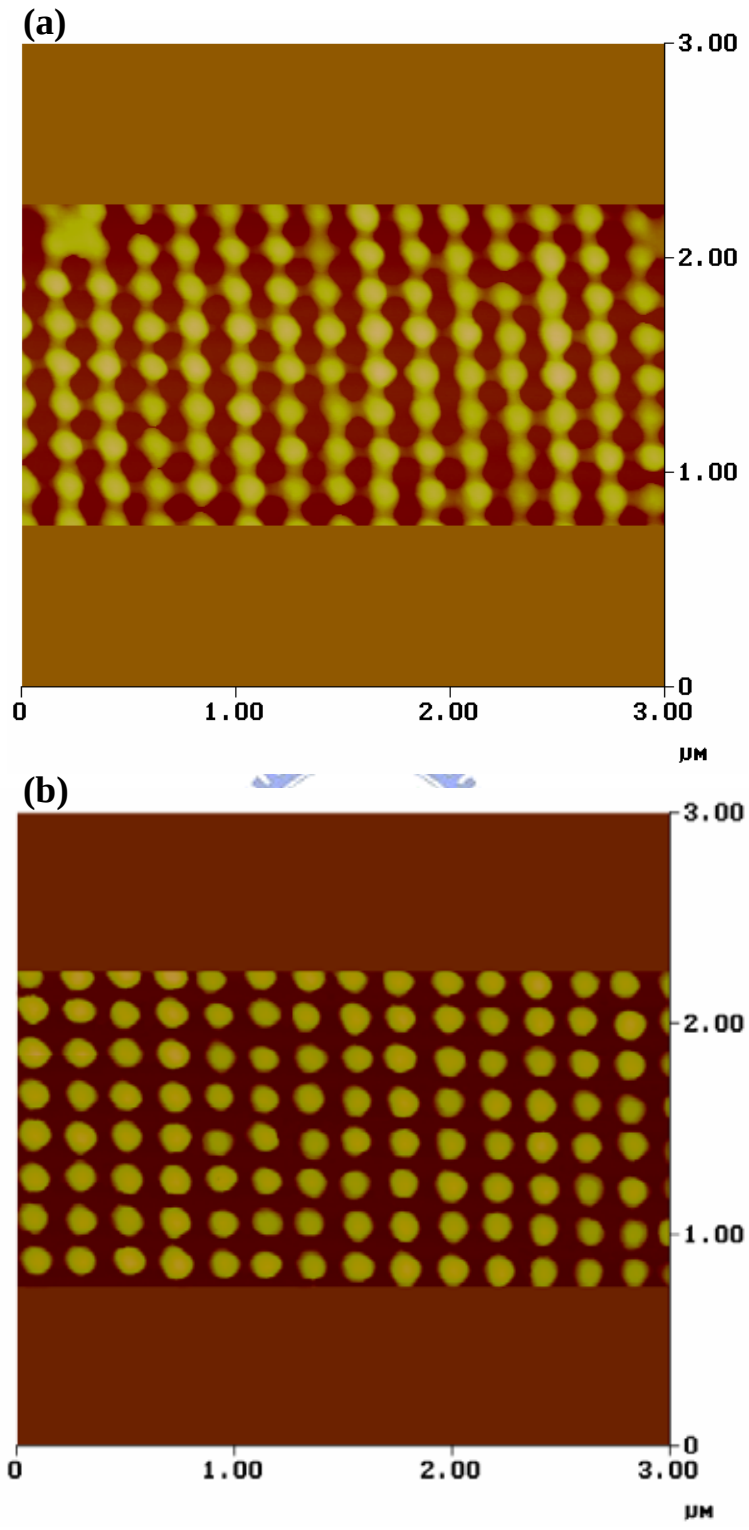


Fig. 3-2. AFM images of (a) the irregular PMMA pattern caused by insufficient EB dosage and (b) the well-defined 100 nm PMMA dots array with 200 nm period.

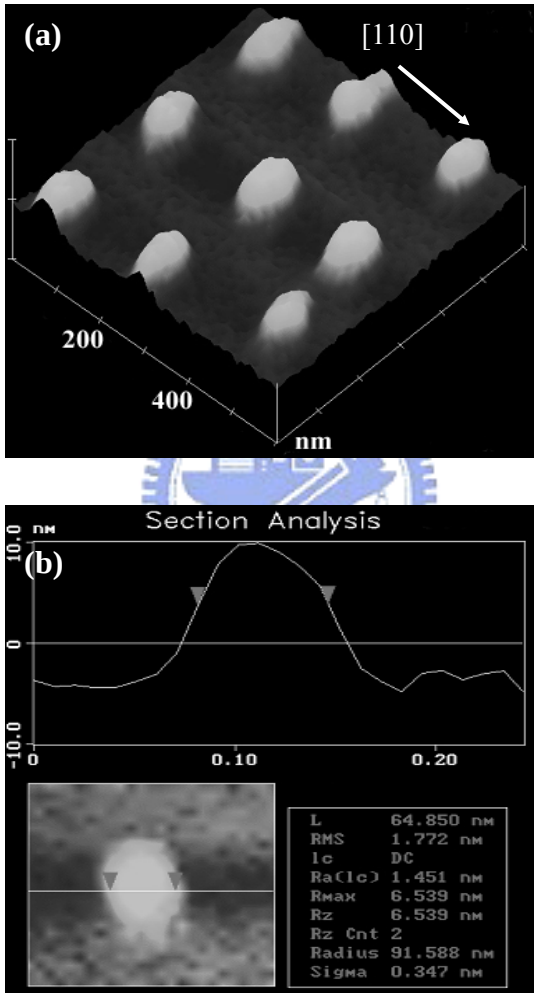


Fig. 3-3. AFM images of (a) three-dimensional 3 × 3 Si dots array and (b) cross-sectional analysis of one Si dot mesa, resulting in the size of 65 nm.

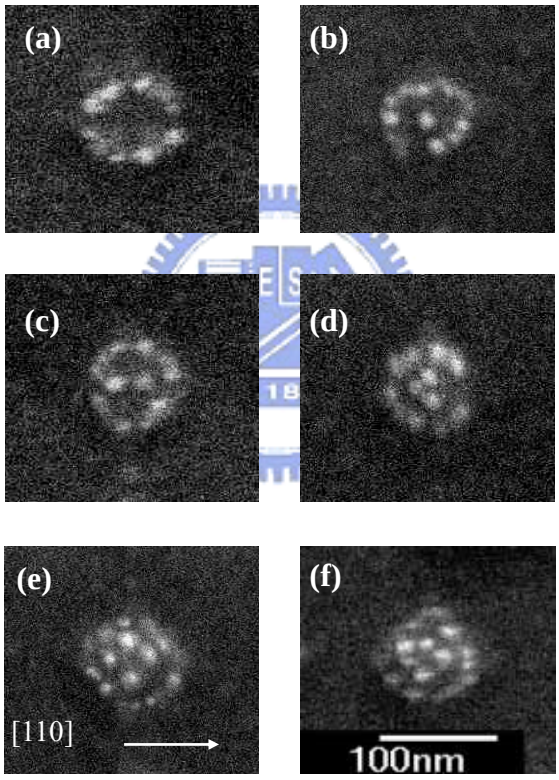


Fig. 3-4. SEM pictures of typical arrangements of the self-organized Ge dots on patterned Si dot mesas with mesa dimensions of 65/23/200 nm in diameter/height/period.

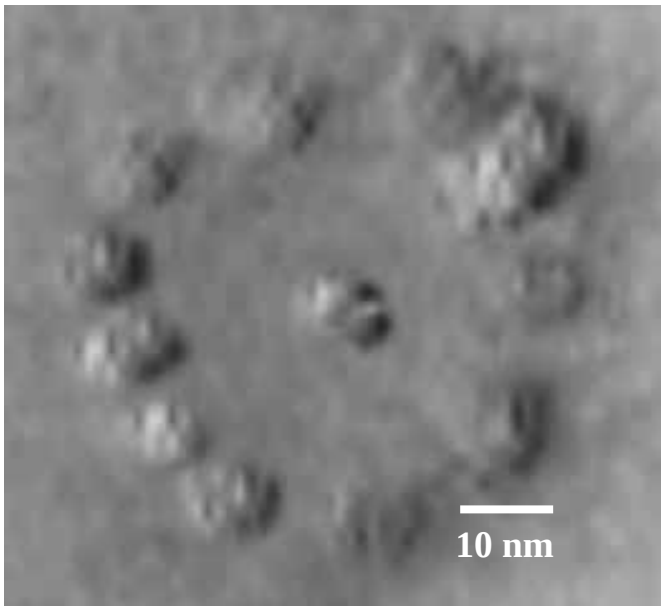


Fig. 3-5. AFM image of the distributed self-organized Ge dots on patterned Si mesas.

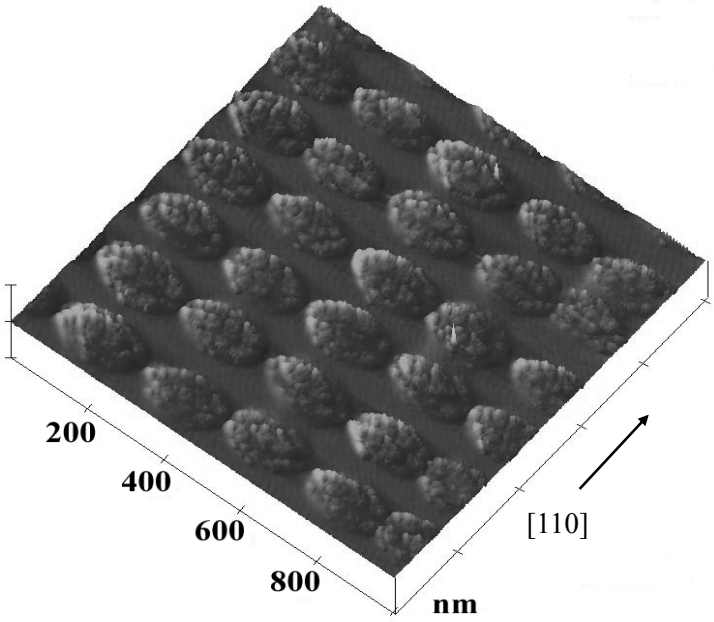


Fig. 3-6. 3D AFM image of uniformly distributed self-organized Ge dots on patterned Si dot mesas.

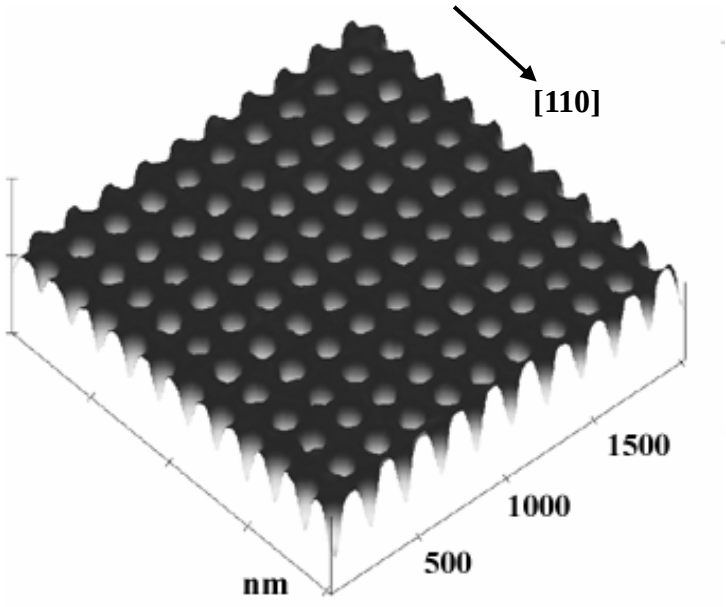


Fig. 3-7. AFM image of the 3D PMMA anti-dot array. The diameter and pitch of the holes are 100 nm and 200 nm, respectively.

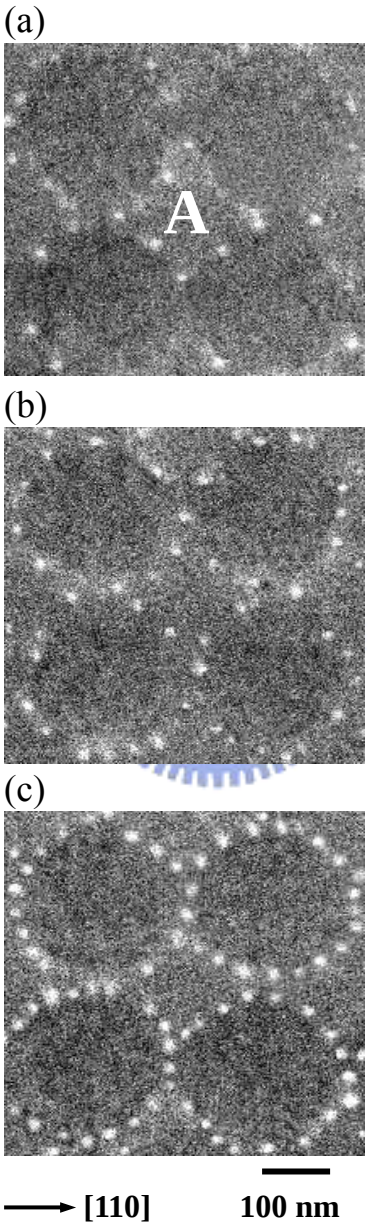


Fig. 3-8. SEM images of regimented arrays of the self-organized Ge dots on patternedSi anti-dot mesas. (a) Mesa over etched with discontinued edges. (etch depth > 50 nm) (b) Mesa over etched with rough edges. (etch depth = 23 nm) (c) Mesa properly etched with smooth edges. (etch depth = 13 nm)

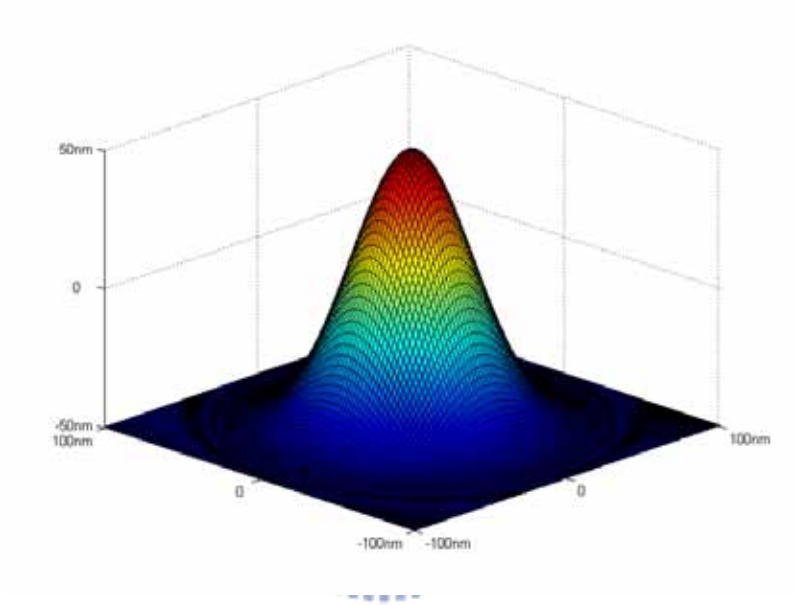


Fig. 3-9. 3D surface profile of the artificial Si dot mesa generated by Gauss function. The diameter/height is all 100 nm.

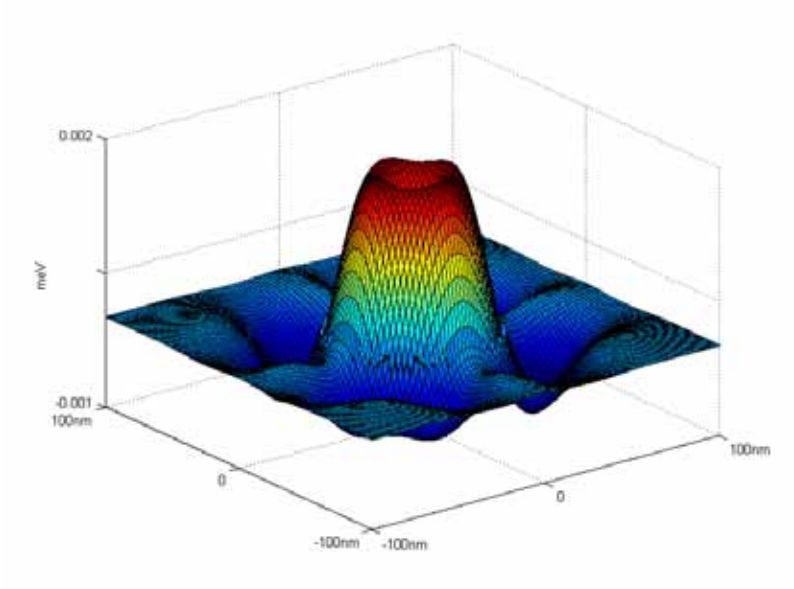


Fig. 3-10. 3D distribution of the total surface chemical potential along the artifical Si dot mesa.

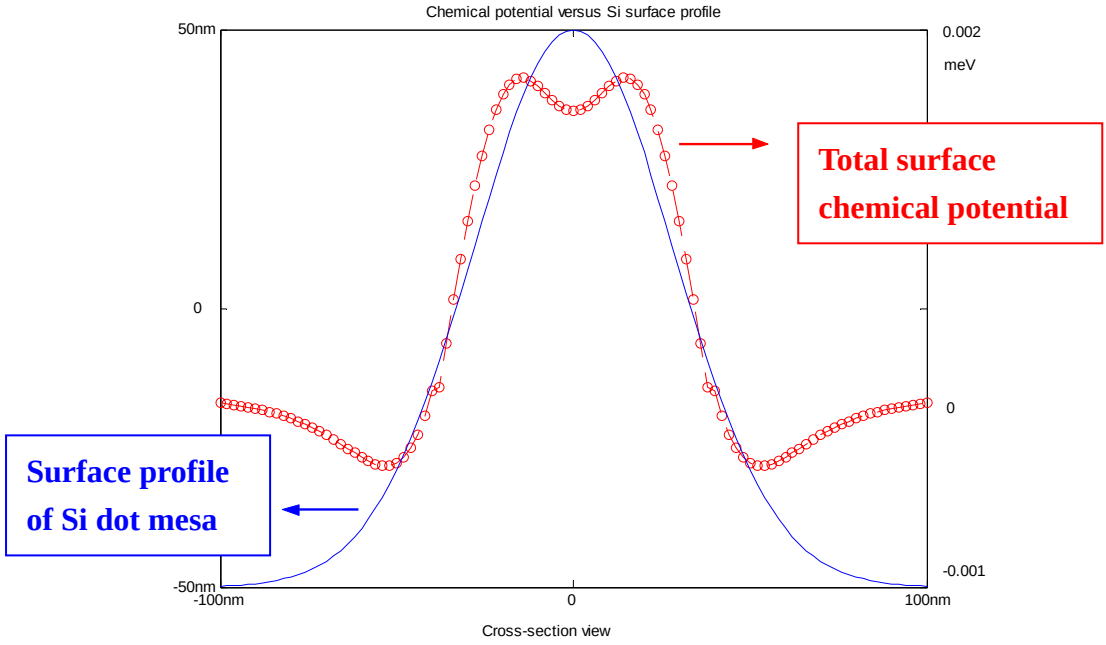


Fig. 3-11. 1D variation of the total surface chemical potential along the Si dot mesa on x-axis.

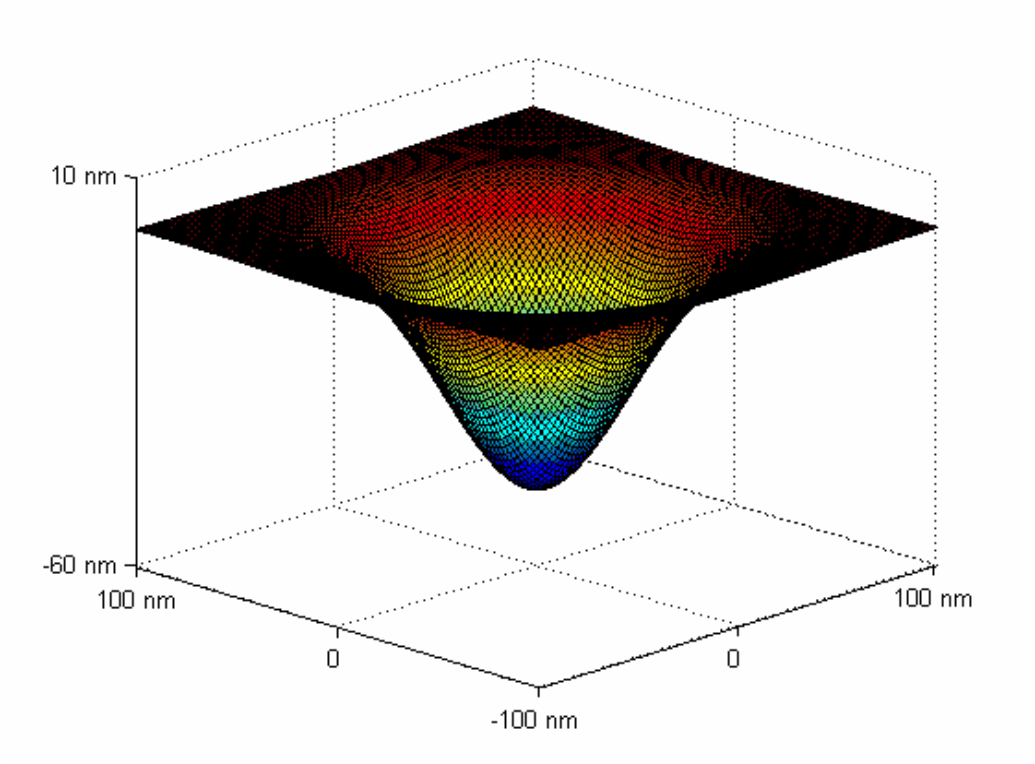


Fig. 3-12. 3D surface profile of the artificial Si anti-dot mesa generated by Gauss function. The diameter/depth is 100 nm/ 50 nm, respectively.

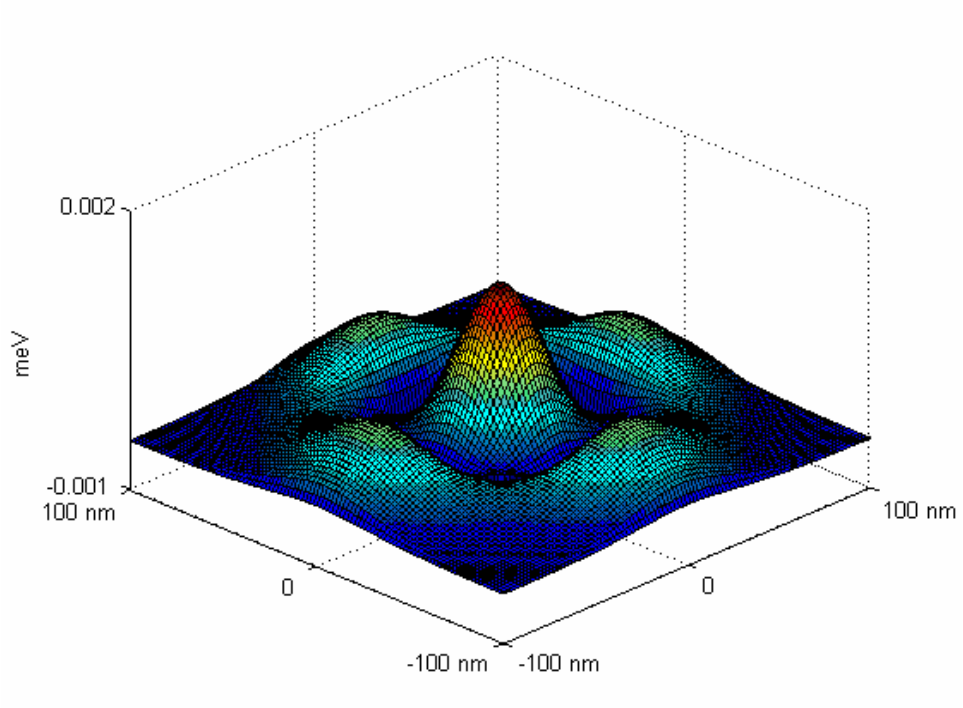


Fig. 3-13. 3D distribution of the total surface chemical potential along the artifical Si anti-dot mesa.

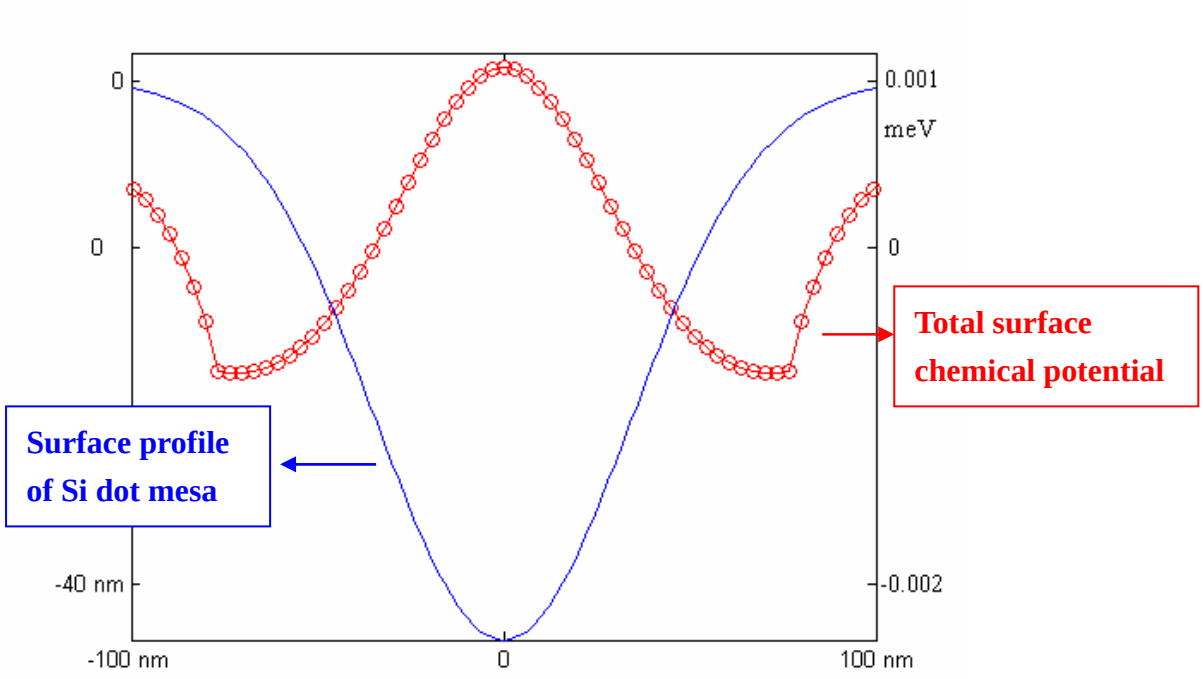


Fig. 3-14. 1D variation of the total surface chemical potential along the Si anti-dot mesa on x-axis.

Chapter 4

Electronic Transport Characteristics in One-Dimensional Constrictions Defined by a Triple-Gate Structure

4.1 Introduction

Electron transport through 1D narrow constrictions such as quantum point contacts (QPCs) [1], [2] or quantum wires [3] has been a focus of research in mesoscopic systems since the first thinking of ballistic transport in single-crystalline metal was pioneered in 1965 [4]. When the mean free path of electrons is larger than the channel length and the width of the constriction is comparable to the de Broglie wavelength of electrons, the conductance (G) through the constriction is quantized in units of $2e^2/h$ ($\equiv G_0$) [1], [2], where e is the electronic charge and h is Planck's constant with the factor of 2 arising from the spin degeneracy. Advances in nano-processing and material growth have led to successful fabrication of such structures with high integrity, thus providing opportunities to investigate novel physics emerging in a clean 1D system [3], [5]. In addition, QPCs are building blocks for other mesoscopic devices such as quantum dots or artificial atoms, and can be integrated into more sophisticated devices as a sensitive charge detector [6] or a read-out device of a qubit [7]. Therefore, the capability to precisely tune the characteristics of QPCs or quantum wires is becoming increasingly important for both fundamental physics and applications for quantum-information devices.

Typically, narrow constrictions are short 1D channels connected adiabatically to large source and drain reservoirs, which are defined in a 2DEG confined at a

modulation-doped GaAs/$Al_xGa_{1-x}As$ heterostructure by using a pair of split surface Schottky gates to deplete the 2DEG underneath and then squeeze the channel in between [1], [2]. The important structural parameters are the width and length of the split-gate opening, the density of the 2DEG, and its distance from the surface; these predetermine the ultimate characteristics of the device, such as the 1D subband energy separation (ΔE) and the number of conductance plateaus resolved [8]. Thus far, various approaches have been taken to add in-situ control over these characteristics, by incorporating an additional gate, either a back gate [9], [10] that varies the density of the whole 2DEG, or a top gate separated by the split gates by etched trenches [11] or an insulator [12], [13]. While these studies have demonstrated the in-situ control of the transport characteristics, they require additional fabrication processes [11]-[13] or special care in order to avoid shorting the ohmic contacts to the additional gate [9]-[11].

In this chapter, it is dedicated to the understanding of the transport characteristics on 1D narrow constriction. Two kinds of device structures were grown and studied including SQW and DQW GaAs/$Al_xGa_{1-x}As$ heterostructures. On one hand, we focus on SQW device and examine a simple triple-gate structure that incorporates an additional surface Schottky gate (center gate) in between the pair of split gates. Comparison between samples with and without a center gate reveals that the center gate, even when zero-biased, significantly affects the surface potential and thereby facilitates the 1D confinement in a deep 2DEG. Nonlinear transport spectroscopy with an additional dc bias [14] shows that ΔE changes linearly with the center gate voltage (V_{CG}) and can be enhanced by 70% for V_{CG} = 0.8 V. A simple model is used to calculate the lowest subband energy separation ($\Delta E_{1,2}$), which well reproduces the overall behavior of the measured $\Delta E_{1,2}$. In addition, effects of impurities [15],

occasionally found for long-channel devices, are shown to be greatly suppressed by applying a positive V_{CG} and thereby enhancing $\Delta E_{1,2}$. We also present data for the transport anomaly below the first conductance plateau, the so-called '0.7 anomaly' [3], to demonstrate that the triple-gate structure is useful for the study of density-dependent phenomena in a 1D system.

On the other hand, we put emphasis on the device equipped with DQW. The DQW heterostructures have recently attracted a lot of attention since they display a variety of interesting physical effects related to electron-electron interactions such as tunneling and Coulomb drag between DQW. Though MBE growth, barriers between the wells can be fabricated with high accuracy, thus allowing to realize devise with almost no coupling between the layers and independent parallel electron transport in both channels or devices with strong coupling depending on the barrier thickness. In our DQW device, instead of having tunneling observed, two wells behave as isolated wells due to thicker barrier (~ 22 nm). The upper electron layer is supplied via conventional modulation doping, while the lower layer is induced through the field effect from a highly-doped Si-GaAs back gate. To observe Coulomb drag behavior, vertically aligned constrictions defined by triple-gate structure in DQW with separate ohmic contacts have been successfully fabricated. The 2DEG in both layers can be operated independently through isolation gate and FIB lithographic back gate. Clear conductance plateaus for both layers were observed showing that ΔE of the upper quantum well is larger than that of the lower quantum well. The transconductance plot of the DQW sample shows that two layers can be simultaneously pinch-off when applying suitable biases to center gate and back gate and there is no tunneling observed in between. Finally, the frictional drag signal caused by narrow constriction was discovered.

4.2 Sample Design, Fabrication and Bonding

This section follows a bottom up approach, starting from the characteristics of the designed layer structures and ending with the bonding procedure. It first presents single and double quantum well structures used in order to familiarize the readers with the structures and provide them with the relevant parameters under consideration. The sample quality characterized by magnetoresistance measurement is also introduced. We then proceed to present the sample design and briefly describe the processing and bonding procedures.

4.2.1 Single Quantum Well Structure

The SQW layer structure is schematically presented in Fig. 4-1. The wafer was fabricated from a GaAs/$Al_xGa_{1-x}As$ (x = 0.3) heterostructure grown by MBE on a Si-doped n^+-GaAs (100) substrate, which functions as a back gate. The heterostructure comprises a 30-nm-wide GaAs quantum well modulation doped with Si at a 90-nm setback in the upper $Al_xGa_{1-x}As$ barrier. The quantum well is separated from a heavily Si-doped (10^{18} cm^{-3}) GaAs buffer layer by 20 nm of $Al_xGa_{1-x}As$, 1.2 μm of AlAs/GaAs short-period (2 nm/2 nm) superlattice and an undoped-50-nm-thick GaAs layer that prevents leakage to the back gate [16]. The distance d between the surface and the center of the quantum well (and hence the 2DEG) is 260 nm, considerably larger than the typical value (~ 100 nm) for defining mesoscopic structures. The distance between back gate and the quantum well is 1.27 μm. Characterized by magnetoresistance measurement, the SQW structure has a sheet electron density (n_{2D}) of 1.5 × 10^{11} cm^{-2} and a mobility (μ) of 3 × 10^6 cm^2/Vs at 1.5 K, which correspond to a mean free path of 20 μm.

Additionally, we calculated the electron density distribution of the SQW sample by using a 1D Poisson's solver [17]. This program can perform self-consist calculation by solving 1D Poisson's and Schrödinger's equation together in order to obtain the band edge diagram, the Fermi energy, the quantized states, their energies and electron wave functions and the electron density distributions. For simplification, we suppose that AlGlAs with full Al content can equally replace the GaAs/AlAs superlattice. Figure 4-2 shows the results of the simulation on the conduction band edge around the SQW region. The displayed depth in Fig. 4-2 is between 2200 and 3000 angstrom. The Fermi level represented by the red dash line is at E = 0 meV. The blue solid line shows the electron density distribution in the quantum well having a higher electron density. The n_{2D} of the 2DEG in the SQW structure is calculated to be 1.48 $\times 10^{11}$ cm^{-2} at 1.5 K, which is close to the experimental result, 1.5 $\times$ 10^{11} cm^{-2}, obtained from the magnetoresistance measurement.

4.2.2 Double Quantum Well Structure

Figure 4-3 shows schematic cross-sectional view of the DQW layer structure. First, a Si-doped (10^{18} cm^{-3}) back gate layer with thickness of 100 nm was formed on a semi-insulating GaAs (100) substrate by MBE. Then, the sample was transferred to FIB implantation chamber via ultrahigh vacuum conditions to selectively define back gate patterns using accelerating Ga^{+} ions with dosage in the order of 10^{12} ions/cm^2. The exposed areas thus became insulating [18], which is used to divide the back gate into separate conducting regions. Following implantation the wafer was transferred back into the MBE growth chamber, where the remainder barrier layers consisting of an undoped-50-nm-thick GaAs layer, a 1.22-μm-thick GaAs/AlAs (2 nm/2 nm)

superlattice and a 20-nm-thick AlGaAs layer were grown to restrain the leakage current to the back gate [16]. The DQW structure was performed including two 30-nm-thick GaAs quantum wells separated by a 22-nm-thick barrier layer of GaAs/AlAs superlattice. The Si-delta-dopes were carried out in a 130-nm-thick AlGaAs layer. The lower Si-delta-dope at a distance of 90 nm from the interface with the upper quantum well serves as an electron supplier with doping density of 10^{12} cm^{-2} while the upper one is to compensate for the surface depletion effect. The distance between the surface and the upper quantum well is 145 nm, which is close to the typical value (~ 100 nm) for defining mesoscopic devices. The distance between back gate and the lower quantum well is 1.29 μm, which is similar to the SQW wafer.

Figure 4-4 shows the results of the simulation of the conduction band edge around the DQW region by using a 1D Poisson's solver [17]. As described in section 4.2.1, it is supposed that AlGlAs with full Al content can equally replace the GaAs/AlAs superlattice. The displayed depth in Fig. 4-4 is between 1200 and 2400 angstrom. The Fermi level represented by the red dash line is at E = 0 meV. The blue solid line shows the electron density distribution in the upper quantum well having a higher electron density. The n_{2D} in the upper quantum well is calculated to be 1.46 $\times 10^{11}$ cm^{-2} at 1.5 K, which is close to the experimental result of 1.5 $\times 10^{11}$ cm^{-2} obtained form magnetoresistance measurement.

In the following section, we will elaborate on the magnetoresistance measurement introducing how to obtain the electron density and mobility experimentally. Furthermore, the wafer quality of the DQW structure will be examined using back gate.

4.2.3 Magnetoresistance Measurement

The magnetoresistance measurement is usually referred to the measurement of the conductivity between source and drain electrodes dependent on external magnetic field. As illustrated in Fig. 4-5, the electric circuit is set up to measure the four-terminal source-drain resistance as a function of perpendicular magnetic field (B). In order to reduce the background noise coming along with measured data, the lock-in amplifier technique (please refer to appendix A) is commonly employed. The source-drain current kept constant is given by $I_{SD} = V_{AC}/R_L = 1\ \text{V}/10\ \text{M}\Omega = 100\ \text{nA}$. Accordingly, the source-drain resistance is $R_{SD} = V_S/I_{SD}$, where V_S is the real voltage drop between source and drain derived by $V_{out}/10\times V_{sen}$, in which V_{out} and V_{sen} are the voltage output and sensitivity of the lock-in amplifier. Besides, the virtual equipment of LabVIEW is used to acquire and analyze data automatically.

The device structure shown in the left part of Fig. 4-5 is called Hall bar, which is typically fabricated and used to determine the n_{2D} of the 2DEG and the corresponding μ of an epitaxial wafer by measuring the longitudinal and transverse resistances (Hall resistance) as a function of perpendicular B. On one hand, in the lower magnetic field region (smaller than 1 Tesla), the n_{2D} can be extracted using a Fast Fourier Transform (FFT) of the longitudinal resistance as a function of the inverse of magnetic field by $1/B$. The periodicity of the oscillations known as Shubnikov-de Haas (SdH) oscillations is then related to the n_{2D} by $\Delta(1/B) = (1/B_n - 1/B_{n+1}) = g_s g_v e/hn_{2D}$, where B_n is the magnetic field at which the nth oscillation minimum occurs, g_s and g_v are the appropriate spin and valley degeneracy. Because of no valley degeneracy in GaAs system, the above formula becomes $\Delta(1/B) = (1/B_n - 1/B_{n+1}) = 2e/hn_{2D}$ in which the spin degeneracy is 2. On the other hand, from the Hall resistance,

one can get n_{2D} as well by the relation of $R_{XY} = B/en_{2D}$. Furthermore, the μ can be figured out from the related formula of n_{2D} and μ at zero magnetic field by $\mu = 1/n_{2D}e\rho$, where ρ is the resistivity that is related to the resistance R by RL_H/W_H, in which the length (L_H) over width (W_H) is 16/5 in our Hall bar geometry. With above analytic technique, the n_{2D} and μ of the grown structures can be easily extracted.

As described in section 4.2.2, the DQW structure is equipped with two quantum wells that the modulation doping is performed only on the upper side of the DQW, so that only the upper quantum well is conductive without applying back gate biases (V_{BG}). While applying a positive voltage to the underlying back gate, the electrons get started to accumulate in the lower quantum well. Figure 4-6 shows the SdH oscillations of this DQW sample as function of B at temperature of 1.5 K. When V_{BG} is around 2.3 V, the SdH oscillations exhibit only one frequency, which is believed that the electron densities of the upper and lower quantum wells are almost equal. Besides, when those with V_{BG} are close to 2.3 V, the extra structures in the SdH oscillations are generated due to the unlike electron densities in two layers. To further prove the assumption, the electron carrier density in each layers as a function of V_{BG} were determined experimentally by taking the FFT in $1/B$ of the SdH oscillations observed in magnetoresistance measurements as can be seen is Fig. 4-7. For $V_{BG} \leqq$ 0 V, only the upper quantum well is populated as expected from the upper side doping. When V_{BG} is increased above 0 V, the electron density (n_2) of the lower layer starts to be field-induced along with V_{BG}. Once n_2 forms, the lower 2DEG screens the electric field from the back gate, so that the electron density (n_1) of the upper layer becomes almost constant. As a result, n_1 is almost equal with n_2 when applying V_{BG} is between 2.2 and 2.4 V, showing that n_2 can be fully controlled independent on n_1. For FFT, one can use professional plotting software (IGOR and Origin) or refer to MatLab code

developed to analyze the data in appendix B.

In addition to deriving the electron densities of the two quantum wells by FFT, the dependence between the electron density (n_H) deduced from Hall resistance with the total electron density ($n_T = n_1 + n_2$) is compared as shown in Fig. 4-8. The n_T of the two quantum wells was observed to depend almost linearly on V_{BG}, while n_1 remains relatively unchanged as long as n_2 starts to be field-induced. Furthermore, n_H agrees very well with n_T. The good agreement is supposed that the mobility for both layers is sufficiently high so that the Hall coefficient can be further reduced to a simple relation by $R_H = 1/(n_1 + n_2)e$. Furthermore, by assuming that the scattering occurred in each layer is independent, the zero-field conductivity can be expressed by $\sigma = n_1 e \mu_1 + n_2 e \mu_2 = n_H e \mu_H$, where μ_1, μ_2 and μ_H are the mobilities of upper quantum well, lower quantum well and the field-dependent Hall effect, respectively. Using above deduction, μ_2 can be derived by $\mu_2 = (n_H e \mu_H - n_1 e \mu_1)/n_2$, where μ_1 is nearly constant for $V_{BG} > 0$. Figure 4-9 shows the measured μ_H and estimated μ_2 of the lower layer as a function of V_{BG}. The μ_H reaches 300 m^2/Vs for $n_T = 1.5\times10^{11}$ cm^{-2}, indicating that the upper quantum well is with high epitaxial quality. Detailed discussions please refer to cited reference [16]. Through these low temperature transport analyses, it is clear that the DQW structure with equally high mobilities are formed in the lower quantum well as well as the upper one, and the independent densities can be manipulated by back gate.

Not only the low field magnetoresistance measurements are demonstrated but also the high field SdH oscillations are carried out. Figure 4-10 shows the longitudinal resistance (R_{XX}) and transverse resistance (R_{XY}) as a function of perpendicular B up to 7 Tesla, where the V_{BG} is kept at 2.3 V to make sure that both quantum wells have the same electron densities. As can be seen in this figure, the filling factor 1 occurs when

R_{XY} = 12.9 KΩ because of the equivalent electron densities on both layers. Also, the irregular oscillation due to the spin splitting was discovered at Landau-level filling factor $\nu = 3$ at around 2 Tesla.

4.2.4 Device Fabrication

Single and double quantum well devices were both fabricated using the same photo mask pattern as indicated in Fig. 4-11. For SQW samples, the FIB implantation process was omitted. However, for DQW samples as described in section 4.2.2, the wafers after first growth were Ga^+ ions implanted to define the back gate into separate conducting regions, i.e. the inner back gate and the outer back gate regions. This mask pattern was designed specifically for the fabrication of the DQW sample. However, it is also compatible for SQW wafer. Detailed processing steps are described in the following.

Firstly, the etchant, H_2SO_4 : H_2O_2 : H_2O = 5 : 1 : 25, was prepared and kept at constant 10 ℃, which provides the typical etching rate of around 10 nm/sec for GaAs/AlGaAs heterostructure. To avoid leakage from back gate, an ideal etching depth is typically 50 nm deeper than the channel depth. Therefore, the etching depth for SQW and DQW devices is expected to be 325 nm and 277 nm respectively. Following standard clean treatment with ACE and IPA the wafers were processed into a square-shaped mesa (120 μm × 120 μm) with eight arms on the corners, to which ohmic contacts were formed by alloying AuGeNi (80:10:10 *wt*.) at 390 °C for 1 min in H_2 [16]. As shown in Fig. 4-11, there are four small ohmic patterns designed to contact the 2DEG in the lower layer. In this operation mode, the isolation gate voltage (V_{IG}) negatively biased is applied to totally deplete the upper 2DEG. Meanwhile, a

positive V_{BG} through a pre-etched square hole is applied to the inner back gate. The induced electrons in the lower layer only exist inside the rectangular boundary, which was previously made insulating by implantation process. Besides, there are four big ohmic contacts which are used to contact the upper 2DEG. Both quantum wells, therefore, can be manipulated independently in this design.

On the top of square-shaped mesa, the triple-gate pattern was defined by EB lithography and lift-off of evaporated 20-nm-thick Ti/Au (detailed descriptions for EB lithography and lift-off processes, please see section 2.1). The EB dosage test run has been first carried out in order to make sure that the fine patterns can be successfully formed. Figure 4-12 shows the SEM pictures of the triple-gate structure with six different EB dosages after lift-off process. As shown in this figure, the incomplete structure (f) is due to insufficient EB dosage making rounded resist profile, resulting in difficult lift-off. In contrast, structure (a) shows the sharp and clean edges due to an ideal undercut resist profile. Another enlarged SEM image shown in Fig. 4-13 defines the parameters of the triple-gate structure. The length (L) and width (W) of the split gates were varied as L = 0.2-2 μm and W = 0.4-0.8 μm, respectively, while the width of the center gate was always fixed at 0.2 μm [19], [20]. We also fabricated control samples without a center gate for comparison (not shown here).

4.2.5 Wire Bonding

After lithography process and metallization, the wafers were cut to square pieces (1.5 mm × 1.5 mm) ready for wire bonding, which is an electrical interconnect technology used to attach a fine wire from one connection pad to another, completing the electrical connection in an electronic device [21]. The materials of these thin wires could be Gold, Aluminum or Copper depending on the bonding process. The bonding

process is a solid phase weld, where the two metallic materials (wire and pad surface) are brought into intimate contact with transfer of a combination of pressure and ultrasonic energy via the resonating bond tool (capillary or wedge) to the interface between the bond wire and the bond pad. Once the surfaces are in intimate contact, electron sharing or interdiffusion of atoms takes place, resulting in the formation of wirebond. In such process, bonding force can lead to material deformation, breaking up contamination layer and smoothing out surface asperity, which can be enhanced by the application of ultrasonic energy. Heat can accelerate interatomic diffusion, thus the bond formation.

There are basically two forms of wire bonding. They are wedge bonds and ball bonds as shown in Fig. 4-14. The bond tools (upper part of the schematic drawing in figure 4-14) and the way the wire is held are quite different. The orientation of the wedge tool (b) defines the bond direction. The bond head of a wedge bonder must therefore be oriented in a straight line from the 1st pad to the 2nd pad, before the 1st bond can be made. This requires a suitable rotating of bond holder than for ball bonder (a), where the wire can be bent and drawn from the first bond in any direction. The heavier mechanics and the more complex bond head movement slow down the wire bonding process. In ball bonding the first bond is made by means of a ball that is formed before by means of an electrical spark, while the second bond resembles a wedge bond.

In this experiment, the thermosonic wedge bonder (West Bond) is used to perform the wire bonding process. With holder temperature of around 120℃ and suitable ultrasonic power, the bonds can be easily formed using a thin Gold wire. Figure 4-15 shows the sample carrier and the device with gold wires soldered to the carrier's leads. Just before doing bonding, the device was mounted on the metal base

of the sample carrier using conductive Silver glue and oven baked at temperature of 110℃ for 30 minutes to make sure device adhered well to metal base. As demonstrated in Fig. 4-15, the four terminal resistances can be obtained with source-drain voltage applying through lead 3 and 5 and observed current from lead 14 and 12. The lead 15 serves as a back gate in this case.

4.3 Measurement Set-ups

Transport measurements were performed with the sample cooled in pumped liquid helium (^{4}He or ^{3}He) cryostats in the dark without illumination. Two different set-ups, four-terminal current and voltage bias measurements, are commonly used to measure the conductance through a device depending on its average resistance. For four-terminal current bias measurement, a constant ac current is sourced from a lock-in amplifier with a large serial resistor while ,for four-terminal voltage measurement, a standard lock-in technique is used with an ac modulation voltage at a suitable frequency. For most measurements, it is essential to keep the current and voltage across the device relatively small. In particular, the voltage drop across the device, V_D, should not exceed the temperature of electrons or higher energy states in the device may become accessible; that is $eV_D < kT$, where k is Boltzman's constant. For high resistance devices, it is easy to apply a constant bias voltage to meet the above condition and measure the current through the sample. For low resistance devices, a more reliable measurement comes from passing a constant current through the device and measuring the voltage drop. All of these experiment set-ups mentioned will be discussed in the following sections.

4.3.1 Low Temperature Set-up

It is know that most of the important physical phenomena only become apparent when the temperature of the environment surrounded is getting even lower, which means to further weaken the effect coming from the thermal fluctuation included in this system. The easiest way for this purpose is to contact your system directly to a cold environment prepared. Regardless of the highly cost, liquid ^{4}He with its boiling temperature of just 4.2 K is an ideal substance in studying low temperature Physics. However, it cannot be so easy just to build a container into which we can put our sample and then pour liquid ^{4}He on top. In such way, all liquid ^{4}He will boil when put into contact with anything that is warmer than 4.2 K. Not only direct contact, but also even heat transfer through radiation will blow all your ^{4}He. Considering this issue, a thermal insulating container called cryostat was created. Figure 4-16 shows the 1.5 K ^{4}He cryostat system equipped with superconductive magnet. You can see two distinct walls. The outer wall (blue solid line) is a thick stainless steel container, with pump and pressure gauge ports. The inner walls (black solid line) are aluminum shield foil with several layers of aluminized mylar. They also serve as the containers for liquid ^{4}He. The volume between the outer and the inner walls has to be pumped out to low pressure (around 10^{-7} torr) to reduce conductive heat exchange. The layers of aluminized mylar help to cut off the thermal radiation flux and to intercept hot molecules that would otherwise hit the ^{4}He container. When liquid ^{4}He is filled inside, it surely boils off firstly. The cold ^{4}He vapor will cool down the inner containers and be recovered through recovery line before escaping into the atmosphere. Continuing filling, the liquid phrase of ^{4}He finally stay inside the container. Now we can put the sample into the cryostat through the loading probe, which is connected to the measurement equipment and superconductive magnet controller. By small amount

of liquid ^{4}He flow, which is usually set to 15% in our case, and continually pumping, the base temperature of sample space can reach around 1.4-1.5 K in this system. This is enough to observe ballistic 1D conductance plateaus of the constrictions in our device.

But what if you need even lower temperature? The difference between 4.2 K and 1 K for a scientist is not just 3.2 K, but also a ratio of 4.2. In this sense it is somewhat like the difference between room temperature (300 K) and the melting point of copper (1356 K). It is known that the boiling temperature of a liquid ^{4}He is a function of its vapor pressure. It means that just by pumping on a liquid ^{4}He it is possible to cool down the system to the extent to which you can reduce the pressure. This allows cooling down ^{4}He to around 1 K without any further complex processes. However, the only problem is that while cooling the liquid ^{4}He itself, you have to evaporate a sizable portion of it. By the time only 1.2 K is achieved, almost half of the liquid ^{4}He is gone. In this case, a more complicated cryostat is thus designed. The outer wall looks just the same as previously described system, but the inner contents are quite different. A sorption pump controlling the ^{3}He and a 1 K pot serving as ^{3}He condenser are added to the new system. Figure 4-17 shows the schematic cross-sectional drawing of the 0.3 K ^{3}He cryostat system. It also comprises superconductive magnet immerging in liquid ^{4}He. The diaphragm and rotary pumps are connected to the sorption pump and the 1 K pot, respectively, which are being fed by liquid ^{4}He through thin long capillaries by adjusting the corresponding needle valves. When cooled, gases generally adsorb to solid surfaces forming a monolayer or two. Sorption pump is based on the idea that at around 10 K almost all of the ^{3}He gets adsorbed, whereas at about 35 K practically all of the molecules desorbed. Sorption pump is a cylinder that contains materials like activated charcoal, which have enormous total

surface area. After the cryostat has been cooled to 1.1 K, the sorption pump is heated up and ^{3}He is introduced into the system. When passing through the cold 1 K pot (the condenser), ^{3}He becomes liquid and drips down into the sample space as shown in the figure. After the condensation is complete, we close the heater. The sorption pump is cooled down through a weak thermal link to the liquid ^{4}He container. Then, when sorption pump gets cooling, it starts to adsorb the vapor of ^{3}H, resulting in reducing the vapor pressure and lowering the temperature of the sample space further. After all of the ^{3}He evaporates, the sorption pump has to be heated up to condense ^{3}He and so on. With this condensation cycle, the lowest temperature of this system can be stably kept around 0.24 for long-term measurement.

4.3.2 Four-Terminal Current Bias Measurement

Four-terminal current bias measurement is often used when the sample resistance is in the order of 25 kΩ or less, or equivalently, the conductance is larger than e^2/h. This measurement set-up requires two lock-in amplifiers with the same phase locked at 13 or 77 Hz, which is used to avoid noise signal coming from measurement equipment and power supply. Typically, a constant ac current is generated from one lock-in amplifer using an rms voltage (0.1 V – 5 V) through a serial resistor (100 MΩ – 1 GΩ). As seen in the schematic circuit diagram of Fig. 4-18, the first lock-in amplifier sources an ac voltage, V_{rms} = 0.1 V, which is converted into a constant ac current, I_{rms} = 1 nA, via a 100 MΩ resistor. In the figure, two ohmics are used for the current path and the other two are used to measure the voltage drop across the device which is accomplished with the second lock-in amplifier. Because no current flows through the voltage probe leads, the measured voltage drop is only due to the resistance of the device itself. One caution which must be taken in the current bias

set-up is to ensure that the voltage across the device dose not become too large if the sample resistance grows significantly. Excessive voltage loads can be prevented by placing a voltage divider on the first lock-in output, before the serial resistor. The gate voltages are all computer controlled by virtual equipment of LabVIEW automatically. The range of the applied center gate bias was - 0.45 ≤ V_{CG} ≤ 0.9 V, for which the leakage current was negligibly small. Unless otherwise specified, the V_{BG} was kept to zero and the split-gate voltage, V_{SG}, was applied to both split-gates simultaneously.

4.3.3 Four-Terminal Voltage Bias Measurement

Four-terminal voltage bias measurement is usually used when the average sample resistance is greater than 25 kΩ, or equivalently, the conductance is smaller than e^2/h. Such a circuit is as shown in Fig. 4-19 and consists primarily of a small ac voltage applied between the ohmics in the source and drain electron reservoirs and an additional set of voltage probes to determine the voltage drop across the device itself using a second lock-in amplifier, phase locked to the first one. This gives an accurate measurement of the device resistance. For the determination of ΔE, a finite dc bias ($|V_{DC}| \leq 3$ mV) was added to the ac modulation voltage [14]. Note that some fraction of the applied dc voltage drops at the ohmic contacts, which then varies with the current and hence with the V_{SG}. To extract the voltage across the constriction, we separately measured the dc voltage between the voltage probes, which we denote as V_{SD}. The ac + dc adder box combines and divides the two voltage components; the box has a 100,000 : 1 divider for the ac voltage and a 1000 :1 divider for the dc voltage at 77 Hz. Therefore, an ac modulation voltage of 20 μV (V_{rms} = 2 V) and a dc voltage of 1 mV (V_{DC} = 1 V) are produced in this circuit.

For DQW sample, the measurement circuit can be seen in Fig. 4-20. Compared to Fig. 4-19, two additional lock-in amplifiers (phase locked) and an additional ac + dc adder box are added to measure the quantized G in the lower quantum well through four small ohmic contacts, in which four depletion gates, V_{IG}, are negatively biased to stop current flow in the upper quantum well. The n_{2D} in the lower well is controlled by V_{BG}, which is positively biased, and the induced electrons only exist inside the implantation region, meaning that there is no current flow observed outside the rectangular boundary. The n_{2D} in the upper well can be finely tuned by V_{CG}.

4.4 Experimental Results and Discussions

Following sections we will present the electronic transport characteristics on the narrow constrictions defined by triple-gate structure both on SQW and DQW samples. For SQW device, the effects of center gate on the surface potential, control of 1D confinement with center gate, and effects of 1D confinement and electron density on transport anomalies (impurity effects and the 0.7 anomaly) will be discussed. For DQW device, we will demonstrat the basic operation in two layers using separate ohimc contacts techniques [18]. Accordingly, Coulomb drag behavior occurred on the constriction was observed. All discussed results will be concluded with a summary.

4.4.1 Experimental Results on SQW devices

4.4.1.1 Effects of Center Gate on the Surface Potential

We start by comparing samples with and without a center gate. Figure 4-21 shows the measured G at 1.5 K of the devices with (thick line) and without (thin line) a center gate as a function of V_{SG}. The split gates of the two devices have the same

dimensions, W = 0.6 μm and L = 0.2 μm. For the sample with the center gate, V_{CG} was set to zero. The data reveal that, even when V_{CG} = 0 V, the center gate significantly affects the characteristics of the device. The pinch-off voltage (V_P) is found to be much deeper (i.e., more negative) in the sample with the center gate. Furthermore, with the center gate the conductance plateaus are seen to be better defined. We have confirmed similar behavior in other devices with different W and L. Note that the rather poor conductance quantization in the samples without a center gate is partly due to the large depth of the 2DEG in our heterostructure [22]. The much improved quantization in the samples with a center gate, in turn, suggests that the center gate helps defining constrictions in a deep 2DEG.

We investigated the pinch-off characteristics of many devices with various W and L. The results are summarized in Fig. 4-22, where V_P of each device is plotted as a function of L. The solid (open) symbols represent devices with (without) a center gate. For the samples with a center gate, V_{CG} is kept at zero. It is seen that, for a given W, V_P becomes shallower (i.e., less negative) with increasing L, and then tends to saturate for larger L. In addition, the plot reveals that the devices without a center gate have consistently shallower V_P compared to those with one. This clearly shows that, even when V_{CG} = 0 V, the center gate significantly affects the electric potential at the constriction.

In the figure, we plot the pinch-off voltages calculated from the analytical formula for the standard rectangular split-gate geometry [23]. The model assumes a pinned surface for the exposed semiconductor surface. Although the pinned-surface model may not be appropriate for GaAs at cryogenic temperatures [24], it greatly simplifies the mathematical treatment, allowing for the analytical expression of V_P. Accordingly, the required V_P to remove electrons from the narrow constriction with W

= 2*a*, *L* = 2*b* can be expressed by the following equation [23]

$$V_P = V_t \left[\frac{2}{\pi} \arctan \frac{b}{d} - \frac{2}{\pi} \arctan \frac{ab}{d\sqrt{a^2 + b^2 + d^2}} \right]^{-1} \quad (4\text{-}1)$$

The parameters used in the calculation are d = 0.26 μm and V_t = -0.45 V, the latter being the split-gate gate voltage at which the 2DEG underneath the gate is depleted. As the figure shows, the calculation reproduces the behavior of the devices with a center gate very well. On the other hand, the agreement is poorer for those without a center gate, which exhibit V_P much shallower than the calculation. This is consistent with the analysis in Ref. 23, where it was shown that the frozen-surface model results in a shallower pinch-off voltage than the pinned-surface model. In our triple-gate structure, the potential at the surface just above the 1D channel is kept at zero by the center gate, making the pinned-surface model more appropriate. On the other hand, for the standard split-gate geometry, the frozen-surface model is more appropriate. Hence, the difference between the devices with and without a center gate can be interpreted as due to the difference between the pinned surface and the frozen surface [25].

As shown in Ref. 23, the pinned surface results in a stronger 1D confinement than the frozen surface. This is consistent with our results that the conductance plateaus are better developed in devices with a center gate. The more negative V_{SG} required squeezing the 1D channel in those devices results in a correspondingly stronger confinement, thereby facilitating the conductance quantization even in a deep 2DEG as used here. In the following, we focus on samples with a center gate and describe how the transport characteristics can be modified by V_{CG}.

4.4.1.2 Control of 1D Confinement with Center Gate

Figure 4-23 presents results for a device with $W = 0.6$ μm and $L = 0.4$ μm, where the measured G at 1.5 K is plotted as a function of V_{SG} for different V_{CG} ranging from –0.45 to 0.9 V. The thick line corresponds to $V_{CG} = 0$ V. For this sample, having a larger L of 0.4 μm, the pinch-off voltage at $V_{CG} = 0$ V is shallower, and correspondingly, only a small number of conductance plateaus are visible for $V_{CG} = 0$ V. However, as V_{CG} is made progressively positive, V_P shifts linearly with V_{CG} to more negative values, and accordingly, an increasing number of plateaus become resolved. For the highest V_{CG} of 0.9 V, as many as 14 conductance steps are clearly observed. On the other hand, when V_{CG} is made negative, the features become obscured until no structure except the '0.7 anomaly' [5] is discernible at $V_{CG} = –0.4$ V.

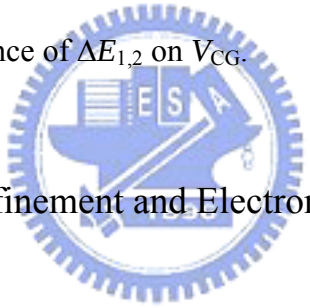
In order to clarify the effects of the center gate on the confinement, we determined the 1D subband energy separation by adding a finite dc voltage ($|V_{DC}| \leq 3$ mV) to the small ac modulation voltage [14]. Figure 4-24 displays the gray-scale plots of the transconductance (dG/dV_{SG}) at 0.24 K for different values of V_{CG}. The data are plotted against V_{SG} (horizontal axis) and V_{SD} (vertical axis), the latter being the dc voltage across the constriction measured separately. The transconductance was calculated by numerically differentiating the measured G with respect to V_{SG}. The bright features represent peaks in dG/dV_{SG}, which occur when the bottom of a 1D subband matches the electrochemical potential of either the source or drain reservoir [26]. The energy separations between adjacent subbands can be determined by the value of V_{SD} at which two lines forming an apex meet at the top. The data clearly show that ΔE for the same subbands increases with V_{CG}.

Figure 4-25 plots the measured $\Delta E_{i,i+1}$ as a function of V_{SG} for different V_{CG}.

Here, $\Delta E_{i,i+1}$ denotes the energy separation between the ith and (i+1)th subbands. It is seen that $\Delta E_{1,2}$ has a linear relationship with V_{SG}. It is also seen that the position of each conductance step (in V_{SG}) moves in proportion to V_{CG}, which in turn implies a linear relationship between $\Delta E_{1,2}$ and V_{CG}, similar to previous reports using different gate structures [13]. The values of $\Delta E_{1,2}$ for V_{CG} = 0 and 0.8 V are 2.1 and 3.6 meV, respectively, corresponding to an enhancement of 70%. If we extrapolate the linear relationship between $\Delta E_{1,2}$ and V_{CG}, the values of $\Delta E_{1,2}$ for the data in Fig. 4-23 are estimated to be 1.4 and 3.8 meV for V_{CG} = -0.4 and 0.9 V, respectively, corresponding to a change by a factor of 2.7.

We simulated $\Delta E_{1,2}$ using a simple model assuming an infinitely long 1D channel and no self-consistent potential from the electrons in the 1D channel [27]. The approximation of no self-consistent is reasonable for the present case of calculating $\Delta E_{1,2}$, where only one subband is occupied and so the electron density is low, as verified by the relatively good agreement with experiment described below. The electric potential in the 2D plane perpendicular to the 1D channel was obtained by solving the Poisson equation using a finite element method. Then, using the extracted 1D potential transverse to the channel, the Schrödinger equation was solved to obtain the 1D subband energies. The calculated $\Delta E_{1,2}$ is plotted in Fig. 4-25 for comparison with experiment. The simulation shows $\Delta E_{1,2}$ consistently larger than the experiment, which is a result of the infinitely long channel assumed. However, it well reproduces the linear dependence of $\Delta E_{1,2}$ on V_{SG} and hence on V_{CG}. The enhanced $\Delta E_{1,2}$ for positive V_{CG} is partly due to the more negative V_{SG} required to squeeze the channel. We therefore examined $\Delta E_{1,2}$ for different V_{CG} while keeping V_{SG} constant by using a back gate.

Figure 4-26 depicts the measured G of the same device as in Fig. 4-23, where the combinations of V_{CG} and V_{BG} are chosen to keep V_P constant, varying in equal steps from $V_{CG} = V_{BG} = 0$ V to $V_{CG} = 0.6$ V and $V_{BG} = -1.5$ V. The data demonstrate that, even though V_P is kept constant, the conductance plateaus become better resolved with increasing V_{CG}. The 2DEG density estimated from a separate Hall measurement (please refer to section 4.2.3) is $n_{2D} = 1.5 \times 10^{11}$ cm^{-2} for $V_{BG} = 0$ V, which decreases to $n_{2D} = 0.7 \times 10^{11}$ cm^{-2} for $V_{BG} = -1.5$ V. The values of $\Delta E_{1,2}$ measured for these conditions are 2.1 and 2.9 meV, respectively. Even though the n_{2D} in the reservoir is significantly decreased by negative V_{BG}, the confinement in the constriction is improved by positive V_{CG}, resulting in $\Delta E_{1,2}$ enhanced by 40%. Figure 4-27 compares the measured and calculated $\Delta E_{1,2}$ as a function of V_{CG}. The calculation again well reproduces the linear dependence of $\Delta E_{1,2}$ on V_{CG}.



4.4.1.3 Effects of 1D Confinement and Electron Density on Transport Anomalies

A. Impurity Effects

We next used the center gate to study effects of the 1D confinement and electron density on various transport anomalies. Figure 4-28 shows the measured G at 1.4 K of a long-channel device with $W = 0.6$ μm and $L = 1$ μm for different V_{CG} ranging from 0 to 0.8 V. Compared to the $L = 0.4$ μm device shown in Fig. 4-23, the longer L of this device results in shallower V_P. For $V_{CG} = 0$ V, the conductance plateaus are not well developed, and their positions are somewhat below the integral multiples of $2e^2/h$. Also note that the plateau positions are not equally spaced, indicating that each subband has a different contribution to the measured G. We have investigated many

devices and found such behavior only in those with $L \gtrsim 1$ μm. By applying asymmetric biases to the split gates [15], we have confirmed that this is due to an impurity near the 1D channel that happens to be charged in this particular case. Indeed, details of the conductance traces for these samples vary from cool-down to cool-down, and occasionally, the plateaus can be well aligned at integer multiples of $2e2/h$, with no trace of impurity effects (please refer to inset of Fig. 4-28).

When positive V_{CG} is applied, the positions of the plateaus start to line up at integral multiples of $2e^2/h$. The measured $\Delta E_{1,2}$ for V_{CG} = 0, 0.4, and 0.8 V, are 2.3, 3.0, and 4.1 meV, respectively [28]. The enhanced subband separation is also accompanied by an increase in the 1D electron density. The observed suppression of the impurity effects may therefore be ascribed to the enhanced confinement and the increased screening due to the increased 1D electron density, both of which would reduce impurity scattering and thereby facilitate the ballistic transport.

B. The 0.7 Anomaly

It is widely known that the conductance of a 1D ballistic channel exhibits an additional plateau-like feature, the so-called 'the 0.7 anomaly,' around $G = 0.7$ ($2e^2/h$) below the first plateau [5]. While experiments have suggested that the 0.7 anomaly is associated with the spin degree of freedom [5], its exact origin remains an issue of active research [10], [29]-[34]. In our samples, the 0.7 anomaly is observed ubiquitously, as clearly seen in Figs. 4-21, 4-23, 4-26 and 4-33. Since the 0.7 anomaly is known to exhibit complicated dependence on temperature [5], [29], [30], [33], electron density [10], [32], [34], and channel length [32], [34], we here used the center gate to investigate the density dependence of the anomaly.

Figure 4-29 displays the measured G around the first plateau of the L = 1 μm device

with V_{CG} varied from 0 to 0.8 V. We here applied a positive back-gate bias of V_{BG} = 1 V to further increase $\Delta E_{1,2}$ and enhance the ballistic transport. At T = 1.4 K, the position of the additional feature evolved from $0.65G_0$ to $0.55G_0$ with increasing V_{CG} and hence increasing electron density. When the temperature was reduced to 0.24 K, the anomalous structure became slightly weaker and its positions were higher, evolving from $0.7G_0$ to $0.6G_0$. As also seen in Fig. 4-23, such density dependence was not observed for devices with $L \leq 0.5$ μm. The observed dependence of the anomalous feature on the electron density and the channel length is consistent with a previous report [32] on ultra-low-disorder quantum wires in which electrons were field-induced through a top gate. These results demonstrate that the triple-gate structure provides an alternative and simpler way of investigating density dependent phenomena in a clean 1D system.

4.4.2 Experimental Results on DQW devices

4.4.2.1 Basic operation on DWQ sample

Figure 4-30 presents depletion characteristics of the DQW sample as a function of V_{IG} with V_{BG} varied from 0 to 4 V in steps of 0.5 V at 4.2 K. For this measurement, a constant 10 mV was applied onto a small ohmic contact and the corresponding current was measured through another small ohimc contact; that is to investigate the electric transport inside the implantation region. Due to only modulation doping in the upper quantum well (front layer), when V_{BG} = 0, there is no electrons existing in the lower well (back layer). When V_{BG} is increased greater than 1 V, as shown in the figure, the electrons of the back layer start to be field-induced. The lower layer thus becomes conducting, resulting in the increase of the total current measured. The front

layer is fully pinch-off when V_{IG} is smaller than - 0.35 V. When V_{IG} is continuously made more negative till - 0.9 V, the back layer is also depleted, leading to no current flow observed. In this sample, two layers have equal n_{2D} when V_{BG} is around 2.3 V, which is quite consistent with the magnetoresistance measurement in section 4.2.3.

In Fig. 4-31, we use the same measurement approach as described in Fig. 4-30 except that the corresponding current was measured through another big ohimc contact, which is outside the implantation region. When V_{IG} is greater than -0.35 V, only the current flow in the front layer is observed. Ideally, the current in front layer should not be affected by varied V_{BG}. However, it grows up slightly as the V_{BG} is applied. This may be due to the change of the ohimc properties in the small contact biased by large positive back gate voltage. When V_{IG} is smaller than -0.35 V, the current suddenly drops to zero, meaning that the front layer is already cut off by large negative biases.

Following the same measurement circuit described in Fig. 4-31 is used to check the interlayer isolation as displayed in Fig. 4-32. Instead of using a constant 10 mV, a varied voltage source, $V_{S\text{-}B}$, is applied to the small ohmic contact. Here, the V_{BG} is fixed at 3 V to produce electrons in the lower layer while V_{IG} is varied from -0.3 to -0.4 V. In this independent contact configuration, the interlayer bias of 20 mV could be applied with leakage current smaller than 1 nA (please refer to insert of Fig. 4-32), showing that tunneling between the layers was negligible.

4.4.2.2 Conductance measurement with separate contacts

The electric circuit, introduced in Fig. 4-20, is employed to measure G on each layer of the DQW device. The lower 2DEG is contacted through four small ohmic patterns by applying V_{IG} = - 0.35 V, which is previously proved to fully deplete upper

2DEG but leave the lower one unaffected. Meanwhile, a positive back gate bias (V_{BG} = 3 V) is applied to the inner back gate, hence making the lower layer conducting inside the rectangular boundary. Four big ohmic contacts outside the implantation region are used to contact the upper 2DEG. Figure 4-33 shows results for the device with W = 0.6 μm and L = 0.2 μm, where the measured G at 1.4 K is plotted as a function of V_{SG} for different V_{CG} ranging from - 0.2 to 0.4 V. The blue curve presents the measured G of the front layer while the red one shows the G for the back layer. When V_{CG} is - 0.2 V, front layer is pinch-off earlier than the back layer. On the contrary, the back layer is pinch-off earlier than front layer when V_{CG} is 0.4 V. Two layers can be simultaneously pinch-off at V_{CG} around 0.1 V, where V_{BG} is always kept at 3 V. For this sample, the distance between the surface and the upper quantum well is 145 nm, close to the typical value (~ 100 nm) for defining mesoscopic devices. Compared to the SQW device (the distance between the surface and the quantum well is 245 nm), the conductance plateaus of the DQW sample are much better defined. Further, comparing the G plots of the two layers, we found that the ΔE of the front layer is larger than that of the back layer.

Figure 4-34 displays the gray-scale plot of the transconductance (dG/dV_{SG}) at 1.4 K for different values of V_{CG}. The data taken from Fig. 4-33 are plotted against V_{SG} (horizontal axis) and V_{CG} (vertical axis). The transconductance was calculated by numerically differentiating the measured G with respect to V_{SG}. The bright features represent peaks in dG/dV_{SG}, which occur at transition slope between two plateaus. The vertical black line at V_{SG} = -2 V in all plots is an equipment related artifact. As shown in the figure, we can see three regions, i.e. the front layer, back layer and bilayer regions. Because the barrier between two wells is thick (~ 22 nm), there is no tunneling effect observed from this plot. Clear crossing of the sublevels can be

observed at the balance point of equal densities in the bilayer region.

4.4.2.3 Coulomb Drag measurement

In section 4.4.2.2, we have proved that there is no tunneling in our bilayer sample. Therefore, the interlayer correlation called Coulomb drag could be an interesting topic. Coulomb drag measurement basically consists of a current in one layer inducing a voltage in the other layer due in part to the loss of momentum caused by interlayer electron-electron interactions. In this measurement, we slightly modified the circuit diagram in Fig. 4-20 by one layer with four-terminal current bias, creating a constant current passing through one quantum well (the drive well). The drift of the electrons creates a frictional drag force that acts on the electrons in the adjacent quantum well (drag well). If no current is allowed to flow in the drag well, a voltage is developed due to the buildup of charges swept along in the direction of the drive current [35]. The drag voltage is the opposite of the resistive voltage drop in the drive well and balances the drag due to the interlayer interactions. This effect is due to momentum-transfer processes between the layers. Figure 4-35 shows the gray-scale plots of transconductance dG/dV_{SG} measured at T = 1.4 K as a function of V_{SG} for V_{CG} = 0 to 0.4 V. The dimension of sample is the same as in Fig. 4-23 (L = 0.4 μm and W = 0.6 μm). Bright features in the upper plot of Fig. 4-35 indicate peaks in dG/dV_{SG}. The upper plot shows the transconductance of one quantum well while the lower one exhibits the corresponding drag signal on the adjacent well. The negative resistance occurs at the cross point of the bilayer region as indicated in Fig. 4-34, where the sublevels on both layers are observed with equal electron density. Furthermore, the drag signal dramatically decreased on high-index sublevels due to the decrease of the confinement on the constrictions.

4.5 Summary

In summary, we have fabricated 1D narrow constrictions defined by a triple-gate structure incorporating an additional surface Schottky gate (center gate) in between the pair of split gates, and studied their transport characteristics both on SQW and DQW devices at low temperature. We performed magnetoresistance measurement to check the wafer quality of the grown wafers.

For SQW sample, comparison between devices with and without a center gate revealed that the center gate, even when zero-biased, affects the surface potential and significantly enhances the 1D confinement. Because of the fixed surface potential above the 1D channel, the pinch-off voltage of these devices can be well predicted by an analytical formula based on the pinned-surface model. Nonlinear transport spectroscopy showed that the energy separation between the lowest 1D subbands varies in proportion to the center-gate bias V_{CG} and can be enhanced by 70% for V_{CG} = 0.8 V. The enhanced 1D confinement for positive V_{CG} greatly enhanced 1D ballistic transport, as manifested by the better-developed conductance plateaus and the suppression of impurity scattering in long-channel devices. For a 1-μm-long-channel device, the anomalous plateau-like feature below the first conductance plateau (the '0.7 anomaly') was observed to evolve toward 0.5(2e2/h) with increasing V_{CG} and hence increasing electron density.

For DQW sample, we demonstrated the basic operations and measured the individual conductance on both layers with separate ohimc contact techniques. Two layers have equal n_{2D} when V_{BG} is around 2.3 V. Front layer can be pinch-off when V_{IG} is around – 0.35 V. Interlayer bias is measured around 20 mV with negligible leakage current smaller than 1 nA. Further, Coulomb drag measurement is carried out

showing that the negative resistance tends to occur at the cross point in bilayer region, where the sublevels on both layers are observed with equal electron density. The drag signal dramatically decreased on high-index sublevels due to the decrease of the confinement on the constrictions.

These results clearly demonstrate that the triple-gate structure provides a simple way of controlling the characteristics of 1D constrictions and investigating density-dependent phenomena in a 1D system. In addition, its predictable pinch-off characteristics and enhanced 1D confinement are major advantages over the conventional split-gate structure, the latter being of particular importance when defining constrictions in deep 2DEGs. The structure, which does not require any additional fabrication steps or interfere with other parts of the device, will be particularly suited for lateral integration.

4.6 References

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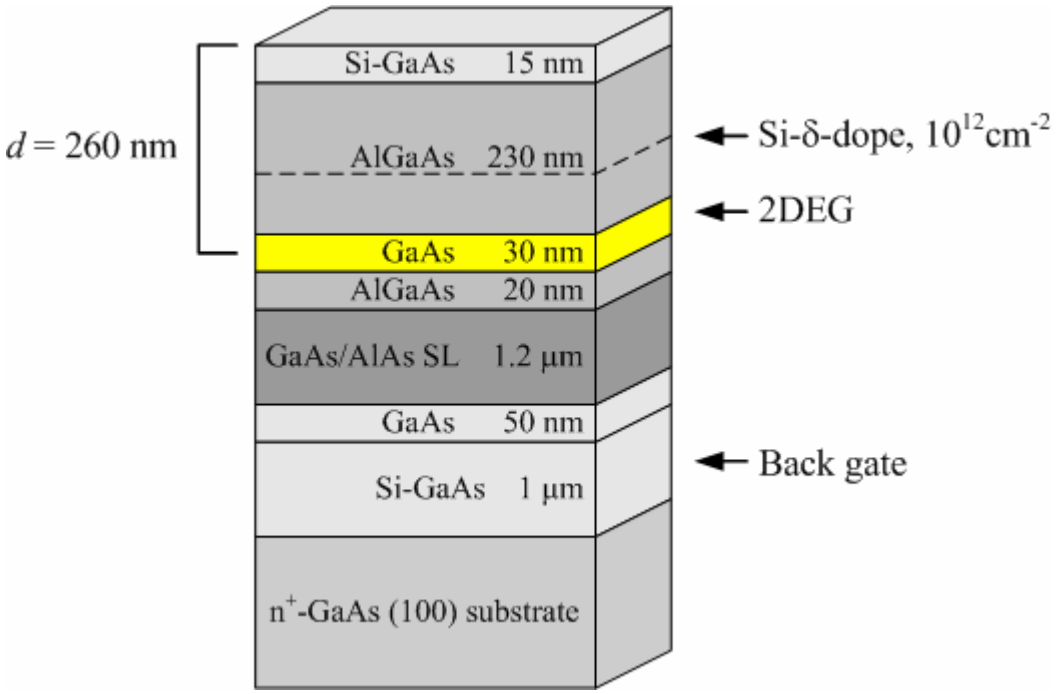

Fig. 4-1. Schematic cross-sectional view of the single quantum well structure.

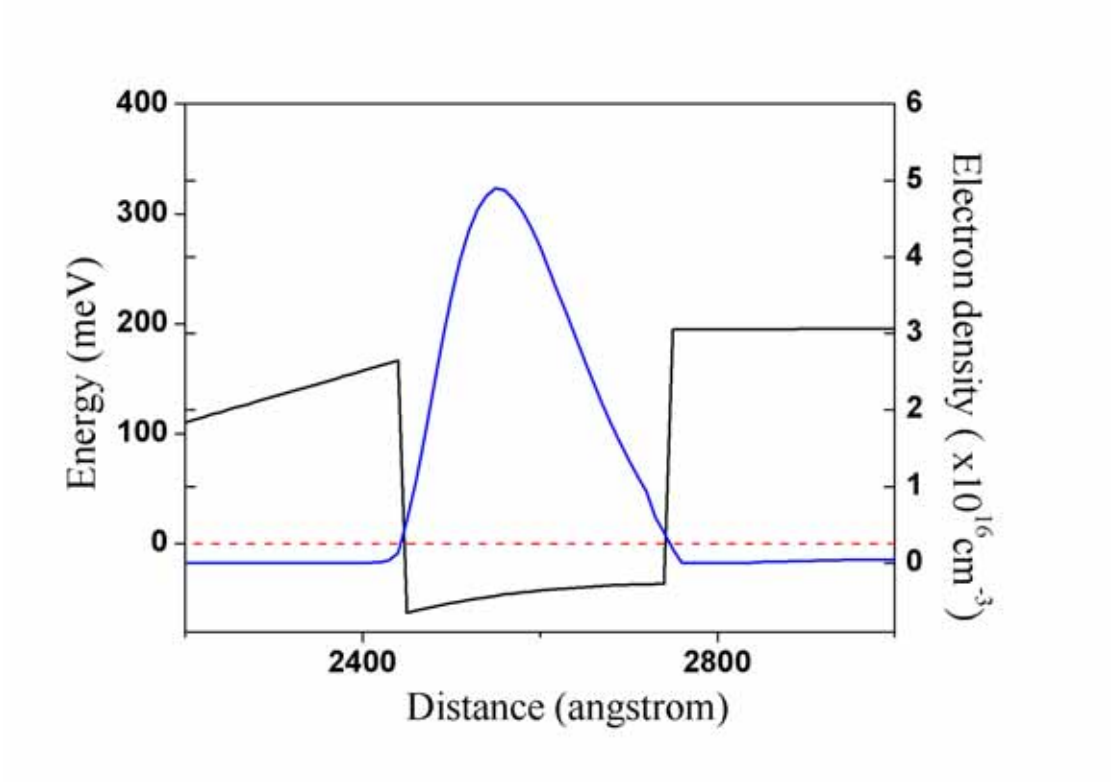

Fig. 4-2. Conduction band edge diagram around the single quantum well (SQW). The depth displayed is between 2200 and 3000 angstrom. The red dash line at E = 0 meV represents the Fermi level. The blue solid line denotes electron density distribution. The sheet electron density (n_{2D}) of the SQW is calculated to be 1.48×10^{11} cm^{-2} at 1.5K.

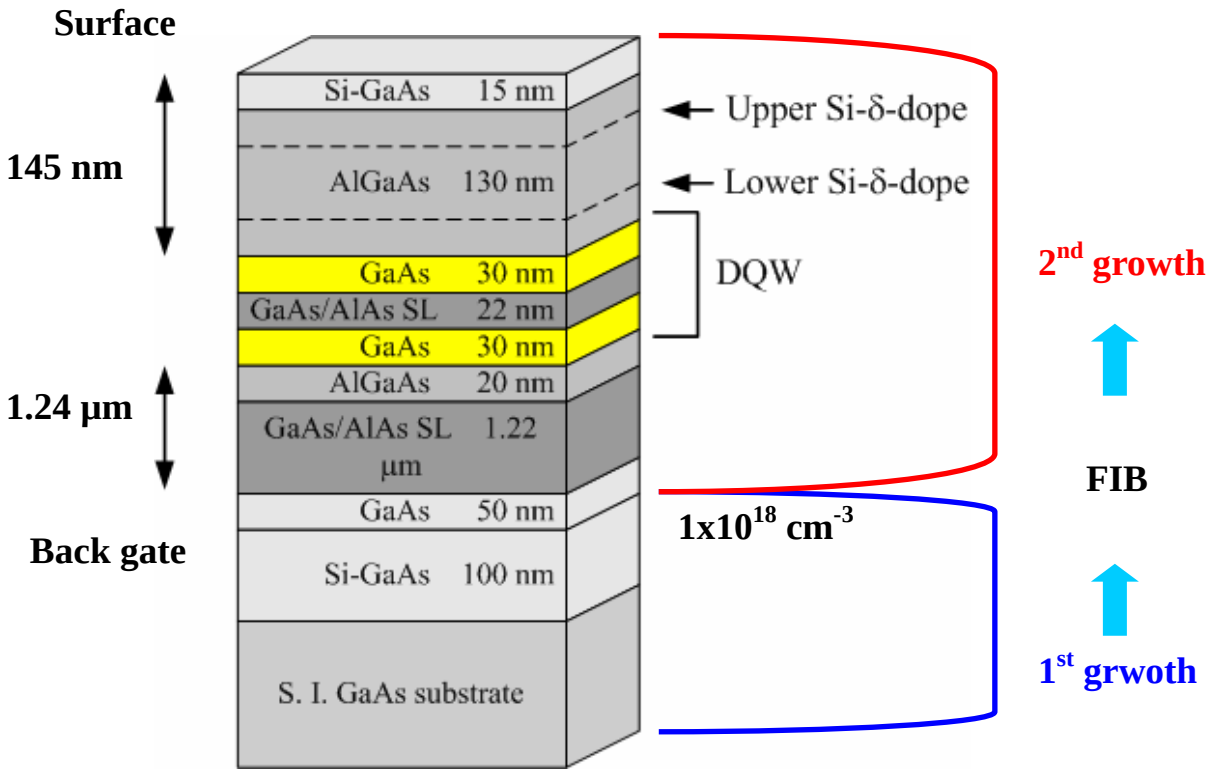

Fig. 4-3. Schematic cross-sectional view of the double quantum well (DQW) structure. Between 1st growth and 2nd growth, in-situ focus ion beam lithography was employed to selectively define back gate region. All growth processes are under vacuum using multi-chamber MBE.

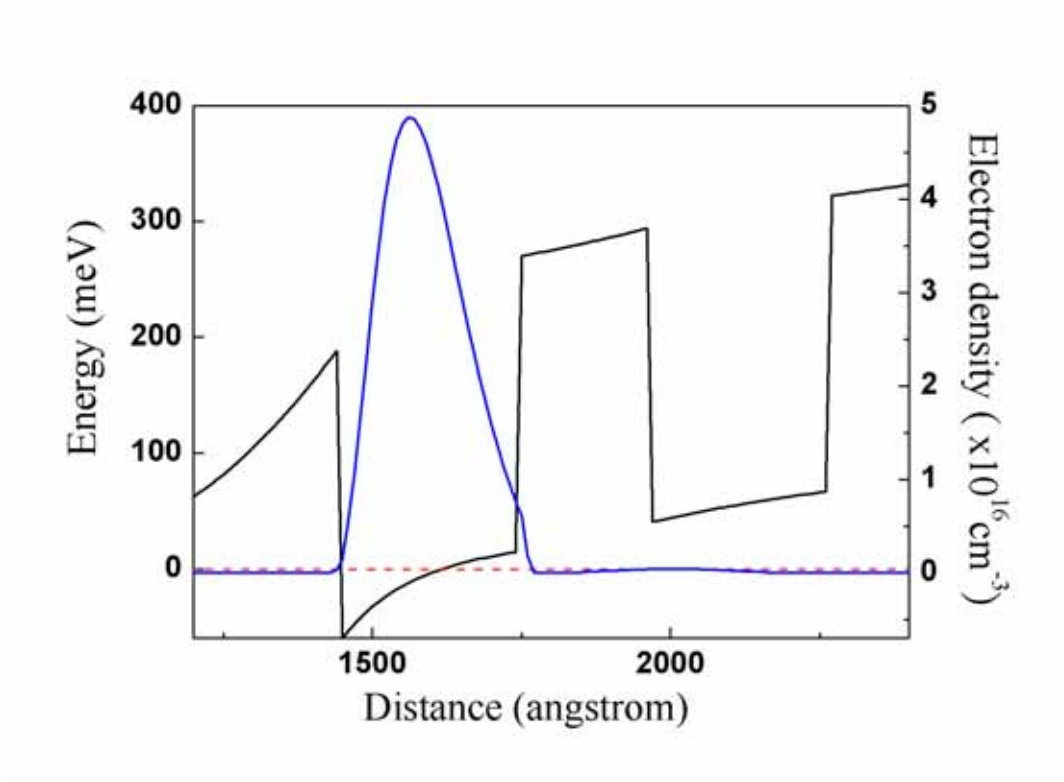

Fig. 4-4. Conduction band edge diagram around the DQW structure. The depth displayed is between 1200 and 2400 angstrom. The red dash line at E = 0 meV represents the Fermi level. The blue solid line denotes electron density distribution. The n_{2D} of the upper layer is calculated to be 1.46 $\times 10^{11}$ cm^{-2} at 1.5 K.

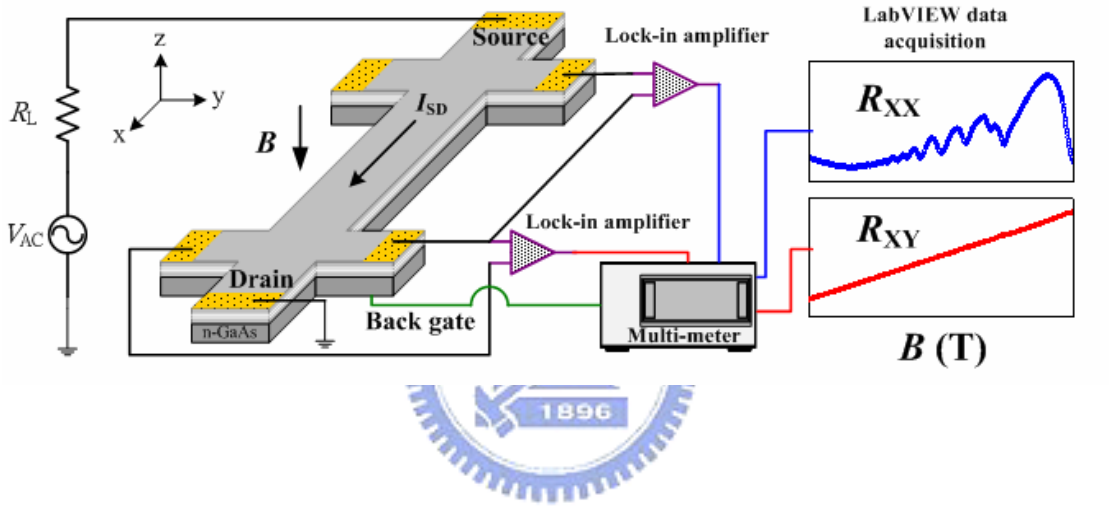

Fig. 4-5. Electric circuit set-up in the measurement of the source-drain resistance as a function of perpendicular magnetic field (B). The longitudinal resistance (R_{xx}) and transverse resistance (R_{xy}) as a function of perpendicular B can be acquired through two lock-in amplifiers by HP 4142b multi-meter, which also serves as a voltage source to back gate.

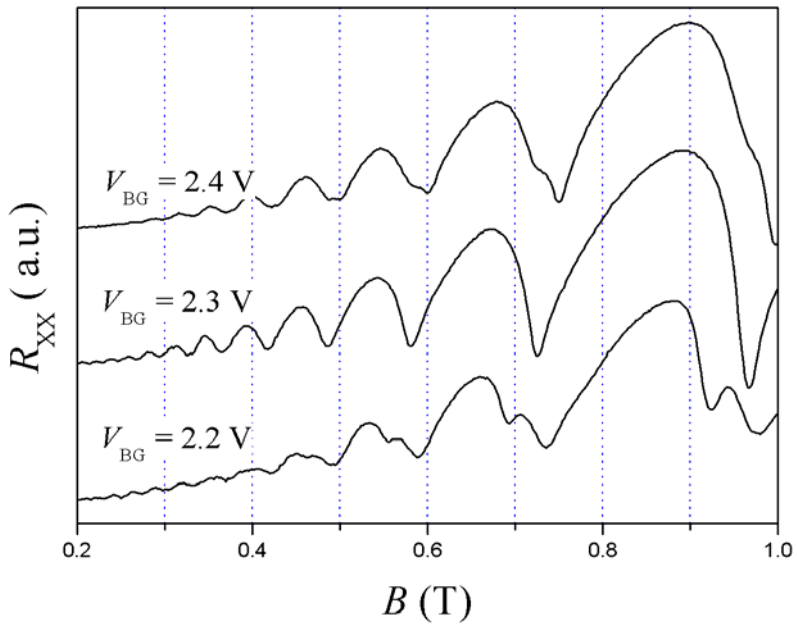

Fig. 4-6. Shubnikov-de Haas (SdH) oscillations of the DQW sample at T = 1.5 K. The SdH oscillations with three different back gate biases (V_{BG}) near the equal electron densities of both quantum wells are displayed. The unit of y-axis is set to be arbitrary for simplicity.

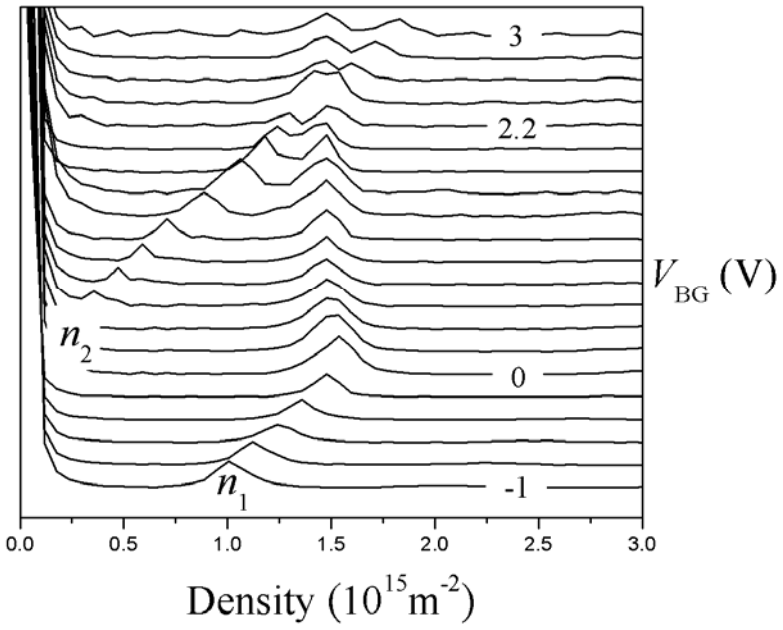

Fig. 4-7. 1/ *B* Fast Fourier Transforms of SdH oscillations for V_{BG} from –1 to 3 V in steps of 0.2 V at T = 1.5 K. When V_{BG} is between 2.2 and 2.4 V, n_1 is almost equal with n_2.

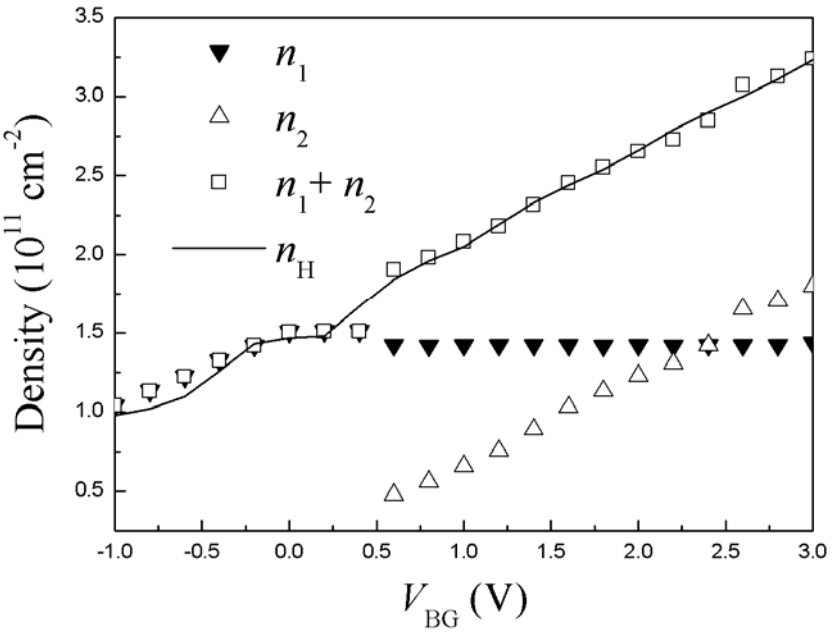

Fig. 4-8. Measured electron densities as a function of V_{BG} determined by FFT analysis of SdH oscillations (symbols) and the Hall effect (solid line).

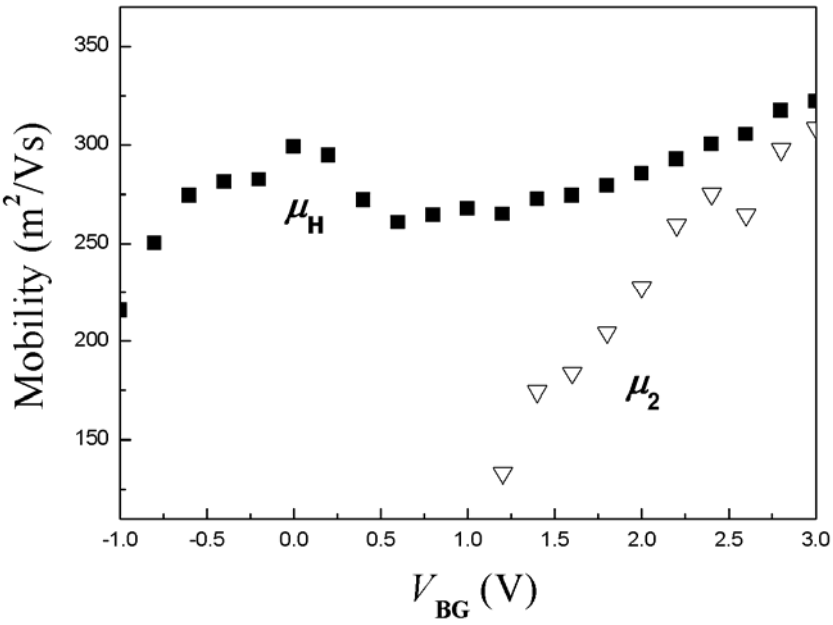

Fig. 4-9. Measured Hall mobility, μ_H (close squares), and estimated mobility, $\mu_{2,}$ (open triangles) of the lower quantum well as a function of V_{BG}.

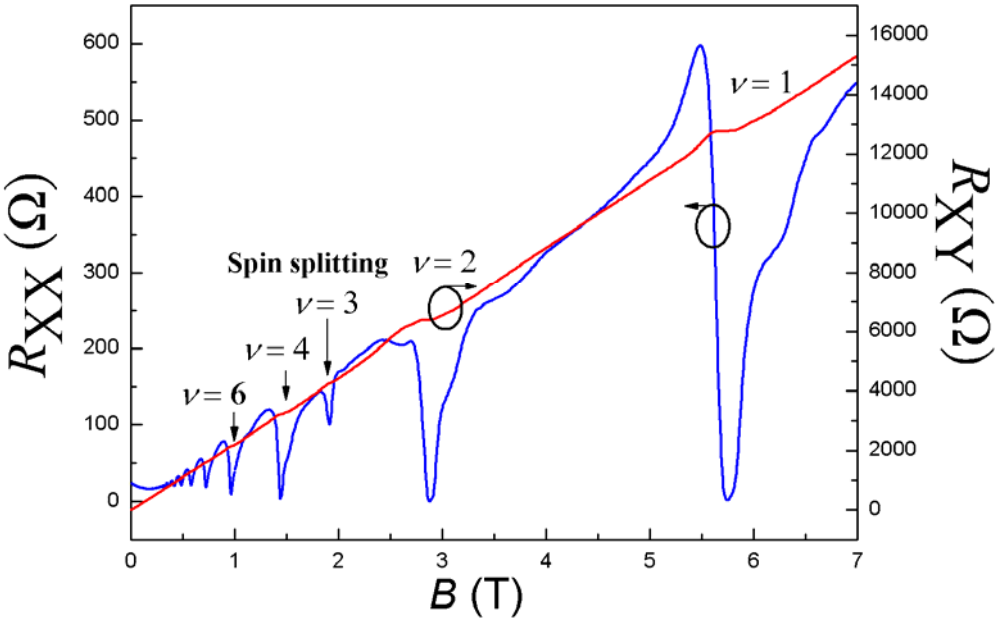

Fig. 4-10. Longitudinal resistance (R_{XX}) and transverse resistance (R_{XY}) as a function of perpendicular B (V_{BG} = 2.3 V). The filling factor 1 occurs when R_{xy} = 12.9 K because of the equivalent electron densities on both layers. The spin splitting can be seen at $\nu = 3$ at around 2 Tesla.

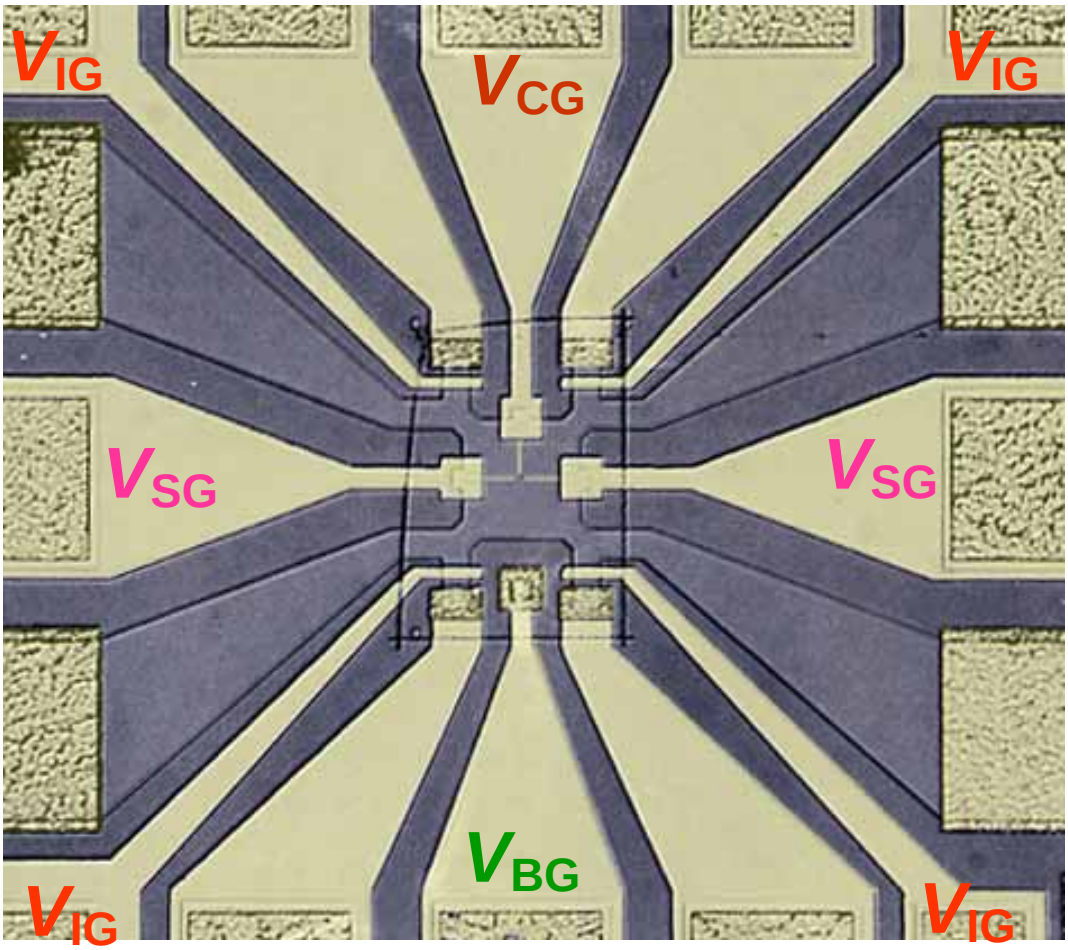

Fig. 4-11. Optical picture of the device layout after metallization. This mask pattern was designed specifically for the fabrication of the DQW sample. However, it is also compatible for SQW wafer. Two quantum wells in the DQW sample can be operated independently through isolation gate and focus ion beam (FIB) lithographic back gate.

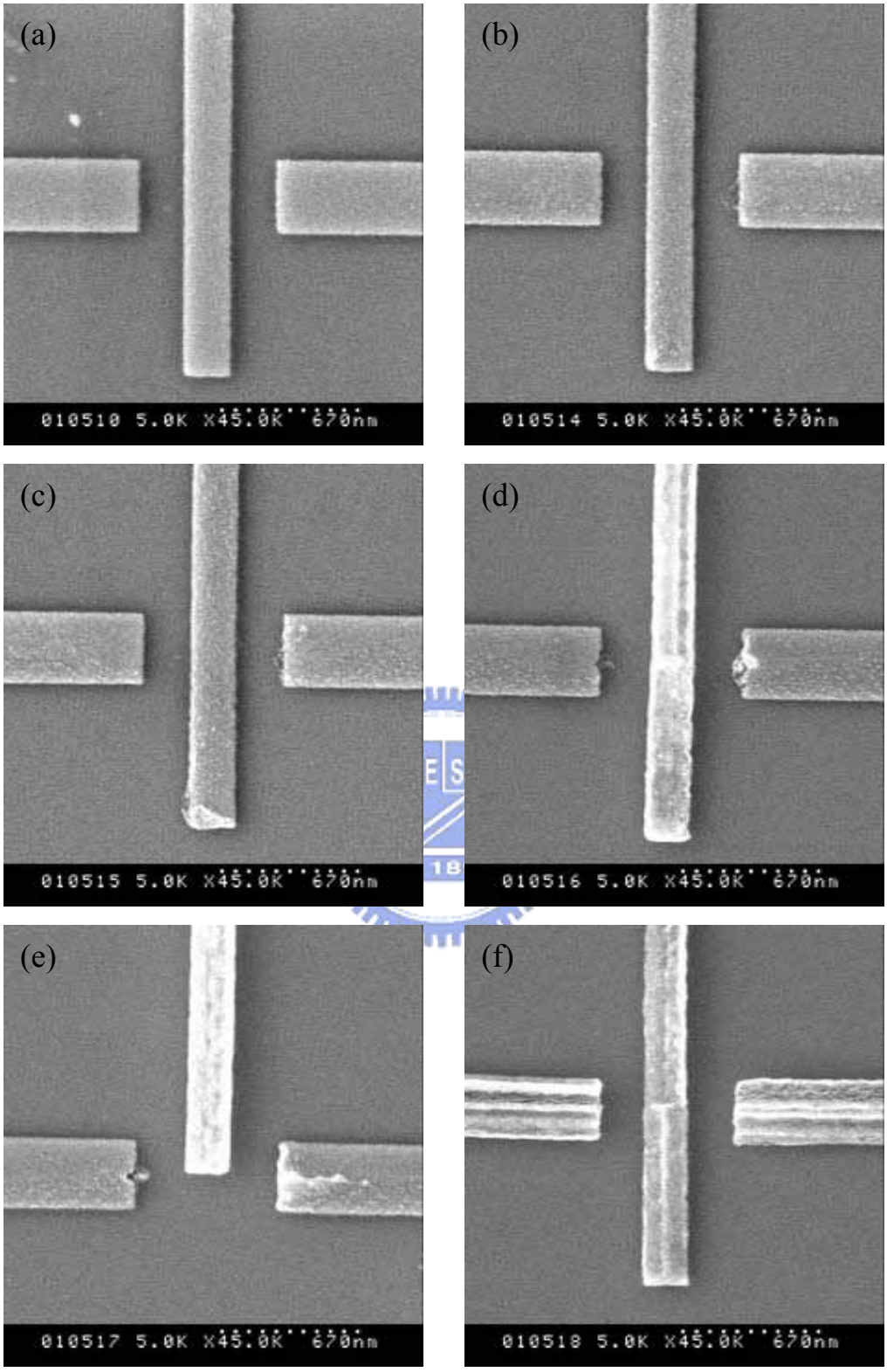

Fig. 4-12. SEM photographs of the triple-gate structure with six different EB dosages after lift-off process. The EB dosage decreases as the figure number increases. As shown in figure (f), the incomplete structure is due to insufficient EB dosage in comparison with figure (a) showing the sharp and clean structure with gap of about 200 nm.

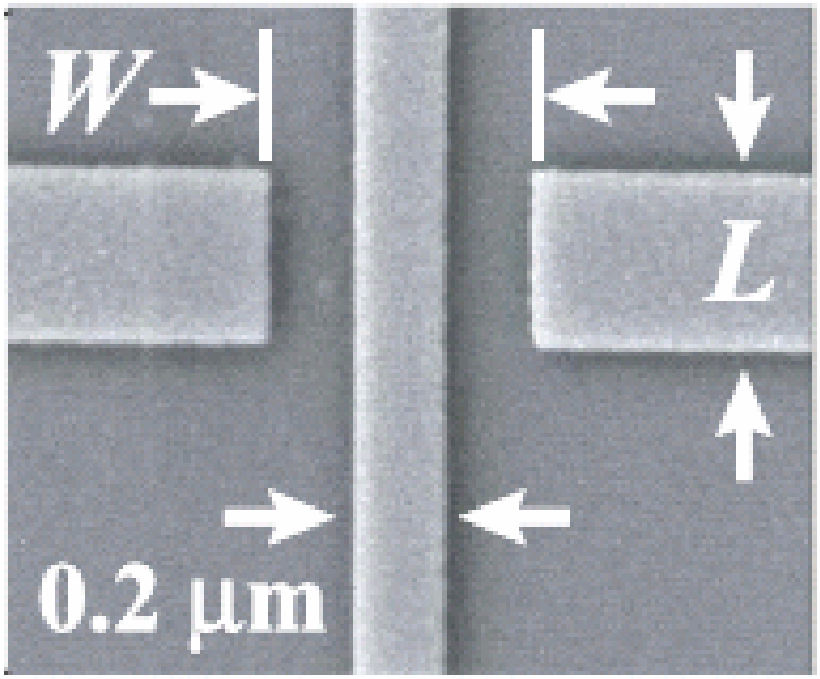

Fig. 4-13. Enlarged SEM image of the triple-gate structure. The length (L) and width (W) of the split gates were varied as L = 0.2-2 μm and W = 0.4-0.8 μm, respectively, while the width of the center gate was fixed at 0.2 μm.

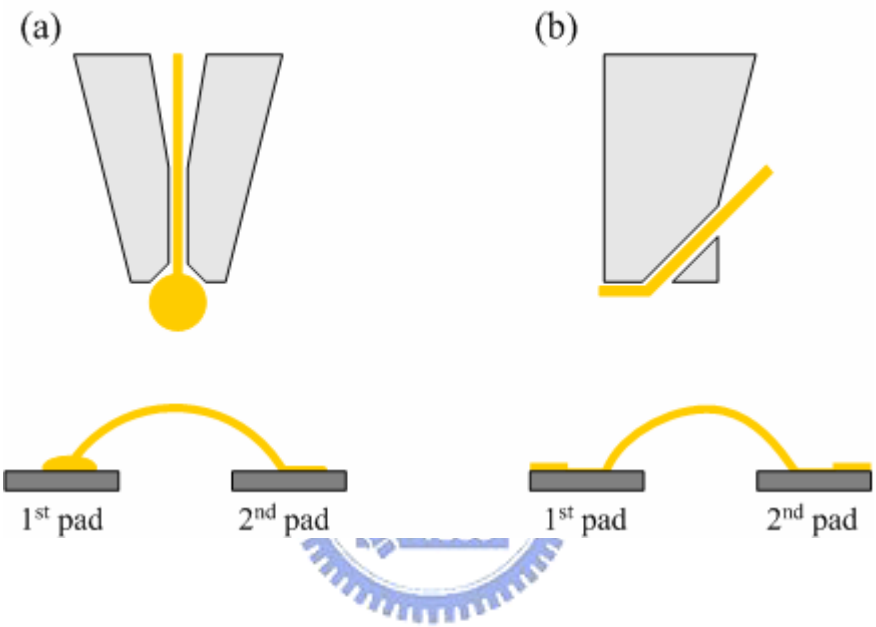

Fig. 4-14. Schematic drawing in comparison of ball bonds (a) and wedge bonds (b). The upper part shows the difference of the bonding tools (capillary and wedge). The lower part shows the bonds formed on 1st pad and 2nd pad, respectively.

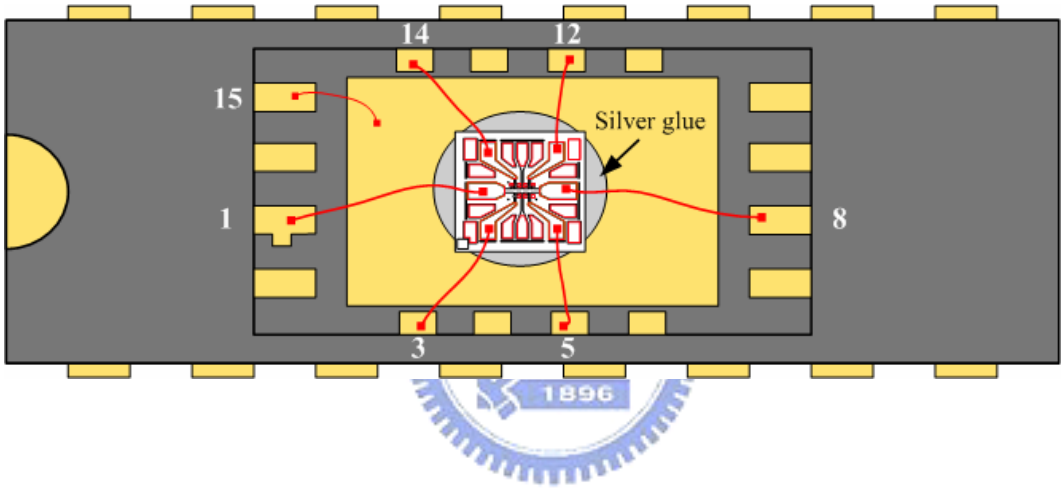

Fig. 4-15. Schematic top view of the chip carrier and the sample with the gold wires soldered to the carrier's leads.

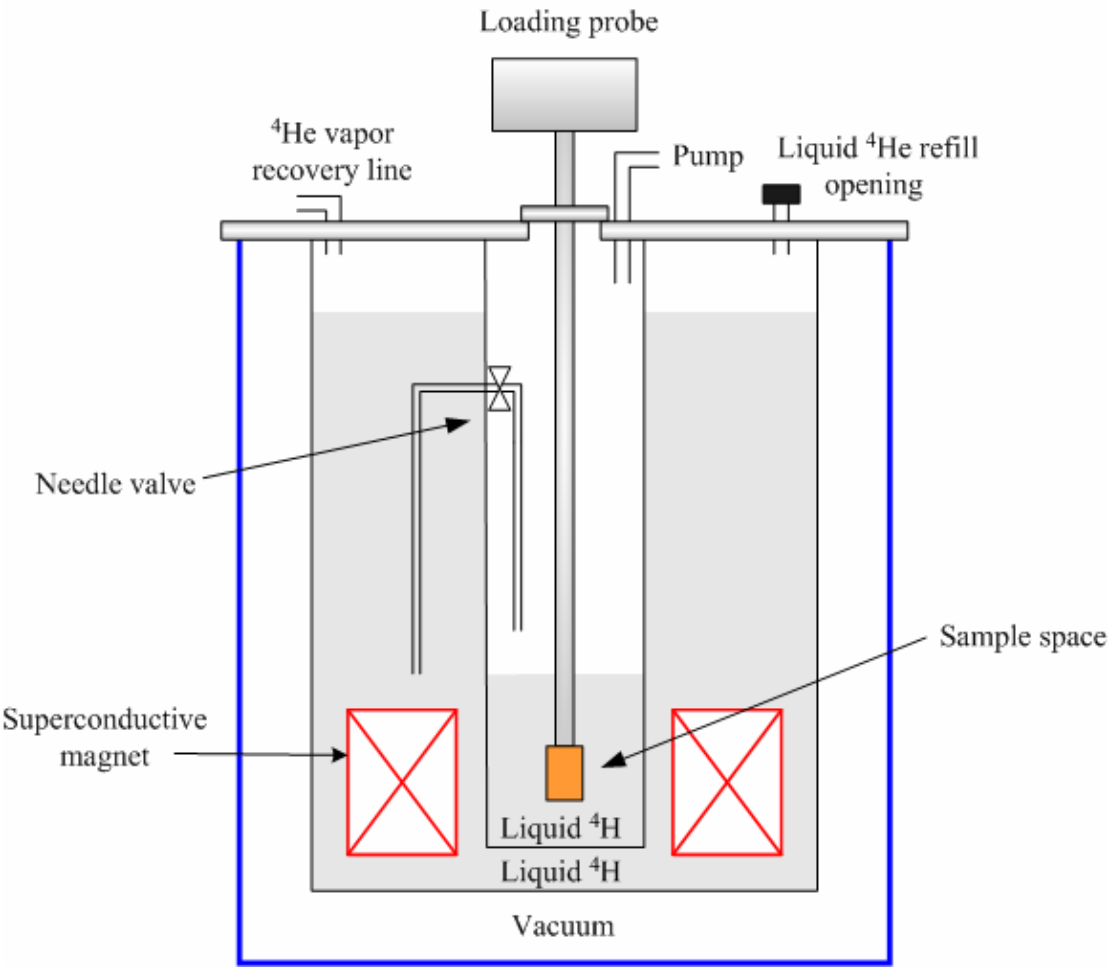

Fig. 4-16. Schematic cross-sectional drawing of the 1.5 K ^{4}He cryostat system (Oxford).

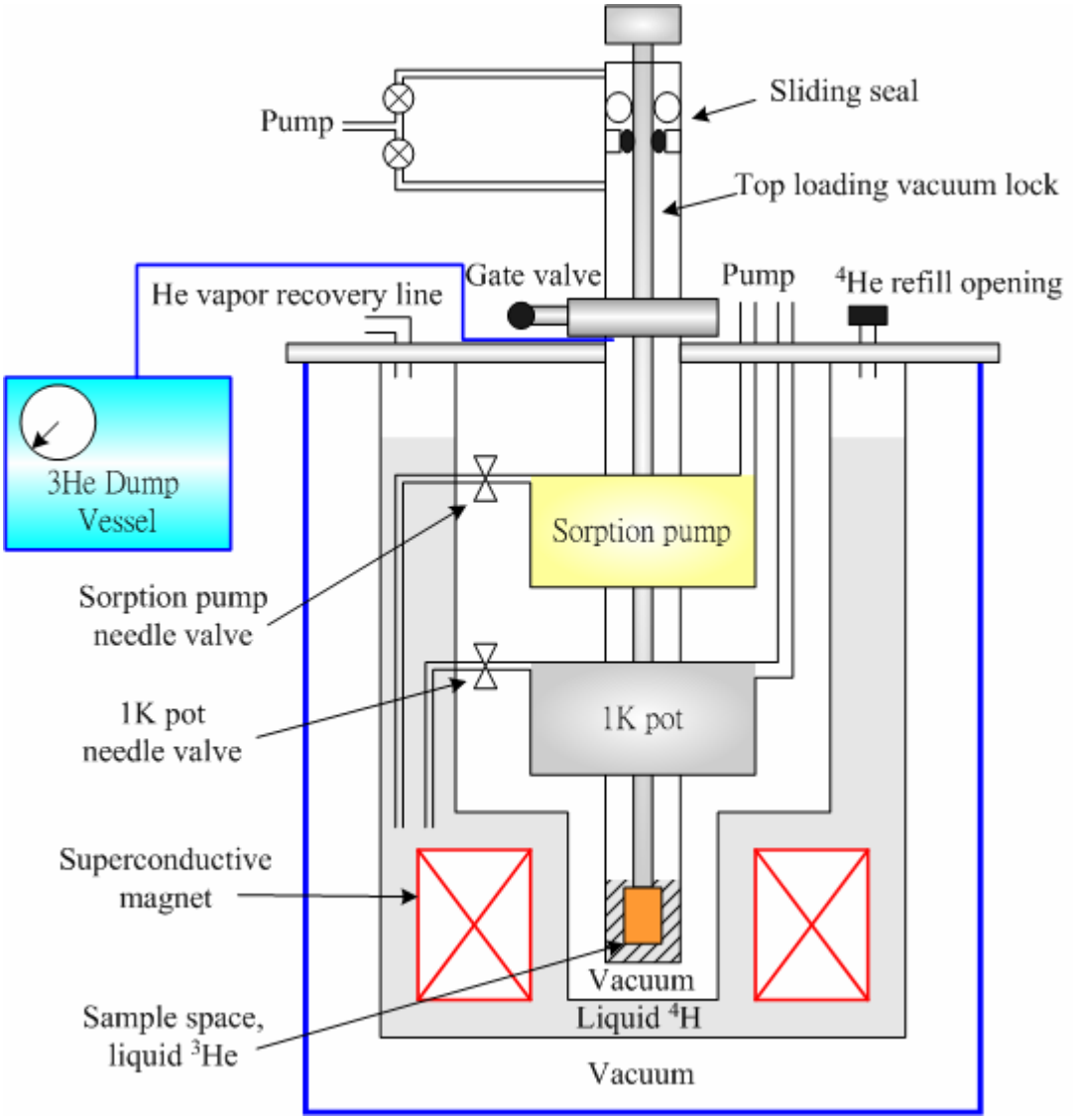

Fig. 4-17. Schematic cross-sectional drawing of the 0.3 K ^{3}He cryostat system (Oxford).

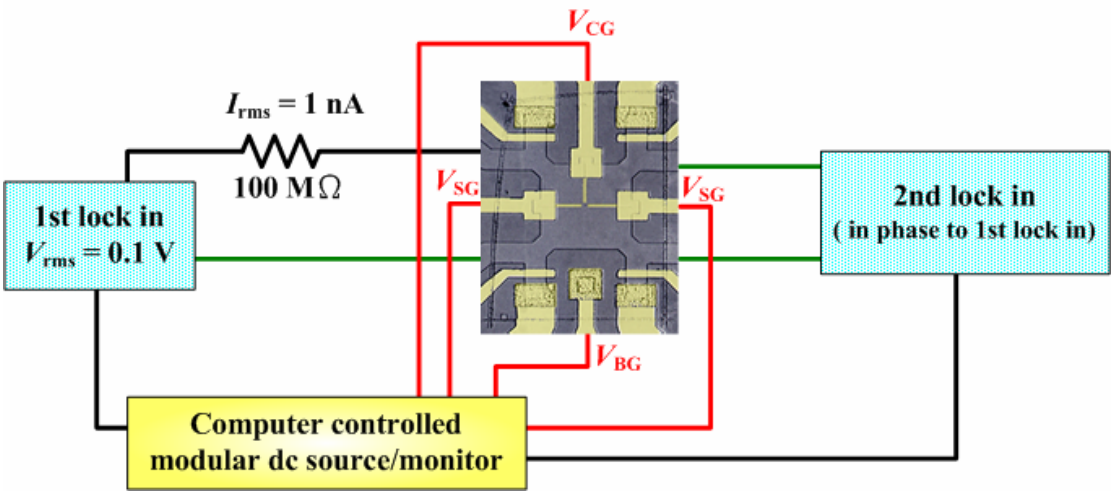

Fig. 4-18. Schematic circuit diagram of a four-terminal current bias measurement set-up. The first lock-in amplifier sources an ac voltage, V_{rms} = 0.1 V, which is converted into a constant ac current, I_{rms} = 1 nA, via a 100 MΩ resistor. The gate voltages are all computer controlled by virtual equipment of LabVIEW automatically.

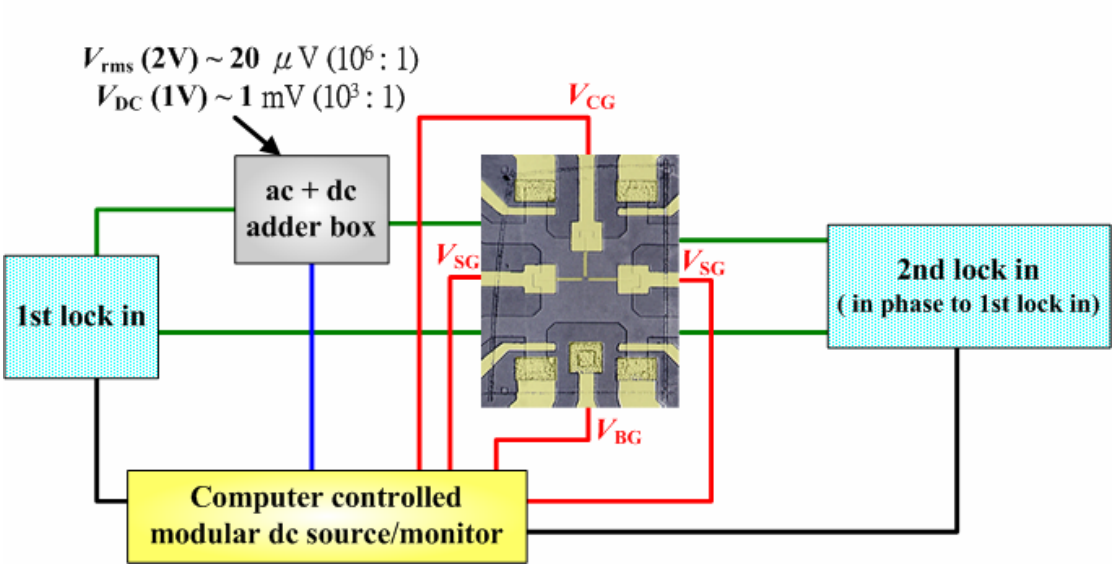

Fig. 4-19. Schematic circuit diagram of a four-terminal voltage bias measurement set-up. The ac + dc adder box combines and divides the two voltage components; the box has a 100,000 : 1 divider for the ac voltage and a 1000 :1 divider for the dc voltage at 77 Hz.

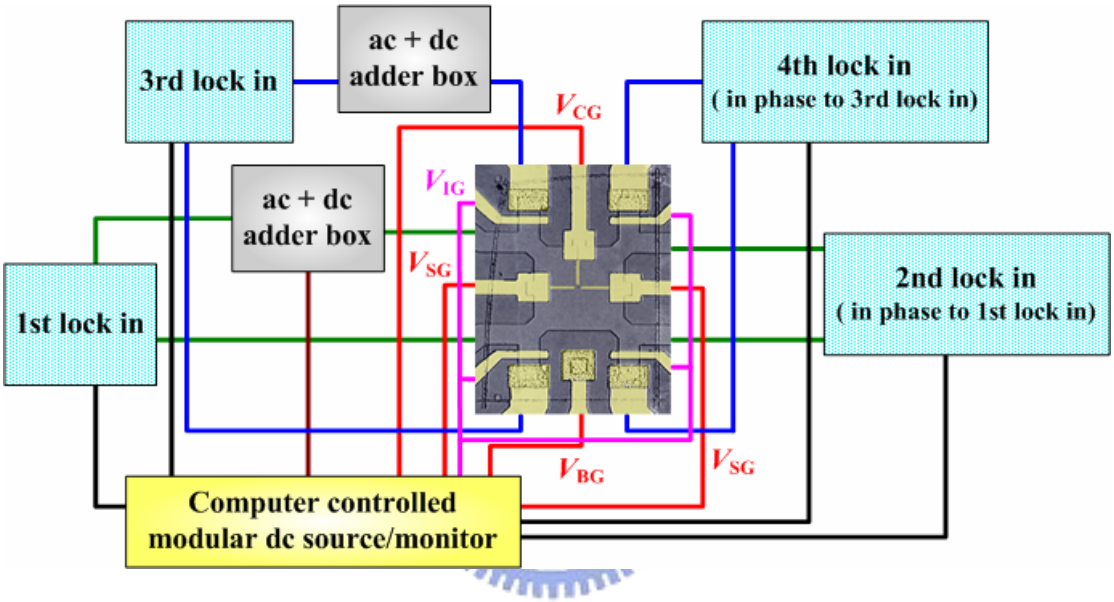

Fig. 4-20. Schematic circuit diagram of a four-terminal voltage bias measurement set-up used for DQW sample.

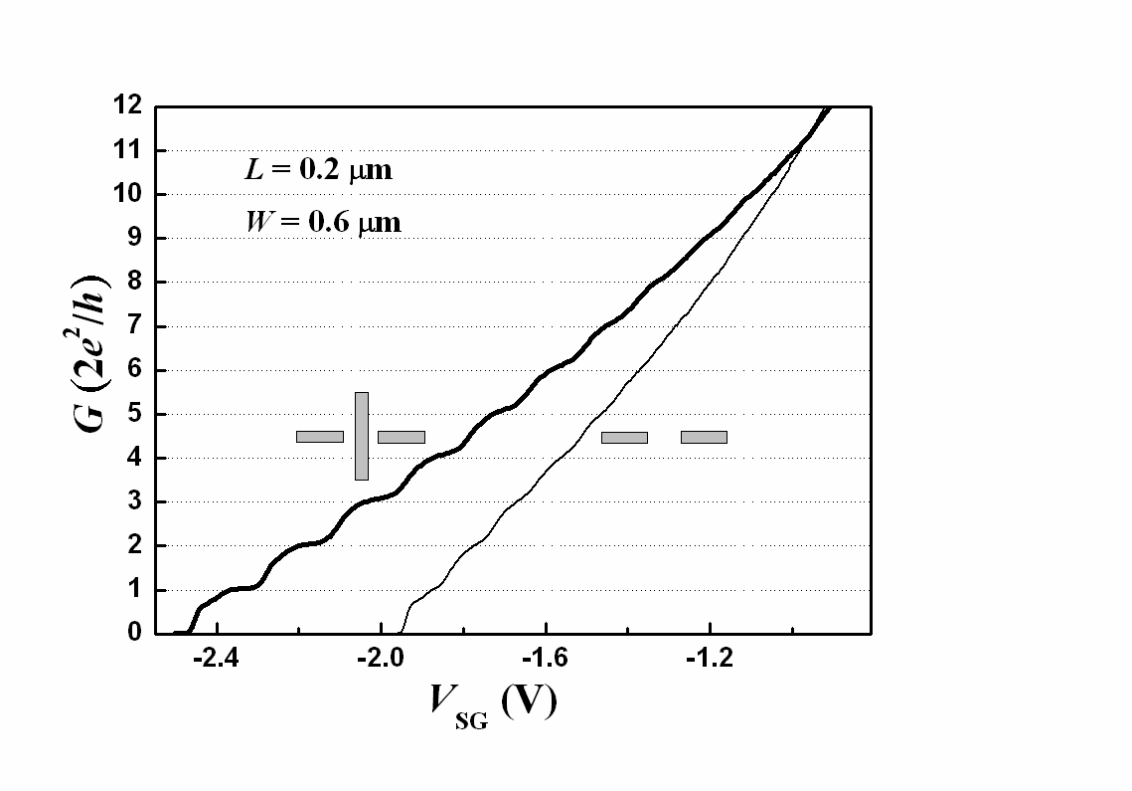

Fig. 4-21. Conductance G measured at 1.5 K as a function of split gate voltage V_{SG} of devices with (thick line) and without (thin line) center gate. The two devices have the same split-gate geometry, L = 0.2 and W = 0.6 μm.

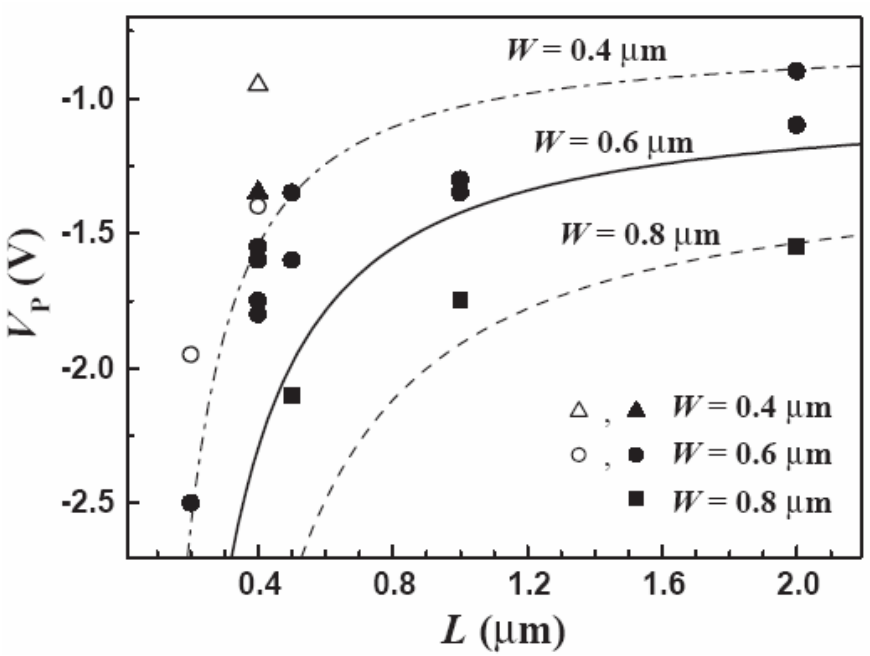

Fig. 4-22. Pinch-off voltage V_P of devices with different channel width W, plotted as a function of channel length L. Solid (open) symbols indicate devices with (without) center gate. For those with center gate, the center-gate bias is kept at V_{CG} = 0 V. Three curves represent the pinch-off voltages calculated as a function of L for different W using eq.(4-1).

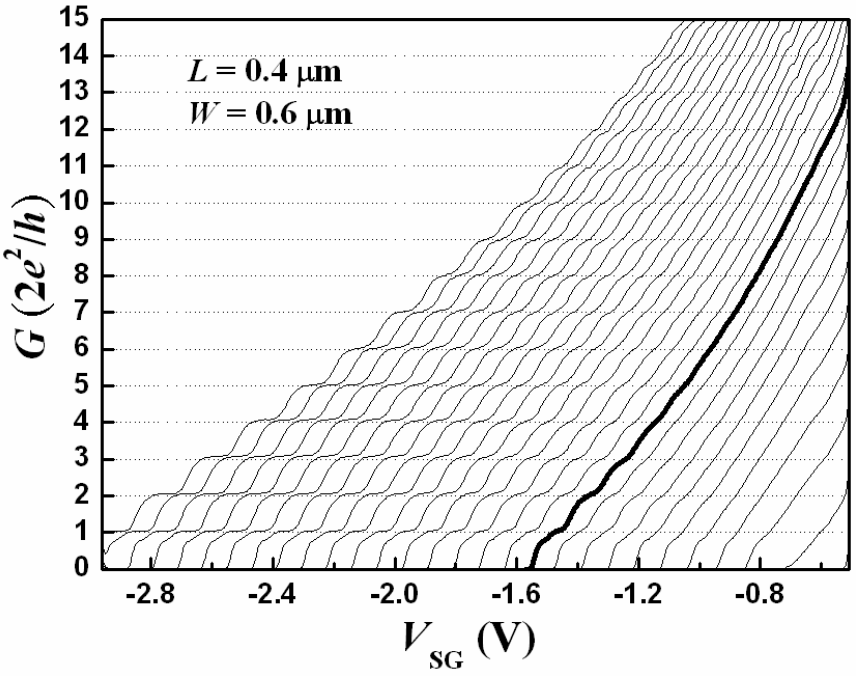

Fig. 4-23. G of a device with L = 0.4 μm and W = 0.6 μm measured at 1.5 K as a function of V_{SG}. From left to right, the center gate voltage V_{CG} is varied from 0.9 to -0.45 V in 0.05 V step. The thick line corresponds to V_{CG} = 0 V.

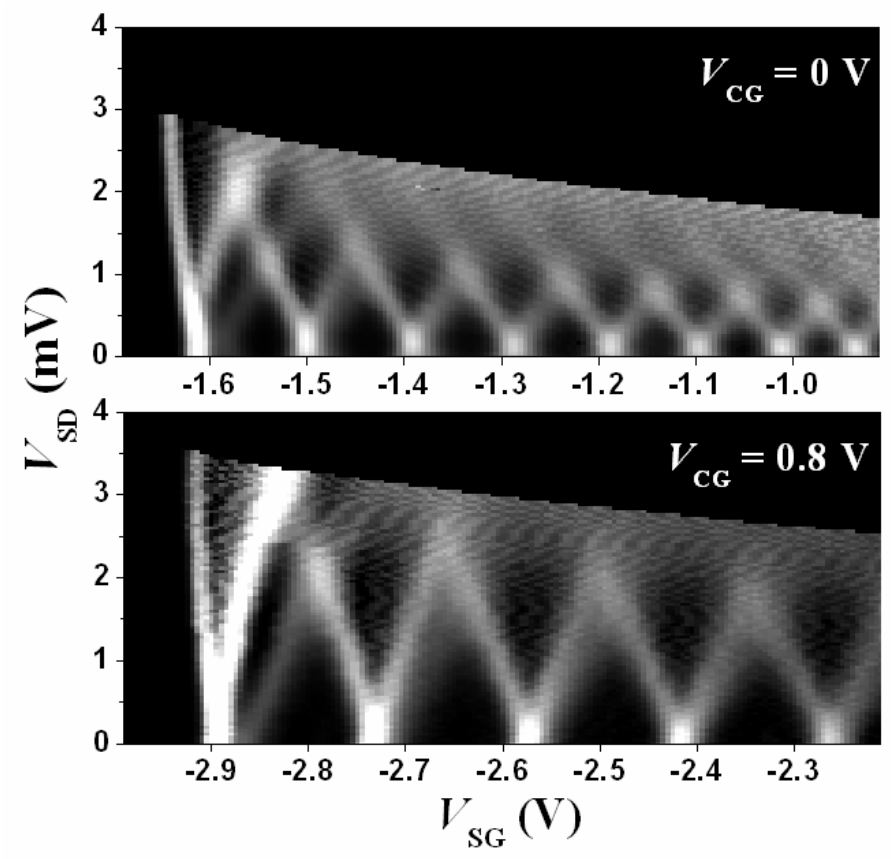

Fig. 4-24. Gray-scale plots of transconductance dG/dV_{SG} measured at T = 0.24 K as a function of V_{SG} and source-drain bias (V_{SD}) for V_{CG} = 0 (upper panel) and 0.8 V (lower panel). Bright features indicate peaks in dG/dV_{SG}.The sample is the same as in Fig. 4-23 (L = 0.4 μm and W = 0.6 μm).

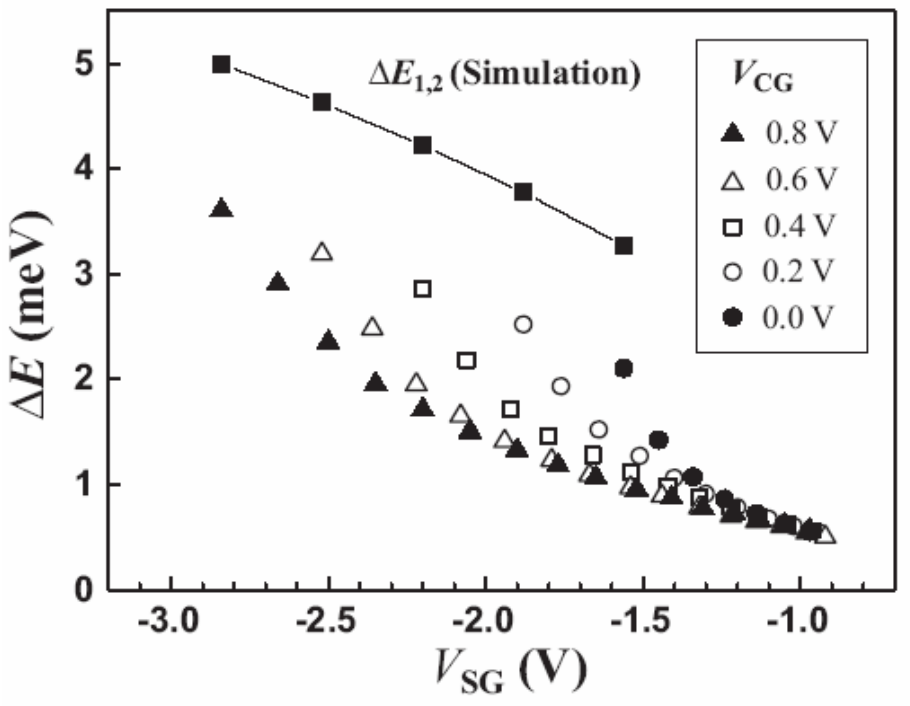

Fig. 4-25. Energy separation ΔE of adjacent subbands deduced from the transconductance data in Fig. 4-24, plotted as a function of V_{SG} for various V_{CG} varied from 0 to 0.8 V in 0.2 V step. The leftmost data point for each V_{CG} corresponds to the lowest subband energy separation $\Delta E_{1,2}$. Solid squares represent $\Delta E_{1,2}$ calculated for each set of V_{SG} and V_{CG}. The sample is the same as in Fig. 4-23 (L = 0.4 μm and W = 0.6 μm).

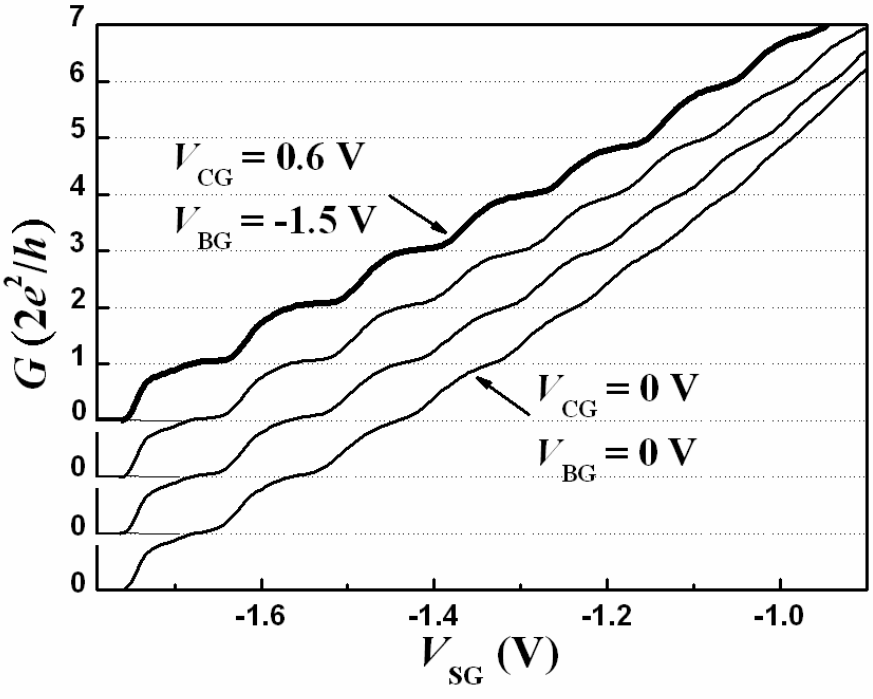

Fig. 4-26. G vs. V_{SG} for different combinations of V_{CG} and V_{BG} at 1.5 K. From bottom to top, V_{CG} is increased from 0 to 0.6 V in 0.2 V step while V_{BG} is decreased from 0 to -1.5 V in 0.5 V step to keep the same pinch-off voltage. The sample is the same as in Fig. 4-23 (L = 0.4 μm and W = 0.6 μm).

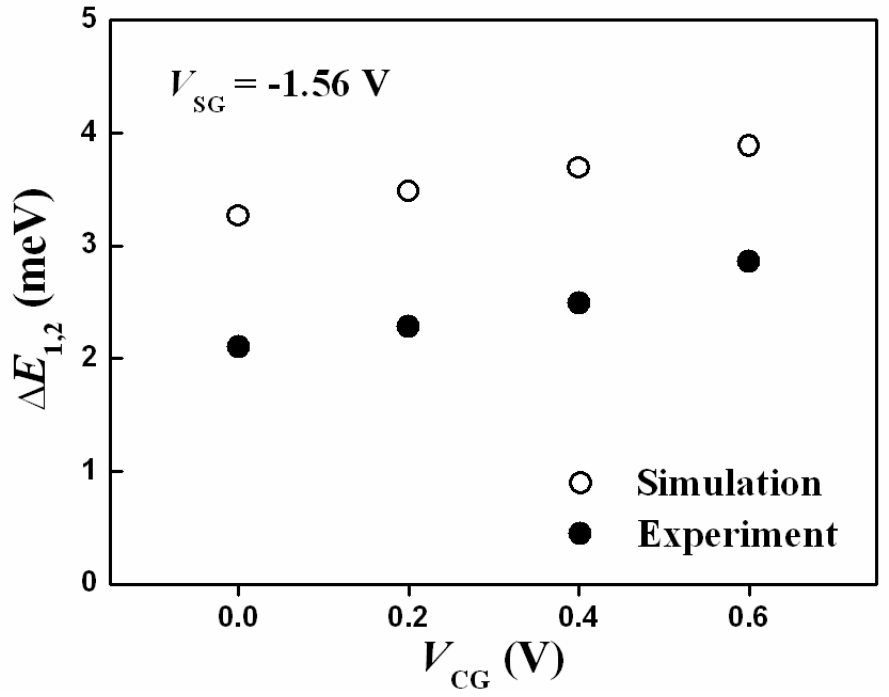

Fig. 4-27. $\Delta E_{1,2}$ for each set of V_{CG} and V_{BG}, in Fig. 4-26, plotted as a function of V_{CG}. Open and closed symbols represent results of simulation and experiment, respectively.

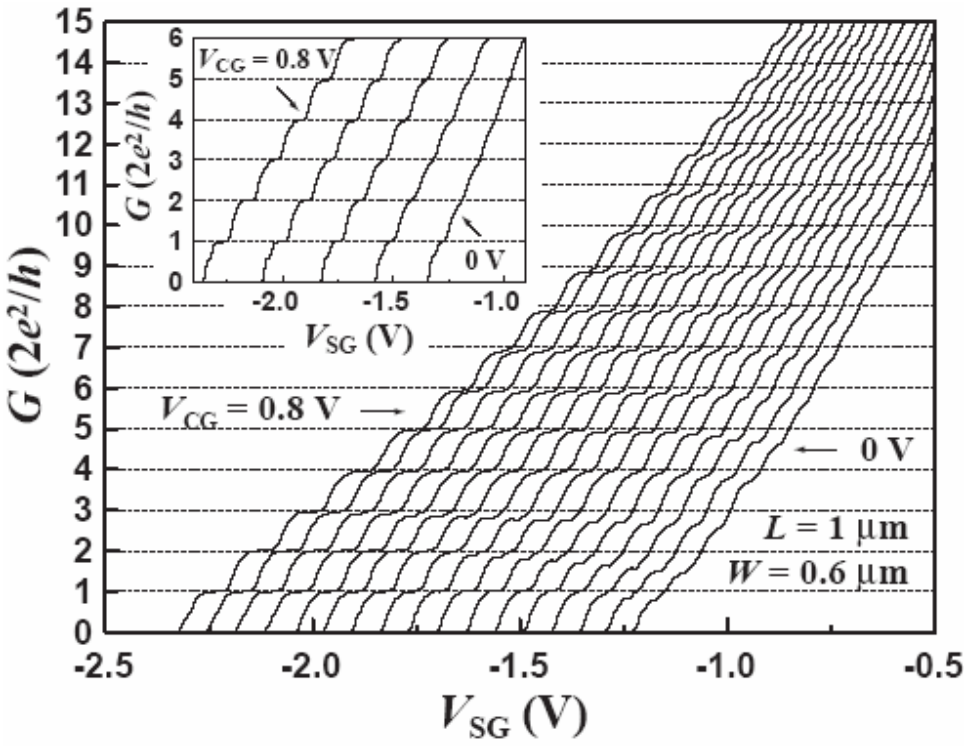

Fig. 4-28. G vs. V_{SG} of a device with L = 1 μm and W = 0.6 μm (T = 1.4 K). From right to left, V_{CG} is increased from 0 to 0.8 V in 0.05 V step. Inset: G vs. V_{SG} of the same device for a different cool down.

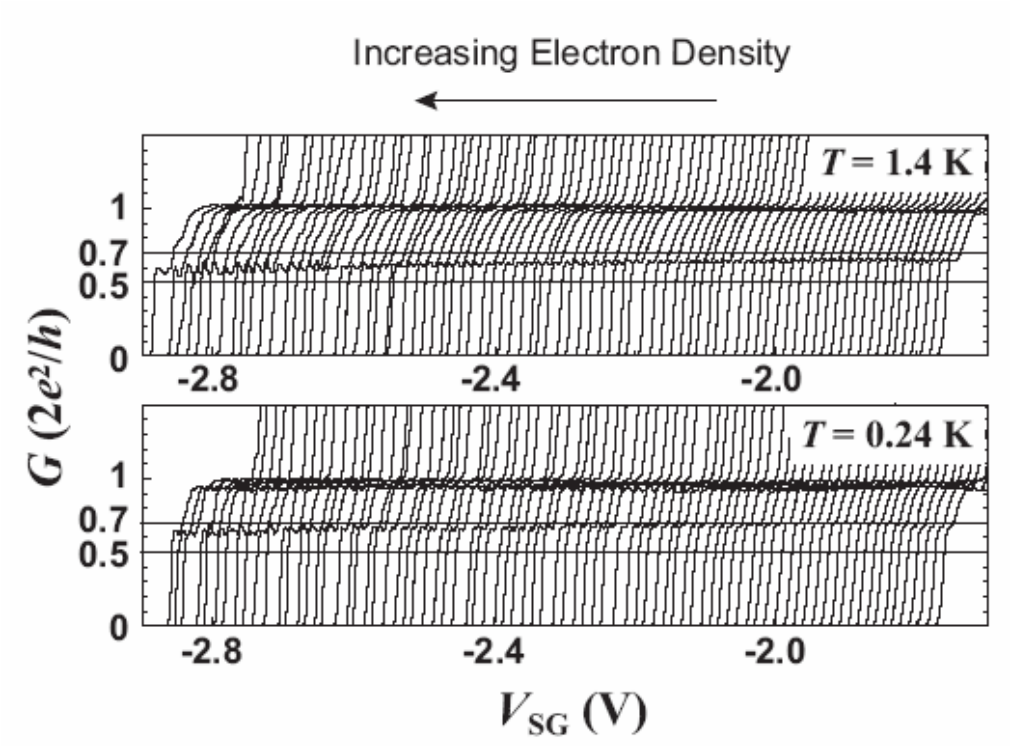

Fig. 4-29. G vs. V_{SG} of the same device as in Fig.4-28 (L = 1 μm and W = 0.6 μm), measured at 1.4 K (upper panel) and 0.24 K (lower panel). From right to left, V_{CG} is increased from 0 to 0.8 V in steps of 0.01 V. Here, positive back-gate bias of V_{BG} = 1 V is applied to enhance ballistic transport. Two horizontal lines indicate the positions of $0.7\times 2e^2/h$ and $0.5\times 2e^2/h$.

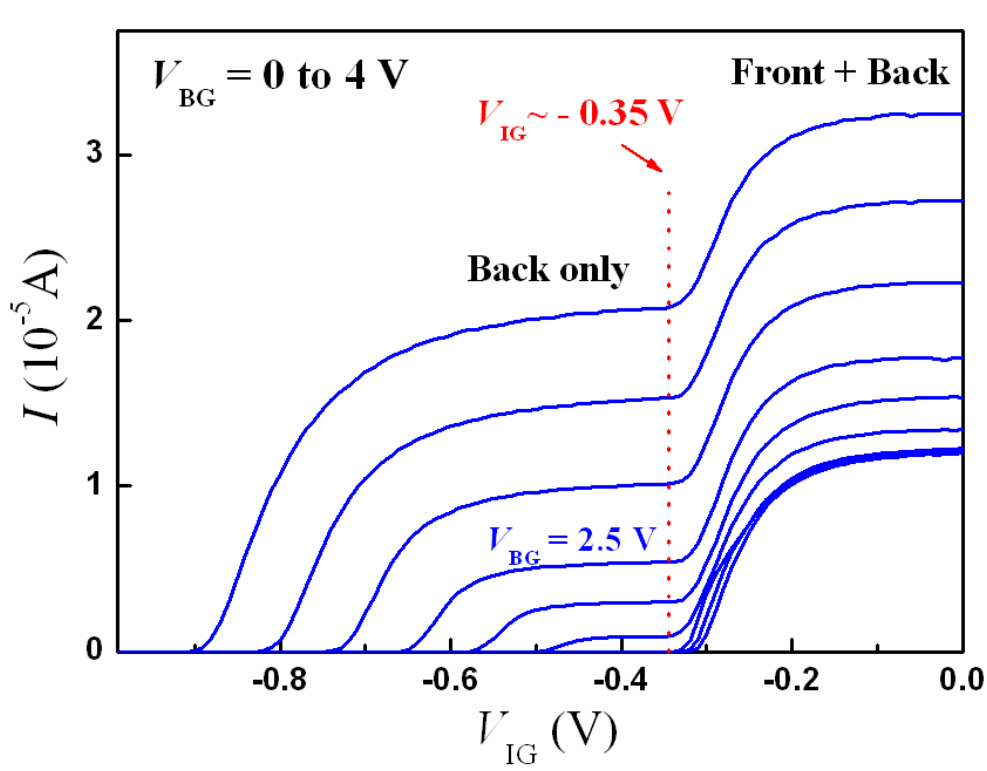

Fig. 4-30. Depletion characteristics of the DQW sample as a function of V_{IG} with V_{BG} varied from 0 to 4 V at 4.2 K. A constant 10 mV is fed to small contact and the current is measured by another small contact.

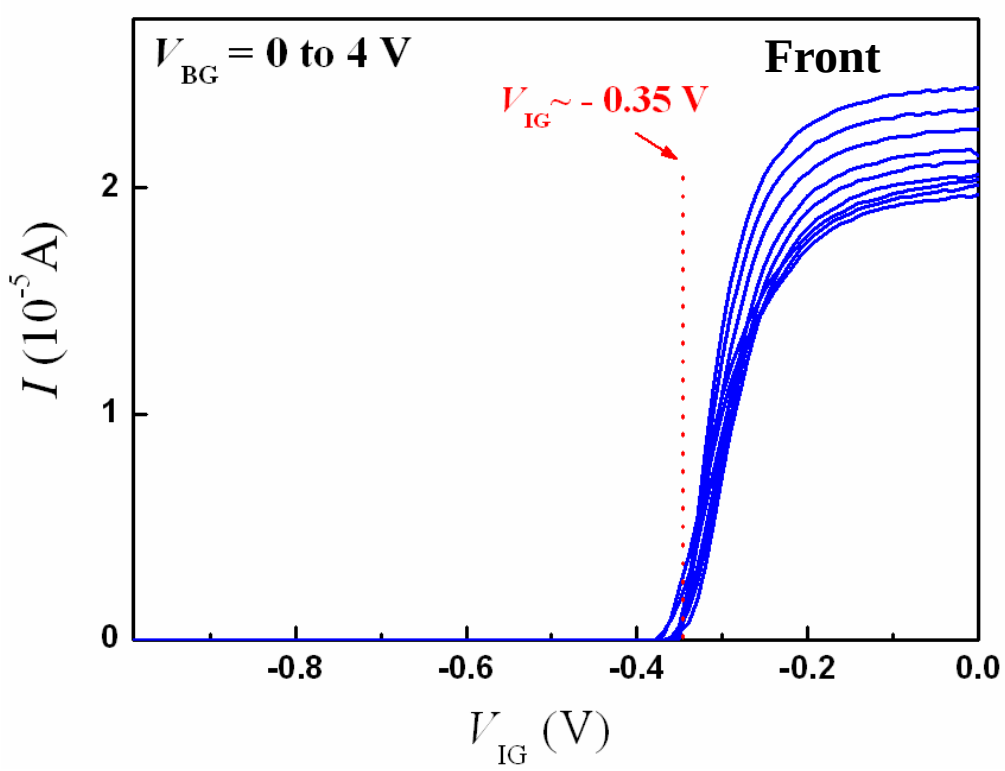

Fig. 4-31. Depletion characteristics of DQW sample as a function of V_{IG} with V_{BG} varied from 0 to 4 V at 4.2 K. A constant 10 mV is fed to small contact and the current is measured by another big ohimc contact.

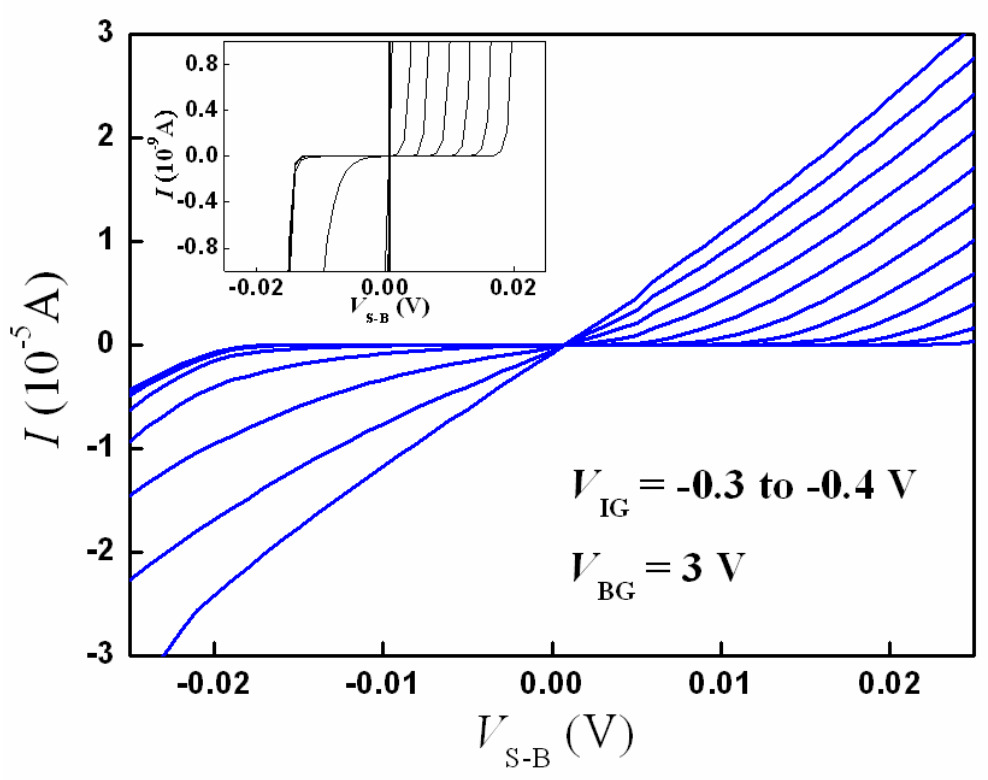

Fig. 4-32. Interlayer leakage current measurement of the DQW device. The V_{IG} is varied from -0.3 to -0.4 V. The V_{BG} is kept at 3 V to make lower layer conducting. Inset: the interlayer bias of 20 mV with leakage current smaller than 1 nA.

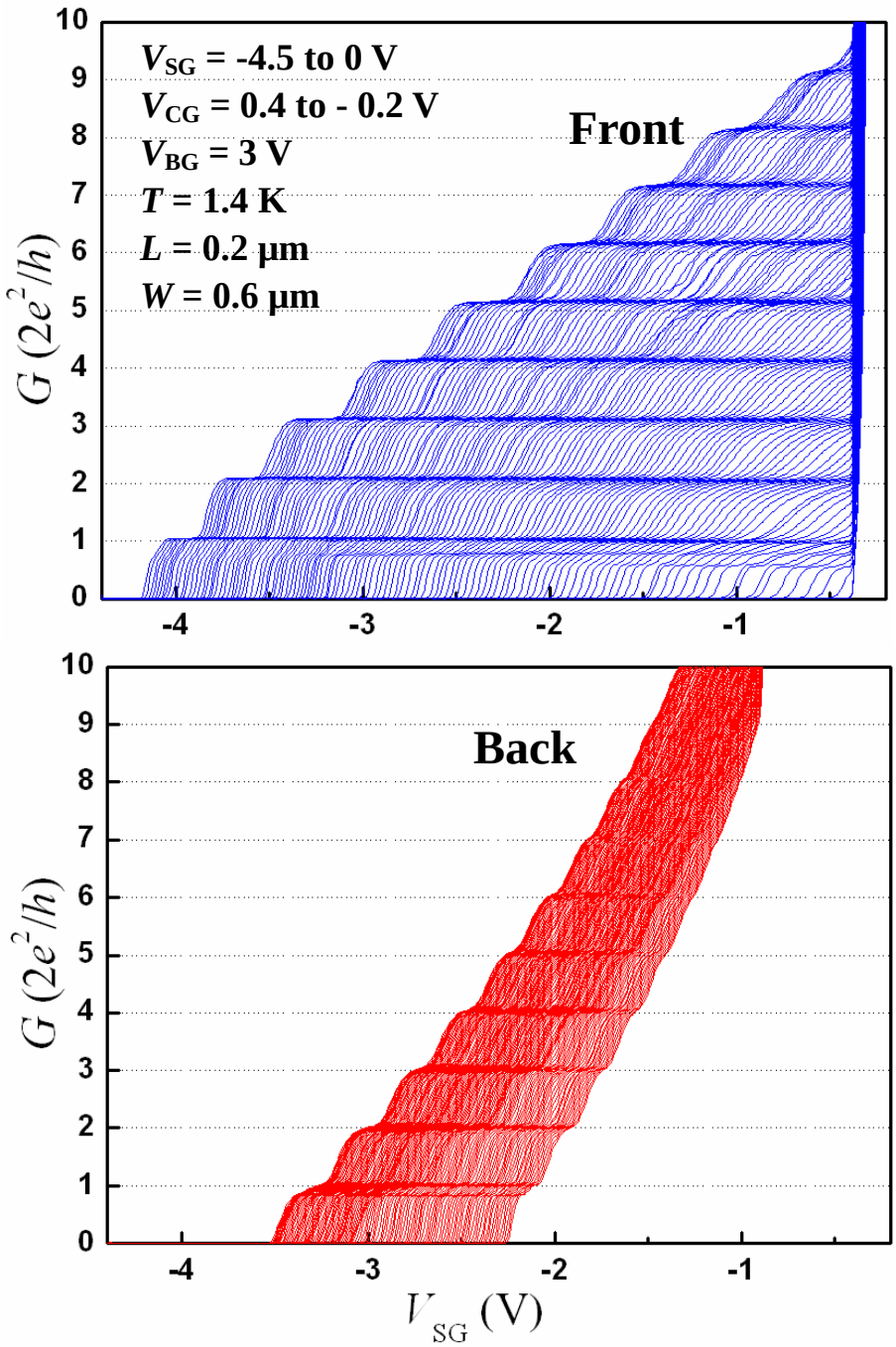

Fig. 4-33. G plots of the DQW device with L = 0.2 μm and W = 0.6 μm measured at 1.4 K as a function of V_{SG}. From left to right, the V_{CG} is varied from 0.4 to -0.2 V. The blue curve presents the measured G of the front layer while the red one shows the G for the back layer.

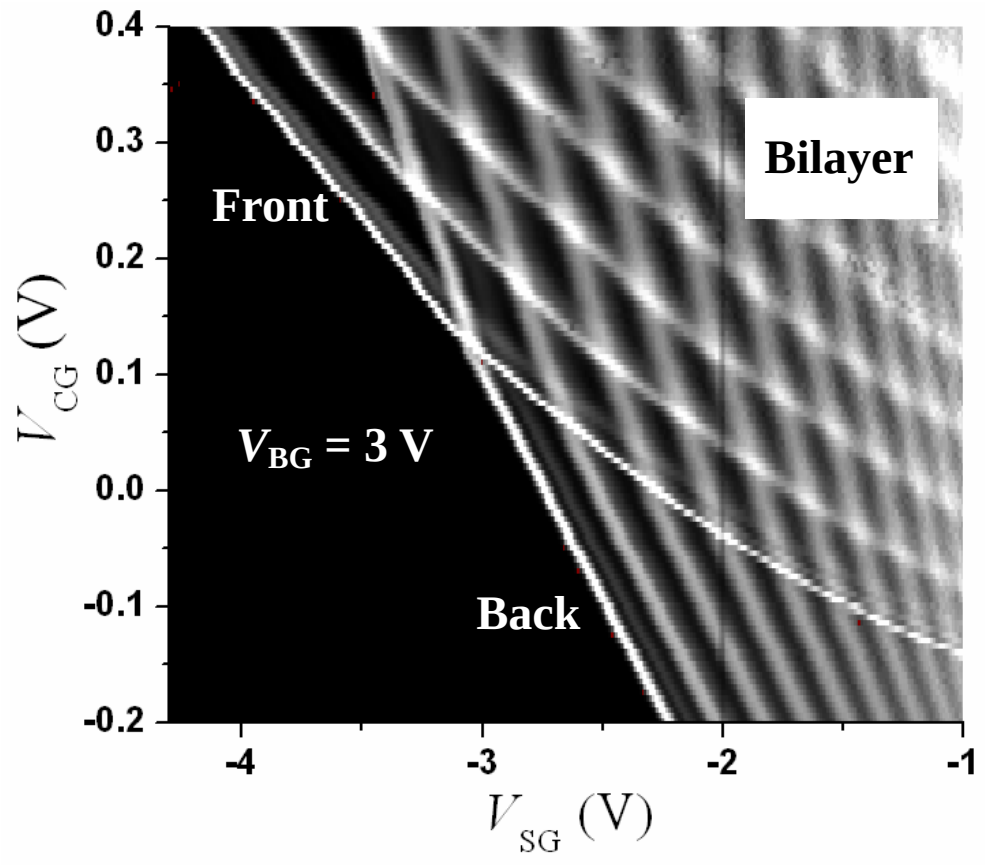

Fig. 4-34. Gray-scale plot of transconductance dG/dV_{SG} measured at T = 1.4 K as a function of V_{SG} for V_{CG} = - 0.2 to 0.4 V. Bright features indicate peaks in dG/dV_{SG}. V_{BG} is kept at 3 V. Two layers are simultaneously pinch-off at V_{CG} = 0.1 V. The sample is the same as in Fig. 4-33 (L = 0.2 μm and W = 0.6 μm).

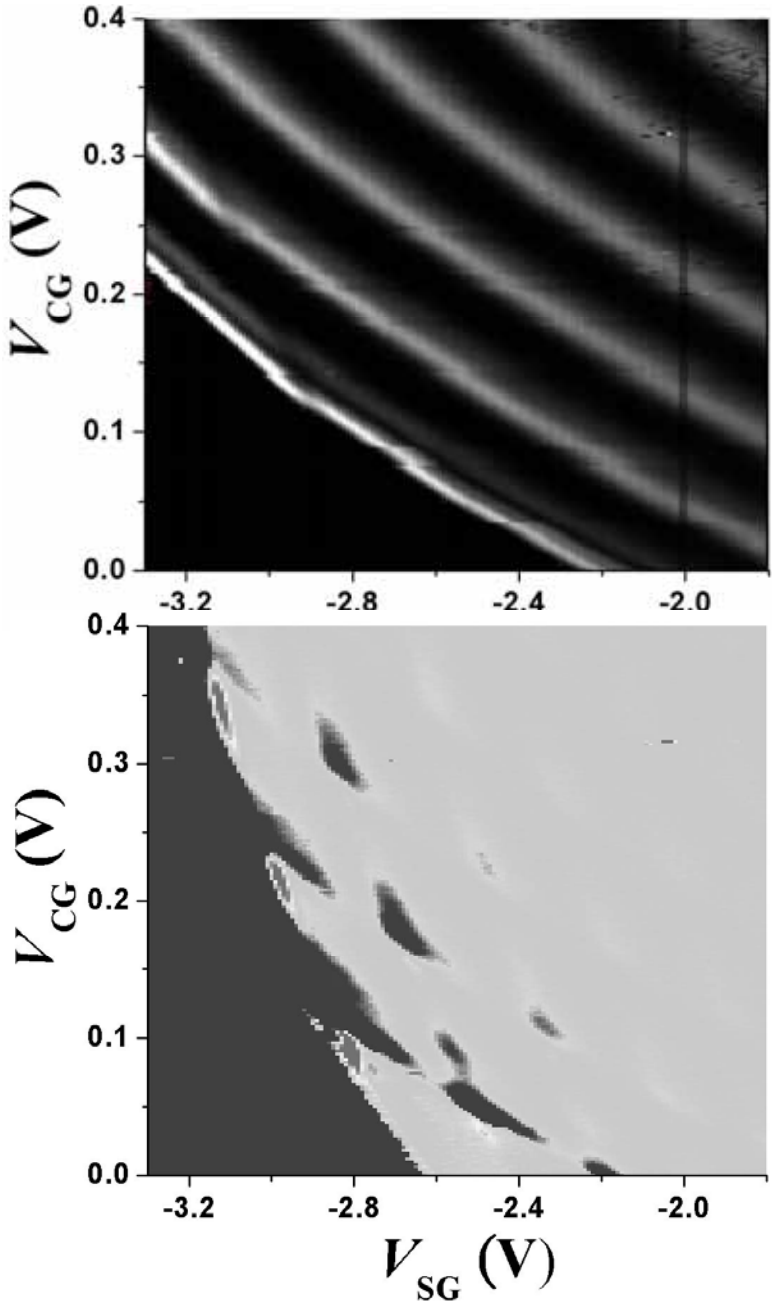

Fig. 4-35. Gray-scale plots of transconductance dG/dV_{SG} measured at T = 1.4 K as a function of V_{SG} for V_{CG} = 0 to 0.4 V. Bright features in the upper plot indicate peaks in dG/dV_{SG}. The upper plot shows the transconductance of one quantum well while the lower one exhibits the drag signal on the adjacent well. The negative resistance occurs at the cross point of the bilayer region as indicated in Fig. 4-34.

Chapter 5

Conclusions

In this dissertation, on one hand, we briefly introduced the EB lithography technique used in our laboratory and demonstrated its practical application in fabrication of nanometer T-shaped gate by using thermally reflowed resist for high speed devices. On the other hand, for LD semiconductor structures, the control of ordering of self-organized Ge dots by the surface morphology of the patterned Si substrate and the quantum transport characteristics in 1D narrow constrictions have been extensively studied both on experiment as well as numerical simulation. The primary results obtained in this dissertation are concluded below:

(1) The novel method for fabricating ultra-short 30-nm T-gate on the GaAs substrate by combining advanced EB lithography and thermally reflowed resist technique has successfully been demonstrated. The effects of reflow temperature and reflow time on the gate length formed were illustrated. The typical as-developed 160-nm-T-gate patterns can be easily shrunk to nanometer scale in length ranging from 150nm to 30 nm after a simple thermal reflow procedure without any substential change to the top layer resist structure of the T-gate. Finally, a 30 nm T-gate was demonstrated using this reflow technique which is the smallest T-gate with the thermally reflowed technique reported in the literature so far and can practically be used in the GaAs MMIC fabrications.

(2) The controlled placement of self-organized Ge QDs by the surface morphology of the patterned Si (001) substrate has been studied. We have observed the formation of the Ge dots on dot and anti-dot mesas. The sizes of the grown Ge dots are

approximately 10 nm. The dot density of Ge on Si dot mesa was estimated to be 3×10^{10} cm^{-2}. The Ge dots tend to form along the Si mesa edge, and their distribution could be controlled by the pattern shape. In some cases, in addition to the formation on the mesa edge, the Ge dots were also observed at the center of the mesa top. We also found that inhomogeneous mesa pattern may cause poor uniformity of the formation of the Ge dots. We also calculated the formation of Ge dots on Si dot mesas by a local strain-mediated surface chemical potential in 3D models. The simulation data clearly reproduce the positions of the local minima of the total surface chemical potential where the Ge dots tend to form. The overall behavior between simulation and experiment is quite consistent. This study provides a possible picture to manipulate the self-organized nanostructures with expected places.

(3) We have fabricated 1D narrow constrictions defined by a triple-gate structure incorporating an additional surface center gate in between the pair of split gates, and studied their transport characteristics both on DQW and SQW devices at low temperature. We performed magnetoresistance measurement to check the wafer quality of the grown wafers. For SQW sample, comparison between devices with and without a center gate revealed that the center gate, even when zero-biased, affects the surface potential and significantly enhances the 1D confinement. Because of the fixed surface potential above the 1D channel, the pinch-off voltage of these devices can be well predicted by an analytical formula based on the pinned-surface model. Nonlinear transport spectroscopy showed that the energy separation between the lowest 1D subbands varies in proportion to the center-gate bias V_{CG} and can be enhanced by 70% for V_{CG} = 0.8 V. The enhanced 1D confinement for positive V_{CG} greatly enhanced 1D ballistic transport, as

manifested by the better-developed conductance plateaus and the suppression of impurity scattering in long-channel devices. For a 1-μm-long-channel device, the anomalous plateau-like feature below the first conductance plateau (the '0.7 anomaly') was observed to evolve toward 0.5(2*e*2/*h*) with increasing V_{CG} and hence increasing electron density. For DQW sample, we demonstrated the basic operations and measured the individual conductance on both layers with separate ohimc contact techniques. Two layers have equal n_{2D} when V_{BG} is around 2.3 V. Front layer can be pinch-off when V_{IG} is around – 0.35 V. Interlayer bias is measured around 20 mV with negligible leakage current smaller than 1 nA. Further, Coulomb drag measurement is carried out showing that the negative resistance tends to occur at the cross point in bilayer region, where the sublevels on both layers are observed with equal electron density. These results clearly demonstrate that the triple-gate structure provides a simple way of controlling the characteristics of 1D constrictions and investigating density-dependent phenomena in a 1D system. In addition, its predictable pinch-off characteristics and enhanced 1D confinement are major advantages over the conventional split-gate structure, the latter being of particular importance when defining constrictions in deep 2DEGs. The structure, which does not require any additional fabrication steps or interfere with other parts of the device, will be particularly suited for lateral integration.