Adaptive Pole-Zero Position (APZP) Technique of Regulated Power Supply for Improving SNR

Chun-Yu Hsieh and Ke-Horng Chen

***Abstract*—This paper proposes an adaptive pole-zero position (APZP) technique to achieve excellent transient response of dc–dc converters. The APZP technique triggers the two-step nonlinear control mechanism to speed up the transient response at the beginning of load variations. Before the output voltage is regulated back to its voltage level, the APZP technique merely functions as a linear control method to regulate output voltage in order to ensure the stability of the system. Fast transient response time, low output ripples, and stable transient operation are achieved at the same time by the proposed APZP technique. Experimental results in the UMC 0.18-μm process show that the transient undershoot/overshoot voltage and the recovery time do not exceed 48 mV and 10 μs, respectively. Compared with conventional design without any fast transient technique, the performances of overshoot voltage and recovery time are enhanced by 37.2% and 77.8%. With the APZP technique, the performance of dc–dc converters is improved significantly.**

***Index Terms*—Adaptive frequency control, current-mode dc–dc converter, fast transient response, load transient, on-chip compensation.**

I. Introduction

AMONG the numerous requirements included in the ability to build high-performance system-on-chip (SoC) applications, the imperative demand is to supply a dynamic voltage in terms of the processing throughputs. Dynamic voltage scaling (DVS) technique is the most popular power-management technique for reducing power loss of SoC applications. Hence, the design consideration for dc–dc converters with good transient performance is necessary to provide good dynamic performance and simultaneously ensure the regulator's stability. In other words, several techniques are demanded for improving transient response time and voltage ripples in order to ensure low supply voltage ripple and maintain a reliable supply voltage to SoC applications.

For low-voltage designs in SoC applications, the signal level is decreased with the same noise level in high-voltage systems. The SNR is significantly reduced. It is obvious that the operating range and the SNR of 0.35-μm process are larger than those of 0.18 μm, which are shown in Fig. 1(a) and (b). Thus, it is imperative to keep a stable and continuous power to the SoC applications in order to react to fast load variations. However, due to the low-voltage and low-power operation in SoC applications, it is very difficult to rapidly recover supply voltage in case of load variations. Besides, the large output ripples in case of load variations may cause the malfunctions of the SoC applications, i.e., the value of SNR is worse than that of the system with ideal power supply. Fig. 1(c) shows the dilemma that we meet in the design of low-voltage SoC applications. The actual operating range is further reduced due to the nonideal power-supply voltage. Most importantly, the long response time in case of large load variations may continuously increase the noise to the SoC applications and reduce the SNR value.

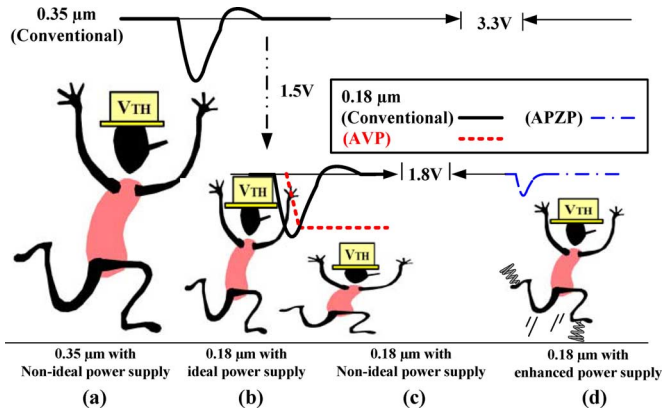

Fig. 1. Operating ranges of the SoC applications with different power-supply transient techniques by different process techniques [1].

There are several on-chip and fast transient techniques that have been published for improving the transient response time. The most popular literature in today's fast transient technique is to speed up the charging or discharging time of the large compensation capacitor [2]–[4]. Thus, large driving current is sourcing or sinking into the compensation capacitor when load current changes. However, a careful design consideration of the system stability is needed to ensure the stable operation. Another famous literature is the prediction technique that has two representative methods. One is the adaptive voltage position (AVP) technique [5], which improves the dynamic performance like transient response time and dropout voltage at the sacrifice of static performance like load regulation. The other is endpoint prediction (EPP) technique [6], which is proposed to speed up the reference tracking time.

The transient performance is enhanced in [7] by a deliberately controlling low-frequency gain to stabilize the system in case of load current variations. The response time is decreased by raising the loop gain higher than that of steady state for getting higher bandwidth. Thus, the unstable response increases the

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transient voltage variations for fast recovery of output voltage. Once the output voltage returns to its original level, the adaptive gain control technique decreases the loop gain to ensure the output voltage returns to its steady-state value. However, the comparators need large biasing current to respond to such a fast transient response. Thus, it is not suitable for portable devices, which need low-quiescent current operation.

Considering a famous off-chip fast transient technique and the skill of fast-response double-buck converters (FRDB) [8], an auxiliary converter is utilized to reduce the recovery time of the output voltage. Besides, this technique also increases the driving ability of the dc–dc converters by using the nonlinear controlling technique in case of large voltage variation at the output. The advantage of this off-chip technique is that the fast transient performance is achieved by the large current injected from the auxiliary converter and the fast response of the nonlinear control. However, it must need an extra external inductor to get such a large current supplement. Once the output voltage is above or below the predefined threshold voltages, the auxiliary converter and nonlinear control are started to react to large load variations. As we know, it still suffers from the oscillation problem because of the nonsmooth transition between the fast transient mode and the normal operation mode.

According to the analysis of the on-chip and off-chip fast transient techniques, we can summarize that the fast transient technique must contain three important characteristics: the promises of the system stability, small overshoot/undershoot output voltage, and good load regulation. Thus, the object of our proposed adaptive pole-zero position (APZP) technique is to provide these three fast transient characteristics at the same time in order to get a regulated power supply to the low-voltage SoC applications, as shown in Fig. 1(d). In other words, we can extend the operating range and the value of SNR for the SoC applications.

In this paper, an on-chip APZP technique is proposed for enhancing the transient performance of a continuous-conduction-mode (CCM) dc–dc converter. The operation theorem is proposed in Section II. The implementation of the APZP circuit is presented in Section III. Timing analysis of the two-step positive feedback control is presented in Section IV. The chip is fabricated by a UMC 0.18-μm process, and experimental results are shown in Section V. Finally, we present the conclusion in Section VI.

II. Analysis of the Proposed DC–DC Converter With APZP Technique

The control-to-output transfer function of the conventional current-mode buck dc–dc converter has two separated real poles, as shown in Fig. 2 [9]–[11]. The dominant pole is located at the output of the regulator $V_{\rm out}$, i.e., $P_1 = 1/(C_L R_{\rm load}) \propto I_{\rm load}$. C_L is the output filter capacitor and $R_{\rm load} \propto 1/I_{\rm load}$. It is heavily dependent on load current. The other pole is located near the switching frequency because of the current-programmed controller design. It means that the compensator is needed to increase the low-frequency loop gain by using the simple and effective proportional-integral (PI) compensation for improving the regulating performance. Furthermore, the bandwidth

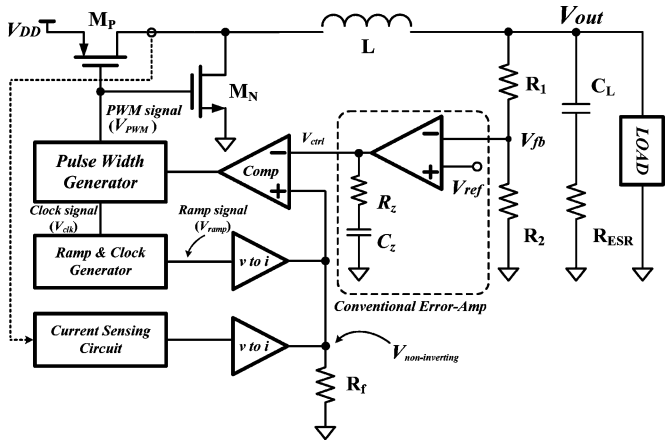


Fig. 2. DC-DC buck converter with conventional error-amplifier and compensator.

can be extended by pole-zero cancellation technique to decrease the transient response time. The PI compensation technique is preferable compared to the dominant pole compensation technique because it enhances the closed-loop gain and bandwidth.

The compensation pole-zero pair (P_c and Z_c) provided by the conventional compensator is composed of the discrete components (R_z and C_z), shown in Fig. 2. Due to the large passive value, extra external pins are needed to connect the external components at the output of the error amplifier. It increases the cost of discrete components, printed board circuit (PCB) layout, and IC packages. The error amplifier with on-chip compensation and fast transient technique successfully improves the transient response and eliminates the large off-chip compensation components at the same time in literature [3].

The transfer function of an equivalent PI compensation technique proposed in [3] is given as

$$T(s) \approx -g_m R_o \frac{1 + sKC_{z1}R_{z1}}{1 + sKC_{z1}(R_{z1} + R_o)} \tag{1}$$

where R_{z1} and C_{z1} are the on-chip small compensation resistor and capacitor, respectively. R_o is the output resistance of the operational transconductance amplifier (OTA) and its value is much larger than that of R_{z1}, g_m is the transconductance of the OTA, and the value of K is defined as the factor to amplify the small value of an on-chip capacitor to be equivalent to that of an external off-chip capacitor with a large value.

The low-frequency zero generated by R_{z1} and C_{z1} is higher than the low-frequency pole generated by $(R_{z1} + R_o)$ and C_{z1} because R_o is larger than R_z. Generally speaking, an equivalent low-frequency pole-zero pair that is similar to that generated by C_z and R_z in Fig. 2 can effectively compensate the current-mode buck dc–dc converter. The advantage of the current-mode Miller capacitance is that the current can be redirected to charge or discharge the small on-chip capacitor C_{z1} in case of large load current variations. Thus, it achieves on-chip compensation and a fast transient mechanism at the same time.

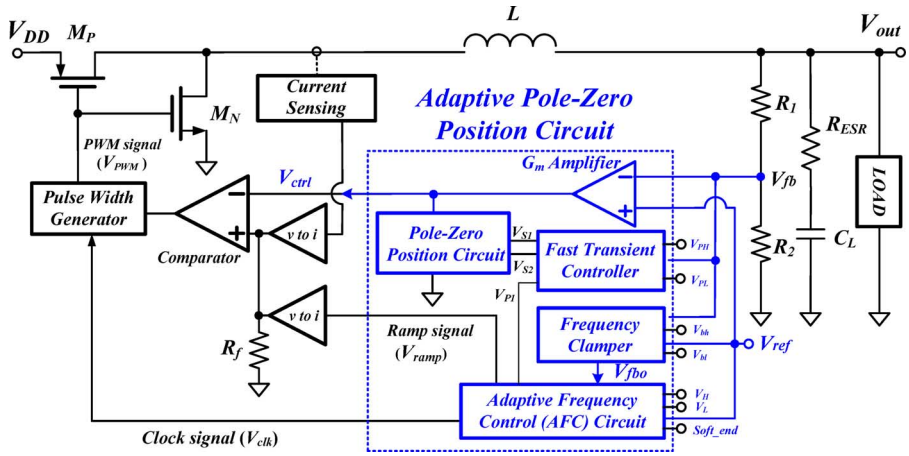


Fig. 3. Architecture of the proposed dc–dc buck converter with the APZP technique.

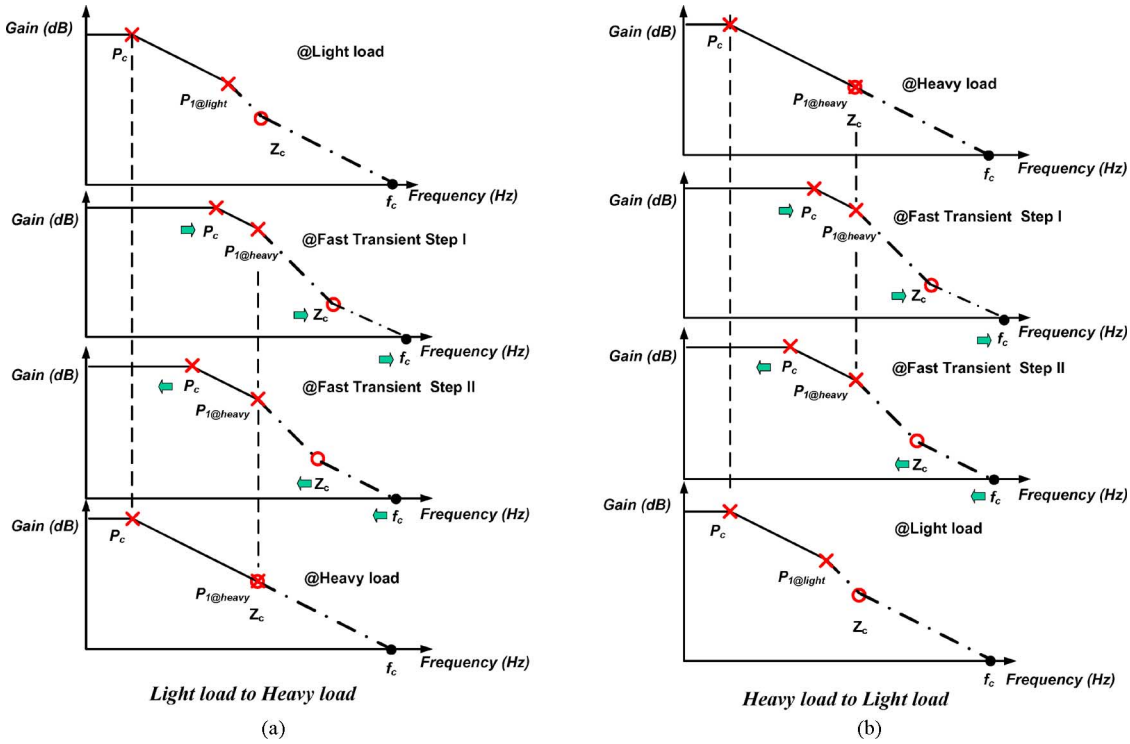


Fig. 4. Frequency response of the APZP circuit. (a) Load current changes from light to heavy. (b) Load current changes from heavy to light.

The implementation of the on-chip compensation with a fast transient mechanism still suffers from the oscillation problem like other positive-feedback techniques. We can carefully control the amount of redirecting current to fast charge or discharge the small on-chip capacitor by a digital trimming method. Therefore, in order to prohibit the system from being unstable because of large positive-feedback current, we propose an APZP technique in Fig. 3 that combines linear and nonlinear controls to effectively eliminate the possibility of unstable scenario. The linear control is implemented by an adaptive frequency control (AFC) technique [12], which consists of AFC circuit and frequency clamper. Nonlinear control is implemented by two-step positive-feedback control that is composed of a transconductance amplifier with an auxiliary gain stage, fast transient controller, and pole-zero position circuit. The following subsections will describe the advantages of these two techniques.

A. Concept of Two-Step Positive Feedback for Improving Transient Response Time and Reducing the Unstable Possibility

The frequency response of the APZP circuit is illustrated in Fig. 4 in case of load variations. In Fig. 4(a), the load-dependent

pole P_1 is moved from $P_{1@\mathrm{light}}$ to $P_{1@\mathrm{heavy}}$ when the load current changes from light to heavy. $P_{1@\mathrm{light}}$ and $P_{1@\mathrm{heavy}}$ are defined as the output pole at light and heavy loads, respectively. At the beginning of the load variation, the pole-zero pair (P_c, Z_c) is moved far away from the origin due to the positive-feedback control of the fast transient step I [3]. It is obvious that the crossover frequency is also moved to a higher frequency, and the transient response is enhanced. The slew-rate problem is also solved by the redirecting compensation current. However, the system is unstable because the phase margin is deteriorated by the two poles $P_{1@\mathrm{heavy}}$ and P_c. It suffers from the oscillation problem of the redirecting current not being removed before the output voltage comes back to its the regulated value. Thus, the operation of two-step positive feedback is adapted to improve the system stability. The operation of fast transient step II starts to pull back the pole-zero pair (P_c, Z_c) toward the origin, and thus, the crossover frequency is decreased. The stability of the system is again ensured.

The operation of the two-step positive-feedback circuit moves the pole-zero pair to a higher frequency similar to that of the previous design [3]. After a short time of large redirecting current charging or discharging the small compensation capacitor, the operation of two-step positive feedback turns off part of the redirecting current in order to move the pole-zero pair (P_c, Z_c) back to its original position for stabilizing the system. Therefore, the phase margin of the fast transient step II is larger than that of the fast transient step I. The phase margin is still not enough to ensure that the system has a smooth and fast response, i.e., the pole-zero pair (P_c, Z_c) is pulled back to its original position at the end of the operation of fast transient II. In other words, the position of the pole-zero pair (P_c, Z_c) is not changed at steady state.

Similarly, the analysis that load current changes from heavy to light is depicted in Fig. 4(b). It also demonstrates that the pole-zero pair is rapidly moved to a higher frequency at the beginning of the fast transient step I in order to get a higher crossover frequency. After the operation of fast transient step I, the phase margin is increased due to the operation of the fast transient step II. Finally, the compensation pole-zero pair is moved back to its original value at steady state.

In order not to amplify the switching ripples, the design of the crossover frequency of the system is usually smaller than 20% of the switching frequency (f_s). Since the operation of the two-step fast transient mechanism moves the crossover frequency to a higher frequency, the output switching ripple at the load transient condition is larger than that of at steady state. Thus, how to alleviate the possibility of increase of the output ripples is an important issue. The proposed AFC technique not only alleviates the limitation of the switching frequency smaller than 20%, but also enhances the slew rate by varying the switching frequency to speed up the charging/discharging time of the output capacitor.

B. Concept of AFC Technique for Reducing the Output Ripples

The AFC technique is the operation control technique that adaptively and smoothly adjusts the switching frequency by dynamically varying the switching frequency. During the load transient period, switching frequency will step up (step down) to increase (decrease) the duty cycle according to the quantity of the error voltage (ΔV) between the reference voltage V_{ref} and the scaled voltage V_{fb} when $V_{\mathrm{fb}} < V_{\mathrm{ref}}$ in case of load current variation from light to heavy ($V_{\mathrm{fb}} > V_{\mathrm{ref}}$ in case of load current variation from heavy to light).

As illustrated in Fig. 4, at the beginning of the fast transient step I, the compensation pole-zero pair is moved far away from the origin. The implementation of the adaptive frequency controller can effectively increase the value of the switching frequency, i.e., the movement of the compensation pole-zero pair causes the increase of the crossover frequency. The switching ripples may be amplified due to the increase of the crossover frequency. However, the value is not large enough to affect the performance of the system, due to the increase of the switching frequency.

Besides, the modification of the switching frequency depends on the load variations, and has the ability to rapidly charge or discharge the compensation capacitor. Thus, the AFC technique is in response to reduce the overshoots or undershoots of output voltage instantly, and creates an adaptive adjustment of the duty cycle at the output of the comparator by comparing the output voltage V_{ctrl} of the error amplifier and the voltage at the resistor R_f, as shown in Fig. 3.

The waveforms of ramp signal generated by the AFC technique are depicted in Fig. 5(a) when load current changes from heavy to light. Due to the width of ON-times stands for turn-on time of power p-type MOSFET, the increasing rise time and decreasing fall time of ramp signal make the ON-time of power p-type MOSFET smaller than that of conventional design. The following equation demonstrates that less energy is transferred to output node in every switching period:

$$D_1 = \frac{T_{\mathrm{clk}} + T_a}{T_{\mathrm{clk}} + T_{\mathrm{ramp}}} = \frac{T_{\mathrm{clk}}/T_{\mathrm{ramp}} + T_a/T_{\mathrm{ramp}}}{T_{\mathrm{clk}}/T_{\mathrm{ramp}}+1}$$
$$= \frac{T_{\mathrm{clk}}T'_{\mathrm{ramp}}/T_{\mathrm{ramp}} + T'_a}{T_{\mathrm{clk}}T'_{\mathrm{ramp}}/T_{\mathrm{ramp}} + T'_{\mathrm{ramp}}} > \frac{T'_{\mathrm{clk}} + T'_a}{T'_{\mathrm{clk}} + T'_{\mathrm{ramp}}} = D'_1$$

where

$$\frac{T_{a1}}{T_{\mathrm{ramp1}}} = \frac{T'_{a1}}{T'_{\mathrm{ramp1}}} \quad \text{and} \quad T_{\mathrm{clk1}}\frac{T'_{\mathrm{ramp1}}}{T_{\mathrm{ramp1}}} > T'_{\mathrm{clk1}}. \qquad (2)$$

On the contrary, the decreasing rise time and increasing fall time of the ramp signal make the ON-time of power p-type MOSFET larger than that of conventional design, as shown in Fig. 5(b). Similar to (2), it is easy to prove that more energy is transferred to output node in every switching period.

Based on the foregoing description, the AFC technique can use the error voltage between V_{fb} and V_{ref} to control rise time and fall time of the ramp signal for automatically and rapidly determining the switching frequency.

C. Operation Mode of APZP Technique

The load-dependent crossover frequency (f_c) decides the operation of the fast transient mechanism [13]. In Fig. 6, the

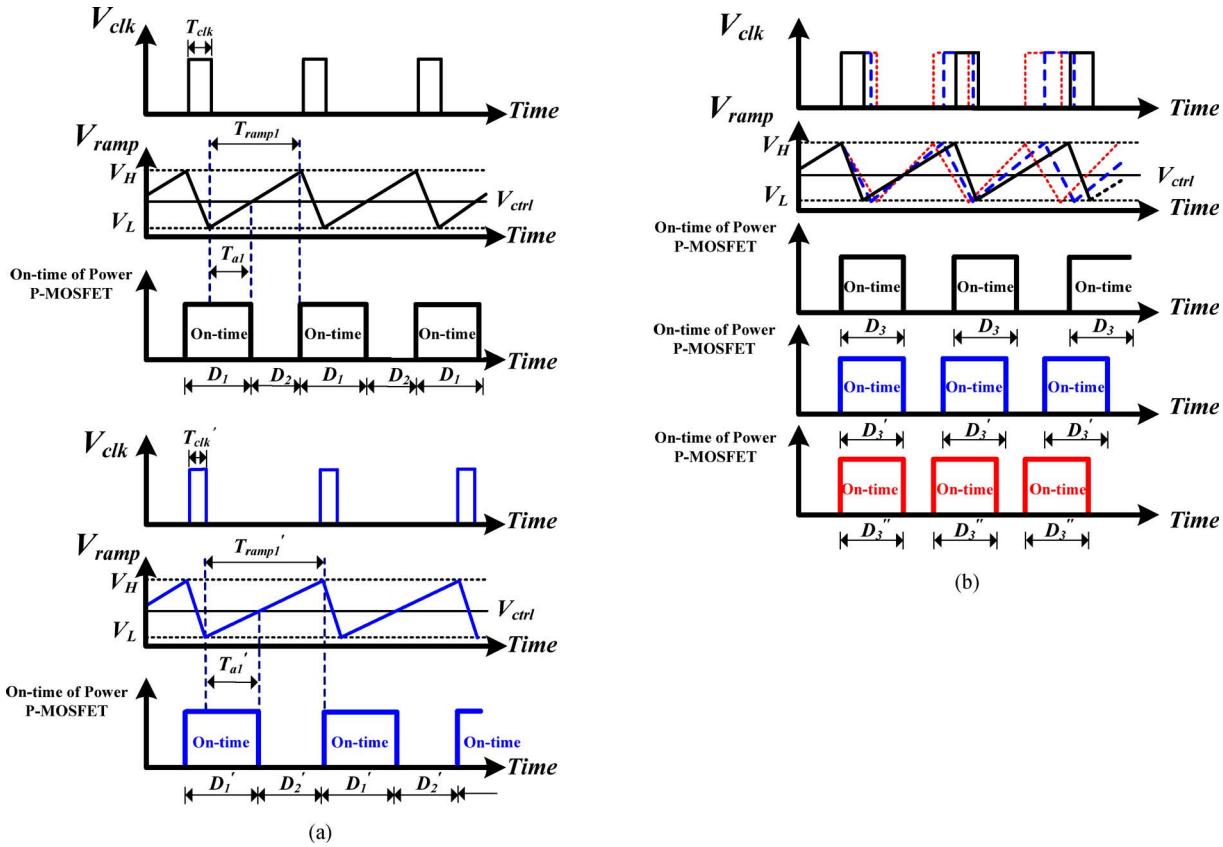
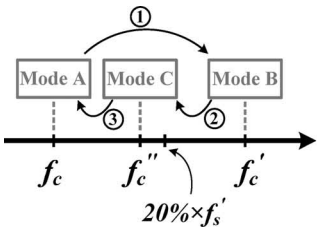


Fig. 5. Timing diagrams of the operation of AFC technique for automatically and smoothly adjusting switching frequency. (a) Load current changes from heavy to light. (b) Load current changes from light to heavy.



Mode A (f_c)	AFC
Mode B ($f_c^{'}$)	AFC+two redirecting current
Mode C ($f_c^{''}$)	AFC+one redirecting current

Fig. 6. Crossover frequency of the APZP technique when load current changes from light to heavy ($f_c' > 20\% \times f_s' > f_c'' > f_c$).

crossover frequency is moved away from the original frequency at the beginning of transient variations. At this time, the operation mode is changed from mode A to mode B. The two-step positive-feedback control and AFC techniques are used to immediately recover the output voltage level. After a period of time, the operation mode is changed from mode B to mode C to prevent the system from ringing by disabling one part of the positive-feedback mechanisms. Operation mode goes back to mode A when output voltage V_{out} stops dropping and trends back to the regulated value; then the control mechanism is fully determined by the AFC technique. The advantage of the APZP technique is that it can smoothly and effectively regulate the output voltage level when load current changes.

In other words, the proposed APZP technique provides three fast transient modes in order to get a regulated power supply to the low-voltage SoC applications. These three important fast transient modes are the promises of the system stability, small overshoot/undershoot output voltage, and the good load regulation.

III. Design of the Proposed Circuits

A. Two-Step Positive-Feedback Control Circuit

The two-step positive-feedback control circuit is composed of a transconductance amplifier with an auxiliary gain stage [14], fast transient controller, and pole-zero position circuit, as shown in Fig. 7. There are two operation modes in this circuit. At

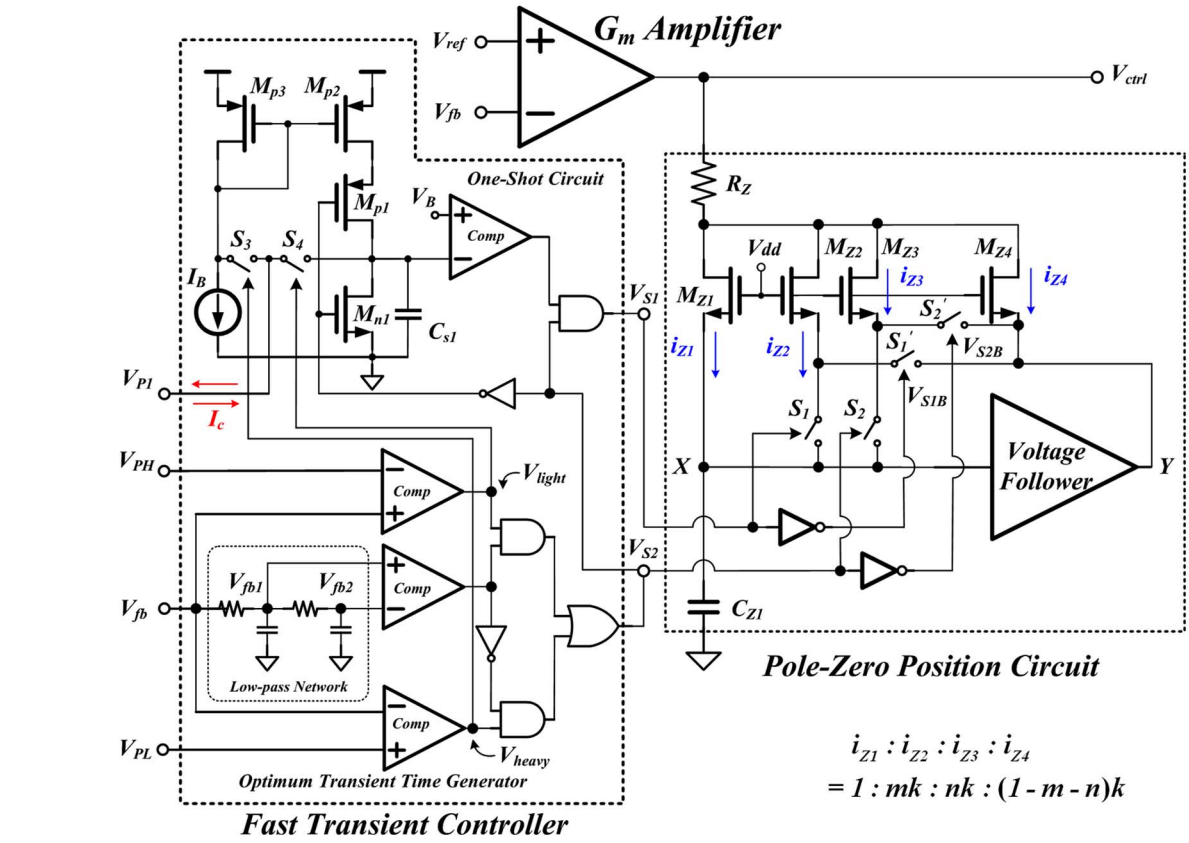
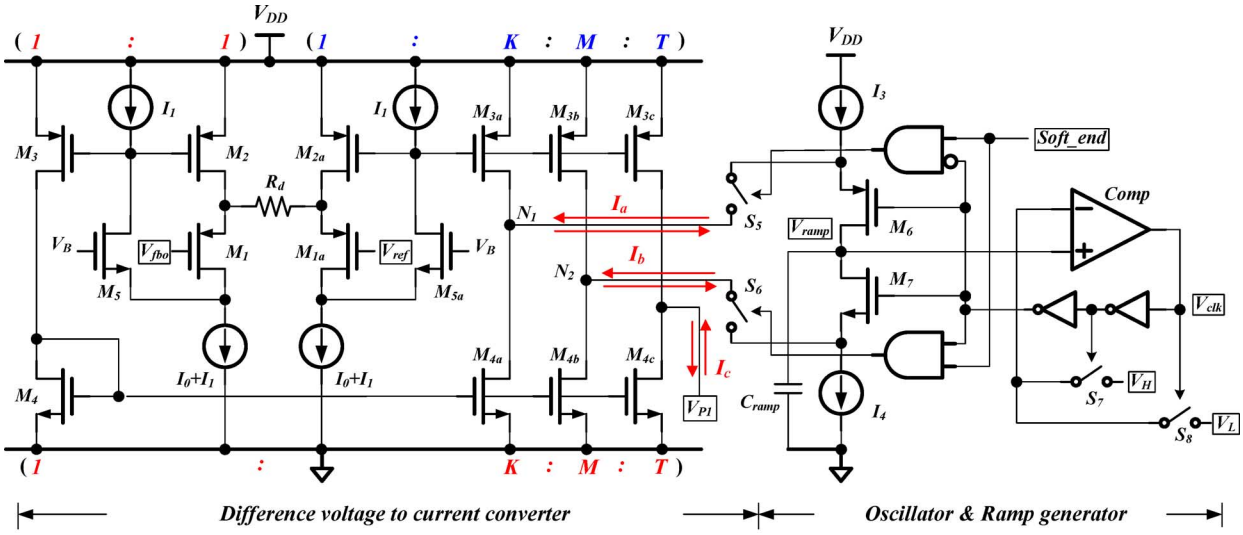


Fig. 7. Two-step positive-feedback control circuit. (a) Architecture of two-step positive feedback control. (b) Schematic of error amplifier. (c) Schematic of the voltage follower.

normal operation, the signals V_{S1}, V_{S2}, V_{S1B}, and V_{S2B} that are generated by the fast transient controller set the switches S_1 and S_2 OFF and S_1' and S_2' ON. Besides, the aspect ratios of transistors M_{Z2}, M_{Z3}, and M_{Z4} are, respectively, set mk, nk, and $(1-m-n)k$ times that of transistor M_{Z1}. Hence, the ratio $(i_{z1} : i_{z2} : i_{z3} : i_{z4})$ of the four different currents is $(1 : mk : nk : (1-m-n)k)$. Once a large load variation occurs, the output capacitor of the error amplifier needs to be charged or discharged as quickly as possible. Thus, the fast transient mechanism is started by setting switches S_1 and S_2 ON and switches S_1' and S_2' OFF.

The redirecting current is partitioned into two current branches. One current branch composed of I_{z2} and I_{z3} is utilized to charge or discharge the small capacitor C_{z1} for speeding up the transient response time. The other current branch I_{z4} is still utilized to compensate the dc–dc converters. Thus,



(a)

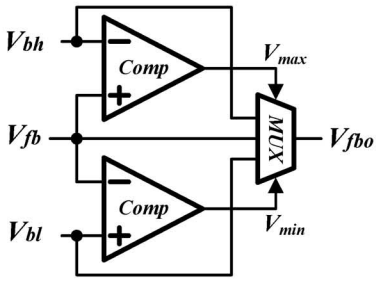


Table		
V_{max}	V_{min}	V_{fbo}
0	0	V_{fb}
1	0	V_{bh}
0	1	V_{bl}

(b)

Fig. 8. AFC circuit. (a) Schematic of proposed AFC circuit for automatically and smoothly adjusting the switching frequency of dc–dc converters. (b) Frequency clamper circuit in Fig. 3 to prevent the switching dc–dc converters from having too fast or slow switching frequencies and eliminates the sub-harmonic oscillation.

the slew rate of the error amplifier can be increased. As we know, if the compensation circuit is implemented by a voltage-mode Miller capacitor, the compensation circuit has no extra current to speed up the transient time for output voltage of the error amplifier. It is why we use a current-mode Miller capacitor to speed up, and compensate current-mode buck dc–dc converters.

The other operation mode is the fast operation that is dependent on the fast transient controllers, as shown in Fig. 7(a). Fig. 7(b) and (c) shows the schematics of the error amplifier and the voltage follower. The transistors M_{B1}–M_{B9} constitute a standard bias circuit for a cascode operational transconductance amplifier, which is a high-gain single-stage amplifier with one dominant pole [15]. For the voltage follower M_{V1}–M_{V14}, due to the symmetry of voltage follower [16], [17], the input voltage level (the gate of M_{V1}) is equal to the output node (the gate of M_{V2}).

This fast transient controller is composed of an optimum transient-time generator with low-pass network and a one-shot circuit. The optimum transient-time generator is used to generate the signal V_{S2} for controlling the equivalent current of transistor M_{Z3}. Similarly, the signal V_{S1} is generated to control the equivalent current of transistor M_{Z2} by a one-shot circuit. Node V_{P1} is connected to the AFC circuit, as shown in Fig. 8(a), in order to regulate the first step positive-feedback time of signal V_{S1} by a correction current I_c. Once a large load variation occurs, output voltage $V_{\rm out}$ will be dropped down or pulled high. In order to detect this instant variation, we use two comparators to compare the scaled voltage $V_{\rm fb}$ with the high $V_{\rm PH}$ and low $V_{\rm PL}$ threshold voltages for enabling the APZP circuit into fast operation mode. In a design aspect, we should increase the redirecting current as large as possible to charge or discharge the output capacitor of error amplifier for enhancing the transient response time and reducing the overshoot/undershoot voltage. However, large current may cause the oscillation scenario. Thus, a two-step positive-feedback mechanism is utilized to ensure the stable operation and achieve fast transient response.

B. AFC Circuit With Frequency Clamper

The oscillator and ramp generator, as shown in Fig. 8(a), are used to generate the clock ($V_{\rm clk}$) and ramp ($V_{\rm ramp}$) signals as periodically initial signal and the slope compensation

signal in the current-mode converter, respectively. In normal operation with a constant frequency, the bias currents I_3 and I_4 are used as the charging and discharging currents, respectively for capacitor $C_{\rm ramp}$. Besides, the current I_4 is much larger than the current I_3. As we know, two limitation voltages V_H and V_L are needed to define the upper and lower bounds of sawtooth.

I_a and I_b are converted from the error voltage ($V_{\rm fbo}$–$V_{\rm ref}$) by the difference voltage to current circuit [17]. These two current sources can determine the increase/decrease of the rising/falling time of a ramp signal, which is illustrated in Fig. 5. Two flipped voltage followers composed of $(M_1, M_2,$ and $M_5)$ and $(M_{1a}, M_{2a},$ and $M_{5a})$ have small output impedances to improve the linearity of level shifters. A resistor R_d is connected between the outputs of the two flipped voltage followers. Therefore, the transconductance of the difference voltage to current circuit is about $1/R_d$ because of high linearity. By using five current mirror pairs, which are (M_2, M_3), (M_{2a}, M_{3a}), (M_{2a}, M_{3b}), (M_4, M_{4a}), and (M_4, M_{4b}), the values of current I_a and I_b are determined by the following equations:

$$I_a = 2K\frac{V_{\rm ref} - V_{\rm fb}}{R_d} \qquad \text{and} \qquad I_b = 2M\frac{V_{\rm ref} - V_{\rm fb}}{R_d}. \quad (3)$$

The values of current I_a and I_b are used to automatically and smoothly revise the rising and falling slopes of the ramp signal, respectively. In other words, they decide the values of slope of ramp signal and the width of clock signal, respectively. Once the soft start is finished and signal *Soft_end* is set to "1," switches S_5 and S_6 are synchronized with transistors M_6 and M_7 to adjust the values of current flowing through transistors M_6 and M_7. For instance, once the load current rapidly changes from light to heavy, the duty cycle cannot be adjusted immediately due to the slew rate of the error amplifier. The output capacitor C_L supplies the insufficient charge between load current and input supplying source, and then, causes a dropout voltage at the output node. Thus, the difference in voltage and current circuit converts the error voltage to a revised current that increases the charge current of $I(M_6)$ and gets a steep ramp signal. Besides, the discharge current of $I(M_7)$ is decreased to get a wide clock pulse signal. As illustrated in Fig. 5(b), these actions indeed increase duty cycle and reduce the transient dropout voltage at the output node. When the output voltage is regulated back to the expected voltage, i.e., ΔV is small, the revised currents become trickle currents and are not large enough to affect the switching frequency. Finally, frequency is constant again during steady state.

The AFC technique can automatically and smoothly adjust the frequency according to the error voltage (ΔV). In order to avoid too fast or slow switching frequencies, we define the maximum and minimum switching frequencies by clamping the feedback voltage $V_{\rm fb}$ between lower voltage $V_{\rm bl}$ and upper voltage $V_{\rm bh}$, which is shown in Fig. 8(b). Thus, the switching frequency is limited between $f_{\max}$ and $f_{\min}$ defined by the frequency clamper circuit. If $V_{\rm fb} > V_{\rm bh}$, we set $V_{\rm fbo} = V_{\rm bh}$. If $V_{\rm fb} < V_{\rm bl}$, we set $V_{\rm fbo} = V_{\rm bl}$. Equations (4) and (5) determine $f_{\max}$ and $f_{\min}$

$$f_{\max} = \left(\frac{C_{\rm ramp}(V_H - V_L)}{I_3 + 2K(V_{\rm ref} - V_{\rm bl})/R_d} + \frac{C_{\rm ramp}(V_H - V_L)}{I_4 - 2M(V_{\rm ref} - V_{\rm bl})/R_d}\right)^{-1} \quad (4)$$

$$f_{\min} = \left(\frac{C_{\rm ramp}(V_H - V_L)}{I_3 - 2K(V_{\rm bh} - V_{\rm ref})/R_d} + \frac{C_{\rm ramp}(V_H - V_L)}{I_4 + 2M(V_{\rm bh} - V_{\rm ref})/R_d}\right)^{-1} \quad (5)$$

where M and K are the current mirror ratios (M_{3a}, M_{2a}) and (M_{3b}, M_{2a}), respectively, in Fig. 8(a).

Importantly, the value of $f_{\min}$ must ensure the slope of ramp signal larger than the half of the slope of inductor current m_2, i.e., turn-on period of power n-type MOSFET, to avoid subharmonic oscillation.

C. Correction Factor Provided by AFC Circuit for Reducing the Oscillation Possibility

The AFC circuit can easily convert the voltage difference between the reference voltage ($V_{\rm ref}$) and the feedback voltage ($V_{\rm fb}$) to a current I_c, which is shown in Fig. 8(a). The correction faction I_c can be determined as

$$I_c = 2T\frac{V_{\rm ref} - V_{\rm fb}}{R_d} \quad (6)$$

where T is the current mirror ratio (M_{3c}, M_{2a}).

In order to solve the oscillation problem, occuring in small output variation because of excess first step positive-feedback current charging/discharging the compensation capacitor C_{z1}, the duration of the first step positive-feedback time should be set to a minimum value according to the lower bound of the output voltage variation. Contrarily, because large output voltage variation needs large current charging/discharging of the compensation capacitor, the first step positive-feedback time needs to be increased. As Fig. 7(a) shows, we use the correction factor I_c to increase the time duration of the first step positive feedback when large output undershoot (overshoot) voltage variation happens and signal $V_{\rm heavy}$ ($V_{\rm light}$) turns on the switch S_3 (S_4). The larger voltage variation leads to the longer the duration of the first step positive-feedback time. Thus, the oscillation possibility can be alleviated by fine-tuning the time duration of the first step positive-feedback control. Experimental results demonstrate that the duration of the first step positive-feedback time is directly proportional to the output voltage variation, and the oscillation problem is fully solved by the correction factor function provided by the AFC circuit.

IV. Timing Analysis of Two-Step Positive-Feedback Control

The timing analysis of the two-step positive-feedback control is shown in Fig. 9 when load current increases/decreases suddenly. In Fig. 9(a), the current $I_{\rm converter}$ increases with a slow slope $dI_{\rm CB}/dt$ in normal operation from t_1 to t_2. Once the scaled voltage $V_{\rm fb}$ is lower than $V_{\rm PL}$, the fast transient controller triggers the signals V_{S1} and V_{S2} from "0" to "1," and

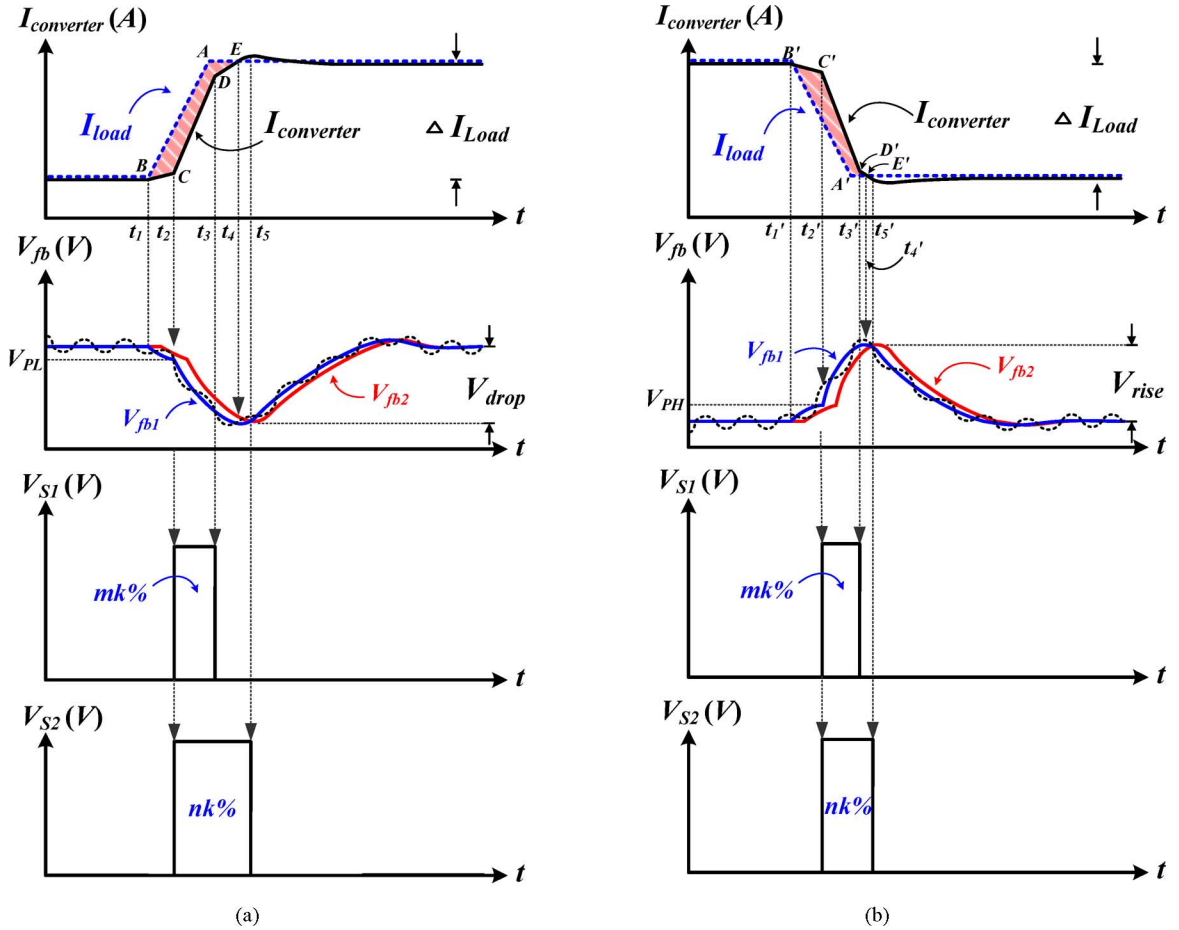


Fig. 9. Timing analysis of signal waveforms. (a) With a positive and sudden load current variation. ($dI_{\rm dc}/dt > dI_{\rm ED}/dt > dI_{\rm CB}/dt$) (b) With a negative and sudden load current variation.

turns the switches S_1 and S_2 ON. In fast operation mode, the equivalent current has a two-step value based on the aspect ratio of M_{Z2} and M_{Z3}, which are set mk and nk times that of M_{Z1}, respectively ($m > n$). Thus, the first step equivalent current that is $(m + n)k$ times the current flow though C_{z1} can be utilized to reduce the transient response time.

After time t_3, the equivalent current switches to second-step value, which is only nk times that flowing though C_{z1}, to avoid the oscillation scenario. The optimum endpoint of the second-step equivalent current is determined when the value of $I_{\rm converter}$ is slightly larger than that of the load current [3]. It is because the energy is sufficient to supply the load and $V_{\rm out}$ stops dropping. Based on the low-pass network of the fast transient controller, the optimum endpoint can be decided automatically, i.e., the cross-point between signals $V_{\rm fb1}$ and $V_{\rm fb2}$, as shown in Fig. 7(a), no matter what the load current is. In case of Fig. 9(a), the optimum endpoint is at t_5. By the fast transient controller with low-pass network, the duty of switching signal can be rapidly and accurately increased [9]. Additionally, Fig. 9(b) is the case of large negative load for fast transient operation.

As illustrated in Fig. 10, the transconductance of the transconductance amplifier with an auxiliary gain stage in Fig. 7(b) for the on-chip capacitor C_{z1}, $g_{m,n}$, is derived as the following equation when the tail current of the error amplifier is I_D and

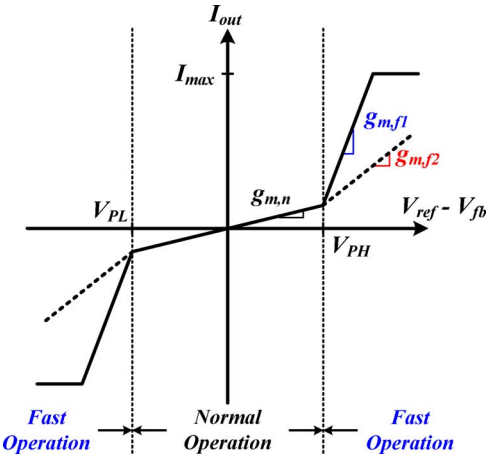


Fig. 10. Transconductance of the transconductance amplifier with an auxiliary gain stage with an on-chip capacitor C_{z1}.

APZP operates in normal operation (mode A):

$$g_{m,n} = \sqrt{2\mu_p C_{\rm ox}\left(\frac{W}{L}\right)_{Me1,2} I_D} \times \frac{(W/L)_{Me14}}{(k+1)\,(W/L)_{Me5}}$$

TABLE I
SPECIFICATIONS OF BUCK CONVERTER

Technology	*UMC 0.18-μm process*
Input Voltage	*1.8 V*
Output Voltage	*1.0 V*
Switching frequency	*~1 MHz*
Output Current Range	*< 500 mA*
Output Ripple Voltage	*< 10 mV*
Output recovery time	*< 10 μs*

TABLE II
COMPONENT VALUES AND REFERENCE VOLTAGES

L	*4.7 μH*	R_1	*200 kΩ*
C_L	*10 μF*	R_2	*200 kΩ*
R_{ESR}	*30 mΩ*	R_{z1}	*100 kΩ*
V_{ref}	*0.5 V*	C_{z1}	*2 pF*
R_{sense}	*400 Ω*	K	*100*
R_s	*50 kΩ*	M	*0.5*
R_f	*95 kΩ*	N	*0.15*

where μ_p is the mobility, $C_{\rm ox}$ is the oxide capacitance per unit area, and $(W/L)_{\rm Mex}$ is the aspect ratio of MOS transistor $M_{\rm ex}$ in Fig. 7(b). Once APZP operates in mode B and mode C for enhancing fast transient performance, the transconductance of the transconductance amplifier with an auxiliary gain stage for the on-chip capacitor C_{z1} is increased from $g_{m,n}$ to $g_{m,f1}$ and $g_{m,f2}$, respectively. The values ($g_{m,f1}$ and $g_{m,f2}$) are derived as

$$g_{m,f1} = g_{m,n} + g_{m,n} \times (m+n)k = g_{m,n}\left[1 + (m+n)k\right] \tag{7}$$

$$g_{m,f2} = g_{m,n} + g_{m,n} \times nk = g_{m,n}(1+nk). \tag{8}$$

In order to prevent the converter from oscillating and ensure the stability of the system, conservative value of the time duration is used to design first-step pulse to achieve minimum output voltage variation. In our design, the appropriate values of m, n, and k are set to 0.5, 0.15, and 100 for this APZP technique. At the beginning of the fast transient step I, the g_m is increased to $g_{m,f1}$. After the fast transient step I, the value of g_m is decreased to $g_{m,f2}$. Therefore, the system is smoothly stabilized and regulated back to its steady state. In other words, at the stage of fast transient step II, the small value of g_m may slow down the recovery speed to ensure stable operation at this stage. The relationship between the value of g_m and the fast transient controller in Fig. 7(a) is determined by the controlling mechanism of the switches. The fast transient controller in Fig. 7(a) turns on/off the switches S_1 and S_2 to redirect the currents for generating the different value of g_m. The ratio $(i_{z1} : i_{z2} : i_{z3} : i_{z4})$ of the four different currents is $(1 : mk : nk : (1-m-n)k)$.

V. VERIFICATION AND EXPERIMENTAL RESULTS

The proposed current-mode buck dc–dc converter with APZP technique is implemented by the UMC 0.18-μm process. Specifications of the dc–dc converters are listed in Table I. The values of passive components and reference voltages are shown in Table II. The chip micrograph is shown in Fig. 11.

Loop-gain simulation results of the proposed dc–dc converter are shown in Fig. 12. Obviously, the results of the frequency response are similar to those of the foregoing illustration, as shown in Fig. 4. Thus, it demonstrates the stability of the transient process when the load current changes rapidly.

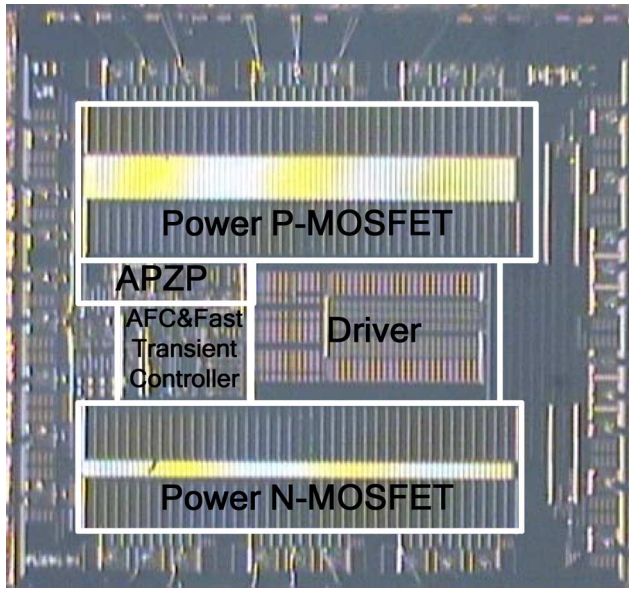


Fig. 11. Chip micrograph of the proposed dc–dc converter.

Besides, the load transient response has been tested to show the good performance of the proposed converter, which is compared with the other case. As shown in Fig. 13, the curves (a)–(c) are the converter with conventional architecture, AFC technique, and positive-feedback technique, respectively. The undershoot voltage and recovery time are quantified and analyzed when the load current changes from 100 to 500 mA within 1 μs, or vice versa. Considering the difference between these three cases, the AFC technique indeed reduces the dropout voltage; however, the recovery time may be extended because of linear control. Additionally, it is obvious that curve (c) shows the best performance in all aspects. But this method is sensitive to the technique process, and the oscillation scenario can be alleviated only by adopting a small redirecting current for charging/discharging the compensation capacitor.

In the proposed dc–dc converter, the waveforms of the inductor current and output voltage are shown in Fig. 14. It is obvious that there is no inrush current happening in the transient response of the inductor current, i.e., the smooth movement of the pole-zero pair controlled by APZP technique. The small overshoot in the inductor current prevents the output voltage from dropping to too low value. Thus, the dropout voltage of the output voltage is less than those of the previous designs. Besides, the transient waveforms are shown in Figs. 15–17 when load current changes

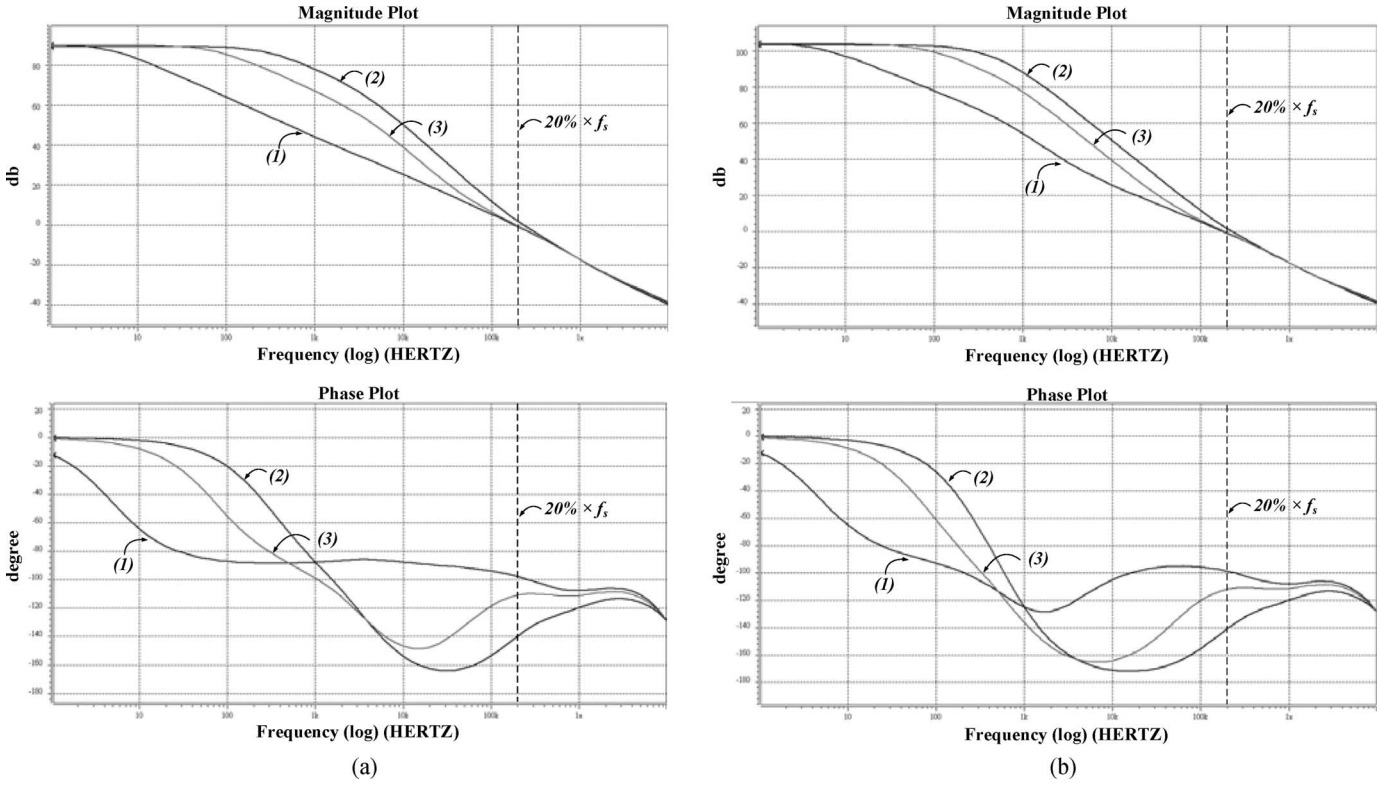


Fig. 12. Loop-gain simulation results of the proposed dc–dc converter. ($V_{\rm DD} = 1.8$ V and $V_{\rm out} = 1$ V). (a) Heavy load current condition ($I_{\rm out} = 500$ mA). (b) Light load current condition ($I_{\rm out} = 100$ mA).

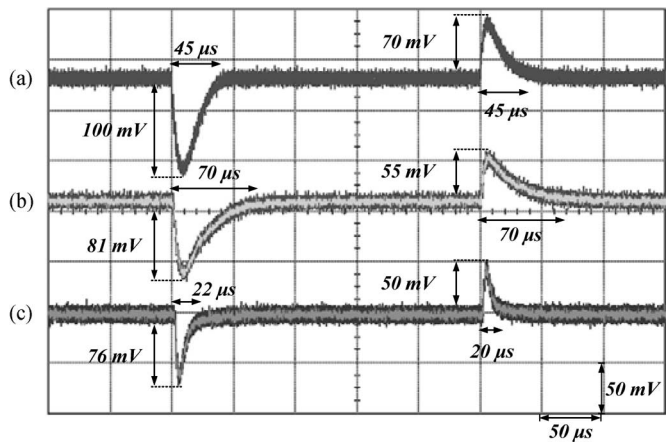


Fig. 13. Output transient waveforms of dc–dc converters with load current step between 100 and 500 mA. (a) Conventional design without fast transient technique. (b) With AFC technique. (c) With positive feedback technique.

from 100 mA to 300 mA, 100 to 400 mA, and 100 to 500 within 1 μs, or vice versa. Moreover, the measured data are listed in Table III. In Fig. 15(a), the transient dropout voltage is about 26 mV and the recovery time is about 8 μs. The enlarged waveforms are shown in Fig. 15(b) and (c). When load current increases from 100 to 300 mA, the switching frequency is increased to 1.05 MHz according to the error voltage. On the contrary, switching frequency is decreased to 800 kHz when load current decreases rapidly. Due to the two-step positive-feedback control scheme and the adaptive switching frequency controlled by the signals V_{S1}, V_{S2}, and $V_{\rm ramp}$, the output voltage smoothly can go back to its regulated voltage level. Thus, the compensation is designed as a value at the heavy load condition. Thus, the bandwidth at the heavy load condition is larger than that at the light load condition. That is why the dropout voltage from the heavy to light load condition is smaller than that of light to heavy. Additionally, experimental results can demonstrate that the first step positive-feedback time is directly proportional to output voltage variation, as shown in Figs. 15–17.

Compared to other techniques, as shown in Fig. 13, the transient undershoot/overshoot voltage and recovery time of the proposed dc–dc converter with the APZP technique do not exceed 48 mV and 10 μs, respectively. Besides, compared with conventional design without any fast transient technique, the performances of overshoot voltage and recovery time are enhanced by 37.2% and 77.8%, as listed in Tables IV and V, respectively. Consequently, from the experiment results, we can find out that the output voltage can be smoothly regulated back to its stable voltage level in case of any load current variation. Fig. 18 shows the measured efficiency, which has a maximum of 85.6% at 280-mA load current. Comparison of current consumption with different controllers is shown in Fig. 19.

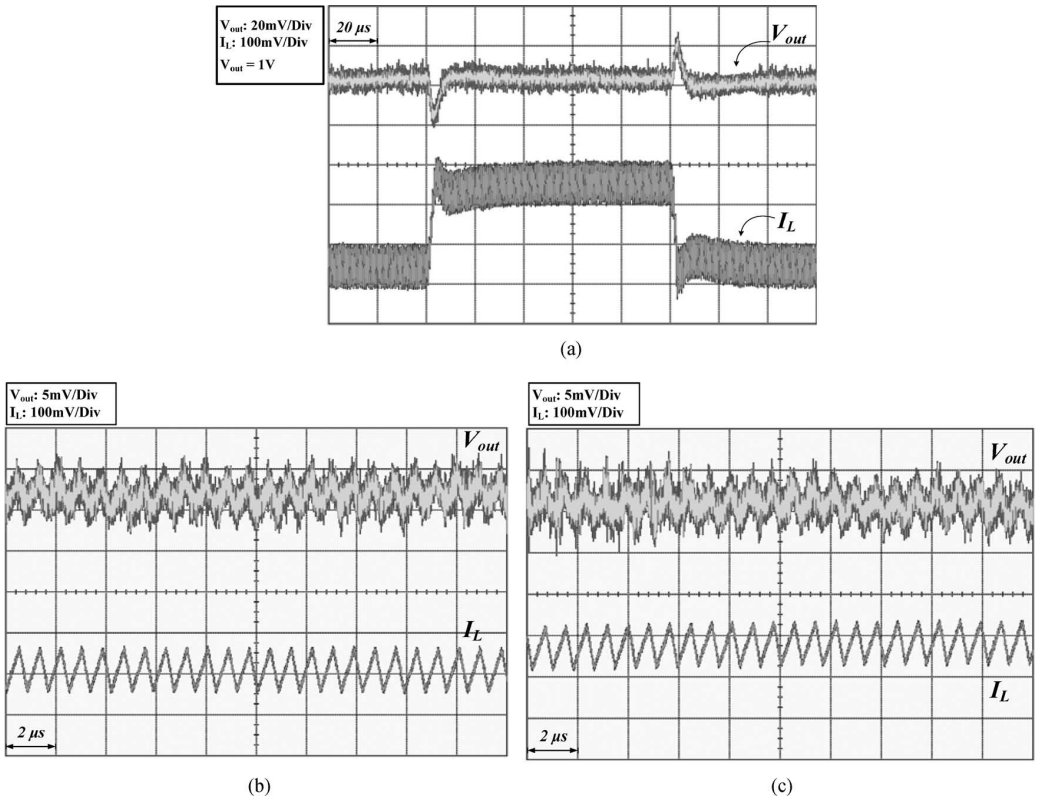


Fig. 14. Waveforms of the proposed dc–dc converter. (a) With load current stepping from 100 to 300 mA, or vice versa. (b) Enlarged waveforms of that load current in 100 mA. (c) Enlarged waveforms of that load current in 300 mA.

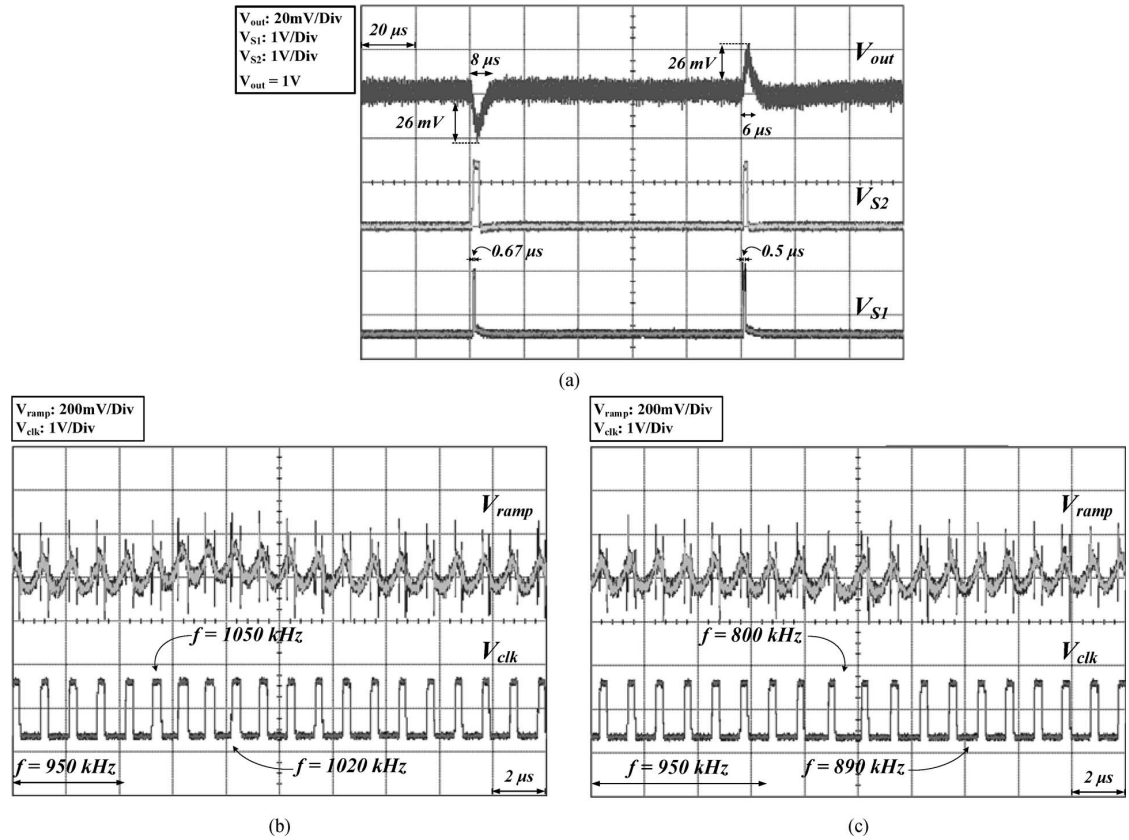


Fig. 15. Transient waveforms of the proposed dc–dc converter. (a) With load current stepping from 100 to 300 mA, or vice versa. (b) Enlarged waveforms of that load current stepping from 100 to 300 mA within 1 μs. (c) Enlarged waveforms of that load current stepping from 300 to 100 mA within 10 μs.

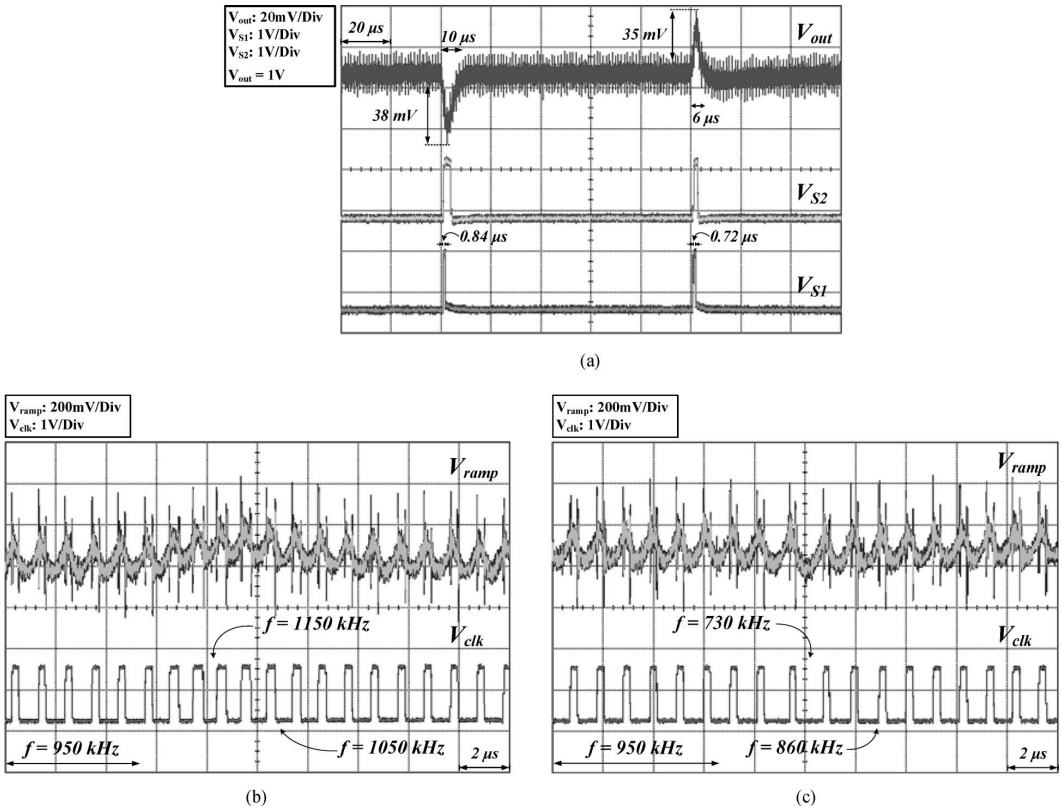


Fig. 16. Transient waveforms of the proposed dc–dc converter. (a) With load current stepping from 100 to 400 mA, or vice versa. (b) Enlarged waveforms of that load current stepping from 100 to 400 mA within 1 μs. (c) Enlarged waveforms of that load current stepping from 400 to 100 mA within 1 μs.

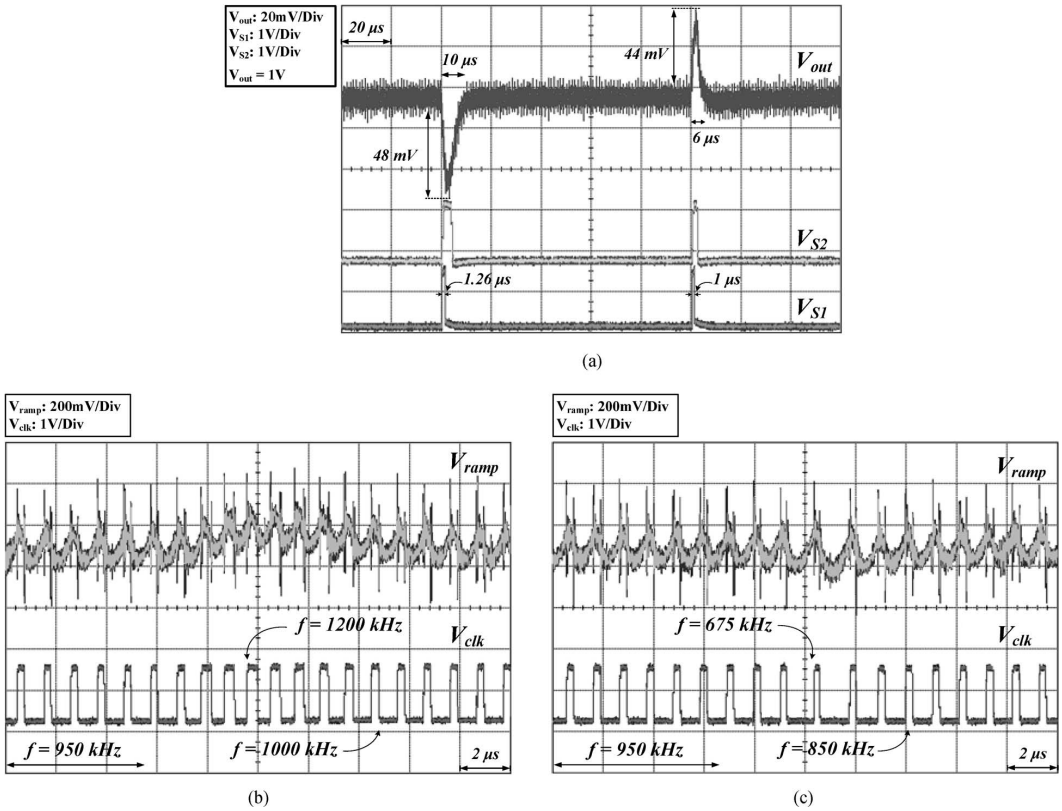


Fig. 17. Transient waveforms of the proposed dc–dc converter. (a) Load current steps from 100 to 500 mA, or vice versa. (b) Enlarged waveforms of that load current stepping from 100 to 500 mA within 1 μs. (c) Enlarged waveforms of that load current stepping from 500 to 100 mA within 1 μs.

TABLE III
COMPARISON WITH OTHER FAST TRANSIENT TECHNIQUE DC–DC CONVERTER

	Load current changes from light to heavy			Load current changes from heavy to light		
	Undershoot voltage (mV)	Recovery time (μs)	Switching Frequency (MHz)	Overshoot voltage (mV)	Recovery time (μs)	Switching Frequency (MHz)
Conventional w/o fast transient (100mA↔500mA)	100	45	~ 1	70	45	~ 1
AFC [12] (100mA↔500mA)	81	70	1 ~ 1.2	55	70	0.7 ~ 1
Positive feedback [3] (100mA↔500mA)	76	22	~ 1	50	20	~ 1
APZP (This work)						
(100mA↔300mA)	26	8	0.95 ~ 1.05	26	6	0.8 ~ 0.95
(100mA↔400mA)	38	10	0.95 ~ 1.15	35	6	0.73 ~ 0.95
(100mA↔500mA)	48	10	0.95 ~ 1.2	44	6	0.675 ~ 0.95

TABLE IV
COMPARISON OF THE DROPOUT VOLTAGE WITH OTHER FAST TRANSIENT TECHNIQUES IN DC–DC CONVERTERS (UNDERSHOOT/OVERSHOOT)

	Conventional w/o fast transient	AFC [12]	Positive feedback [3]	APZP (This work)
Conventional w/o fast transient		81 % / 78.5 %	76 % / 71.4%	48 % / 62.8 %
AFC [12]	123 % / 127 %		93.8 % / 90.9 %	59.2 % / 80 %
Positive feedback [3]	131 % / 140 %	106 % / 110 %		63.1 % / 88 %
APZP (This work)	208 % / 159 %	168 % / 125 %	158 % / 113 %	

TABLE V
COMPARISON OF THE RECOVERY TIME WITH OTHER FAST TRANSIENT TECHNIQUES IN DC–DC CONVERTERS
(LIGHT LOAD CURRENT TO HEAVY LOAD CURRENT/ HEAVY LOAD CURRENT TO LIGHT LOAD CURRENT)

	Conventional w/o fast transient	AFC [12]	Positive feedback [3]	APZP (This work)
Conventional w/o fast transient		155 % / 155 %	48.8 % / 44.4 %	22.2 % / 13.3 %
AFC [12]	64.2 % / 64.2 %		31.4 % / 28.5 %	14.2 % / 8.57 %
Positive feedback [3]	204 % / 225 %	318 % / 350 %		45.4 % / 30 %
APZP (This work)	450 % / 750 %	700 % / 1166 %	220 % / 333 %	

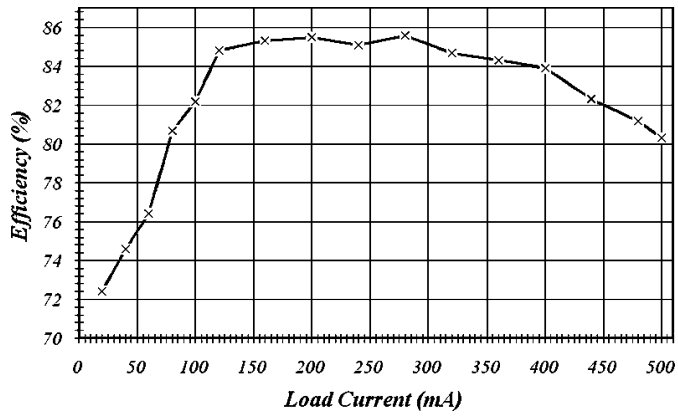


Fig. 18. Efficiency of the dc–dc converter with the proposed APZP technique.

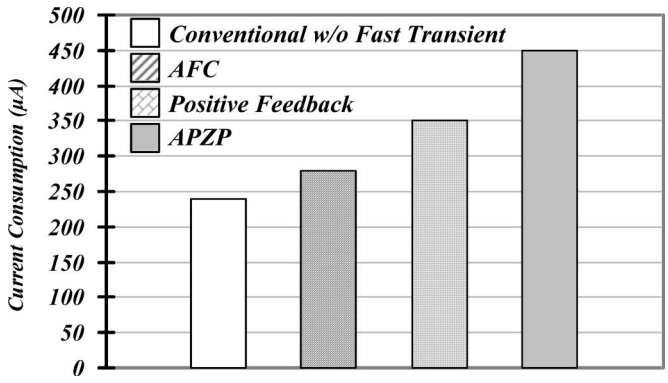


Fig. 19. Comparison of current consumption between different current-mode dc–dc converters.

VI. Conclusion

This paper proposed an APZP technique to achieve excellent transient response of dc–dc converters. Linear control methods reduce the output ripples and guarantee the stability of the system at the sacrifice of the response time. Contrarily, the positive-feedback control method simultaneously speeds up the response time and reduces the output ripples. However, it suffers from the oscillation problem because of large current injection into the output node. Thus, the APZP technique triggers the two-step positive-feedback control mechanism to speed up the transient response at the beginning of load variations. Before the output voltage is regulated back to its voltage level, the APZP technique merely functions as a linear control method to regulate the output voltage in order to ensure the stability of the system. Fast transient response time, low output ripples, and stable transient operation are achieved at the same time by our proposed APZP technique. Experimental results demonstrated that the transient undershoot/overshoot voltage and recovery time are enhanced 37.2% and 77.8%, respectively.

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