Acknowledgments

首先謝謝柯博兩年來的指導,讓我學習了很多研究的方法、精神,也在我擔任班長的職務時,時常給予我解惑,學到很多為人處世的道理以及管理的訣竅, 老師的幽默對話也常常讓我撲嗤一笑~

感謝其昌、俊淇學長在實驗上的帶領以及幫忙,真的是對我助益良多,這兩 年麻煩學長很多地方,真的是大~大~大~感謝~;謝謝佳典學長指導我,讓我知道 很多上至天文地理下至酒精菸草的知識,煮給我們吃的義大利麵真是一絕阿,講 話處處都是爆點,模仿更是厲害(王子麵);感謝坤霖教導我們 DNA 的固定化技 術,以及客運上的兩性關係;感謝乙介在實驗上的指導,以及定時更新 keroro, 讓實驗室多了一份歡笑;感謝志威教導我許多機台,讓我在 NDL 橫行無阻,還有 你的舞步很酷喔~印度麥可~;感謝建文在實驗上的開導及鼓勵,讓我在實驗室生 存下去;感謝小貓長的這麼正,因為我朋友都很羨慕我有一個正妹同學,也讓我 有來實驗室的動力哩; Michael 我們一起在 NDL 考機台的日子還記得吧, 那是我 們共同的美好回憶....有點噁心,不過真的感謝你在實驗及理論上的幫助~;謝 謝中書陪我熬夜做實驗,真的是非常認真聰明的學弟,謝謝你這一年來幫我們搽 煙,有腳脖子再報你知;謝謝阿生提供吃飯的地點,讓我享受美食不打烊…廣告 看太多,發現我們一搭一唱組合好像還不錯,下次一起殺敵吧~;謝謝皮皮在實 驗上的幫忙,真的!!自己也要好好加油喔~妳的動物表演好酷喔,下次來演傻里 巴基的研究生吧~呵;謝謝依臻的貼心,包括小卡以及花束,讓我感覺到很窩心 呢~;謝謝美榕常常問我幾點要回家,雖然我開玩笑回答關你屁事,其實心裡是 很謝謝妳的關心的~;感謝鄭捷這位 local king 的資訊協助,讓我玩遍新竹不迷 路;也謝謝敬雅、子銘、銘清、品麟、薏卉你們的協助與幫忙,我謹記在心~~

最後,要感謝我的父母、家人及室友,在我背後的支持,謝謝,真的!!

發展新穎側向閘極奈米線場效電晶體並應用於甲狀腺乳突 癌的感測

學 生: 吳奕儂 指導教授: 柯富祥 博士

國立交通大學奈米科技研究所碩士班

摘 要

以半導體奈米線為基礎的元件裝置作為免標示、高度敏感且具選擇性的感測器,偵測的生物或化學物種包括低濃度離子,小分子、蛋白質、DNA和病毒。 然而,製作'由下而上'的奈米線所需的流程,在未來的元件製作整合上具有非常大的阻礙。替代的'由上而下'製程近幾年來已經被提出。然而,大多數此類的感測器裝置所製作的開極是由背面開極組成,限制了未來大規模的整合。在這篇論文中,使用了互補式金氧半場效電晶體的技術(包含矽的局部氧化製程及電子東直寫技術)來製作我們的新穎側向閘極矽奈米線場效電晶體。利用矽的局部氧化製程來製作線寬縮小的奈米線,此線可以達到較高的表面體積比以及獲得側向閘極以供未來整合的應用。我們的元件是由矽-絕緣體-矽的晶圓當做基材,可提供一個很好的二氧化矽介電層品質,進而達到一個較低的漏電流以及較優良的場效應性質。

關於疾病診斷的應用,我們想要偵測與甲狀腺乳突癌有關聯的BRAF^{V599E}變異基因。甲狀腺乳突癌是一個人體中較常發生的內分泌腺惡性腫瘤。文獻報導指出,在BRAF這段基因序列產生變異,有66%的機會會導致嚴重的黑色素瘤,但對於人類的其他癌症,卻無法達到這麼高的比例。大部分發生突變的原因80%通

常來自於激酶裡一個鹼基的變異,而造成胺基酸的改變。

我們藉由修飾奈米線表面進而偵測此疾病的DNA序列。矽奈米線表面修飾上APTES使其呈現含氨基的末端,然後將單股的捕捉DNA固定化上去,藉此來偵測另一股互補的DNA,也就是BRAF^{V599 E}變異基因。在控制實驗方面,我們在奈米線接上含螢光標示物的單股DNA,利用螢光顯微鏡來確認DNA確實接在我們的單晶奈米線元件。最後,我們使用一個半導體電性分析儀量測每個步驟的電性變化。

由矽的局部氧化製程製作的奈米通道被鳥嘴效應影響,其線寬縮小的程度可以達到八十奈米以下。此元件的電性達到十萬倍的開關電流比,可偵測到一千億分之一的莫耳濃度,其臨界電壓變化可達0.86伏特。結果顯示此元件可達到免標示、高靈敏度、高選擇性的生物感測器。此外,我們的製作方法提供了未來在多物種的偵測可能性、個別的閘極控制能力,以及在單一晶片上整合的可能性。

Label-free Detection of the BRAF^{V599E} Mutation Genes with a

Novel Side-gated NWFET

Student: Yi-Nung Wu

Advisor: Prof. Fu-Hsiang Ko

Institute of Nanotechnology

National Chiao Tung University

Hsinchu 300, Taiwan, ROC

Abstract

Devices based on semiconducting nanowires are functioning as highly sensitive

and selective sensors for the label-free detection of biological and chemical species,

including low concentrations of ions, small molecules, proteins, DNA and viruses.

However, 'bottom-up' nanowires used for these demonstrations require hybrid

fabrication schemes, which result in severe integration issues that have impeded

widespread application. Alternative 'Top-down' fabrication methods of nanowire-like

devices have been proposed in recent year. Nevertheless, most devices are composed

of a back gate, which limits the application for the large-scale integration. In this

thesis, a novel side-gated Si NWFET was fabricated by an approach that uses

complementary metal oxide semiconductor (CMOS) field effect transistor compatible

technology, including the conventional LOCOS isolation process and electron-beam

writing. The shrinking nanowire with higher surface-to-volume ratio and individual

side gate for integration are achieved by the LOCOS process. Our side-gated devices

which fabricated using silicon-on-insulator (SOI) wafers provide a good quality of

IV

SiO₂ gate dielectric, which exhibits lower leakage current and excellent field effect properties than those with air dielectric.

Regarding to disease diagnosis, we want to detect the BRAF^{V599E} mutation gene, which has been recently reported to be restricted to papillary thyroid carcinomas (PTCs). The PTC is well known to a common endocrine malignancy of human cancer. It is reported that BRAF somatic missense mutations in 66% of malignant melanomas and at lower frequency in a wide range of human cancers. All mutations are within the kinase domain, with a single substitution (V599E) accounting for 80%.

Next, we modified the nanowires' surfaces for the goal of using them for biosensing. The silicon nanowire surface was modified using APTES to present amino groups and then single-stranded DNA was immobilized through these groups to allow the detection of its complementary single-stranded gene sequence (BRAF^{V599E} mutation gene). In a control experiment, we prepared a fluorescently labeled single-strand DNA so that we could observe, using fluorescence microscopy, that it did reside on the single crystal silicon nanowire. Finally, we used a semiconductor analyzer to measure the electrical properties of the nanowires at each step of the modification process.

The width of shrinking nano-channel by the LOCOS "bird's beak" can be 80 nm or thinner practically. The I_{DS} - V_G characteristic of the NWFETs exhibits about five orders of magnitude on I_{on}/I_{off} , and the threshold voltage shifts positively to 0.86V after hybridization of 10 picomolar concentrations of BRAF^{V599E} mutation gene. The results show that the nanowire-based device acts as a label-free, highly sensitive and selective biosensor for mutation gene sensing. In addition, our approach offers the possibility of highly parallel detection of multiple chemical and biological species with local control of individual elements in a single integrated chip.

Contents

Acknowledgments	I
摘 要	II
Abstract	IV
Contents	VI
Table Captions	.VIII
Figure Captions	IX
Chapter 1: Introduction	1
1.1 General Introduction	1
1.2 Top-Down Nanotechnology	2
1.3 Bottom-Up Nanotechnology	5
1.4 MotivationE.S.	9
1.5 Organization of the Thesis	11
Chapter 2: Literatures Review	13
2.1 Silicon Nanowire Nanosensors (Bottom–Up)	13
2.2 Silicon Nanowire Nanosensors (Top–Down)	19
Chapter 3: Experiment	25
3.1 General Information	25
3.2 Experiment Step	27
3.2.1 . Fabrication of Side-gated Silicon Nanowire Field Effect	
Transistor (NWFET)	27
3.2.2 . Covalent Attachment of the Capture DNA to the Nanowire	30
3.2.3 . Complementary and Non-complementary ssDNA Detection	32
Chapter 4: Results and Discussion	35
4.1 Physical and Electrical Property of Side-gated NWFETs	36

4.1.1 Determination of the Threshold Voltage	39
4.1.2 Determination of the Subthreshold Swing	40
4.1.3 Determination of On/Off Current Ratio	40
4.1.4 Determination of the Field-effect Mobility	40
4.1.5 Drain Induced Barrier Lowering (DIBL)	42
4.1.6 Kink Effect	46
4.2 Detection Concept	50
4.3 Sensing of Multi-Steps-APTES Immobilization, DNA Hybridization and	
Dehybridization	54
Chapter 5: Conclusions	59
References	60



Table Captions

Table 1.1 Product generations and chip size model technology trend target	ets of overall
roadmap technology characteristics (ORTC)	3
Table 4.1 Device parameters with channel width = 300nm and channel le	$ngth = 3\mu m$
	41
Table 4.2 Threshold voltage variation of DIBL effect	45
Table 4.3 The excess drain currents of kink effect from $L = 100 \sim 400$ nm,	$V_G = 5 \sim 20 V$
with $W = 300$ nm.	49



Figure Captions

Figure 1.1 Two basic approaches to nanomaterials fabrication
Figure 1.2 Schematic of nanoimprint lithography process
Figure 1.3 SEM image of the SiNW and side gates fabricated by using inorganic EB
resist process.
Figure 1.4 Electric field directed assembly of NWs
Figure 1.5 Fluid flow directed assembly of NWs.
Figure 1.6 NWs (blue lines) in a monolayer of surfactant at the air-water interface9
Figure 2.1 NW nanosensor for pH detection.
Figure 2.2 Real-time detection of protein binding.
Figure 2.3 (A) Schematic of a sensor device consisting of a SiNW(yellow) and a
microfluidic channel (green), where the arrows indicate the direction of sample
flow. (B) The SiNW surface with PNA receptor. (C) PNA-DNA duplex
formation16
Figure 2.4 Selective detection of single viruses
Figure 2.5 Detection of small molecule—protein interactions for tyrosine kinases 18
Figure 2.6 Field emission scanning electron microscopy photos of the fabricated
devices. There are two nanowires between electrodes
Figure 2.7 Electrical response of the device upon exposure to oxygen and nitrogen. 20
Figure 2.8 (a) The optical image of the central region of a sensor test chip used for
the DNA sensing study. (b) and (c) Representative SEM images showing the
SiNW bridging two contact leads.
Figure 2.9 (a) Optical image of the central region of a sensor test chip showing a
portion of the lead and the bridged nanowire (barely visible under the optical
microscope) used for the DNA sensing study; (b) schematic drawing of the
SiNWs with varying widths corresponding to the image in (a); (c) a
representative SEM image showing a portion of a 50-nm-wide SiNW, which
extends between two contact leads.
Figure 2.10 SEM image of SiNW after reaction of the gold nanoparticles with
AEAPTMS pretreated SiNW surface
Figure 2.11 I _{DS} -V _G curves of SiNW after binding of different molecules on the
surface of SiNW.
Figure 2.12 The three-dimensional AFM image of 40 nm width Pt-silicide nanowire.
22
Figure 2.13 Various immobilization steps for the DNA molecules on the Pt-silicide
nanowires22
Figure 3.1 Process flow chart of the side-gated NWFET device fabrication on the SO

wafer2
Figure 3.2 The shrinking nanowire and individual side gate are achieved by the
LOCOS process
Figure 3.3 OM image of the side-gated NWFET.
Figure 3.4 SEM image of 80nm width side-gated silicon nanowire
Figure 3.5 AFM image of 80nm width side-gated silicon nanowire
Figure 3.6 Fluorescence microscope image to ensure DNA existence on silicon
nanowires
Figure 3.7 The schematic of linker and DNA sequences
Figure 3.8 Fluorescence microscope image to ensure target DNA hybridization with
the capture DNA on silicon nanowires
Figure 3.9 The schematic image of overall modification and DNA detection
procedure
Figure 4.1 Noise level of HP-4156 semiconductor analyzer
Figure 4.2 (a) Top-view layout of a side-gated NWFET (b) Amplification of the area
dotted in (a)
Figure 4.3-1 SEM images of side-gated NWFET with channel length = $2\mu m$ 3
Figure 4.3-2 SEM images of side-gated NWFET with channel width = 80nm3
Figure 4.4-1 The I_{DS} - V_G characteristic of the side-gated NWFETs. The applied drain
-to-source voltage is 0.1, 1, and 2V, respectively
Figure 4.4-2 The I _{DS} -V _{DS} characteristic of the side-gated NWFET. The applied gate
voltage is 0, 5, 10, 15, and 20V, respectively
Figure 4.5 Drain induced barrier lowering. A cross-section view of potential energy
distribution along the long and short channels in MOSFETs4
Figure 4.6-1 The I _{DS} -V _G characteristic of the side-gated NWFETs of channel length =
800nm. The applied drain -to-source voltage is 0.1, 1, and 2V, respectively4
Figure 4.6-2 The I _{DS} -V _G characteristic of the side-gated NWFETs of channel length =
600nm. The applied drain -to-source voltage is 0.1, 1, and 2V, respectively4
Figure 4.6-3 The I _{DS} -V _G characteristic of the side-gated NWFETs of channel length =
400nm. The applied drain -to-source voltage is 0.1, 1, and 2V, respectively4
Figure 4.6-4 The I _{DS} -V _G characteristic of the side-gated NWFETs of channel length =
200nm. The applied drain -to-source voltage is 0.1, 1, and 2V, respectively4
Figure 4.6-5 The I _{DS} -V _G characteristic of the side-gated NWFETs of channel length =
100nm. The applied drain -to-source voltage is 0.1, 1, and 2V, respectively4
Figure 4.7 The kink effect in the output characteristics of an n-channel SOI MOSFET
4
Figure 4.8-1 The $I_{\rm DS}\text{-}V_{\rm DS}$ characteristic of the side-gated NWFETs of channel length
= 800nm. The applied gate voltage is 0, 5, 10, 15, and 20V, respectively4

Figure 4.8-2 The I_{DS} - V_{DS} characteristic of the side-gated NWFETs of channel length	h
= 600nm. The applied gate voltage is 0, 5, 10, 15, and 20V, respectively	47
Figure 4.8-3 The I_{DS} - V_{DS} characteristic of the side-gated NWFETs of channel length	h
= 400nm. The applied gate voltage is 0, 5, 10, 15, and 20V, respectively	48
Figure 4.8-4 The I_{DS} - V_{DS} characteristic of the side-gated NWFETs of channel length	h
= 200nm. The applied gate voltage is 0, 5, 10, 15, and 20V, respectively	48
Figure 4.8-5 The I_{DS} - V_{DS} characteristic of the side-gated NWFETs of channel length	h
= 100nm. The applied gate voltage is 0, 5, 10, 15, and 20V, respectively	49
Figure 4.9 Excess drain current (ΔI_{DS}) versus gate voltage (V_G) at channel length =	=
100, 200 and 400nm	50
Figure 4.10 NMOS transistor: qualitative I-V behavior.	52
Figure 4.11 Surface potential energy scheme to show the DNA detection concept	53
Figure 4.12 The schematic image of overall modification and DNA detection	
procedure	56
Figure 4.13 The I _{DS} -V _G curve of complementary DNA detection.	56
Figure 4.14 The I _{DS} -V _G curve of non-complementary DNA detection	57
Figure 4.15 The threshold voltage of immobilized step (1)~(5)	57
Figure 4.16 The threshold voltage of immobilized steps which compare	
complementary and non-complementary DNAs.	58

Chapter 1: Introduction

1.1 General Introduction

Nanotechnology is a revolution in science and technology. It distinguishes itself from all previous scientific and industrial revolutions in many ways. In fact, for the first time in human history, man can (1) change the fundamental properties (such as band gaps and luminescence) of matter as well as tailor make materials with desirable attributes; (2) manipulate nanoscale objects (such as atoms and molecules); and (3) fabricate and build single-nanowire/nanotube single-electron/photon nanodevices. These are just main three of the many characteristics of the nano revolution. The first characteristic is due to the so-called quantum size effects whereby the properties of a material change with its size in the nanometer regime. The second is made possible by the invention of high resolution transmission electron microscopy (TEM) and scanning probe microscopy (SPM), including scanning tunneling microscopy (STM) and atomic force microscopy (AFM). The third is the result of the developments of various nanofabrication techniques (such as nanoimprint lithography (NIL) using electron beams or extreme ultraviolet) as well as due to a physical phenomenon known as "quantum confinement" in the nanorealm. There is no doubt that the nano revolution will impact every aspect of human activities, not just in science and technology.

Figure 1.1 shows, in principle, two approaches to nanotechnology: the "bottom-up" strategy and the "top-down" approach. The "bottom-up" strategy attempts to build nanodevices from atomic or molecular components. The "top-down" approach seeks to fabricate nanodevices on silicon (or other semiconductors) chips directly using electron beam or extreme ultraviolet lithography.

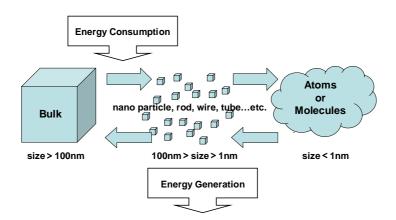


Figure 1.1 Two basic approaches to nanomaterials fabrication: top-down (from left to the right) and bottom-up (from right to the left).

1.2 Top-Down Nanotechnology

The "top-down" approach seeks to fabricate nanodevices "top-down" by etching silicon (or other semiconductors) chips using lithography (either photolithography or electron lithography). Indeed, the "top-down" approach has been the method of choice in the semiconductor industry for making microelectronic and other devices for decades. The semiconductor industry entered the nanotechnology era in the year 2000, and by 2004, the industry was shipping devices with physical gate dimension of less than 40 nm and insulator thickness of less than 1 nm. This is in line with the pace of Moore's Law (Table 1.1^[1]). The current development of the state-of-the-art optical lithography at 193 nm wavelength, together with liquid immersion, is pushing the limit of 32 nm (half pitch). Dimensions smaller than 32 nm and generally viewed as beyond the capabilities of optical lithography at 193 nm wavelength, unless high-index fluids, high-index lens materials, and higher-index resist, can be developed. Another way to extend the lifetime of

optical projection lithography with immersion to 32 nm half pitch and beyond is to divide the pattern into two or more masks. However, this latter strategy will undoubtedly increase the cost of manufacturing.

Year of Production	2005	2006	2007	2008	2011	2014	2017	2020
DRAM ½ Pitch (nm)	80	70	65	57	40	28	20	14
MPU/ASIC ½ Pitch (nm)	90	78	68	59	40	28	20	14
MPU Gate Length (nm)	54	48	42	38	27	19	13	9
ASIC Gate Length (nm)	76	64	54	48	34	24	17	12
Flash ½ Pitch (nm)	76	64	57	51	36	25	18	13

Table 1.1 Product generations and chip size model technology trend targets of overall roadmap technology characteristics (ORTC)

It is generally believed that extension of the Roadmap for semiconductor industry beyond 32 nm will probably require the development of "next-generation" lithography (NGL) technologies such as extreme ultraviolet lithography (EUVL), maskless (ML2), and imprint lithography. Because the "next-generation" lithographies will most likely require the development of substantially new infrastructure, implementation of these new technologies as viable manufacturing solutions can be a real challenge for the industry. [2]

Recent development in EUVL is expected to be used in manufacturing starting at 32 nm half pitch. The EUV lithography is a projection optical technology that uses 13.5 nm wavelength. It is approaching the wavelengths of soft X-rays. At this wavelength, all materials are highly absorbing, so the imaging system is composed of mirrors coated with multilayer structures designed to have high reflectivity at 13.5 nm wavelength.

For definitions or features thinner than 32 nm, it is necessary to use electron

beams, extreme ultraviolet or the so-called "nanoimprint lithography (NIL)" (Figure 1.2).^[3-5] High-energy electron beams or extreme ultraviolet can provide definitions of a few nanometers. The current state-of-the-art definition in NIL using electron beams is about 5 nm.^[3-5] It is obvious that "nanoimprint" lithography can achieve much better resolution than EUVL discussed earlier. However, it suffers from, among other things, cost effectiveness, mass production capability, and defect tolerance problems. The main reason is that NIL is essentially a 1 × multilayer mold technology.

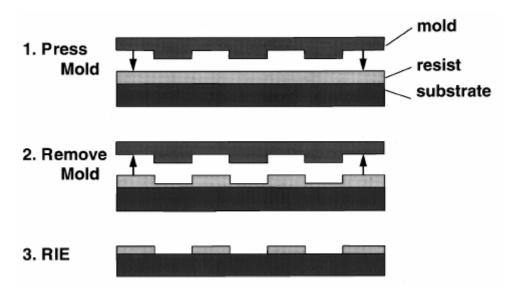


Figure 1.2 Schematic of nanoimprint lithography process: (1) imprinting using a mold to create a thickness contrast in a resist, (2) mold removal, and (3) pattern transfer using anisotropic etching to remove residue resist in the compressed areas.

It is interesting to note that, at or below about 15 nm, quantum confinement sets in, making single-nanowire/nanotube single-electron nanodevices a reality. We shall now mention briefly one example of single electron nanodevices which capitalizes on quantum confinement effects. Figure 1.3^[6] depicts the single-electron memory and single-electron transistor nanodevices fabricated by Tsutsumi et al. using an inorganic SiO₂ electron beam resist. These single-electron nanodevices^[6–8] are possible owing

to the carrier confinement and Coulomb blockade effects exhibited by the very narrow silicon nanowires (SiNWs) and very small silicon nanodots (SiNDs) in the nano regime. Indeed, 15 nm wide SiNW channel and 5-10 nm isolated silicon islands were used in the work of Tsutsumi et al.^[6]

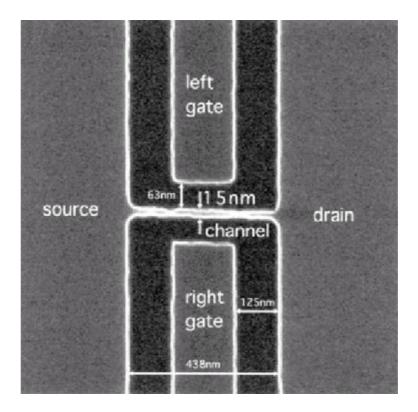


Figure 1.3 SEM image of the SiNW and side gates fabricated by using inorganic EB resist process. The width, height, and length of the SiNW are 15, 20, and 438 nm, respectively.

1.3 Bottom-Up Nanotechnology

The bottom-up approach to nanotechnology seeks to build nanodevices from the atomic or molecular components. There are basically five steps in the bottom-up approach. The first is to tailor make nanomaterials with desirable properties. The second is to etch (clean), passivate, or dope the surface of the nanomaterial for a

particular application. The third is to precision cut or machine nanomaterials into individual components (or to grow them in situ at precise locations). The fourth step is to fabricate various nanostructural elements and assemble or organize these elements or components into nanodevices. And finally, the last step is to link (interconnect and integrate) individual nanodevices together to form functional devices and connect them to the micro, and eventually to the macroscopic world.

Many efforts have been made on the first three steps, namely, a wide variety of nanomaterials with controllable morphology, size, structure, and composition have been synthesized and their physical and chemical properties investigated. Single nanodevices such as FET, diodes, light-emitting diodes, sensors, etc. using serial lithographic processing, such as electron-beam lithography, have also been fabricated (the fourth step). The last step, namely, the controlled assembly and intergration of the various building blocks into functional systems, is still a formidable challenge for the bottom-up approach. Some progress has been made, however, for example, electric fields (Figure 1.4),[9-11] microfluidic (Figure 1.5)[12,13] and Langmuir – Blodgett (LB) techniques (Figure 1.6)[14-17] have recently been used in assembling SiNWs into high-density arrays. Many issues such as mass production and reproducibility, however, remain to be addressed. Finally, organizing various elements into basic units and interconnecting them to form functional nanodevices are yet two more hurdles in the "bottom-up" approach. The ultimate challenge, however, seems to be the interface of the nanodevices to the micro, and eventually to the macro, world.

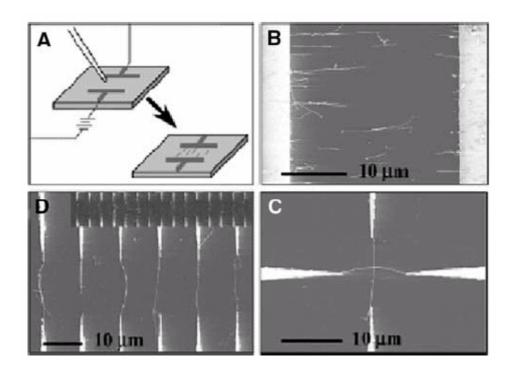


Figure 1.4 Electric field directed assembly of NWs. (A) Schematic representation of E-field alignment. (B) Parallel array of NWs aligned between two parallel electrodes. (C) Spatially positioned parallel array of NWs obtained following E-field assembly. The top inset shows 15 pairs of parallel electrodes with individual NWs bridging each diametrically opposed electrode pair. (D) Crossed NW junction obtained using layer-by-layer alignment with the E-field applied in orthogonal directions in the two assembly steps.

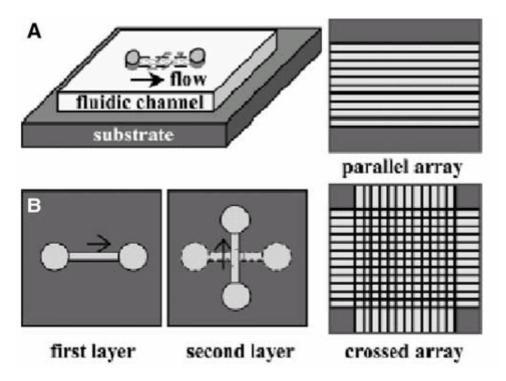


Figure 1.5 Fluid flow directed assembly of NWs. (A) A channel is formed when a trench structure is brought in contact with a flat substrate. Nanowire assembly is carried out by flowing a NW suspension through the channel at a controlled rate and for a set duration. Parallel arrays of NWs are observed in the flow direction on the substrate when the trench structure is removed. (B) Crossed NW arrays can be obtained by changing the flow direction sequentially in a layer-by-layer assembly process.

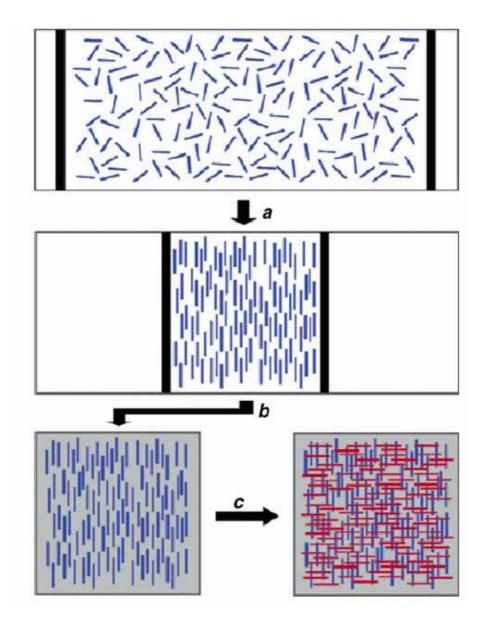


Figure 1.6 NWs (blue lines) in a monolayer of surfactant at the air-water interface are (a) compressed on a Langmuir – Blodgett trough to a specified pitch. (b) The aligned NWs are transferred to the surface of a substrate to make a uniform parallel array. (c) Crossed NW structures are formed by uniform transfer of a second layer of aligned parallel NWs (red lines) perpendicular to the first layer (blue lines).

1.4 Motivation

Ultrasensitive detection of biological and chemical species is fundamental to the screening and detection of disease, discovery and screening of drugs, as well as gas

detection and biomolecular analysis.

One-dimensional nanostructures have been demonstrated as good candidates for ultrasensitive, miniaturized molecule sensors in the above-mentioned applications. Among the variety of systems explored, the sensors based upon semiconductor nanostructures, such as semiconductor single-wall carbon nanotubes, [18-20] silicon nanowires, [21] SnO₂ nanowires, [22] and In₂O₃ nanowires, [23] could be generally understood in terms of change of surface charge of the nanostructures with the presence or absence of molecular species. Because of the high surface-to-volume ratio of the nanostructures, their electronic conductance may be sensitive enough to the surface species that single molecule detection becomes possible.

However, most of the existing studies based on "bottom-up" nanostructures are limited by complex integration, requiring transfer and positioning of an individual nanostructure and making reliable ohmic contacts. Furthermore, the control of doping concentrations in self-assembled semiconducting nanostructures remains a challenge, and the fabrication of high-density sensor arrays is also very difficult. Here we demonstrate the detection of DNA molecules based on their intrinsic charge by using silicon nanowires (SiNWs) fabricated by standard "top-down" semiconductor processes. This method creates a pathway for fabricating high-density, high-quality nanoscale sensors that can be integrated with silicon-based signal processing and communication circuits.

The global back-gate^[24] structure was widely used to achieve working NWFETs. In this structure, all devices on the wafer were forced to share the same gate and they cannot be addressed individually. Furthermore, the back-gate covers the entire source/drain (S/D) region, which induces large parasitic capacitance between gate and the S/D metal electrodes. To solve this problem, top-gate and local back-gate configurations were proposed. However, the top-gate designs lacked the contact area

with biomolecules, and the local back-gate ones were still limited for the large-scale integration.

In this thesis, to address the aforementioned problems of NWFETs, we combine the advantages of in situ-grown LOCOS isolation process, electron-beam writing technology, and SOI technology to propose and demonstrate a local silicon side-gated NWFET configuration. By patterning the doped SOI silicon film to form local gates, an individual gate for every NWFET has been realized.

The shrinking nanowire with higher surface-to-volume ratio and individual side gate for integration are achieved by the LOCOS process. The detection sensitivity is therefore greatly enhanced as the signal can be effectively transduced because of large surface-to-volume ratio. Our side-gated devices which fabricated using silicon-on-insulator (SOI) wafers provide a good quality of SiO₂ gate dielectric, which exhibits lower leakage current and excellent field effect properties than those with air dielectric. With a good quality of SiO₂ gate dielectric, the electric field was induced more by the charged molecule, and the detection signal varied more distinctly, sensitively.

1.5 Organization of the Thesis

In this thesis, we reports that side-gated silicon nanowire field effect transistor (NWFET) as a novel DNA sensor manufactured by standard semiconductor process. We fabricate nanowires on silicon-on-insulator (SOI) wafer and have high sensitivity. Then label-free single-stranded DNA was modified on nanowire, and all reagent and solvent were of reagent-grade quality, commercial purchase, and no further purification. In order to overcome some challenges in this work, for example: pattern definition, nanowire shrinking, label-free DNA modification and electrical signal detection...etc. We need to survey the basic of biology, biochemistry, electronics and

the technology of electron beam lithography, nanofabrication, and self-assembly technique.

In chapter 1, the general overview of the methods "Top-Down" and "Bottom-Up" approach to "Nanotechnology", and the aim to bio-molecules DNA detection. Literature surveys of silicon nanowire nanosensors, fabrication tools and experiment ideals are introduced in chapter 2. The detail of fabrication processes and immobilized steps are presented in chapter 3. In chapter 4, we do not only discuss the electrical property of side-gated silicon NWFET, but also present the application of DNA detection. Then the summaries and contributions of this thesis are addressed in the final chapter.

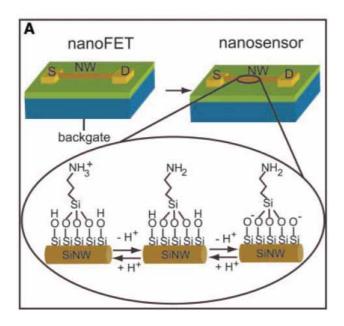


Chapter 2: Literatures Review

2.1 Silicon Nanowire Nanosensors (Bottom-Up)

Lieber's group has done a series of works for bottom-up silicon nanowire nanosensors. They presented highly sensitive and real-time sensors based on electrically boron-doped silicon nanowires (SiNWs) for detecting a biological and chemical species. Amine and the oxide-functionalized SiNWs exhibited pH-dependent conductance that was linear over a wide dynamic range.^[1]

They evaluated the response the of 3-aminopropyltriethoxysilane-modified SiNW to changes in solution pH by fabricating a cell consisting of a microfluidic channel formed between a poly(dimethylsiloxane) (PDMS) mold and the SiNW/substrate.^[2] Continuous flow or static experiments in Figure 2.1 demonstrated that the SiNW conductance increases stepwise with discrete changes in pH from 2 to 9 and that the conductance was constant for a given pH; the changes in conductance were also reversible for increasing and/or decreasing the pH. These results could be understood by considering the change in surface charge during protonation and deprotonation after the surface functionality of the modified SiNWs.



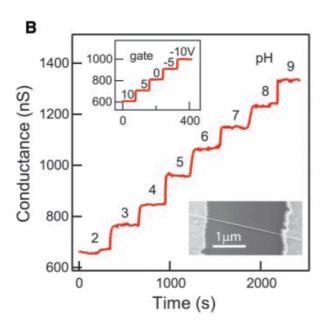


Figure 2.1 NW nanosensor for pH detection. (A) Schematic illustrating the conversion of a NWFET into NW nanosensors for pH sensing. The NW is contacted with two electrodes, a source (S) and drain (D), for measuring conductance. Zoom of the APTES-modified SiNW surface illustrating changes in the surface charge state with pH. (B) Real-time detection of the conductance for an APTES-modified SiNW for pHs from 2 to 9; the pH values are indicated on the conductance plot. (inset, top) Plot of the time-dependent conductance of a SiNW FET as a function of the back-gate voltage. (inset, bottom) Field-emission scanning electron microscopy image of a typical SiNW device.

To explore biomolecular sensors, they functionalized SiNWs with biotin and studied the well-characterized ligand–receptor binding of biotin–streptavidin in Figure 2.2. Measurements showed that the conductance of the biotin-modified SiNWs increased rapidly to a constant value upon addition of a 250nM streptavidin solution and that this conductance value was maintained after the addition of a pure buffer solution. They confirmed that the observed conductance changes were due to the

specific binding of streptavidin to the biotin ligand.

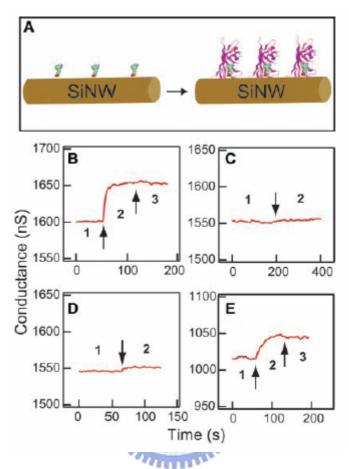


Figure 2.2 Real-time detection of protein binding. (A) Schematic illustrating a biotin-modified SiNW (left) and subsequent binding of streptavidin to the SiNW surface (right). The SiNW and streptavidin are drawn approximately to scale. (B) Plot of conductance versus time for a biotin-modified SiNW, where region 1 corresponds to buffer solution, region 2 corresponds to the addition of 250 nM streptavidin, and region 3 corresponds to pure buffer solution. (C) Conductance versus time for an unmodified SiNW; regions 1 and 2 are the same as in (B). (D) Conductance versus time for a biotin-modified SiNW, where region 1 corresponds to buffer solution and region 2 to the addition of a 250 nM streptavidin solution that was preincubated with 4 equivalents d-biotin. (E) Conductance versus time for a biotin-modified SiNW, where region 1 corresponds to buffer solution, region 2 corresponds to the addition of

25 pM streptavidin, and region 3 corresponds to pure buffer solution. Arrows mark the points when solutions were changed.

Hahm and Lieber^[3] also demonstrated that p-type SiNWs functionalized with peptide nucleic acid (PNA) receptors functioned as ultrasensitive and selective real-time DNA sensors at concentrations down to tens of femtomolar range in Figure 2.3.

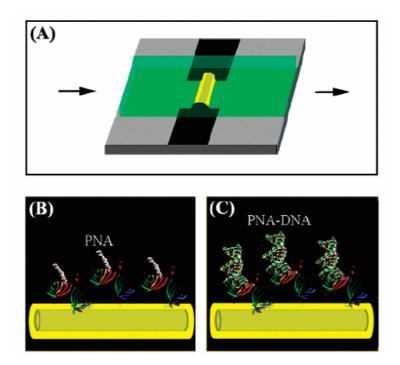


Figure 2.3 (A) Schematic of a sensor device consisting of a SiNW(yellow) and a microfluidic channel (green), where the arrows indicate the direction of sample flow.

(B) The SiNW surface with PNA receptor. (C) PNA-DNA duplex formation.

Direct, real-time electrical detection of single virus particles with high selectivity by using nanowire field-effect transistors was also reported by Lieber and co-workers.^[4] Measurements made with nanowire arrays modified with antibodies for influenza A showed discrete conductance changes characteristic of binding and unbinding in the presence of influenza A but not paramyxovirus or adenovirus. The

authors suggested that the conductance of that device should change from the baseline value when a virus particle was bound to the antibody receptor on a nanowire device, and the conductance should return to the baseline value when the virus was unbound. Figure 2.4 shows the parallel collection of conductance, fluorescence, and right-field data from a single nanowire device with fluorescently labeled viruses.

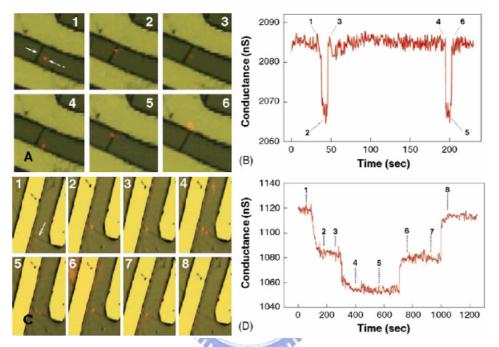


Figure 2.4 Selective detection of single viruses. (A) Optical and (B) conductance data recorded simultaneously versus time for a single silicon nanowire device after introduction of influenza A solution. (C) Optical and (D) simultaneous conductance vs. time data recorded from a single nanowire device with a high density of anti-influenza type A antibody.

They continued to study a highly sensitive detection scheme for identifying small molecule inhibitors that did not require labeling of the protein, ATP, or small molecule and could be carried out in real-time by using SiNWs field-effect transistor (FET) devices.^[5] They linked the Abl tyrosine kinase to the surface of SiNWs FET within microfluidic channels to create active electrical devices and investigated the

binding of ATP and competitive inhibition of ATP binding with organic molecules, as shown schematically in Figure 2.5 (left bottom). Plots of the normalized conductance versus time recorded from the Abl-modified SiNW devices (Figure 2.5, right) exhibit reversible decreases in conductance due to competitive inhibition of ATP binding by small molecules.

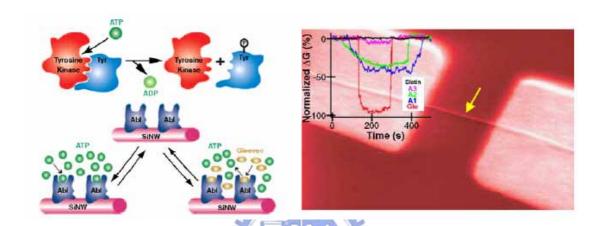


Figure 2.5 Detection of small molecule—protein interactions for tyrosine kinases. (Left, top) Scheme illustrating basic activity of a tyrosine kinase: ATP binds to the

tyrosine kinase active site, and then the —phosphate group is transferred to the tyrosine (Tyr) residue of the substrate protein. (Bottom) Detection of ATP binding and small molecule inhibition of binding by using a SiNW sensor device. The tyrosine kinase Abl is covalently linked to the surface of a SiNW, and then the conductance of the nanowire device is monitored to detect ATP binding and the competitive inhibition of ATP binding by Gleevec. (Right) Scanning electron micrograph of a typical SiNW FET device. The nanowire is highlighted by a yellow arrow and is contacted on either end of Ti–Au metal electrodes. (Inset) Normalized conductance vs. time data recorded from Abl-modified SiNW devices by using solutions containing 100nM ATP and 50nM small molecules for Gleevec (red), A1 (blue), A2 (green), A3 (pink), and biotin (black).

2.2 Silicon Nanowire Nanosensors (Top-Down)

Bashir and co-workers^[6] described silicon nanowire sensor that was realized using top–down microelectronics processing techniques. A process known as confined lateral selective epitaxial growth (CLSEG)^[7] was utilized to obtain single crystal silicon nanoplates that are thin as 7nm and nanowires small as 40nm in diameter at precise locations shown in Figure 2.6.^[6] The method allows the realization of truly integrated dense array of sensor. Initial testing of the device showed sensitivity towards oxygen ambient, and suggested it possibility of using these sensors for chemical and biological detection shown in Figure 2.7.^[6]

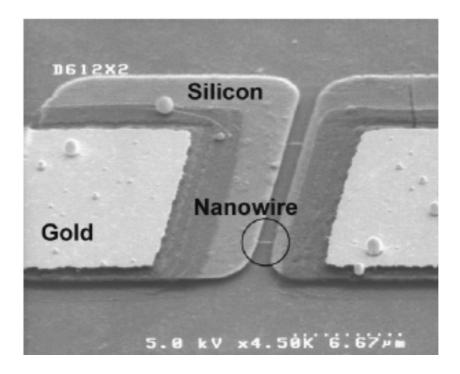


Figure 2.6 Field emission scanning electron microscopy photos of the fabricated devices. There are two nanowires between electrodes.

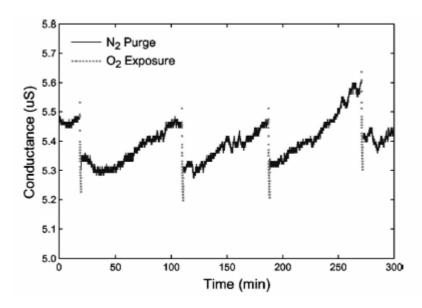


Figure 2.7 Electrical response of the device upon exposure to oxygen and nitrogen.

Li et al.^[8,9] fabricated 50 nm width single crystal silicon nanowire on SOI wafer by electron bean lithography in Hewlett-Packard Laboratories. They demonstrated the detection of DNA molecules based on their intrinsic charge by using silicon nanowires fabricated by standard top-down semiconductor processes. This method creates a pathway for fabricating high-density, high-quality, well organization nanoscale sensors that can be integrated with silicon-based signal processing and communication circuits show in Figure 2.8.^[8] Sequence-specific label-free DNA sensors based on SiNWs with peptide nucleotide acid (PNA) or single-stranded (ss) probe DNA molecules covalently immobilized on the nanowire surfaces in Figure 2.9.^[9] Label-free complementary (target) ss-DNA in sample solutions were recognized when the target DNA was hybridized with the probe DNA attached on the SiNW surfaces, producing a change of the conductance of the SiNWs. For a 12-mer oligonucletide probe, 25pM of the target DNA in solution was detected easily (signal/noise ratio > 6), whereas 12-mer with one base mismatch did not produce a signal above the background noise.

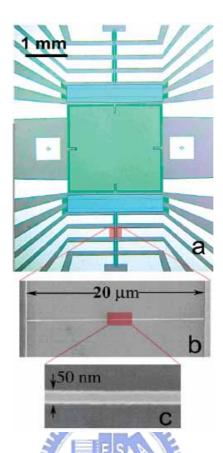


Figure 2.8 (a) The optical image of the central region of a sensor test chip used for the DNA sensing study. (b) and (c) Representative SEM images showing the SiNW bridging two contact leads.

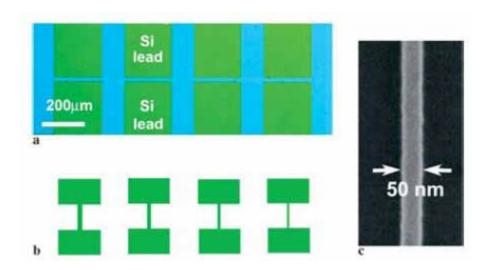


Figure 2.9 (a) Optical image of the central region of a sensor test chip showing a portion of the lead and the bridged nanowire (barely visible under the optical

microscope) used for the DNA sensing study; (b) schematic drawing of the SiNWs with varying widths corresponding to the image in (a); (c) a representative SEM image showing a portion of a 50-nm-wide SiNW, which extends between two contact leads.

Sheu et al.^[10] demonstrated molecular detection based on SiNWs whose surface was pretreated by N-(2-aminoethyl)-3-aminopropyl-trimethoxysilane and then selectively deposited with gold nanoparticles in Figure 2.10 and 2.11.^[10] The gold nanoparticles deposited on the oxide surface of the SiNWs and then functionalized with amino groups served as linkers to detect molecules. The target molecules, such as ⁵-3-ketosteroid isomerase (KSI-126C) molecules, bound with gold nanoparticles on the surface of the SiNWs and resulted in a voltage shift.

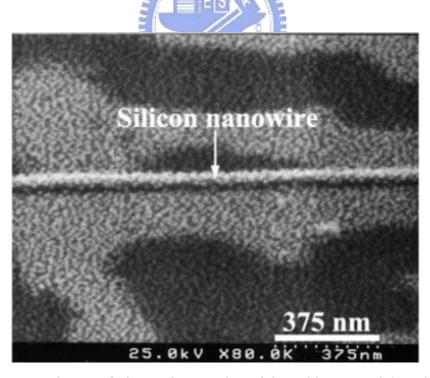


Figure 2.10 SEM image of SiNW after reaction of the gold nanoparticles with AEAPTMS pretreated SiNW surface.

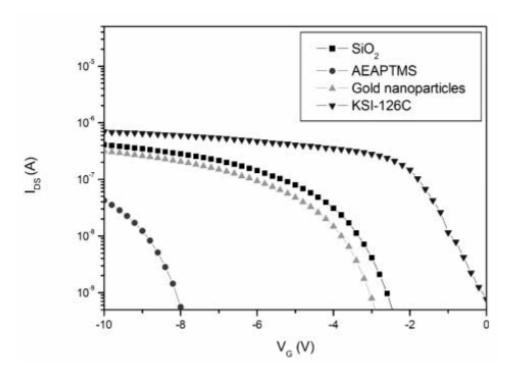


Figure 2.11 I_{DS} - V_G curves of SiNW after binding of different molecules on the surface of SiNW. The turn-on voltage was changed from -2.7V to -8.1V to -3.2V to -0.2V after binding of AEAPTMS, gold nanoparticles and enzyme KSI-126C.

Ko et al.^[11] developed a self-aligned platinum-silicide nanowire for biomolecule sensing in Figure 2.12 and 2.13.^[11]. The 40 nm nanowire is fabricated through a sequence of electron-beam writing on the polysilicon film, line shrinkage with alkaline solution, platinum film deposition, 550 °C annealing, and aqua regia dissolution. The immobilization of single-stranded capture DNA onto the platinum-silicide nanowire is verified from the fluorescence-labeled technique. The field-effect transistor can distinguish the complementary, mismatched, and denatured DNA via the conductance difference. Although the nanowire sensor has not been integrated into a fluid channel system, they can sense the minimal target DNA concentration down to 100 fM, and the signal is still 1000-fold larger than the noise signal.

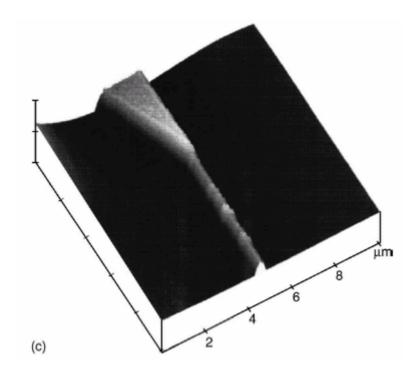


Figure 2.12 The three-dimensional AFM image of 40 nm width Pt-silicide nanowire.

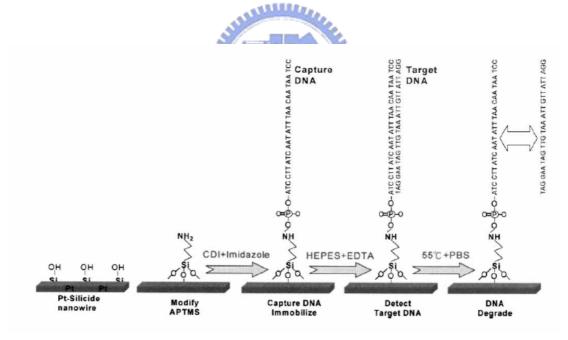


Figure 2.13 Various immobilization steps for the DNA molecules on the Pt-silicide nanowires.

Chapter 3: Experiment

In Chapter 2, we have introduced some kind of fabrication technologies of silicon nanowire, including "bottom-up" and "top-down" processes. Here, we will introduce a nanowire structure of single crystalline silicon. We fabricated silicon nanowire field effect transistor (NWFET) by electron beam lithography (EBL) and shrinked by LOCOS process. In our fabrication process, we use commercial semiconductor equipments located at National Nano Device Laboratories.^[1]

3.1 General Information

All reagent and solvent were of reagent-grade quality, purchased commercially, and used no further purification unless otherwise noted. The experimental reagents are showed as follows:

- 1. Deoxyribonucleic acids (OPC grade; MDBio Inc.)
 - Capture DNA

5'-AAATATATTA-TTACTCTTGA-GGTCTCTGTG-3'

■ Complementary target DNA

3'-TTTATATAAT-AATGA**GAACT-**CCAGAGACAC-5'

■ Non-complementary target DNA

3'-TTTATATAAT-AATGA**TGCCG**-CCAGAGACAC-5'

- Sulfuric acid (molecular formula H₂SO₄; purity 98%; Sigma)
 Sulfuric acid is mixed with hydrogen peroxide as ratio of 3:1 to clean the sample.
- 3. Deionized and distilled water (DI water, ddH₂O)

The water we used was purified with filters, reverse osmosis, and deionized system until the resistance was more than 18 M Ω . DI water was used to clean,

wash, and be a solvent.

4. (3-Aminopropyl)triethoxysilane (APTES; molecular formula

H₂N(CH₂)₃Si(OCH₂CH₃)₃; purity 98%; Fluka)

The purpose of APTES molecule is to modify the exposed SiO₂ surface on silicon nanowire. Ethoxy functional groups of APTES will form covalent bonding with hydrophilic hydroxyl groups attached to the SiO₂ surface to form molecular layer of amino groups in order to bond with DNA molecules.

- 5. Acetone (molecular formula CH₃COCH₃; purity 99.5%; Sigma)

 Acetone was mixed with DI water to provide an environment that facilitates the APTES binding to the SiO₂ surface.
- 6. Hydrogen chloride (HCl; ≥99% purity; Sigma)1 M HCl in DI water was used for pH adjustment.
- Glutaraldehyde (molecular formula OHC(CH₂)₃CHO; purity Grade I, 25% in H₂O; Sigma-Aldrich)

It was a traditional fixative in the histocytometry and electron microscopy. We used it as a linker to combine two amine-contained molecules. This chemical needs to store at -20° C.

- 8. N-2-Hydroxyethylpiperazine-N'-2-ethanesulfonic acid (HEPES; molecular formula C₈H₁₈N₂O₄S; purity 99%; CALBIOCHEM)
 HEPES is a biological buffer solution and is mixed with EDTA to conserve capture and target DNA molecules during the reactions.
- 9. Ethylenediaminetetraacetic acid (EDTA; molecular formula (HOOCCH₂)₂NCH₂CH₂N(CH₂COOH)₂; purity 99%;CALBIOCHEM)
 The aim of EDTA agent is to capture the cations like Mg²⁺, Ca²⁺, and so on , which can induce the activities of some enzymes to digest and destroy the structures of nucleic acids during experimental processes..

3.2 Experiment Step

All experiments were performed with silicon-on-insulator (SOI) wafer. In our experiment, there are four major steps- (1) fabrication of side-gated silicon nanowire field effect transistor (NWFET), (2) self-assembly linker layer between DNA and nanowire, (3) complementary and mismatch single stranded DNAs detection.

3.2.1 . Fabrication of Side-gated Silicon Nanowire Field Effect Transistor (NWFET)

The procedure of device fabrication is illustrated in Figure 3.1. Silicon-on-insulator (SOI) wafers were used. First, standard RCA cleaning and SiO₂/Si₃N₄ film were deposited using APCVD/LPCVD as the masking layer for LOCOS process. Second, the electron beam resist NEB 22-A was spin-coated by TEL CLEAN TRACK MK-8. Next, The Leica WePrint 200 e-beam writer was used to pattern nanowires of various widthes and lengthes and isolated gate. TMAH (Tetra-Methyl Ammonium Hydroxide) 2.38% reagent was used to develop the unexposed resist. Due to the resolution of Leica e-beam direct writer, we need to choose the optimal exposure dose. Then, masking layer was etched using TEL (TEL TE5000) oxide etcher, and followed, removal of the resist by thermal ozone (FUSION OZONE ASHER) and H_2O_2/H_2SO_4 ($H_2O_2/H_2SO_4 = 3:1$) dipping for 10 minutes. The LOCOS process was executed to form the nanowire structure, isolated gate, and gate oxide at the same time by APCVD, followed by the removal of masking layer by wet bench. Third, the e-beam lithography process was used again to pattern the N⁺ implantation area which was implanted with As(arsenic) ion by implanter (VARIAN E500HP). Then, the As ion was activated at 1050°C for 30s by rapid thermal annealing (KORONA RTP 800). Finally, the matel pad area was patterned by e-beam lithography and deposited with Cr/Au (20nm/80nm) by thermal coater. Then, the lift-off process took the needless resist and metal away by NMP (N-Methyl-2-Pyrrolidone) stripper.

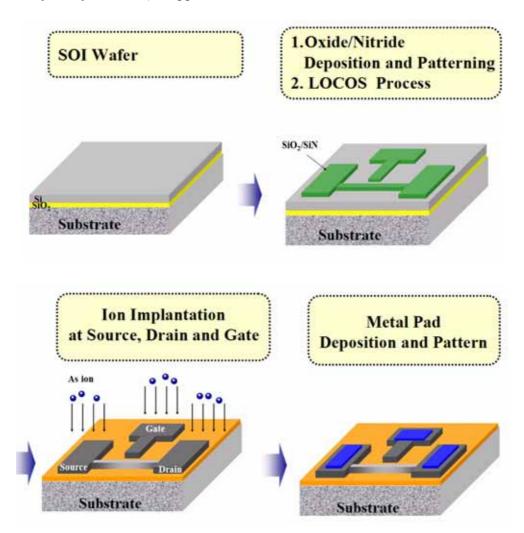


Figure 3.1 Process flow chart of the side-gated NWFET device fabrication on the SOI wafer.

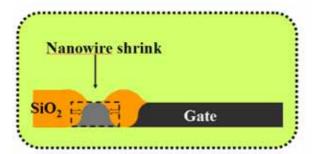


Figure 3.2 The shrinking nanowire and individual side gate are achieved by the LOCOS process.

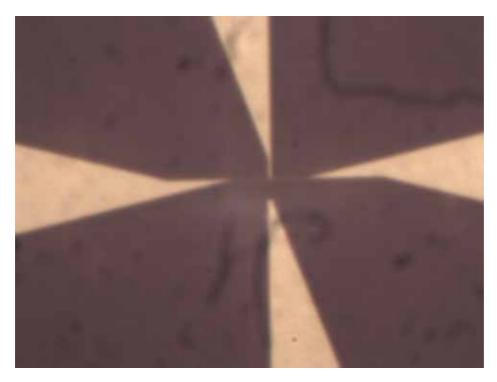


Figure 3.3 OM image of the side-gated NWFET.

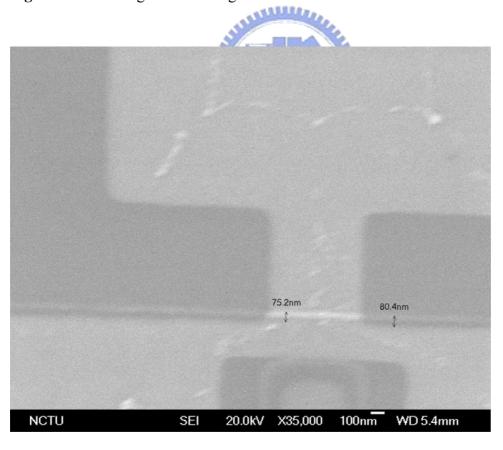


Figure 3.4 SEM image of 80nm width side-gated silicon nanowire.

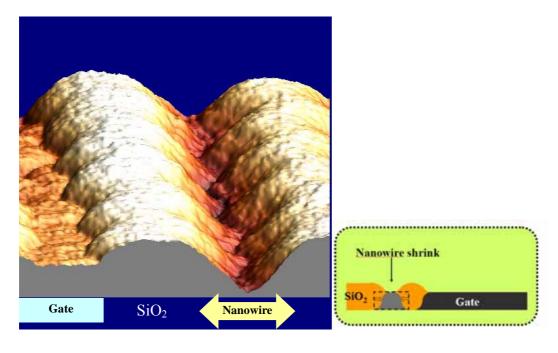


Figure 3.5 AFM image of 80nm width side-gated silicon nanowire.

3.2.2 . Covalent Attachment of the Capture DNA to the Nanowire

For the purpose of biosening, the nanowire surface has to modify to attach DNA. The silicon nanowire surface was first modified into the form of amino group using APTES (3-amino-propyl-triethoxy-silane). Samples were prepared by following three main processes^[2]:

(1) Silicon nanowire surface pre-clean.

First, samples were rinsed with D.I. water. Second, cleaning the patterned wafer with fresh-prepared piranha solution ($H_2O_2/H_2SO_4=1:3$) for 1 hour at 85 . Then washed sample by D.I. water.

(2) Immobilization of APTES and glutaraldehyde linker.

The samples were immersed to 5% APTES (3-amino-propyl-triethoxy -silane) aqueous solution for 75mins at room temperature which were titrated to pH3.5 by HCl. Then, rinse with D.I. water and dry with hot baking at 120 . After baking, let sample immersed in the linker solution, 2.5 % glutaraldehyde, [3]

for 1hr at room temperature.

(3) Single strand DNAs immobilized.

Covalent immobilization was used to bind the terminal 5' amine group of the oligonuclcotide to the carbonyl group on the surface. The procedure was preparing solution of water-soluble 10mM HEPES (4-(2-hydroxyethyl)-1-piperazineethanesulfonic acid, J.T. Baker Chem. Co.) and 5 mM EDTA buffer (Ethylene-Diamine-Tetra-Acetate) to adjust the above solution to pH 6.6 (i.e., HEPES buffer). Mixing the solution with 10nM single stranded DNA named capture-DNA, and the wafers were immersed in the mixture solution for 16 hours to ensure the complete bonding. After immobilization, DI water was used to wash the wafer, purged the sample with N₂ and dried with hot baking. A fluorescence-labeled single stranded DNA was prepared for control experiment, and the evidence of DNA existence on silicon nanowire is characterized under fluorescence microscope in Figure 3.6.

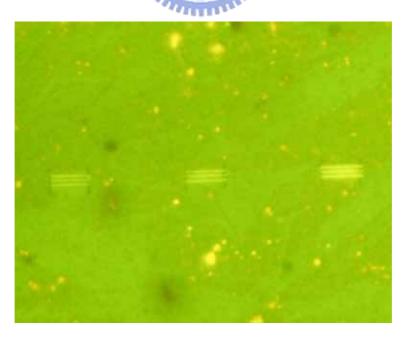


Figure 3.6 Fluorescence microscope image to ensure DNA existence on silicon nanowires.

3.2.3 . Complementary and Non-complementary ssDNA Detection

After surface modification and capture DNA bonding procedure above, another

strand of DNA named target DNA was applied to hybridize with capture DNA. The

sequences of target DNA are both complementary and mismatch to capture DNA.

Schematic diagram of complementary and mismatch DNA sequences were illustrated

in Figure 3.7. The 30-mer target DNA (10 nM) was deaerated in prepared HEPES

buffer. Next, the wafers were immersed in the buffer about 8 hours for DNA detection.

Followed, washing with the DI water to remove excesses target DNA and drying

under N₂. The resulting chip was washed with DI water again to ensure the target

DNA and capture DNA hybridization. Then, chips were immersed to DI water for

seconds and dried by N₂ purge, and put into a low vacuum chamber for preservation.

A fluorescence-labeled single stranded target DNA was prepared for control

experiment, and the evidence of DNA existence on silicon nanowire is measured

under fluorescence microscope in Figure 3.8.

Linker:

APTES and glutaraldehyde

Capture DNA:

5'-AAATATATTA-TTACT**CTTGA**-GGTCTCTGTG-3'

Complementary DNA:

3'-TTTATATAAT-AATGA**GAACT-**CCAGAGACAC-5'

Noncomplementary DNA: 3'-TTTATATAAT-AATGA**TGCCG**-CCAGAGACAC-5'

Figure 3.7 The schematic of linker and DNA sequences.

32

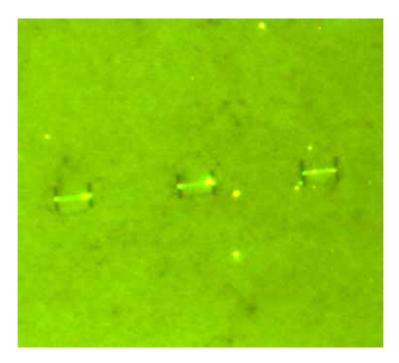


Figure 3.8 Fluorescence microscope image to ensure target DNA hybridization with the capture DNA on silicon nanowires.

The electrical behaviors of the DNA sensors were characterized using the HP 4156A semiconductor parameter analyzer. We measured silicon nanowire I_{DS} - V_{G} curve in every immobilized step, and we found the significant change of electrical signal. In our experiment, not only measured the I_{DS} - V_{G} curve of complementary DNA, but also mismatch DNA. After electrical measurement was done, the chips were washed by 60°C and 72°C DI water to denature the complementary hybridization double stranded DNA. We found I_{DS} - V_{G} curves having distinct difference from target DNAs. The electrical characteristics were again measured. The overall procedure is depicted in Figure 3.9. Finally, the result and discussion of the fabricated biosensors will show in next chapter.

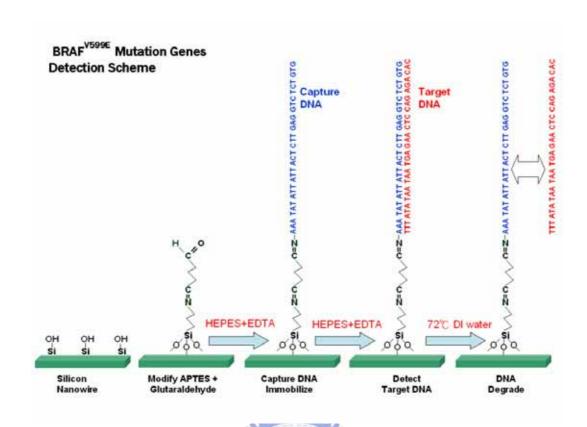


Figure 3.9 The schematic image of overall modification and DNA detection

procedure.

Chapter 4: Results and Discussion

Side-gated silicon nanowire field effect transistors (NWFETs) have been successfully fabricated on silicon-on-insulator wafer. The I_{DS} - V_{DS} curve of the nanowire FET can be controlled by applying side-gate voltage (V_G). The electrical behaviors of the nanowire device and DNA sensors were characterized using the HP 4156A semiconductor parameter analyzer at room temperature. Besides, ICS (Interactive Characterization Software) software is used to calculate some important electrical parameters of SOI devices. Before sample measurements, the noise level of the electrical analyzer is around 50 fA during the stressing voltage in Figure 4.1.

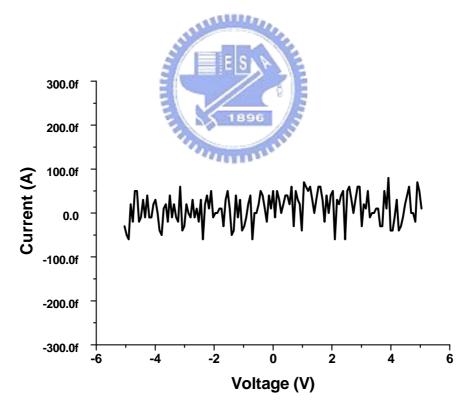


Figure 4.1 Noise level of HP-4156 semiconductor analyzer

4.1 Physical and Electrical Property of Side-gated NWFETs

Figure 4.2 displays the side-gated field effect transistor structure of silicon nanowire. The length of nanowire ranges from 100nm to 3 μ m and the width ranges from 80nm to 300nm.

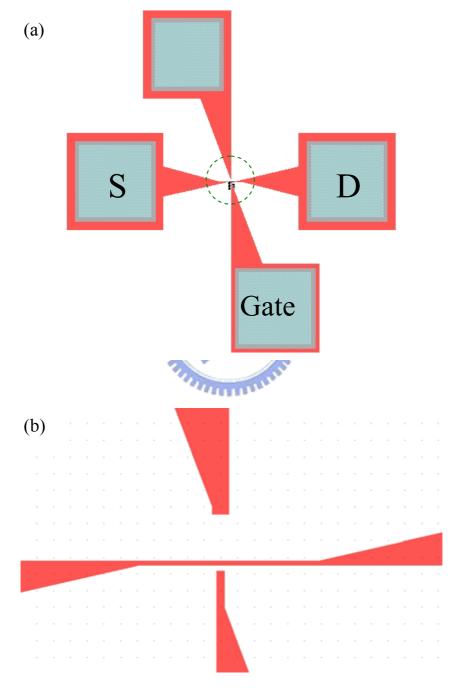


Figure 4.2 (a) Top-view layout of a side-gated NWFET (b) Amplification of the area dotted in (a)

The ED factor (energy vs dose) in e-beam lithography may affect the wire width and length to deviate from the original design to a certain extent. After comparison with our design layout, we record the length and width of the practical nanowire by SEM in Figure 4.3-1 and 4.3-2.

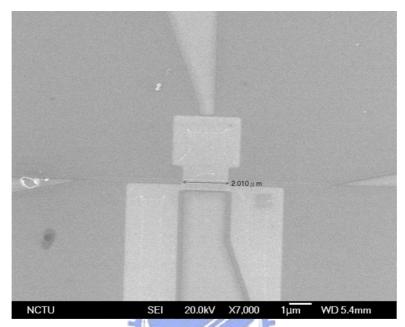


Figure 4.3-1 SEM images of side-gated NWFET with channel length = 2μ m

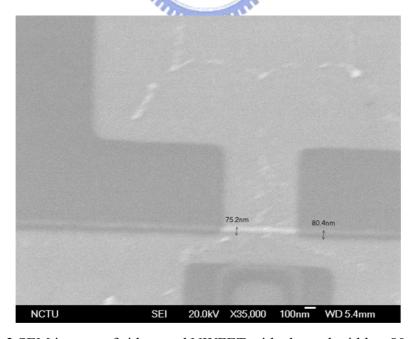


Figure 4.3-2 SEM images of side-gated NWFET with channel width = 80nm

Like general metal oxide semiconductor field effect transistors (MOSFETs), we use gate to control the energy barrier and the on/off state. As a n-channel FET, the gate voltage (V_G) is applied from negative to positive direction to induce negative charges in the channel. When the gate voltage is low, the high quality p-n junction can guarantee the very low leakage current (I_{off}) at the picoampere (pA) level. When the gate voltage is high enough to construct the conducting inversion layer and "open" the channel, the drain-to-source current (I_{DS}) inceases obviously and the gate voltage is called "threshold voltage (V_{th})". Finally, the currents (I_{on}) reach different saturations with different drain-to-source voltages (V_{DS}). The electrical characteristics of side-gated NWFET (300nm width and 3 μ m length) is shown in Figure 4.4-1 and 4.4-2.

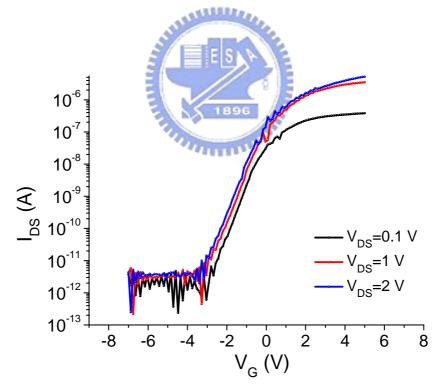


Figure 4.4-1 The I_{DS} - V_G characteristic of the side-gated NWFETs. The applied drain -to-source voltage is 0.1, 1, and 2V, respectively.

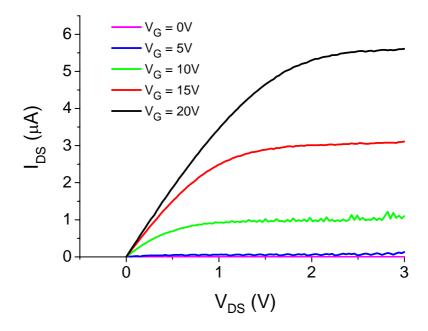


Figure 4.4-2 The I_{DS}-V_{DS} characteristic of the side-gated NWFET. The applied gate voltage is 0, 5, 10, 15, and 20V, respectively.

4.1.1 Determination of the Threshold Voltage

There exist numerous methods^[1~23] to extract the value of threshold voltage, V_{th} , which is the most important parameter of semiconductor devices. In many MOSFETs, the method to determinate the threshold voltage is *constant drain current method*.^[2] This method is widely used in industry because of its simplicity. The threshold voltage is usually defined at a fixed drain current scaled by the device dimensions:

$$I_{DT} = I_{DN} \times \frac{W}{I_{L}}$$

I_{DT} is threshold current to determine the threshold voltage,

I_{DN} is normalized threshold current defined as 10nA in this thesis,

W is channel width,

L is channel length,

4.1.2 Determination of the Subthreshold Swing

Subthreshold swing S.S. (V/dec) is a typical parameter to describe the control ability of gate toward channel. It is defined as the amount of gate voltage required to increase/decrease drain current by one order of magnitude. The subthreshold swing should be independent of drain voltage and gate voltage. However, in reality, the subthreshold swing might increase with drain voltage due to short-channel effects such as charge sharing, avalanche multiplication, and punchthrough-like effect. The subthreshold swing is also related to gate voltage due to undesirable factors such as serial resistance and interface state. In this experiment, the subthreshold swing is defined as one-half of the gate voltage required to decrease the threshold current by two orders of magnitude. The threshold current is specified to be the drain current when the gate voltage is equal to the threshold voltage.

4.1.3 Determination of On/Off Current Ratio

Drain On/Off current ratio is another important factor for FETs. High On/Off ratio represents not only large turn-on current but also small off current (leakage current). There are many methods to describe the on and off current. The practical one is to define the maximum current as on current and the minimum leakage current as off current.

4.1.4 Determination of the Field-effect Mobility

The field-effect mobility (μ_{FE}) is determined from the transconductance g_m at low drain voltage. The transfer I-V characteristics of FETs can be expressed as

$$I_{D} = \mu_{FE} C_{ox} \frac{W}{L} \left[(V_{G} - V_{TH}) V_{D} - \frac{1}{2} V_{D}^{2} \right]$$

where

Cox is the gate oxide capacitance per unit area,

W is channel width,

L is channel length,

V_{TH} is the threshold voltage.

If V_D is much smaller than $V_G\text{-}V_{TH}$ (i.e. $V_D << V_G\text{-}V_{TH}$) and $V_G > V_{TH}$, the drain current can be approximated as:

$$I_{D} = \mu_{FE} C_{ox} \frac{W}{L} (V_{G} - V_{TH}) V_{D}$$

The transconductance is defined as

$$g_{m} = \frac{\partial I_{D}}{\partial V_{G}} \Big|_{V_{D} = const.} = \frac{WC_{ox} \mu_{FE}}{L} V_{D}$$

Therefore, the field-effect mobility can be obtained by

$$\mu_{\text{FE}} = \frac{L}{C_{\text{ox}}WV_{\text{D}}}g_{\text{m}}$$

Table 4.1 Device parameters with channel width = 300nm and channel length = 3μ m

Device Parameters	The amounts extracted at V _{DS} =0.1V
V _{th} , threshold voltage	-1.22V
S.S., subthreshold swing	0.61V/dec
I _{on} /I _{off} , On/Off current ratio	2.86×10 ⁵
g _{m,} transconductance	7.50×10 ⁻⁸ S
μ_{FE} , field-effect mobility	$652.17 \frac{\text{cm}^2}{\text{V} \cdot \text{s}}$

4.1.5 Drain Induced Barrier Lowering (DIBL)^[24]

In a short channel MOSEFT, when the drain-to-source voltage (V_{DS}) increase from the linear region toward the saturation region, its threshold voltage becomes smaller. This effect is called drain-induced barrier lowering (DIBL). The effect is also observed in short channel silicon NWFETs. When the gate voltage is below V_{th} , the p-Si substrate forms a potential barrier between n^+ source and drain and limits the current flow from source to drain. For a device operated in the saturation region, the depletion-layer width of the drain junction is significantly wider than that of the source junction (Figure 4.5). [25] Therefore, the energy barrier from source to channel is pulled down and the threshold voltage of short channel becomes smaller than long channel when V_{DS} increase (Figure 4.6 and Table 4.2).

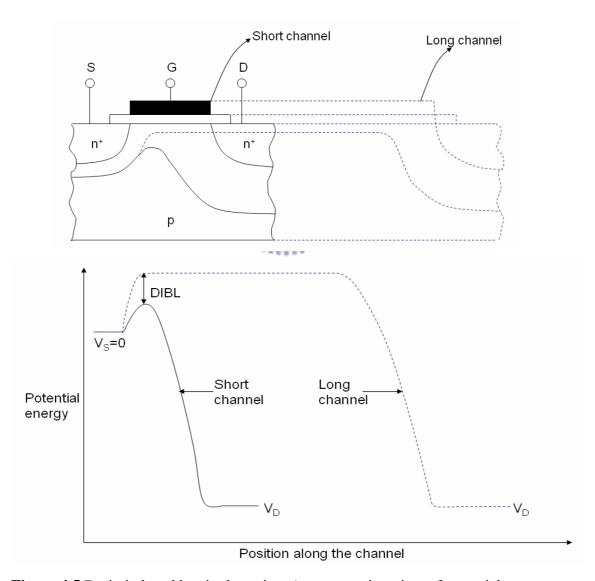


Figure 4.5 Drain induced barrier lowering. A cross-section view of potential energy distribution along the long and short channels in MOSFETs.

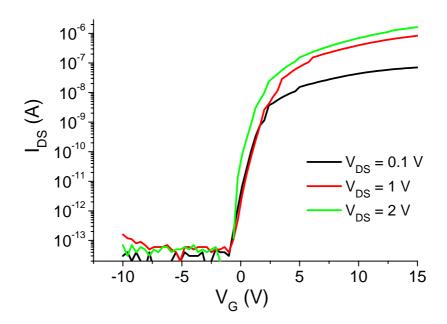


Figure 4.6-1 The I_{DS} - V_G characteristic of the side-gated NWFETs of channel length = 800nm. The applied drain -to-source voltage is 0.1, 1, and 2V, respectively.

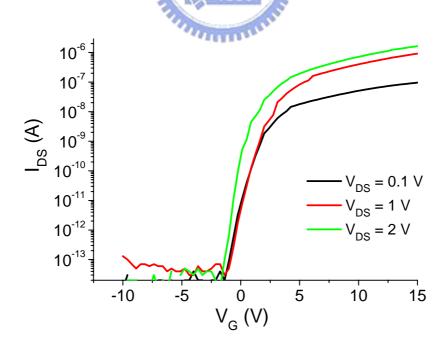


Figure 4.6-2 The I_{DS} - V_G characteristic of the side-gated NWFETs of channel length = 600nm. The applied drain -to-source voltage is 0.1, 1, and 2V, respectively.

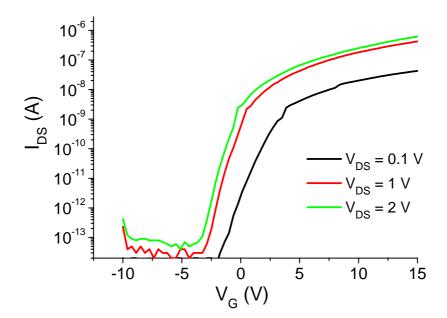


Figure 4.6-3 The I_{DS} - V_G characteristic of the side-gated NWFETs of channel length = 400nm. The applied drain -to-source voltage is 0.1, 1, and 2V, respectively.

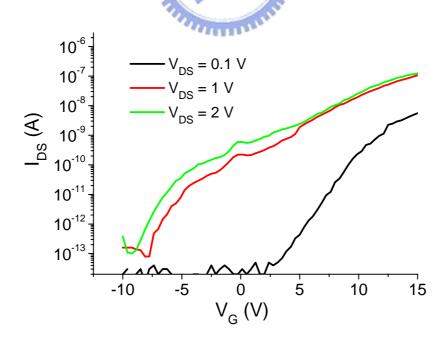


Figure 4.6-4 The I_{DS} - V_G characteristic of the side-gated NWFETs of channel length = 200nm. The applied drain -to-source voltage is 0.1, 1, and 2V, respectively.

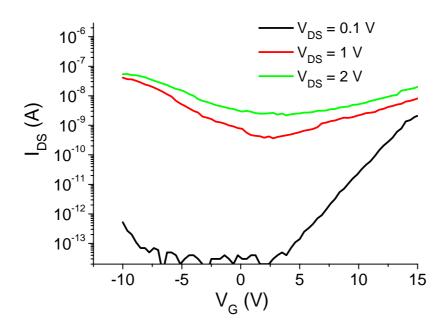


Figure 4.6-5 The I_{DS} - V_G characteristic of the side-gated NWFETs of channel length = 100nm. The applied drain -to-source voltage is 0.1, 1, and 2V, respectively.

1896

Table 4.2 Threshold voltage variation of DIBL effect

Channel Length, L (nm)	Threshold Voltage Variation, ΔV_{th} (V _{DS} from 0.1V to 2V)		
(Channel Width = 300nm)			
800	1.0		
600	1.5		
400	4.0		
200	10.1		
100	12.2		

4.1.6 Kink Effect^[24]

During devices operation, a high field near the drain could induce impact ionization effect. Majority carriers, holes in the p-substrate for an n-channel FETs, generate by impact ionization will be stored in the substrate, since there is no substrate contact with drain to away these charges. Therefore the substrate potential will be changed and will result in a reduction of the threshold voltage. This, in turn, may cause an increase or a kink in the current-voltage characteristics. The kink phenomenon is shown in Figure 4.7. This kink effect is especially dramatic for n-channel devices, because of the higher impact-ionization rate of electrons. The kink effect can be eliminated by forming a substrate contact to the source of the transistor. The excess drain currents (ΔI_{DS}) with different channel lengths (\leq 400nm) and different gate voltages are shown in Table 4.3, Figure 4.8 and 4.9, respectively.

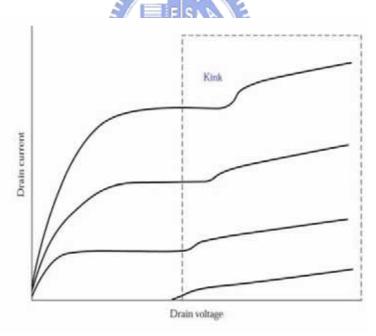


Figure 4.7 The kink effect in the output characteristics of an n-channel SOI MOSFET

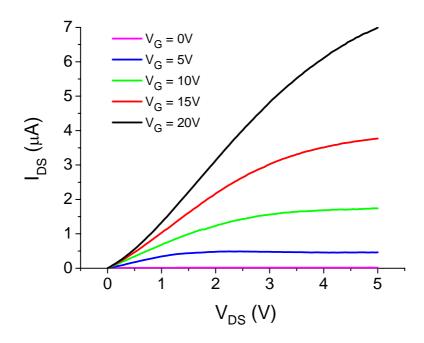


Figure 4.8-1 The I_{DS} - V_{DS} characteristic of the side-gated NWFETs of channel length

= 800nm. The applied gate voltage is 0, 5, 10, 15, and 20V, respectively.

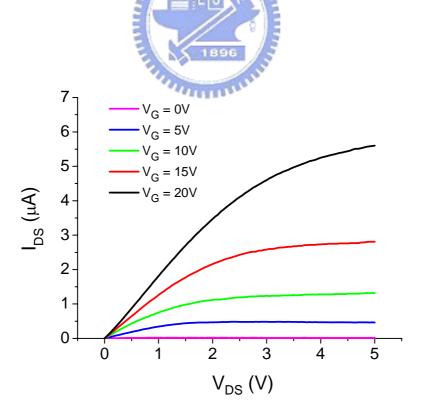


Figure 4.8-2 The I_{DS} - V_{DS} characteristic of the side-gated NWFETs of channel length = 600nm. The applied gate voltage is 0, 5, 10, 15, and 20V, respectively.

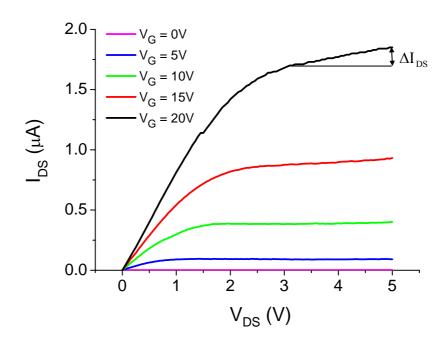


Figure 4.8-3 The I_{DS} - V_{DS} characteristic of the side-gated NWFETs of channel length = 400nm. The applied gate voltage is 0, 5, 10, 15, and 20V, respectively.

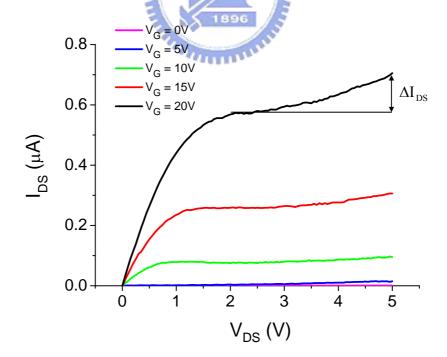


Figure 4.8-4 The I_{DS} - V_{DS} characteristic of the side-gated NWFETs of channel length = 200nm. The applied gate voltage is 0, 5, 10, 15, and 20V, respectively.

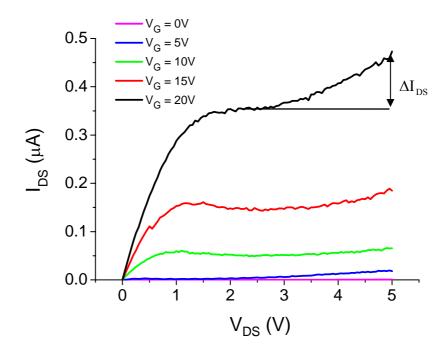


Figure 4.8-5 The I_{DS} - V_{DS} characteristic of the side-gated NWFETs of channel length = 100nm. The applied gate voltage is 0, 5, 10, 15, and 20V, respectively.

Table 4.3 The excess drain currents of kink effect from $L = 100 \sim 400$ nm, $V_G = 5 \sim 20$ V with W = 300nm.

Excess d	Irain currents,	Gate voltage, V _G				
I	_{DS} (µ A)	A) 20 V		10 V	5 V	
Channel	400 nm	0.140	0.074	0.018	0	
Length,	200 nm	0.132	0.047	0.019	0.01	
L	100 nm	0.116	0.039	0.015	0.01	

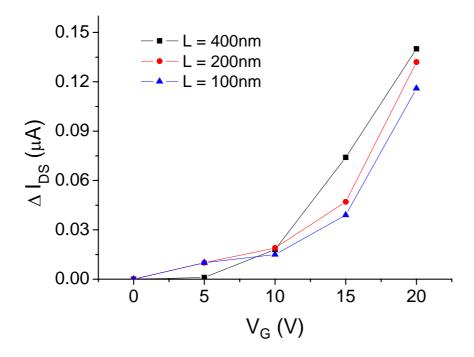


Figure 4.9 Excess drain current (ΔI_{DS}) versus gate voltage (V_G) at channel length = 100, 200 and 400nm.

4.2 Detection Concept

The threshold voltage of a MOSFET is usually defined as the gate voltage where an inversion region forms in the substrate of the transistor. In Figure 4.10,^[26] the substrate of the nMOSFET is composed of p-type silicon which has more positively charged electron holes compared to electrons. When a voltage is applied on the gate, an electric field causes the electrons in the substrate to become concentrated at the region of the substrate nearest the gate causing the concentration of electrons to be equal to that of the electron holes, creating a depletion region.

If the gate voltage is below the threshold voltage, the transistor is turned off and ideally there is no current from the drain to the source of the transistor. If the gate voltage is larger than the threshold voltage, the transistor is turned on, due to there being more electrons than holes in the substrate near the gate and creating a channel

where current can flow from drain to source region. This situation is called the strong inversion.

As Figure 4.11 shows, we simply consider the gate voltage can be regarded as a charge supply, and a charging molecular is bonding to the nanowire. If a molecule with electrical charge adsorbed onto the nanowire surface, this causes electric field either to accumulate or to be depleted within the channel surface, depending on the charge on the bound molecule and on the charge carriers is in the same or opposite sign. DNA is suggested to be negative charged, [27] and more gate voltage should be applied to get the inversion layer. So, the threshold voltage shifted positively. Thus, we can measure the threshold voltage shift to make sure the binding of the target DNA and capture DNA for the purpose of detection.



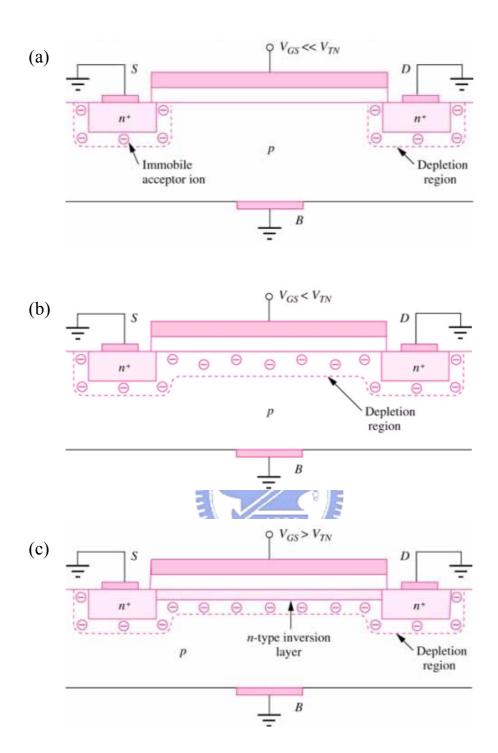


Figure 4.10 NMOS transistor: qualitative I-V behavior. (a) $V_{GS} << V_{TN}$: Only small leakage current flows. (b) $V_{GS} < V_{TN}$: Depletion region formed under gate merges with source and drain depletion regions. No current flows between source and drain. (c) $V_{GS} > V_{TN}$: Channel formed between source and drain. If $V_{DS} > 0$, finite I_D flows from drain to source

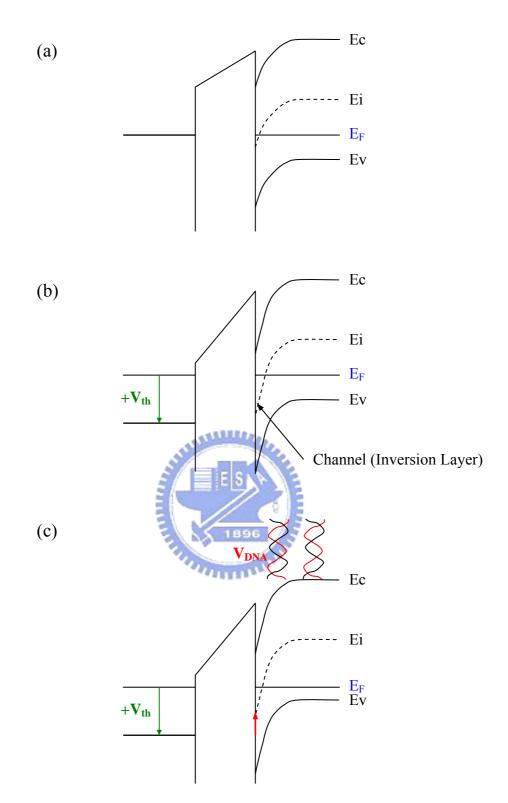


Figure 4.11 Surface potential energy scheme to show the DNA detection concept.

(a)No gate voltage was applied. (b) Threshold voltage was applied to get the inversion layer. (c) After surface DNA modification regarded as a negative gate voltage, more gate voltage should be applied to get the inversion layer, and the threshold voltage shifted.

4.3 Sensing of Multi-Steps-APTES Immobilization, DNA Hybridization and Dehybridization

At last section, the side-gated silicon NWFET device has been fabricated. Based on the charge effect, the NWFET device was used as a biosensor to detect the chemical molecules. In this thesis, we used amino-propyl-triethoxy-silane (APTES) to modify the surface condition around the silicon nanowire. The hydroxyl molecules were replaced by the ethoxy side of APTES that the surface voltage of silicon nanowire was changed from negative to positive. The I_{DS}-V_G curve of each chemical treatment is measured and the concept diagram of the experiment flow is illustrated in Figure 4.12. Figure 4.13 is the original I_{DS}-V_G characteristic curve of immobilized steps (1) to (5). In the following section, we always transform I-V characteristic curve to threshold voltage v.s immobilized steps diagram. The threshold voltage of 300nm width and 3µm length is calculated at (1) silicon nanowire, (2) APTES modification, (3) capture DNA attached, (4) hybridization of target DNA and (5) denaturation of in Figure 4.15. Firstly, the threshold voltage has little negative DNAs at 60 and 72 shift because APTES modification on nanowire affects the surface of nanowire toward positive charge rich and the depletion of positive charge in silicon nanowire. Secondly, upon capture DNA attached, the threshold voltage shifts to positive distinct. In this step, negative charge characteristic of DNA is formed due to negative gate voltage applied. The nanowire can be a good negative molecular indicator because of the high surface-to-volume ratio of the nanostructures, their electronic I-V curve may be sensitive enough to the surface species that single-molecule detection becomes possible. Thirdly, the target DNA was applied to hybridize with capture DNA. The amount of threshold voltage shifts further. It can be explained that the more negative charges are applied on the nanowire. But the threshold voltage shift of target DNAs hybridization does not equal to that of capture DNAs immobilization on the silicon

nanowire. Because the target DNAs maybe not hybridize with capture DNAs completely. The shift of threshold voltage is about 0.86V. From the results of threshold voltage shift during DNA hybridization, the potential of applying this type of nanowire to biomolecular sensing is possible. For the control of experiment, a denaturation process is also tested. Hybridized DNAs are washed at 72 with DI water. When the denaturation occurs, target DNA will leave capture DNA and be stripped out by washing. The nanowire device restores to near the original threshold voltage value once only capture DNAs attachment after washing with DI water. This test depicts the positively shift of threshold voltage at hybridization step is contributed by the target DNA.

An alternate control of experiments by using with noncomplementary DNAs as target DNAs is performed. When we take mismatch target DNAs to hybridize with capture DNAs on silicon nanowire, there is also a positive shift (\sim 0.72V) between the measured threshold voltages. However, the mismatch target DNAs are stripped away after washing with 60 DI water. The original I_{DS} - V_G characteristic curve of immobilized steps is shown in Figure 4.14. We compare the threshold voltage of complementary DNAs with noncomplementary DNAs after 60 water stripping, and we can easily find that only the threshold voltage of noncomplementary DNAs is shifted back to original value as only capture DNAs attachment in step (4) of Figure 4.16. If target DNAs are not complementary with the capture DNAs, it will be washed away out by 60 DI water easily.

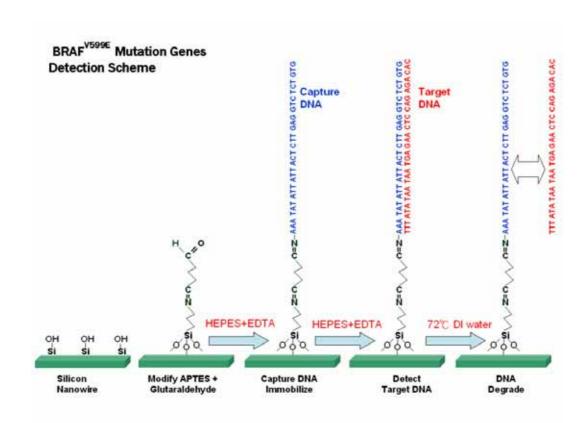


Figure 4.12 The schematic image of overall modification and DNA detection

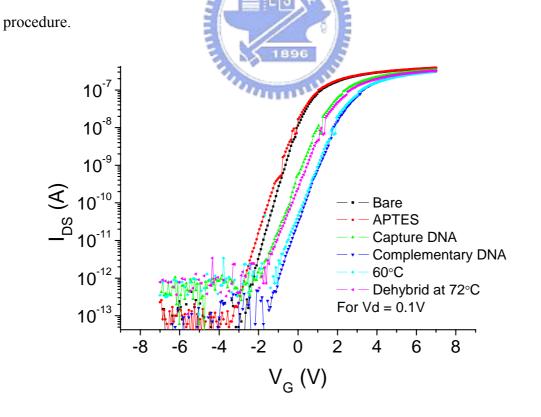


Figure 4.13 The I_{DS} - V_G curve of complementary DNA detection.

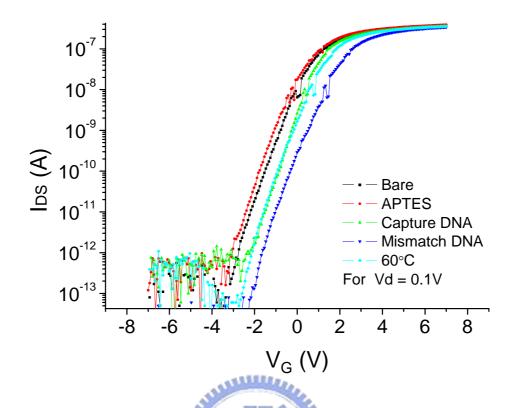


Figure 4.14 The I_{DS} - V_G curve of non-complementary DNA detection.

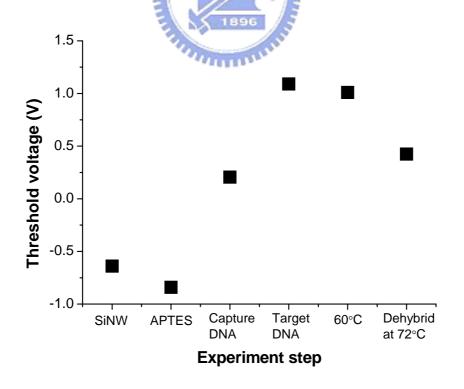


Figure 4.15 The threshold voltage of immobilized step $(1)\sim(5)$.

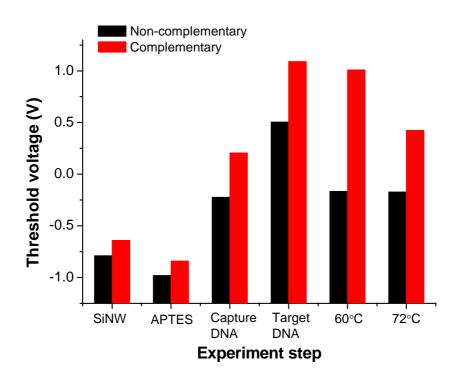


Figure 4.16 The threshold voltage of immobilized steps which compare complementary and non-complementary DNAs.

Chapter 5: Conclusions

In conclusion, a novel side-gated Si NWFET for sensing BRAF mutation gene was fabricated by integrating the top-down complementary metal oxide semiconductor (CMOS) field effect transistor compatible technology, including the conventional LOCOS isolation process and electron-beam writing. The shrinking nanowire with higher surface-to-volume ratio and individual side gate for integration are achieved by the LOCOS process. Our side-gated devices which were fabricated using silicon-on-insulator (SOI) wafers provide a good quality of SiO₂ gate dielectric. The device demonstrates exhibits lower leakage current and excellent field effect properties than those with air dielectric. The width of shrinking nano-channel by the LOCOS "bird's beak" can be 80 nm or thinner practically. The I_{DS} - V_G characteristic of the NWFETs exhibits about five orders of magnitude on I_{on}/I_{off}, and the threshold voltage shifts positively to 0.86V after hybridization of 10 picomolar concentrations of BRAF v599E mutation gene. The results show that the nanowire-based device acts as a label-free, highly sensitive and selective biosensor for mutation gene sensing. In addition, our approach offers the possibility of highly parallel detection of multiple chemical and biological species with local control of individual elements in a single integrated chip in the future.

References

Chapter 1

- 1. International Technology Roadmaps for Semiconductors ITRS, 2006 Edition.
- 2. Lithography ITRS, 2006.
- 3. S. Y. Chou, P. R. Krauss, and P. J. Renstrom, Science 272, 85 (1996).
- S. Y. Chou, P. R. Krauss, and P. J. Renstrom, J. Vac. Sci. Technol. B 14, 4129 (1996).
- 5. S. Y. Chou, Mrs Bulletin **26**, 512 (2001).
- T. Tsutsumi, E. Suzuki, K. Ishii, H. Hiroshima, M. Yamanaka, I. Sakata, S. Hazra
 K. Tomizawa, Superlattices Microstruct. 28, 453 (2000).
- 7. M. A. Kastner, Rev. Mod. Phys. 64, 849 (1992).
- 8. E. Leobandung, L. J. Guo, Y. Wang, and S. Y. Chou, Appl. Phys. Lett. **67**, 938 (1995).
- 9. X. F. Duan, Y. Huang, Y. Cui, J. F. Wang, and C. M. Lieber, Nature **409**, 66 (2001).
- P. A. Smith, C. D. Nordquist, T. N. Jackson, T. S. Mayer, B. R. Martin, J. Mbindyo, and T. E. Mallouk, Appl. Phys. Lett. 77, 1399 (2000).
- 11. M. R. Diehl, S. N. Yaliraki, R. A. Beckman, M. Barahona, and J. R. Heath, Angew. Chem. Int. Edit. 41, 353 (2001).
- 12. Y. Huang, X. F. Duan, Q. Q. Wei, and C. M. Lieber, Science 291, 630 (2001).
- 13. B. Messer, J. H. Song, and P. D. Yang, J. Am. Chem. Soc. 122, 10232 (2000).
- 14. D. Whang, S. Jin, Y. Wu, and C. M. Lieber, Nano Lett. 3, 1255 (2003).
- 15. D. Whang, S. Jin, and C. M. Lieber, Nano Lett. 3, 951 (2003).
- S. Jin, D. M. Whang, M. C. McAlpine, R. S. Friedman, Y. Wu, and C. M. Lieber,
 Nano Lett. 4, 915 (2004).

- 17. A. Tao, F. Kim, C. Hess, J. Goldberger, R. R. He, Y. G. Sun, Y. N. Xia, and P. D. Yang, Nano Lett. 3, 1229 (2003).
- J. Kong, N. R. Franklin, C. Zhou, M. G. Chapline, S. Peng, K. Cho, and H. Dai,
 Science 287, 622 (2000).
- 19. K. Besteman, J. Lee, F. Wiertz, H. Heering, and C. Deeker, Nano Lett. 3, 727 (2003).
- 20. J. Li, Y. Lu, Q. Ye, M. Cinke, J. Han, and M. Meyyappan, Nano Lett. 3, 929 (2003).
- 21. Y. Cui, Q. Q. Wei, H. K. Park, and C. M. Lieber, Science 293, 1289 (2001).
- 22. M. Law, H. Kind, F. Kim, B. Messer, and P. Yang, Angew. Chem., Int. Ed. **41**, 2405 (2002).
- 23. C. Li, D. H. Zhang, X. L. Liu, S. Han, T. Tang, J. Han, and C. W. Zhou, Appl. Phys. Lett. **82**, 1613 (2003).
- 24. Z. Fan, D. Wang, P. C. Chang, W. Y. Tseng, and J. G. Lu, Appl. Phys. Lett. 85, 5923 (2004).
- 25. Y. Chen, X. Wang, S. Erramilli, P. Mohanty, and A. Kalinowski, Appl. Phys. Lett. **89**, 223512 (2006).

Chapter 2

- 1. Y. Cui, Q.Q.Wei, H. Park, and C.M. Lieber, Science 293, 1289 (2001).
- 2. Y. Huang, X.F. Duan, Q.Q. Wei, and C.M. Lieber, Science **291**, 630 (2001).
- 3. J. Hahm, and C.M. Lieber, Nano Lett. 4, 51 (2004).
- 4. F. Patolsky, G.F. Zheng, O. Hayden, M. Lakadamyali, X.W. Zhuang, C.M. Lieber, PNAS **101**, 14017 (2004).
- W. U. Wang, C. Chen, K. H. Lin, Y. Fang, and C. M. Lieber, PNAS 102, 3208 (2005).

- O. H. Elibol, D. Morisette, D. Akin, J. P. Denton, and R. Bashir, Appl. Phys. Lett.
 83, 4613 (2003).
- 7. P. J. Schubert and G. W. Neudeck, IEEE Electron Device Lett. 11, 181 (1990)
- 8. Z. Li, Y. Chen, X. Li, T. I. Kamins, K. Nauka, and R. S. Williams, Nano Lett. **4** 245 (2004).
- Z. Li, B. Rajendran, T. I. Kamins, X. Li, Y. Chen, R. S. Williams, Appl. Phys. A 80, 1257 (2005).
- J. T. Sheu, C. C. Chen, P. C. Huang, Y. K. Lee, and M. L. Hsu, Jpn. J. Appl. Phys.
 44, 2864 (2005).
- F. H. Ko, Z. H. Yeh, C. C. Chen and T. F. Liu, J. Vac. Sci. Technol. B 23 3000
 (2005)

Chapter 3

- 1. National Nano Device Laboratories. http://www.ndl.gov.tw/
- 2. H. Yuan, W. M. Mullett, J. Pawliszyn, Analyst 126, 1456 (2001).
- 3. A. Simon, T. Cohen-Bouhacina, M. C. Porté, J. P. Aimé, and C. Baquey, Journal of Colloid and Interface Science **251**, 278 (2002).

Chapter 4

- Semiconductor material and device characterization, 2nd edition, written by D. K.
 Schroeder, Wiley, pp.183 (1998).
- 2. K. Terada, K. Nishiyama, and K. I. Hatanaka, Solid-State Electron 45, 35 (2001).
- 3. J. J. Liou, A. Ortiz-Conde, and F. J. Garcia Sanchez, In: Proceedings of IEEE HKEDM, Hong Kong, 31 (1997).
- 4. A. Ortiz-Conde, F. J. Garcia Sanchez, J. J. Liou, Acta Cientifica Venezolana **51**, 176 (2000).

- 5. X. Zhou, K. Y. Lim, and D. Lim, IEEE Trans Electron Dev, **46**, 807 (1999).
- 6. X. Zhou, K. Y. Lim, and W. Qian, Solid-State Electron, 45, 507 (2001).
- 7. H. S. Wong, M. H. White, T. J. Krutsick, R. V. Booth, Solid-State Electron, 30, 953 (1987).
- 8. S. Jain, IEE Proc Cir Dev Syst, 135 (1988).
- 9. G. Ghibaudo, Electron Lett **24**, 543 (1988).
- W. Fikry, G. Ghibaudo, H. Haddara, and S. Cristoloveanu, Electron Lett 31, 762 (1995).
- M. Sasaki, H. Ito, and T. Horiuchi, In: Proceedings of IEEE International Conference on Microelectronic Test Structures (ICMTS), 139 (1996).
- 12. S. Hardillier, C. Mourrain, M. J. Bouzid, and G. Ghibaudo, In: Proceedings of IEEE International Conference on Microelectronic Test Structures (ICMTS), 63 (1997).
- C. Mourrain, B. Cretu, G. Ghibaudo, and P. Cottin, In: Proceedings of the 2000 International Conference on Microelectronic Test Structures (ICMTS), 181 (2000).
- M. Tsuno, M. Suga, M. Tanaka, K. Shibahara, M. Miura-Mattausch, and M. Hirose, In: Proceedings of Asia and South Pacific Conference, 111 (1998).
- 15. M. Tsuno, M. Suga, M. Tanaka, K. Shibahara, M. Miura-Mattausch, and M. Hirose, IEEE Trans Electron Dev **46**, 1429 (1999).
- 16. F. Corsi, C. Marzocca, and G. V. Portacci, Electron Lett, 29, 1358 (1993).
- 17. C. C. McAndrew and P. A. Layman, IEEE Trans Electron Dev ED-39, 2298 (1992).
- 18. P. R. Karlsson and K. O. Jeppson, IEEE Trans Semicond Manuf 9, 215 (1996).
- 19. K. Aoyama, Simul Semicond Dev Process 6, 118 (1995).
- 20. A. Ortiz-Conde, E. Gouveia, J. J. Liou, M. R. Hassan, F. J. Garcia Sanchez, G.

- De Mercato, and W. Wang. IEEE Trans Electron Dev 44, 1523 (1997).
- 21. F. J. Garcia Sanchez, A. Ortiz-Conde, G. D. Mercato, J. A. Salcedo, J. J. Liou, and Y. Yue, Solid-State Electron 44, 673 675 (2000).
- A. Ortiz-Conde, F. J. Garcia Sanchez, A. Cerdeira, M. Estrada, D. Flandre, and J. J. Liou, Shanghai, China., 887 (2001).
- F. J. Garcia Sanchez, A. Ortiz-Conde, A. Cerdeira, M. Estrada, D. Flandre, and J. J. Liou, IEEE Trans Electron Dev 49, 82 (2002).
- Semiconductor devices physics and technology, second edition, written by S.M
 Sze, pp. 199-213
- Solid state electronic devices, fifth edition, written by B. G. Streetman and S.
 Banerjee, pp.360
- 26. Microelectronic circuit design, written by R. C. Jaeger, pp.120
- 27. B. Liu, G. C. Bazan, Proc. Natl. Acad. Sci. U.S.A. 102, 589 (2005).

1896