Chapter 1

Introduction

1.1 General Background and Motivation

The heteroepitaxial growth of III-V materials on Si substrate has attracted great attention in recent years due to its potential of integrating Si and III-V based devices on the same platform. The physical gate length of Si transistors used in current 90-nm generation node is about 50 nm. The size of transistor will reach 10 nm in 2011. In order to extend Moore's law well into next decade, Si-CMOS incorporated with III-V semiconductor compound materials in the device structure is one of the promising solutions for the CMOS technology. III-V materials have advantages over Si for some applications due to its higher electron mobility, wider bandgap as well as direct bandgap. Silicon, however, has several advantages over III-V materials such as larger area integration, SiO_2 coverage, and higher thermal conductivity than most III-V materials.

The main problem to overcome in growing GaAs on Si by heteroepitaxy is the large lattice mismatch of 4% and the difference in the thermal expansion coefficients (63%) of these two materials. To achieve high quality device structure, it is necessary to reduce the dislocations density in the epitaxial GaAs layer. Several methods for reducing the dislocation density have been reported, such as using strained layer superlattice to confine dislocations [2], or using

thermal cycle annealing to reduce threading dislocations. Motorola has reported GaAs MESFETs fabricated on Si substrate using a $SrTiO_3$ buffer layer in a MBE system. However, the $SrTiO_3$ buffer layer is hard to grow in the MBE system.

Recently, one highly sought after heteroepitaxial system has been the monolithic integration of GaAs-based materials on Si. The growth of low threading dislocation density (~ 2 x $10^6 cm^{-2}$) relaxed graded Ge/Ge_xSi_{1-x}/Si heterostructures can bridge the gap between lattice constants by replacing the high mismatch GaAs/Si interface with a low mismatch (< 0.1%) GaAs/Ge interface.

1.2 Outline of the Dissertation

This dissertation covers the study of III-V epitaxial material on Si substrate for high-speed electronic and optioelectron applications and divided into 7 chapters.

In Chapter 2, use of Si^+ pre-ion-implantation on Si substrate to enhance the strain relaxation of the Ge_xSi_{1-x} metamorphic buffer layer for the growth of Ge layer on Si substrate was investigated. Enhanced strain relaxation of the Ge_xSi_{1-x} metamorphic buffer layer on Si substrate was achieved due to the introduction of the point-defects by heavy dose Si^+ ion-implantation. Because of the strain relaxation enhancement and the interface-blocking of the dislocations in the Ge_xSi_{1-x} metamorphic buffer structure, the total thickness of the buffer layers was only 0.45μm. No cross-hatch pattern was observed on the Ge surface and the

dislocation density for the top Ge film was only 7.6×10^{6} cm^{-2} .

In Chapter 3, the growth of epitaxial GaAs on Si substrates for high-speed electronic applications is presented. GaAs metal gate semiconductor field effect transistor (MESFET) structures fabricated on Si substrate with Ge/SiGe metamorphic buffer layers using low pressure metal organic vapor phase (LP-MOVPE) method was investigated. The buffer layer was a $Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}$ metamorphic layer between the Si substrate and the GaAs epitaxial layers. A Ge layer was grown on the top of the buffer layer. The electron mobility in the GaAs of the GaAs/Ge/Si_xGe_{1-x}/Si sample was 2,130cm^2/Vs when the doping concentration of GaAs was $5.45\times10^{17}cm^{-3}$. The diffusion length of Ge into the GaAs layer was about 0.25μm in 6° off (100) toward <110> direction Si substrate. Transmission electron microscopy (TEM) was used to observe the microstructures of the GaAs/Ge/Si_xGe_{1-x}/Si layer grown. Atomic force microscopy（AFM）images were used to measure the surface roughness of the GaAs epitaxial layer. The root mean square (RMS) was 7.35 Å and the average roughness (RA) was 5.81 Å for the GaAs layers grown.

In Chapter 4, the epitaxial growth of the AlGaAs/InGaAs HEMT's on Si substrates was demonstrated with Si^+ pre-ion-implantation on Si substrate and interface-blocking $Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}/Ge_{0.8}Si_{0.2}$ metamorphic buffer. An AlGaAs/InGaAs HEMT structure was grown by low pressure metal organic vapor phase epitaxy (LP-MOVPE) method and the $Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}/Ge_{0.8}Si_{0.2}$ metamorphic structure was grown on the Si substrate with Si^+

pre-ion implantation by ultra high vacuum chemical vapor deposition (UHV-CVD) method. The good quality of the $In_{01.8}Ga_{0.82}As$ HEMT epistructure was attributed to precisely control of the composition of the Ge_xSi_{1-x} metamorphic buffer structures and the thin buffer thickness (1.0μm) achieved. The electron mobility in the $In_{0.18}Ga_{0.82}As$ channel of the HEMT sample was 3,550 cm^2/Vs. After fabrication, the HEMT device demonstrated a saturation current of 150 mA/mm with a transconductance of 155 mS/mm and the breakdown voltage was 3.5V. The well behaved characteristics of the HEMT device on the Si substrate are believed to be due to the very thin buffer layer achieved and the lack of the antiphase boundaries (APBs) formation and Ge diffusion in the GaAs layers.

In Chapter 5. The InAs channel MHEMT grown on the Si substrate using the high quality metamorphic GaAs/Ge/Ge_xSi_{1-x} buffer layer is demonstrated. The InAs channel MHEMT was grown with $Al_{0.5}Ga_{0.5}Sb$ buffer layer grown on the GaAs/Ge/Ge_xSi_{1-x} template with Si substrate that is 6^o off angle toward to [110]. Few misfit dislocations were observed at the interface between AlSb and GaAs layer. It has been speculated that the tilted Si substrate with 6^o off angle toward to [110] provides more nucleation sites and the compressive stress at the interface inhibited the dislocations from climbing resulting in high quality crystalline. The Hall measurement showed that electron mobility InAs MHEMT (27,300 $cm^2/v\text{-}s$) was grown on Si. The strains at the interface and the film quality of the InAs MHEMT grown on Si substrate were characterized by X-ray measurement and TEM analysis. Atomic Force

Microscopy (AFM) was used to investigate the surface morphologies and the formation of APBs on GaAs.

In Chapter 6, self-assembled $In_{0.22}Ga_{0.78}As$ quantum dots (QDs) was grown on Si substrate with Ge/Ge_xSi_{1-x} as buffer layer grown by metal organic vapor phase (MOVPE) method. Transmission electron microscopy (TEM) and atomic force microscopy （AFM）images were used to observe the size and space distribution of the $In_{0.22}Ga_{0.78}As$ QDs grown on the $GaAs/Ge/Ge_xSi_{1-x}/Si$ layer structure. The influence of the growth temperature on the QDs size and density was investigated. For QDs grown at 450℃, the density of the $In_{0.22}Ga_{0.78}As$ dots was estimated to be 1×10^{11} cm^{-2} and the $In_{0.22}Ga_{0.78}As$ QDs thickness was 5 monolayer thick.

Chapter 7 is the conclusion of this dissertation.

Chapter 2

Use of Si^+ pre-ion-implantation on Si substrate to enhance the strain relaxation of the Ge_xSi_{1-x} metamorphic buffer layer for the growth of Ge layer on Si substrate

2.1 Introduction

Due to the higher mobility of its carriers and its narrower band gap as compared to those of silicon (Si), Ge is now emerging as a viable candidate to supplement Si for CMOS devices and 1.3-1.55μm optoelectronics applications [1-2]. As a result, it is essential to develop new methods for the hetero-epitaxial growth of Ge on Si. Such growth is not straightforward because of the large lattice mismatch (4%) between Ge and Si, which limits the quality of the epitaxial layers grown. After reaching a critical thickness, the Ge layer usually contains many misfit and threading dislocations, making it unsuitable for any practical applications.

The large lattice mismatch (4%) results in a high lattice strain at the interface between the Si and Ge layers. This high level of lattice strain can be relaxed by forming a large number of dislocations. This study reports on a high dose (5×10^{15} cm^{-2}) Si^+ pre-ion-implantation technique at an acceleration voltage of 50 keV which is used to enhance strain relaxation at the interface between the metamorphic buffer layers and the Si substrate in order to facilitate the growth of a high quality Ge on the Si.layer The exitaxial structure in this study is

illustrated in Fig.2-1. The composition of the Ge_xSi_{1-x} metamorphic buffer layers was carefully formulated to block the dislocations in the lower layers [9]. The Ge compositions in the two metamorphic buffer layers were intentionally grown to 80% and 90% each. Because the point-defects were introduced by a Si^+ pre-ion implantation on the surface of the Si substrate, the level of relaxation was enhanced, the thickness of the metamorphic buffer was greatly reduced and the surface morphology was improved. More interestingly, the dislocation density of the top Ge layer was effectively reduced to$10^6 cm^{-2}$.

2.2 Experimental

The experiments in this work can be divided into two parts. The first part involves the growth of the Ge_xSi_{1-x} metamorphic buffer layers on the Si substrates without Si^+ ion implantations. The growth of the Ge_xSi_{1-x} and Ge layers was carried out using an ultra-high vacuum, chemical-vapor deposition (UHV/CVD) system with a base pressure of less than 2×10^{-8} Torr. After RCA cleaning of the 4 inch Si (100) substrate surface, a Ge_xSi_{1-x} metamorphic buffer structure, including one $Ge_{0.8}Si_{0.2}$ layer and one $Ge_{0.8}Si_{0.2}$ layer, was grown at 430^{o}C with a vapor pressure of 30 mTorr on the substrate, [9]. Then a pure Ge top layer was subsequently grown at 400^{o}C with the same vapor pressure and with a constant GeH_4 flow rate of 10 sccm. After the Ge growth was finished, in-situ annealing at 750^{o}C for a duration of 15 minutes was employed to improve the crystalline quality of the epitaxial layers.

The optimum thickness of the Ge_xSi_{1-x} metamorphic buffer layer should be larger than 1.45 μm for strain relaxation to occur so that a high quality pure Ge film can be achieved [9].

The second part of this work focuses on the study of the effect of Si^+ pre-ion implantation on the growth of the Ge_xSi_{1-x} metamorphic layer. As mentioned above, the Ge_xSi_{1-x} buffer structure was grown with the same Ge composition as that of the Si^+ implanted Si substrate. The implantation involved a Si^+ dose of 5×10^{15} cm^{-2} administered at an acceleration voltage of 50 keV. Cross-sectional Transmission electron microscopy (XTEM) was used to observe the thickness of the epitaxial layers and the dislocation distribution.

2.3 Results and Discussion

Figs. 2-2(a) and (b) show the bright-field, cross-sectional TEM images of the samples with and without the Si^+ pre-ion implantation respectively. Fig. 2-2(a) was taken by using a diffraction vector **g** = [004] and the surface of the Si substrate was modified with a Si^+ pre-ion implantation. By contrast, Fig. 2-2(b) was taken by using a diffraction vector **g** =[004], and the Si substrate was not implanted. The top Ge layer and the Ge_xSi_{1-x} metamorphic buffer are clearly shown in both images. In Fig. 2-2(a) a dark region can be observed at the interface between the Ge_xSi_{1-x} buffer and the Si substrate, this region is associated with the defects induced by the Si^+ pre-ion implantation. The thinner buffer layers were observed in the Ge_xSi_{1-x} metamorphic buffer layers with a pre-ion implantation and the optimized thickness of

the Ge_xSi_{1-x} metamorphic buffer required for the growth of a high quality Ge film was only 0.45 μm. By contrast, in Fig. 2-2(b), in order to obtain a high-quality Ge top layer, a thicker metamorphic buffer layer was required to relax the strain energy for the sample without pre-ion-implantation. In this case, the optimized thickness of the Ge_xSi_{1-x} metamorphic buffer for the growth of high quality Ge film was larger than 1.45μm.

The (004) double crystal X-ray rocking curves for the samples with and without Si^+ pre-ion implantations are shown in Fig. 2-3(a) and Fig. 2-3(b). In Fig. 2-3(a), the single crystalline peak for the top Ge layer (θ_{Ge}) is clearly visible with a strong intensity. It separated from the Si substrate peak (θ_{Si}) with a distance of $\theta_{Si} - \theta_{Ge}$ = 5,380 arcsec, which indicates that the top Ge layer is close to full relaxation (in case of full relaxation, $\theta_{Si} - \theta_{Ge}$ =5,366 arcsec). Other smaller additional peaks are shown on the right side of the Ge peak. These smaller peaks correspond to the different Ge_xSi_{1-x} layers in the metamorphic buffer. Because the Ge composition in the buffer begins at x = 0.8 (rather than at x = 0), these peaks are also a great distance from the Si substrate peak. The dislocation density (D) in the top Ge layer can be estimated from the FWHM of the X-ray Bragg peak by using the equation [4-5]:

$$D = \Delta\varphi^2/(9b^2) \qquad (1)$$

where b is the length of the Burger vector of the dislocations and Δφ is the FWHM. Assuming the dislocations contained in the Ge layer are the 60° dislocations, then the value b = $\sqrt{2}\,a$, where a is the lattice parameter. From Fig.2-3(a), Δφ = 134 arcsec can be obtained. With

these values, the dislocation density in the Ge film grown with a Si^+ pre-ion implantation is calculated to be D =7.6×10^6 cm^{-2}.

Fig. 2-3(b) shows the Ge_xSi_{1-x} metamorphic buffer grown on the Si substrate without Si^+ pre-ion implantation. The highly intense peak for the top Ge layer (θ_{Ge}) is also clearly visible. It is separated from the Si substrate peak (θ_{Si}) by a distance of θ_{Si} - θ_{Ge} = 5,425 arcsec, which indicates that the top Ge layer has higher strain than the Ge layer grown on the Si substrate with pre-ion implantation. This result indicates that the Si^+ pre-ion implantation induced point-defects in the Si substrate clearly result in the reduction of strain in the buffer layer. Other smaller peaks in Fig. 2-3(b) are broader than their counterpart peaks in Fig 2-3(a), which can be attributed to more dislocations generated at the lower layer of the metamorphic buffer when grown on the Si substrate without pre-ion implantation. This result is also consistent with the TEM observation in Fig.2-2 (b), where higher dislocation densities can be observed in the metamorphic buffer layers grown on the substrate without an implantation. It is postulated that this is due to the increased density of defect nucleation sites arising from point-defect condensation to form incipient dislocation loops. These nucleation sites then help the system to overcome the high nucleation barrier which would exist in the absence of the implantation. It is the enhanced dislocation nucleation which is responsible for the accelerated relaxation of the implanted structure. Once nucleated, it is favorable for the dislocations to propagate energetically, thus relaxing the structure. At the same time, point-defects promote

dislocations it climb which help to annihilate threading dislocation arms with opposite Burgers vectors. Consequently, the density of threading dislocations is reduced [10-12].

Fig. 2-4 shows symmetrical (004) and asymmetrical (224) reciprocal space maps of the sample. The reflections from top Ge layer, Ge_xSi_{1-x} metamorphic layers and Si substrate are clearly shown. The nearly circle-shaped iso-intensity contours from the Si substrate (see Fig. 2-4(a)) indicate that the curvature of the epitaxial layers is insignificant. In both maps, there is a broadening along the ω-scan direction, which implies that there is mosaicity in the epitaxial layers. In Fig.2-4 (b), the Ge peak centers on the dashed line along the [224] direction through Si substrate peak, which indicates that the top Ge layer is nearly fully relaxed. The peaks from the initial layers of the metamorphic buffer slightly deviate from [224] line, which indicate that these layers have weak strain.

An atomic force microscopy image of the surface of the Ge film grown on the Si substrate with Si^+ pre-ion implantation is shown in Fig.2-5. The surface is smooth, and no cross-hatch pattern is visible. The measured root mean square (RMS) of the surface roughness is only 0.38nm in contrast to that of 210nm for the conventional composition graded buffer [3]. The cross-hatch pattern on the conventional graded GeSi layers is related to the accumulation of dislocations on the same or nearby parallel slip planes (this type of arrangement is also referred to as dislocation pileups) [6]. However, for the current case, the disappearance of the cross-hatch pattern is because that the metamorphic buffer takes a three-dimensional growth

mode in its initial stage, and the resulted behavior of the dislocations is different from that in the conventional composition graded GeSi layers. From the TEM images in Fig. 2(a) and Fig. 2-2(b), no dislocation pileup can be observed in the Ge_xSi_{1-x} metamorphic buffer layer This probably explains why no cross-hatch pattern is exhibited on the sample surface. Nomarski interference microscopy image of the grown Ge surface is shown in Fig.2-6 by etching 15sec in the etching solution (CH_3COOH 134 ml, HNO_3 40 ml, HF 20 ml, and I_2 60 mg) [6]. By counting the pits on the surface, the threading dislocation density was evaluated to be about $9.0\times10^6 cm^{-2}$.

2.4 Conclusions

A thin Ge_xSi_{1-x} metamorphic buffer layer for the growth of a high-quality Ge film on a Si substrate was achieved by using a Si^+ on implantation on the Si substrate before the growth of the Ge_xSi_{1-x} metamorphic buffer layers. The enhanced level of relaxation can be attributed to the introduction of point-defects in the Si substrate with a heavy dose Si^+ pre-ion-implantation. Due to the use of the pre-ion-implantation technique and the interface-blocking of the dislocations in the Ge_xSi_{1-x} metamorphic buffer structure, the total thickness of the Ge_xSi_{1-x} metamorphic buffer layer was greatly reduced to a thickness of 0.45μm, which is much thinner than in the previous report [9]. Because the formation of the dislocation pileups in the Ge_xSi_{1-x} metamorphic buffer layer was eliminated, the surface of the Ge film grown was very

smooth, no cross-hatch pattern could be observed and the dislocations in the top Ge layer were reduced to about $7.6\times10^{6}cm^{-2}$. The approach described in this paper can be used to grow high-quality Ge film on a Si substrate and can also be easily applied to the fabrication of the Ge MOSFETs and optoelectronic devices on Si substrates.

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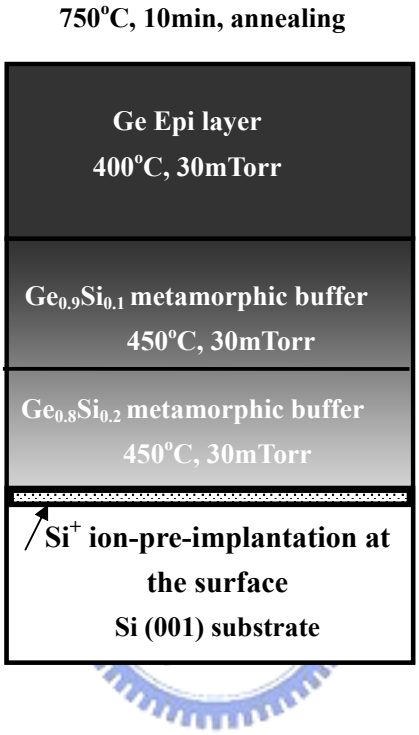
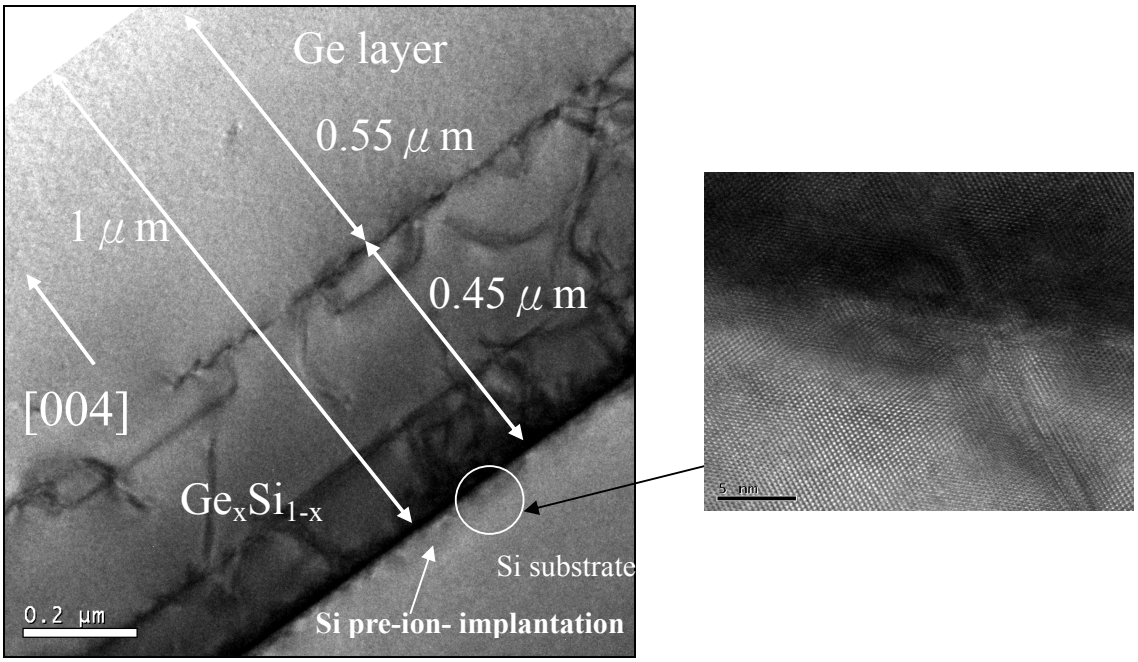
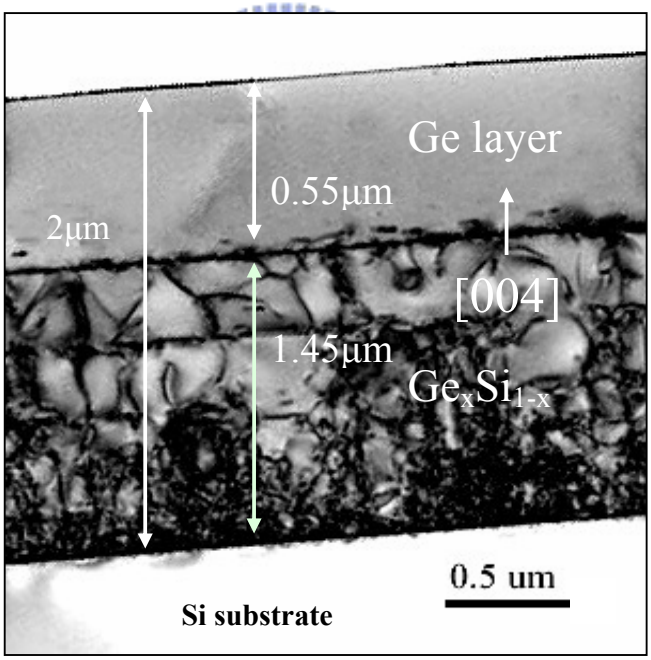


Fig. 2-1. The layer structure and the growth conditions for the Ge film grown on the Si substrate with Ge_xSi_{1-x} metamorphic buffer layers. Note that Ge_xSi_{1-x} was grown at two growth rates ,the Ge composition set at 80% and 90%, and the Si substrate implanted with high dose Si^+ ions.

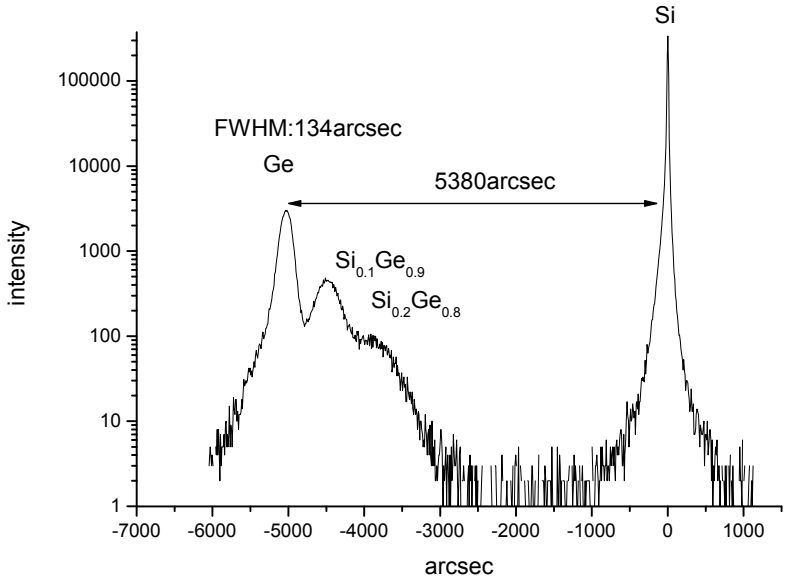


(a)

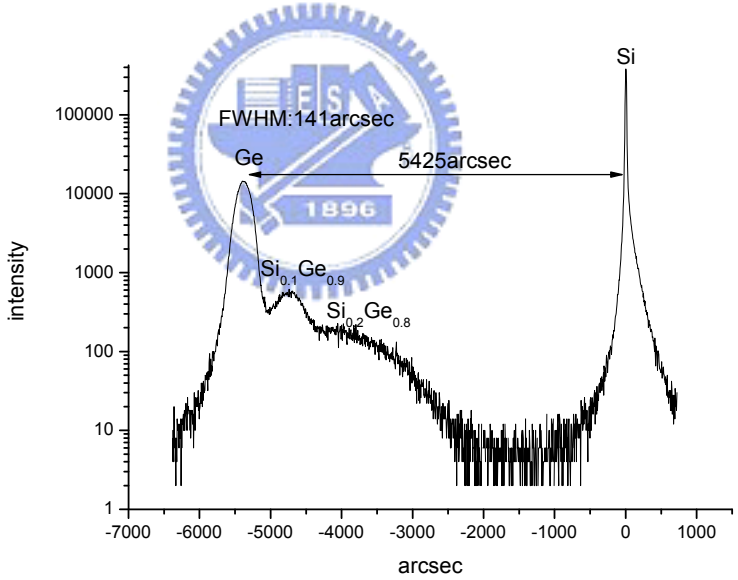


(b)

Fig. 2-2. Cross-sectional TEM images of sample (a) with a Si^+ pre-ion implantation into the Si substrate; the inserted image is the high-resolution TEM image at the interface between the Ge_xSi_{1-x} metamorphic layer and the Si substrate. (b) the Ge_xSi_{1-x} metamorphic grown on the Si substrate without a Si^+ pre-ion implantation into the Si substrate.



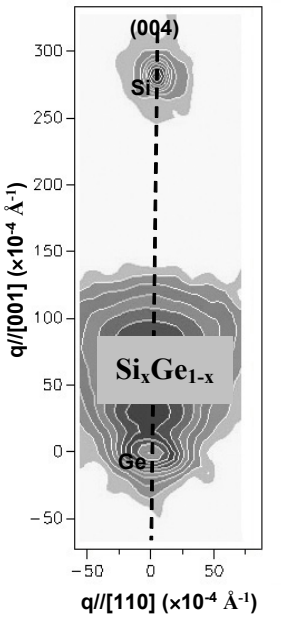
(a)



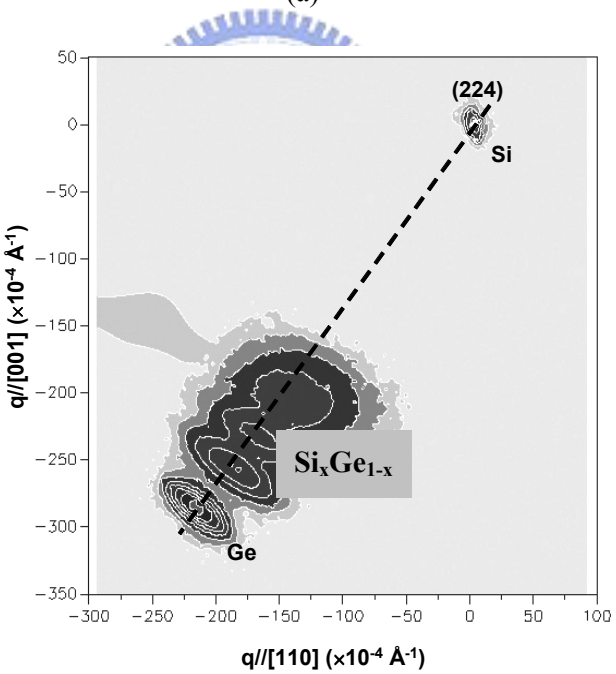
(b)

Fig. 2-3 (a) Double crystal x-ray data indicating variations at a [004] orientation for the Ge_xSi_{1-x} metamorphic buffer layer on the Si substrate with a Si^+ pre-ion-implantation.

(b) Double crystal x-ray difference data indicating variations at [004] orientation for the Ge_xSi_{1-x} metamorphic buffer layer on the Si substrate without a Si^+ pre-ion-implantation.



(a)



(b)

Fig. 2-4 (a) Reciprocal Space Map data of [004] orientation of Ge_xSi_{1-x} metamorphic buffer layer on Si substrate with Si^+ pre-ion-implantation. (b) Reciprocal Space Map data of [224] orientation of Ge_xSi_{1-x} metamorphic buffer layer on Si substrate with Si^+ pre-ion-implantation.

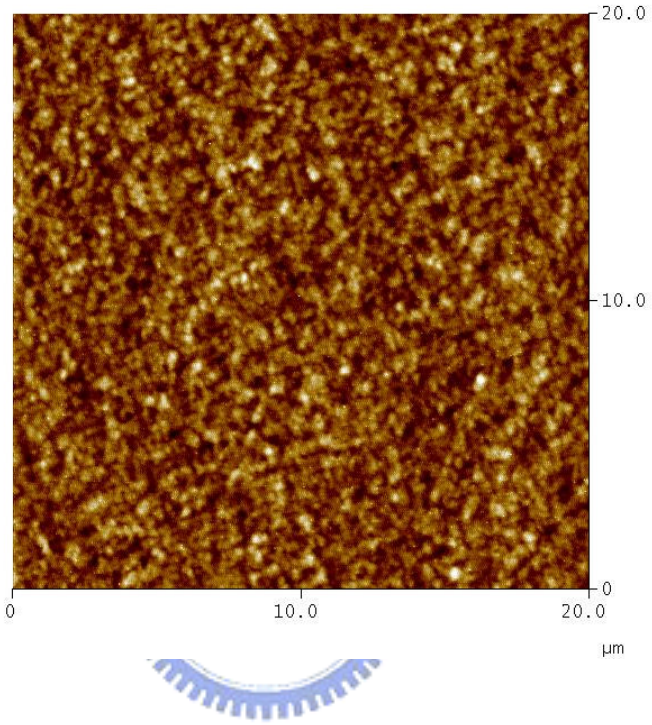


Fig. 2-5 AFM image of the surface morphology of the sample with a Si^{+} pre-ion implantation. The root mean square (RMS) of the roughness is 0.38nm.

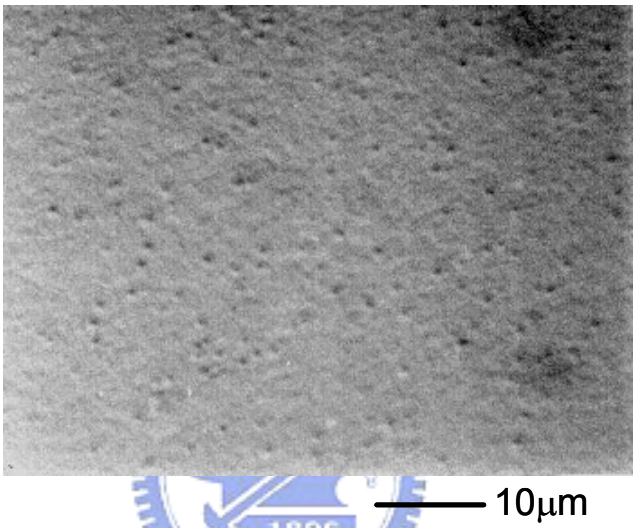


Fig. 2-6 Nomarski image of the etched Ge film, the etch pits arise from threading dislocations.

Chapter 3

Growth of epitaxial GaAs on Si substrates for high-speed electronic applications

3.1 Introduction

The heteroepitaxial growth of GaAs on Si substrates has attracted great attention in recent years due to the potential integration of the Si and GaAs based devices. GaAs has advantages over Si for some application due to higher electron mobility, wider bandgap, and direct bandgap. Silicon, however, has several advantages over GaAs such as larger area, SiO_2 coverage, and higher thermal conductivity. The main problem to overcome in growing GaAs on Si by heteroepitaxy is the large lattice mismatch of 4% and the difference in the thermal expansion coefficients (63%) of these two materials. [1] To achieve high quality device structure, it is necessary to reduce the dislocations density in the epitaxial layer. Several methods for reducing the dislocation density have been reported, such as using strained layers superlattice to confine dislocations [2], or using thermal cycle annealing to reduce threading dislocation. Motorola lab has reported GaAs MESFETs fabricated on Si using a $SrTiO_3$ buffer layer in the MBE system. However, the $SrTiO_3$ buffer layer is hard to be grown in the MBE system. [3-4]

In this study, we use Ge_xSi_{1-x} metamorphic buffer layers with a Ge layer on top of the

structure because Ge is only 0.07% lattice mismatched with GaAs, and the thermal expansion coefficient difference between Ge and GaAs is 2%, i.e. the lattice constant and thermal expansion coefficients of Ge are almost identical as for GaAs. Using Ge/SiGe metamorphic structure as buffer layer can solve the mismatch problems of the interface between GaAs and Si.

Many publications [5] have reported that a pure Ge layer was grown compositionally graded GeSi buffer layers in ultra-high vacuum chemical vapor deposition (UHV/CVD). However, the graded Ge_xSi_{1-x} buffer layer must be thick enough (10μm). It may also show surface roughness and crosshatch pattern. M.T. Currie [4] has described a method utilizing chemical-mechanical polished (CMP) to grow a relaxed graded SiGe buffer to 100% Ge layer.

In our former studies, a Ge_xSi_{1-x} buffer structure for the growth of high-quality GaAs layers on Si (100) substrate was employed [5]. For the growth of this Ge_xSi_{1-x} buffer structure, a 0.8μm $Ge_{0.9}Si_{0.1}$ layer was first grown. Due to the large mismatch between this layer and the Si substrate, many dislocations formed near the interface, and in the low part of the $Ge_{0.9}Si_{0.1}$ layer. A 0.8μm $Ge_{0.95}Si_{0.05}$ layer and a 1.0μm top Ge layer were subsequently grown. The strained $Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}$ and Ge/ $Ge_{0.95}Si_{0.05}$ interfaces formed terminate and can bend the upward-propagated dislocations very effectively [8].

A common problem with the GaAs/Ge interface is the formation of antiphase domains

(APDs), which occurs when growing polar GaAs on nonpolar Ge. Several models were reported on the suppression of APDs by using Ge wafer 6^0 off (100) toward <110> direction. As the growth proceeds, the initial nuclei grown at the steps coalesce so that the APB-free GaAs is achieved. Another problem is the diffusion of Ga and As into the Ge buffer layer, both of which act as a dopant atoms in Ge. The detail of the growth process was reported in literature [7].

In this study, the Ge/Ge_xSi_{1-x} buffer was grown by ultra-high vacuum chemical vapor deposition (UHV/CVD). Then, the sample was switched to the MOVPE system and grew the GaAs MESFET structure. We will describe this $GaAs/Ge/Ge_xSi_{1-x}/Si$ heterostructure in detail.

3.2 Experimental

The growth of the Ge_xSi_{1-x} and Ge buffer layers was carried out using an ultra-high vacuum chemical vapor deposition (UHV/CVD) system with a base pressure of less than 2×10^{-8} torr. First, a 4-inch Si wafer 6^0 off (100) toward <110> direction was cleaned by 10% HF dipping and high-temperature baking at 800℃ in the growth chamber for 5 min. Then, a 0.8 μm $Ge_{0.9}Si_{0.1}$, a 0.8 μm $Ge_{0.95}Si_{0.05}$, and a 1.0μm Ge layer were grown at 400℃ in sequence. Between successive layers, growth was interrupted in situ for 15 min for annealing at 750℃. After a Ge layer was grown on the SiGe layer, the sample was switched to a LP-MOVPE system to grown GaAs on the Ge/GeSi/Si heterostructure at 620℃ and 40 Torr reactor

pressure. The investigations in this work are composed of two parts. The first part studies the formation of antiphase boundary at different growth temperature. For comparison, we try to grow also at different temperature GaAs buffer layers on $Ge/Ge_xSi_{1-x}/Si$ metamorphic heterostructure without using off angle substrate. In this case, the GaAs buffer layer thickness was 100nm grown at 450℃, 500℃ and 550℃, respectively. Then an undoped 1μm GaAs layer was grown at 630℃. In the second part of this work, we grew the same structure on Si substrate with 6^0 off (100) toward <110> direction. This part focuses on the suppression of the antiphase boundaries by using misorientation substrate. There is still a 0.1% lattice mismatch and 2 % thermal expansion coefficient difference. Then 15 superlattices with pairs AlGaAs/GaAs were grown to restrict the dislocation propagation and modify the surface. A GaAs MESFET structure with 2μm undoped GaAs layer, a 1500 Å channel doped at 5×10^{17} cm^{-3} and a 500 Å contact layer doped at 5×10^{18} cm^{-3} was successively grown on the top of the heterostructures with Si substrate (see Fig. 3-1). The TEM was used to measure the thickness of the epitaxial layers and observe the dislocation distribution.

3.3 Results and discussion

3.3.1 Low temperature buffer GaAs buffer grown on Si substrates

GaAs layers were grown on Si substrate with $Ge/Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}$ layer as buffer by LP-MOVPE system have low mismatch (< 0.12%) and low thermal expansion difference

(<2%) between GaAs and Ge. Although the low lattice mismatch of the GaAs/Ge system suggests that it should be nearly dislocation free, considerable problems still exist related to the epitaxy between polar (GaAs) on non-polar (Ge) semiconductors resulting in the formation of antiphase domains. The polarity phases are related to the growth temperature and substrate misorientation angle [9]. The atoms nuclei form at the steps and terraces with the latter having crystal orientation 90^0 rotated. APBs provide deep levels in the forbidden gap and act as non-radiative recombination surface. We try to grow low temperature GaAs buffer on Si substrates without misorientation angle to suppress antiphase boundaries. However, it could not control the nucleation sites at the steps or terraces only in one domain. Fig. 3-2(a) shows the two possible growth orientations of the GaAs layer in the 0^0 off sample. There are two domains differing from each other in a reversal Ga and As atoms in the sublattices resulting in a rotation of 90^o with respect to the substrate. The two domains were separated by an antiphase boundary. Many irregular lines were observed on the surface. The sizes of antiphase boundaries increase with growth temperature of GaAs buffer layer. The higher temperature increases diffusion length of the surface species may affect size of the antiphase boundaries. The mobility of atoms is enhanced because atoms can diffuse longer distance before low-density and large grain formation. The root mean square (RMS) was 70.35 Å and the roughness average (Ra) was 60.61 Å. The vertical distances of APBs were 10nm. At low growth temperature, atoms can only diffuse short distance before they are

incorporated. Therefore, the mobility of atom was kinetically delayed of frozen out and the small size formation of antiphase boundaries was observed in Fig 3-2(c). The small and vague features of antiphase boundary observed at low temperature are explained by poor surface diffusion kinetics.

3.3.2 The suppression of antiphase boundaries by using tilted Si substrate

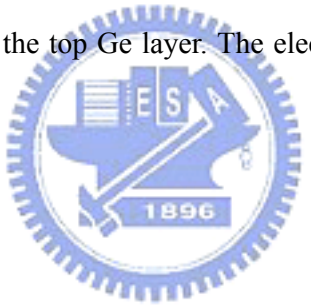
The most common method for avoiding the antiphase domains (APDs) at the GaAs/Ge interface is by the use of tilted substrates with sufficient thermal annealing. The suppression of APDs can be achieved by using Ge wafer with 6^0 off (100) toward <110> direction. For the substrates with a larger miscut angle (6^0), in which the terraces between the steps are very narrow, the steps are so close to each other that no nucleus can be formed on the terraces. As the growth proceeds, the initial nuclei coalesce so that a single domain of GaAs is achieved [9]. This diminishes the chance for two-dimensional nucleation on the terraces. Therefore, only GaAs nuclei will be formed at the steps. Consequently, all the layers have the same sublattice orientation. In this study, the sample was grown on $Ge/Ge_xSi_{1-x}/Si$ substrate with 6^0 off (100) toward <110> direction. No APB was observed on the surface. In our study, the twins and the lattice defects finally disappeared when the $GaAs/Ge/Ge_xSi_{1-x}$ epilayers were grown on Si substrate with 6^0 off (100) toward <110> direction. The reason for this may be found in the structure and the density of the steps, not the (110) terrace. The occurrence of the

self-annihilation processes of APBs is very importation for the growth of the device quality GaAs/Ge/Ge_xSi_{1-x}/Si epitaxial layers. For the substrates with a larger miscut angle, in which the terraces between the steps are very narrow, the steps are so close to each other that no nucleus can be formed on the terraces. As the growth proceeds, the initial nuclei that were grown on the steps will coalesce so that a single domain of GaAs can be achieved [8]. In this study, the sample was grown on Ge/Ge_xSi_{1-x}/Si substrate with 6^0 off (100) toward <110> direction. No APD on the surface was observed. The surface roughness was measured by AFM (see Fig. 3-3.) The root mean square (RMS) was 7.35 Å and the roughness average (Ra) was 5.81 Å.

In order to verify the interdiffusion of Ge layer into GaAs, secondary ion mass spectroscopy (SIMS) technique was used. This technique yields quantitative measurements of dopants and impurity levels in semiconductors. According to W. Li [10], the formation of APBs was found to depend primarily on the magnitude of the misorientation angle of the (001) Si substrate. Fig. 3-5(a), (b) and (c) show the depth profile of the Ge diffusion into the GaAs layer. We found different diffusion lengths of the Ge diffusion into the GaAs layer according to the different misorientation of the Si substrate. Fig. 3-5(a) shows the distance of the Ge diffusion into GaAs layer is about 0.75μm with 0^0 misorientation of the substrate. When the degree of the substrate misorientation is larger than 6^0 off (100) toward <110> direction, it could suppress the antiphase boundary. Fig. 3-5 (c) shows the distance of the Ge diffusion

into GaAs layer to be about 0.25μm with 6^0 misorientation (100) toward <110> direction of the substrate. The antiphase boundaries may be considered as defects, Ge atoms could diffuse along the boundaries into the GaAs layer during the growth procedure. Fig 3-5(a) shows a GaAs layer grown on Si substrate with 6^0 off (100) toward <110> direction. We saw misfit dislocations blocking at the Ge_xSi_{1-x} metamorphic buffer layer. Fig. 3-5(b) shows the GaAs layer grown on Si substrate without misorientation. We observed the antiphase boundaries through the GaAs layer from the Ge layer. These results explain the relation of the Ge diffusion on the formation of antiphase boundaries. Our data compare favorably with in the literature [10]. Fig. 3-6(a) shows the double crystal x-ray diffraction pattern of the Ge layer and Ge_xSi_{1-x} layer grown on the Si substrate; the FWHM is 150 arcsec. The wide two peaks in Fig. 3-6 are due to the $Ge_{0.95}Si_{0.05}$/ $Ge_{0.9}Si_{0.1}$ layer. The narrow FWHM of the GaAs peak indicates there high quality GaAs layer was grown on Si substrate with a misorientation of 6^0 (100) toward <110> direction; its FWHM is 160 arcsec (compare Fig 3-6(b)). There's still a 0.1% lattice mismatch and a 2 % thermal expansion coefficient difference. As a precaution we insert 15 pairs AlGaAs/GaAs layers before the actual GaAs layer in orders to block threading dislocations penetrating through the GaAs layer during the cooling stages. Fig. 3-7(a) shows a 3 μm GaAs layer and 15 pairs of an AlGaAs/GaAs superlattice grown by MOVPE on $Ge/Ge_{1-x}Si_x/Si$ substrate structure. On top of the undoped GaAs layer, a MESFET structure with a 1,500 Å channel Si doped 5×10^{17} cm^{-3} and 500 Å contact layer Si doped at 5×10^{18} cm

$^{-3}$ was grown. As mentioned the AlGaAs/GaAs supperlattice will modify the surface and prevents the threading dislocations to penetrate through the GaAs layer to the surface [1]. Fig. 3-7 shows the cross-section at TEM image of the $Ge_{1-x}Si_x$ buffer layers grown on Si substrate. The total thickness of the epitaxial structure is only approximately 2.6μm. There was a large number of dislocations located near the $Ge_{0.9}Si_{0.1}$/Si interface and at the lower part of the $Ge_{0.9}Si_{0.1}$ layer. The strain energy is obviously relaxed by forming these dislocations. The upward propagating dislocations were found to be bent sideward and terminating very effectively at the $Ge_{0.95}Si_{0.05}$/$Ge_{0.9}Si_{0.1}$ and Ge/$Ge_{0.95}Si_{0.05}$ interfaces. Almost no threading dislocation can propagate into the top Ge layer. The electronic device data will be published to another journal



3.4. Conclusions

A Ge/$Ge_{0.95}Si_{0.05}$/$Ge_{0.9}Si_{0.1}$ buffer layer was used to accommodate the strain induced between the Si substrate and the GaAs layer and prevent threading dislocations from propagating into the top GaAs layers. A AlGaAs/GaAs supperlattice structure was used to improve the surface roughness and reduce the dislocation density in the GaAs layer. The surface roughness RMS of the sample was 7.35 Å and the roughness average was 5.81 Å. The mobility of the GaAs layer grown on the Ge/$Ge_{1-x}Si_x$/Si structure was 2,130cm^2/v-s when the doping concentration of the GaAs layer was $5.45\times10^{17}/cm^3$.

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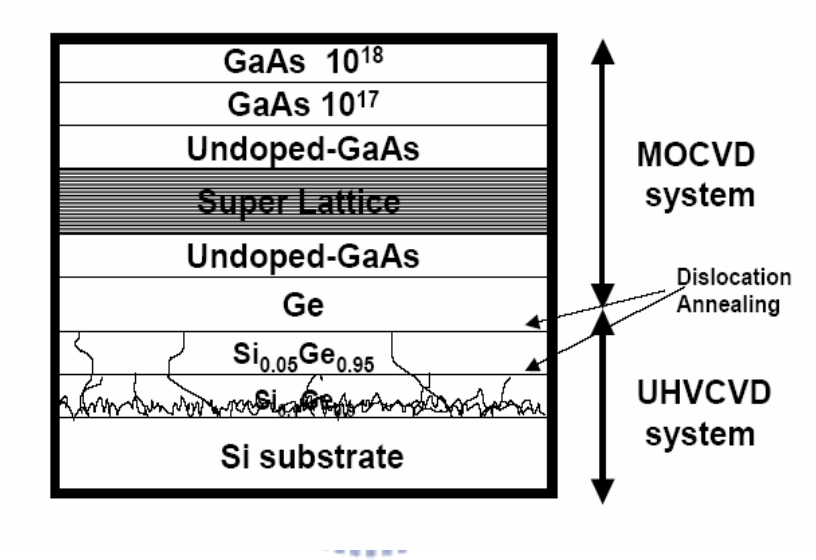
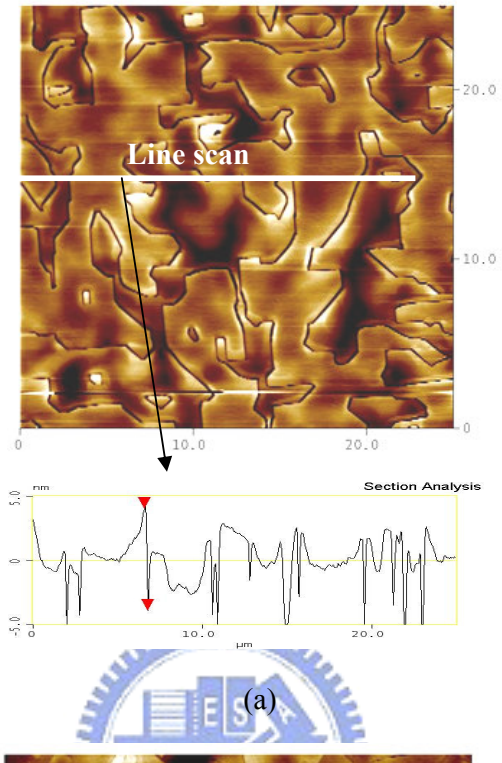


Fig. 3-1 Schematic diagram of GaAs MESFETs on Si substrate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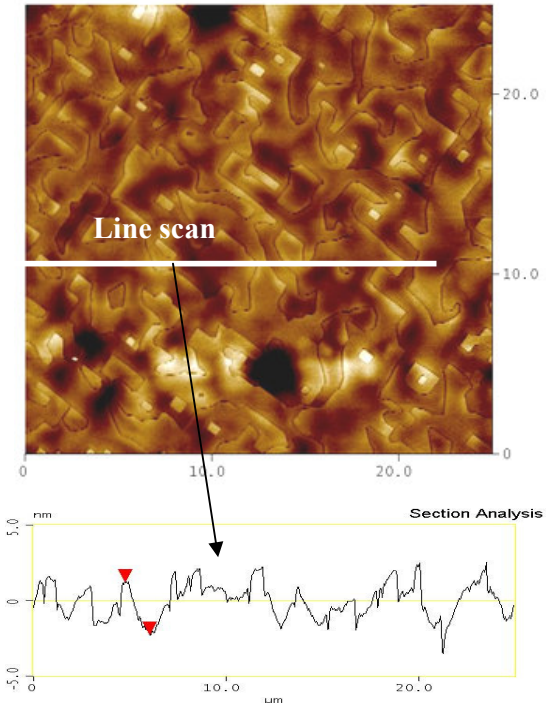
20.0
10.0
0
0
10.0
20.0
Section Analysis
nm
5.0
0
-5.0
0
10.0
20.0
μm

(a)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20.0
10.0
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0
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Section Analysis
nm
5.0
0
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10.0
20.0
μm

(b)

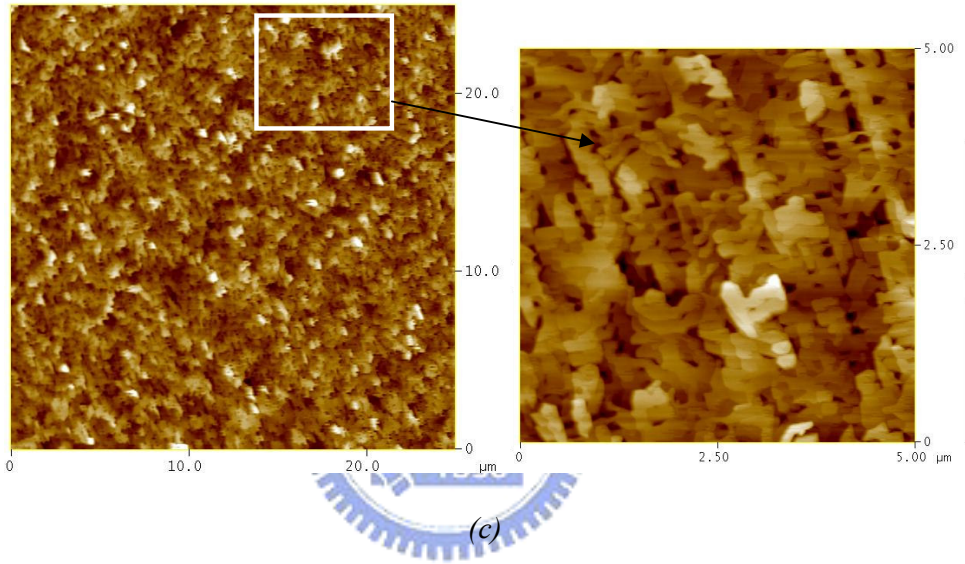


Fig. 3-2 The different low growth temperature GaAs buffer layers grown on the composite substrate structure with $Ge/Si_xGe_{1-x}/Si$ substrate (Si substrate without off angle). (a)550℃ (b)500 ℃(c) 450℃. The scanned area is 25 μm×25 μm .

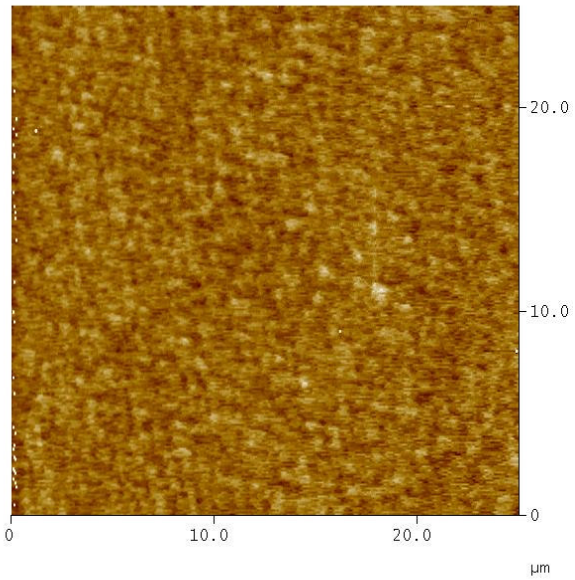
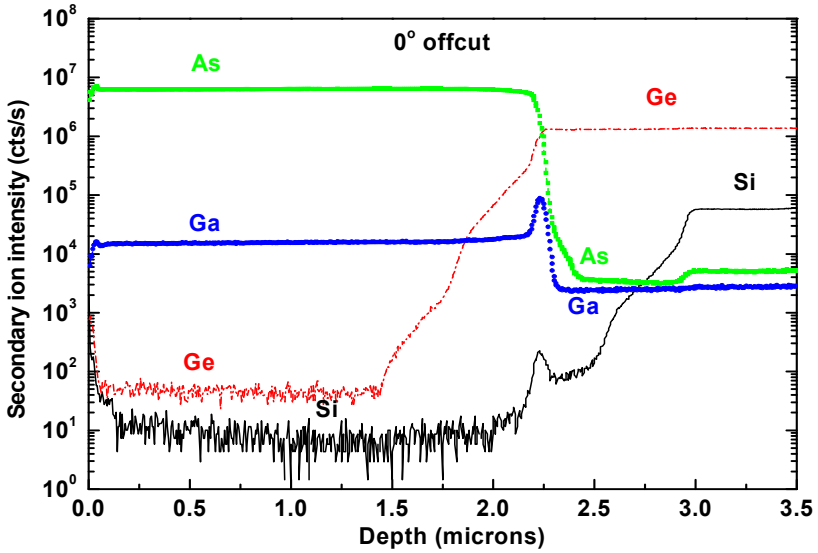
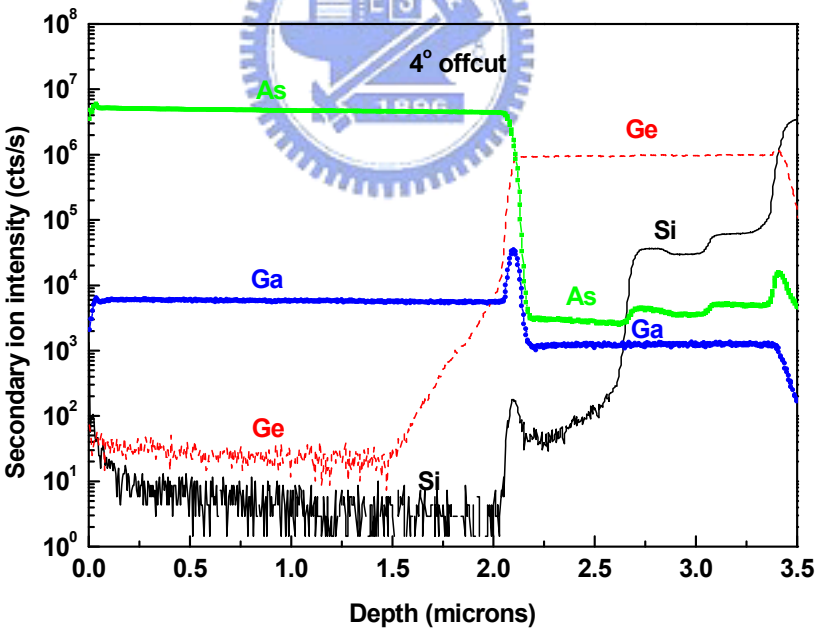


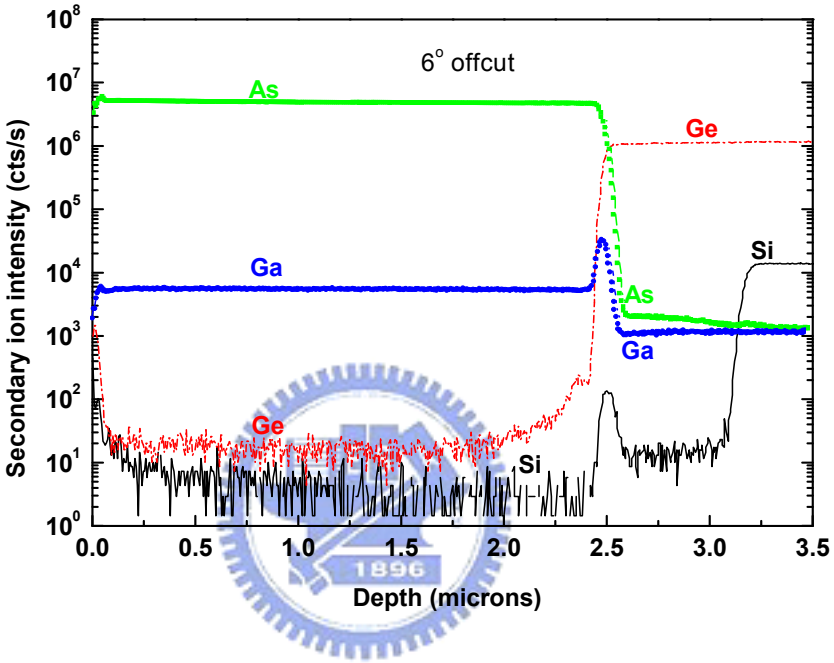
Fig. 3-3 AFM image of the GaAs grown on the composite structure with $Ge/Si_xGe_{1-x}/Si$ (Si substrate with 6^0 off toward <110>). The scanning area is 25 μ m×25 μ m .


0° offcut
As
Ge
Si
Ga
As
Ga
Ge
Si
Secondary ion intensity (cts/s)
Depth (microns)

(a)

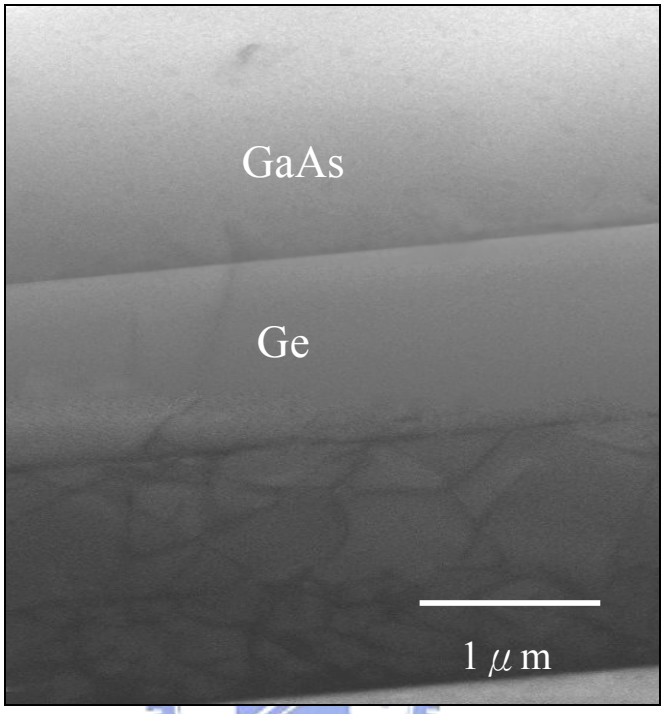

4° offcut
As
Ge
Si
Ga
As
Ga
Ge
Si
Secondary ion intensity (cts/s)
Depth (microns)

(b)

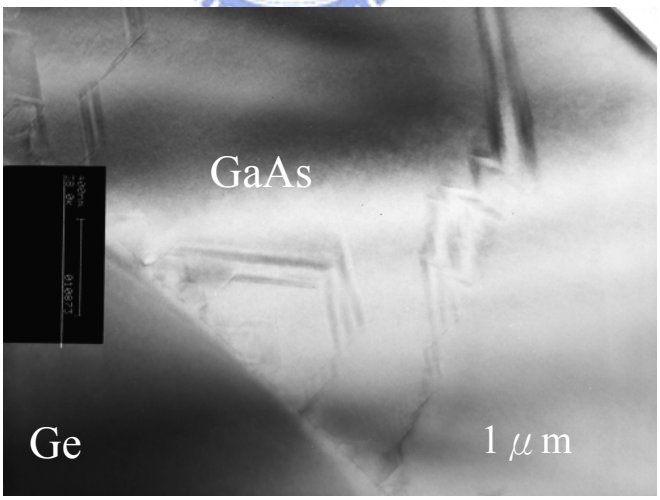


(c)

Fig. 3-4 SIMS profiles of As, Ga and Ge in a 2 μm thick GaAs layer grown on Si with different off angle toward [110] direction. (a) 0 off (b) 4° off (c) 6° off.

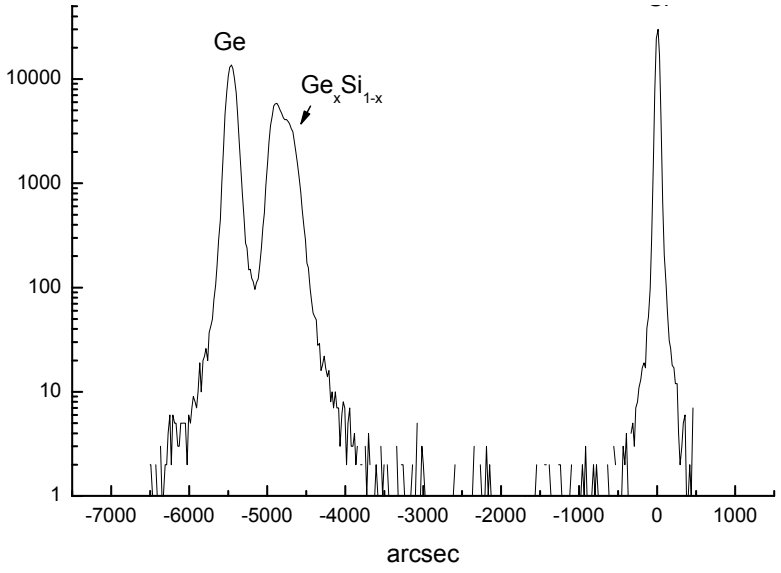


(a)

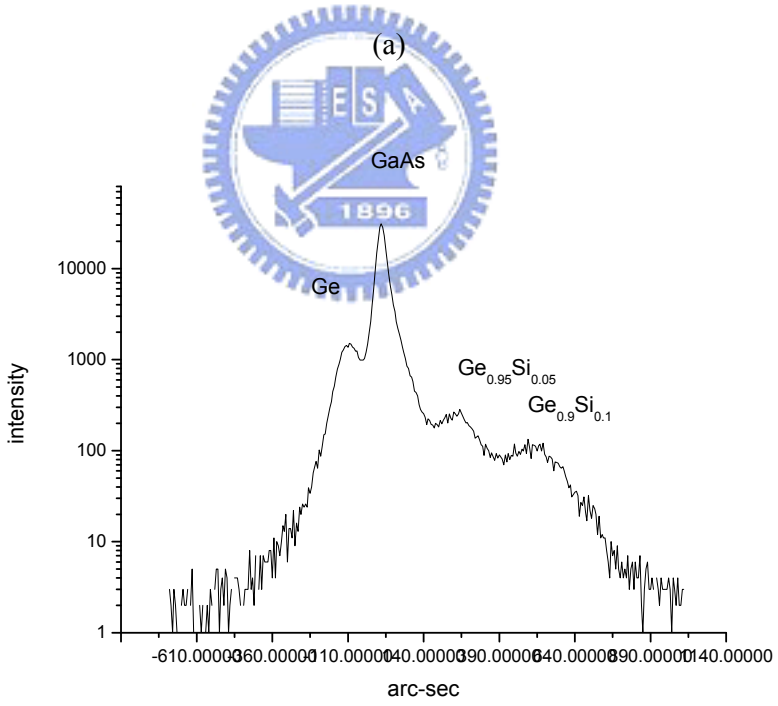


(b)

Fig. 3-5 Transmission electron micrograph of grown structure with from Si to Ge buffer layer to GaAs transitions. (a) GaAs layer grown on Si substrate with 6^0 off (100) toward <110> direction. (b) GaAs layer grown on Si substrate without off angle.



(a)



(b)

Fig. 3-6 Double crystal x-ray diffraction pattern of (a)Ge and SiGe metamorphic layer grown on a Si.substrate (b)GaAs layer grown on a $Ge/Si_xGe_{1-x}/Si$ substrate.

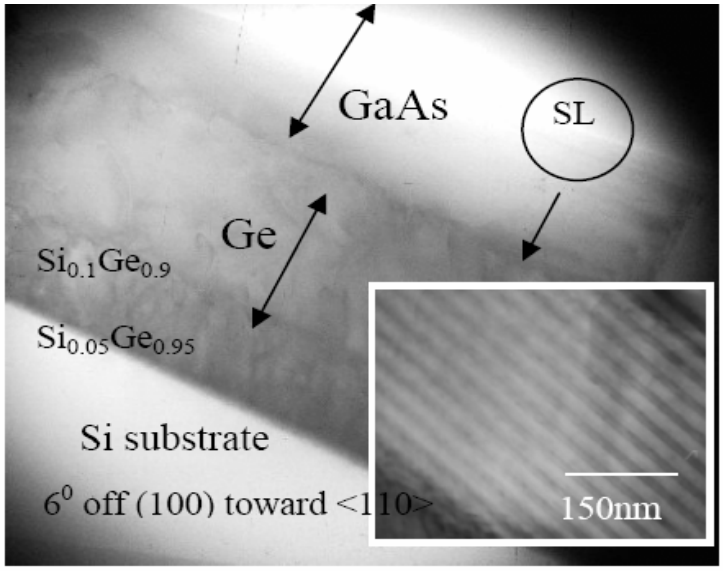


Fig. 3-7 Transmission electron micrograph of a structure grown with Si to Ge buffer layers and a transistion to GaAs transitions with AlGaAs/GaAs superlattice in the GaAs layer.

Chapter 4

An AlGaAs/InGaAs HEMT's on Si substrate with Si^+ pre-ion-implantation and $Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}/Ge_{0.8}Si_{0.2}$ metamorphic buffer

4.1 Introduction

Heteroepitaxial growth processes have gained in prominence and importance in recent years, as the number of devices incorporating heteroepitaxial layers has steadily increased. Recently, one highly sought after heteroepitaxial system has been produced the monolithic integration of GaAs-based materials on Si. The growth of low threading dislocation density (~ 2 x $10^6 cm^{-2}$) relaxed graded $Ge/Ge_xSi_{1-x}/Si$ heterostructures can bridge the gap between lattice constants by replacing the high mismatch GaAs/Si interface with a low mismatch (< 0.1%) GaAs/Ge interface. Although the lattice mismatch problem is thus eliminated, the heterovalent GaAs/Ge interface remains highly susceptible to antiphase boundaries. Several models were reported for the suppression of APBs by using Ge wafer 6^o off (100) toward <110> direction [7-11]. As the growth proceeds, the initial nuclei grown at the steps coalesce so that APB-free GaAs is achieved. The details of the growth process were reported in literature [11]. Previous literature reported relaxed GeSi graded layers on Si substrate has produced the highest quality GaAs on Si to date for the integration of GaAs on Si substrate

[7-11]. The thermal expansion coefficient of Si substrate is dominated by that of Si substrate is much thicker than the total thickness the graded layers plus the top Ge layer, which is approximately 10μm. The presences of cracks in thin films which caused thicker thickness of the buffer layer are not desirable for the device fabrication because they can act as scattering centers for light propagation, can resist in-plane electrical current flow, and can introduce electrical shorting paths in vertical current [7-8].

In our former studies, Si^+ pre-ion-implantation combined with a Ge_xSi_{1-x} metamorphic buffer structure for growth of the Ge layer on Si substrate was proposed. We design the three buffer layers with different composition of Ge_xSi_{1-x}. When the stress field around the interface is strong enough, the dislocation can be bent and traverse along the interface. In advance, we use Si^+ ion bombard the Si substrate to introduce the point-defects in the Si substrate. Enhanced strain relaxation of the Ge_xSi_{1-x} metamorphic buffer layer on Si substrate was achieved due to the introduction of point-defects by heavy dose Si^+ ion-implantation [13-14]. Because of both strain relaxation enhancement and interface-blocking of dislocations in the Ge_xSi_{1-x} metamorphic buffer structure, the total thickness of all the layers were only 1.0μm. The thinner buffer layers will reduce the effect of the thermal strain between the buffer layers and Si substrate. Additionally, well controlled precisely the compositions of Ge_xSi_{1-x} buffer layer make the lattice constant of buffer layers match with GaAs layer. This design of metamorphic structures could reduce the formations of misfit dislocations and cracks in the film to improve

the crystalline quality.

4.2 Experimental

In this study, the buffer layers were grown by ultra-high vacuum chemical vapor deposition (UHV/CVD). Then, the sample was switched to the MOVPE system to grow the HEMT structure [12]. We describe this $In_{0.18}Ga_{0.82}As$ channel HEMT's grown on $Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}/Ge_{0.8}Si_{0.2}$ heterostructure as shown in Fig 4-1 in detail.

The growth of the Ge_xSi_{1-x} buffer layers was carried out using an ultra-high vacuum chemical vapor deposition (UHV/CVD) system with a base pressure of less than 2×10^{-8} torr. First, a 4-inch Si wafer 6^o off (100) toward <110> direction was implanted with a Si^+ dose of 5×10^{15} cm^{-2} at an acceleration voltage of 50 keV into Si substrate. This sample was cleaned by 10% HF dipping and high-temperature baking at 800℃ in the growth chamber for 5 min. Then, a 0.2 μm $Ge_{0.8}$,$Si_{0.2}$ a 0.25 μm $Ge_{0.9}Si_{0.1}$, and a 0.55 μm $Ge_{0.95}Si_{0.05}$ layer were grown at 400^oC in sequence. Between successive layers, growth procedure was interrupted in situ for 15 min for annealing at 750℃. After a $Ge_{0.95}Si_{0.05}$ layer was grown on the buffer layer, the sample was switched to a low-pressure metal organic vapor epitaxy (LP-MOVPE) system to grown HEMT structure on the $Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}/Ge_{0.8}Si_{0.2}$ heterostructure at 40 Torr reactor pressure. . The InGaAs channel layer was grown at 590℃, the AlGaAs layer and the GaAs layer were grown at 620℃. Fig. 4-1 shows the HEMT structure grown on the

Si substrate. The device structure was composed of 150Å undoped $In_{0.18}Ga_{0.82}As$ channel layer, 40Å undoped $Al_{0.12}Ga_{0.88}As$ spacer layer, 320Å $Al_{0.12}Ga_{0.88}As$ Schottky layer with doping concentration of 5.34×10^{17} cm^{-3} and 200Å GaAs cap layer with doping concentration of 2×10^{18} cm^{-3}. For comparison, we have also tried to grow at HEMT structure on Ge substrate. Fig. 4-2(a) and (b) show the crystalline quality of $In_{0.18}Ga_{0.82}As$ channel HEMT layer stack on Si substrate and Ge substrate was investigated by (400) x-ray diffraction measurement. Si substrate peak, $Ge_{0.9}Si_{0.1}/Ge_{0.8}Si_{0.2}$ metamorphic buffer peaks and AlGaAs/GaAs/$Ge_{0.95}Si_{0.05}$ peak and $In_{0.18}Ga_{0.82}As$ peak are clearly resolved in the Fig 4-2(a). An x-ray diffraction rocking of the layer structure of the $In_{0.18}Ga_{0.82}As$ channel and AlGaAs layer grown on Ge substrate was shown in Fig. 4-2(b). The dislocation density is correlated to the FWHM of the x-ray diffraction peak, the result of $In_{0.18}Ga_{0.82}As$ channel grown on Si substrate is comparable to the one grown on the germanium substrate. The higher quality of the epistructure could be attributed to control precisely the compositions of Ge_xSi_{1-x} metamorphic buffer structures and the thinner thicknesses of the buffer layers.

4.3 Results and discussion

4.3.1 Epitaxial growth of AlGaAs/InGaAs HEMT's on Si substrates

Fig. 4-3(a) shows the cross-section transmission electron microscope pictures of the HEMT structure grown on Si substrate. The composed structure were the 200Å GaAs cap

layer with doped concentration of 2×10^{18} cm^{-3}, 320Å AlGaAs schottky layer with doped concentration of 1.7×10^{18} cm^{-3}, 40Å AlGaAs spacer layer and 150Å $In_{0.18}Ga_{0.82}As$ channel layer. Hall measurement shows HEMTs structure grown on Si substrate with the electron mobility of 3,550cm^2/Vs. The effect of tilt substrate cause glide of the dislocation into the GaAs buffer layer tends to more effectively release the vertical component of tensile stress in the InGaAs channel layer. The stress filed caused by the steps are quite strong but decay rapidly with distance from the step, so the dislocation will not be pushed deeply in to the InGaAs channel layer, but should located within a few angstroms form the interface.

The most common method for avoiding the antiphase boundaries (APBs) at the GaAs/Ge interface is by the use of tilted substrates. The suppression of APBs can be achieved by using Si wafer with 6^o off (100) toward the <110> direction. For the substrates with a larger miscut angle ($>6^o$), in which the terraces between the steps are very narrower, the steps are so close to each other that no nucleus can be formed on the terraces. As the growth proceeds, the initial nuclei coalesce so that a single domain of GaAs is achieved [9]. In our study, the twins and the lattice defects finally disappeared when the GaAs/$Ge_{0.95}Si_{0.05}$/$Ge_{0.9}Si_{0.1}$/$Ge_{0.8}Si_{0.2}$ epilayers were grown on Si substrate with 6^o off (100) toward <110> direction. The TEM image of interface between $Ga_{0.95}Si_{0.05}$ metamorphic layer and GaAs layer as shown in Fig. 3(b). We saw dislocation loop at the interface. However, the antiphase boundaries and the cracks in the film were not found. The reason for this result could be the thinner buffer thicknesses in the

structures reduce effect of the thermal stress during the cooling stage. No APBs and cracks on the film were observed on the surface as shown in Fig. 4-4. The surface roughness was measured by AFM measurement (see Fig. 4-4.) The root mean square (RMS) was 16.56 Å and the roughness average (Ra) was 11.67 Å. The occurrence of the self-annihilation processes of APBs is very importation for the growth of device quality GaAs/$Ge_{0.95}Si_{0.05}$/$Ge_{0.9}Si_{0.1}$/$Ge_{0.8}Si_{0.2}$/Si epitaxial layers.

In order to verify the interdiffusion of Ge layer into GaAs, secondary ion mass spectroscopy (SIMS) technique was used. This technique yields quantitative measurements of dopants and impurity levels in semiconductors. According to Yuan Li etc al. [9], the formation of APBs was found to depend primarily on the magnitude of the misorientation angle of the (001) Si substrate. Fig. 4-5 shows the depth profile of the Ge diffusion into the GaAs layer. When the degree of the substrate misorientation is larger than 6^o off (100) toward <110> direction, it could suppress the antiphase boundary. Fig. 4-5 shows the distance of the Ge diffusion into GaAs layer to be about 0.25μm with 6^o misorientation (100) toward <110> direction of the substrate. The antiphase boundaries may be considered as defects, and Ge atoms could diffuse along the boundaries into the GaAs layer during the growth procedure. These results explain the relation of the Ge diffusion on the formation of antiphase boundaries [10].

4.3.2 Device process of AlGaAs/InGaAs HEMT's on Si substrates

For the HEMT device fabrication, the mesa isolation was done by wet chemical etching. Ohmic contacts were formed by evaporating Au/Ge/Ni/Au (20/40/14/180 nm) on n^+ GaAs layer and then alloyed at 350°C using RTA (Rapid Thermal Annealing). For T-gate definition, the bi-layer resist structure consisting of PMMA (polymethylmethacrylate) and (PMMA-MAA) (polymethyl methacrylate-methacrylic) were exposed by E-beam lithography (Leica EBML300) with footprint of 0.4 μm. Citrate acid/H_2O/H_2O_2 solution were used for gate recess process. Then, gate metals Ti/Pt/Au (100/100/300 nm) were deposited as the Schottky metal for the T-shaped gate. After T-gate formation, 100-nm-thick silicon nitride film was deposited by plasma enhanced chemical vapor deposition (PECVD) as the passivation layer.

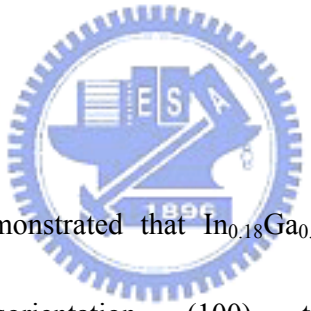
Another problem is the diffusion of Ge into the GaAs buffer layer, which the Ge atoms then act as dopant atoms in the GaAs layers. The antiphase boundaries may be considered as defects, and Ge atoms could diffuse along the boundaries into the GaAs layers during the growth process. Both the APBs formation and the Ge diffusion into the GaAs layers will affect the isolation between devices and result in the increased leakage current and thus influence the pinch off characteristics of the devices.

The isolation step in this study was carried out by wet chemical etch. The HEMT structure was etched 300nm down to the AlGaAs buffer layer. After isolation etch, the HEMT structure

demonstrated a leakage current of 0.016μA/μm when the bias voltage was up to 14.2V as measured by the isolation pattern with a pad spacing of 10μm, the result is as shown in Fig. 4-6. The data indicate that use of 6° off substrate had efficiently suppressed the APBs formation and the Ge diffusion into the GaAs layer, and the AlGaAs/GaAs buffer layer and the Ge/Ge_xSi_{1-x} buffer layer qualities were good enough for the device application.

The I-V characteristics of the fabricated 0.35 × 100 μm^2 AlGaAs/InGaAs HEMTs on Si with Ge/Ge_xSi_{1-x} metamorphic buffer layers were measured. The drain-to-source saturation current (I_{dss}) was 150 mA/mm at V_{DS}=1.5V and the pinch off voltage of the device was -1.6V. The device showed very good pinch off characteristics as shown in Fig 4-7(a). The maximum transconductance measured at V_{DS} =1.5V was 155mS/mm as shown in Fig 4-7(b). The drain-to-gate breakdown voltage (V_{BK}) was 3.5V, which was defined at a gate current of 1mA/mm. For the device grown on the Ge substrate, the drain-to-source current (I_{ds}) was 190 mA/mm as shown in Fig 4-8(a). The transconductance measured at V_{DS} =2V was 220mS/mm as shown in Fig 4-8(b). The drain-to-gate breakdown voltage (V_{BK}) was 4V. For the growth of heterostructure materials, the thermal expansion coefficient of the substrate affects the film quality of the heterostructure layers grown when the thermal mismatch between these two materials is large and the epilayer grown is thick. The large thermal mismatch between the Si substrate and the GaAs layer (62%) may cause the threading dislocations and cracks in the film grown during the growth process. These defects can resist in-plane electrical current flow

to introduce electrical shorting paths in vertical current [7]. In this study, the HEMT structure on the Si substrate demonstrated good performance, despite the high temperature MOCVD growth process and the large thermal expansion coefficient difference between GaAs and Si. This may be attributed to the thin buffer layer achieved between the Si substrate and the HEMT structure by using Si^+ ion implantation to enhance the Ge_xSi_{1-x} layer strain relaxation and the use of two steps Ge_xSi_{1-x} layer growth to block the dislocation propagation. However, the better performance of the HEMT device on the Ge substrate could be due to the lower defect density and smoother surface of the Ge substrate.



4.4 Conclusions

In summary, we have demonstrated that $In_{0.18}Ga_{0.82}As$ channel HEMT grown on Si substrate with 6^o misorientation (100) toward <110> direction and $Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}/Ge_{0.8}Si_{0.2}$ metamorphic buffer layers. Due to the Si substrate with Si^+ pre-on-implantation and interface-blocking in Ge_xSi_{1-x} metamorphic buffer layers could reduce the buffer thickness to 1μm, the lattice mismatch and thermal mismatch between GaAs and Si substrate could be solved. The misorientation Si substrate suppressed the formation of antiphase boundary to inhibit the Ge atoms interdiffusion into the GaAs layer. High electron mobility of $In_{0.18}Ga_{0.82}As$ HEMT structure on Si substrate was 3,550cm^2/Vs. The distance of the Ge diffusion into GaAs layer is about 0.25μm with 6^o misorientation (100) toward <110>

direction of the substrate. The short distance of Ge interdiffusion in the GaAs layer could not result in high leakage current of HEMT structure on Si substrate which could be applied for low power and high performance electronic device. A working AlGaAs/InGaAs HEMT device on Si substrate was investigated. The 0.4 μm AlGaAs/InGaAs HEMT fabricated on the Si substrate demonstrated a transconductance of 155 mS/mm and a saturation channel current of 150 mA/mm with well behaved pinch off characteristics. The device also had a breakdown voltage of 3.5Volt. After device isolation process, the leakage current of the HEMT structure on Si substrate was 0.016μA/μm at a bias voltage of 14.2V as measured by the isolation pattern. The results indicate that the buffer layer quality was good with no Ge diffusion into the GaAs layers and no APBs formation. The good HEMT performance is attributed to the very thin buffer layer (1μm) achieved using Si^+ ion implantation and two steps buffer layer growth technique, which helps alleviate the stress effect caused by the large expansion coefficient between these two materials. The technology demonstrated shows great potential for III-V/Si integration and can be applied to the future optoelectronics and microelectronics applications.

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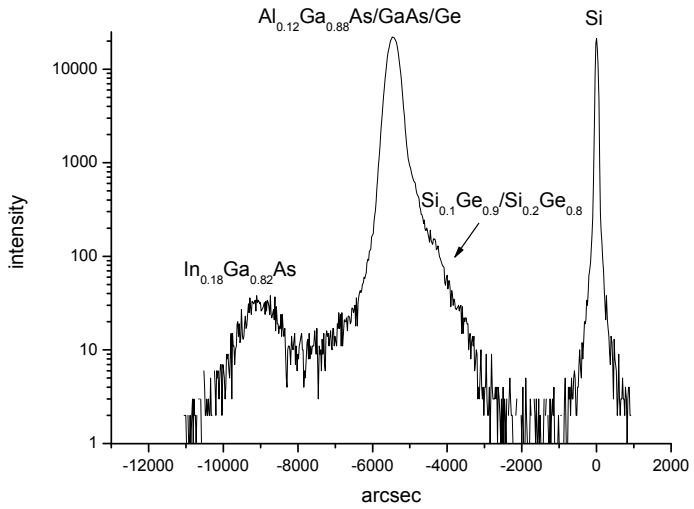
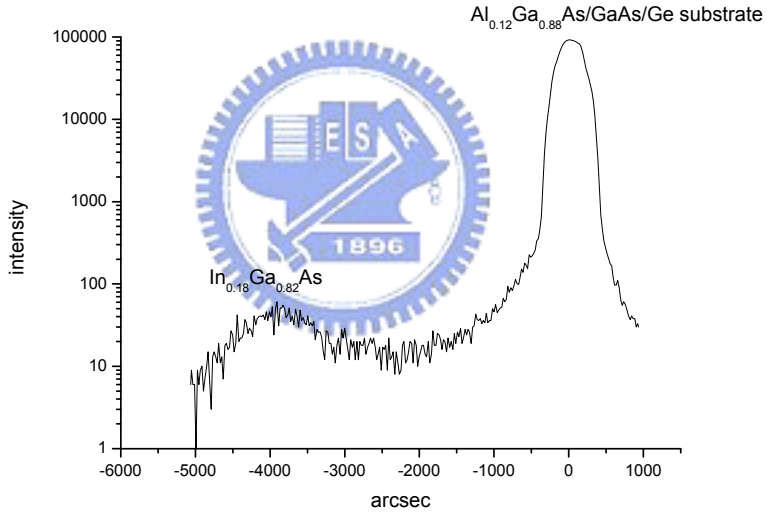
200Å	GaAs	2×10^{18}	n^+
320Å	$Al_{0.12}Ga_{0.88}As$	1.7×10^{18}	n^+
40Å	$Al_{0.12}Ga_{0.88}As$	undoped	
150Å	$In_{0.18}Ga_{0.82}As$	undoped	
1000Å	GaAs	undoped	
5000Å	$Al_{0.12}Ga_{0.88}As$	undoped	
2μm	GaAs	undoped	
0.55μm	$Ge_{0.95}Si_{0.05}$	layer	
0.25μm	$Ge_{0.9}Si_{0.1}$ metamorphic buffer		
0.2μm	$Ge_{0.8}Si_{0.2}$ metamorphic buffer		
Si substrate			

Fig. 4-1. The layer structure and the growth conditions for InGaAs channel HEMT grown on Si substrate with Ge_xSi_{1-x} metamorphic buffer layers. Note that Ge_xSi_{1-x} was grown with two step growth with the Ge composition set at 80%, 90% and 95%.



(a)



(b)

Fig. 4-2 (a) Double crystal x-ray difference data at [004] orientation for a HEMT structure grown on a Si substrate (b) Double crystal x-ray difference data at [004] orientation for a HEMT structure grown on a Ge substrate.

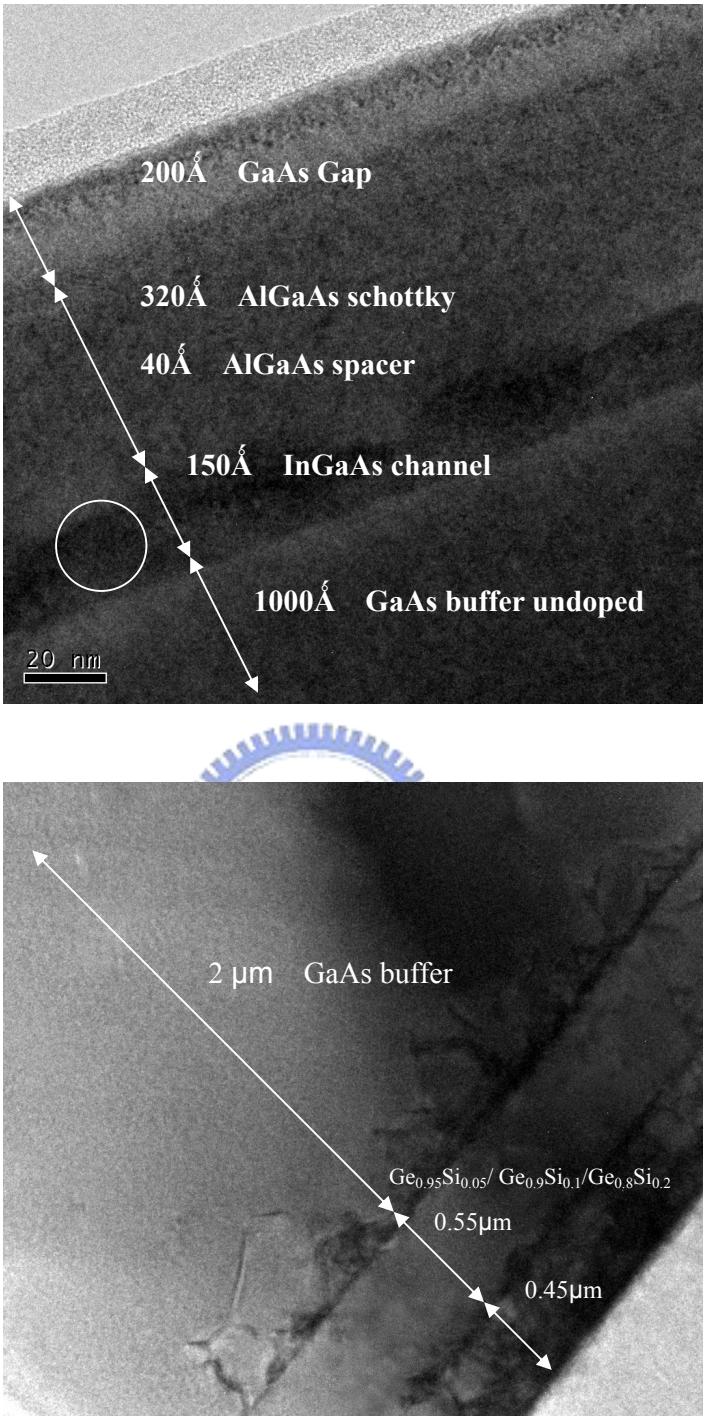


Fig. 4-3(a) The cross section TEM image of a HEMT structure grown on Si substrate. (b) The cross section TEM image of the interface between the GaAs layer and $Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}/Ge_{0.8}Si_{0.2}$ metamorphic buffer layer.

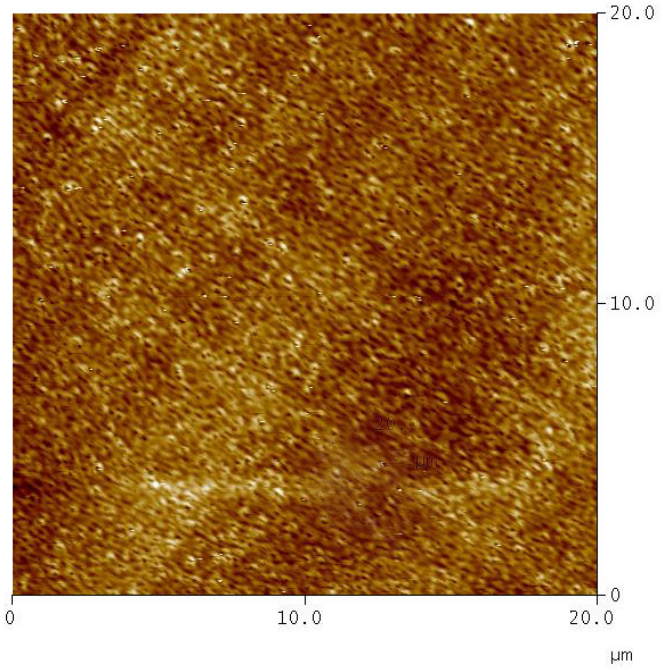


Fig. 4-4 The AFM image of HEMT structure grown on Si substrate. The root mean square (RMS) of the roughness is 0.38nm.

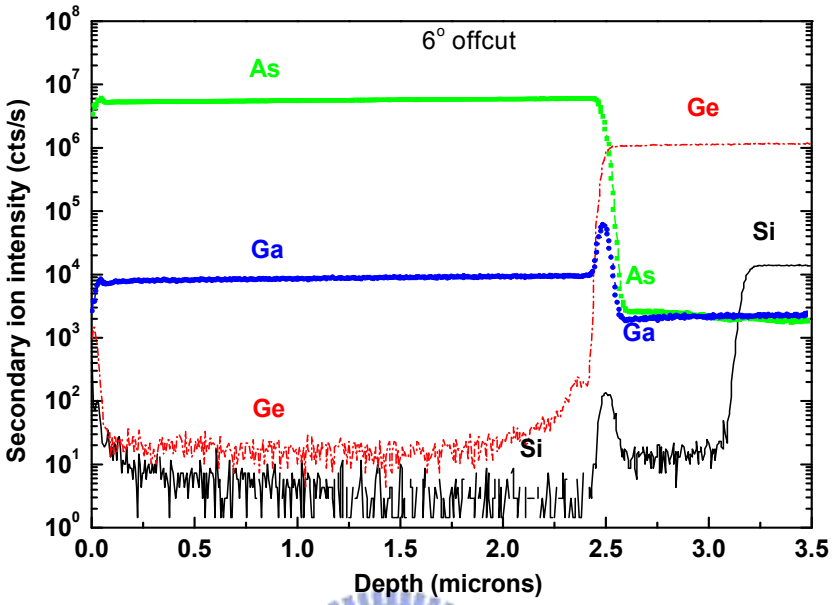


Fig. 4-5 SIMS profiles of As, Ga and Ge in a 2 μ m thick GaAs layer grown on Si with 6^0 off angle toward [110] direction.

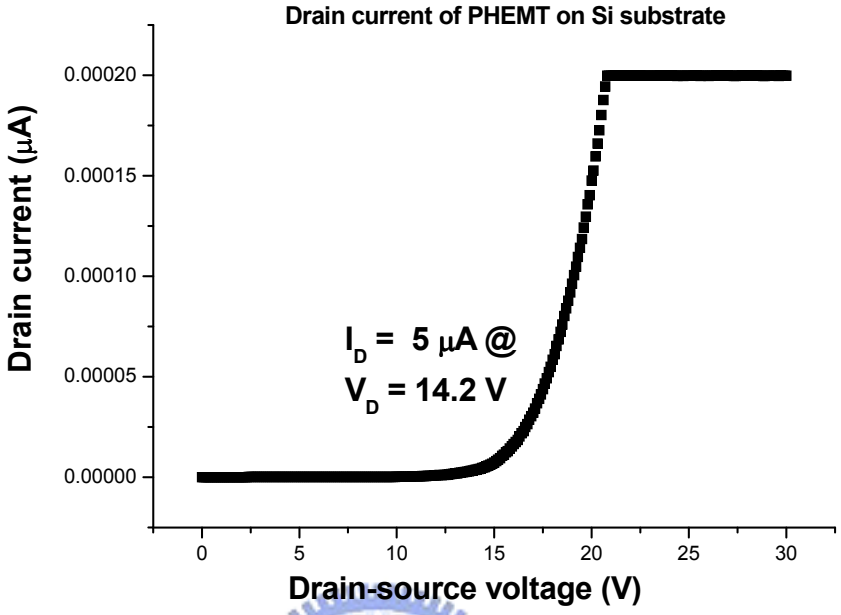
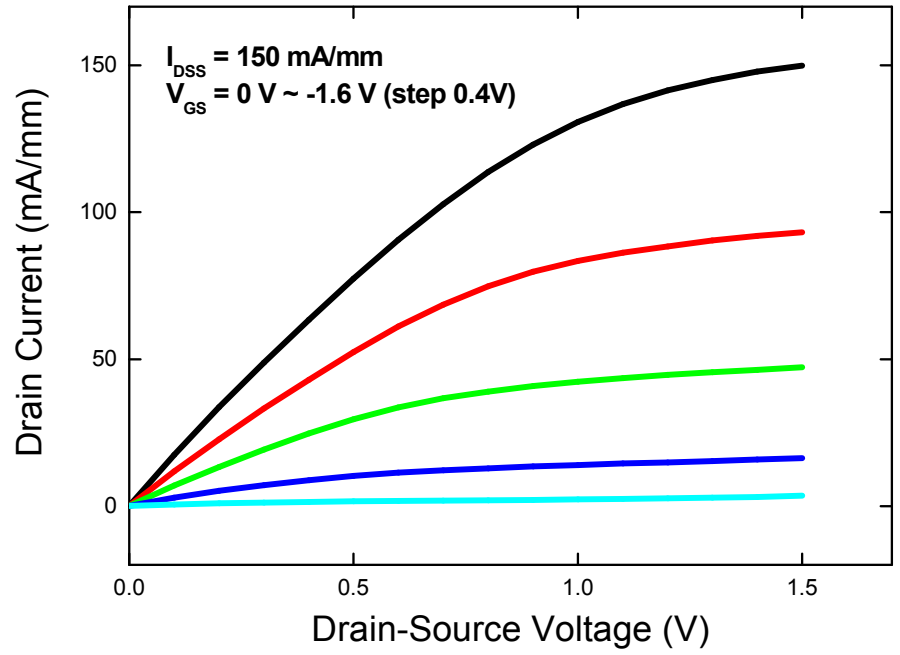
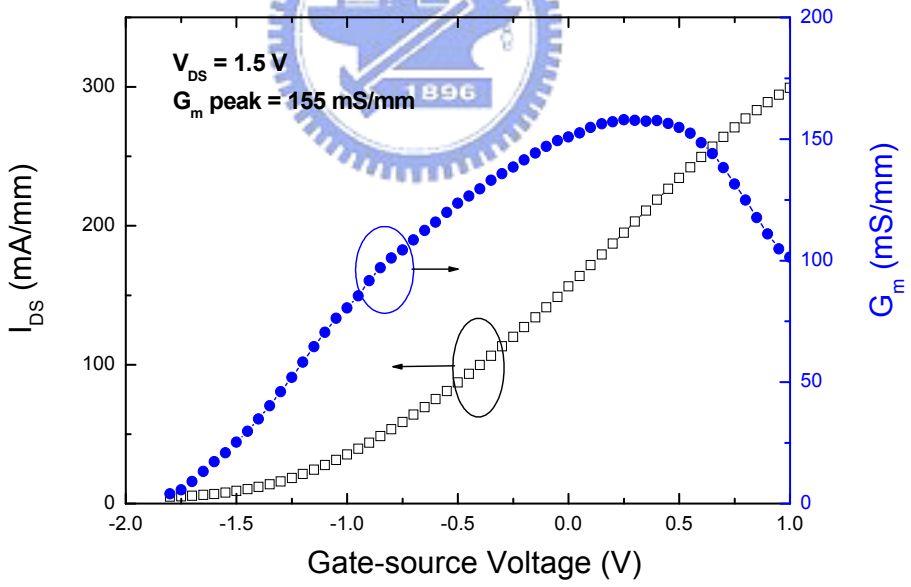


Fig. 4-6 Leakage current as a function of the bias voltage. The data was measured on a pad pattern of 300 μm wide with a spacing of 10 μm between pads.



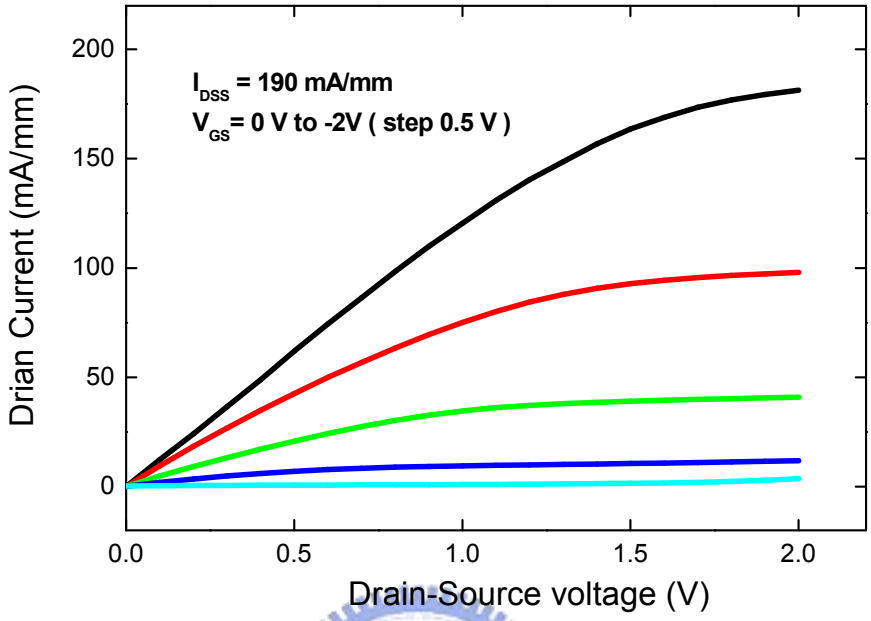
(a)



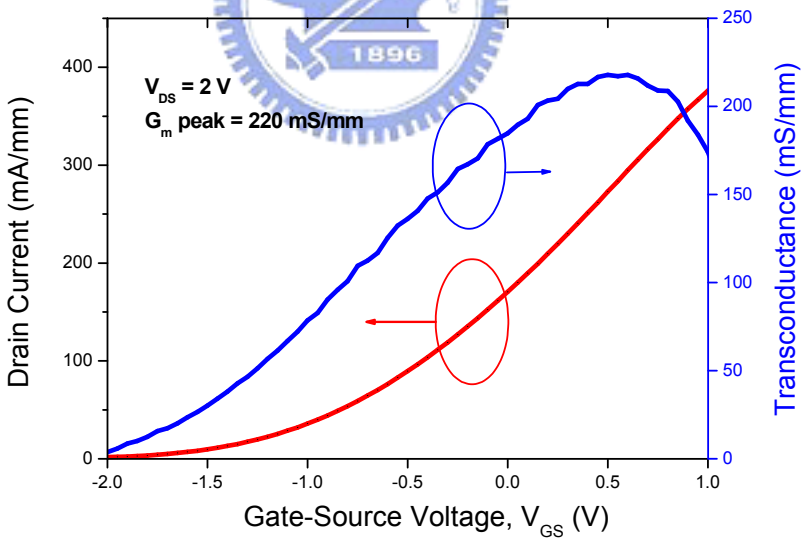
(b)

Fig. 4-7 (a) I-V characteristics of a 0.35 μm × 100μm AlGaAs/InGaAs HEMT on a Si substrate with Ge/GeSi metamorphic layer.

(b) Transconductance and drain-source current vs. V_{GS} of a 0.35 μm × 100μm AlGaAs/InGaAs HEMT on the Si substrate with Ge/GeSi metamorphic layer.



(a)



(b)

Fig. 4-8 (a) I-V characteristics of a 0.35 μm × 100μm AlGaAs/InGaAs HEMT on the Ge substrate.

(b) Transconductance and drain-source current vs. V_{GS} of the 0.35 μm × 100μm HEMT on the Ge substrate.

Chapter 5

Growth of InAs channel HEMT on Si Substrates for high-speed electronic applications

5.1 Introduction

III-V compound semiconductors have high electron mobility and direct band gap. Due to these characteristics, III-V compound semiconductors are used in the applications as electron devices, magnetic sensors and used as a base to produce far-infrared InSb/$In_xAs_{1-x}Sb$ supperlattice photodetectors. In order to take the advantages of the superior GaAs material properties and the low cost of Si manufacturing, III-V/Si integration has been extensively studied in the past. The large lattice mismatch, different thermal expansion coefficients and antiphase boundary formation (polar on non-polar material growth) create formidable challenges. Several laboratories have reported the successful growth of GaAs on Si using tilt substrate [1]. However, direct growth of the InAs MHEMT structure on Si substrate is very difficult because of large lattice mismatch (12%) between InAs and the Si substrate. NTT lab has succeeded in the growth of InAs MEHMT on GaAs substrate using AlSb buffer layer in the past. In the UHV/CVD system grown Ge_xSi_{1-x} metamorphic buffer layers was used to integrate the InAs MHEMT on the Si substrate. High quality InAs HEMT structure was gown on Si substrate with few dislocations. In addition, the electron mobility of the InAs MHEMT

grown on Si substrate with 6° angle off toward to [110] was as high as 27,300cm^2/v-s. The use of the tilted substrate properly suppresses the antiphase boundary (APB) formation for the GaAs grown on the Si substrate which is accounted for the high mobility observed [4].

5.2 Experimental procedures

The experiments in this work are composed of two parts. First, the growth of the SiGe and Ge buffer layers was carried out using an ultra-high vacuum chemical vapor deposition (UHV/CVD) system with a base pressure of less than 5×10^{-9} torr is described. A 4-inch Si wafer 6° off(100) toward <110> direction, was cleaned by dipping into a 10% HF solution with subsequent high-temperature baking at 800℃ in the growth chamber for 5 min. Then, a 0.8 μm $Ge_{0.9}Si_{0.1}$, a 0.8 μm $Ge_{0.95}Si_{0.05}$, and a 1.0 μm Ge layer were grown at 480℃ in sequence. Between successive layers, growth procedure was interrupted for an in situ 15 min 750℃ annealing. After the Ge layer was grown on Si substrate, the sample was switched to the MBE system to grown InAs MHEMT on the Ge/GeSi/Si heterostructure. The depositions were performed in a MBE chamber equipped with reflection high-energy electron diffraction (RHEED). The background and growth pressures in the growth chamber were about 4×10^{-11} and 2×10^{-9} Torr, respectively. The structures of the epilayers were 1μm GaAs buffer, and AlSb nucleation layer of 150nm grown at 450℃. A GaSb/AlSb superlattice with 10 pairs was used to modify the surface of AlSb and suppress the misfit dislocations at the interface [14]. The

Fig. 5-1(a) shows the diagram of the whole epilayers structure on GaAs. Fig. 5-1(b) shows the diagram of the whole epilayers on a Si substrate with 6^{o} off (100) toward <110> direction.

The quality of the structure of the layer was investigated with several techniques. The lattice mismatched, composition and crystalline quality were derived from the X-ray diffraction rocking curves. This TEM samples were prepared by using the standard 'sandwich' technique followed by ion milling for this study. Structural analyses of the epitaxial layers were performed on the cross-section by high resolution transmission electron microscope (HRTEM). This study was carried out on a Joel-2100 field emission electron microscope operating at 200 kV with an interpretable resolution of 0.16nm. Localized spatial information from HRTEM micrographs was obtained by digital diffractograms (DDFs). The method was based on the measurements of the interplanar spacing in reciprocal space and was used to determine the frequency and amplitude of the lattice images. Image simulation was performed using the Cerius simulation program.

5.3 Results and discussions

5.3.1 Suppression of the misfit dislocations at the interface between AlSb and GaAs layer with tilted substrate.

Fig. 5-2 shows the cross section of the structure of an InAs MHEMT on a Si substrate by TEM analysis. TEM images are connected in order to show the detailed of the structure from

top bottom. The structures of the epilayers are 1.0μm GaAs buffer layer, 150nm AlSb nucleation layer, 10 pairs of GaSb/AlSb superlattice 10 pairs used to modify the surface of AlSb and suppress the misfit dislocations at the interface, then a 2μm $Al_{0.5}Ga_{0.5}Sb$ buffer layer, GaSb/AlSb superlattice to block the threading dislocations. Finally, the HEMT structure consists of a 15nm InAs channel layer, a 10nm $Al_{0.5}Ga_{0.5}Sb$ Schottky layer, and a 5nm GaSb cap layer. Previously, we have succeeded growing pure Ge on Si substrate via a novel Ge_xSi_{1-x} metamorphic buffer layer. In the case GaAs layers were grown on a Si substrate with $Ge/Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}$ as buffer which having low mismatch (< 0.12%) and low thermal expansion difference (<2%) between GaAs and Ge. The most common method for avoiding antiphase boundaries (APBs) at the GaAs/Ge interface is by the use of tilted substrates and sufficient thermal annealing. The suppression of APBs can be achieved by using Si wafer with 6^o off (100) toward <110> direction. Fig. 5-3(a) shows the APBs looking through the GaAs layer forward the surface. Fig. 5-3(b) shows the GaAs layer grown on Si substrate with $Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}$ metamorphic buffer layers which is free of APBs. Detailed discussions for the growth of APBs free GaAs on Si can be found in the literature [3]. A double crystal X-ray investigation data shows the structure of an InAs MHEMT on a GaAs substrate and on Si substrate are shown in Fig 5-4. Fig. 5-4(a) shows the peaks consisting of GaAs substrate; InAs channel layer, GaSb cap layer, $Al_{0.5}Ga_{0.5}Sb$ buffer layer and AlSb nucleation layer. Fig. 5-4(b) shows the peaks of the structure grown on Si substrate, these peaks are from

GaAs/Ge/$Si_{0.05}Ge_{0.95}$/$Si_{0.1}Ge_{0.9}$ metamorphic buffer layers, $Al_{0.5}Ga_{0.5}Sb$ buffer layer and AlSb nucleation layer, InAs channel layer, and GaSb cap layer. The lattice mismatch ($\triangle a_o/a_o$) is 13% between AlSb and the Si substrate. AlSb has been shown to produce defect-free buffers on the lattice mismatched substrates. The growth of AlSb on GaAs results in a smooth surface with very few threading dislocations according to the transmission electron microscopy (TEM) analysis [15]. The lattice mismatch between AlSb and GaAs is 7.8%. It results in compressive stress between AlSb and GaAs layers. Comparing the positions of all peaks and fixed with GaAs peak on the DC x-ray data, it appears that the AlSb peak of the InAs MHEMT on Si substrate shifted by 425 arcsec to the $Al_{0.5}Ga_{0.5}Sb$ peak as shown on Fig. 5-4(c). The distortion of the lattice and the higher strain energy at the interface was by the compressive stress. As we known, the high strain energies could be relaxed by forming dislocations or by three dimension growth. The initial nucleation of the highly mismatched materials AlSb layer on GaAs leads to forming self-assembled QDs. The continuation of the growth results in the QD coalescence followed by undulations of the AlSb layer. It has large strain energy and can lower its total energy by forming isolated thick islands. The undulations increase the surface area of the AlSb and provide strain relief. In this case, the stress on a crystal surface can provide a natural driving force for the nanostructure formation and the three-dimensional island formation for the lattice mismatched epitaxial growth on the substrates. At the initial stage of the heteroepitaxy growth of the AlSb layer on GaAs, a three-dimensional nucleation

step is shown to take place before the surface is smoothed out by a thicker layer growth [7]. The lower temperature AlSb buffer layer will reduce the surface diffusion; atoms can only diffuse a short distance before they are incorporated. In additional the growth temperature is too low to allow for significant atomic mobility. The tilted substrate will increase the elastic deformation and induce the atom migration at low temperatures. Elastically driven diffusion atoms attracted to the core region [8]. The dislocations are very hard to form on the island surface [10]. The tilted Si substrate with 6^{o} off (100) toward to [110] was used to supply more nucleation sites, the atoms are incorporated without longer diffusion distance and thus reduce the dislocations at the interface The undulating material contains misfit dislocations parallel to the (100) plane. The tilted substrate also increases the height for the steps resulting in higher energy for dislocation climbing and inhibits the misfit dislocation moving. These don't propagate vertically as threading or screw dislocations. The tilted substrate inhibits the dislocation climbing. Fig. 5-5(a) shows the formation of misfit dislocations at the interface between AlSb layer and GaAs substrate. Fig. 5-5(b) only shows few misfit dislocations at the interface between the AlSb layer and the GaAs layer by using Si substrate with 6^{o} off (100) toward to [110]. The tilted substrate will increase the elastic deformation and induce the atoms migration at low temperature. The dislocation climb necessary for the sessile configuration to move, is not possible and the dislocations cannot be produced at the island surface once it is far from the interface [11].

5.3.2 Growth of high electron mobility InAs MHEMTs on Si substrates with 6° off angle toward to [110]

Fig. 5-4(c) shows that the FWHM of the an InAs channel on a Si substrate is about 358 arcsec. The FWHM of the InAs channel on a GaAs substrate is about 506 arcsec. The improved results on tilted substrates can be attributed in part to the fact that tilted surfaces have steps terminated with In. As incident on the surface can form three bonds, two to the In atoms on the surface, and one to the In atom on the (111) face of the step [11]. The lateral steps might arise from the initiation of InAs epitaxy at the step edges on the misoriented substrate, they might also be enhanced by lateral and/or vertical segregation of In atoms to improve the film quality [12]. Another mechanism was suggested by Y. Chen and N.D. Zakharov, etc [13]. When the film exceeds a crystal thickness, misfit dislocation are introduced, possibly as half-loops from the surface, or as loops nucleated at a defect near the interface. This asymmetry in dislocation density can be explained by the asymmetry in the dislocations glide force on the two (111) slip planes caused by the interfacial misorientation. Glide of the dislocation into the $Al_{0.5}Ga_{0.5}Sb$ buffer layer tends to be more effective releasing the vertical component of tensile stress in the InAs channel layer. The stress fields cause by the steps is quite strong but decay rapidly with distance from the step, so the dislocation will not be pushed deeply in to the InAs channel layer, but will locate within a few angstorms from the interface [13-14].

According to the high resolution TEM image shown in Fig. 5-6, the lattice image shows a the dark areas between between $Al_{0.5}Ga_{0.5}Sb$ interface and the InAs channel layer are areas with high strain energy. The lattice constant of InAs layer is smaller than the $Al_{0.5}Ga_{0.5}Sb$ layer. The large lattice mismatch cause high strain energy. This results in the tensile strain in the InAs layer and compressive strain in the $Al_{0.5}Ga_{0.5}Sb$ layer. This result explains why the position of InAs peak at DC x-ray measurement shift 341 arcsec to $Al_{0.5}Ga_{0.5}Sb$ peak. We saw the distortion of several lattices at the interface between the $Al_{0.5}Ga_{0.5}Sb$ layer and InAs layer. In addition, the Hall measurement shows the electron mobility (27,300 $cm^2/v.s$) of the InAs MHEMT grown on Si with 6^o off (100) toward to [110]. Fig.5-7(a) shows that Reciprocal Space Map data of [004] orientation of InAs/AlGaSb on a Si substrate. The Y axial is ω to 2θ scan for [004] orientation, the X axial is ω scan for [110] orientation. The peaks consisted of Si, GaAs/Ge/GeSi, InAs channel, GaSb cap, $Al_{0.5}Ga_{0.5}Sb$ buffer layer peak. Fig. 5-7(b) shows that Reciprocal Space Map data of a [004] orientation of the InAs channel on the GaAs substrate. Because the Si substrate is 6^o off (100) toward to [110], it was observed that the Si peak, GaAs/Ge/GeSi peak, InAs channel peak and $Al_{0.5}Ga_{0.5}Sb$ peak are not in [004] orientation.

In this geometry, the equations for the lattice parameters become:

$$a_{\perp} = a_s \cdot \frac{\sin\theta_B}{\sin(\theta_B + \Delta\theta)} \cdot \frac{\cos\phi}{\cos(\phi + \Delta\phi)}$$

$$a_{ll} = a_s \cdot \frac{\sin\theta_B}{\sin(\theta_B + \Delta\theta)} \cdot \frac{\sin\phi}{\sin(\phi + \Delta\phi)}$$

Where θ_B is the Bragg angle for the diffraction of the substrate, and $\Delta\theta$ the shift from that position of the layer peak; ϕ is the inclination of the reflecting planes relative to the surface for the substrate, and the $\Delta\phi$ is difference in angle between the equivalent planes of the substrate and epilayer.

The parameters $\Delta\theta$ and $\Delta\phi$ are given by:

$$\Delta\theta = \frac{\Delta\omega_{ge} + \Delta\omega_{g_i}}{2}$$

$$\Delta\phi = \frac{\Delta\omega_{ge} - \Delta\omega_{g_i}}{2}$$

The relaxed lattice parameter can now be calculated by:

$$a_r = \frac{-(a_\perp \cdot (\nu - 1) - 2 \cdot \nu a_{ll})}{1 + \nu}$$

The epilayer composition can be calculated using a known relationship between the lattice parameter and the composition, and the percent relaxation is defined by:

$$\%\ \text{Relaxed} = \frac{a_{ll} - a_{sub}}{a_r - a_{sub}} \cdot 100\%$$

The thicknesses of the InAs channel and the GaSb cap layer are 10nm and 5nm, which are within in critical thickness. The InAs channel layer grown on Si substrate and GaAs substrate has a 2% and 6% relaxation, respectively.

In the literature, it is shows [15] that InSb grown on Si substrate with [100] orientation, leads to APBs were through the epilayer to the surface forming the square line on the surface. We did not observe any APBs on the surface by using the Si substrate with 6^{o} off angle toward [110]. In addition, comparing InAs MHEMTs grown on GaAs substrates and grown on Si substrates with 6^{o} off angle toward to [110], the tilted substrate increases the height of the steps. The atoms accumulated along the steps on the surface, which resulted in rougher surface. Fig. 5-8(a) shows an AFM image of an InAs channel grown on a GaAs substrate. The Ra (roughness average) value is 1.68nm for per 10μm scale. Fig. 5-8(b) shows the detailed surface image for per 1.0μm scale. We used an AFM measurement line-scan of the surface and calculated the vertical height and horizontal distances for each small island to be 5nm and 111nm, respectively. Fig. 5-9(a) shows the AFM image of an InAs channel grown on a Si substrate with 6^{o} off angle toward to [110]. The Ra (roughness average) value is 3.20nm for per 10μm scale. Fig. 5-9(b) shows the detailed surface image at 1.0μm scale. AFM measurement line-scan was used on the surface to calculate the vertical height and horizontal distances for each small island, the two values to be 5nm and 290nm, respectively.

5.4 Conclusions

The integration of the InAs MHEMT on a Si substrate via GeSi metamorphic buffer layers has been demonstrated. The tilted Si substrate with 6^{o} off (100) toward [110] supplies more nucleation sites, the atoms are incorporated without longer diffusion distance and thus reduces dislocations at the interface and improve the crystalline between AlSb and GaAs layer. The electron mobility of the InAs MHEMT grown on Si with 6^{o} off angle toward to [110] achieved 27,300cm^2/v-s which is height ever reported on a Si substrate so far. .

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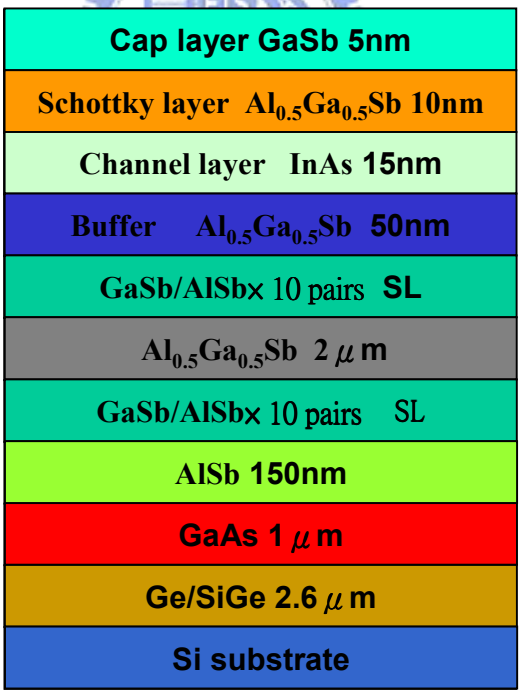
(a)



(b)

Fig. 5-1 (a) Schematic diagram of InAs MHEMT on GaAs substrate.
(b) Schematic diagram of InAs MHEMT on Si substrate

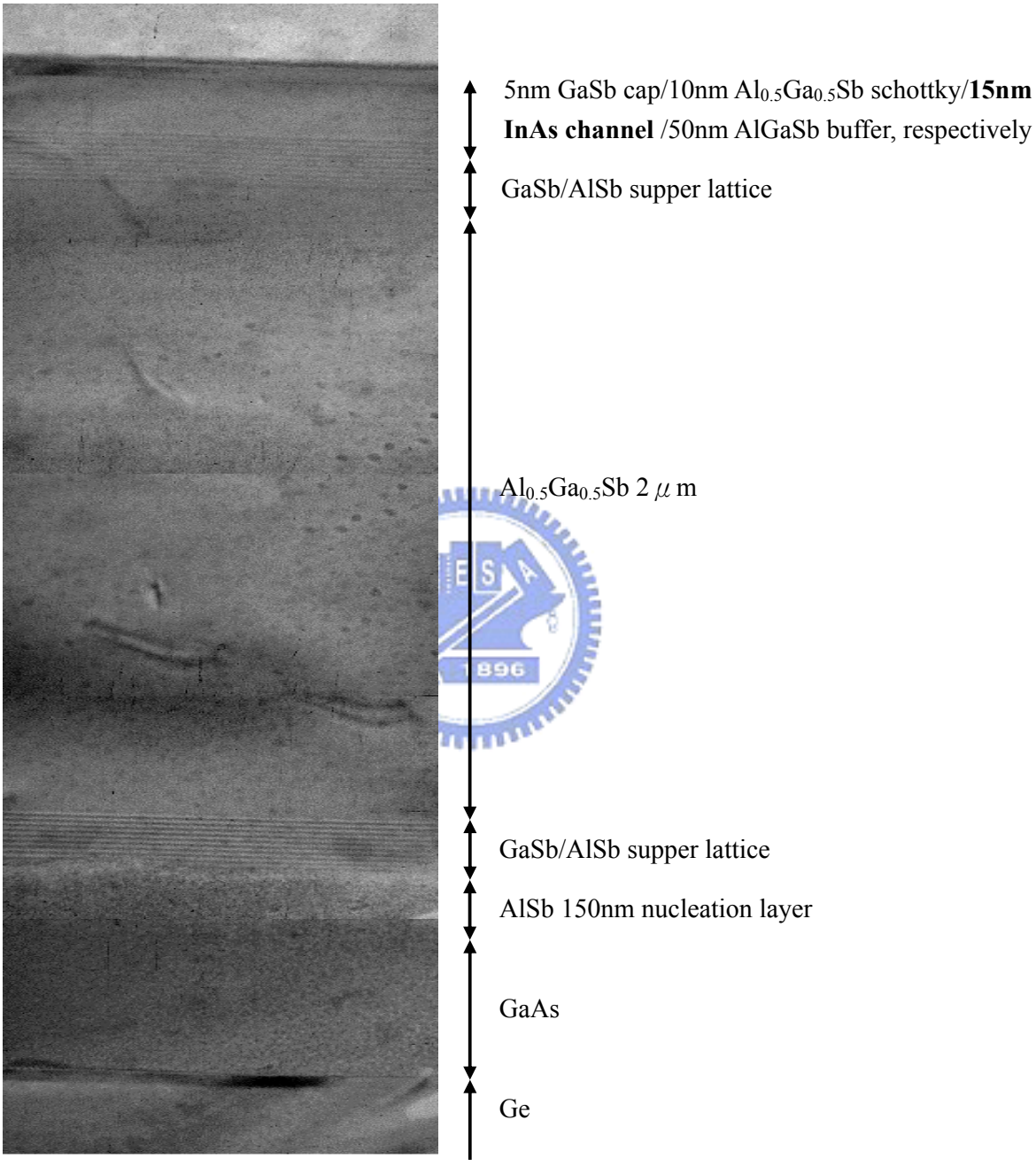
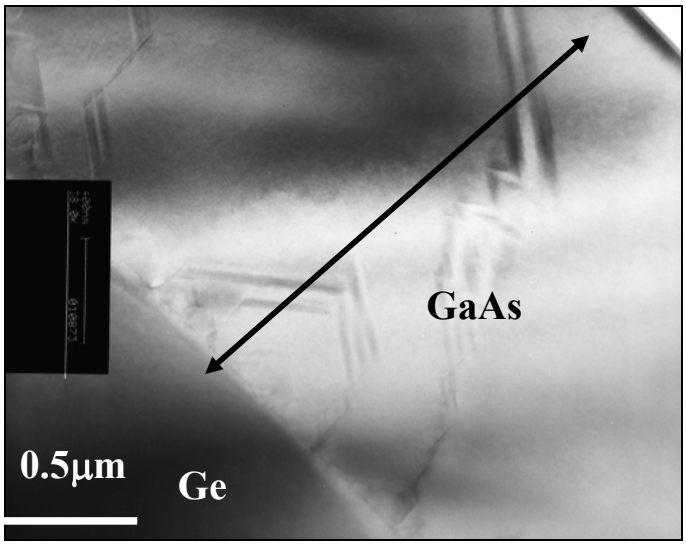
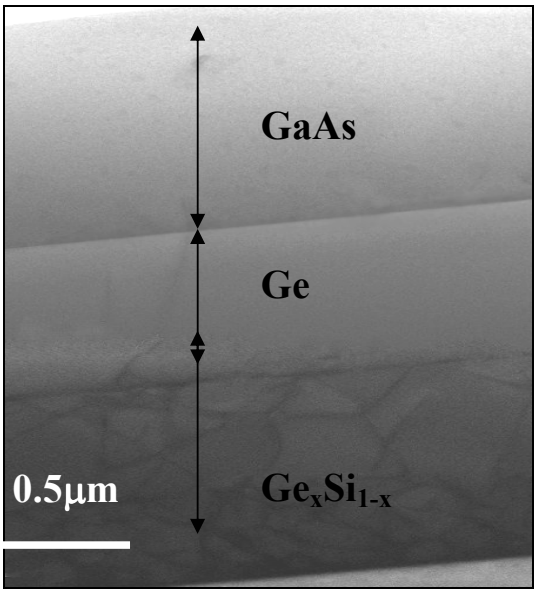


Fig. 5-2 Cross-sectional TEM image of InAs MHEMT epilayer structure on Si



(a)



(b)

Fig. 5-3 (a) The cross-section TEM image of antiphase boundary formation at GaAs layer on Si without off angle. (b) The suppression of antiphase boundary formation by Si substrate 6^0 off angle toward to [110].

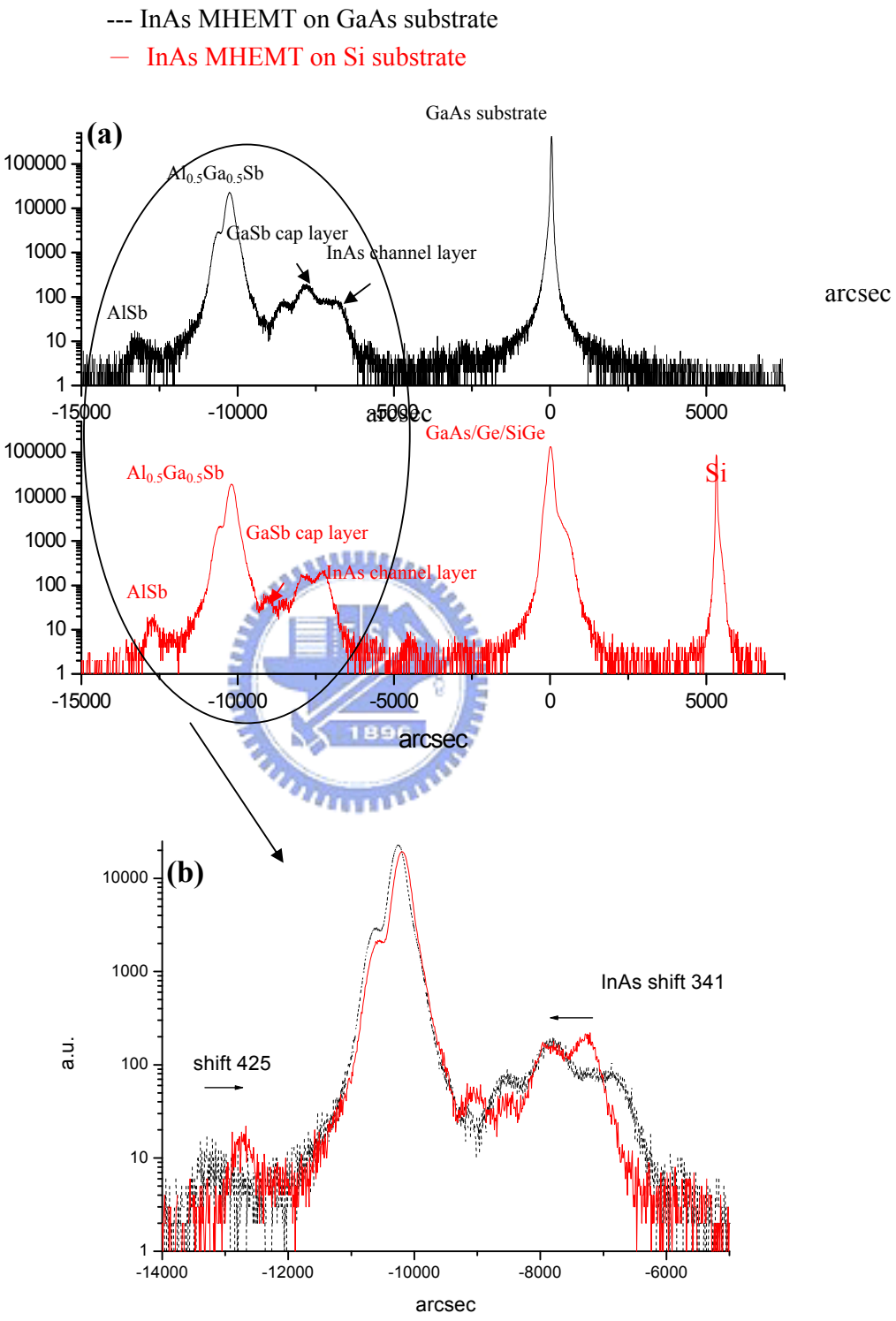
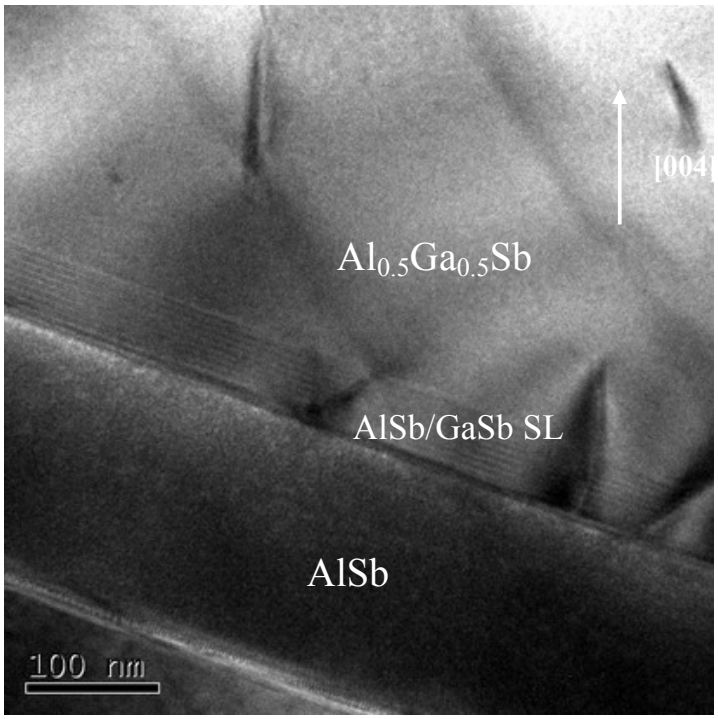
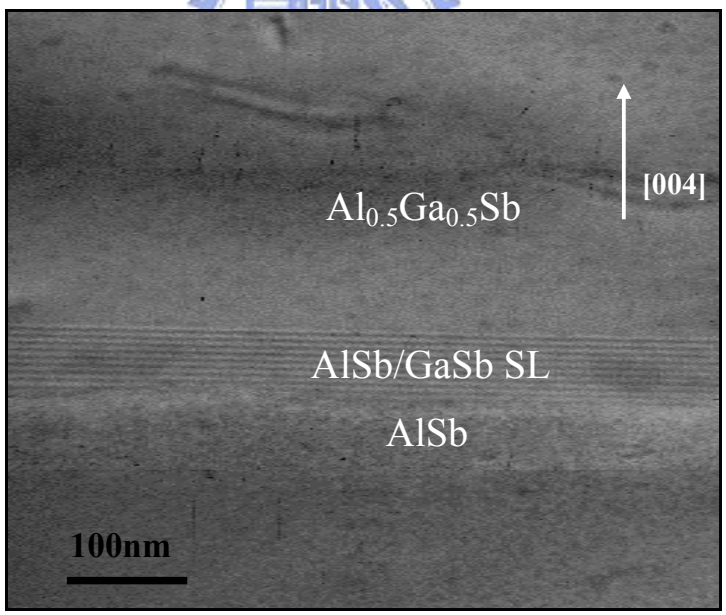


Fig. 5-4 (a) The comparison double crystal x-ray [004] orientation of crystalline quality of InAs MHEMT structure on GaAs substrate and Si substrate. (b)The detail comparison of InAs MHEMT structure on GaAs substrate and Si



(a)



(b)

Fig. 5-5 High resolution TEM image of AlSb nucleation on (a)GaAs substrate (b) Si substrate

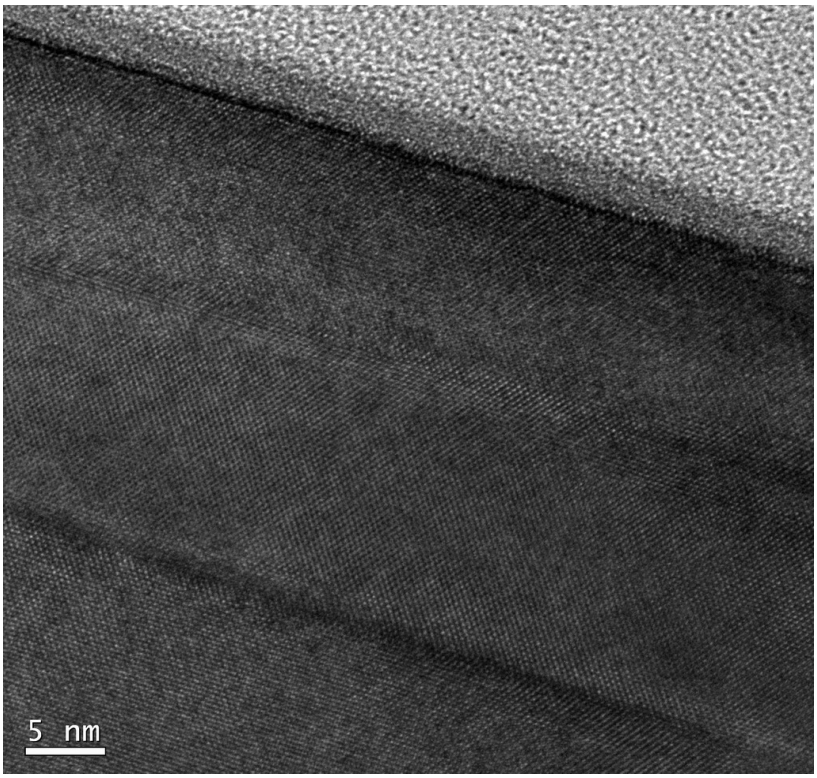
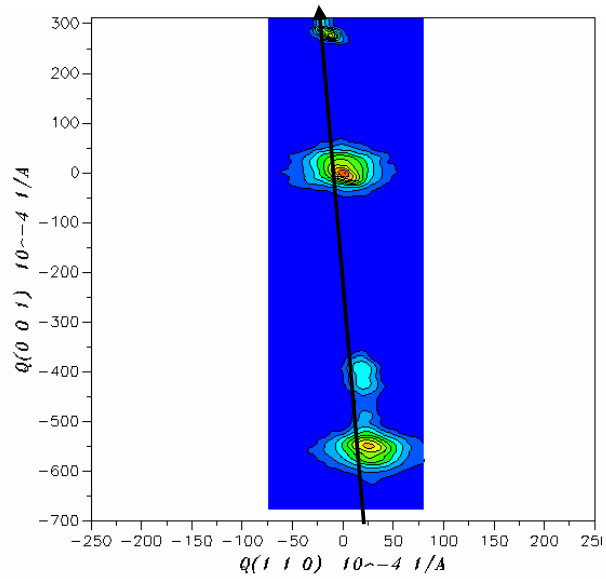
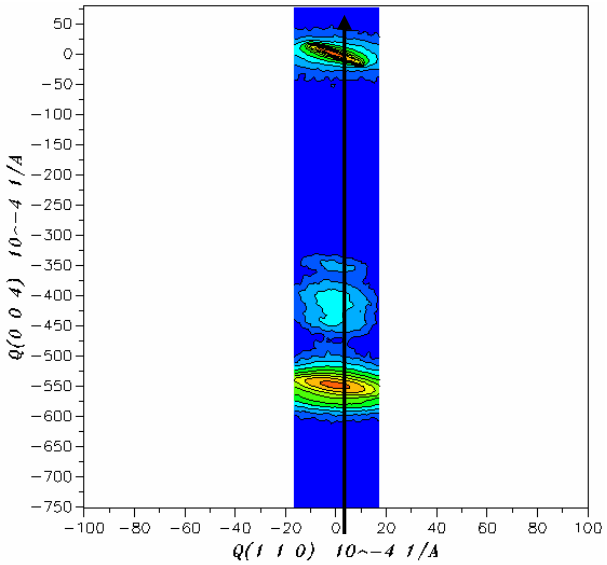


Fig. 5-6 High resolution TEM image of InAs channel on Si substrate



(a)



(b)

Fig. 5-7 (a) Reciprocal Space Map data [004] orientation of InAs/AlGaSb on GaAs substrate
(b) Reciprocal Space Map data [004] orientation of InAs/AlGaSb on Si substrate 6^{o} off angle toward to [110]

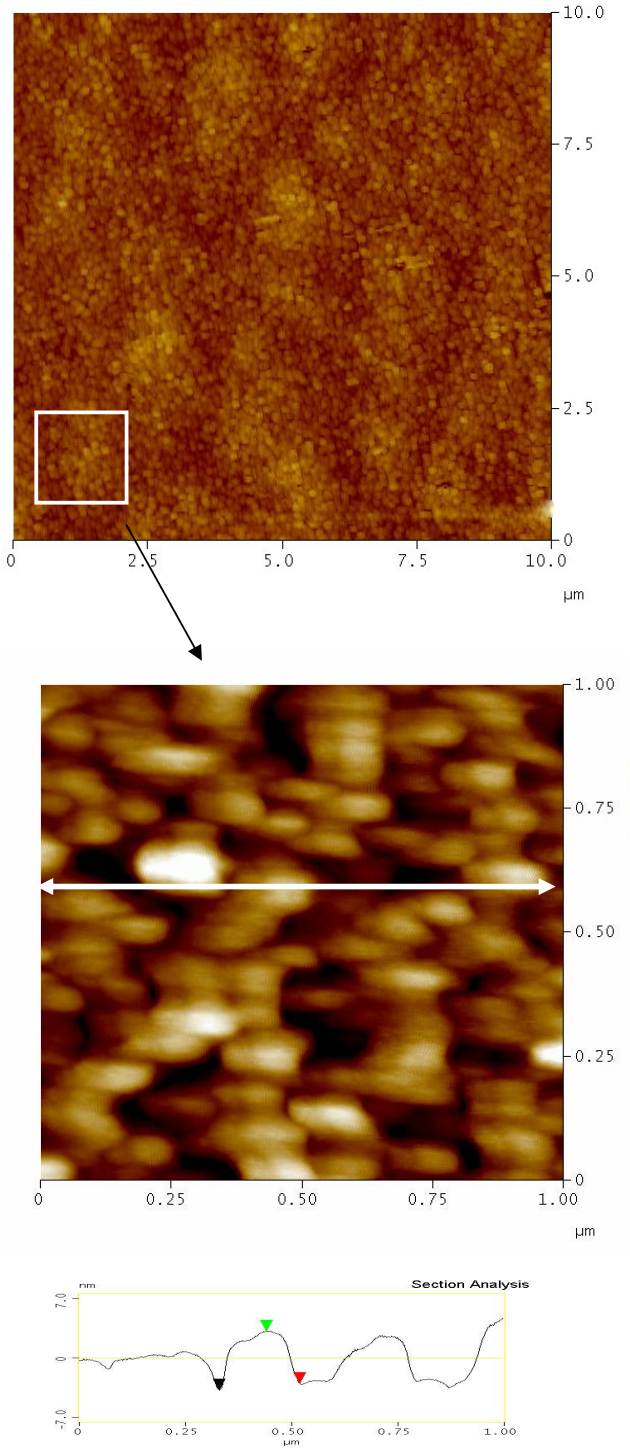


Fig. 5-8 AFM image of InAs MHEMT on GaAs substrate

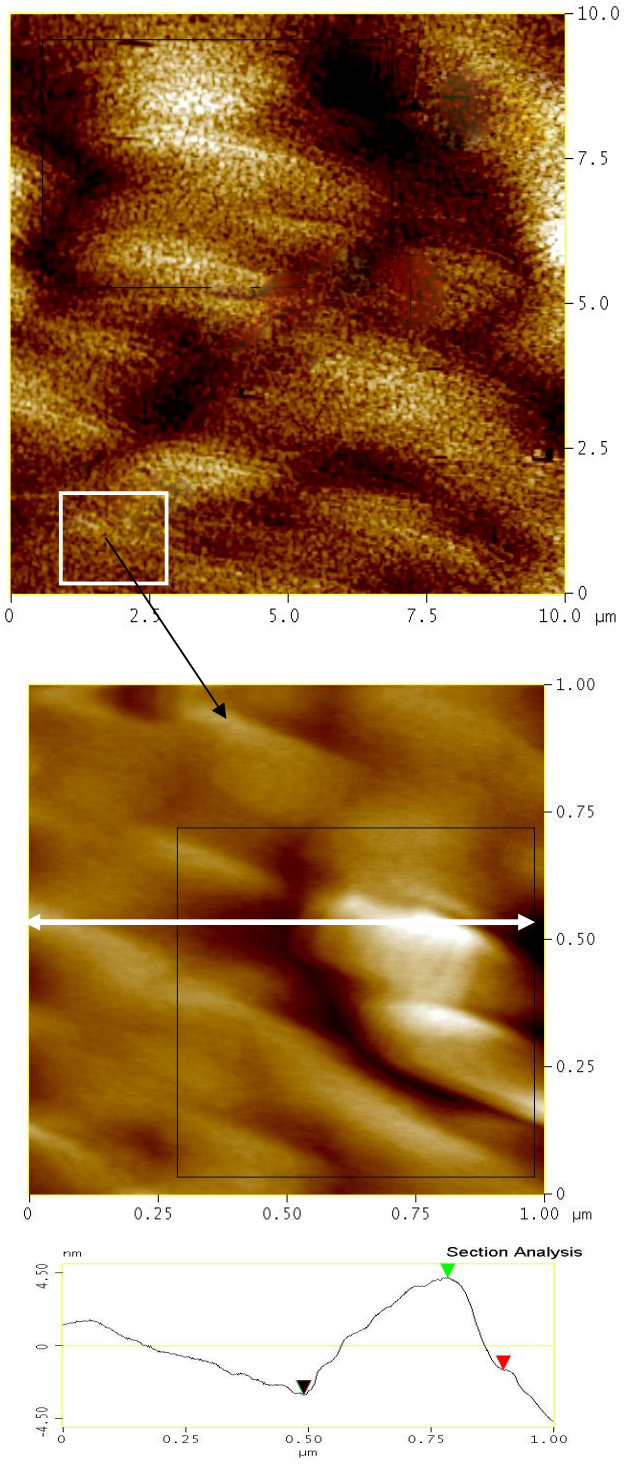


Fig. 5-9 AFM image of InAs MHEMT on Si substrate

Chapter 6

Self-assembled $In_{0.22}Ga_{0.78}As$ quantum dots grown on metamorphic GaAs/Ge/$Ge_{1-x}Si_x$ /Si substrates

6.1 Introduction

III-V compound semiconductor devices have been widely used for high-speed electronics and opto-electonics applications. Recent progress of the epitaxial growth technique has allowed the realization of III-V basedsemiconductor nanostructures such as quantum wires and quantum dots (QDs). Using Stranski-Krastanov (S-K) growth mode with InGaAs quantum dots (QDs) (0.9-1.7 μm wavelength response) are expected electronic and optical properties for the optical communications and near-infrared imaging application [1-3] such as near-infrared spectrography, laser beam profiling and semiconductor inspection. However, most of the quantum dots structures were growth on GaAs substrate, which is easy to grow and less dislocations. Si substrate has superior mechanical properties, higher thermal conductivity and lower cost than GaAs. As s result, quantum dots grown on Si substrate provide great potential in fabrication cost-down or integration of III-V based and Si based devices. However, there is a large lattice constant difference between Si and GaAs. This crystallographic problem indicates that there is a need for a well-designed buffer layer growth technology to accommodate the large lattice mismatch. One of the approaches is via graded

GeSi buffer layer [4]. This method has already been extensive studied; however, a very thick buffer layer is required to get a high quality GaAs layer on Si. In our former studies, a novel GeSi strained buffer structure for the growth of high-quality GaAs layers on Si (100) substrate is proposed [5]. The total buffer thickness is only 2.6μm, which is very thin compared with that grown by MBE system using graded GeSi buffer layer which is 10μm in thickness [4]. In this paper, we demonstrate the feasibility of using GeSi metamorphic buffer technology for the growth of III-V based structures on Si substrate. The effect of the growth temperature on the InGaAs quantum dot size distribution was investigated. It was found that a thin GaAs layer inserted between the Ge buffer and the GaAs layer can improve the QDs size uniformity and distribution. AFM measurement on these QDs showed that if the QDs were grown at 450℃ with 30 sec gas interruption time, the dot density about $1\times10^{11}cm^{-2}$ can be achieved successfully.

6.2 Experimental procedures

The growth of the Ge/GeSi buffer layers on Si was carried out using an urta-high vacuum chemical vapor deposition (UHV/CVD) system using Si_2H_6 and GeH_4 as the depositing sources with a base pressure of less than 2×10^{-8} torr by the Furnace. First, a 4-inch Si wafer with 6^0 off (100) toward <110> direction was cleaned by 10% HF dipping followed by high-temperature baking at 800℃ in the growth chamber for 5 min. Then, a 0.8 μm $Si_{0.1}Ge_{0.9}$,

a 0.8 μm $Si_{0.05}Ge_{0.95}$, and a 1.0 μm Ge layer were grown at 400℃ in sequence. Between successive layers, growth was interrupted for an in situ 15 min 750℃ annealing. After Ge layer were grown on the Si substrate, the sample was changed to another MOVPE system to grow GaAs and $In_{0.22}Ga_{0.78}As$ QDs. The $In_{0.22}Ga_{0.78}As$ QDs /GaAs layer were grown on the Ge/SiGe/Si heterostructure by MOVPE method at 40 Torr reactor pressure at different growth temperatures and 30sec interruption time for the AsH_3 gas. InGaAs QDs layers were grown at 450℃, 480℃ and 520℃. The triethyl gallium (TEGa) and trimethyl indium (TMIn) were used as the III source, and the arsine (AsH_3) was used as the V source. V/III ratio was kept at 60 for the GaAs layer and 10 for the $In_{0.22}Ga_{0.78}As$ QDs layer. TEM was used to observe the thickness of the epitaxial layers and the dislocation distribution. The Transmission electron microscopy (TEM) samples were prepared using the standard 'sandwich' technique followed by ion milling. Structural analyses of the epitaxial layers were performed on the cross-section by high-resolution transmission electron microscope (HRTEM). This study was carried out on a Phillips-200 electron microscope operating at 200 kV with an interpretable resolution of 0.16 nm. Fig.6-1 shows the schematic of the structure of the $In_{0.22}Ga_{0.78}As$ QDs/GaAs/Ge/Si. The surface morphology and the size of the quantum dots were analyzed by atomic force microscopy (AFM) in the contact mode.

6.3 Results and discussions

Fig. 6-2 shows the cross-section TEM image of the Ge buffer layers grown on the Si substrate. The total thickness of the epitaxial structure is only approximately 2.6 μm. The method mainly involves: (1) growth of two Si_xGe_{1-x} layers consisting of a 0.8 μm $Si_{0.1}Ge_{0.9}$ layer, a 0.8 μm $Si_{0.05}Ge_{0.95}$ layer, and (2) in situ 15min 750℃ annealing performed on each individual layer. There were a large number of dislocations located near the $Si_{0.1}Ge_{0.9}$/Si interface and at the lower part of the $Si_{0.1}Ge_{0.9}$ layer due to the large Ge composition difference in the Ge two layers. The upward propagated dislocations were bent sideward and terminated very effectively by the $Si_{0.05}Ge_{0.95}/Si_{0.1}Ge_{0.9}$ and $Ge/Si_{0.05}Ge_{0.95}$ interfaces due to compressive stress induced in the interfaces. Almost no threading dislocation can propagate into the top Ge layer. The details of the growth of the Ge/SiGe buffer layers can be found in the reference [5].

Fig. 6-3(a) shows the surface roughness of the Ge layer grown on Si wafer with 6^0 off (100) toward <110> direction. The root mean square (RMS) of the Ge layer was 1.3 Å and the roughness average (Ra) was 1.04 Å. The smooth surface is useful for the growth of the III-V material on the top of the Ge layer. The top Ge layer grown exhibits a low threading dislocation density and very smooth surface. It is shown that this proposed growth technique is very practical for the growth of high-quality Ge layers on Si substrates. Fig. 6-3(b) shows the rocking curve of the stacked Ge and SiGe epilayers. The value of full width half maximum (FWHM) for the top Ge layer was 150 arcsec.

GaAs layers were grown on Si substrate with Ge/$Si_{0.05}Ge_{0.95}$/$Si_{0.1}Ge_{0.9}$ layer as buffer by LP-MOVPE system have low mismatch (< 0.12%) and low thermal expansion difference (<2%) GaAs and Ge. Although the low lattice mismatch of the GaAs/Ge system suggests that it should be nearly dislocation free still exit considerable problems related to the epitaxy between polar (GaAs) and non-polar (Ge) semiconductors resulting in the formation of antiphase domains. The most common method for avoiding the antiphase domains (APDs) at the GaAs/Ge interface is by the use of tilted substrates with sufficient thermal annealing. The suppression of APDs can be achieved by using Ge wafer with 6^0 off (100) toward <110> direction. For the substrates with a larger miscut angle (6^0), in which the terraces between the steps are very narrow, the steps are so close to each other that no nucleus can be formed on the terraces. As the growth proceeds, the initial nuclei coalesce so that a single domain of GaAs is achieved [7]. This diminishes the chance for two-dimensional nucleation on the terraces. Therefore, only GaAs nuclei at the steps will be formed. Consequently, all the layers have the same sublattice orientation. In this study, the sample was grown on Ge/SiGe/Si substrate with 6^0 off (100) toward <110> direction. No APB was observed on the surface. The AFM data of the surface roughness was shown in Fig.6- 4(a). The root mean square (RMS) of the GaAs layer grown was 7.35 Å and the roughness average (Ra) was 5.81 Å. Double crystal X-ray measurement of the sample shows five peaks in the diffraction spectra, with GaAs peak (30.2 arcsec), pure Ge peak, $Si_{0.1}Ge_{0.9}$ peak, $Si_{0.05}Ge_{0.95}$ peak and Si substrate peak as shown

in Fig. 6-4(b). The narrower FWHM of the GaAs peak indicates high quality GaAs layer were grown on Si.

For the substrate with a small miscut angle, nuclei form at the steps and terraces with the latter having crystal orientation 90^0 rotated. Fig. 6-5(a) shows the two possible growth orientations of the GaAs layer on the 0^0 off sample. The two domains differ from each other in a reversal Ga and As atoms in the sublattices resulting in a rotation of 90^0 with respect to the substrate [8]. AFM measurement shows many square lines on the surface. The vertical distance of the APB was 13nm and Ra value was 8nm Fig. 6-5(a) for the GaAs grown on 0 off Si substrate. APBs provide deep levels in the forbidden gap and acte as non-radiative recombination surface. In our study, the twins and the lattice defects finally disappeared when the GaAs/Ge/SiGe epilayers was grown on Si substrate with 6^0 off (100) toward <110> direction. The reason for this resides in the structure and the density of the steps, not the (110) terrace. The occurrence of the self-annihilation processes of APBs is very importation for the growth of the device quality GaAs/Ge/SiGe/Si epitaxial layers.

Fig.6-6. shows the top layer of the $In_{0.22}Ga_{0.78}As$ QDs/GaAs/Ge/SiGe/Si structure. These QDs were grown at 480℃ after a 30sec growth interruption time without AsH_3. During the growth interruption, arsenic surface is unstable to result in Indium segregation increases and instead appears as an unbounded indium-floating layer. The thickness of the GaAs layer was

40nm. The $In_{0.22}Ga_{0.78}As$ QDs (~5 monolayer) were grown on the top of the GaAs layer, which corresponds to the critical layer thickness for the InGaAs QDs formation on the GaAs layers [9]. For the GaAs/InGaAs material system, typically, the growth appears in Sranski-Krastanow mode, the driving force for the QDs formation is the 2% lattice mismatch of InGaAs /GaAs. The stress on a crystal surface can provide a natural driving force for nanostructure formation and three-dimensional island formation in the lattice mismatched growth on the planar low index substrates. For GaAs/InGaAs material system with small interface energy but large lattice mismatch, initial growth is layer by layer, when thicker layer was grown, it has large strain energy and can lower its total energy by forming isolated thick islands [10]. InGaAs QDs were grown on different off-orientation Si substrate for compasion. Fig. 6-7(a). shows the InGaAs QDs grown on the 6^0 off angle substrate, there was no APB on the surface and the distribution of the InGaAs QDs is uniform. Fig. 6-7(b). shows InGaAs QDs were grown on the substrate with 0^0 off (100) toward <110> direction. The InGaAs QDs accumulated along the APBs, which support enough energy for the formation of the InGaAs QDs resulting in non-uniform quantum dots distribution on the surface.

While InGaAs QDs grown at 0^0 Si substrate gives a weak asymmetric PL emission profile, the InGaAs QDs grown at 6^0 off substrate shows narrow and high intensity peaks. Fig. 6-8(a). shows the PL emission of the InGaAs QDs grown on the substrate with 6^0 off (100) toward <110> direction, the FWHM of the PL emission is 77nm in the case. Fig. 8(b). shows

the PL emission of the InGaAs QDs grown on substrate 0^0 off (100), the FWHM of the PL emission is 103nm. The non-uniform InGaAs QDs results in the larger FWHM of the PL emission.

Atomic force microscopy (AFM) image of the $In_{0.22}Ga_{0.78}As$ QDs grown on the composite structure with silicon substrate is shown in Fig 6-9(a). The growth condition of these quantum dots are the growth temperature 450℃ and the TMIn, TEGa and AsH_3 flows were 3 μ mol/sec, 3 μ mol/sec and 90 μ mol/sec respectively at the mean growth rate of the $In_{0.22}Ga_{0.78}As$ QDs is 0.2ML/s. The $In_{0.22}Ga_{0.78}As$ QDs in the sample was 5ML $In_{0.22}Ga_{0.78}As$ QDs/GaAs/Ge/Si with the density of $In_{0.22}Ga_{0.78}As$ QDs was about $1\times10^{11}cm^{-2}$. The small and vague features of QDs observed at low temperature are explained by poor surface diffusion kinetics. At low growth temperature, atoms can only diffuse short distance before they are incorporated. Therefore, island formation is kinetically delayed of frozen out [11]-[13]. Reduced mass transport may limit the amount of indium participating in the gallium-indium exchange and reduce the effect of arsenic on the surface. At high growth temperatures, the dot formation is kinetically enhanced because atoms can diffuse longer distance before low-density and large dots formation. Atomic force microscopy (AFM) image in Fig. 6-9(c) reflecting the feature with QDs array density decreases and the size of each dot increases. shows $In_{0.22}Ga_{0.78}As$ QDs were formed on the sample with 5ML $In_{0.22}Ga_{0.78}As$ on Si substrate with the growth temperature of 520℃, the thickness of the $In_{0.22}Ga_{0.78}As$ QD was

5 ML and the density was about $4.5\times10^{9}cm^{-2}$. The Indium segregation is different with temperature. At the lower temperature, the arsenic surface became more stable and adatom diffusion length was reduced to lower mass transport properties. The higher temperature increases diffusion length of the surface species may improve the segregation of indium to increase the InGaAs QDs size and distribution.

. The Fig. 6-10(a) and Fig. 6-10(b) shows the size distribution of the $In_{0.22}Ga_{0.78}As$ QDs on the Si substrate at different temperatures. Fig. 6-10(a). the QDs were grown at 480℃, the QDs grown have an average lateral dot size around 31nm and 7nm in heights. Fig. 6-10(b). shows the size distribution of the $In_{0.22}Ga_{0.78}As$ QDs/GaAs/Ge/Si substrate grown at 480℃. The $In_{0.22}Ga_{0.78}As$ QDs grown at 480℃ have an average lateral dot size around 36nm. Fig. 6-10(c). shows the size distribution of the $In_{0.22}Ga_{0.78}As$ QDs/GaAs/Ge/Si substrate when grown at 520℃, the $In_{0.22}Ga_{0.78}As$ QDs grown at 520℃ have an average lateral dot size around 75nm.

6.4 Conclusions

The twins and APBs disappeared at Si substrate with 6^{0} off (100) towards <110> orientation. $In_{0.22}Ga_{0.78}As$ QDs were deposited successfully on Si substrate with Ge buffer layer. From the PL measurement, it shows strong PL intensity with narrow linewith when InGaAs QDs was formed on Si substrate with 6^{0} off (100) towards <110> orientation. The

density of $In_{0.22}Ga_{0.78}As$ dots was estimated to be 1×10^{11} cm^{-2} for the sample with 5 monolayers thick $In_{0.22}Ga_{0.78}As$ grown at 450℃, $5\times10^{10}cm^{-2}$ for the sample with 5ML thick $In_{0.22}Ga_{0.78}As$ grown at 480℃ and $4.5\times10^{9}cm^{-2}$ for the sample with 5ML thick $In_{0.22}Ga_{0.78}As$ grown at 520℃. The corresponding average distribution sizes of $In_{0.22}Ga_{0.78}As$ QDs were 31nm, 36nm and 75nm respectively. These results indicate that Ge/SiGe/Si strained buffer is promising method for the fabrication of InGaAs QDs on Si substrate.

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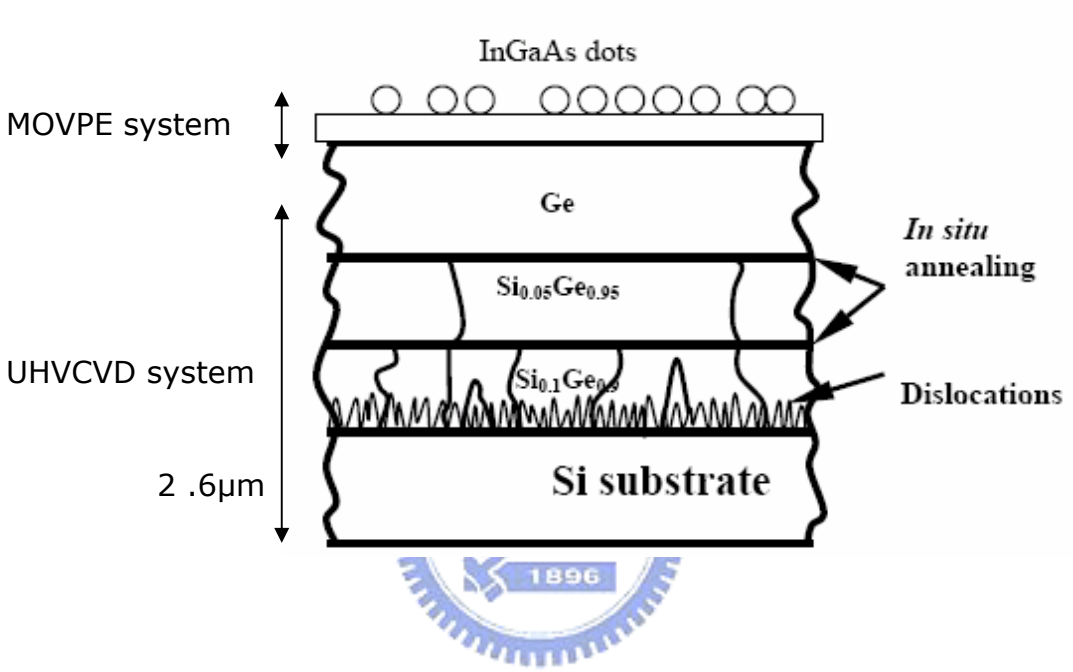


Fig. 6-1. Schematic diagram of InGaAs QDs on Si substrate.

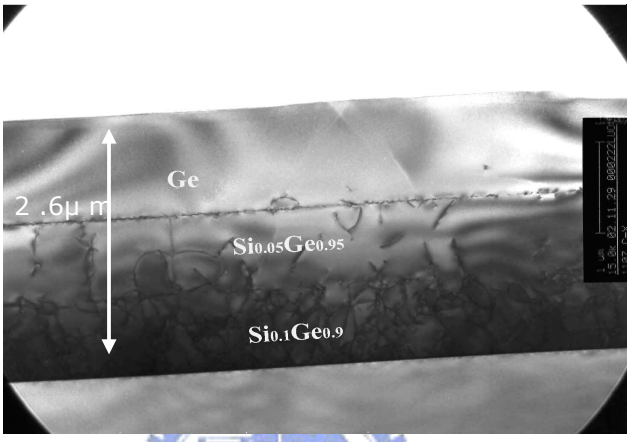
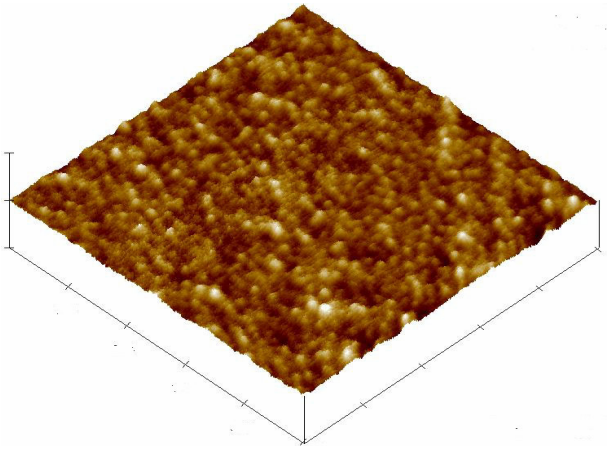
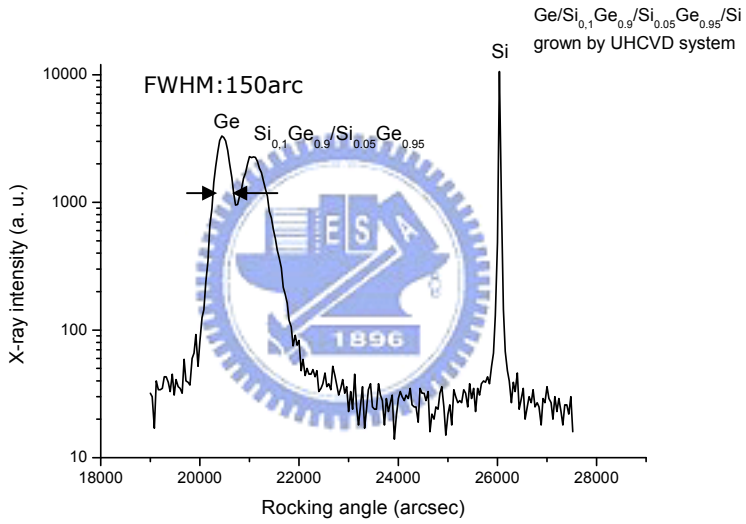


Fig. 6-2. Cross-sectional TEM image of the epitaxial structure.

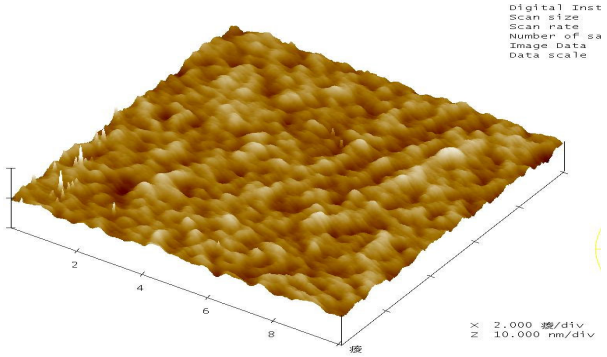


(a)

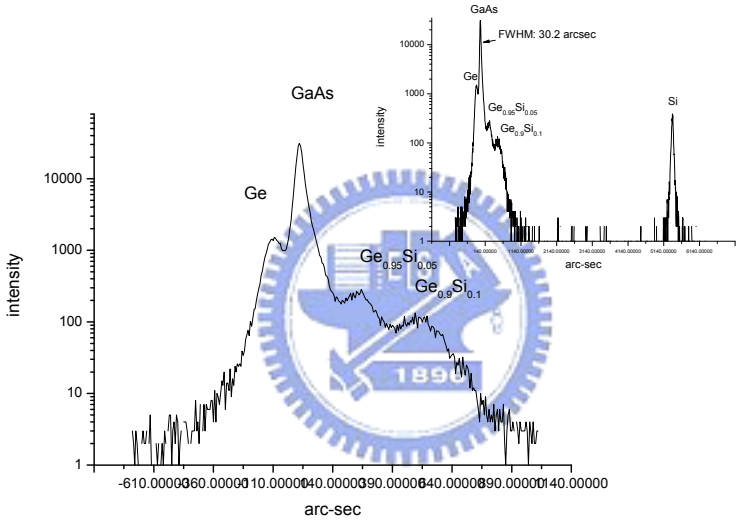


(b)

Fig. 6-3. (a)AFM image of the surface of the Ge layer. (b) The Quality of Ge layer of FWHM of X-ray rocking curves.

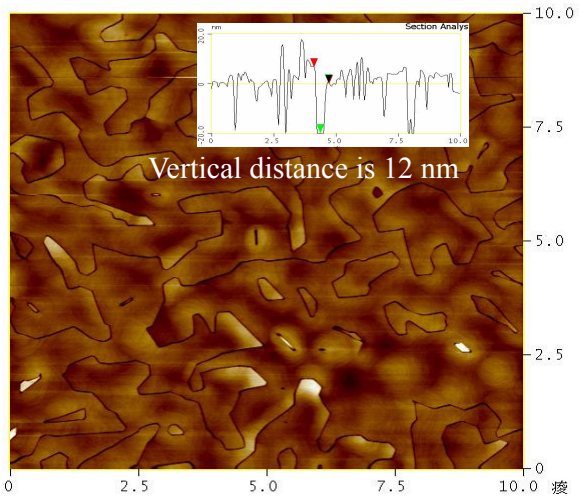


(a)

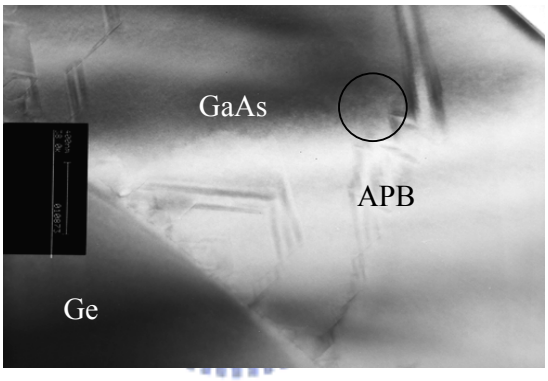


(b)

Fig. 6-4. AFM scans (10 μm×10 μm) of the typical GaAs grown on the composite structure with Ge/SiGe/Si sub with 6^{o} off-degree toward [110] (b) The Quality of GaAs layer of FWHM of X-ray rocking curves.



(a)



(b)

Fig. 6-5. (a) AFM scans (10 μ m×10 μ m) of the typical GaAs grown on the composite structure with Ge/SiGe/Si sub with 6^0 off-degree toward <110>. (b) The TEM micrograph of GaA layer grown on Si sub. with 6^0 off-degree toward <110> shows the APBs cross the GaAs layer.

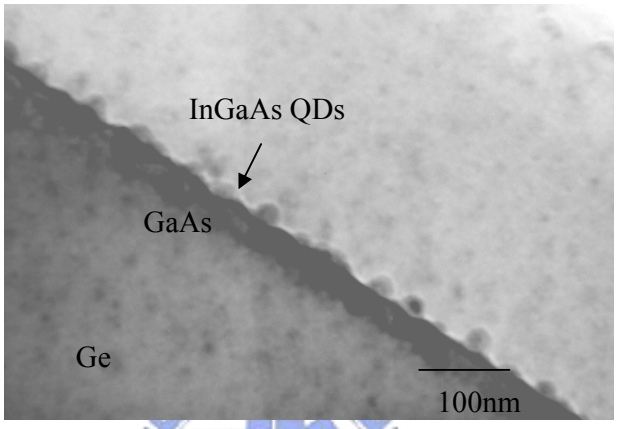
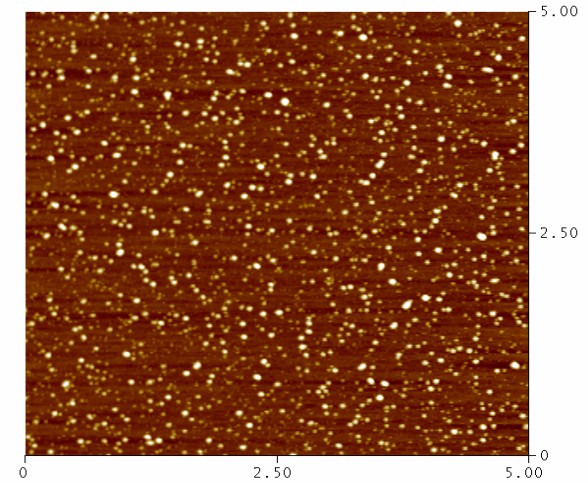
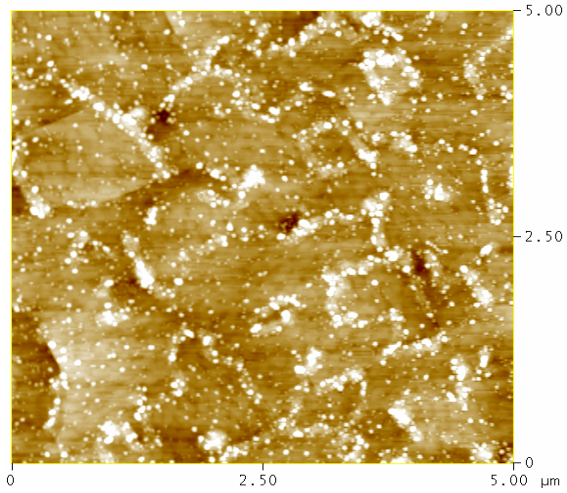


Fig. 6-6. Bright-field cross-section TEM image of the $In_{0.22}Ga_{0.78}As$ QDs formed on GaAs/Ge/SiGe/Si.

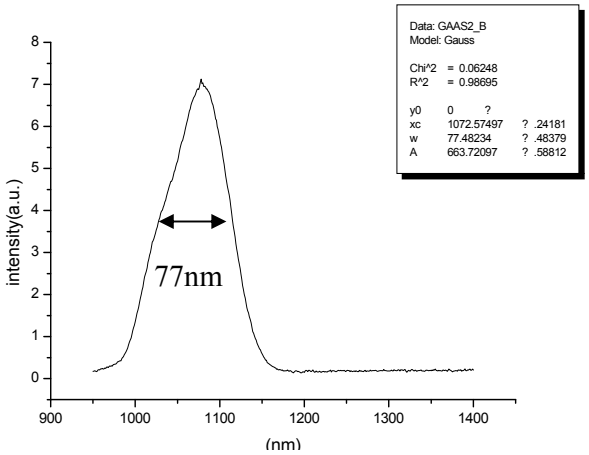


(a)

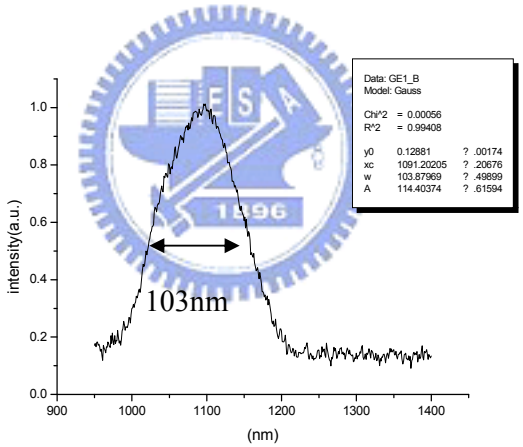


(b)

Fig. 6-7. Distribution of InGaAs QDs grown on misorientated Si substrate. (a) 6^0 off-degree toward <110> (b) 0^0 off-degree toward <110>

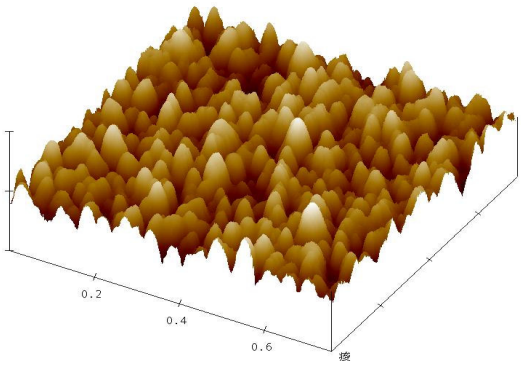


(a)

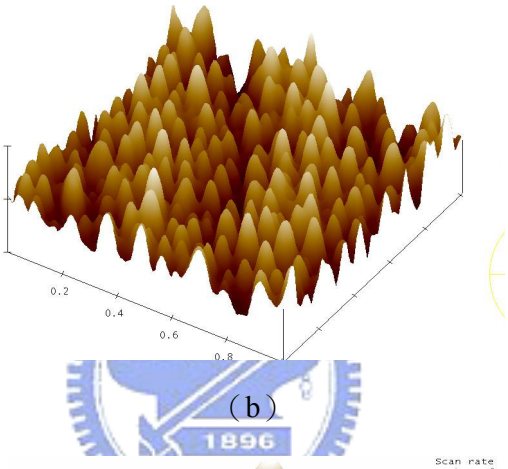


(b)

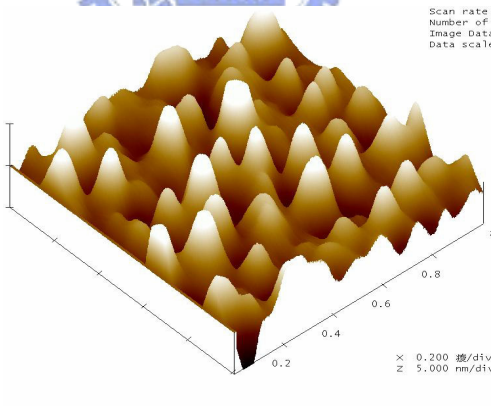
Fig. 6-8. PL measurement of the InGaAs QDs grown on misorientated Si substrate. (a) 6^0 off-degree toward <110> (b) 0^0 off-degree toward <110>



（a）

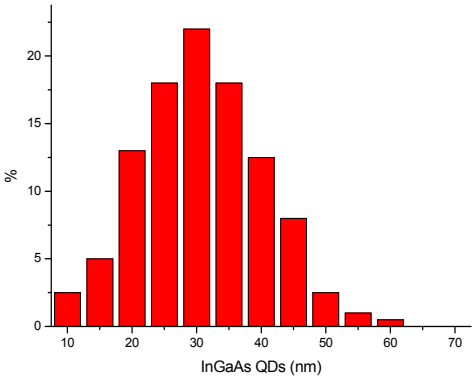


（b）

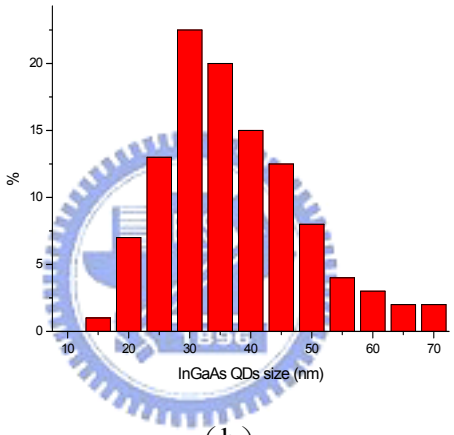


（c）

Fig. 6-9. AFM images of Self-assemble InGaAs QDs grown at different temperatures. (a) 450 ℃（b）480℃ (c) 520℃



（a）



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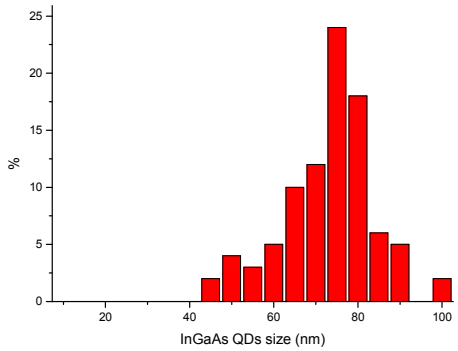

（c）

Fig. 6-10. Average size distribution of the $In_{0.22}Ga_{0.78}As$ QDs grown at different temperatures. (a) 450℃（b）480℃ (c) 520℃

Chapter 7

Conclusions

In this dissertation, Ge_xSi_{1-x} metamorphic buffer layers was used for the growth of III-V material on a Si substrate. The Ge_xSi_{1-x} metamorphic buffer layer with a Ge layer on top of the III-V structure was proposed, because Ge was only 0.07% lattice mismatched with GaAs, and the thermal expansion coefficient difference between Ge and GaAs is only 2%, i.e. the lattice constant and thermal expansion coefficients of Ge are almost identical to those of GaAs. Using a Ge/Ge_xSi_{1-x} metamorphic structure as the buffer layer with proper design can solve the thermal expansion mismatch and the lattice mismatch problems of the interface between GaAs and Si. After the GaAs epilayer growth, III-V quantum well based device structure was grown on the Si substrate for the high speed device applications. Our group have demonstrated high quality III-V epitaxial layer grown on Si substrate using Ge/Ge_xSi_{1-x} metamorphic buffer already in the past. In this study, III-V based metamorphic quantum well devices structure was grown on $Ge/Ge_xSi_{1-x}/Si$ template. The Ge_xSi_{1-x} buffer layer was grown using a UHV-CVD technology, and the III-V device structure was grown by MBE technique. The novel GaAs on Si template is a promising technique for the integration of the III-V based high speed device with the Si substrates for the application of opto-electronic integrated circuits and for the CMOS technology beyond 35nm.

In summary, the following technologies have been demonstrated in this thesis.

(1) A thin Ge_xSi_{1-x} metamorphic buffer layer for the growth of a high-quality Ge film on a Si substrate was achieved by using a Si^+ ion implantation on the Si substrate before the growth of the Ge_xSi_{1-x} metamorphic buffer layers. The enhanced level of relaxation can be attributed to the introduction of point-defects in the Si substrate with a heavy dose Si^+ pre-ion-implantation. Due to the use of the pre-ion-implantation technique, and the interface-blocking of the dislocations in the Ge_xSi_{1-x} metamorphic buffer structure, the total thickness of the Ge_xSi_{1-x} metamorphic buffer layer was greatly reduced to a thickness of 1.0μm, which is much thinner than in the previous literature. Because the formation of the dislocation pileups in the Ge_xSi_{1-x} metamorphic buffer layer was eliminated, the surface of the Ge films grown was very smooth, no cross-hatch pattern could be observed, and the dislocations in the top Ge layer were reduced to about $7.6\times10^6 cm^{-2}$. The approach described in this paper can be used to grow high-quality Ge film on a Si substrate and can also be easily applied to the fabrication of the Ge MOSFETs and optoelectronic devices on Si substrates.

(2) We have demonstrated a working AlGaAs/InGaAs HEMT device on Si substrate. The 0.4 μm AlGaAs/InGaAs HEMT fabricated on the Si substrate had a transconductance of 155 mS/mm, and a saturation channel current of 150 mA/mm with well behaved pinch off characteristics. Furthermore, the device had a breakdown voltage of 3.5Volt. After a device isolation process, the leakage current of the HEMT structure on Si substrate was 0.016μA/μm

at a bias voltage of 14.2V as measured by the isolation pattern. The results indicate that the buffer layer quality was good with no Ge diffusion into the GaAs layers and no APBs formation. The good HEMT performance is attributed to the very thin buffer layer (1.0μm) achieved using Si^+ ion implantation, and a two step buffer layer growth technique, which helps to alleviate the stress effect caused by the large expansion coefficient difference between these two materials. The technology demonstrated shows great potential for III-V/Si integration and can be applied to the future optoelectronics and microelectronics applications.

(3) The growth of the InAs MHEMT structure on the Si base substrate via GeSi metamorphic buffer layers has been demonstrated. A tilted Si substrate with 6^o angle off (100) toward to [110] was used to supply more nucleation sites. The atoms are incorporated without long distance of diffusion, and are the same lattice orientation to improve the crystalline quality. An electron mobility 27,300cm^2/v-s of the InAs MHEMT grown on the Si with 6^o angle off (100) toward to [110] could be achieved.

(4) $In_{0.22}Ga_{0.78}As$ QDs were deposited successfully on the Si substrates with Ge as the buffer layers. The PL measurements result shows strong PL intensity with narrow FWHM when InGaAs QDs were formed on the Si substrate with 6^o off (100) towards <110> orientation. The density of the $In_{0.22}Ga_{0.78}As$ dots was estimated to be 1×10^{11} cm^{-2} for the sample with 5 $In_{0.22}Ga_{0.78}As$ monolayers grown at 450℃, $5\times10^{10}cm^{-2}$ for the sample with 5 $In_{0.22}Ga_{0.78}As$ ML grown at 480℃ and $4.5\times10^{9}cm^{-2}$,and for a sample with 5 $In_{0.22}Ga_{0.78}As$

ML grown at 520℃. The corresponding average sizes of the $In_{0.22}Ga_{0.78}As$ QDs were 31nm, 36nm and 75nm respectively. These results indicate that using $Ge/Ge_xSi_{1-x}/Si$ strained buffers is a promising method to be used the fabrication of the InGaAs QDs on Si substrates.