Chapter 1

Introduction

1.1 General Background and Motivation

The demand for high-frequency devices is increasing in recent years with two major system applications: high-speed optical fiber communication systems and high-frequency wireless systems. With the rapid development of the wireless communication systems, the demands of low cost, low power consumption, high-level integration and high frequency operation devices become more and more strong. For high frequency applications, compound semiconductor devices such as GaAs pseudomorphic high electron mobility transistors (PHEMTs), metamorphic HEMTs (MHEMTs), conventional lattice-matched or pseudomorphic InAlAs/InGaAs/InP HEMTs (InP HEMTs), have shown superior performance as compared to Si devices for high-frequency applications. MHEMT have received much attention recently due to its capability of combining the advantages of the high-performance InP-based structure and the low-cost, high mechanical strength GaAs substrate. MHEMTs have been considered as a cost-effective alternative to the InP HEMTs. Many efforts have been made to improve the device performance. Devices with higher carrier concentration, higher electron mobility and shorter gate length by use of refined heterojunction structure and novel gate shrinkage technique have been demonstrated and have shown outstanding performances. In this study, high RF performance MHEMTs with submicron gates were developed by using advanced device structures and novel gate shrinking technologies, and the characteristics of these devices were evaluated.

1.2 Overview of High Electron Mobility Transistors (HEMTs)

High electron mobility transistor (HEMT) is one of the most mature III-V semiconductor transistors which rely on the use of heterojunction for its operation. Fig. 1.1 shows a conventional HEMT structure. As compared with the silicon-based transistors, such as metal-oxide-semiconductor field effect transistors (MOSFETs) and bipolar-junction transistor

(BJTs), GaAs transistors exhibit inherent advantages over Si-based transistors for high frequency applications [1-1]. GaAs HEMT is was invented by Takashi Mimura [1-2] and have been successfully manufactured and commercialized for many applications. The epitaxial layers of the HEMT structure are designed to form two-dimension electron gas (2-DEG) in the channel layer with an un-doped spacer in the high band gap material to separate the ionized donors from the channel to increase the electron mobility. Consequently, GaAs HEMTs have superior carrier transport properties due to the band-gap engineering design.

Conventional HEMT structure is consisted of AlGaAs barrier layer and GaAs channel structure. The band gap discontinuity between AlGaAs/GaAs increases as the Al content increases and the large discontinuity in the band gap results in better confinement of the electrons in the channel. However, the deep-complex center (DX center) phenomenon exists while Al content is over 20% which traps the electrons and influences the device performance [1-1]. In order to avoid the DX center phenomenon and increase the electron mobility, AlGaAs/InGaAs/GaAs pseudomorphic HEMT (PHEMT) structure was developed. InGaAs is a preferred channel material over GaAs for HEMTs because of its superior transport properties as compared to GaAs. The In content in the channel was increased to enhance the electron transport properties and improve the confinement of the carriers in the channel. However, InGaAs channel in PHEMTs is limited to an In content of 25% [1-3] to avoid lattice relaxation of the channel.

Higher In mole fractions are feasible in the HEMT structure on InP substrates, e.g., lattice matched $In_{0.52}Al_{0.53}As/In_{0.53}Ga_{0.47}As$ heterostructures. InP-based HEMTs have shown very high frequency characteristics, low noise figure, high gain, and high efficiency as compared to the GaAs-based PHEMTs [1-4]. However, InP substrates are more expensive, smaller in size, and more brittle than the GaAs substrates. GaAs substrates of 6” diameter are commercially available, while the largest available InP substrates are only 4” in diameter [1-5]. Therefore, a new device structure, metamorphic HEMT (MHEMT) structure, is developed on GaAs substrates. In the MHEMT structure, the device active layers are grown on a strain relaxed, compositionally graded, metamorphic buffer layer. The buffer layer provides the ability to accommodate the lattice mismatch between InGaAs channel and GaAs substrate. Therefore, the high In content in the InGaAs channel can be achieved in spite of the large lattice mismatch between the active epilayers and the substrate. The relation between the lattice constant and the bandgap of $In_xAl_{1-x}As$ and $In_yGa_{1-y}As$ is shown in Fig. 1.2. Using the metamorphic buffer layer, PHEMT structure lattice matched to InP can be grown on the GaAs substrates for a substantial cost reduction and manufacturability improvement. Table 1-1

shows the comparisons of the properties between MHEMT and InP HEMT. As can be seen in Table 1-1 [1-6], MHEMT has the advantage over InP HEMT in cost and fabrication yield. Therefore, this study will focus on the development of the MHEMT technology. The high frequency performance of the HEMTs can be improved by optimizing the device structure and reducing the gate length. A shorter gate is very essential for achieving ultra-high frequency operation. Therefore, in next section we will discuss the technologies of gate length shrinkage.

1.3 Gate Shrinking Technologies

Tetsuya et al. [1-7] proposed a nanocomposite resist (a mixture ZEP-520 and fullerences C_{60}) system that incorporated sub-nm carbon particles into a resist film to enable an ultra thin resist process for nanometer pattern fabrication. Fullerence-incorporated nanocomposite resist, which can enhance dry-etching resistance and pattern contrast, was able to achieve high resolution. Gate footprint by electron beam direct writing can achieve a fine feature size of 30nm as shown in Fig. 1.3. The gate pattern was defined and replicated on SiO_2 /SiN_x layers. After forming the gate opening, both SiO_2 and SiN_x were etched by C_2F_6 RIE and then the side-etching of SiN_x was done by using SF_6 RIE in order to reduce the aspect ration of the gate foot. Fig. 1.4 was the SEM photography of the cross section of the 30-nm T-shaped gate.

Fabrication of ultra-short 25-nm-gate has been demonstrated by Yoshimi Yamashita et al. [1-8] using the two-step SiO_2 dielectric layer deposition and two-step recess to confirm the ultra short gate. Firstly, a 20 nm SiO_2 was deposited over the cap layer. The gate pattern was written and replicated on the SiO_2 film by RIE using CF_4 gas. After RIE, the first gate recess in cap layer was formed by wet-chemical etching (C.A. and H_2O_2 mixture). The second 20 nm SiO_2 film was re-deposited over the wafer and etched again by RIE with CF_4 gas. Finally, the foot of the T-shaped gate was formed, then with second gate recess. The second gate recess was formed by using the same solution as that for the first one. Fig. 1.5(a) and Fig.1.5(b) showed the final cross-section structure after gate metal deposited.

Szu-Hung Chen et al. [1-9] developed a phase shift mask (PSM) technique to define the 0.16μm gate length by I-line lithography. The 2000Å SiN_x was first deposited by chemical vapor deposition (CVD). Then the 8% half-tone PSM was used for the definition of the SiN_x opening. After the PSM exposure, the SiN_x was etched by RIE, and a 0.2-μm-wide opening was formed. In order to further reduce the dimension of opening, an addition SiN_x was deposited by CVD and etched back by RIE without any mask. Using the silicon nitride

re-deposition and etch-back technologies could reduce the dimension of the openings. Finally the T-shaped gate with a length of 0.16μm was achieved. The overall process is depicted in Fig. 1.6. In this study, the high frequency performance of MHEMT can be improved by optimizing the device structure and reducing the gate length using several novel gate-shrinking techniques as described in the next section.

1.4 Outline of this dissertation

Several newly developed gate shrinkage techniques for GaAs MHEMTs are introduced in order to overcome the restriction of resolution limit of the equipment. This dissertation covers the study of the gate shrinkage techniques for GaAs MHEMTs and is divided into 9 chapters.

In chapter 2, the details of the fabrication process of the GaAs MHEMT are introduced. The epi-structure, layout design, and front-side metallization are described. In addition, the DC and RF characterization of the device are studied and stated in chapter 3.

In chapter 4, a description of a novel gate shrinking process for $In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As$ MHEMTs is given. For cost-effective production of submicron MHEMTs, a 0.15-μm Γ-shaped gate MHEMT technology using DUV lithography and a tilt dry-etching technique was developed and demonstrated for the first time. The final gate-length of the Γ-shaped gate was mainly controlled by the top photoresist opening, the total resist thickness and the tilt angle for the anisotropic dry etching. The tilt dry-etching gate process is a simple and inexpensive process for the fabrication of submicron MHEMTs and monolithic microwave integrated circuits (MMICs) for high-frequency applications.

In chapter 5, a 0.1 μm T-shaped gate was achieved by thermally reflowing the bi-layer E-beam resist using hotplate and the 0.1 μm T-shaped gate was achieved by the standard lift off process and was applied to the $In_{0.52}Al_{0.48}As/In_{0.52}Ga_{0.48}As$ MHEMT manufacture. Comparing with 2 step lithography of conventional E-Beam T-shaped gates, the reflowed gate process is a much simpler, relatively inexpensive and flexible process. Additionally, it is also free of plasma damage and is compatible with the MHEMT process for high frequency application.

In chapter 6, the $In_{0.52}Al_{0.48}As/In_{0.52}Ga_{0.48}As$ MHEMTs using 90nm sidewall T-gate process is successfully applied to the fabrication for high frequency application. In addition, the equivalent circuit parameters (ECPs) of the small-signal model for the MHEMT has also been extracted and discussed.

In chapter 7, a 70-nm $In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As$ power MHEMT with double δ-doping was fabricated and evaluated. The device shows a high transconductance and high saturation current. High cutoff frequency and high maximum oscillation frequency of the device were achieved due to the nanometer gate length and the high Indium content in the channel. The excellent DC and RF performance of the 70-nm MHEMT shows a great potential for Ka-band power applications.

In chapter 8, the use of Ti/Pt/Cu as the Schottky contact to InAlAs is studied. The electrical characteristics and thermal stability of the Ti/Pt/Cu Schottky contact are investigated. Platinum is used as the diffusion barrier because it has a high melting point, is compatible with the lift-off process, and is a good diffusion barrier for preventing Au from diffusing into the conventional Ti/Pt/Au Schottky and ohmic structure. The study of the electrical characteristics and the thermal stability of the Ti/Pt/Cu Schottky contact on i-InAlAs is indispensable for the realization of the gold free fully copper metallized InAlAs/InGaAs based HEMTs and MMICs.

Finally, chapter 9 is the conclusion of the dissertation. The performances of the MHEMTs have been improved by optimizing the device structure and reducing the gate length using several novel gate-shrinking techniques in this dissertation. The MHEMTs developed showed excellent DC and RF performances and demonstrated great potential for high-frequency applications.

TABLE

Property	InP HEMT	MHEMT
Substrate Availability, Cost	- 4-inch now, higher cost	+ 6-inch available now
MBE Growth Time	+ ～1/2 hour	- 1-2 hours
Process Difficulty Yield	- Higher breakage, more difficult /slower backside process	+ Lower breakage, standard GaAs backside process
Performance, Impedance char.	No difference	No difference
Achievable Channel In Content	53-80 %	30-80 %
Thermal Resistance	+ InP has 50% higher thermal conductivity than GaAs	Comparable to GaAs PHEMT, effect of buffer unclear
Reliability	Proven for low noise, unproven for power	Excellent initial data for low noise, power unknown

Table 1.1 Comparison of lattice-matched InP HEMT and metamorphic GaAs HEMT.

FIGURES:

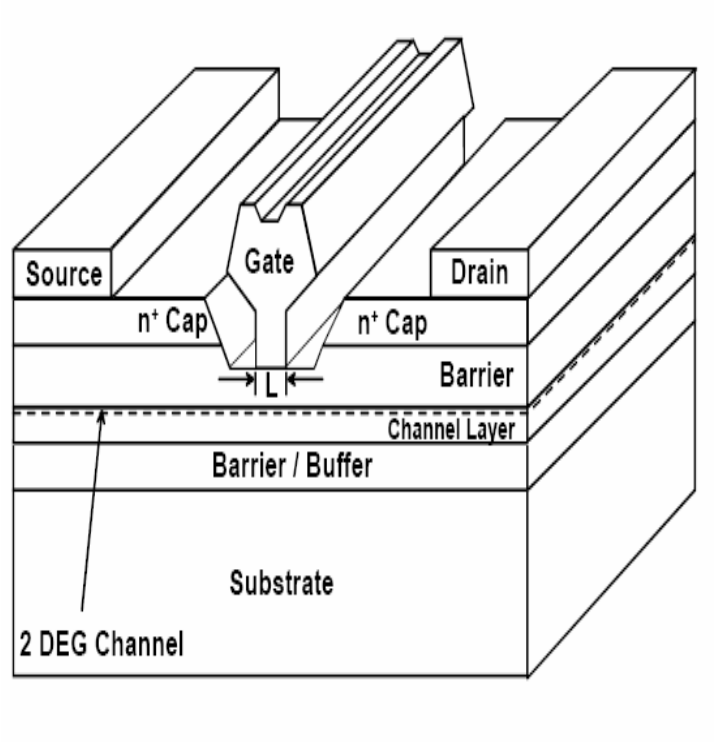


Fig. 1.1 Conventional HEMT structure.

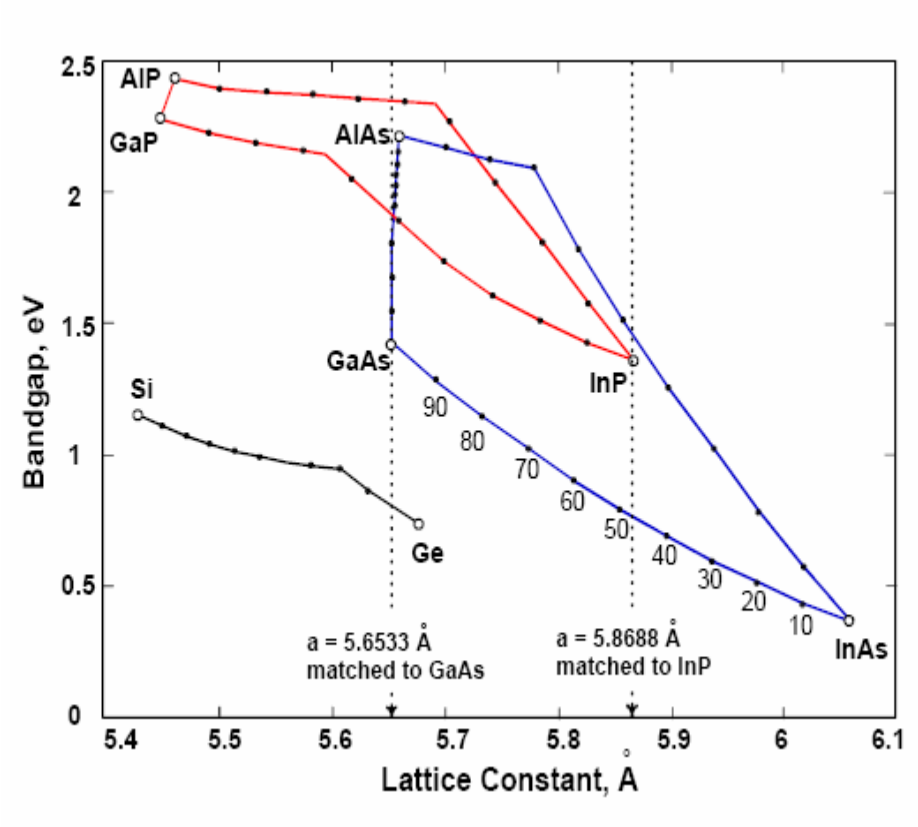


Fig. 1.2 Energy band gap v. s. lattice constant for the $In_xAl_{1-x}As/In_yGa_{1-y}As$ system.

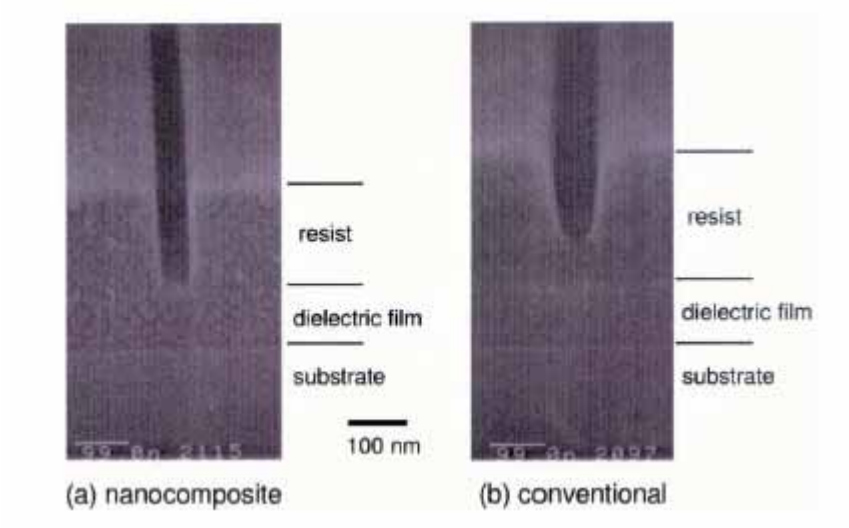


Fig. 1.3 SEM photographs of the EB resist pattern for nanocomposite and conventional ZEP.

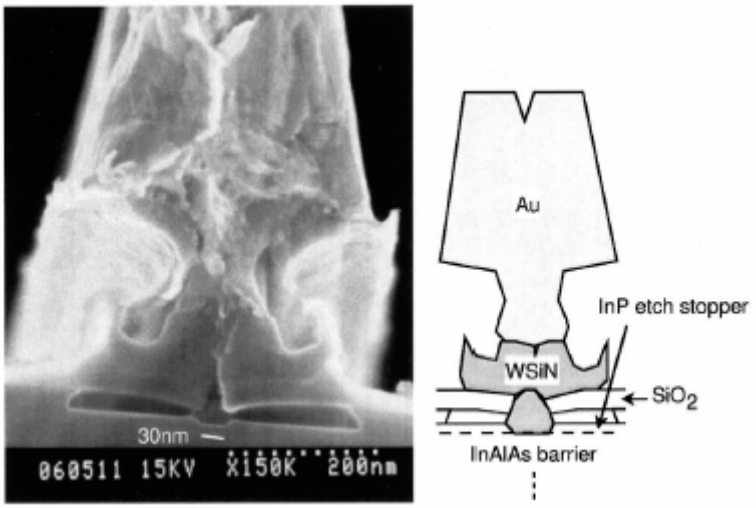


Fig. 1.4 Cleaved cross section of a 30-nm T-gate. Each material is specified in the figure.

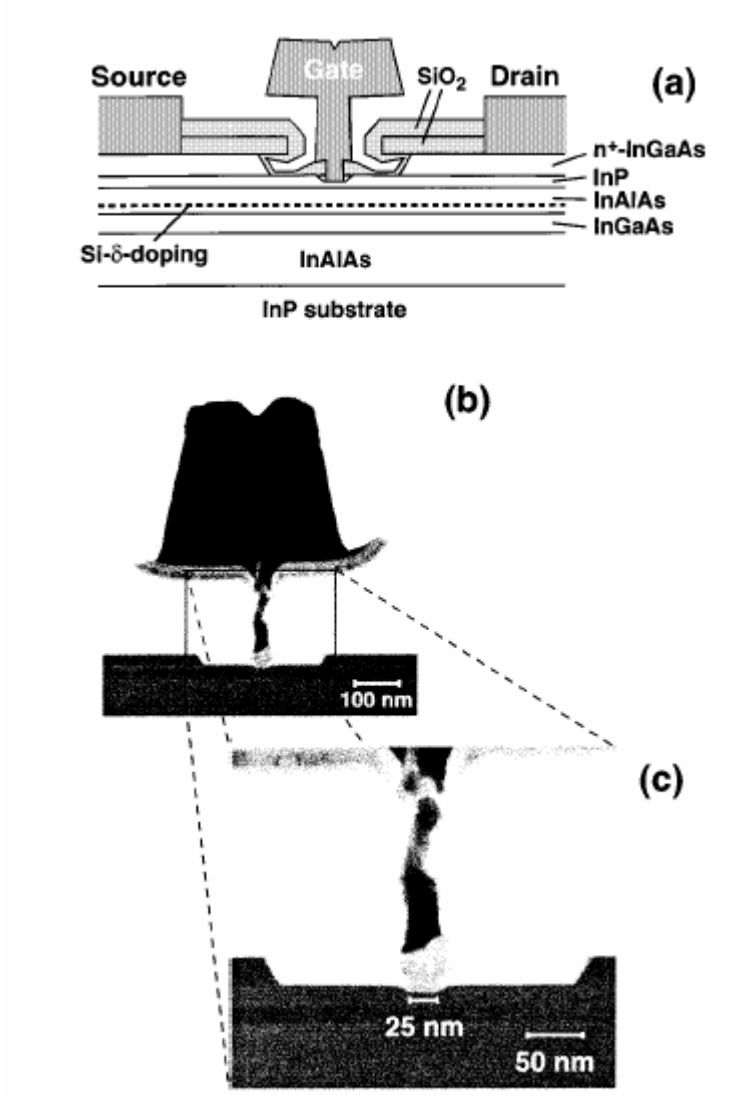


Fig. 1.5 (a) Schematic cross-section view of the HEMT, (b) Cross-sectional TEM image of the 25-nm-long T-shaped gate, and (c) Magnification of the TEM image around the bottom of the 25-nm-long T-shaped gate.

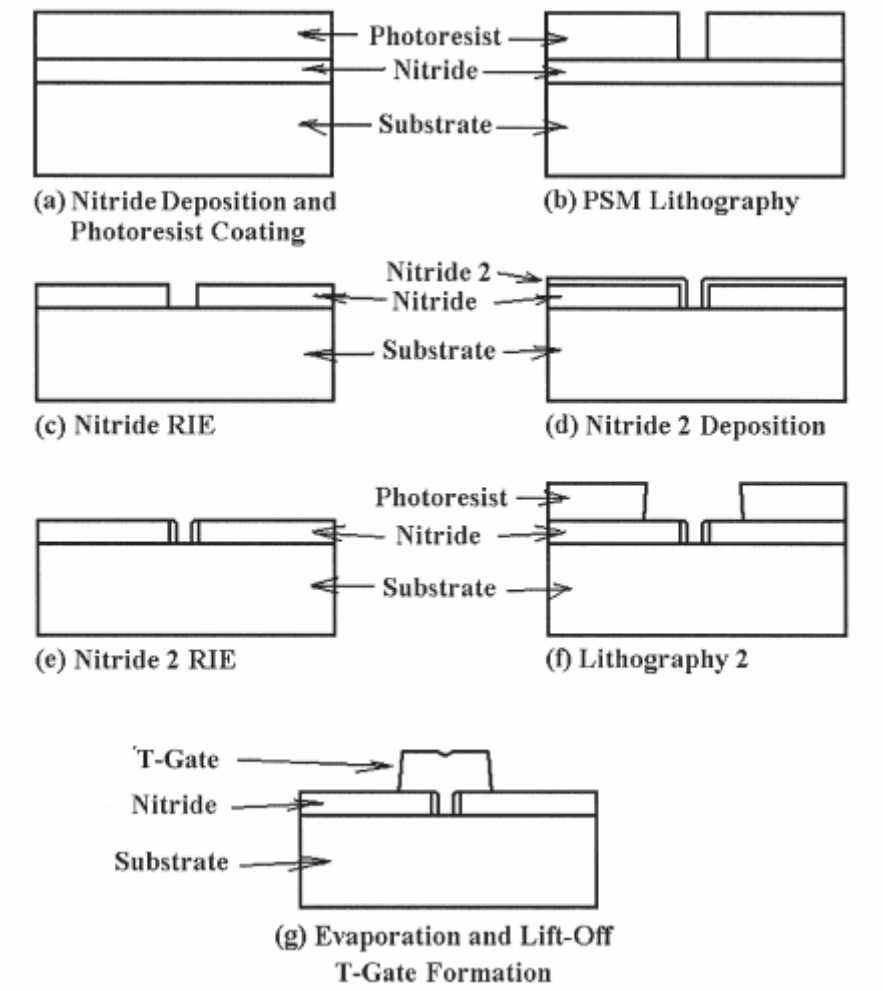


Fig. 1.6 T-gate process flow of the PSM technique

Chapter 2

Fabrication of GaAs Metamorphic High Electron Mobility Transistors

2.1 Material Properties and Growth of MHEMT

The InGaAs/InAlAs materials system offers numerous advantages over traditional PHEMTs which lead to improved device performance. The most important advantage is the higher conduction band discontinuity present at the InGaAs/InAlAs heterojunction interface. The value has been determined to be 0.5 eV compared to 0.25 eV for GaAs/AlGaAs heterojuction and approximately 0.4 eV for the InGaAs/AlGaAs pseudomorphic structure.[2-1] The higher conduction band discontinuity allows for a higher two-dimensional electron gas concentration. Besides, InAlAs does not suffer from a similar DX center problem of AlGaAs and can be easily doped in the 10^{19} cm^{-2} range with Si. Once a sufficient concentration of electrons is present in the InGaAs channel of the MHEMT, the velocity field characteristics of the channel material determine the ultimate frequency and noise performance limits. In addition, in short-gate devices where the average velocity of electrons under the gate is closer to the peak velocity, electron transit time in InGaAs will be significant shorter.

In this study, the epitaxial layers of the metamorphic HEMT with $In_xAl_{1-x}As$ grading buffer layer were grown by molecular beam epitaxy (MBE). The cross-section of the single δ-doped structure for low-noise MHEMT structure is shown in Fig. 2.1(a). The Indium graded $In_xAl_{1-x}As$ metamorphic buffer layer was grown on a 3-inch semi-insulating GaAs wafer, followed by an undoped $In_{0.52}Al_{0.48}As$ buffer layer. 15 nm $In_{0.52}Ga_{0.48}As$ was chosen as the channel layer. The Si-planar doping ($2x10^{12}$ cm^{-2}) layers were separated from the channel layer by 4 nm thin undoped $In0_{.52}Al_{0.48}As$ spacer. The undoped $In_{0.52}Al_{0.48}As$ Schottky layer was 15 nm. Then, the 18 nm thick $In_{0.52}Ga_{0.48}As$ cap layer was heavily doped with Si of $2x10^{18}$ cm^{-3} for Ohmic contact formation. The double δ-doped structure for the power MHEMT in this study is shown in Fig. 2.1(b). The structure is as following: a 15-nm pseudomorphic $In_{0.6}Ga_{0.4}As$ channel layer was grown on top of the InAlAs buffer layer. The top and bottom Si-δ-doping layers were separated from the channel layer by the upper and lower 4-nm-thick undoped $In_{0.52}Al_{0.48}As$ spacers, respectively. The $In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As$

hetero-interface provides higher electron mobility and better carrier confinement in the quantum well region. The Schottky layer was 15-nm-thick undoped $In_{0.52}Al_{0.48}As$. The same 15-nm-thick Si-doped $In_{0.52}Ga_{0.48}As$ cap (2×10^{18} cm^{-3}) layer was finally grown on the top for ohmic formation.

2.2 Device Fabrication

The fabrication process of the MHEMTs in this study includes:

1. Mesa/device isolation
2. Ohmic contact formation
3. Gate formation
4. Device passivation
5. Airbridge formation

The detail will be described in the following sections.

2.2.1 Mesa isolation

Device isolation is the very first step of the whole HEMT fabrication process which was used to define the active region of the device on the wafer. In these defined areas by lithography technique, the current flow is restricted to the desired path and each active device is isolated from each other (Fig. 2.2). There are three typical ways to achieve device isolation: wet etching, ion bombardment, and selective implantation. Wet etching is the simplest way of the three. In this study, mesa isolation was carried out by a phosphoric based solution etching. The active areas were masked by Shipley S1818 photo resist. According to the device structure, the mesa was etched to the buffer layer to provide good device isolation. In order to avoid the photo resist peeling during the etching, the wafer surface was pre-treated before resist coating by Hexamethyldisilazane (HMDS). Finally, the etching depth was measured by α-step or surface profiler after the photo-resist was stripped. The etched profile was checked by Scanning electron microscopy (SEM). To inspect the mesa isolation process, a test pattern with a 10μm gap is used to measure the leakage current.

2.2.2 Ohmic contact Formation

After wafer cleaning by using ACE and IPA, the negative photo resist and I-line aligner

were used to define the Ohmic pattern and to form the undercut profile for the metal lift-off (Fig. 2.3). Ohmic metals multilayer Au/Ge/Ni/Au, from the bottom to the top, was deposited in the appropriate composition by e-gun evaporation system. After lift-off process, source and drain Ohmic contacts were formed by 320℃ annealing for 20 sec in nitrogen atmosphere (Fig. 2.4). Germanium atoms diffused into the InGaAs and heavily doped InGaAs during the thermal annealing process. The specific contact resistance was checked by the transmission line method (TLM) in the process control pattern monitor (PCM). The typical measured contact resistance was < 1 x 10^{-6} Ω-cm^2 (Fig. 2.9). The TLM patterns and the illustration of utilizing TLM to measure the Ohmic contact resistance were shown in Fig. 2.10 (a) and (b).

2.2.3 T-shaped gate and Recess process

For high frequency and high speed application, short gate length with low gate resistance is desired. T-shaped gate structure was the most common approach for obtaining low gate resistance. According to the T-gate structure design, the gate length is defined by the small footprint and the wide top offers low gate resistance.

T-shaped gates were achieved by using a multilayer resist technique with E-beam lithography. After patterning the T-shaped gate, the exposed HEMT active layers were recessed to achieve the desired channel current and pinch-off voltage characteristics. That means a groove is formed in the exposed surface of the wafer to “recess” the gate. This process is done by wet etch technique in this study, although dry etching methods may also be used. The recess etching was performed using PH-adjusted solution of succinic (S.A.) and H_2O_2 mixture for selective etching of the heavily doped InGaAs cap layer over InAlAs Schottky layer. The concentration of the etchant should be adjusted to provide an etch rate that is sufficiently slow to allow good control over the recess process, thus enable the operation to approach the target current value, without over etching it. The etching selectivity of InGaAs cap layer over InAlAs Schottky layer was beyond 100.

The target current after the gate recess is a critical parameter affecting the HEMT performance. In order to get the desired recess depth, the recess process was controlled by monitoring the ungated I_{ds}. The method used to control the recess depth is to monitor the source-to-drain current during the etching process. For low noise PHEMT, the saturation current and the slope of the linear region go down as the recess groove was etched deeper and deeper. The wet etchant usually leaves a thin oxide layer on the InAlAs. HCl-based solution was used to remove the surface oxide. After recess etching, Ti/Pt/Au gate metal was

evaporated and lifted off as shown in Fig. 2.6. In chapter 8, the Ti/Pt/Cu Schottky gate on InAlAs layer for the MHEMT was also studied.

2.2.4 Device passivation and contact via formation

FETs are very susceptible to the surface condition, especially in the gate region. As the device scales down, the gate length and spaces of source-to-drain and gate-to-drain become smaller. In situation like this, the devices are very sensitive to the damages and contaminations such as chemicals, gases, and particles. The passivation layer protects the device from damage during process handling (such as "airbridge") and wafer probing (Fig. 2.7). The dielectric layer SiN_x is a common choice for device passivation.

In this study, Samco PECVD system was used for depositing the silicon nitride film. The processing gases of the passivation PECVD were Silane, ammonia, and nitrogen. The process condition is: process pressure: 100Pa, process temperature: 300°C and process time: 10 minutes to form the silicon nitride film 1000Å. The reflection index was inspected by Ellipsometer about 2.0. Then the contact openings of the devices were formed by photo lithography (Fig. 2.8). The RIE was used to open the contact via hole region of the source and drain pads for interconnection. The plasma gases source for SiN_x etching were mixture of CF_4 and O_2.

In order to reduce the total device area, finger-type layout was adopted. As a result, airbridge process was necessary to contact the fingers. The use of airbridge had several advantages including lowest dielectric constant of air, low parasitic capacitance, and the ability to carry substantial currents. The airbridge process flow will be discussed in detail in next section.

2.3 Airbridge formation

Airbridge is built by metal with air between the metal interconnect and the wafer surface beneath. Airbridges are used extensively in GaAs analog devices and MMICs for interconnections. They may be used to interconnect sources of FETs, to cross over a lower level of metallization, or to connect the top plate of a MIM capacitor to adjacent metallization. The airbridges have several advantages including low parasitic capacitance, and the ability to carry substantial currents if the plated airbridge is thick enough.

Analog GaAs devices operating at high current density benefit from airbridges with

thick plated metal layer. Low parasitic capacitance (between the bridge and any metallization beneath) follows from the large spacing and low dielectric constant of the intervening medium. The capacitance is a function of the thickness, and the dielectric constant of the intervening material. Air (k=1.0) has a much lower dielectric constant than any other dielectric, and the space under the airbridge tends to be greater than the thickness of typical dielectrics. These considerations mean that airbridge crossovers are less capacitive than the dielectric type by a factor (typically) of five to twenty.

The following process flow was used to fabricate the airbridge interconnects.

1. The first photolithography for plating vias
2. Thin metals deposition
3. The second photolithography for plating Areas.
4. Electroplating.
5. Second PR removal and thin metal etching.
6. First PR removal

The thickness of the first layer of resist determines the spacing between the bridge and the material beneath (usually a dielectric). The thickness of the photo resist was about 2.5 μm. (Fig. 2.11) After the wafer was immersed in Acetone (ACE) and isopropyl alcohol (IPA) for 5 minutes, and dried by compressed dried air (CDA) blowing, the first layer of photo resist lithography was performed. The thickness was about 2.5 μm. In order to remove the thin PR residues in the exposed region, an O_2 descum process was required after the photolithography. The wafer was plate-baked immediately after the ICP descum. This bake was used to evaporate the remaining solvent in the photo resist. On the other hand, the first photo resist must be sufficiently baked to prevent the “bubbling” after thin metal deposition and the later thermal bake of the second photolithography.

The thin metal structure of the Au airbridge was Ti/Au with Ti as the adhesion layers. The thicknesses of these two metal layers were 300 Å, and 1000 Å, respectively, from the bottom to the top. (Fig. 2.12) The second photolithography was performed on thin multilayer metals. The thickness of the second PR was about 2.5 μm. Same as the first lithography, descum is necessary to remove the polymer residues after development. (Fig. 2.13) The wafer was cleaned before plating to prevent contamination. The current density of the Au electroplating was 1 A/dm^2 and the plating time was 10 minutes for 2.5 μm thick Au. (Fig. 2.14)

The samples after electroplating were immersed in ACE to remove the second photo

resist of the airbridges. The Au of the Ti/Au thin metal was then etched by KI/I2 solution for about 60 seconds. The etching rate of this step is high, and the etching of Au stops at the underlying Ti as the color turned from red to grey. Ti thin metal was also etched by mixed HF: H_2O (1:100) solution. HF is the active ingredient in this etchant, so it also etches oxides. Raising the fraction of HF in the solution increases the etching rate. Titanium is readily oxidized, so it is likely to form an oxide layer from the water, which is readily etched by the HF in this solution, resulting in the formation of bubbles of oxygen.

The samples were dipped in ACE for 20 minutes to remove the first photo resist for plating vias. The PR residues were stripped by O_2 plasma using ICP etcher. And then the specimens were dipped in IPA for 2 min. They were finally immersed in D.I. water, and then followed by CDA drying (Fig. 2.15). Finally, Fig. 2.16(a) shows the plan view for 40μm x 4 MHEMTs and Fig. 2.16(b) shows the SEM photo side view of Au airbridge of the device.

FIGURES:

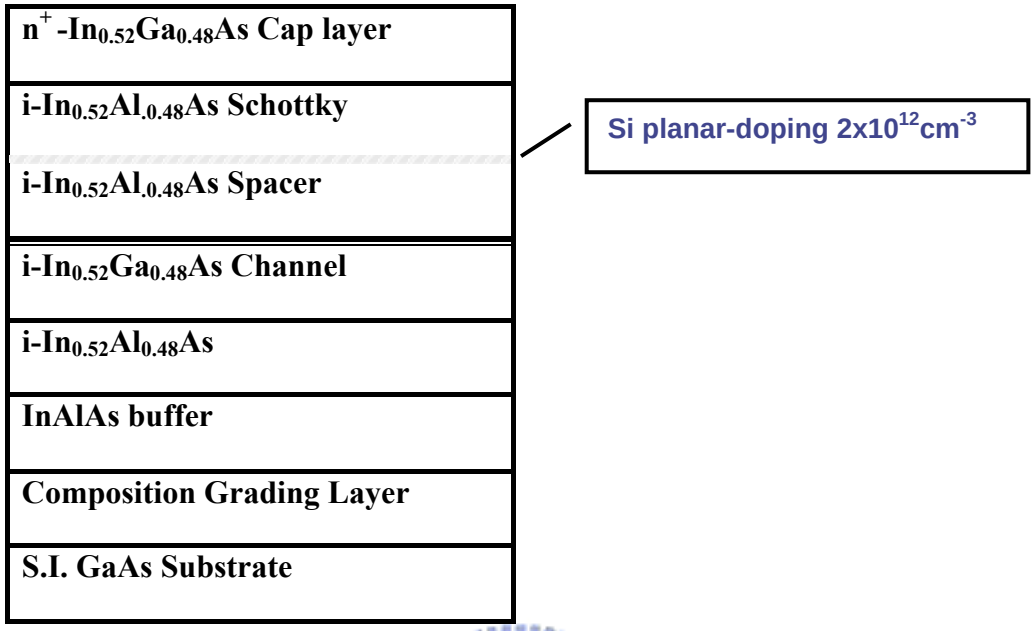


Fig. 2.1(a) Single δ-doped MHENT structure for Low-Noise application

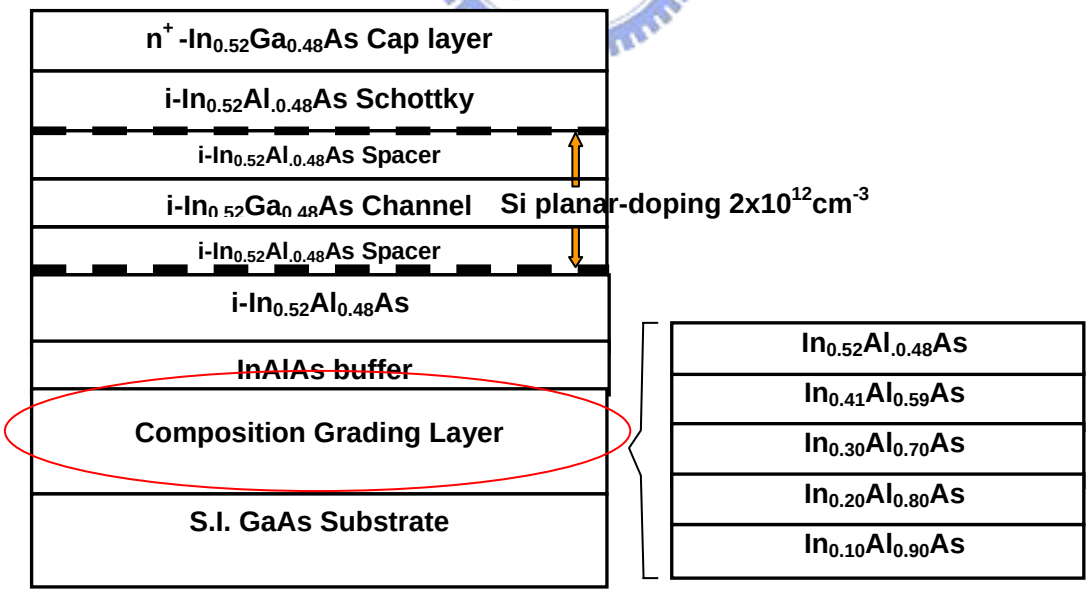


Fig. 2.1(b) Double δ-doped MHENT structure for Power application

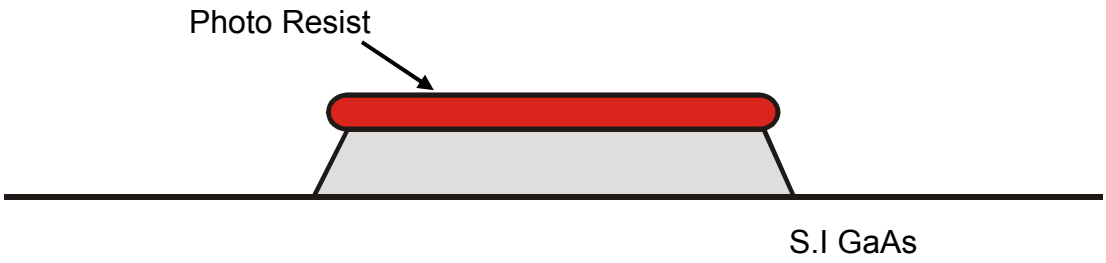


Fig. 2.2 Mesa Etching

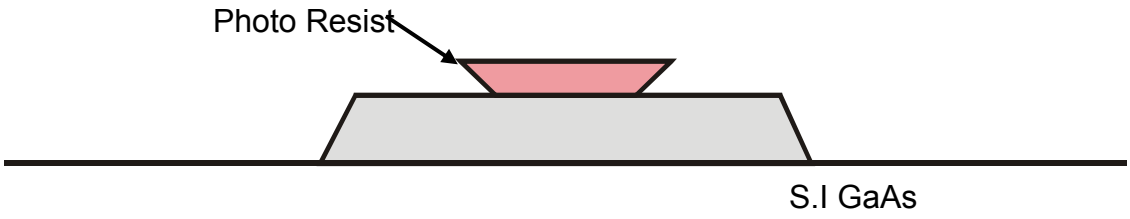


Fig. 2.3 Ohmic photo

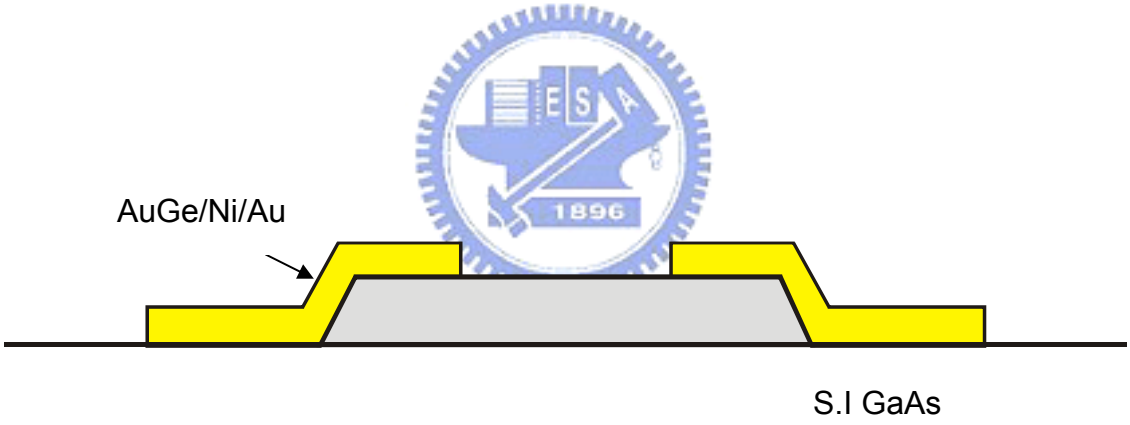


Fig. 2.4 Ohmic metal

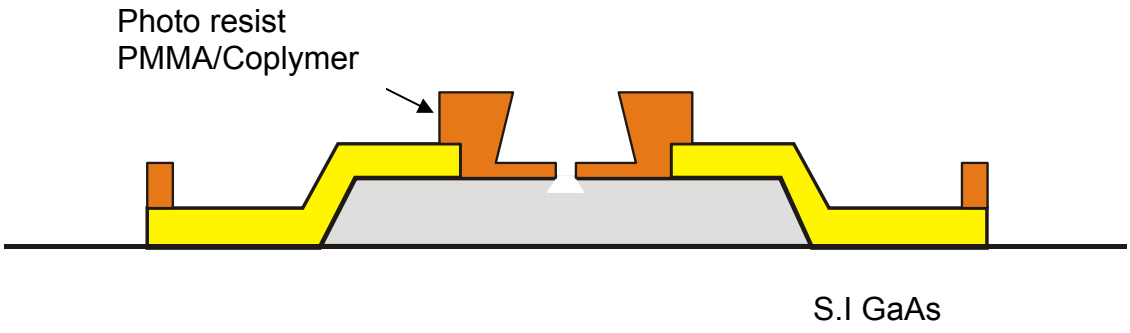


Fig. 2.5 Ohmic window and ebeam T-gate followed by recess

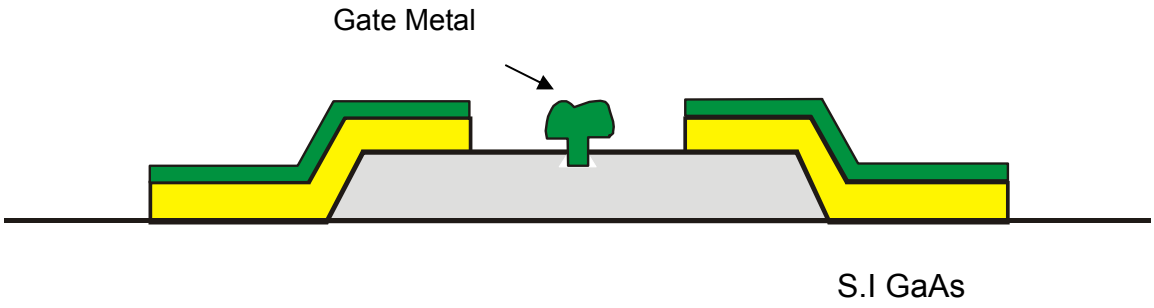


Fig. 2.6 Gate metal deposition

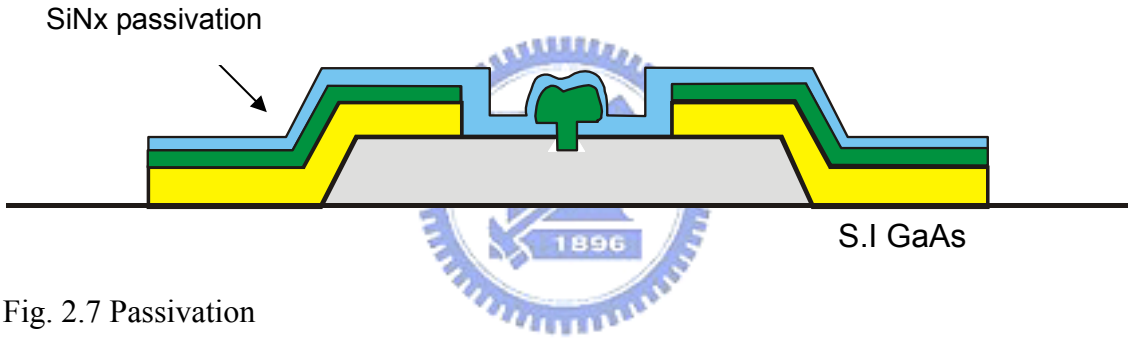


Fig. 2.7 Passivation

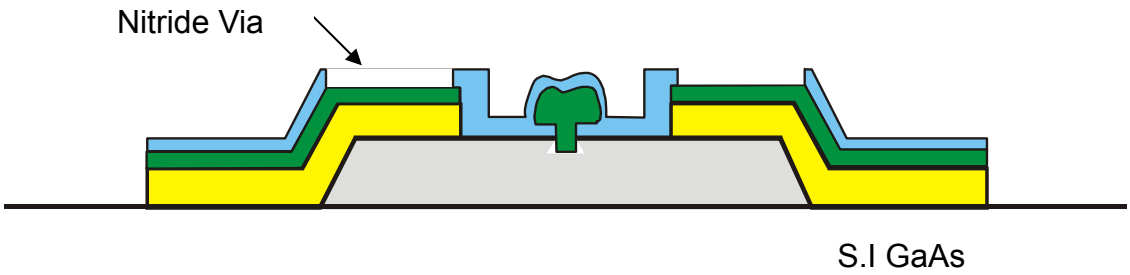


Fig. 2.8 Nitride Via Etching

SPACE(μm)	3	5	10	20	36
Line 1 (Ω)	6.523	8.882	15.753	28.659	50.213
Line 2 (Ω)	6.872	9.001	15.972	29.123	51.345

Lien 1 (Ω/□)	9.8081E+01
Line 2 (Ω/□)	1.0010E+02
Line 1, rc(Ω-cm^2)	**8.77E-07**
Line 2, rc(Ω-cm^2)	**9.06E-07**

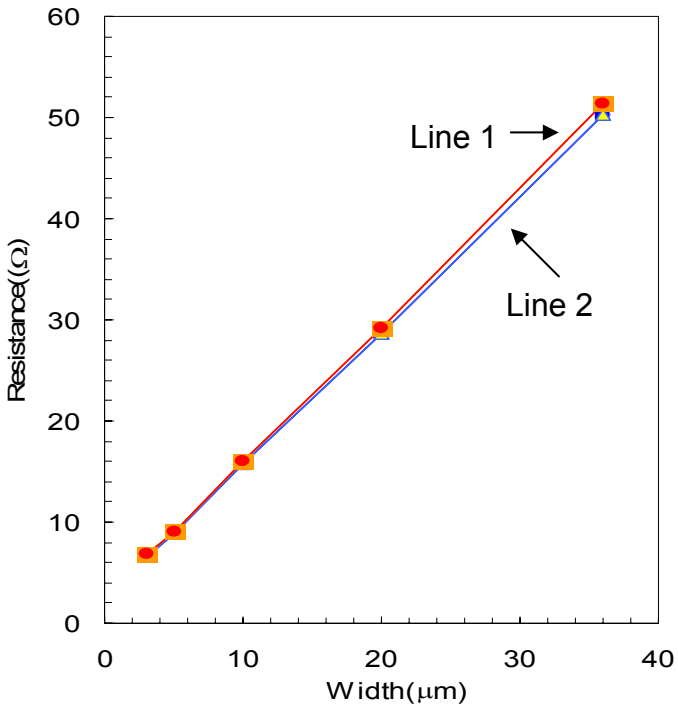


Fig. 2.9 TLM measurement results of the AuGe/Ni/Au Ohmic contact for MHEMT

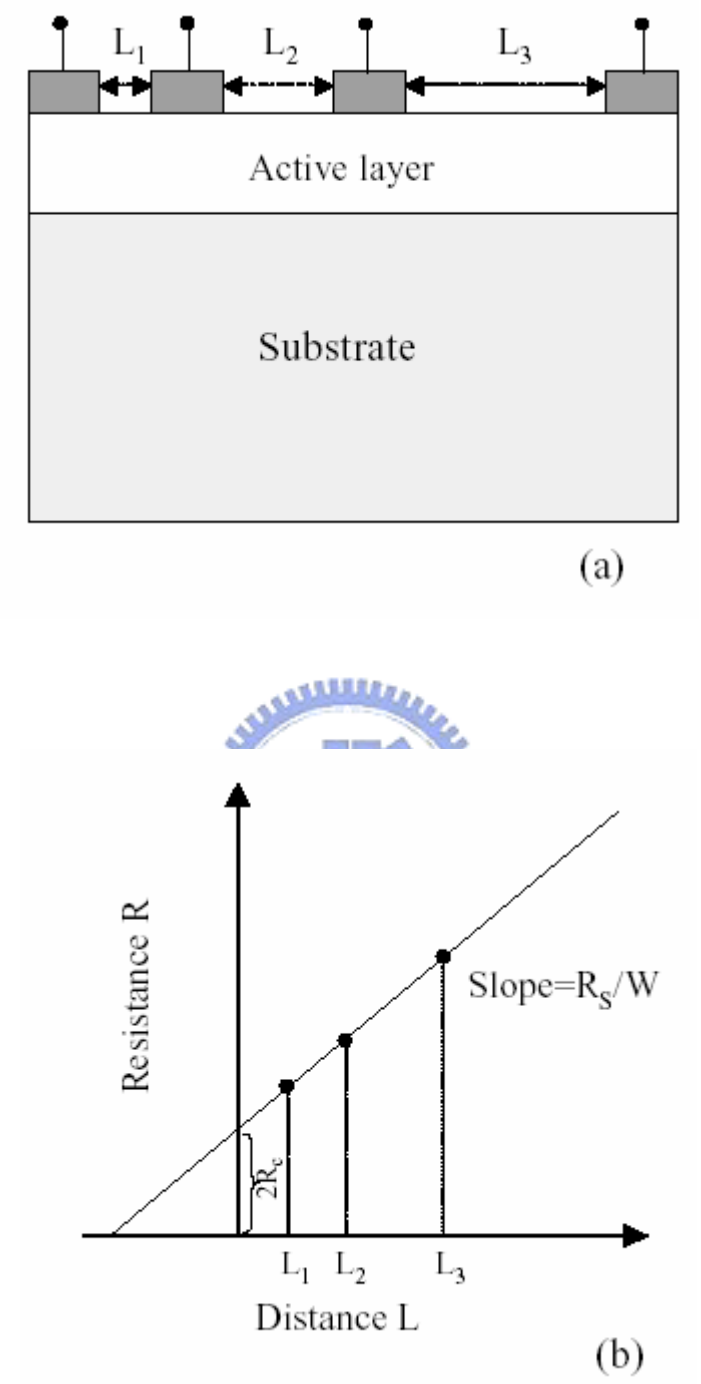


Fig. 2.10 (a) The TLM patterns, (b) The illustration of utilizing TLM to measure the Ohmic contact resistanc.

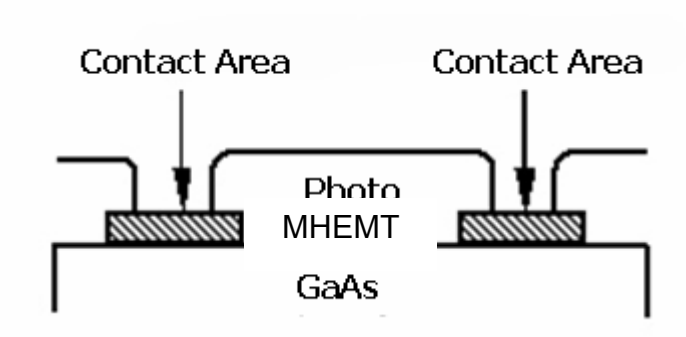


Fig. 2.11 The First Photolithography for Plating Vias

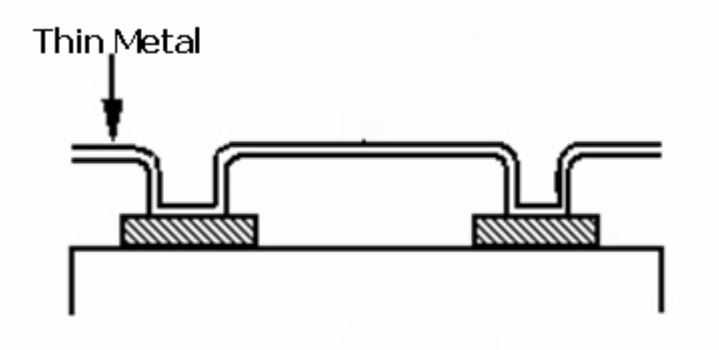


Fig. 2.12 Thin Metals Ti/Au Deposition.

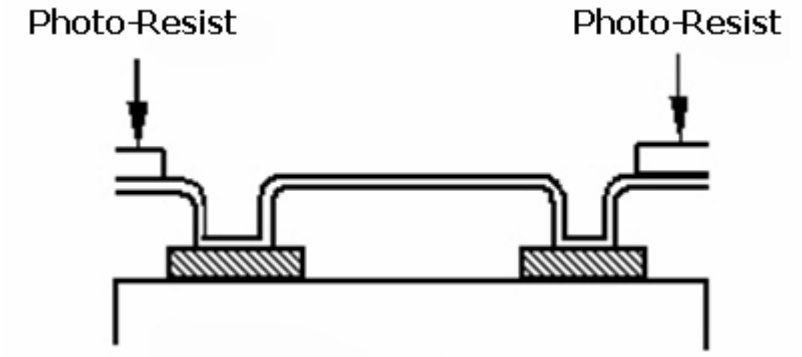


Fig. 2.13 The Second Photolithography for Plating Areas.

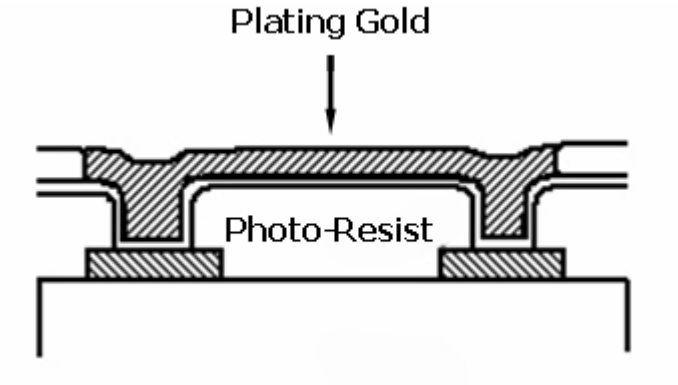


Fig. 2.14 Au electroplating.

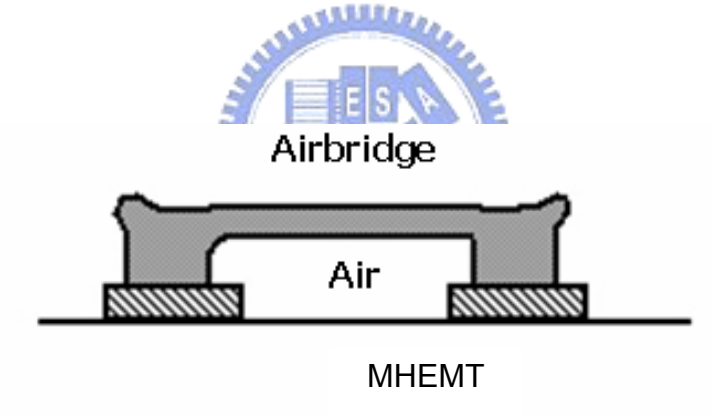
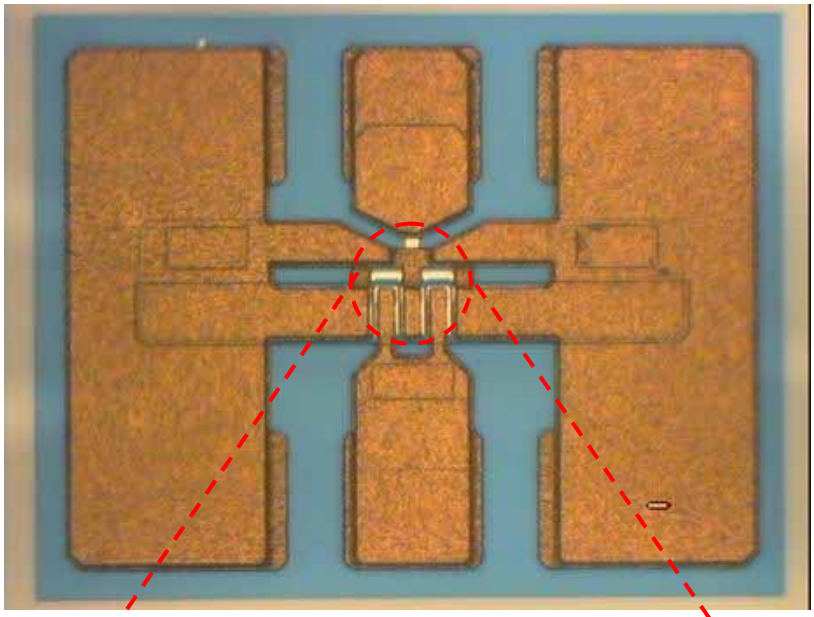
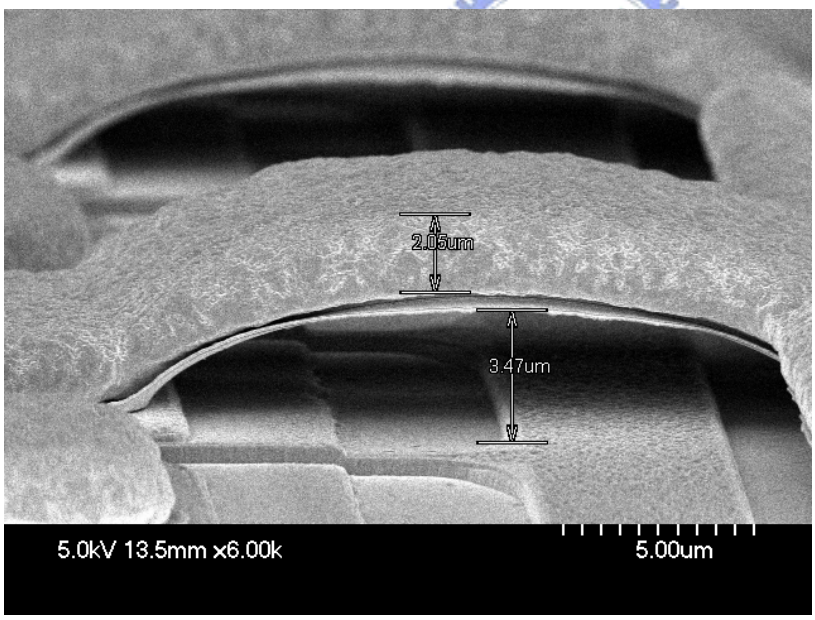


Fig. 2.15 After thin metal etching and PR Removal



(a) Plan view for 40μm x 4 MHEMT



(b) SEM photo of Au airbridge side view

Fig. 2.16 Photos of the Au airbridges of the device

Chapter 3

DC and RF Measurements of GaAs Metamorphic High Electron Mobility Transistors

3.1 Device Characterization

After the device fabrication process, DC and RF performance of the GaAs MHEMTs must be measured using on-wafer measurement. For the DC measurement, the I-V characteristics were obtained easily by using an HP4142B Modular DC Source/Monitor and SUSS PA200 Semi-Auto Probe Station. The Transmission Line Model (TLM) method for determining specific contact resistance was adopted by using 4-wires measurement and Keithley 2400 SourceMeter. The *S*-parameters for the MHEMT devices were measured by HP8510XF Vector Network Analyzer using on-wafer GSG probes from Cascade MicroTech. However, finding the RF behavior of a device on a wafer was a complicated process. For conventional RF measurement of a packaged device, the wafer needs to be diced and then an individual die should be mounted into a text fixture. Discriminating between the die's and the fixture's responses became an issue. Furthermore, fixturing die was a time-consuming process, making it impractical for high-volume screening. Thus the need for on-wafer RF characterization was arisen [3-1, 3-2].

Before examining the RF measuring process for the MHEMTs, the electrical behavior and characterization of the device are stated in the following section. In this study, de-embedding which must also be performed to discover the RF performance of the on-wafer device is discussed. Therefore, device layout designing for calibration will be described in section 3.4 is an important step of on-wafer RF characterization.

3.2 DC characteristics

3.2.1 I-V characteristics [3.3]

The band diagrams at three different positions along the channel are illustrated in Fig.

3.1. There is a potential drop of channel charge density in the direction parallel to the channel, causing q'_{CH} to be a function of the position x. In order to relate the HEMT equations to the well-developed MOSFET equations, a per area gate oxide capacitance was define as C'_{OX}. [3.3] Therefore, the channel charge sheet density is expressed as:

$$q'_{CH} = -C'_{OX}[V_{GS} - V_T - V_{CS}(\chi)] \qquad (3\text{-}1)$$

We denote the channel-to-source potential resulting from the applied Gate-Source voltage V_{GS} and Drain-Source voltage V_{DS}. V_T is threshold voltage and the x means the position along the channel. The additional potential $V_{CS}(x)$ is called the channel-source potential. When $V_{DS} \neq 0$, the channel channel-source varies with x. In this figure, the channel-source potential measures the potential difference between any point x along the channel with respect to the potential of the source. The channel current equation which we are familiar with $I = qA\mu_n\varepsilon$ (A=area) is proportional to the cross-section area of the current conduction, the charge density, the mobility μ_n, and the electric field. Therefore, we obtain the form of the drift equation in HEMT:

$$I_{CH}(\chi) = -WC_{OX}\mu_n[V_{GS} - V_T - V_{CS}(\chi)]\frac{dV_{CS}(\chi)}{d\chi} \qquad (3\text{-}2)$$

We note that q'_{CH} is a negative quantity in HEMT, since electrons accumulated in the channel are negative charges. In fact, if we choose $x = L$ at the drain, this constant channel current is equal to the negative of the drain current. Hence, we have $I_D = -I_{CH}$, we find:

$$\int_0^L I_{DS}\,dx = -C'O\int_{V_{CS(O)}}^{V_{CS(L)}} C_{OX}\,\mu_n[V_{(GS)} - V_{(T)} - V_{(CS)}(\chi)]dV_{CS}(\chi) \qquad (3\text{-}3)$$

To carry out the integration in Eq. (3-3), we assume temporarily that we are working in the linear region such that current saturation due to channel pinch off at the drain does not occur. The I-V characteristics after pinch off will be dealt with shortly. In the linear operating region, the boundary conditions are $V_{CS}(L) = V_{DS}$ and $V_{CS}(0) = 0$. Hence, Eq. (3-3) leads to:

$$I_D = \frac{W_g C'_{OX} \mu_n}{L g}[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}] \qquad (3\text{-}4)$$

Eq. (3-5) is plotted schematically in Fig. 3.2, with I_D shown as a function of V_{DS}. The value of V_{DS} corresponding to the attainment of $I_{D,sat}$ is denoted as $V_{DS,sat}$, the saturation voltage. The saturation voltage can be obtained by taking the derivative of I_D will respect to V_{DS} and setting the result to zero. We find that:

$$V_{DS,SAT} = V_{GS} - V_T \qquad (3\text{-}5)$$

At this saturation voltage, q'_{CH} calculated from Eq. (3-1) is identically zero at the drain (pinch off). However, we realize that this conclusion originates from the fact that we are extending the validity of Eq. (3-1) all the way to where $q'_{CH}(L)$ is identically zero. Physically, the channel at the drain does not pinch off completely. Instead, there is a finite thickness of accumulation of charges at which q'_{CH} $x=L$ is nonzero. The drift velocity is high, but nonetheless finite, so a constant current is maintained throughout the channel. Therefore, a complete model of the drain current is given by:

$$I_{DS} = \frac{W_g C'_{OX} \mu_n}{L g}[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}] \quad \text{for } V_{DS} < V_{DS,SAT}$$

$$= \frac{W_g C'_{OX} \mu_n}{L g}[\frac{(V_{GS} - V_T)^2}{2}] \quad \text{for } V_{DS} \geqq V_{DS,SAT} \qquad (3\text{-}8)$$

For HEMTs, it is convenient to define the *saturation index (α)* as:

$$\alpha = 1 - \frac{V_{DS}}{V_{DS,SAT}} \quad \text{for } V_{DS} < V_{DS,SAT}$$

$$= 0 \quad \text{for } V_{DS} \geqq V_{DS,SAT} \qquad (3\text{-}9)$$

The drain current increases due to the perturbations in V_{GS} and V_{DS}. The mutual transconductance measures the amount of current increase due to the increment in the gate bias.

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS}=const.} \quad (3\text{-}10)$$

We also can write:

$$g_m = \frac{W_g C'_{OX}\ \mu_n}{L_g}(V_{GS} - V_T) * (1-\alpha) \quad (3\text{-}11)$$

3.2.2 Transmission line model (TLM) [3.4]

The most widely used method for determining specific resistance is the method of Transmission Line Model (TLM) which is also mentioned in chapter 2. In this particular approach, a linear array of contacts is fabricated with various spacings between them as shown in Fig 3.3. The distances between TLM electrodes are 3μm, 5μm, 10μm, 20μm, and 36μm, respectively in this study. The resistance between the two adjacent electrodes can be plotted as a function of the space between electrodes. The plot is shown in the Fig. 3.4. Extrapolating the data to L= 0, one can calculate a value for the term R_c (Ω-mm).

$$R = 2R_C + \frac{R_S L}{W} \quad (3\text{-}12)$$

where R is measured resistance, R_c is contact resistance, R_s is sheet resistance of the channel region, W is electrodes width, and L is space between electrodes. Another important parameter is the specific contact resistance ρ_c (Ω-cm^2), which is defined as

$$\rho_C = \frac{W^2 R^2}{R_S} \quad (3\text{-}13)$$

This specific contact resistance is a practical figure of merit for contact resistance. It includes a portion of the metal immediately above the metal-semiconductor interface, a part of the semiconductor below the interface, current crowding effects, spreading resistance under the contact, and any interfacial oxide that may present between the metal and the

semiconductor.

3.2.3 Breakdown characteristics [3.5]

Breakdown mechanisms and models discussed in many articles. One of the models showing it is dominated by the thermionic filed emission (TFE) / tunneling current from the Schottky gate. This model predicts that the two-terminal breakdown voltage is lower at higher temperature because tunneling current increases with the temperature. Higher tunneling current occurs at higher temperature because carriers have higher energy to overcome the Schottky barrier. Other model suggests that impact-ionization determines the final two-terminal breakdown voltage, because the avalanche current decreases with increasing temperature. Lower avalanche current occurs at higher temperature because phonon vibrations as well as carrier-carrier scattering increase with increasing temperature. Either model is incomplete since coupling exists between TFE and impact ionization mechanisms. In addition, different devices may suffer from different breakdown mechanisms, depending on the details of the device design (insulator thickness, recess, channel composition, and so forth). In this study, the gate-to-drain breakdown voltage BV_{gd} is defined as the gate-to-drain voltage when the gate current is 1mA/mm.

3.3 RF Characteristics & Measurements

3.3.1 Scattering parameters [3.6]

Scattering parameters, generally referred to as *S*-parameters, are fundamental to microwave measurement. This section discusses *S*-parameters and the motivation for their use. For a device such as field-effect transistor with the input and output terminals can be treated as a two-port network as shown in Fig. 3.5. V_1 and I_1 are the voltage and current at the input, and V_2 and I_2 are the voltage and current at the output. Major characteristics, such as gain, return loss, and impedance matching can be calculated from known relationship among the input and output signals. The impedance parameters (*z*-parameters), conductance parameters (*y*-parameters) and hybrid parameters (*h*-parameters) are used to characteristic the devices because the parameter can be measured by open or short termination. The *z*-, *y*- and *h*-parameters can therefore be stated by the following equations:

z-parameters: $\begin{bmatrix} V1 \\ V2 \end{bmatrix} = \begin{bmatrix} z11 & z12 \\ z21 & z22 \end{bmatrix} * \begin{bmatrix} i1 \\ i2 \end{bmatrix}$

y-parameters: $\begin{bmatrix} i1 \\ i2 \end{bmatrix} = \begin{bmatrix} y11 & y12 \\ y21 & y22 \end{bmatrix} * \begin{bmatrix} V1 \\ V2 \end{bmatrix}$

h-parameters: $\begin{bmatrix} V1 \\ i2 \end{bmatrix} = \begin{bmatrix} h11 & h12 \\ h21 & h22 \end{bmatrix} * \begin{bmatrix} i1 \\ V2 \end{bmatrix}$

When the frequency is up to several GHz, the *z*-, *y*-, *h*- parameters can not be directly obtained by the open or short circuit because of the reflected wave from the open or short terminations. The open or short terminations will induce the network oscillation. Therefore the scattering parameters are used to characterize the performance of a device. Fig. 3.6 shows the two-ports 1 and 2. The relation of the microwave signals and *s*-parameters can be described as

s-parameters: $\begin{bmatrix} b1 \\ b2 \end{bmatrix} = \begin{bmatrix} s11 & s12 \\ s21 & s22 \end{bmatrix} * \begin{bmatrix} a1 \\ a2 \end{bmatrix}$

a_1: the electric field of the microwave signal entering the component input

b_1: the electric field of the microwave signal leaving the component input

a_2: the electric field of the microwave signal entering the component output

b_2: the electric field of the microwave signal leaving the component output

By the definition, then,

$$s11 = \left.\frac{b1}{a1}\right|_{a2=0}, \quad s21 = \left.\frac{b2}{a1}\right|_{a2=0}, \quad s12 = \left.\frac{b1}{a2}\right|_{a1=0}, \quad s22 = \left.\frac{b2}{a2}\right|_{a1=0}$$

Therefore, s_{11} is the electric field leaving the input divided by the electric field entering the input, under the condition that no signal enters the output. The measurement includes instruments for the DC and RF measurement. Where a_1 and b_1 are electric fields, their ratio is a reflection coefficient. Similarly, s_{21} is the electric field leaving the output divided by the electric field entering the input, when no signal enters the output. Therefore, s_{21} is a transmission coefficient and is related to the insertion loss or the gain of the device. Similarly, s_{21} is a transmission coefficient related to the isolation of the device and specifies how much

power leaks back through the device in the wrong direction. s_{22} is similar to s_{11}, but looks in the other direction into the device. The *s*-parameters have both the amplitude and phase.

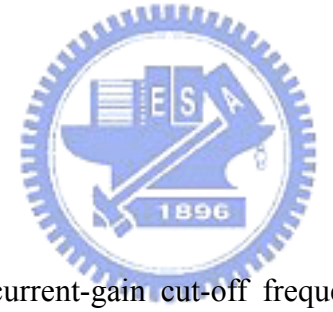
3.3.2 Current gain cutoff frequency f_T

Traditionally, transistors are characterized using figures of merit such as the unity current-gain cutoff frequency (f_T). Consider a transistor characterized by the following small-signal *y*-parameters

$$i_1 = y_{11}(\omega)V_1 + y_{21}(\omega)V_2$$
$$i_2 = y_{21}(\omega)V_1 + y_{22}(\omega)V_2$$

The currents and voltages are defined in Fig. 3.5. For example, we use the *y*-parameters of a FET in the common source configuration in Fig. 3.7.

$$i_g = y_{gg}(\omega)V_{gs} + y_{gd}(\omega)V_{ds}$$
$$i_d = y_{ds}(\omega)V_{gs} + y_{dd}(\omega)V_{ds}$$



The unity short-circuit current-gain cut-off frequency is defined as the frequency at which the short-circuit current gain is unity:

$$h_{21}(\omega) = \left|\frac{y_{21}(\omega_T)}{y_{11}(\omega_T)}\right| = 1$$

Since the HEMT is the common source configuration, the maximum short-circuit current gain can be approximated by

$$\left|\frac{y_{21}(\omega_T)}{y_{11}(\omega_T)}\right| = \left|\frac{y_{ds}(\omega_T)}{y_{gg}(\omega_T)}\right| \approx \frac{g_m}{\omega C_g W_g L_g}$$

Where g_m is the transconductance. Notice the 1/ω decrease with frequency (20 dB per decade) using $20\log(y_{21}/y_{11})$ of the short-circuit gain. The intrinsic *S* parameters are used to determine

the unity current-gain cut-off frequency (f_T). It can be determined by extrapolation of the short-circuit current gain $h_{21} = 0$ dB. h_{21} can be defined as

$$h_{21} = \frac{2 s_{21}}{(1 - s_{11})(1 + s_{22}) + s_{12} s_{21}}$$

Fig. 3.8 shows the definition of the cut-off frequency (f_T).

3.3.3 Maximum frequency of oscillation f_{max}

The microwave performance of a transistor is usually characterized by the maximum stable power gain as a function of frequency. The maximum power gain is obtained by simultaneously matching the input and output to obtain a conjugate match. Conjugate match means that the source impedance Z_S and the load impedance Z_L satisfy simultaneously:

$$Z_S = Z^*_{IN}, \quad Z_L = Z^*_{OUT}$$

Where Z_{IN} is the input impedance of the two-port network measured at port 1 with the load impedance Z_L connected at port 2 and where Z_{OUT} is the output impedance of the two-port network measured at port 2 with the source impedance Z_S connected at port 1. The maximum power stable gain (G_{max}) consisting of the maximum available gain (MAG), and the maximum stable gain (MSG) were derived from the *S*-parameter data by the equation:

$$GMAX = \left|\frac{S_{21}}{S_{12}}\right| K - \sqrt{(K^2 - 1)},$$

where K is the Rollett stability factor

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |D|^2}{2|S_{12}\,|S_{21}||}$$

$$D = S_{11} S_{22} - S_{12} S_{21}$$

The MAG is the highest power gain of the two-port network with the

impedance-matched input and output. The MAG of a transistor can only be obtained when the transistor is unconditionally stable, *i.e*. $K>1$. The MSG is the highest power gain of a two-port network with the resistive loaded in both input and output ports. The MSG can be obtained if the transistor where potentially unstable according to:

$$MSG = MAG|_{K=1} = \left|\frac{S21}{S12}\right|$$

The device maximum power gain cut-off frequency can then be defined as the frequency at $G_{max} = 0$ dB.

The comparison of the high-frequency performance of two-port devices is usually done using the unilateral power gain U derived by Mason [3.7]:

$$U = \frac{\frac{1}{2}\left|\frac{S_{21}}{S_{12}} - 1\right|^2}{K\left|\frac{S_{21}}{S_{12}}\right| - Re\left(\frac{S_{21}}{S_{12}}\right)}$$

U is the maximum available power gain (MAG is introduced in the previous section) of a device once it has been unilateralized ($y_{12} = 0$) using lossless feedback techniques.

The maximum frequency of oscillation f_{max} is then defined as the frequency at which U is unity. f_{max} is often referred to as the frequency at which a three-port device switches form active to passive. U can then be written

$$U(\omega) = \left(\frac{\omega_{max}}{\omega}\right)^2$$

The unilateral power gain will then decrease at a rate of 20 dB per decade (using 10logU) like the short-circuit current gain.

3.3.4 Noise figure [3.8]

Noise is related to the device channel and capacitive coupling between the channel and

the gate. The gate noise is represented by a gate-current noise generator i_{ng}^2 and is caused by charge fluctuation in the channel, which in turn induces the fluctuation of compensating charge on the gate electrode. The gate-noise is proportional to f^2 in HEMTs. The channel noise is represented by a drain-current noise generator i_{nd}^2 and is caused by various physical mechanisms driven by the electric field in the channel. In the linear region of the device channel, the channel noise is caused by thermal noise (Johnson noise). A thermal noise voltage caused in the channel leads to a modulation of the channel resistance and causes a drain voltage fluctuation at the channel end (drain). The corresponding drain noise current is inversely proportional to $g_m I_{DS}$. In the high-field region, hot electron scattering, intervalley scattering, and high diffusion noise contribute to the channel noise.

Another noise source is gate leakage. A new model that takes this effect into account by an additional parallel resistor to the gate capacitance and the resistor R_i has been proven to a good correlation between predicted and measured minimum noise figures even at low frequencies. The negative influence of the gate leakage on the noise figure vanishes at higher frequencies. Noise figure reflects the noise added to the signal by the imperfect amplifier, and is defined as the signal-to-noise ratio (S/N) of the input signal divided by the signal-to-noise ratio of the output signal,

$$F = (S_i/N_i)/(S_0/F_0)$$

It is usually expressed in dB:

$$NF = 10\log F$$

We shall use F to designate absolute noise figure and NF to designate figure expressed in dB. The noise performance of a FET may be quantified by the noise figure, NF, which is a function of frequency, FET bias voltages, and impedance matching. Another noise figure of FETs structure is shown as the following equation.

$$NF = 1 + \sqrt{2}\frac{f}{f_t}\sqrt{g_m(R_S + Rg)}, f_t = \frac{g_m}{2\pi C_{gs}}$$

In general, high source-drain current contributes to noise by electron scattering, and this

noise is reduced as the current is reduced. However, reducing the current too close to pinch-off reduces the transconductance, which causes increased noise figure because of decrease gain. There will exist an optimum gate bias that presents the best compromise.

3.3.5 RF measurement calibration [3.6]

Before the on-wafer measurement, the measuring system must be calibrated first to eliminate the extrinsic parasitic components of the cables, adaptors, probes and so on. The GSG (ground-signal-ground) probe tips are used in this study. The planar calibration was first carried out to make the tips are at the same height to prevent the nonuniform contacts. After the planar calibration of the probe tips, the calibrations for the measurement were made. In this study, the Short-Open-Load-Thru (through) (SOLT) calibration was adopted for the frequency ranging up to 40GHz. Fig. 3.9 shows the calibration pads for the short, through and load, respectively. Above the frequency of 40GHz for *S*-parameter measurement, the Thru-Reflect-Line (TRL) calibration was adopted and discussed in the following section.

3.4 Device Layout Designing

3.4.1 Effect of Pad Parasitics & De-embedding

When defining the high frequency performance of the MHEMT, de-embedding all the conductors on the top surface of the wafer (pad, interconnect, and metal) and defining the reference plane horizontally are necessary. This helps to understand what is going on of the active region of the device and is helpful in device model development where RF quantities can be miniscule. Yet the device cannot be run without metal, so de-embedding using this method is not useful for designing circuits. Rather, de-embed up to the edge of the device, cutting the reference plane vertically through the wafer. The Device-Under-Test (DUT) then includes some device metal but not the probe pads and interconnecting lines. Because the interconnecting lines are different with layout, they should be excluded from the DUT model.

In addition, pad parasitics can have a demonsratable effect on the device cut-off frequency f_T. In field effect transistors (FETs), f_T is defined as

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

where g_m is the transconductance, C_{gs} the gate-source capacitance, C_{gd} the gate-drain capacitance, h_{21} the device's gain (a hybrid parameter), and f the frequency. The input admittance measurement y_{11} that captures the gate behavior is sensitive to parasitics. The parasitic capacitance between the pad and interconnects adds to C_{gs} and C_{gd}. Contact variability of the probes to the pads can also affect the admittances. When defining the reference plane, probe placement error varies from touchdown to touchdown, slightly changing the amount of series inductance L_s. Fig. 3.10 shows the effect of pad parasitics on h21 & f_T. In this figure, the series inductance L_s can resonate with the device's output capacitance C_0, causing $|h_{21}|$ to shift up. C_0 is composed principally of the drain-to-source capacitance C_{DS}. Because C_{DS} is on the order of femtofarads, pad and interconnect parasitics add a pole to the plot around which the upward shift occurs [3-9]. Making the pads as small as possible is the simplest way to lessen this effect.

3.4.2 Device Layout

Fig. 3.11 (a) and (b) show the top-views of the A-type and the C-type device layout in this study. The C-type layout is designed for Ka band applications. The A-type is mostly used in this study and designed for above-Ka band. The transmission line pads type of the layout is designed by using simulation software which is called AppCAD from Agilent Technology. Fig. 3.12(a) shows the Coplanar Waveguide (CPW) structure which is designed at 94 GHz for the A-type device. The substrate in this simulation was GaAs with the dielectric constant of 13. The width of signal pad (W) and the space between signal and ground are 50 μm and 40 μm, respectively. The characteristic impedance (Z_0) is 49.3 Ω at 94 GHz. Fig. 3.12(b) show the final designed A-type layout using the result of the simulation. The calibration standards discussed in next section is also designed by the rule.

3.4.3 Thru-Reflect-Line (TRL) calibration

Transmission lines are simple to understand and easy to fabricate. Their physical dimensions and the board material decide their characteristics impedance. Because it is based on a transmission line standard, TRL is a powerful method [3-2]. Fig. 3.13 shows the TRL standards of the MHEMT devices (A-type). A short transmission line serves as the thru. When the offset delay is set to zero, the THRU's midpoint sets the electrical reference plane. In

general, the line lengths leading to the device should be the same length as the THRU. Known to within +/-90° is the THRU's phase length θ. The reflect standard can be either an open or a short. Both of them are designed for the MHEMTs.

In Fig. 3.13, the reflect does mot have to be a perfect open or short, although the best results have a $|\Gamma|_{REFLECT}$ close to 1. The REFLECT's phase should be generally known to within +/-90°. When selecting a REFLECT, an open operates over a broader bandwidth than a shorter [3-1]. After we know the phase of the REFLECT, it can be used to define the electrical reference plane instead of the thru.

The precision standard is the LINE. Its characteristic impedance Z_0 sets the reference impedance for the entire RF test system. TRL sets the test system's Z_0 to be equal to the impedance of the line standard. The LINE standard is usually good over an 8:1 (frequency span: start frequency). In this study, there are LINE-1 and LINE-2 shown in Fig. 3.13. In order to present different phases during calibration, the THRU and LINE standards must be different lengths. The THRU's optimum length is 90°, or λ/4 of the center frequency. The length of LINE-1 for frequency range 10 to 80 GHz is 600 μm, and the length of LINE-2 frequency range 21 to >110 GHz is 300 μm. The time delay (*Tdelay*) of these two line standards are 5.18 ps and 2.59 ps, respectively. Time delay was defined as follow equation:

$$Tdelay = \frac{L}{V} = \frac{\lambda / 4\sqrt{\varepsilon_r}}{C / \sqrt{\varepsilon_r}}$$

where L is the length of transmission line, ε_r is the dielectric constant of the GaAs substrate, and V is 0.386 fraction of C which is the light velocity. All of these parameters were also shown in Fig. 3.12(a).

3.4.4 RF measurement after TRL calibration

After a successful TRL calibration, the reference plane is not necessarily in-phase with the RF signal coming out of the test port. In this study, the reference plane was set in the center line of the thru patterns. The corresponding reference plane of the A-type device was move forward to active region for 100 μm.

Fig. 14 and Fig. 15 show the measured *S*-parameters of REFLECT-Open and REFELCT-Short, respectively. In order to focus on the high frequency behavior of the TRL

standards, the frequency range was from 75 to 110 GHz. The two REFELCT standards were measured first after using the system calibration (SOLT). After the TRL calibration, the *S*-parameters of two REFLECT standards were measured again for comparison. After TRL calibration, the S_{11} and S_{22} of the two REFLECTs are both more close to the point of reflect coefficient Γ= 1 of the Smith chart. In addition, the S_{12} and S_{21} of the two REFLECTs are also closer to the designed point (Open and Close) of the Smith chart. This shows the improvement for the matching between test port and the patterns after TRL calibration. The improvements were also shown in Fig. 16 and Fig. 17 for LINE-1 and LINE-2, respectively.

The THRU standard was measured for checking the magnitude and phase of S_{21}. Fig. 3.18(a) and Fig. 3.18(b) show the Smith charts of the S-parameter and the magnitude/phase of S_{21} before and after TRL calibration. After TRL calibration, the S_{21} becomes stable value 0dB and 0 degree. The improvement shows that the offset delay is 0 ps for the THRU standard and the loss and phase were calibrated successfully.

In order to verify the TRL standards are useful for the device, the HEMTs were measured before and after TRL calibration. Fig. 3.19(a) shows the current gain h_{21} from 1 to 110 GHz without TRL calibration. The h_{21} which is shifted up above 30 GHz is caused by parasitic inductance and capacitance. In Fig. 3.19(b), we focus on high frequency h_{21} & power gain (MAG/MSG) ranging from 60 to 110 GHz before and after on-wafer TRL calibration. After on-wafer TRL calibration, the h_{21} shows linear behavior and no more shift-up. The cut-off frequency f_T and maximum frequency f_{max} can also be defined clearly.

The TRL calibration and the designed patterns will be used for high frequency measurement in this study.

FIGURES:

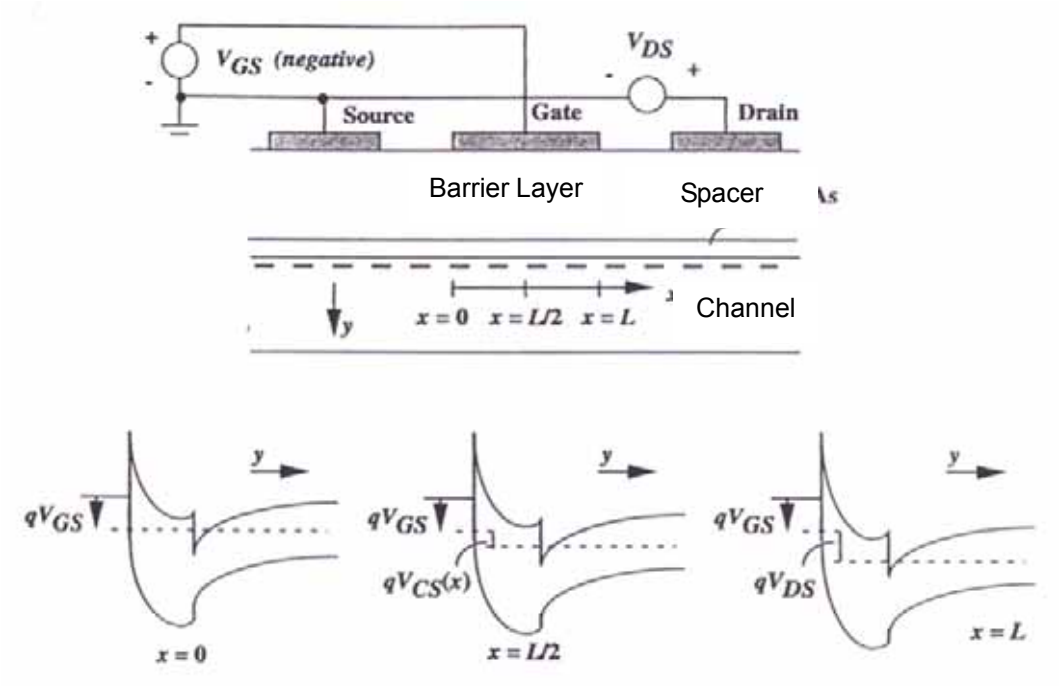


Fig. 3.1 Band diagrams at three different locations along the channel of a HEMT

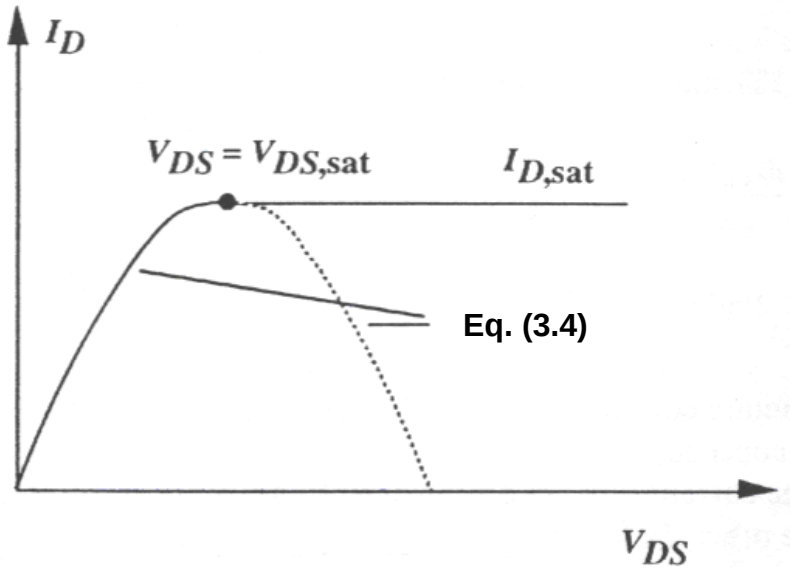


Fig. 3.2 Actual characteristics and those predicted by Eq. (3-3)

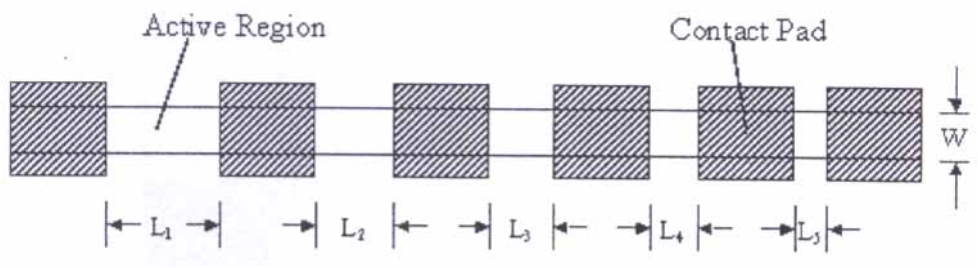


Fig. 3.3 TLM pattern

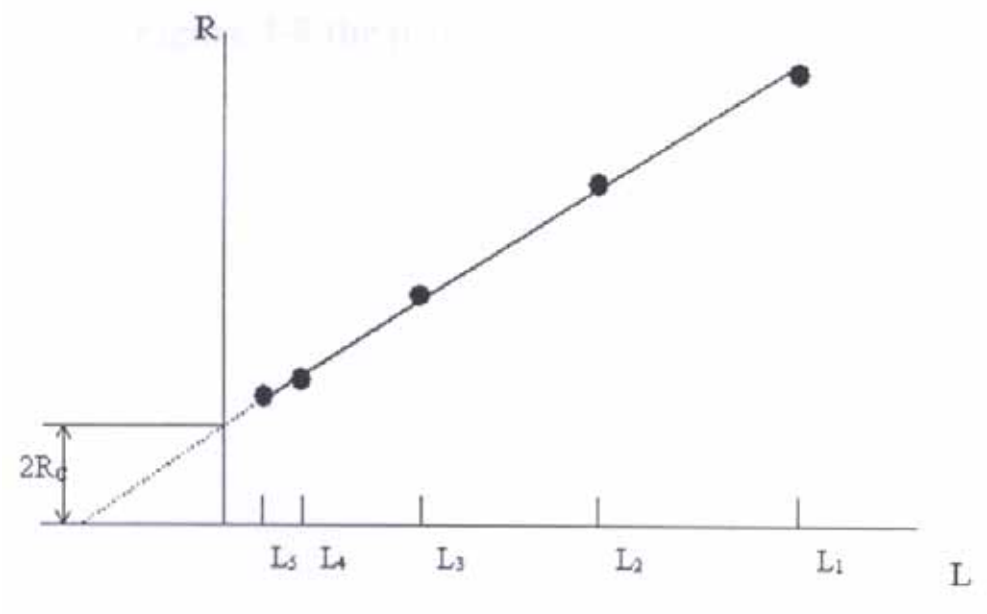


Fig. 3.4 The illustration of utilizing TLM to measure ohmic contact resistance

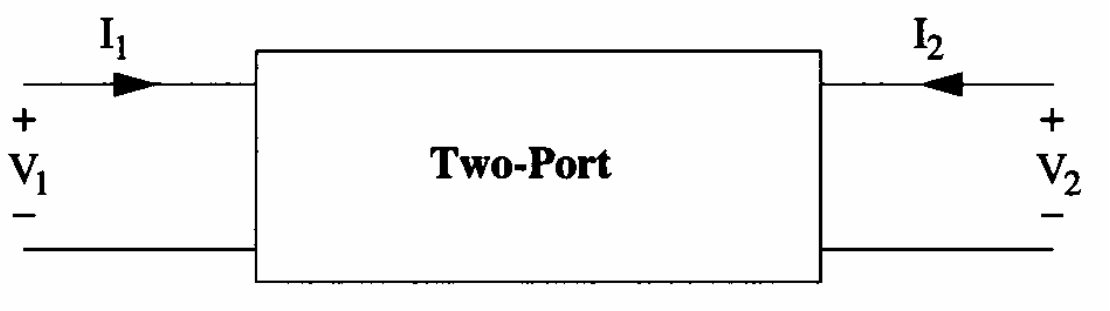


Fig. 3.5 The equivalent two-port network schematic at low frequency

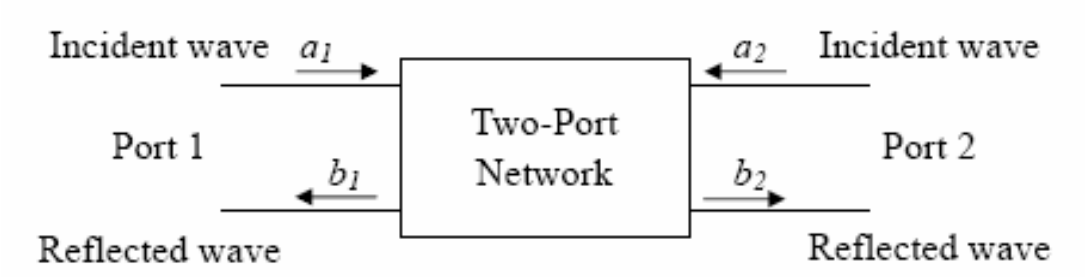


Fig. 3.6 The equivalent two-port network schematic at high frequency

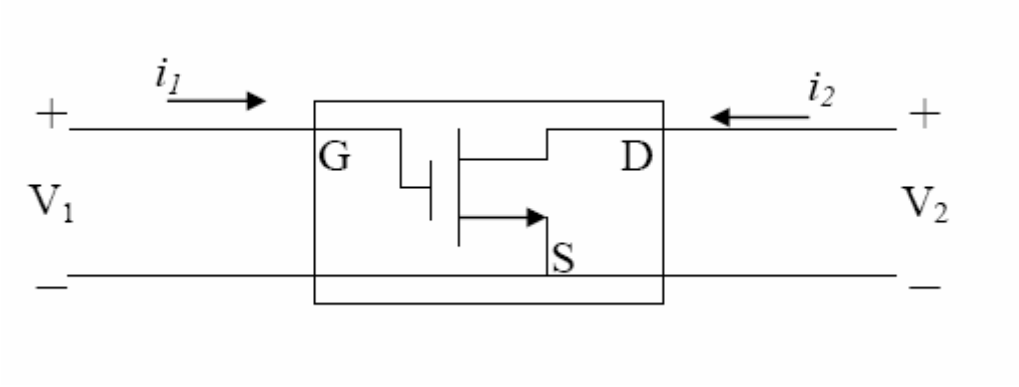


Fig. 3.7 Small signal representation of a common source FET

fT is the cutoff frequency where H21 = 1 (0dB). This is usually extrapolated from H21 measurements by fitting a -20dB/decade slope, see below.

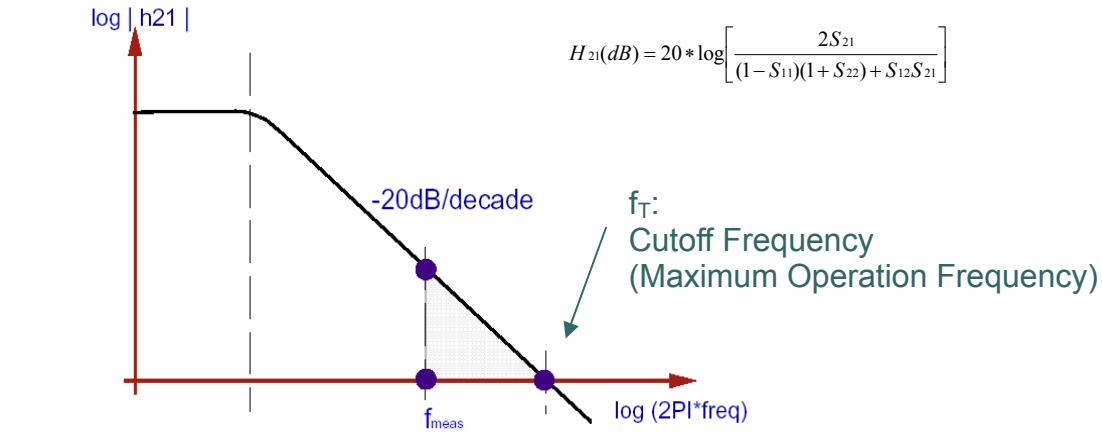


Fig 3.8 Definition of Cutoff Frequency f_T

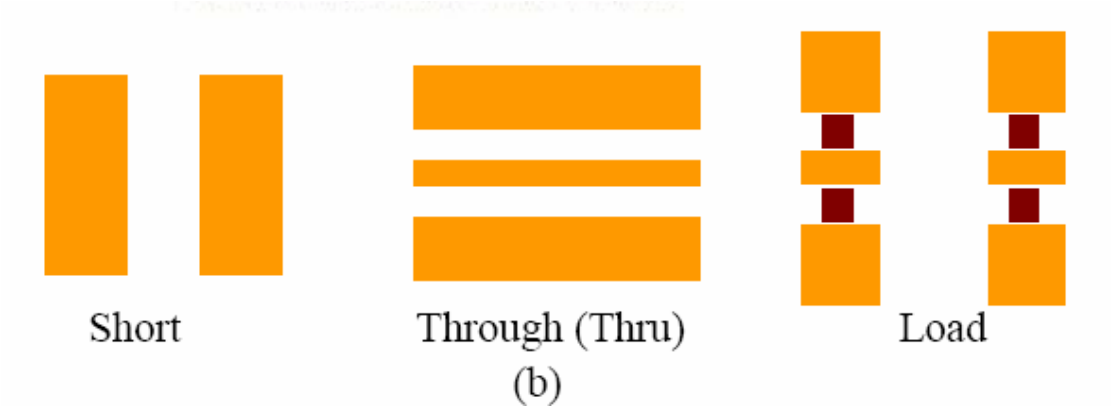
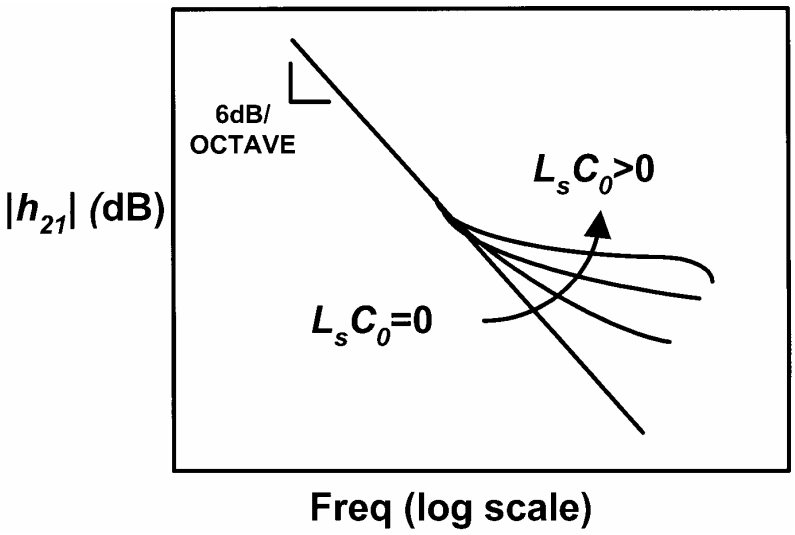


Fig. 3.9 Short, through and loads for the calibration

(-20dB/decade = -6dB/octave)

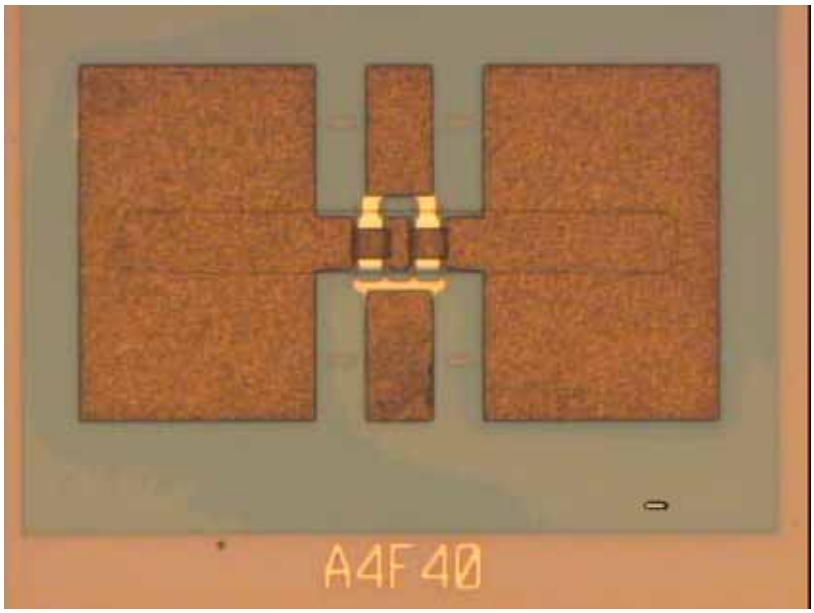


L_s: parasitic serious inductance
C_O: C_{DS} (principally),
C_{gs}, C_{gd} ⇒ affect f_T

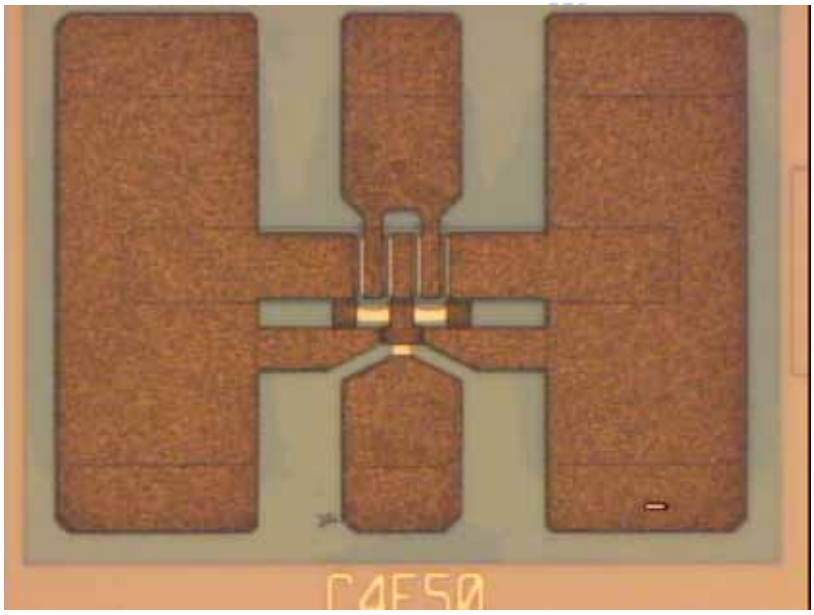
Reduce the Effect:
1. Make the Pads as small as possible.
2, De-embed the Pads and interconnects.

Reference: Scott A. Waternberg, IEEE Transactions on Microwave theory and Techniques, April 2003. (RF Micro Devices, USA)

Fig. 3.10 Effect of Pad Parasitics on h21 & f_T

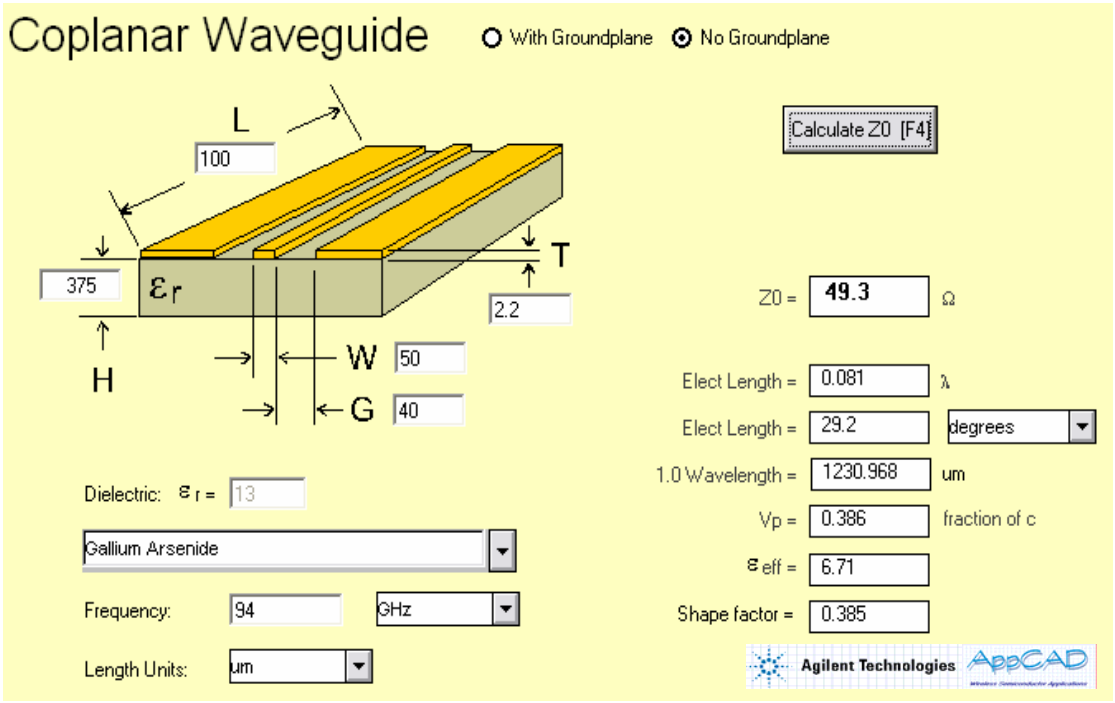


(a) A-type device

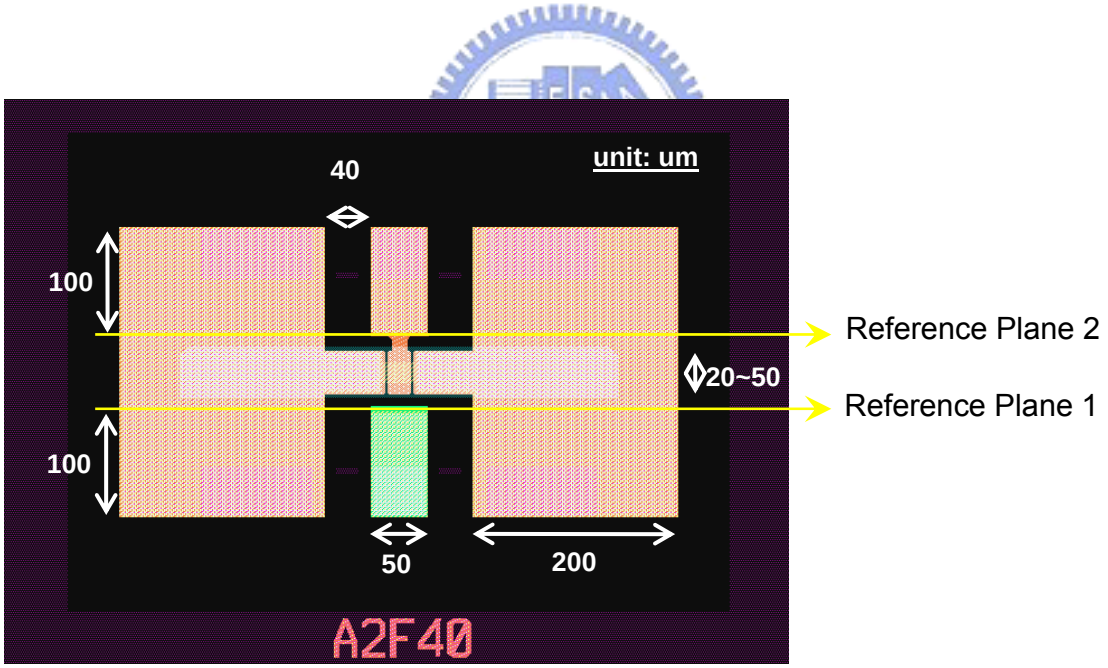


(b) C-type device

Fig. 3.11 (a) Top-views of the A-type layout, and (b) C-type device layout



(a)



(b)

Fig. 3.12(a) coplanar waveguide structure designed at 94 GHz for the A-type layout using software, and (b) final designed A-type layout using the result of the simulation.

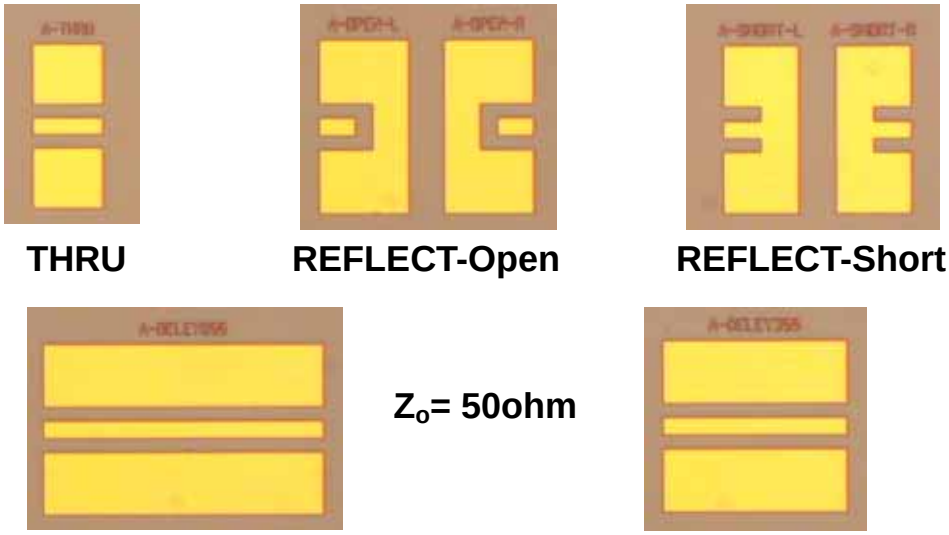


Fig. 3.13 On-wafer TRL standards (Metal patterns on substrate) for A-type layout

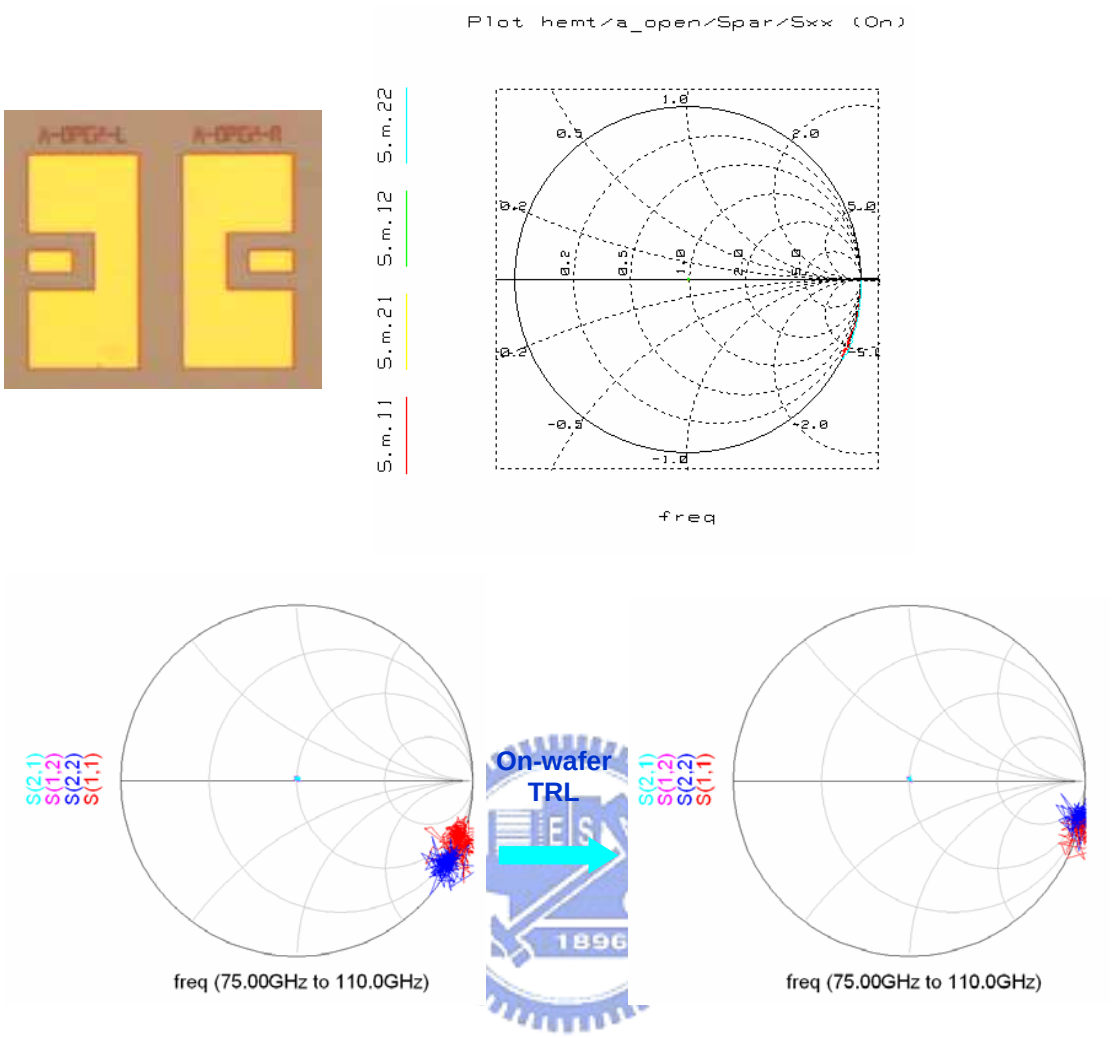


Fig. 3.14 Measured S-parameters of REFLECT-Open

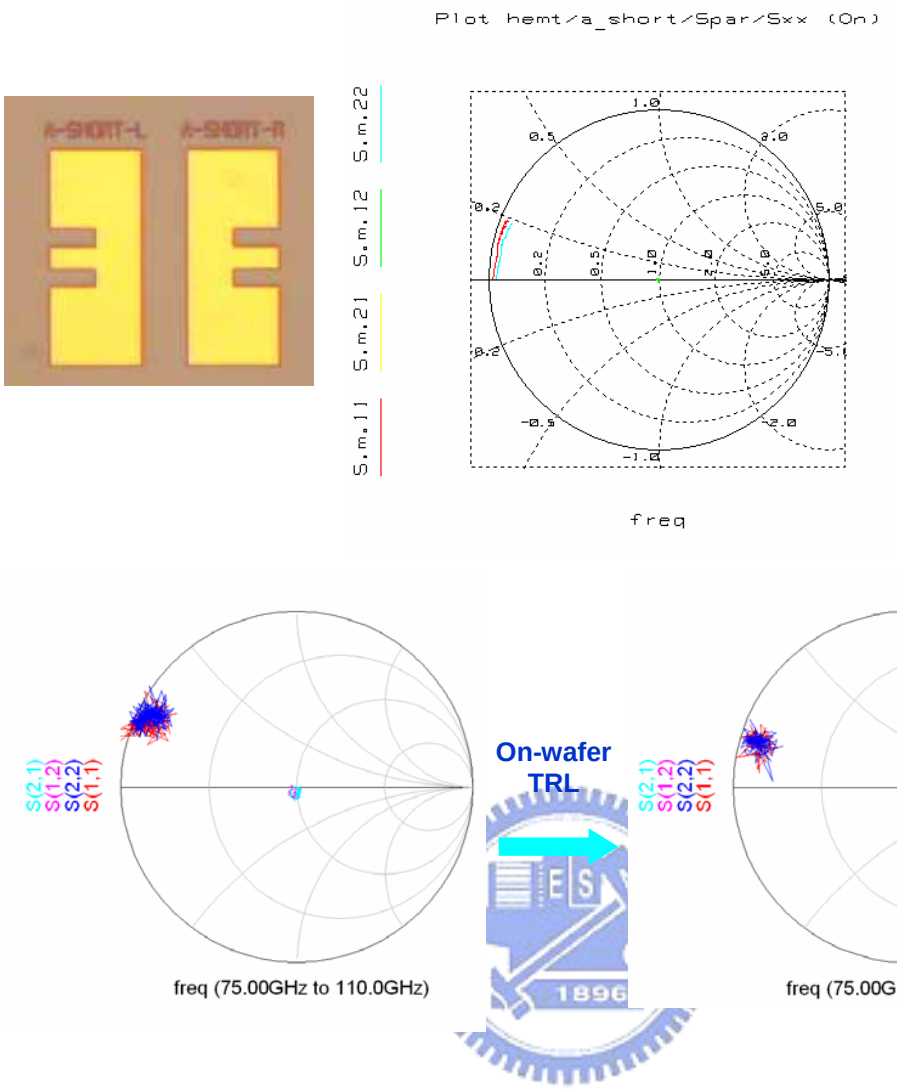


Fig. 3.15 Measured S-parameters of REFLECT-Short

$$Tdelay = \frac{L}{V} = \frac{\lambda / 4\sqrt{\varepsilon_r}}{C / \sqrt{\varepsilon_r}}$$

OFFSET DELAY:
600um/Vp= 5.1813ps

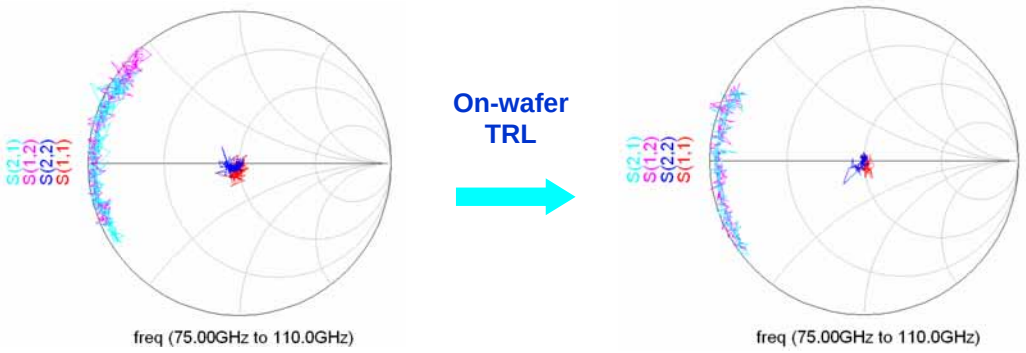


Fig. 3.16 Measured S-parameters of LINE-1: 600um

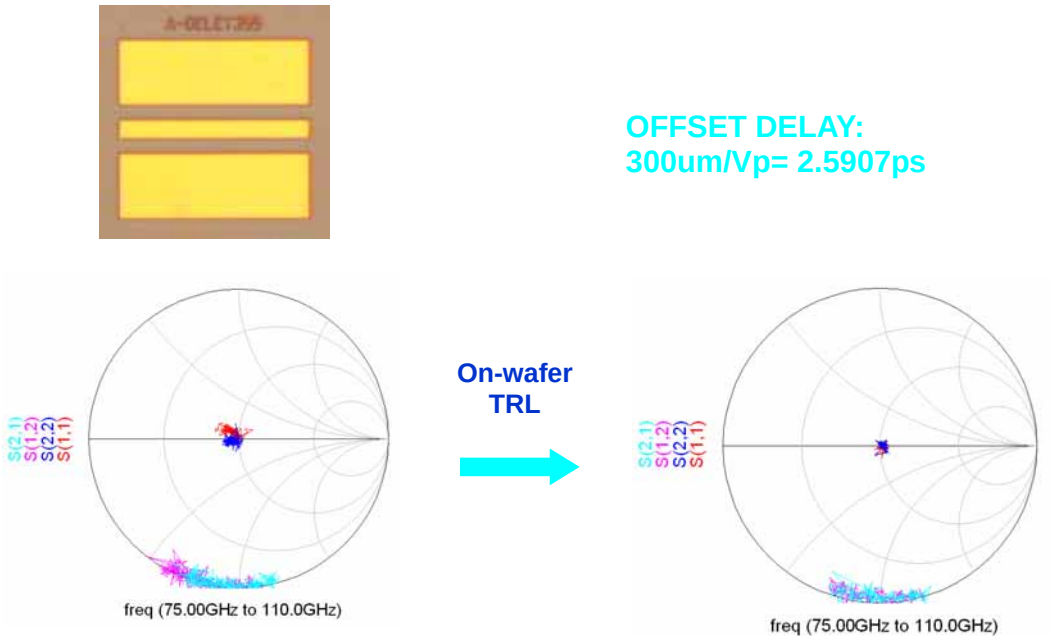
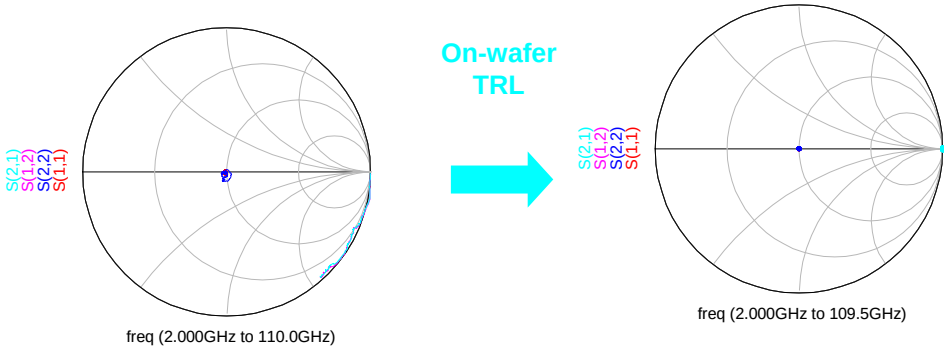
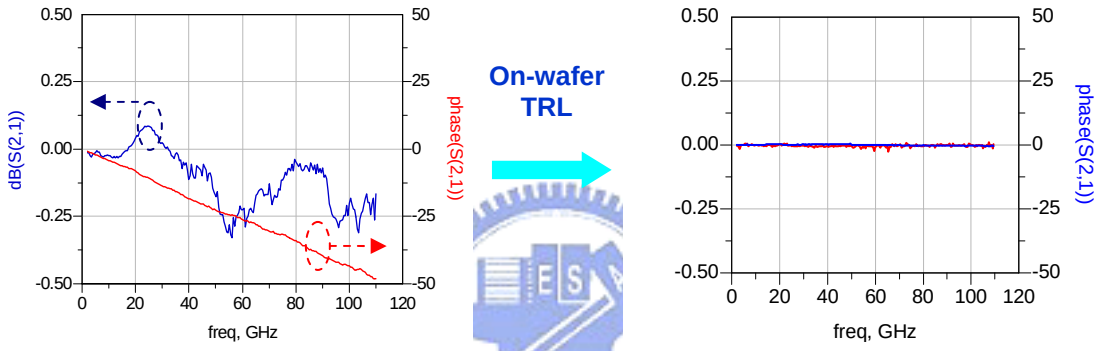


Fig. 3.17 Measured S-parameters of LINE-2: 300um



(a)



(b)

Only calibration for system.

On-wafer TRL calibration.

- S21 becomes stable value 0dB and 0 degree.
- Calibrate loss and phase. (to reference plane)
- OFFSET DELAY: 0 ps

Fig. 3.18 Check THRU after TRL Calibration, (a) the Smith chart of the S-parameter before and after TRL calibration, (b) magnitude and phase of S21

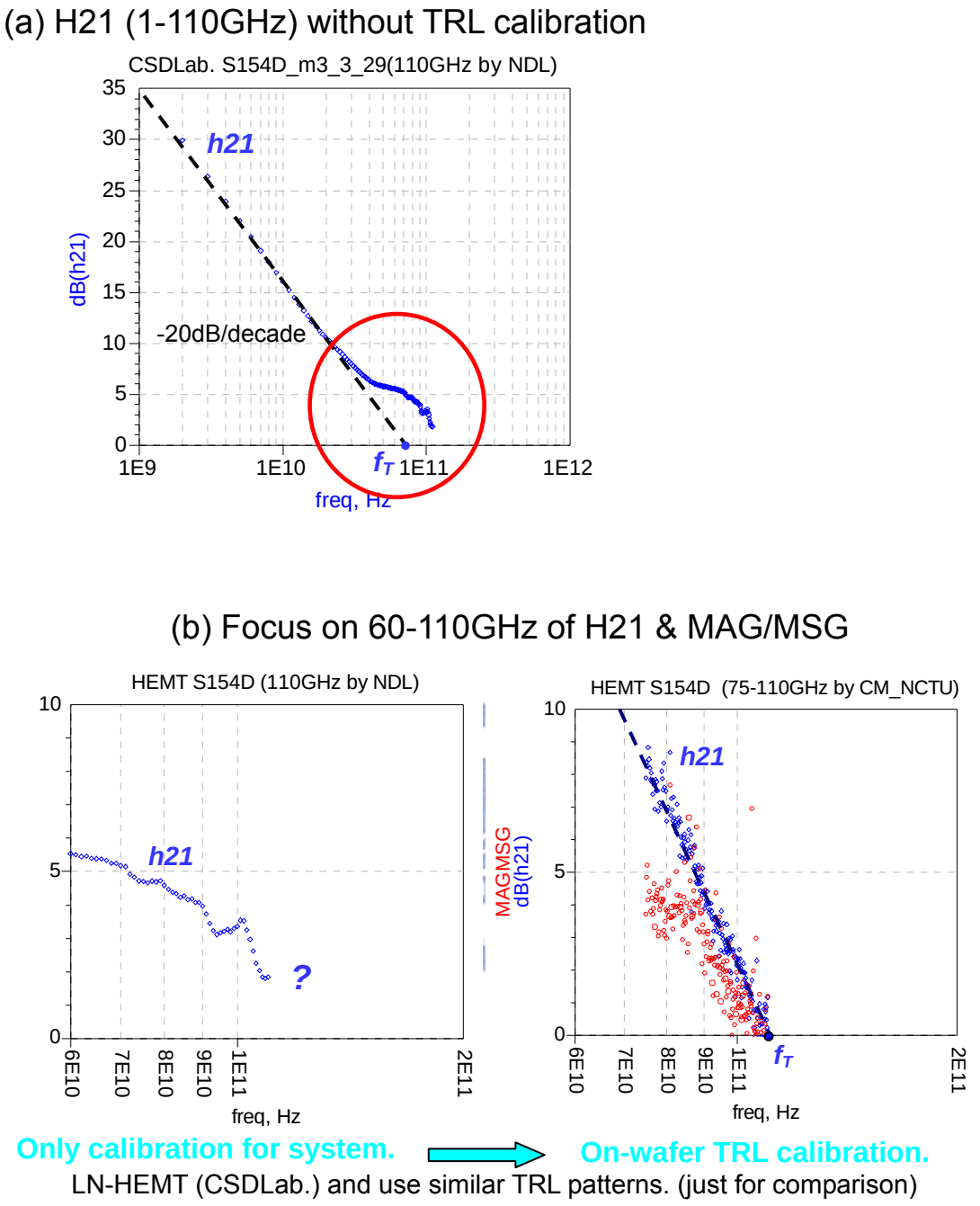


Fig. 3.19 Current gain h_{21} and MAG/MSG of MHEMT before and after TRL calibration, (a) H21 (1-110GHz) without TRL calibration, (b) Focus on 60-110GHz of H21 & MAG/MSG before and after on-wafer TRL calibration.

Chapter 4

0.15-μm Γ-Shaped Gate $In_{0.52}Al_{0.48}As$/ $In_{0.6}Ga_{0.4}As$ Metamorphic HEMTs Using DUV Lithography and Tilt Dry-Etching Technique

4.1 Introduction

For high-speed wireless communications, metamorphic high electron mobility transistors (MHEMTs) have received much attention recently due to its capability of combining the advantages of the high-performance InP-based structure and the low-cost, high mechanical strength GaAs substrate. MHEMTs with excellent high-frequency performance comparable to the InP-based HEMTs have also been demonstrated [4-1, 4-2]. MHEMTs have been considered as a cost-effective alternative to the conventional lattice-matched or pseudomorphic InAlAs/InGaAs/InP HEMTs (InP-HEMTs). The gain and noise characteristics of the MHEMTs at high frequencies are strongly dependent on the gate length (L_g) and the gate resistance, therefore T-shaped or Γ-shaped gates with small footprint and wide tee-top are commonly used for HEMTs to maximize the device performance. A wide variety of lithography methods have been used for the fabrication of submicron gates with T, Γ, or Y-shapes to improve device performance [4-3]-[4-5]. Fabrications of submicron gates using angle and angled-shadow evaporation processes have been reported [4-6, 4-7]. Multilayer deep UV (DUV) photo resist process has been used to obtain 0.2 μm T-shaped gates [4-8]. A hybrid method using E-beam Lithography and reflowed resist technology to shrink the gate length down to 0.1 μm was also demonstrated [4-9]. I-line lithography combined with chemical shrinking process has shown the capability of fabricating 0.1μm-gate InP HEMTs.[4-10] However, tightly controlled process conditions, complicated process steps or expensive E-beam lithography tools are required for these processes.

For cost-effective production of submicron MHEMTs, a 0.15-μm Γ-shaped gate MHEMT technology using DUV lithography and a tilt dry-etching technique was developed and demonstrated for the first time. A selectively developed bi-layer resist trench was first formed on the substrate by taking the advantage of the different photo sensitivity between the bottom and the top resist layers. The final gate-length of the Γ-shaped gate was mainly

controlled by the top photoresist opening, the total resist thickness and the tilt angle for the anisotropic dry etching. Comparing with the previously reported gate fabrication techniques, the tilt dry-etching gate process is a relatively simple, inexpensive and flexible process for the fabrication of submicron GaAs MHEMTs and monolithic microwave integrated circuits (MMICs) for high-frequency applications.

4.2 Experimental

The MHEMT structure was grown on the (100) GaAs substrate by the molecular beam epitaxy (MBE). The structure is as following: a 15-nm pseudomorphic $In_{0.6}Ga_{0.4}As$ channel layer was grown on top of the InAlAs buffer layer. The top and bottom Si-δ-doping layers were separated from the channel layer by the upper and lower 4-nm-thick undoped $In_{0.52}Al_{0.48}As$ spacers, respectively. The $In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As$ hetero-interfaces provide higher electron mobility and better carrier confinement in the quantum well region. The Schottky layer was 15-nm-thick undoped $In_{0.52}Al_{0.48}As$. The 15-nm-thick Si-doped $In_{0.52}Ga_{0.48}As$ cap (2×10^{18} cm^{-3}) layer was finally grown on the top for ohmic formation.

For the device fabrication, the mesa isolation was done by wet chemical etch, the ohmic contacts were formed by evaporating Au/Ge/Ni/Au on the n-InGaAs cap layer and then alloyed at 300℃ for 20sec to achieve a low contact resistance of 0.05 Ωmm. After ohmic contact formation, the gate process followed. The process for fabricating the 0.15-μm Γ-shaped gate using DUV lithography and tilt dry-etching in this study is illustrated in Fig. 4.1. The bi-layer resists consisting of the bottom 150 nm polymethyl methacrylate (PMMA) and the top 600 nm polymethyl methacrylate-methacrylic acid (P(MMA-MAA)) were coated on the substrate sequentially. In Fig. 4.1(a), the opening of 0.55 μm on the top layer was defined by DUV (λ= 254 nm) exposure for 3 minutes using a contact aligner with high-intensity DUV light source. The exposure dose (1600mJ/cm^2) was carefully adjusted so that only the P(MMA-MAA) resist layer was opened after the DUV exposure and development. The selective development for the photoresist was realized easily due to the high sensitivity ratio of P(MMA-MAA) to PMMA (~5:1). In Fig. 4.1(b), the undercut profile of the P(MMA-MAA) trench was due to the surface rate retardation during development, which can enhance the gate metal lift-off process. After the development, the wafer was tilted at an angle and was etched using inductive coupled plasma (ICP) ion etching with SF_6/Ar

etching gases. The dry etching condition in this study was carefully tuned to minimize the surface damage. The low RF power of 50 watt was applied to both the ICP source and the chuck to minimize the etch-induced damage for the underlying InGaAs layer. A set of tilt angles (θ), 0°, 15°, and 32°, was chosen to obtain the desired feature size in the bottom PMMA layer (Fig. 4.1(c)). Another advantage of using bi-layer resist structure is the high etching selectivity between the top and bottom resist layers (about 3:1). During the tilt dry-etching process, the part of the underlying PMMA layer which was not shielded by P(MMA-MAA) layer was etched to form the small footprint of the gate. The optimum gas ratio, SF_6: Ar = 1:1, was used to achieve highly anisotropic etching, and the etch rate of PMMA was 160 nm/min.

After the tilt dry-etching process, gate recess was performed using succinic acid/H_2O_2/NH_4OH solution. After gate recess, Ti/Pt/Au (80/80/200nm) gate metal was deposited. Lift-off process was performed after gate metal deposition to form the 0.15-μm Γ-shaped gate (Fig. 4.1(d)). The cross-sectional scanning electron microscopy (SEM) images of the 0.15-μm Γ-shaped gate and the resist profile just after 32° tilt dry-etching process are shown in Fig. 4.2(a) and Fig. 4.2(b), respectively. After the dry-etching process, the observed angle of the P(MMA-MAA) undercut profile is 100° as shown in Fig. 4.2(b). Finally, 60-nm-thick SiN_x was deposited by plasma enhanced chemical vapor deposition (PECVD) as the passivation layer.

4.3 Results and Discussion

Fig. 4.3 shows the critical dimension (C.D.) of the measured gate length (L_g) as a function of the tangent of the tilt angle during the dry-etching process. The statistic data of the average gate length (L_g) and the standard deviation (σ) were estimated from 10 samples on each test wafer by using SEM observation. The data are shown in the insert Table in Fig. 4.3. As can be seen in the figure, L_g was decreased by increasing the dry-etching tilt angle θ. A line of the predicted ideal gate length ($L_{gi} = L_o - h \times tan\ \theta$) was also plotted in the same figure for comparison. L_o is the initial opening of the top P(MMA-MAA) layer, which is 0.55 μm, and the total resist thickness h, as indicated in Fig. 4.1(b), is 0.75 μm in this study. The ideal gate length (L_{gi}) decreased linearly with the tangent of the tilt dry-etching angle. As shown in Fig. 4.3, there is a difference (ΔL) between the ideal gate length (L_{gi}) and the

measured gate length (L_g). ΔL increased with increasing tilt angle which is due to the etching of the side wall of the resist trench when tilt angle is applied. ΔL is about 0.06 μm when the tilted angle is 32°, as shown in Fig. 3.3. The maximum allowed tilt angle is about $\tan^{-1}(L_o/h)$ = 36°. Therefore, the L_g can be controlled from 0.55 μm down to 0.15 μm or shorter by simply varying the tilt angle θ. When the tilt angle θ was increased to 32°, gate length L_g of 0.15 μm was achieved. This condition was applied for the submicron MHEMT fabrication in this study. From the atomic force microscopy (AFM) analysis, the surface morphologies of the samples with- and without plasma treatment showed average surface roughness (RA) of the InGaAs layers of 2.4 nm and 1.4 nm, respectively. In addition, the 150-nm-thick InGaAs cap layer exposed to the plasma was removed by the wet gate recess process after the tilt dry etching. Therefore, the etch-induced damages had little influence on the device performance. This can be clearly seen from the electrical measurement data.

The drain-souce current (I_{ds}) vs. drain–source voltage (V_{ds}) curves and transconductance (g_m) vs. gate–source voltage (V_{gs}) curves of the 0.15 μm Γ-shaped gate MHEMT fabricated using the DUV lithography and tilt dry-etching technique are shown in Fig. 4.4(a) and Fig. 4.4(b), respectively. The 2 × 50-μm-wide device exhibited a good pinch-off characteristics and the saturation I_{dss} was 680 mA/mm. The maximum g_m of the device at V_{ds} of 1.5 V was 728 mS/mm and the pinchoff voltage was -1.3 V. In Fig. 4.4(c), the gate-drain breakdown voltage (V_{BR}) of the MHEMT using tilt dry-etching method was 7.5 V (defined at gate-drain current of 1mA/mm) which is the same as the device manufactured with conventional E-beam T-gate. Based on the above AFM data and the Schottky gate breakdown characteristics of the device, the etch-induced damages were minimized in this study. The *S*-parameters for the MHEMT devices were measured from 2 to 65 GHz by HP8510XF Vector Network Analyzer using on-wafer 100-μm-pitch GSG probes from Cascade MicroTech. Fig. 4.5 shows the input impedance (Z_{in}) vs. frequency from 1 to 40 GHz extracted from one-port forward-bias *S*-parameter measurement. The average Z_{in} of three samples was 8.27Ω, which could be seemed as the gate resistance (R_g) of the device.

Fig. 4.6 shows the frequency dependence of the current gain H_{21}, power gain *MAG/MSG*, and unilateral gain *U* of the 0.15 μm Γ-shaped gate MHEMT measured at V_{ds} = 1.5 V and V_{gs} = -0.7 V. The H_{21} was 7.5 dB and the MAG/MSG was 8.1 dB at 60 GHz, respectively. The current gain cut-off frequency f_T and the maximum oscillation frequency f_{max} obtained for the 2 × 50 μm MHEMT were 130 GHz and 180 GHz, respectively. The f_T of the 0.15 μm Γ-gate MHEMT in this study is comparable to that of the devices reported by other

groups with same gate length [4-11, 4-12] and the device fabricated by E-beam lithography in our previous work [4-9]. The excellent DC and RF performances of the devices demonstrate that the developed tilt dry-etching gate technology is a promising alternative to the conventional gate fabrication technology using E-beam direct writing or hybrid techniques.

4.4 Conclusion

A 0.15-μm Γ-shaped gate $In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As$ MHEMT fabricated on GaAs substrate using deep UV lithography and a tilt dry-etching technique is demonstrated for the first time in this work. The developed technology is simple, low-cost and flexible for the submicron Γ-shaped gate fabrication. The 100-μm-wide MHEMT with 0.15-μm Γ-shaped gate fabricated with dry-etching tilt angle of 32° shows an I_{dss} of 680 mA/mm and g_m of 728 mS/mm. The MHEMT also exhibits a f_T of 130 GHz and a f_{max} up to 180 GHz. The excellent device performance shows that the developed 0.15 μm Γ-shaped technology can practically be used for high-performance MHEMT devices and MMICs manufacturing.

FIGHRES

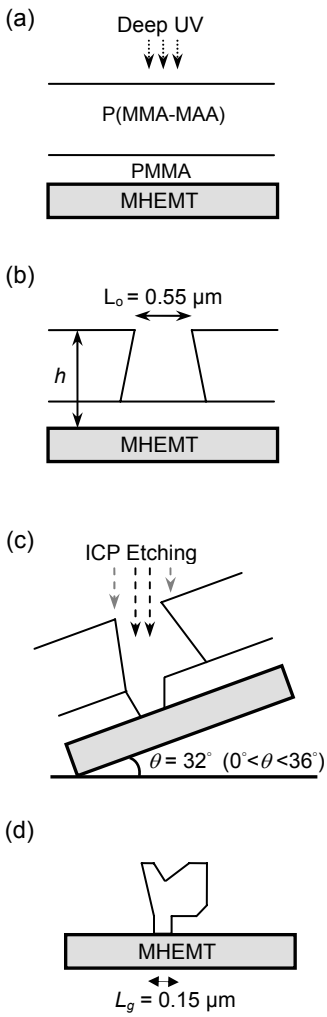


Fig. 4.1 The deep UV lithography and tilt dry-etching process steps for fabricating the submicron Γ-shaped gate MHEMT. (a) Deep UV exposure, (b) selective development of the top layer, (c) tilt dry-etching of the bottom layer, and (d) Γ-shaped gate profile after gate metal lift-off.

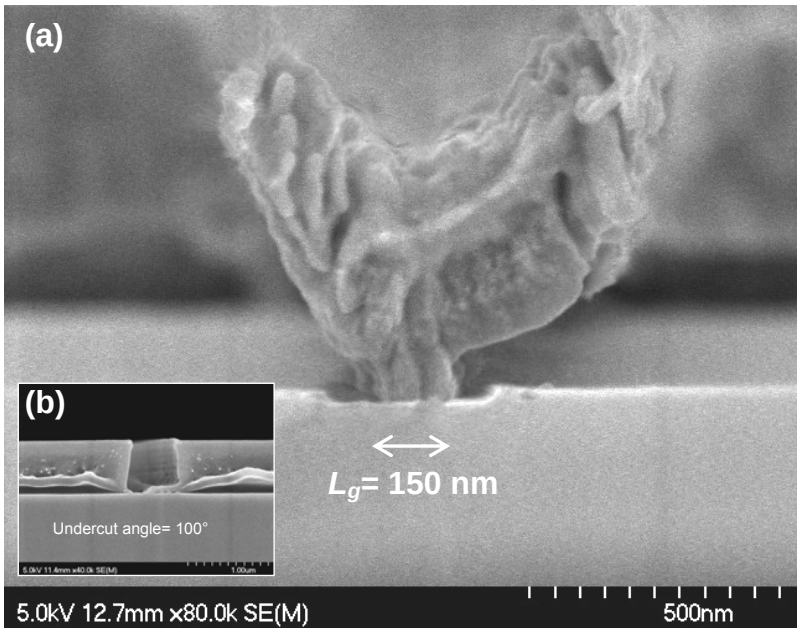
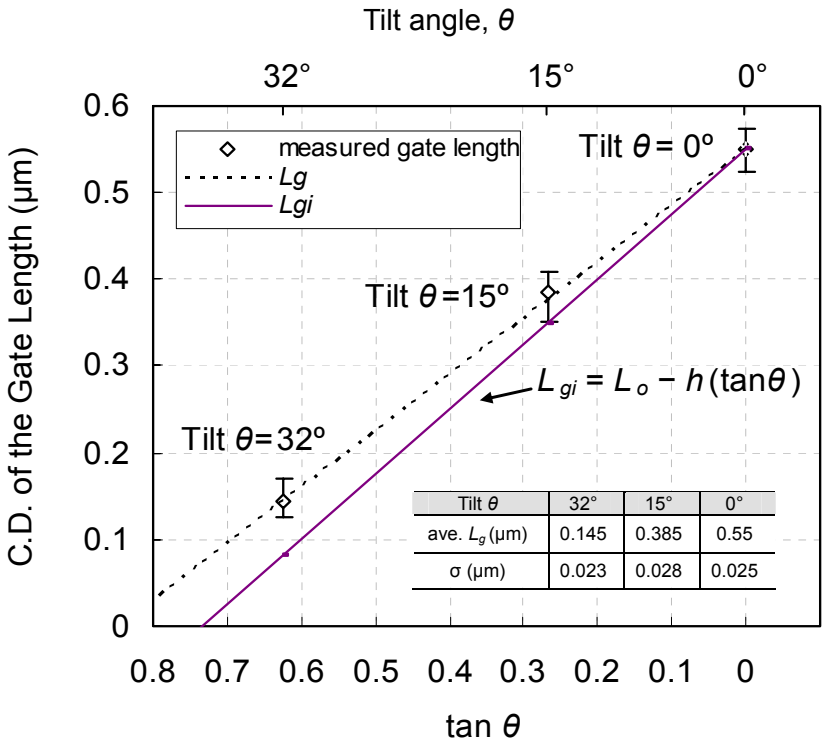


Fig. 4.2 The cross-sectional SEM images of (a) 0.15-μm Ti/Pt/Au Γ-shaped gate, and (b) resist profile after the tilt dry-etching process.



Tilt θ	32°	15°	0°
ave. L_g (μm)	0.145	0.385	0.55
σ (μm)	0.023	0.028	0.025

Fig. 4.3 Critical dimension (C.D.) of the measured gate length (L_g) and the ideal gate length (L_{gi}) as a function of the tangent of the tilt angle θ.

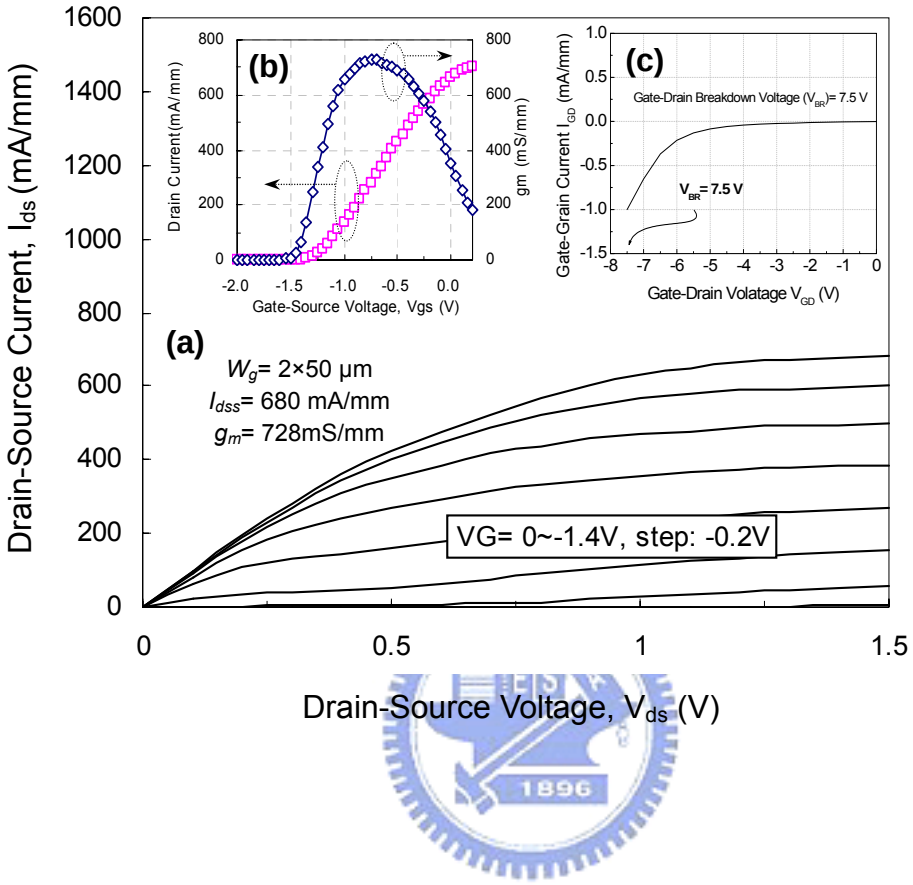


Fig. 4.4 (a) Drain-source current vs. drain–source voltage curves, (b) transconductance vs. gate–source voltage, and (c) gate-drain breakdown voltage (V_{BR}) of the 0.15 μm Γ-shaped gate MHEMT.

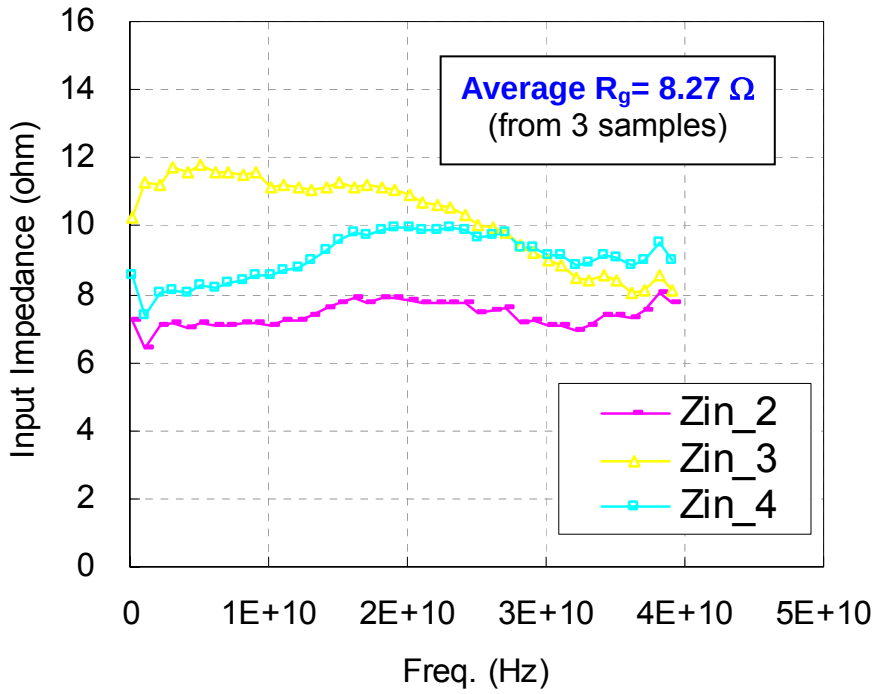


Fig. 4.5 Input impedance (Z_{in}) vs. frequency from 1 to 40 GHz extracted from one-port forward-bias *S*-parameter measurement

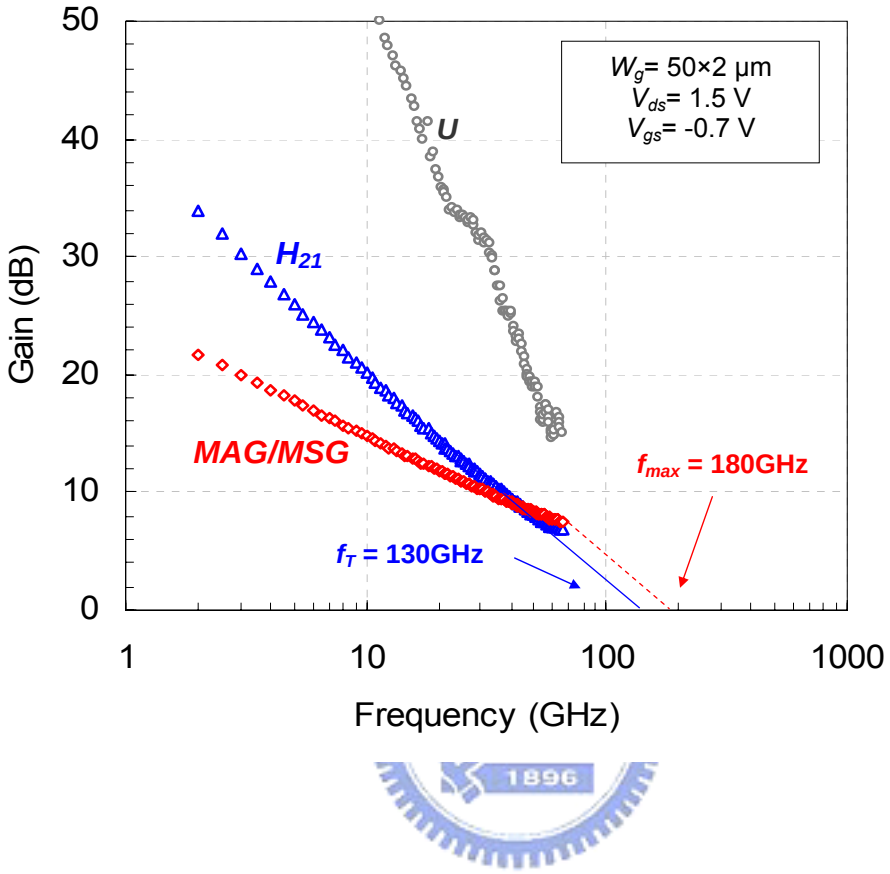


Fig. 4.6 Frequency dependence of the current gain H_{21}, power gain *MAG/MSG*, and unilateral gain U of the 0.15 μm Γ-shaped gate MHEMT. Frequency range was from 2 GHz to 65 GHz and device was biased at V_{ds}= 1.5 V and V_{gs}= -0.7 V.

Chapter 5

Low Noise Metamorphic HEMTs with Reflowed 0.1 μm T-Gate

5.1 Introduction

For the high-frequency wireless applications, metamorphic HEMTs (MHEMTs) using an $In_xAl_{1-x}As/In_xGa_{1-x}As$ heterostructure grown on GaAs substrate [5-1,5-2] constitutes a good alternative to pseudomorphic AlGaAs/InGaAs/GaAs HEMTs (PHEMTs) and to lattice matched InAlAs/InGaAs/InP HEMTs (InP-HEMTs). For the MHEMT devices, a strain relaxed, compositionally graded metamorphic buffer layer is used to accommodate the large lattice mismatch between the top layers and the substrate. The MHEMT has received much attention recently due to its capability to combine the advantage of the InP-based structure and the GaAs substrate and has demonstrated excellent electrical performance for high frequency applications [5-3, 5-4]. In order to achieve superior RF performance for high frequency applications, short gate length is required for the compound semiconductor field effect transistors. The gain and noise characteristics of the MHEMTs at high frequency are strongly dependent on the gate length (*Lg*) and the gate resistance values. T-shaped gates are generally used for the HEMTs to maximize the device performance.

Different lithography methods have been developed for the submicron T-gates in recent years [5-5, 5-6]. For example, multilayer photo resist processes have been used to obtain submicron T-shaped gates [5-7]. In order to further improve device performance, dielectric deposition process with etching back technology have been widely used to form dielectric sidewall and shrink the *Lg* that is originally limited by the lithography resolution [5-8]. However, tightly controlled process and relatively complicated steps with long process time are required for these processes.

The thermally reflowed resist process is another approach for gate shrinkage and has previous been reported [5-9, 5-10]. However, thermally reflow of E-Beam photo resist to achieve sub-0.1 um T-gate for MHEMT application has never been reported. In this study, resist profile for 0.1 μm T-shaped gate was achieved by thermally

reflowing the bi-layer E-beam resist using hotplate and the 0.1 μm T-shaped gate was achieved by the standard lift off process and was applied to the MHEMT manufacture. Comparing with 2 step lithography of hybrid T-shaped gate [5-11] and Y-shaped gate [5-12], the reflowed gate process is a much simpler, relatively inexpensive and flexible process. Additionally, it is also free of plasma damage and is compatible with the MHEMT process for high frequency application.

5.2 Process Flow

The $In_{0.53}Al_{0.47}As/In_{0.53}Ga_{0.47}As$ MHEMT uses $In_xAl_{1-x}As$ as the buffer layer between the GaAs substrate and the InP lattice-matched HEMT structure and was grown by the molecular beam epitaxy (MBE) method on the 3 inch diameter GaAs substrate. The sequence for the device fabrication is as follows. The mesas were isolated by wet chemical etch and the ohmic contacts were formed by evaporating Au/Ge/Ni/Au on heavily doped InGaAs layer and then alloyed at 320^{o}C using RTA (Rapid Thermal Annealing). The contact resistance as measured by the transmission line model (TLM) method was 0.04 Ω mm. For the reflowed T-gate process, the bi-layer resist which consist of polymethylmethacrylate PMMA and polymethyl methacrylate-methacrylic acid P(MMA-MAA) was exposed first by E-beam lithography (Leica EBML300) with opening of 0.25 μm and then went through thermally reflow treatment at 115^{o}C on a hotplate for 60 sec to reduce the opening to 0.1 μm. The lift-off profile was obtained due to the bottom resist PMMA was successfully shrunk to form the desired footprint opening of 0.1 μm without any obvious change on the top P(MMA-MAA) layer after thermal treatment. In addition, the reflow condition was optimized after testing different temperatures (from 105 to 135 ^{o}C, per step= 10 ^{o}C) and time (20, 40, 60, and 80 sec). The detailed process optimization has been published in [10]. Although the reflowed temperature over 125 ^{o}C will obtain shorter gate length, there is a risk of footprint opening being closed by high temperature and long time reflow. Therefore the optimized reflow condition of 115 ^{o}C for 60 sec was decided. In order to verify the reflow effect, MHEMTs with non-reflowed T-gate were also fabricated. Fig. 5.1 illustrates the cross sections of the two types of T-gate profiles. Fig. 5.1(a) is the E-Beam resist after exposure and its 0.25 μm T-gate after lift-off. Fig. 5.1(b) is the resist after thermal reflow and its 0.1

μm T-gate after lift-off. As shown in Fig. 5.1(b), the E-beam resist profile after thermal reflow was very ideal for lift-off and T-gate formation.

After gate lithography process, gate recess was performed using succinic-base solution and Ti/Pt/Au (100/100/300 nm) were deposited as the Schottky gate metal and lift-off process was performed to form the T-shaped gate. As shown in Fig. 5.1, the recess width on the devices was about 0.13 μm for both with and without reflow samples. After T-gate formation, 100-nm-thick silicon nitride film was deposited by PECVD as the passivation layer. Finally, the airbridges were formed with 2 μm of plated Au.

5.3 Device performance

The drain current and transconductance (gm) vs. gate bias of the 0.1 × 160 μm^2 MHEMT fabricated using the thermally reflowed T-gate are shown in Fig. 5.2. The device exhibits a good pinch-off characteristics and the saturation drain current (I_{DSS}) is 200 mA/mm. The transconductance of the device at 1.2 V drain-source voltage (*Vds*) is 750 mS/mm and the pinchoff voltage is -500 mV. The gate to drain breakdown voltage measured was 10 V at a gate reverse current of -1 mA/mm. The high breakdown voltage is due to lower *Idss* target caused by longer recess. The *S* parameters for the MHEMT devices were measured from 1 to 40GHz and current gain H_{21}, *MAG/MSG*, and unilateral gain *U* as a function of frequency are shown in Fig. 5.3. The f_T and f_{max} obtained for the 0.1 × 160 μm^2 MHEMT were 154 GHz and 300 GHz, respectively. In addition, the measurement of the noise figure (*NF*) and associated gain (*Ga*) have been performed in the frequency range between 2 and 18 GHz and the results are shown in Fig. 5.4. The *NF* is less than 1 dB up to 18 GHz with associated gain of 14dB at 18 GHz.

Table 5.1 summarizes the measured electrical performance of the 0.1 × 160 μm^2 MHEMT and the performance was compared with the performance of the non-reflowed 0.25 × 160 μm^2 MHEMT. Although the transconductance of the MHEMT with reflowed T-gate increased only slightly, the f_T and f_{max} were improved substantially from 105 to 154 GHz and from 180 to 300 GHz respectively. However, the increase in transconductance is less pronounced (from 700 mS/mm to 750 mS/mm). In other words, carriers are at their saturation velocity when current

saturates and this is evident by the fact that the knee voltage at *Idss* is less than the pinch-off voltage in the I-V curve. Thus, the transconductance has less dependence on gate length and the increase in cutoff frequency mainly comes from *Cgs*. The improved RF performance was due to the T-gate shrinkage from 0.25 μm to 0.1 μm after the thermal reflow process.

5.4 Conclusion

A thermal reflow process for E-beam bi-layer resist to achieve 0.1μm T-gate formation was successful developed and applied to the MHEMT fabrication. The 0.1 × 160 μm^2 MHEMT fabricated demonstrated a cut-off frequency f_T of 154 GHz and a maximum frequency f_{max} up to 300GHz, the noise figure of the fabricated MHEMT was less than 1 dB with 14 dB associated gain at 18 GHz. The excellent device performance of the 0.1 μm MHEMT manufactured demonstrated that the reflowed T-gate process is compatible with the MHEMT process and can be practically used for the MHEMT manufacturing.

FIGHRES:

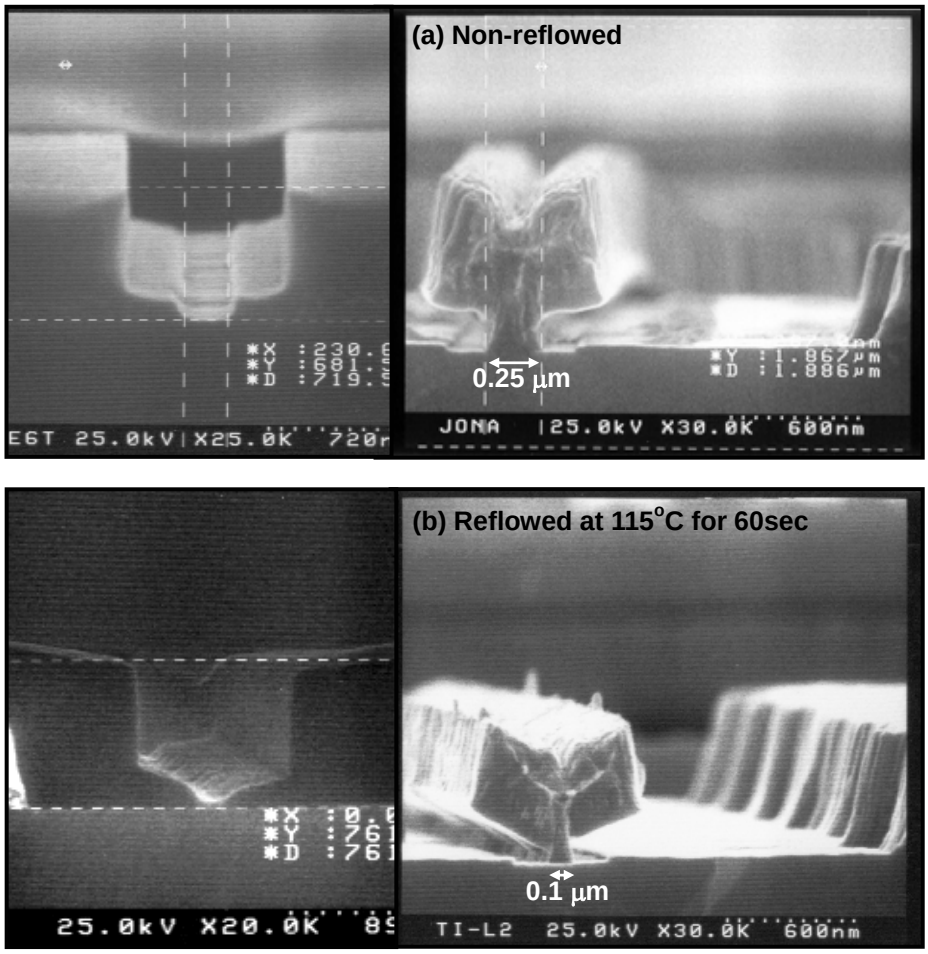


Fig. 5.1 The SEM micrograph: (a) conventional E-beam resist and its 0.25 μm T-gate. (b) the resist after shrinking by thermally reflow and its 0.1 μm T-gate.

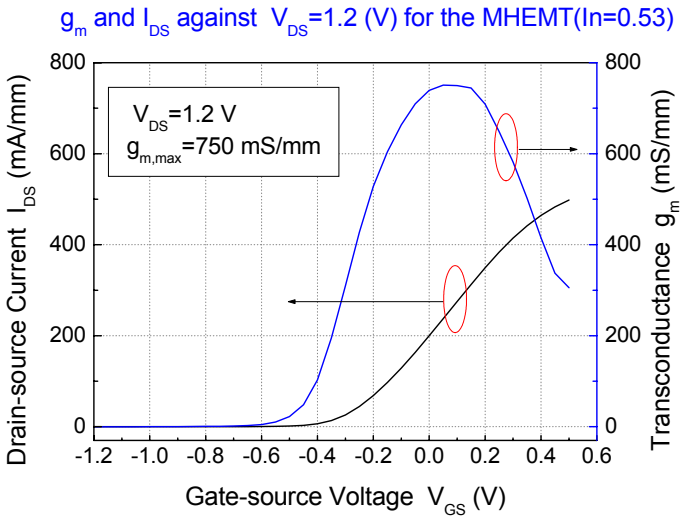


Fig. 5.2 Transconductance of the 0.1 μm × 160μm MHEMT.

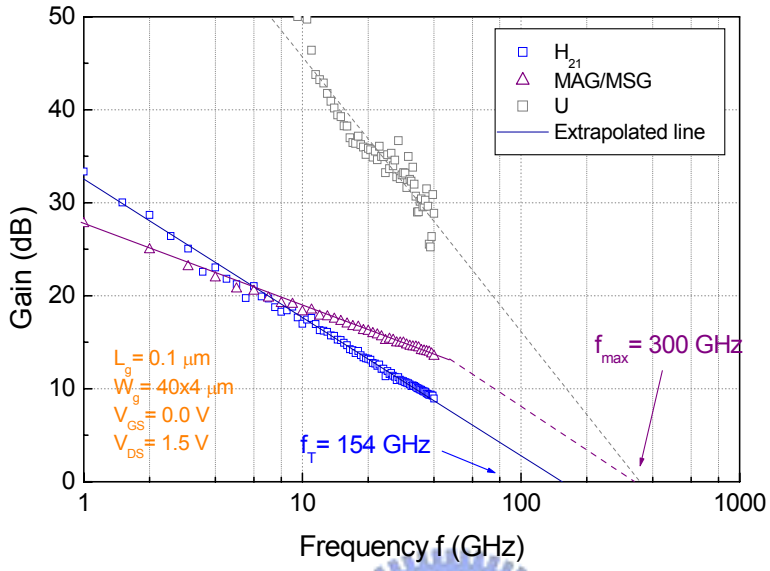


Fig. 5.3 Typical current gain H_{21}, *MAG/MSG*, and unilateral gain U as a function of frequency of the 0.1 μm × 160 μm MHEMT.

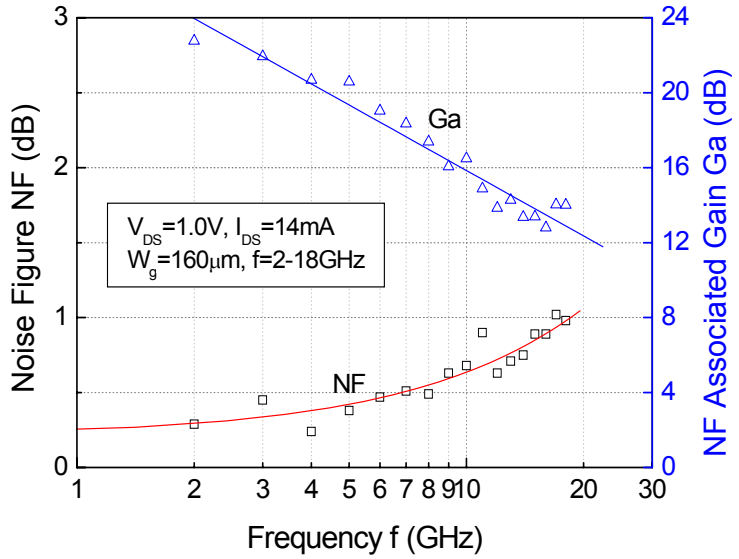


Fig. 5.4 Noise figure and associated gain as a function of frequency at V_{DS} = 1V and I_{DS} = 14 mA of the 0.1 μm × 160 μm MHEMT.

Table 5.1 Summary of device performance of the MHEMT with non-reflowed and reflowed T-Gate.

T-gate type of the MHEMT	Lg(μm)	gm(mS/mm)	V_{BR}(V)	f_T(GHz)	f_{max}(GHz)	NF@18GHz (dB)
Non-reflowed T-gate	0.25	700	8	105	180	1.18
Reflowed T-gate	0.1	750	10	154	300	0.99

Chapter 6

Characterization and Fabrication of Low Noise Metamorphic GaAs HEMTs Using 90nm Sidewall T-gate

6.1 Introduction

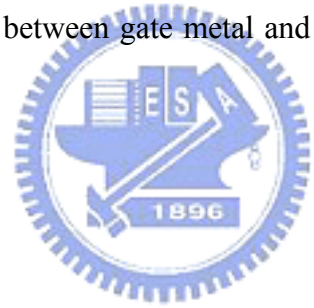
For the high-frequency wireless applications, metamorphic high electron mobility transistors (MHEMTs) using an InAlAs/InGaAs heterostructure grown on GaAs substrate constitutes a good alternative to pseudomorphic AlGaAs/InGaAs/GaAs HEMTs (PHEMTs) and to lattice matched InAlAs/InGaAs/InP HEMTs (InP-HEMTs) [6-1, 6-2]. Although the InP-HEMTs have demonstrate the best RF and noise performance, the advantages of the MHEMTs grown on GaAs substrates are not so expensive, easy to handle and have more mature processing technology. In order to achieve superior RF performance, short gate length is required for the compound semiconductor field effect transistors [6-3]. The gain and noise characteristics of the MHEMTs at high frequency are strongly dependent on the gate length (L_g) and the gate resistance values. Different lithography methods have been developed for the submicron T-gates in recent years [6-4]. In this study, the $In_{0.52}Al_{0.48}As/In_{0.52}Ga_{0.48}As$ MHEMTs using 90nm sidewall T-gate process is successfully and applied to the fabrication for high frequency application. In addition, the equivalent circuit parameters (ECPs) of the small-signal model for the MHEMT has also been extracted and discussed.

6.2 Experimental

The $In_{0.52}Al_{0.48}As/In_{0.52}Ga_{0.48}As$ MHEMT uses $In_xAl_{1-x}As$ as the buffer layer between the GaAs substrate and the InP lattice-matched HEMT structure and was grown by the molecular beam epitaxy (MBE) on the 3 inch diameter GaAs substrate. The mesas were isolated by wet chemical etch and the ohmic contacts were formed by

evaporating Au-Ge-Ni on InGaAs layer and then alloyed to obtain the contact resistance of 0.06 mm. For the sidewall T-gate process, after the 100nm-thick SiN_x deposited by plasma enhanced chemical vapor deposition (PECVD), the initial opening was defined using polymethylmethacrylate (PMMA) exposed by E-beam lithography and was dry-etched by reactive ion etching (RIE) using SF_6 and Ar gases. Following the 80nm SiO_2 deposition and the second dry-etching, the final foot-print opening was decided.

After the photoresist profile of the gate-top was completed, gate recess was performed using succinic acid and Ti/Pt/Au were deposited as the gate metal and lift-off process was performed to form the T-shaped gate. Then 60nm-thick SiN_x was deposited by PECVD as the passivation layer. Finally, the device layout with accomplished air bridges formed with 2 μm of plated Au as shown in Fig. 6.1(a). Fig. 6.1(b) and Fig 6.1(c) show the T-gates under the Au air-bridges. Fig. 6.1(d) and (e) illustrate the cross sections of the SiN_x/SiO_2 sidewall T-gate profile. As shown in Fig. 6.1(e), it shows good contact between gate metal and InAlAs layer, and obtained the L_g of 90nm successfully.



6.3 Results and Discussion

The drain current and transconductance (g_m) vs. gate bias of the 160 m-width MHEMT fabricated using the 90-nm sidewall T-gate are shown in Fig. 6.2. The device exhibits a good pinch-off characteristics and the saturation drain current (I_{dss}) is 620mA/mm. The maximum g_m of the device at 1.5V drain-source voltage (V_{ds}) was 930mS/mm and the pinchoff voltage was -1.1V. The gate to drain breakdown voltage measured was -9.0V at a gate reverse current of -1mA/mm. The *S*-parameters for the MHEMT were measured from 1 to 40GHz and current gain h_{21}, maximum stable/available gain (*MSG/MAG*), and unilateral gain *U* as a function of frequency are shown in Fig. 6.3. The f_T and f_{max} obtained for the 160μm-width MHEMT were 130GHz and over than 200GHz, respectively. In addition, the measurement of the noise figure (*NF*) and associated gain (*Ga*) have been performed in the frequency range between 2 and 16GHz and the results are shown in Fig. 6.4. The *NF* was 0.69dB up to 16GHz with *Ga* of 9.77dB at 16GHz.

Table 6.1 shows the extrinsic and intrinsic equivalent circuit parameters (ECPs)

of the MHEMT under the bias V_{ds} = 1.5V and V_{gs} = -0.6V. The external parasitics are determined by the characterization method [6-5]. In the Fig. 6.5, the *S*-parameters were measured up to 40GHz and compared with the *S*-parameters computed from the equivalent circuit. It shows the calculated *S*-parameters are in quite good agreement with the experimental data. The good agreement indicates that the small signal modeling is applicable up to millimeter wave range as well as for the design of both hybrid and monolithic microwave circuit.

6.4 Conclusions

A sidewall process for E-beam lithography to achieve 90nm T-gate formation was successful developed and applied to the MHEMT fabrication. The 160μm-width MHEMT exhibited a f_T of 130GHz and a f_{max} over than 200GHz, the *NF* of the fabricated MHEMT was 0.69dB with 9.77dB associated gain at 16GHz. In addition, the complete small-signal model for the MHEMT has also been constituted and studied. The excellent device performance of the 90nm-gate MHEMT manufactured demonstrated that the sidewall T-gate process is compatible with the MHEMT process and can be practically used for the MHEMT manufacturing.

FIGURES:

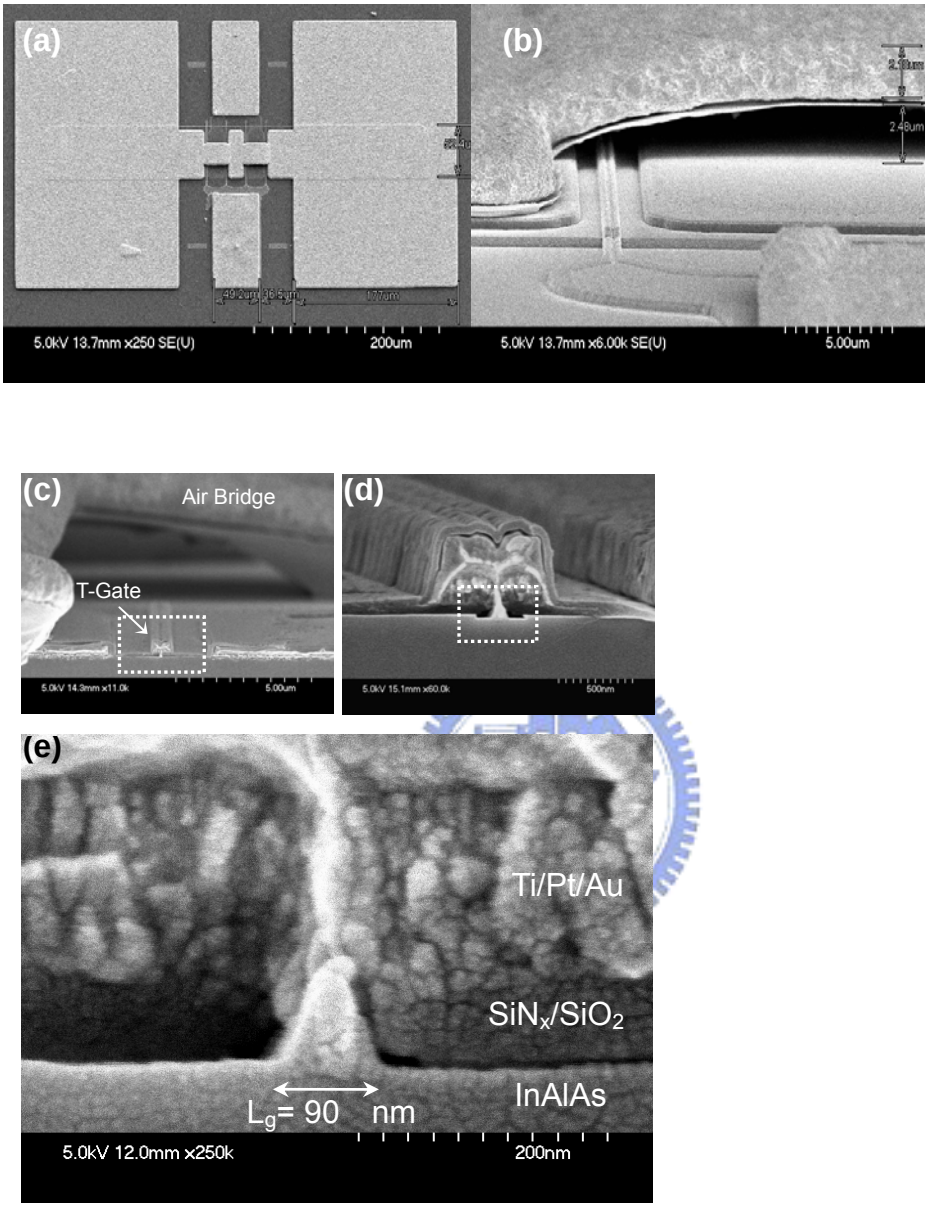


Fig. 6.1 Scanning electron microscopy images: (a) Device layout with accomplished air bridges formed with 2 μm of plated Au, (b) and (c) show the T-gates under the Au air-bridges, (e) and (f) illustrate the cross sections of the SiN_x/SiO_2 sidewall T-gate profile.

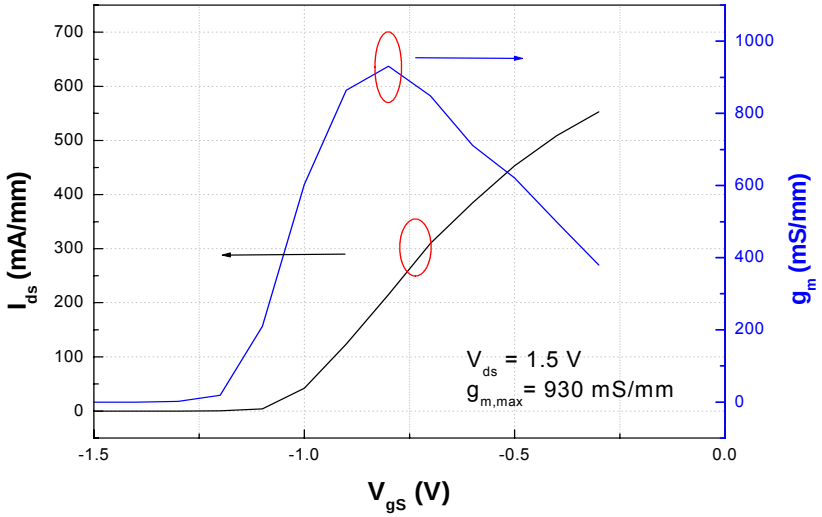


Fig. 6.2 Transconductance (g_m) of the 160μm-width MHEMT

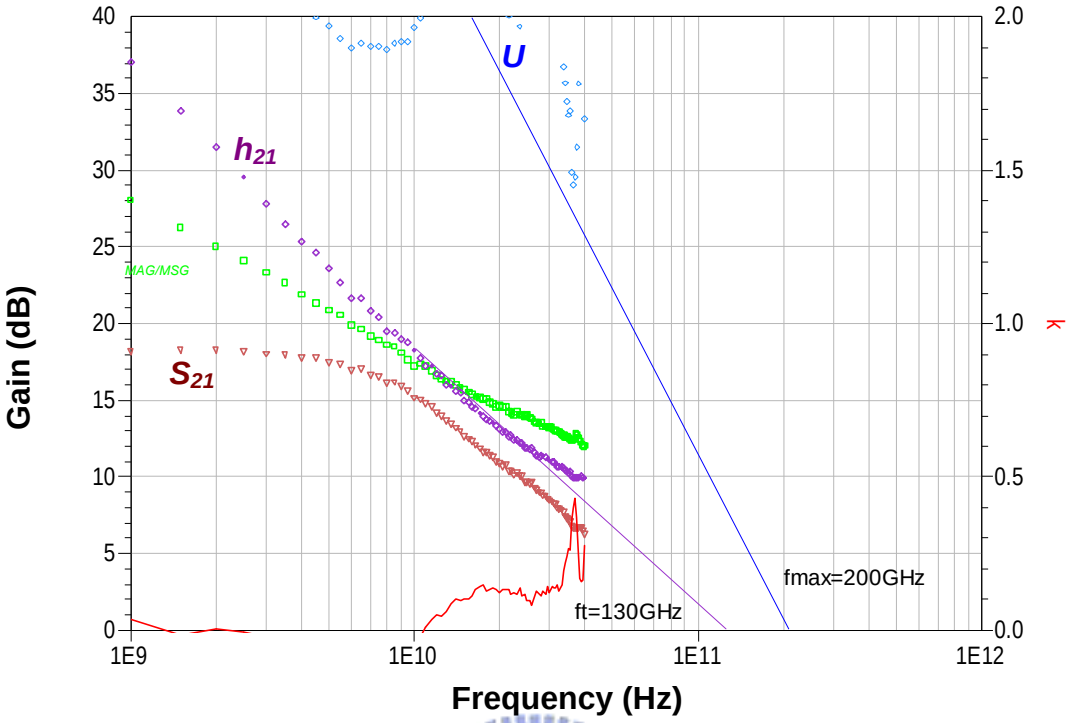


Fig. 6.3 Typical current gain h_{21}, *MAG/MSG*, and unilateral gain U as a function of frequency of the 160μm-width MHEMT

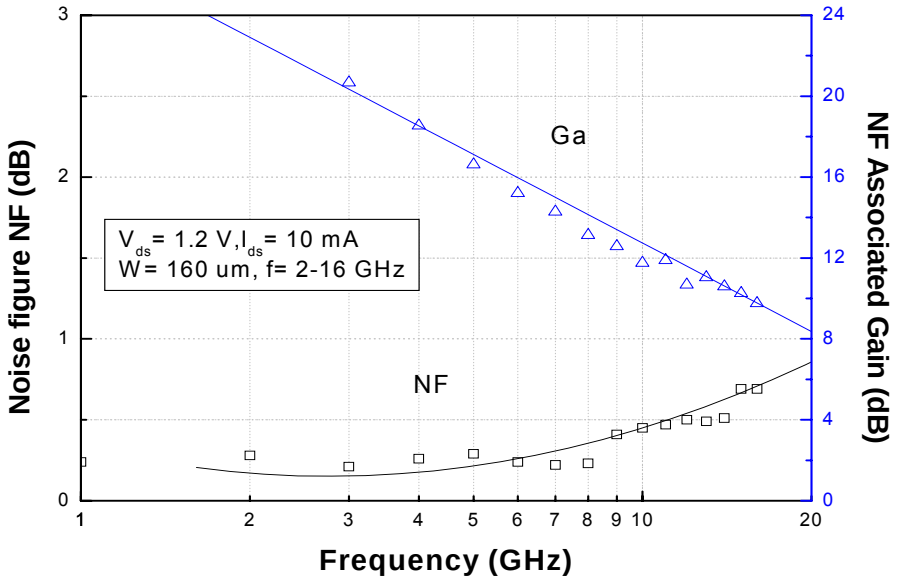


Fig. 6.4 Comparison between the calculated and measured S-parameters under V_{ds} = 1.5V and V_{gs} = -0.6V

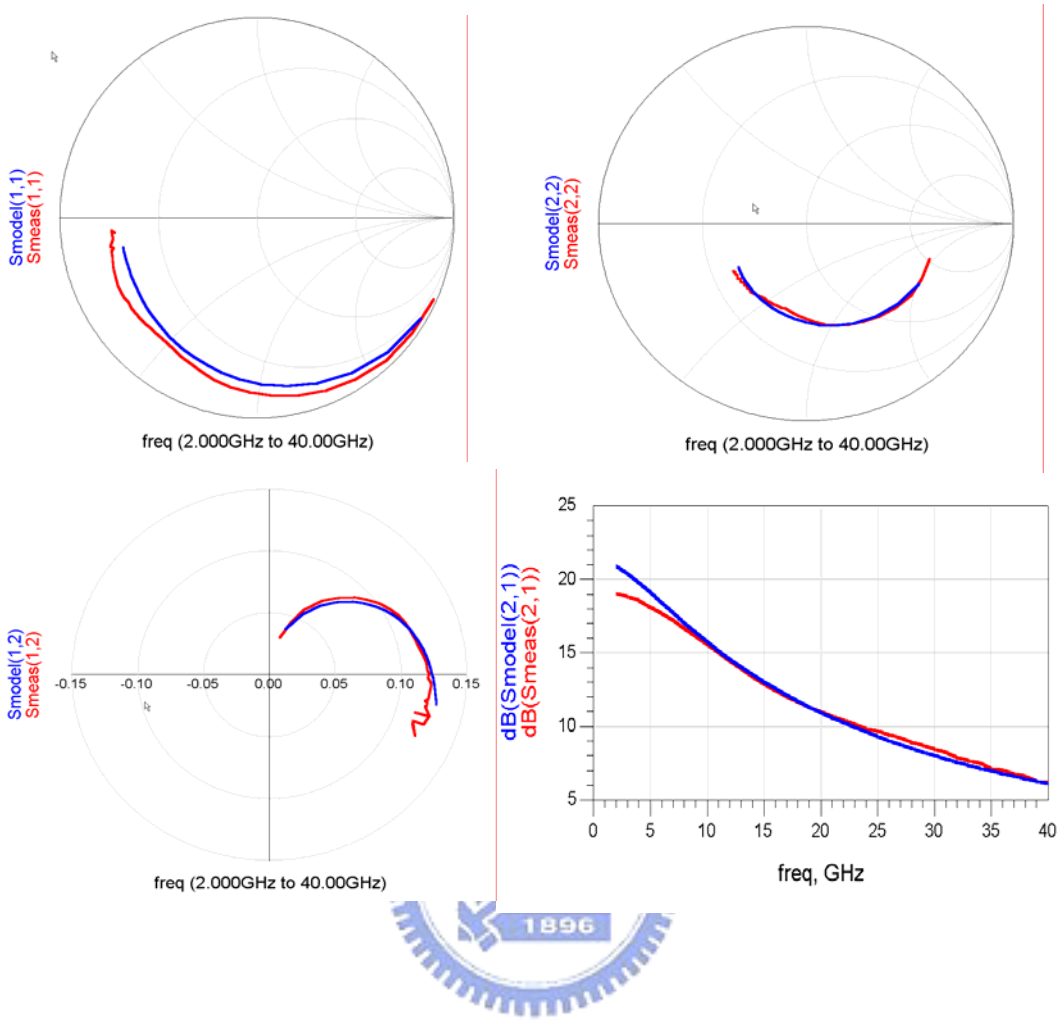


Fig. 6.5 Comparison between the calculated and measured S-parameters under V_{ds} = 1.5V and V_{gs} = -0.6V

Table 6.1 The extrinsic and intrinsic equivalent circuit parameters of the MHEMT device of 160μm of gate width

g_m (mS)	C_{gs} (fF)	C_{gd} (fF)	C_{ds} (fF)	R_i (Ω)	R_{ds} (Ω)	T (ps)
182	200	38	36	0.5	180	2.5
L_g (pH)	L_d (pH)	L_s (pH)	R_g (Ω)	R_d (Ω)	R_s (Ω)	C_{pg} (fF)	C_{pd} (fF)
43	33	2	1.5	1.5	0.83	18	14

Chapter 7

High-Performance $In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As$ Power Metamorphic HEMT for Ka-Band Applications

7.1 Introduction

For high frequency communication system applications such as communication satellites, radar, mobile millimeter-wave communication, and smart munitions, high-performance power amplifiers are required in the emission part. Due to superior low noise and power performances in the millimeter-wave range, InAlAs/InGaAs metamorphic HEMT (MHEMT) is a good alternative to pseudomorphic HEMT (PHEMT) on GaAs or lattice-matched HEMT on InP [7-1]. Although, PHEMT grown on GaAs substrate has demonstrated excellent output power density at 60 and 94 GHz in the previous work [7-2]. The power gain and power added efficiency (PAE) were limited by the low Indium content of the pseudomorphic InGaAs channel. On the contrary, InP-based HEMTs have shown excellent high frequency characteristics by reducing the gate length (L_g) to sub-100nm range [7-3, 7-4]. However, the advantages of InP-based HEMTs, such as higher electron saturation velocity, higher conduction band discontinuity and lower access resistance, also can be achieved with MHEMT that can be grown on less expensive and larger size GaAs substrate [7-5]–[7-7]. In this work, a 70-nm $In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As$ power MHEMT with double δ-doping structure was processed and evaluated. The device demonstrates excellent DC and RF performances at Ka-band and shows great potential for the millimeter-wave power applications.

7.2 Experimental

The epitaxial structure of the MHEMT was grown by molecular beam epitaxy (MBE) on 3-inch semi-insulating GaAs substrate. The structure from bottom to top

consists of an InAlAs buffer layer, a Si δ-doping layer, an $In_{0.52}Al_{0.48}As$ spacer, an $In_{0.6}Ga_{0.4}As$ channel layer, an $In_{0.52}Al_{0.48}As$ spacer, a Si δ-doping layer, an $In_{0.52}Al_{0.48}As$ barrier layer, and a Si-doped $In_{0.53}Ga_{0.47}As$ cap. The double δ-doping structure and the $In_{0.6}Ga_{0.4}As$ channel layer of the MHEMT are designed to provide higher carrier concentration and superior electron transport properties.

The mesa isolation was done by wet chemical etch. Source and drain Ohmic metals were formed with Au/Ge/Ni/Au. The T-shaped gate was carried out in the 50-KeV JEOL electron beam lithography system (E-beam) using tri-layer E-beam resist with two steps exposure. The tri-layer resist system of ZEP-520/PMGI/ZEP520 was used for the E-Beam lithography and shown in Fig. 7.1(a). The Ti/Pt/Au was evaporated as gate metal. The gate length of the T-shaped gate was 70nm as shown in Fig. 7.1(b). The detail of the nano T-gate process was described on next section (7.2.1). Finally, a 100-nm-thick silicon nitride was deposited as passivation layer using PECVD method.

7.2.1 Fabrication of nano T-gate using E-beam lithography and tri-layer resist

In this work, a nano-fabrication technology of the T-shaped gate for the ultrahigh-speed MHEMTs was developed. E-beam lithography using tri-layer resist system was employed to form the expected resist profile for nanometer T-shaped gate formation. High-resolution scanning electron microscope (SEM) was then used to measure the dimension of the footprint. Ultra-short 50-nm T-shaped gate on InP substrate was realized. Fig. 7.2 summarizes the process flow of the fabrication of 50-nm T-shaped gate. First, the tri-layer resist of ZEP-520/PMGI/ZEP-520-12 (150nm/450nm/250nm) was coated on the substrate. The first E-beam exposure for top two layers was used to only define the head (Tee-top) of the T-shaped gate by modulating the exposure doses. After that, the ZEP and PMGI development were executed by using xylene and MF622, respectively. Then, single center exposure with high dose was used to define the footprint of the bottom ZEP-520 layer. The other tri-layer resist of ZEP-520/ PMGI/ FEP-171 (top layer is FEP-171) was also tried to compare with the top-layer ZEP-520-12.

In addition, the samples were descumed using inductively coupled plasma (ICP) in a 1:3 gas mixture of O_2 and Ar for 30 sec. Finally, Ti/Au (100 nm/300 nm) Schottky gate metal layers were sequentially deposited on the substrate by electron gun

evaporation. After lift-off process using ZDMAC solution, the 50-nm T-shaped gate with thickness of about 400 nm was form on the substrate.

Fig. 7.3 shows a cross-sectional SEM image of the profile of ZEP-520/PMGI/ZEP-520-12 (180nm /450nm/240nm) tri-layer resist system after E-beam lithography and development. The desired short foot-print was defined as 50 nm for the bottom ZEP-520. The foot-print was matched with the center Tee-top opening correctly, and the under-cut profile was made for gate-metal lift-off. The Fig. 7.4 shows the cross sectional SEM view of the T-shaped gate. The Ti/Au (100 nm/300 nm) gate metal was deposited by E-gun evaporator and the gate length at the bottom is about 50 nm. The multilayer ZEP-520/PMGI/FEP-171 (top layer is FEP-171) was also tried to compare with the difference of the top-layer ZEP-520-12. The FEP-171 is also an E-beam positive resist for mask process which was made by FUJIFILM Arch Company. There are some problems if the top layer is FEP-171. The T-top opening is too wide and not easy to be controlled. On the other hand, the top FEP-171 was attacked by the xylene development. Therefore, the ZEP-520-12 is a more suitable top layer than FEP-171 for our E-beam lithography process.

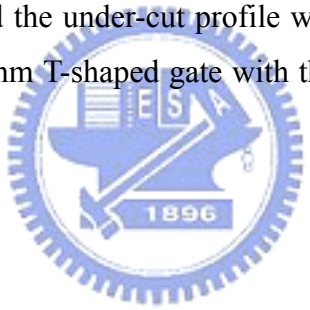
7.2.2 Improvements of resist profile and alignment precision for nano T-shaped gate lithography.

The different doses of E-beam lithography using ZEP-520/PMGI/ZEP-520-12 tri-layer resist system for the T-shaped gate fabrication were tried to obtain the wide Tee-top and short gate length simultaneously. The alignment precision of footprint and Tee-top of the T-shaped gate on device substrate was well improved by scanning the chip mark of every device.

For this experiment, we focus on optimizing the resist profile and the alignment precision of the E-Beam lithography for nano T-shaped gate on InP-based HEMTs. After mesa isolation using wet chemical etching by H_3PO_4: H_2O_2: H_2O= 5:1:40, ohmic contacts were formed by evaporating Au/Ge/Ni/Au metallic layers and then alloyed 300℃ using rapid thermal annealing (RTA). After that, the ZEP-520/PMGI/ZEP-520-12 (150nm/ 450nm/ 250nm) tri-layer resist system was used to form the T-shaped gate by E-Beam lithography. The first E-beam exposure and development for top two layers was used to only define the Tee-top of the T-shaped gate. Then, single center exposure with high dose was used to define the

footprint for the bottom ZEP-520 layer. In order to achieve an optimal resist profile, the dosage of the first E-beam exposure was modulated for the wider Tee-top. Fig. 7.5(a) shows the photo of device pattern after E-Beam lithography. Fig. 7.5(b) shows SEM image for the shifted gate patterns. The alignment precision can be improved by scanning chip mark of every device because of the small dimension of the gate patterns. After the E-beam lithography, the Ti/Pt/Au (80nm/80nm/200nm) gate metal was deposited with e-gun evaporator and lifted-off with ZDMAC. The profile and the gate length of the T-shape gate were observed by scanning electron microscopy (SEM). Fig. 7.6(a) and Fig. 7.6(b) show the ZEP-520/PMGI/ZEP-520-12 tri-layer resist profile after E-Beam lithography. In Fig. 6.6(a), the top opening of ZEP-520-12 is only 200nm. In order to reduce the gate resistance, a wider Tee-top of the T-shaped profile about 450nm was made in Fig. 7.6(b).

Fig. 7.7 shows the T-shaped gate after lift-off process. The width of the Tee-top is 480 nm and the gate length is 50 nm. The foot-print was matched with the center Tee-top opening correctly, and the under-cut profile was made for gate-metal lift-off. The gate resistance of the 50-nm T-shaped gate with the wide Tee-top of 480 nm can be reduced.



7.3 Results and Discussion

Fig. 7.8 shows the current-voltage characteristics of the 2 × 40 μm MHEMT. The fabricated $In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As$ MHEMT shows a maximum drain-source current of 890 mA/mm and transconductance of 827 mS/mm. The high current density was due to the double δ-doping structure which provided higher carrier concentration and superior electron transport properties in the $In_{0.6}Ga_{0.4}As$ channel.

S-parameter measurement was done from 1 – 40 GHz by using a vector network analyzer with an on-wafer configuration. Fig. 7.9 shows the frequency dependence of the current gain (H_{21}) and power gain (*MAG/MSG*) for the 2 × 40 μm MHEMT with gate and drain bias of – 0.6 V and 1.5 V. The f_T and f_{max} of the MHEMT are 200 GHz and 300 GHz, respectively, by extrapolating H_{21} and *MAG/MSG* using least-squares fitting with a –20 dB/decade slop. The H_{21} is 13 dB at 40 GHz and the MAG/MSG is 15 dB at 40 GHz. Fig. 7.10 shows the noise figure (*NF*) of the MHEMT from 1 to 16GHz. The minimum *NF* was below 0.67 dB up to 16 GHz. This superior behavior is attributed to the low access resistance, larger drain current and high transconductance

across a wide range of gate Bias.

Further, the power performance of a 4 × 40 μm gate width device was measured at 32 GHz by load-pull systems for Ka-band application. The measured result is shown in Fig. 7.11, at drain bias of 2.5 V. With the tuner impedance matched for maximum power, the device showed the maximum output power of 14.5 dBm and P1dB of 11.1 dBm with 9.5 dB power gain at 32 GHz. This high power gain is attributed to the high Indium content at the channel and the short gate length. Overall, the MHEMT exhibits comparable RF performances to the InP-based HEMT due to the appropriate epi-structure design and the short gate length.

7.4 Conclusion

The $In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As$ power MHEMT with double δ-doping structure and 70nm T-gate has been designed and fabricated. The MHEMT developed showed excellent DC and RF performances and demonstrated great potential for power applications at Ka-band and millimeter-wave range.

Acknowledgement

A part of this work was supported by "Nanotechnology Support Project" of the Ministry of Education, Culture, Sports, Science and Technology (MEXT), Japan.

FIGURES:

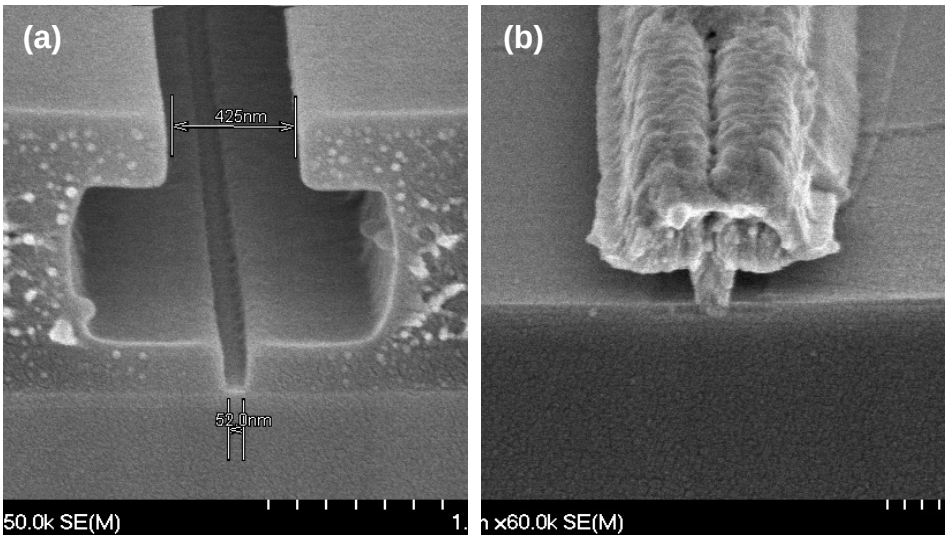


Fig. 7.1 Cross-sectional SEM images of the (a) resist profile and the (b) 70-nm T-gate of the MHEMT.

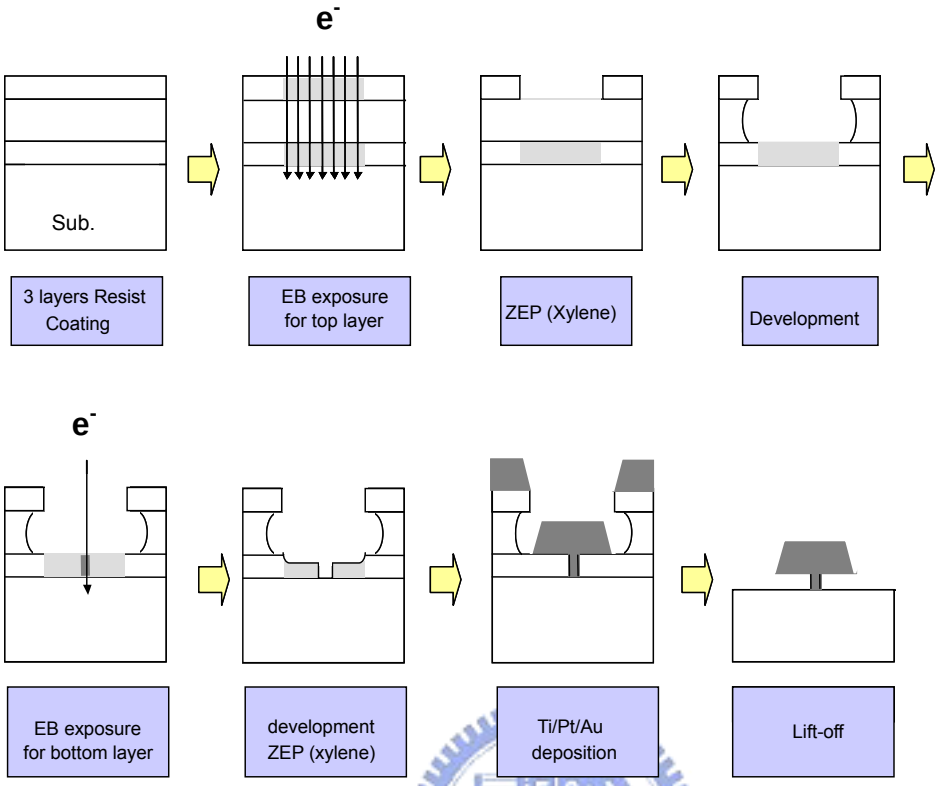


Fig. 7.2 Process flow of fabricating of 50-nm T-shaped gate using E-Beam lithography and tri-layer resist.

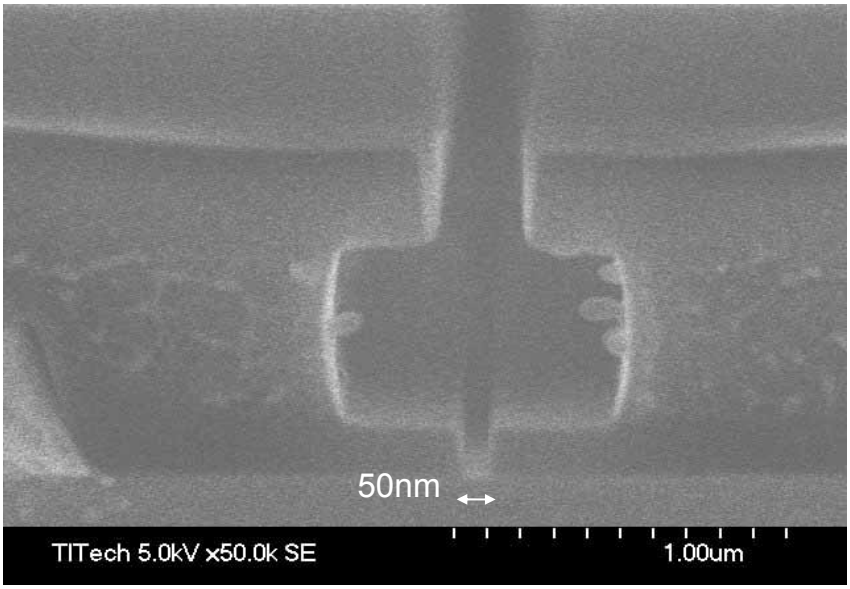


Fig. 7.3 Cross sectional SEM image of the profile of tri-layer resist after E-beam lithography and development.

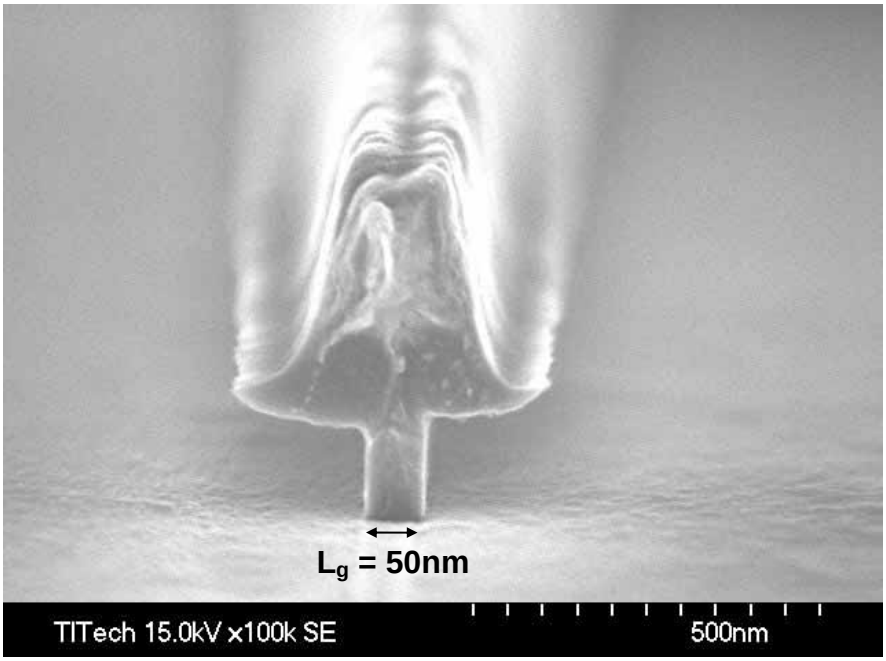


Fig. 7.4 Cross sectional SEM image of the 50-nm Ti/Au (100 nm/300 nm) T-shaped gate on substrate.

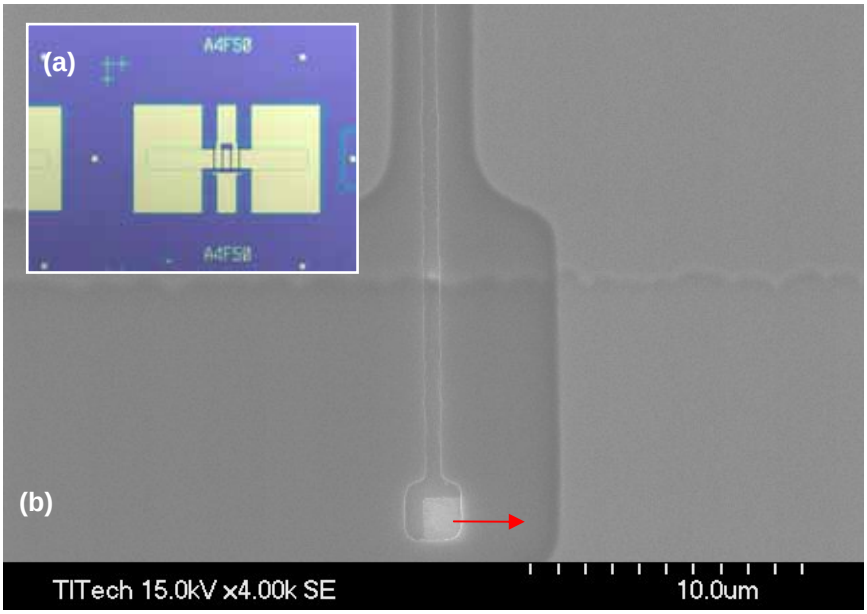


Fig. 7.5 (a) The photo of device pattern after E-Beam lithography. (b) The SEM image for the shifted gate pattern.

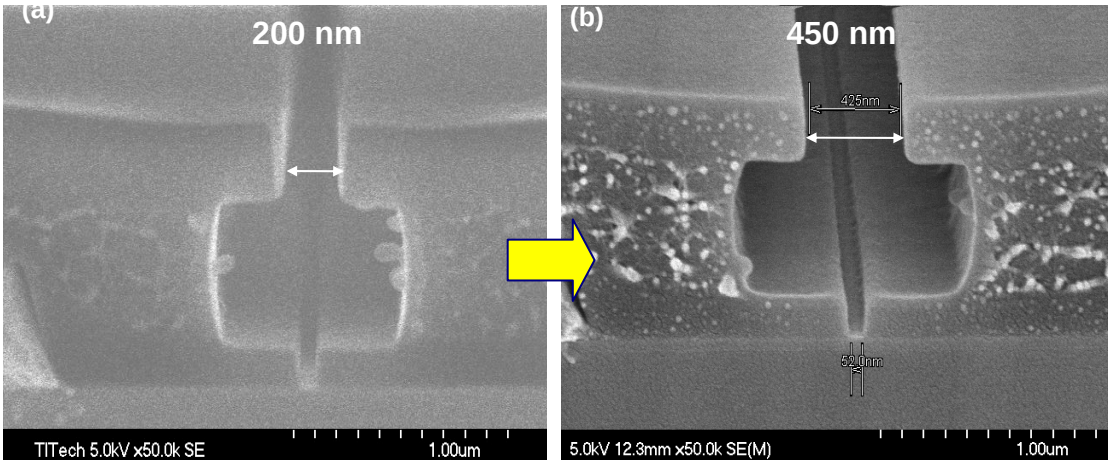


Fig. 7.6 Cross-sectional SEM image of the top opening (a) 200 nm, and (b) 450 nm for the tri-layer resist system.

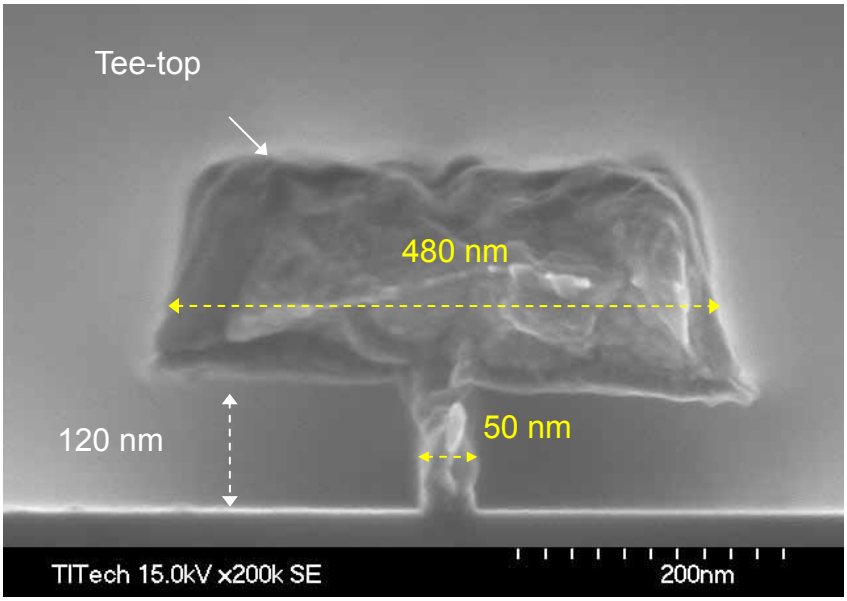


Fig.7.7 Cross-sectional SEM image of the optimal 50-nm T-shaped gate.

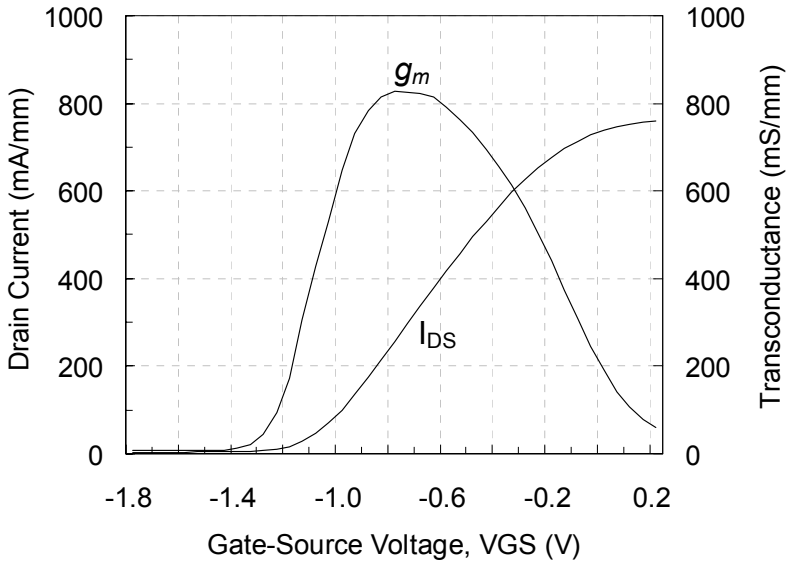


Fig. 7.8 Current-voltage characteristics of the 2 × 40 μm MHEMT.

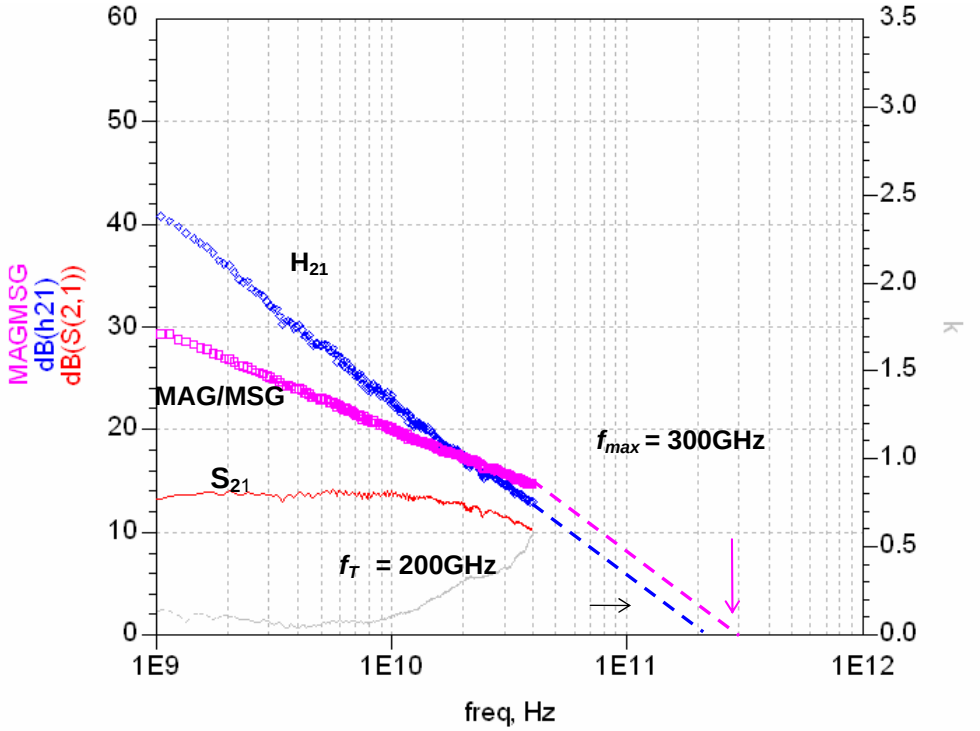


Fig. 7.9 Frequency dependence of the current gain (H_{21}) and *MAG/MSG* of the power MHEMT.

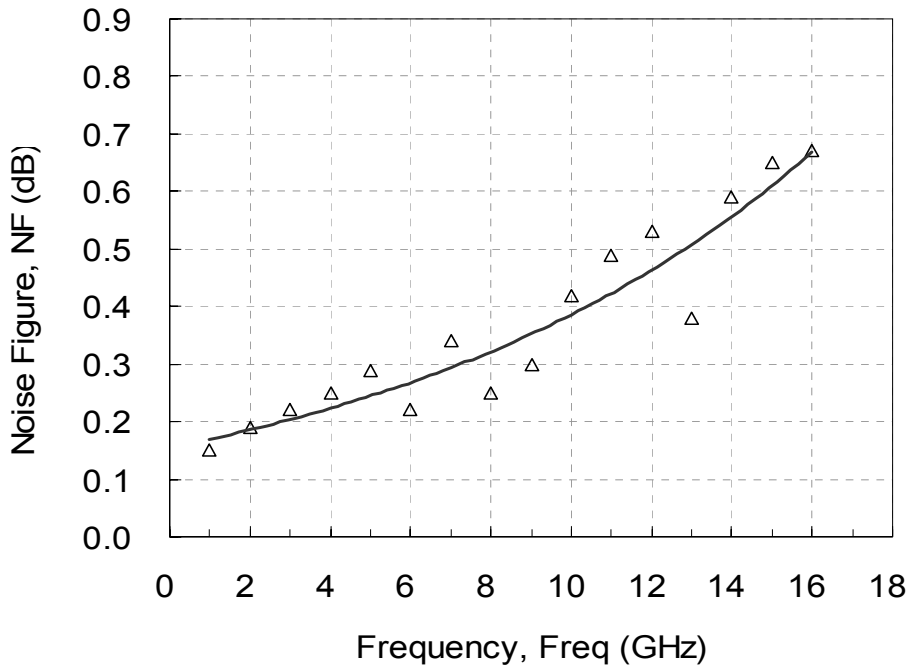


Fig. 7.10 Noise Figure (NF) of the 2 × 40 μm MHEMT measured from 1 to 16 GHz.

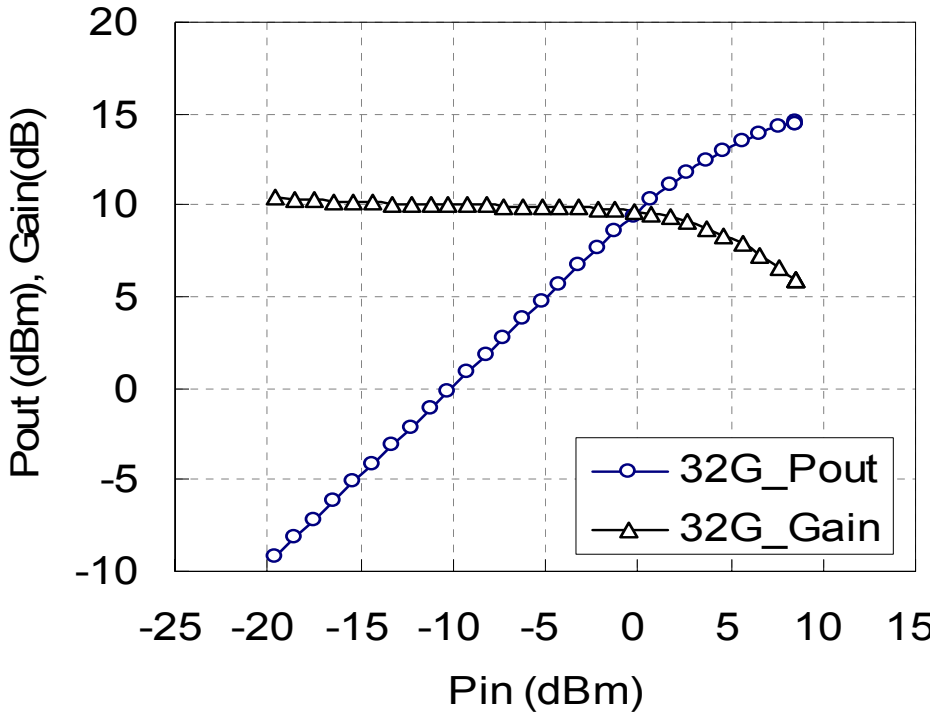


Fig. 7.11 Measured 32-GHz power performance of the 4 × 40 μm power MHEMT at drain bias of 2.5 V.

Chapter 8

Thermal stability of Ti/Pt/Cu Schottky contact on InAlAs layer

8.1 Introduction

Copper metallization has been widely used in silicon integrated circuit industry ever since IBM announced its success in silicon very large scale integration (VLSI) process.[8-1, 8-2] This is because copper has a low bulk resistivity (1.68 μΩ-cm) [8-3] and excellent electromigration resistance.[8-4] However, it is well known that copper diffuses very easily into silicon and silicon oxide at a temperature as low as 200℃ if without any diffusion barrier.[8-5, 8-6] Even though the use of copper as metallization metal has become very popular in Si industry, only a few reports of copper metallization for GaAs devices have been published so far. As in the silicon case, copper also diffuses into GaAs if without any diffusion barrier.[8-7] In recent years, the studies of backside copper metallization of GaAs FETs (field-effect transistor) [8-8] and copper airbridge for low-noise GaAs PHEMT (high-electron mobility transistors) [8-9] have been reported. The use of copper metallization for GaAs devices also requires suitable diffusion barriers which are compatible with the GaAs FET processes to prevent copper inter-diffusion into the underlying semiconductor layers.

Cu-metallized ohmic contact to n-type GaAs using Cu_3Ge [8-10] and non-alloyed ohmic contact to n-type InGaAs using Ti/Pt/Au [8-11, 8-12] have been reported, and the Ti/Pt/Au non-alloyed ohmic contact was demonstrated to have better thermal stability than the conventional eutectic-based AuGeNi contact. On the other hand, the effect of inter-diffusion of the Ti/Pt/Au gate metal on the performance of the GaAs PHEMTs and InGaAs/InAlAs/InP HEMTs has been studied.[8-13, 8-14] In this work, the use of Ti/Pt/Cu as the Schottky contact to InAlAs is studied. The electrical characteristics and thermal stability of the Ti/Pt/Cu Schottky contact are investigated. Platinum is used as the diffusion barrier because it has a high melting point, is compatible with the lift-off process, and is a good diffusion barrier for preventing Au

from diffusing into the conventional Ti/Pt/Au Schottky and ohmic structure.[8-15] By using the new copper Schottky contact structure, it is possible to realize a gold free copper metallized InAlAs/InGaAs HEMT with proper design of the FET process. The use of copper as the metallization metal for high frequency HEMT devices has the following advantages over gold: lower resistivity, higher thermal conductivity, and lower cost. The study of the electrical characteristics and the thermal stability of the Ti/Pt/Cu Schottky contact on i-InAlAs is indispensable for the realization of the gold free fully copper metallized InAlAs/InGaAs based HEMTs and monolithic microwave integrated circuits (MMICs).

8.2 Experimental

The structure of the samples consists of a 30 nm Si-doped n-InGaAs (2×10^{18} cm^{-3}) on top of a 15 nm un-doped InAlAs Schottky layer on the GaAs substrate which is similar to the conventional InAlAs/InGaAs HEMT structure. Rectangular contact pads of AuGeNi metals were evaporated by E-gun evaporation on n-InGaAs and were annealed at 320℃ to form ohmic contacts. The specific contact resistance of the ohmic contacts measured by the transmission line method (TLM) was 8.7×10^{-7} Ω-cm^2. The top n-InGaAs layer was selectively etched over the InAlAs Schottky layer using succinic acid (S.A.) and H_2O_2 mixture. After the etching process, the Ti/Pt/Cu (80/80/200nm) was deposited on the un-doped InAlAs layer to form the Schottky diode. The properties of the Schottky contact are sensitive to the surface condition since InAlAs is quite reactive and tends to be oxided easily, the oxided layer on top of InAlAs should be removed completely before the Schottky metal deposition. Two different surface treatments including dilute HCl (1:10) dipping for 15 sec and N_2 plasma (30 watt) etching for 60 sec before Ti/Pt/Cu deposition were tried. The thermal stability test of the two samples was performed and the Ti/Pt/Cu Schottky characteristics of the samples with different surface pretreatments were compared. In this multilayer Ti/Pt/Cu metal system, Pt is used as the diffusion barrier to prevent the Cu from diffusing into the underlying Ti layer. After Schottky metal evaporation and lift-off, PECVD SiN_x was deposited on the samples at 250℃ for passivation. The nitride via was plasma-etched by CF_4/O_2 gases. The Schottky diodes had a diameter of 200 μm and were annealed at various temperatures for current-voltage (I-V) measurement and material analysis. To investigate the diffusion barrier property of

platinum, the Ti/Pt/Cu multilayer on InAlAs was annealed at various temperatures for 30 min in nitrogen ambient for material analysis. X-ray diffraction (XRD), Auger electron spectroscopy (AES), transmission electron microscopy (TEM), and energy-dispersive X-ray analysis (EDX) were used for the material stability study.

8.3 Results and Discussion

The barrier heights (ψ) and the ideality factors (n) of the Ti/Pt/Cu Schottky contact on InAlAs and the Ti/Pt/Au Schottky contact on InAlAs under various annealing temperatures are summarized in Table 8.1. As shown in Table 8.1, the two samples show similar Schottky characteristics. For the as-deposited Ti/Pt/Cu on InAlAs, the barrier height (ψ) and the ideality factor (n) were 1.01 eV and 1.25, respectively, while they were 1.01 eV and 1.27 for Ti/Pt/Au. Both Ti/Pt/Cu and Ti/Pt/Au exhibited excellent thermal stability up to 350℃ annealing. It means that Ti/Pt/Cu on InAlAs is a good Schottky contact and has comparable electrical performance as the conventional Ti/Pt/Au on InAlAs. The corresponding I-V characteristics of the Ti/Pt/Cu Schottky diodes as a function of the annealing temperature were shown in Fig. 8.1(a). The leakage current density of the as-deposited Ti/Pt/Cu Schottky contact was about 3.83×10^{-7} A/cm^2 at -1 V bias. The leakage current increased to 2×10^{-6} A/cm^2 at -1 V bias after annealing at 200℃ and 300℃. However, the characteristics of the Ti/Pt/Cu on InAlAs Schottky contacts degraded after 400℃ annealing. The Schottky characteristics became ohmic-like behavior when the annealing temperature exceeded 400℃. On the other hand, Fig. 8.1(b) shows the Schottky barrier heights of the samples subjected to two different surface pretreatments before the deposition of the Ti/Pt/Cu multilayer on InAlAs. The two surface treatments were: dilute HCl (1:10) dipping for 15 sec and N_2 plasma with 30 watt etching for 60 sec. In Fig. 8.1(b), the pretreatment using N_2 plasma increased the barrier heights from 1.03 eV to 1.08 eV after 300℃ annealing. The increase of the barrier height after thermal annealing might be due to the defects generated on the InAlAs layer by the ion bombardment caused by the N_2 plasma. The barrier height of the Schottky contact using HCl pretreatment remained stable (1.01 eV) even after 300℃ annealing. As the result, the HCl pretreatment was applied for the Ti/Pt/Cu Schottky contact fabrication and material analysis in this study.

Fig. 8.2 shows the Auger Electron Spectroscopy (AES) depth profiles for the

Ti/Pt/Cu as deposited and after annealing at 350℃ and 400℃, respectively. As can be seen from Fig. 8.2(b), the interface of Ti/Pt/Cu on InAlAs remained sharp after 350℃ annealing, and Cu did not diffuse through Pt into the underlying Ti layer, indicating that the Pt was an effective diffusion barrier even after 350℃ annealing. However, the Cu atoms began to penetrate through Pt layer after 400℃ annealing as shown in Fig. 8.2(c). Moreover, some Cu atoms and accumulated Ti atoms were found at the interface between Ti and InAlAs layers after 400℃ annealing in Fig. 8.2(c). A mechanism proposed in the recent work [8-14] revealed the Ti inter-diffusion and possible formation of $TiAs_x$ in the Ti/InAlAs interface resulted in the degradation of Ti/Pt/Au gate on InAlAs/InGaAs/InP HEMTs structure. This is consistent with the degradation of the Ti/Pt/Cu Schottky characteristics that were found in this study with the barrier height dropped to 0.86 eV and the ideal factor increased to 1.51 after annealing at 400℃ as shown in Table 8.1.

Fig. 8.3(a) and (b) are the Cross-sectional TEM micrographs of the Ti/Pt/Cu on InAlAs layer after 350℃ and 400℃ annealing for 30 min respectively. No significant interface reaction between the Ti/InAlAs and Ti/Pt interfaces was observed in Fig. 8.3(a) which means that the Pt was an effective diffusion barrier after 350℃ annealing. In Fig. 8.3(b), the interface of Cu/Pt was no longer distinguishable after 400℃ annealing for 30 min. A dark area observed at the upper InAlAs layer close to the Ti/InAlAs interface in Fig. 8.3(b) is due to the diffusion of Ti and Cu into Ti/InAlAs interface region as judged from the AES depth profile shown in Fig. 8.2(c). This resulted in the degradation of the Schottky characteristics. Fig. 8.4 shows the XRD results of the Ti/Pt/Cu samples as-deposited and after annealed from 300℃ to 400℃ for 30 min. From the XRD data, the Ti/Pt/Cu on InAlAs structure was quite stable up to 350℃ annealing and the peaks of Cu, Pt, and Ti remained unchanged after 350℃ annealing. However, after 400℃ annealing, Cu started to diffuse through Pt and reacted with the Ti metal. Additional peaks in the XRD pattern emerged after 400℃ annealing, and these peaks were identified as the Cu_4Ti phases. This was further investigated using energy-dispersive X-ray analysis (EDX) in the Ti layer of the InAlAs Ti/Pt/Cu structure. Fig. 8.5(a) and Fig. 8.5(b) show the EDX data of the Ti layer in the InAlAs/Ti/Pt/Cu structure after 30 min annealing of 350℃ and 400℃, respectively. Cu signal appeared only in Fig. 8.5(b) and not in Fig. 8.5(a). The XRD and EDX data indicate that the Pt is a good diffusion barrier for preventing Cu from diffusing into the Ti/Pt/Cu Schottky structure up to 350℃. However, atomic

inter-diffusion occurred after 400℃ annealing. The formation of Cu_4Ti implies that Cu atoms had diffused through the Pt layer and reacted with the Ti layer at 400℃. The results show good consistency with the AES depth profile and the TEM data in Fig. 8.2 and Fig. 8.3.

8.4 Conclusion

The Schottky behaviors of the Ti/Pt/Cu Schottky contact on InAlAs were investigated at various annealing temperatures. Excellent electrical characteristics of the Ti/Pt/Cu Schottky contact on InAlAs were observed with the ideality factor and the barrier height of 1.25 and 1.01 eV respectively, and the data remained almost the same after 350℃ annealing for 30 minutes. The material analysis showed that no interfacial phase was formed after the thermal treatment at 350℃ for 30 minutes and that Pt had successfully blocked the Cu diffusion into the underlying layers. After 400℃ annealing, the TEM images and the EDX data both show the Cu began to penetrate through the diffusion barrier and formed intermetallic compound of Cu_4Ti. Meanwhile the diffusion of Ti and Cu into Ti/InAlAs interface region was observed in AES depth profile, which was responsible for the rise of the ideal factor and the lowering of the effective barrier height. The results show that Ti/Pt/Cu Schottky contact to InAlAs is very stable up to 350℃ annealing and that the Cu-metallized interconnect using Pt as the diffusion barrier can be integrated into the front-side metallization process for the InAlAs/InGaAs based HEMTs and MMICs.

FIGURES

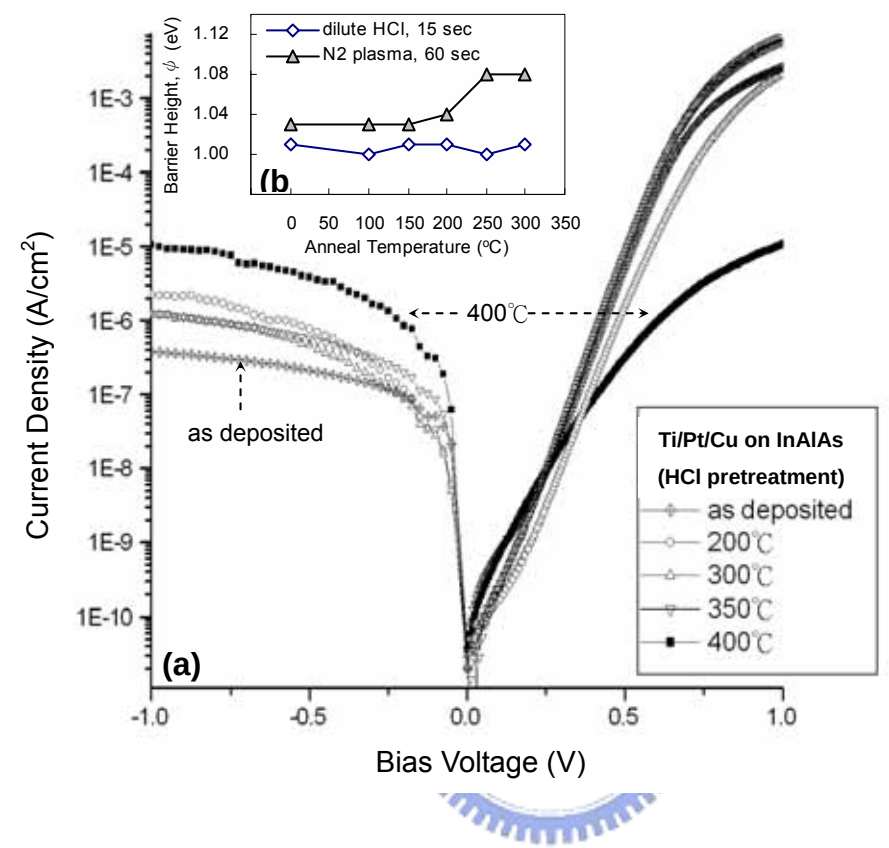


Fig. 8.1. (a) I-V characteristics of the i-InAlAs/Ti/Pt/Cu Schottky diodes using HCl pretreatment with various annealing temperatures for 120 seconds, (b) Barrier height vs. annealing temperature for the diodes with two different surface pretreatments.

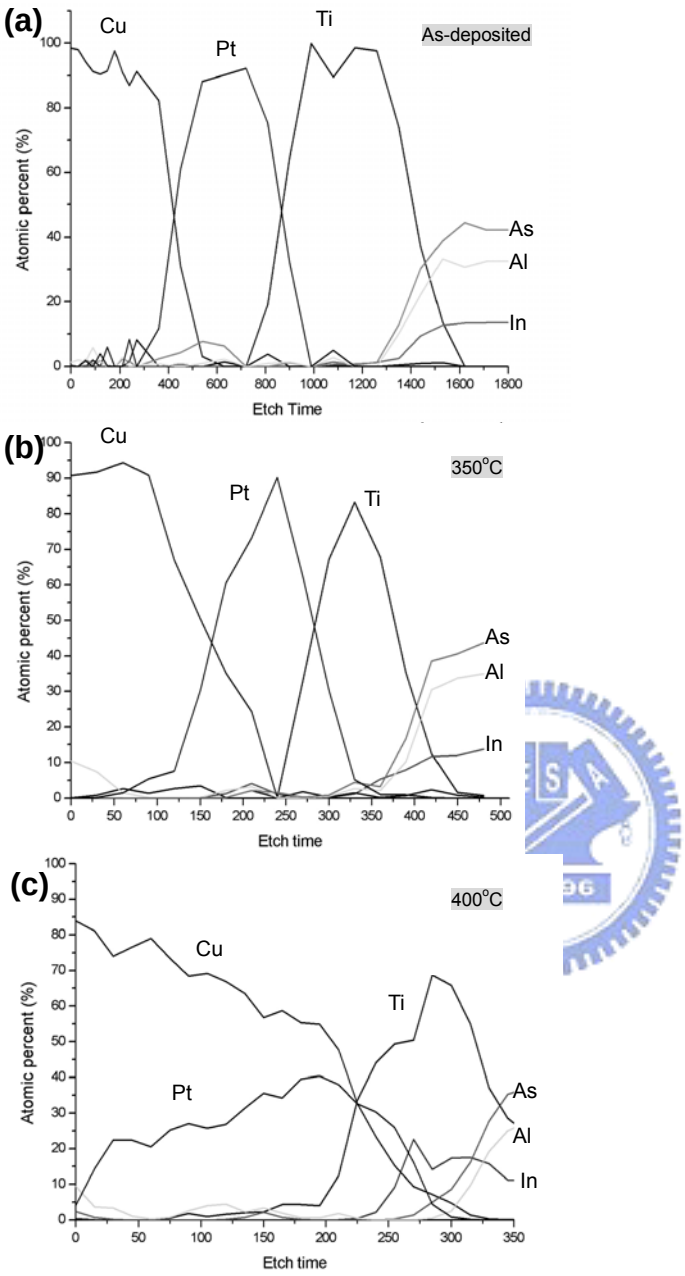


Fig. 8.2. Auger depth profiles of the Ti/Pt/Cu on InAlAs (a) as deposited, (b) after annealing at 350℃ for 30 minutes, and (c) after annealing at 400℃ for 30 minutes.

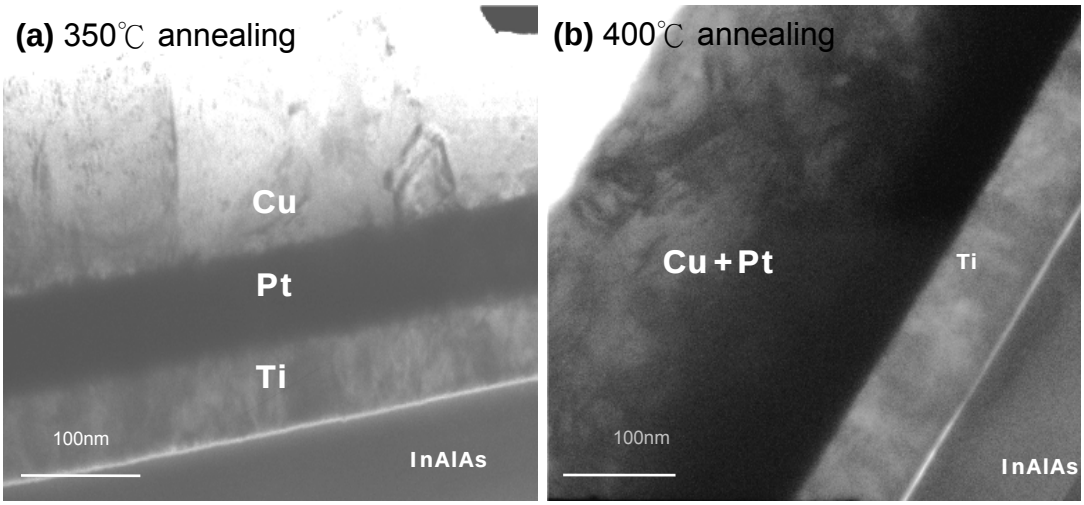


Fig. 8.3. Cross-sectional TEM micrographs of the Ti/Pt/Cu on InAlAs layer (a) after 350℃ annealing for 30 minutes, and (b) after 400℃ annealing for 30 minutes.

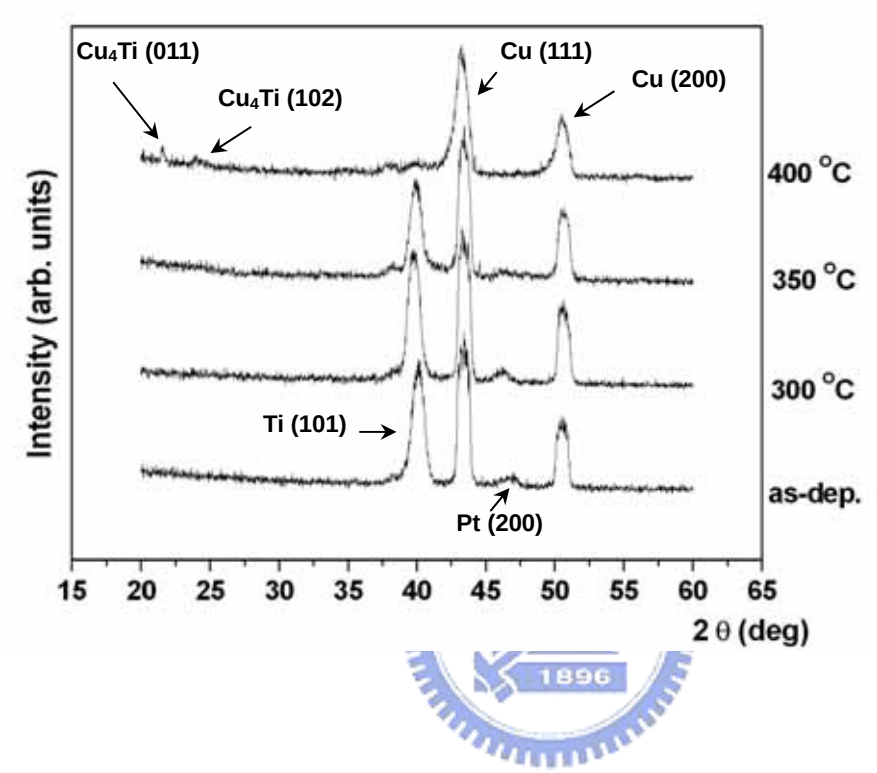


Fig. 8.4. XRD results of Ti/Pt/Cu on InAlAs with various annealing temperatures for 30 minutes.

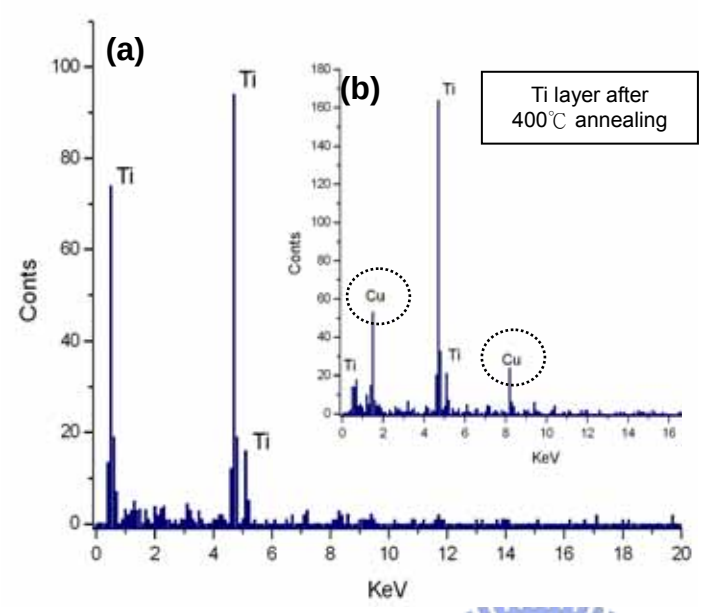


Fig. 8.5. EDX of the Ti layer of the InAlAsTi/Pt/Cu structure after annealed at (c) 350℃ (d) 400℃ for 30 minutes.

Table 8.1. Barrier heights (ψ) and the ideality factors (n) of the Ti/Pt/Cu Schottky contact on InAlAs and the Ti/Pt/Au Schottky contact on InAlAs under various annealing temperatures.

Temp.	**Ti/Pt/Au on InAlAs**		**Ti/Pt/Cu on InAlAs**	
	n	ψ(eV)	*n*	ψ(eV)
As-deposited	1.27	1.01	1.25	1.01
200℃	1.27	1.00	1.25	1.02
300℃	1.26	1.01	1.26	1.01
350℃	1.27	0.99	1.28	0.99
400℃	1.45	0.87	1.51	0.86

Chapter 9

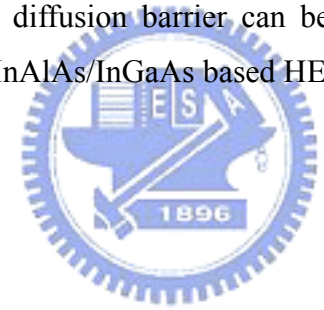
Conclusion

In this dissertation, the performance of the MHEMTs was improved by optimizing the device structure and reducing the gate length using several novel gate-shrinking techniques. A 0.15-μm Γ-shaped gate $In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As$ MHEMT fabricated on GaAs substrate using deep UV lithography and a tilt dry-etching technique is demonstrated for the first time in this work. The developed technology is simple, low-cost and flexible for the submicron Γ-shaped gate fabrication. The 100-μm-wide MHEMT with 0.15-μm Γ-shaped gate fabricated with dry-etching tilt angle of 32° shows an I_{dss} of 680 mA/mm and g_m of 728 mS/mm. The MHEMT also exhibits a f_T of 130 GHz and a f_{max} up to 180 GHz. In addition, a thermal reflow process for E-beam bi-layer resist to achieve 0.1μm T-gate formation was successful developed and applied to the MHEMT fabrication. The 0.1 × 160 μm^2 MHEMT fabricated demonstrated a cut-off frequency f_T of 154 GHz and a maximum frequency f_{max} up to 300GHz, the noise figure of the fabricated MHEMT was less than 1 dB with 14 dB associated gain at 18 GHz. The excellent device performance of the MHEMT manufactured demonstrated that the reflowed T-gate process is compatible with the MHEMT process and can be practically used for the MHEMT manufacturing.

Under 100-nm scale, a sidewall process for E-beam lithography to achieve 90nm T-gate formation was successful developed and applied to the MHEMT fabrication. The 160μm-width MHEMT exhibited a f_T of 130GHz and a f_{max} over than 200GHz, the *NF* of the fabricated MHEMT was 0.69dB with 9.77dB associated gain at 16GHz. Moreover, the $In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As$ power MHEMT with double δ-doping structure and 70nm T-gate has been designed and fabricated. The device has a high transconductance of 827 mS/mm, high saturated drain-source current of 890 mA/mm, high f_T of 200 GHz, and a high f_{max} of 300 GHz were achieved due to the nanometer gate length and the high Indium content in the channel. The MHEMT developed showed excellent DC and RF performances and demonstrated great potential for

power applications at Ka-band and millimeter-wave range.

In addition, the Schottky behaviors of the Ti/Pt/Cu Schottky contact on InAlAs were investigated at various annealing temperatures. Excellent electrical characteristics of the Ti/Pt/Cu Schottky contact on InAlAs were observed with the ideality factor and the barrier height of 1.25 and 1.01 eV respectively, and the data remained almost the same after 350℃ annealing for 30 minutes. The material analysis showed that no interfacial phase was formed after the thermal treatment at 350℃ for 30 minutes and that Pt had successfully blocked the Cu diffusion into the underlying layers. After 400℃ annealing, the TEM images and the EDX data both show the Cu began to penetrate through the diffusion barrier and formed intermetallic compound of Cu_4Ti. The diffusion of Ti and Cu into Ti/InAlAs interface region was also observed in AES depth profile, which was responsible for the rise of the ideal factor and the lowering of the effective barrier height. The results show that Ti/Pt/Cu Schottky contact to InAlAs is very stable up to 350℃ annealing and that the Cu-metallized interconnect using Pt as the diffusion barrier can be integrated into the front-side metallization process for the InAlAs/InGaAs based HEMTs and MMICs.



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